



# AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH

## Faculty of Engineering

### Lab Report Cover Page

Assignment Title:	Studying different digital logic gates and designing of basic logic gates using Universal gates		
Assignment No:	01	Date of Submission:	27 September 2022
Course Title:	DIGITAL LOGIC AND CIRCUITS LAB		
Course Code:	00868	Section:	N
Semester:	Fall 2022-23	Course Teacher:	RETHWAN FAIZ

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2	ABDULLAH AL MAHMUD	19-39500-1	BSc [CSE]
3	MD. OLI ULLAH RAFI	20-42934-1	BSc [CSE]
4	PARTHA MALAKAR	20-42908-1	BSc [CSE]
5	MD. ATIKUR RAHMAN ATIK	19-40033-1	BSc [CSE]

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	Total Marks	

7/4.5

28/9/22



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3	MD. OLI ULLAH RAFI	20-42934-1	BSc [CSE]
4	PARTHA MALAKAR	20-42908-1	BSc [CSE]
5	MD. ATIKUR RAHMAN ATIK	19-40033-1	BSc [CSE]

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FACULTY COMMENTS:	Marks Obtained	
	Total Marks	

## **Abstract:**

To learn about different logic gate and how to implement them using training board and digital integrated circuits.

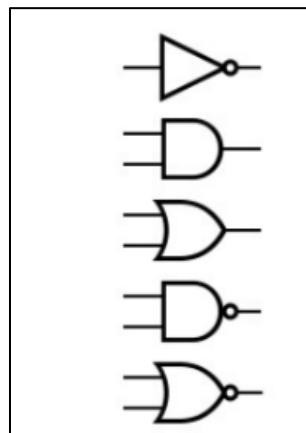
## **Introduction:**

Logic gates are used in electronic devices to perform logical operations. There are seven basic logic gates and two universal logic gates. In this lab the goal is to understand the gates and to implement all the basic gates with universal gates.

## **Theory and Methodology:**

Logic gate implements a Boolean function, which is a logical operation on one or more binary inputs that results in a single binary output. Transistors, diodes, and resistors can all be used to create logic gates. Commonly, resistors are utilized as pull-up or pull-down resistors. When there are any unconnected logic gate inputs that need to be connected to a logic level 1 or 0, pull-up and pull-down resistors are utilized. This stops any erroneous gate switching. Pull-down resistors are wired to ground (0 V), and pull-up resistors are wired to Vcc (+5V) [1].

Basic logic gates are usually NOT, AND, OR, NAND and NOR gates [2] [Figure 1].



*Figure 1 Common symbols of logic gates.*

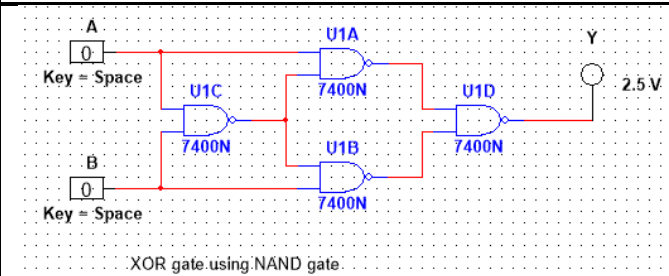
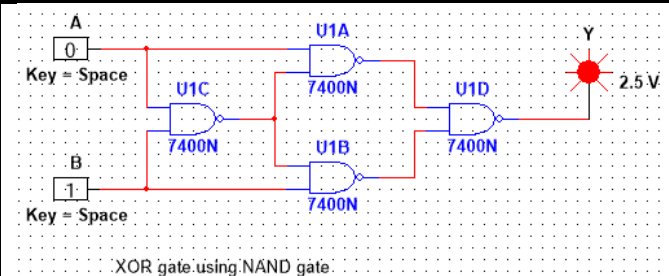
The reason the AND gate is thus named is because it behaves just like the logical "and" operator if 0 is labelled "false" and 1 is labelled "true." The OR gate takes its name from the way it functions, which is like the inclusive "or" in logic. If one or both of the inputs are "true," the result will also be "true." The output is "false" if both inputs are "false." In other words, at least one OR both of the inputs must be 1 for the output to be 1. Logical inverter has a single input and is occasionally referred to as a NOT gate to distinguish it from other kinds of electronic inverter devices. The NAND gate functions as a pair of AND gates and NOT gates. An inverter comes after the NOR gate, which is a combination OR gate [3].

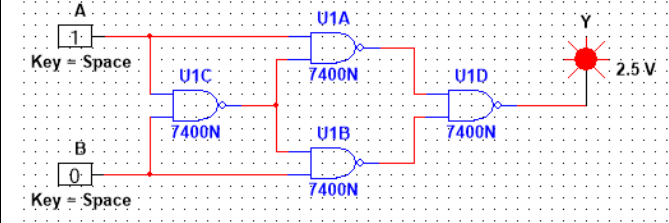
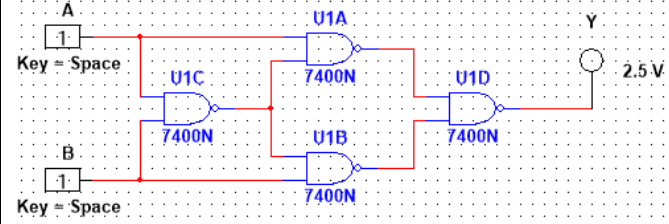
## **Simulation:**

All the simulation are done using NI Multisim.

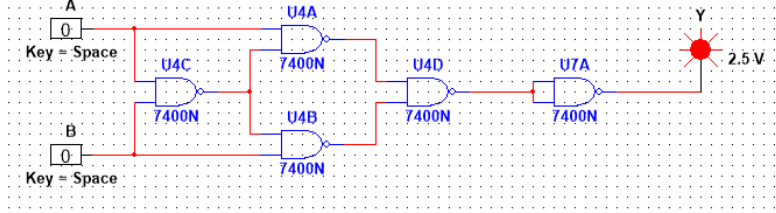
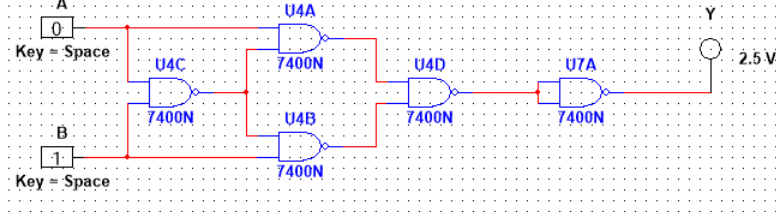
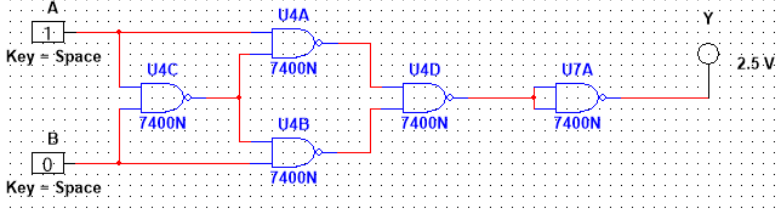
**1. Construct an X-OR and X-NOR gate in your trainer board by using NAND gates only. Use required IC to construct the circuit.**

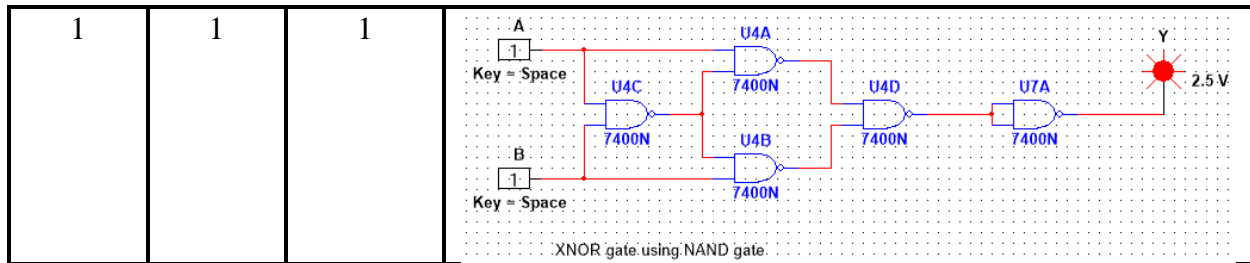
**X-OR gate using NAND gate:**

Input A	Input B	Output Y	Simulation
0	0	0	 <p>XOR gate using NAND gate.</p>
0	1	1	 <p>XOR gate using NAND gate.</p>

1	0	1	 <p>XOR gate using NAND gate.</p>
1	1	0	 <p>XOR gate using NAND gate.</p>

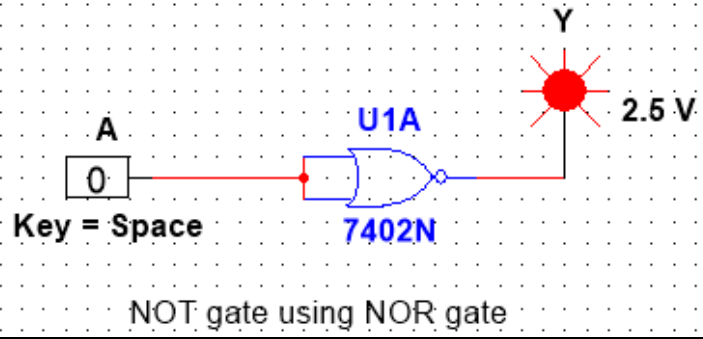
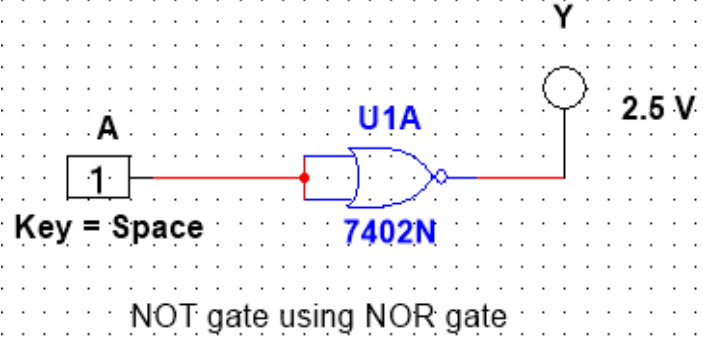
### X-NOR gate using NAND gate:

Input A	Input B	Output Y	Simulation
0	0	1	 <p>XNOR gate using NAND gate.</p>
0	1	0	 <p>XNOR gate using NAND gate.</p>
1	0	0	 <p>XNOR gate using NAND gate.</p>

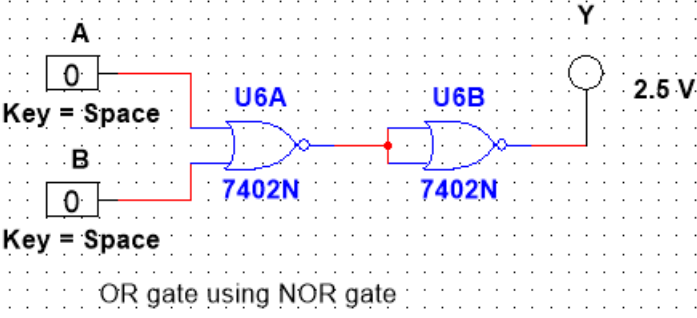
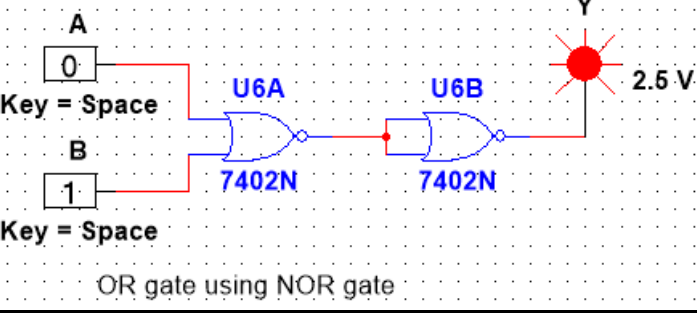
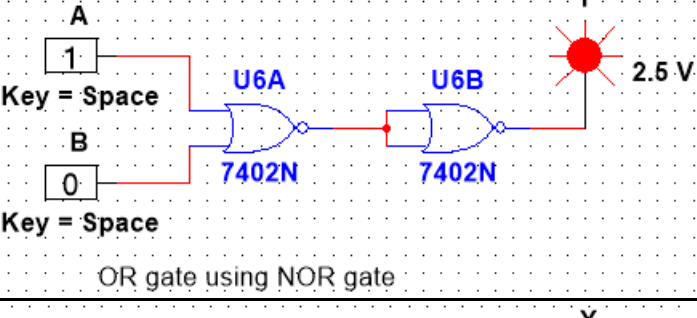
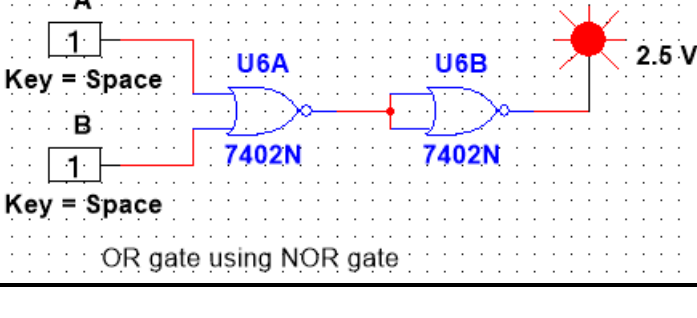


2. Find out the equivalent NOT, OR and AND gate by using NOR gates only. Now construct an X-OR and X-NOR gate in your trainer board by using NOR gates only. Use required IC to construct the circuit.

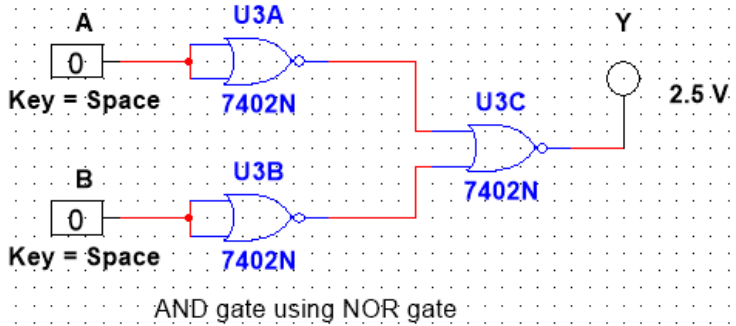
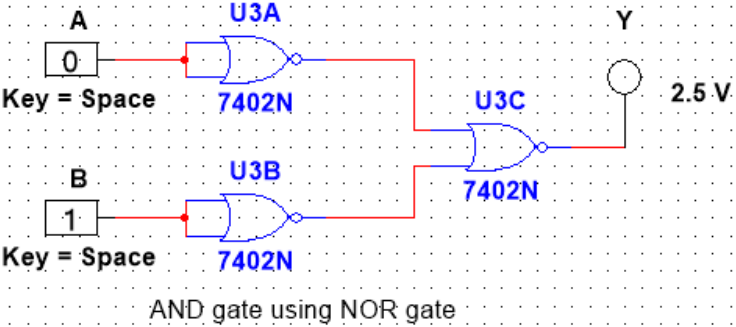
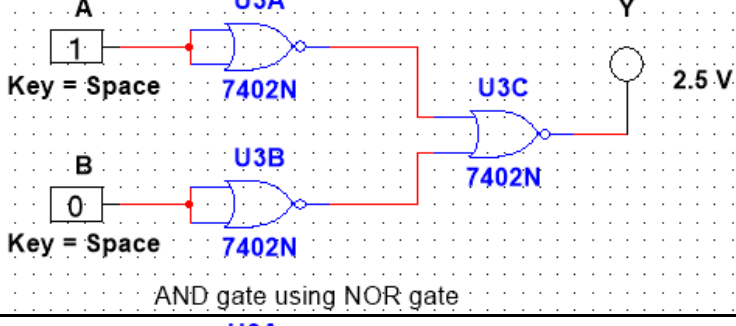
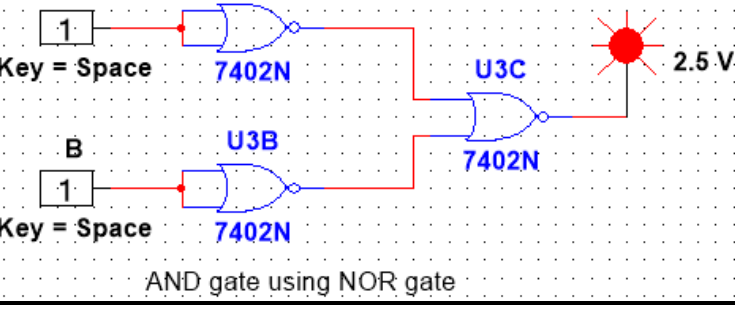
NOT gate using NOR gate:

Input A	Output Y	Simulation
0	1	 <p style="text-align: center;">NOT gate using NOR gate</p>
1	0	 <p style="text-align: center;">NOT gate using NOR gate</p>

### OR gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	0	 <p>OR gate using NOR gate</p>
0	1	1	 <p>OR gate using NOR gate</p>
1	0	1	 <p>OR gate using NOR gate</p>
1	1	1	 <p>OR gate using NOR gate</p>

### AND gate using NOR gate:

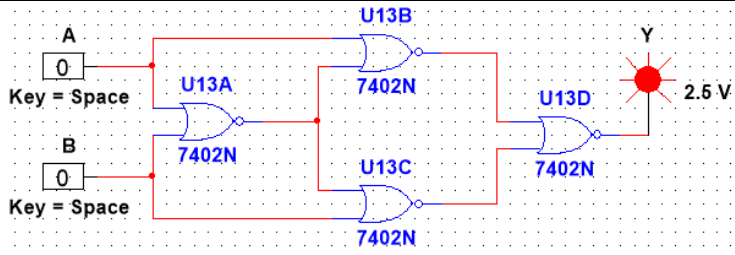
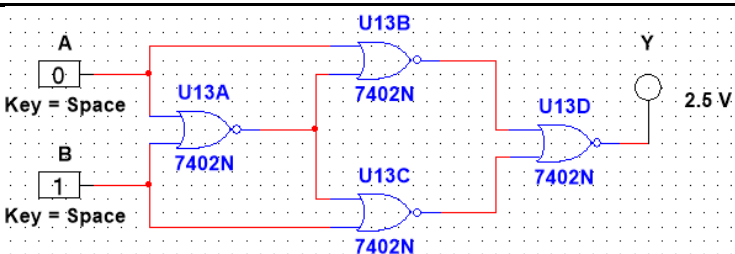
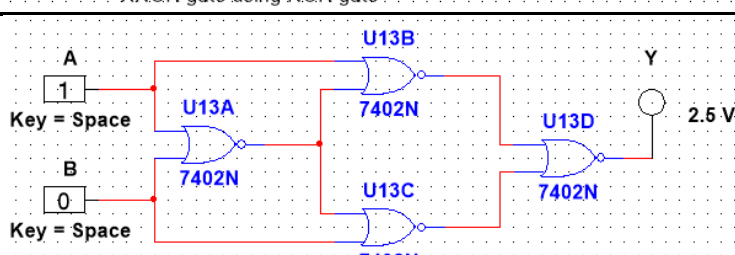
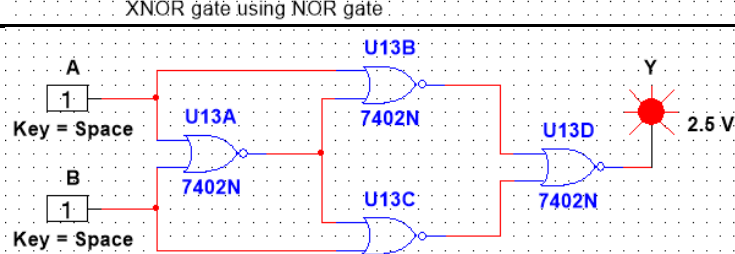
Input A	Input B	Output Y	Simulation
0	0	0	 <p>AND gate using NOR gate</p>
0	1	0	 <p>AND gate using NOR gate</p>
1	0	0	 <p>AND gate using NOR gate</p>
1	1	1	 <p>AND gate using NOR gate</p>



**X-OR gate using NOR gate:**

Input A	Input B	Output Y	Simulation
0	0	0	<p>The diagram shows a circuit with two inputs, A and B, both set to 0. Input A is connected to a switch labeled 'Key = Space'. Input B is also connected to a switch labeled 'Key = Space'. The circuit consists of four NOR gates (U9A, U9B, U9C, U9D) and one output gate (U12A). The inputs are connected to U9A and U9B. The outputs of U9A and U9B are connected to U9C and U9D. The outputs of U9C and U9D are connected to U12A, which produces the output Y. The output Y is 0.</p> <p>XOR gate using NOR gate</p>
0	1	1	<p>The diagram shows a circuit with two inputs, A and B. Input A is set to 0 and input B is set to 1. The circuit consists of four NOR gates (U9A, U9B, U9C, U9D) and one output gate (U12A). The inputs are connected to U9A and U9B. The outputs of U9A and U9B are connected to U9C and U9D. The outputs of U9C and U9D are connected to U12A, which produces the output Y. The output Y is 1.</p> <p>XOR gate using NOR gate</p>
1	0	1	<p>The diagram shows a circuit with two inputs, A and B. Input A is set to 1 and input B is set to 0. The circuit consists of four NOR gates (U9A, U9B, U9C, U9D) and one output gate (U12A). The inputs are connected to U9A and U9B. The outputs of U9A and U9B are connected to U9C and U9D. The outputs of U9C and U9D are connected to U12A, which produces the output Y. The output Y is 1.</p> <p>XOR gate using NOR gate</p>
1	1	0	<p>The diagram shows a circuit with two inputs, A and B, both set to 1. The circuit consists of four NOR gates (U9A, U9B, U9C, U9D) and one output gate (U12A). The inputs are connected to U9A and U9B. The outputs of U9A and U9B are connected to U9C and U9D. The outputs of U9C and U9D are connected to U12A, which produces the output Y. The output Y is 0.</p> <p>XOR gate using NOR gate</p>

### X-NOR gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	1	 <p>Key = Space</p> <p>XNOR gate using NOR gate</p>
0	1	0	 <p>Key = Space</p> <p>XNOR gate using NOR gate</p>
1	0	0	 <p>Key = Space</p> <p>XNOR gate using NOR gate</p>
1	1	1	 <p>Key = Space</p> <p>XNOR gate using NOR gate</p>

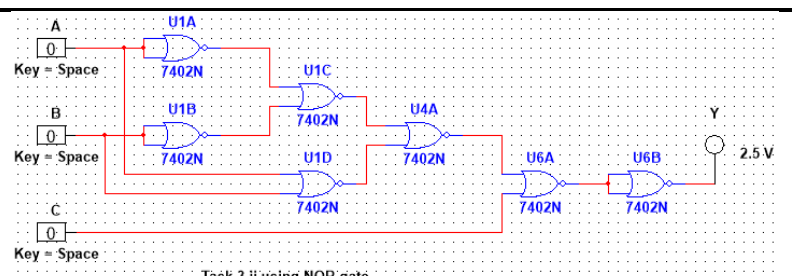
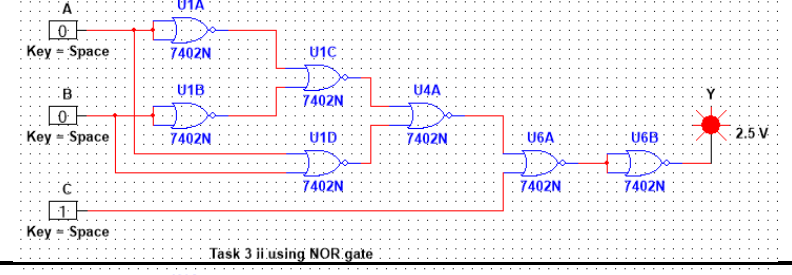
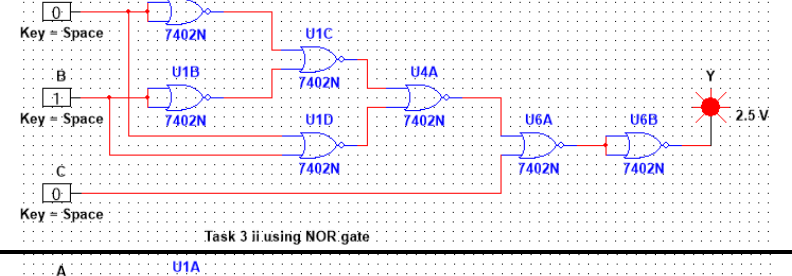
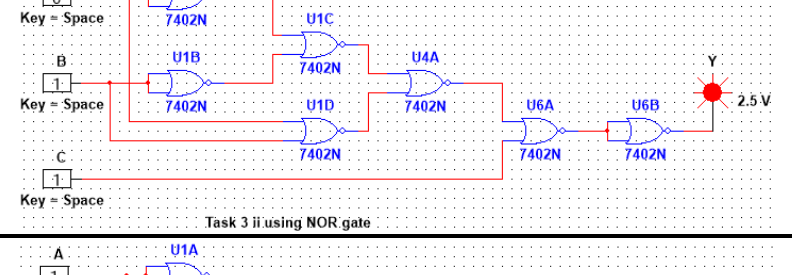
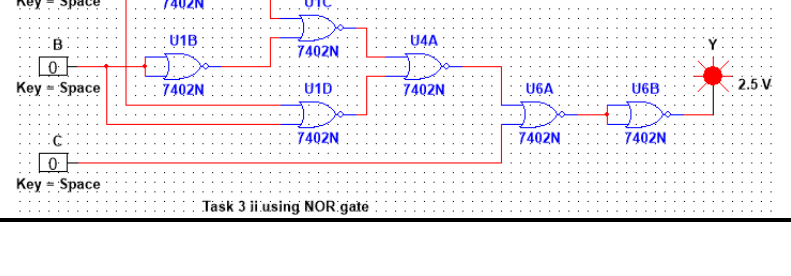
3. Convert the following expressions using universal gates and implement them in the trainer board. Compare the results with the truth table of the equations.

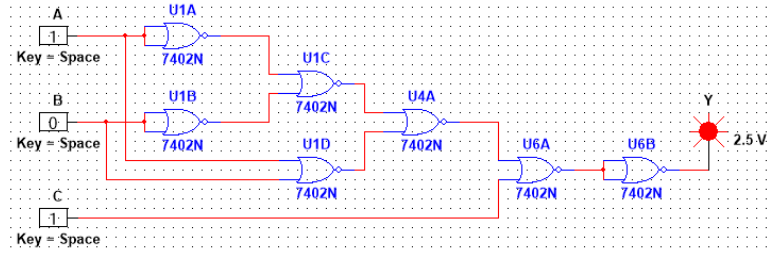
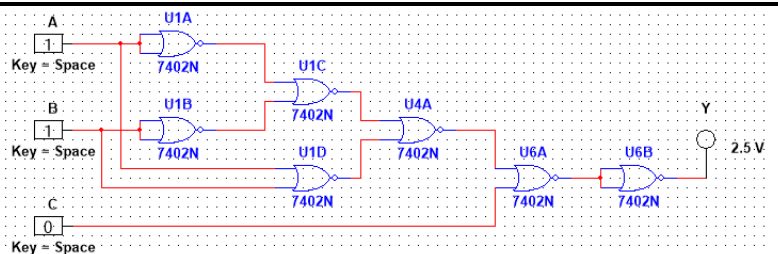
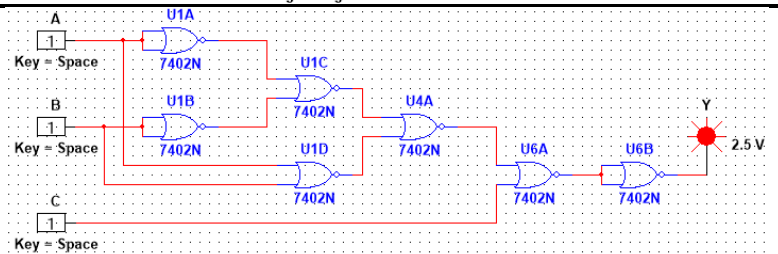
- $A (+) B$
- $(A(+)B) + C$
- $(AB + CD)'$

## Implementation of A (+) B

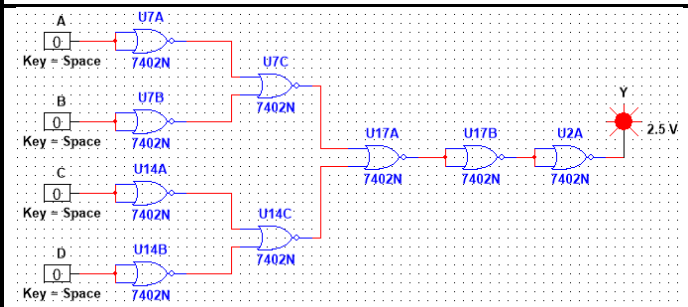
Input A	Input B	Output Y	Simulation
0	0	0	<p>XOR gate using NOR gate</p>
0	1	1	<p>XOR gate using NOR gate</p>
1	0	1	<p>XOR gate using NOR gate</p>
1	1	0	<p>XOR gate using NOR gate</p>

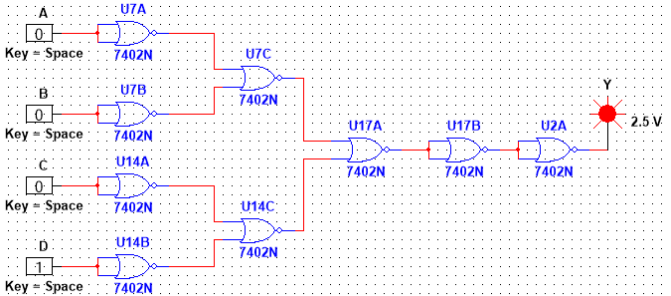
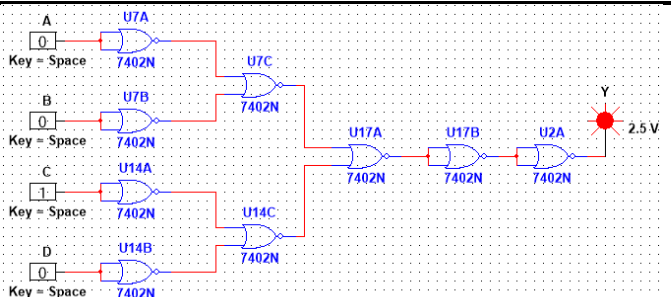
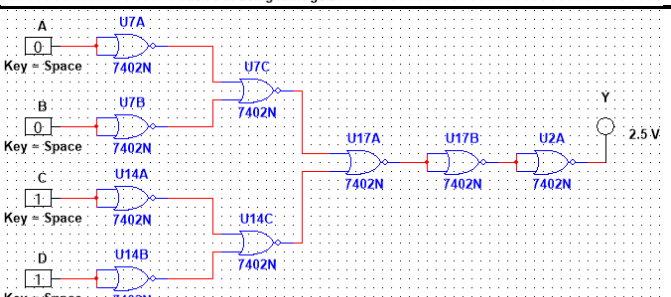
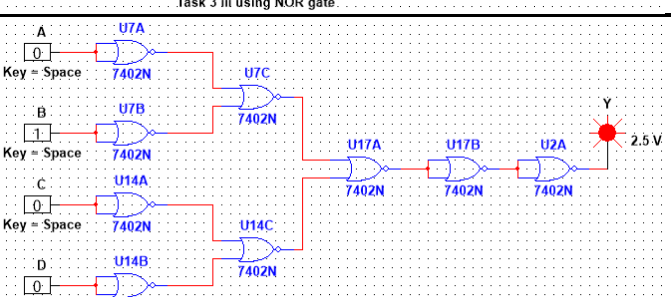
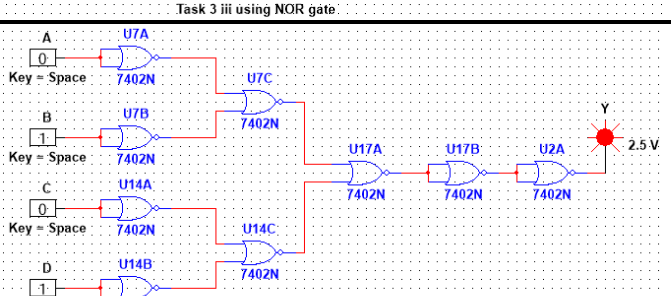
## Implementation of $(A+B)+C$

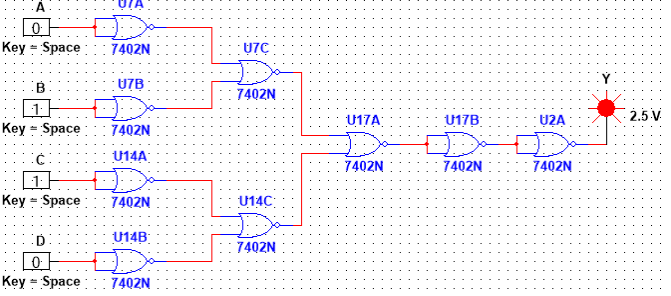
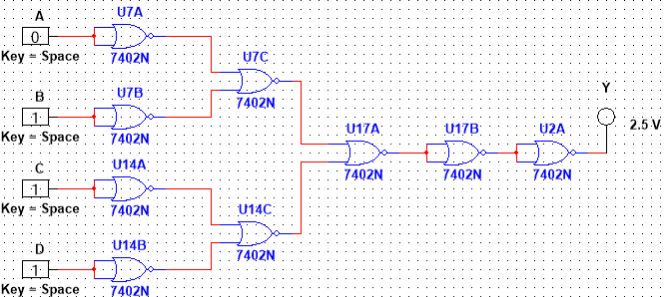
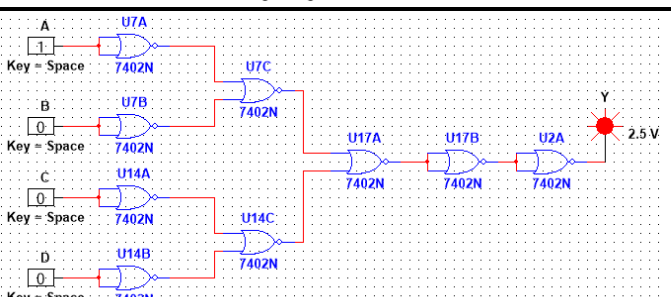
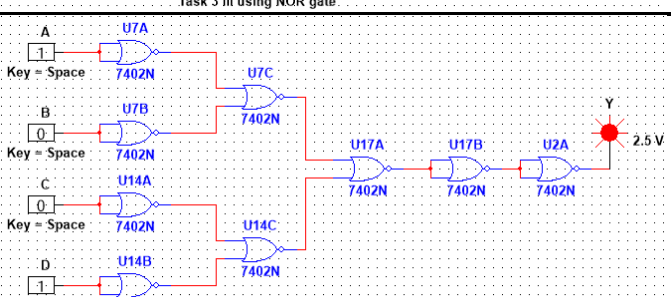
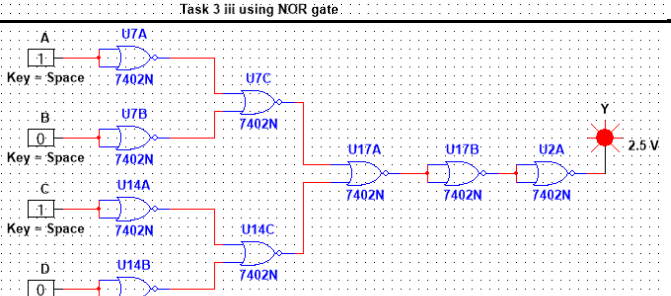
Input A	Input B	Input C	Output Y	Simulation
0	0	0	0	 <p>Task 3 ii using NOR gate</p>
0	0	1	1	 <p>Task 3 ii using NOR gate</p>
0	1	0	1	 <p>Task 3 ii using NOR gate</p>
0	1	1	1	 <p>Task 3 ii using NOR gate</p>
1	0	0	1	 <p>Task 3 ii using NOR gate</p>

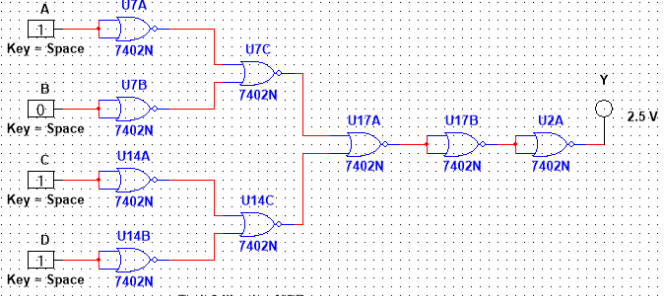
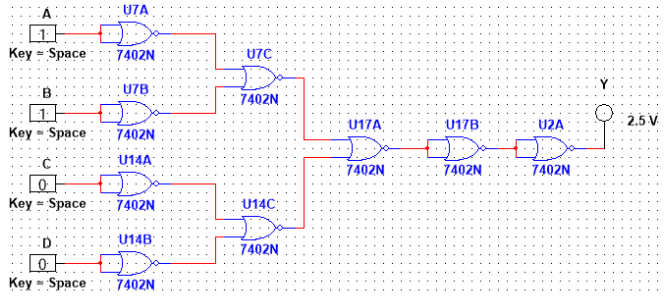
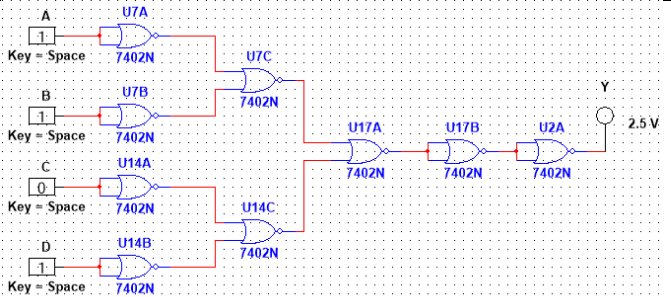
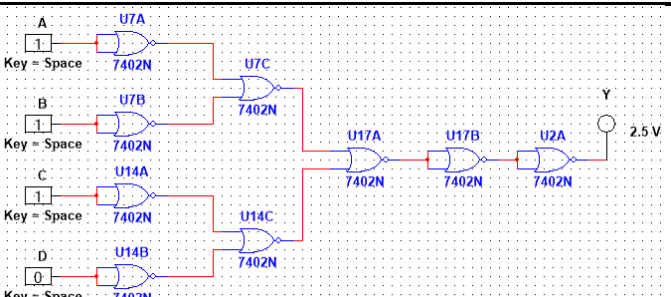
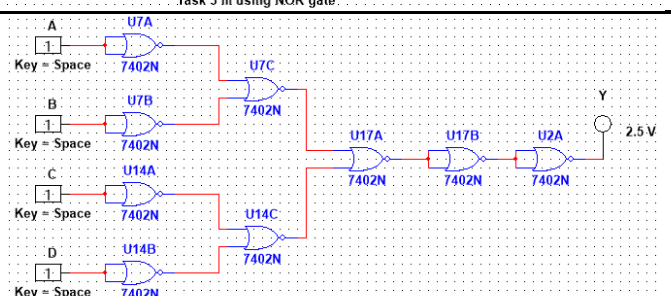
1	0	1	1	 <p>Task 3 ii using NOR gate</p>
1	1	0	0	 <p>Task 3 ii using NOR gate</p>
1	1	1	1	 <p>Task 3 ii using NOR gate</p>

**Implementation of  $(AB + CD)'$**

Input A	Input B	Input C	Input D	Output Y	Simulation
0	0	0	0	1	 <p>Task 3 iii using NOR gate</p>

0	0	0	1	1	 <p>Task 3 iii using NOR gate.</p>
0	0	1	0	1	 <p>Task 3 iii using NOR gate.</p>
0	0	1	1	0	 <p>Task 3 iii using NOR gate.</p>
0	1	0	0	1	 <p>Task 3 iii using NOR gate.</p>
0	1	0	1	1	 <p>Task 3 iii using NOR gate.</p>

0	1	1	0	1	 <p>Task 3 iii using NOR gate.</p>
0	1	1	1	0	 <p>Task 3 iii using NOR gate.</p>
1	0	0	0	1	 <p>Task 3 iii using NOR gate.</p>
1	0	0	1	1	 <p>Task 3 iii using NOR gate.</p>
1	0	1	0	1	 <p>Task 3 iii using NOR gate.</p>

1	0	1	1	0	 <p>Task 3 iii using NOR gate.</p>
1	1	0	0	0	 <p>Task 3 iii using NOR gate.</p>
1	1	0	1	0	 <p>Task 3 iii using NOR gate.</p>
1	1	1	0	0	 <p>Task 3 iii using NOR gate.</p>
1	1	1	1		 <p>Task 3 iii using NOR gate.</p>

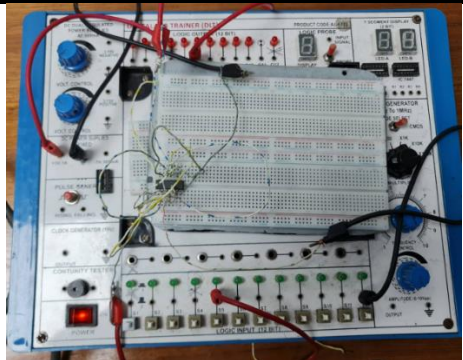
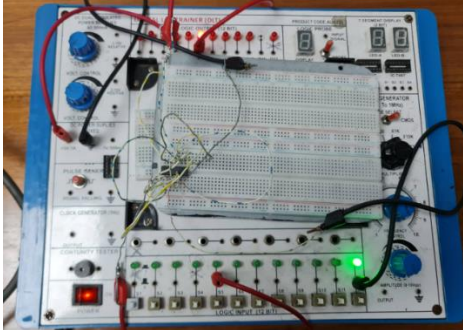
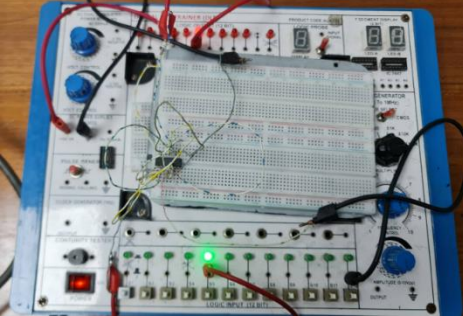


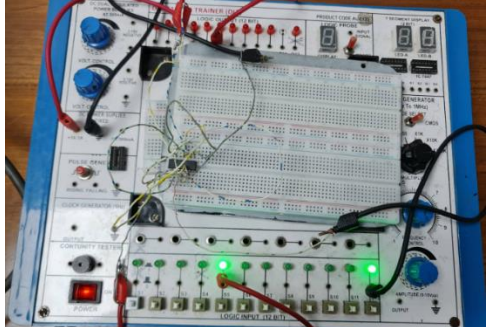
## Experiment

Experiments are done in lab using training board and different ICs.

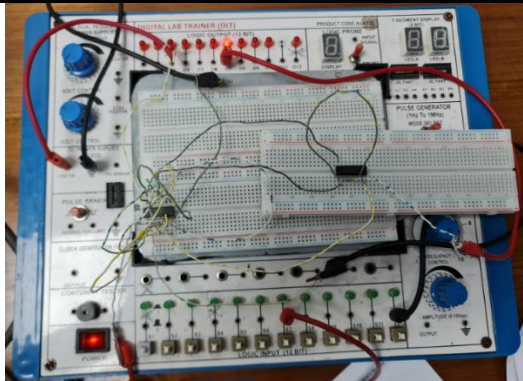
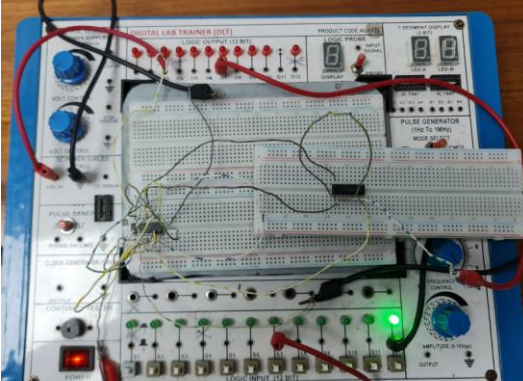
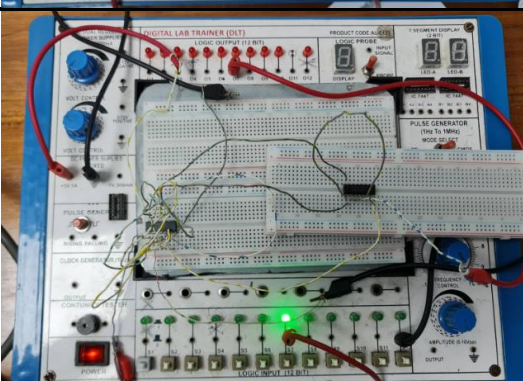
1. Construct an X-OR and X-NOR gate in your trainer board by using NAND gates only. Use required IC to construct the circuit.

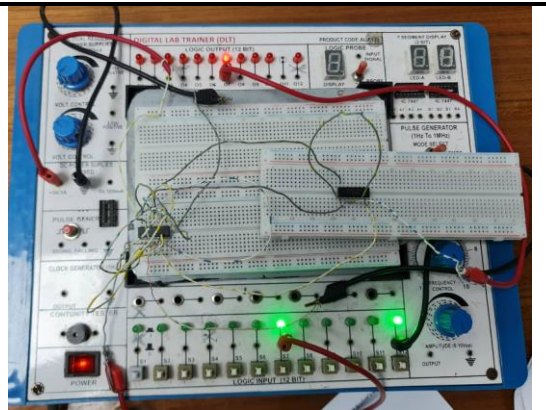
**X-OR gate using NAND gate:**

Input A	Input B	Output Y	Experiment
0	0	0	
0	1	1	
1	0	1	

1	1	0	
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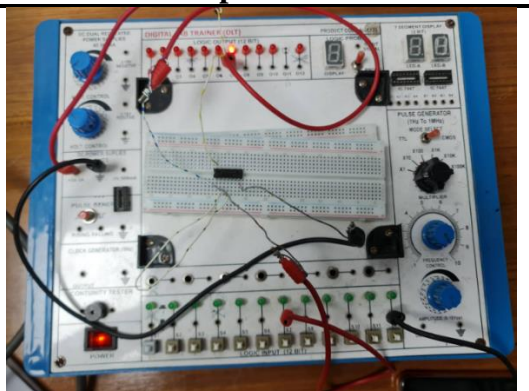
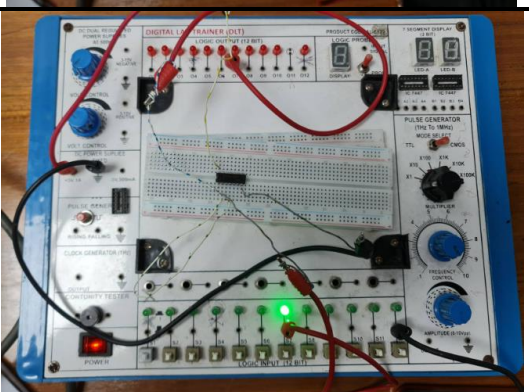
**X-NOR gate using NAND gate:**

Input A	Input B	Output Y	Experiment
0	0	1	
0	1	0	
1	0	0	

1	1	1	
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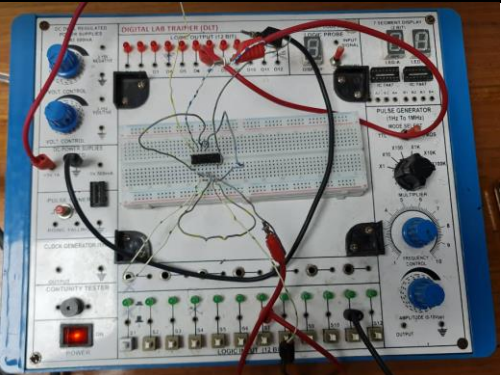
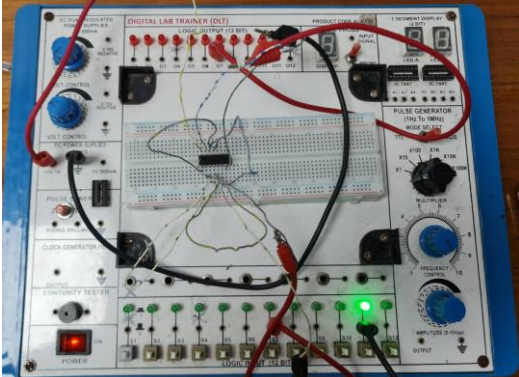
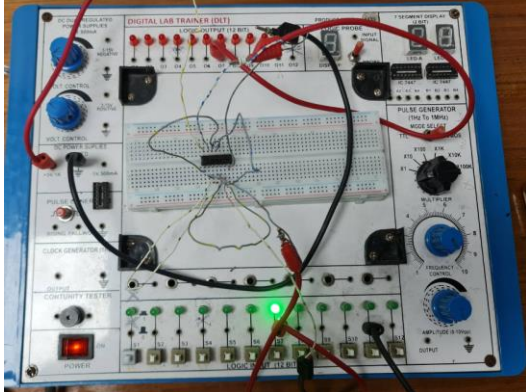
2. Find out the equivalent NOT, OR and AND gate by using NOR gates only. Now construct an X-OR and X-NOR gate in your trainer board by using NOR gates only. Use required IC to construct the circuit.

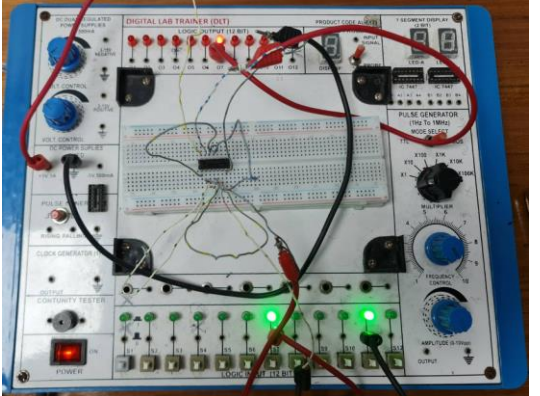
NOT gate using NOR gate:

Input A	Output Y	Experiment
0	1	
1	0	

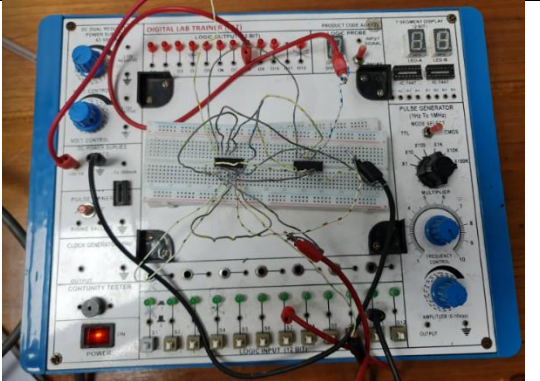
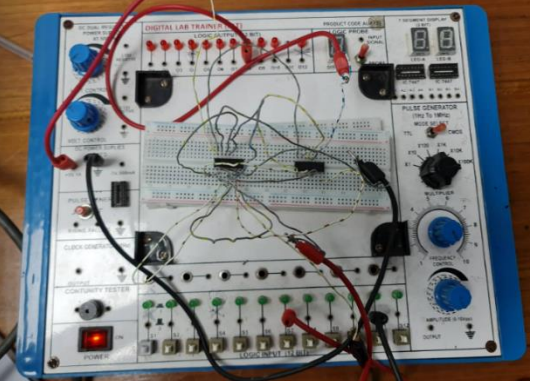
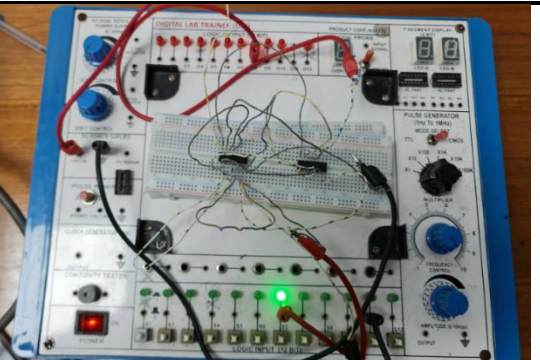


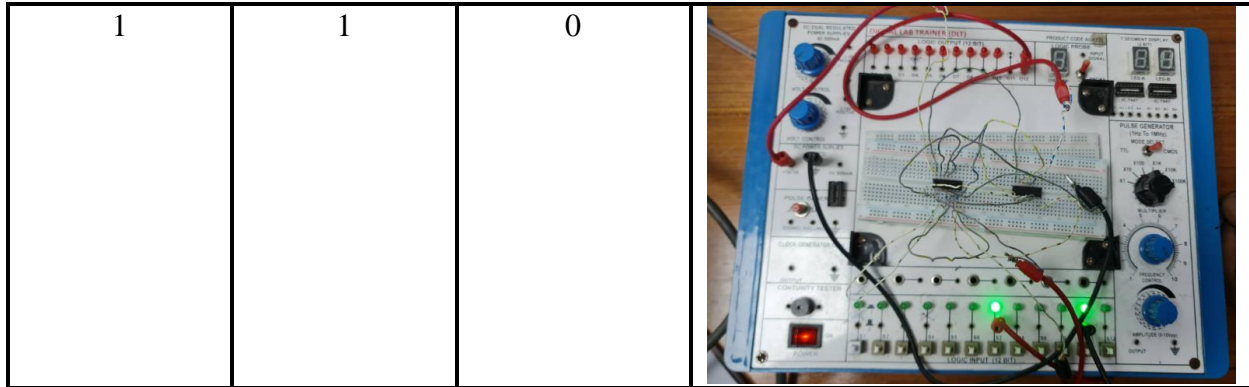
# **AND gate using NOR gate:**

Input A	Input B	Output Y	Experiment
0	0	0	
0	1	0	
1	0	0	

1	1	1	
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**X-OR gate using NOR gate:**

Input A	Input B	Output Y	Experiment
0	0	0	
0	1	1	
1	0	1	



## **Results:**

The simulation is done using NI Multisim and the experiment is done in lab in training board and different ICs.

In simulation all the gates and logical expression are implemented using NAND gate and NOR gate. In experiment IC-74HC00N (NAND) and IC-74HC02N (NOR) ICs are used to implement AND, OR, X-OR, X-NOR gates.

The simulation results and the experimental results are accurate according to truth table. Both simulation and experiment match perfectly.

## **Report Question & answer:**

1. What do you mean by universal gate?

Ans: A universal gate is a logic gate by which any Boolean function can be implemented without the need to use any other type of logic gate. NOR gate and NAND gate are universal gates.

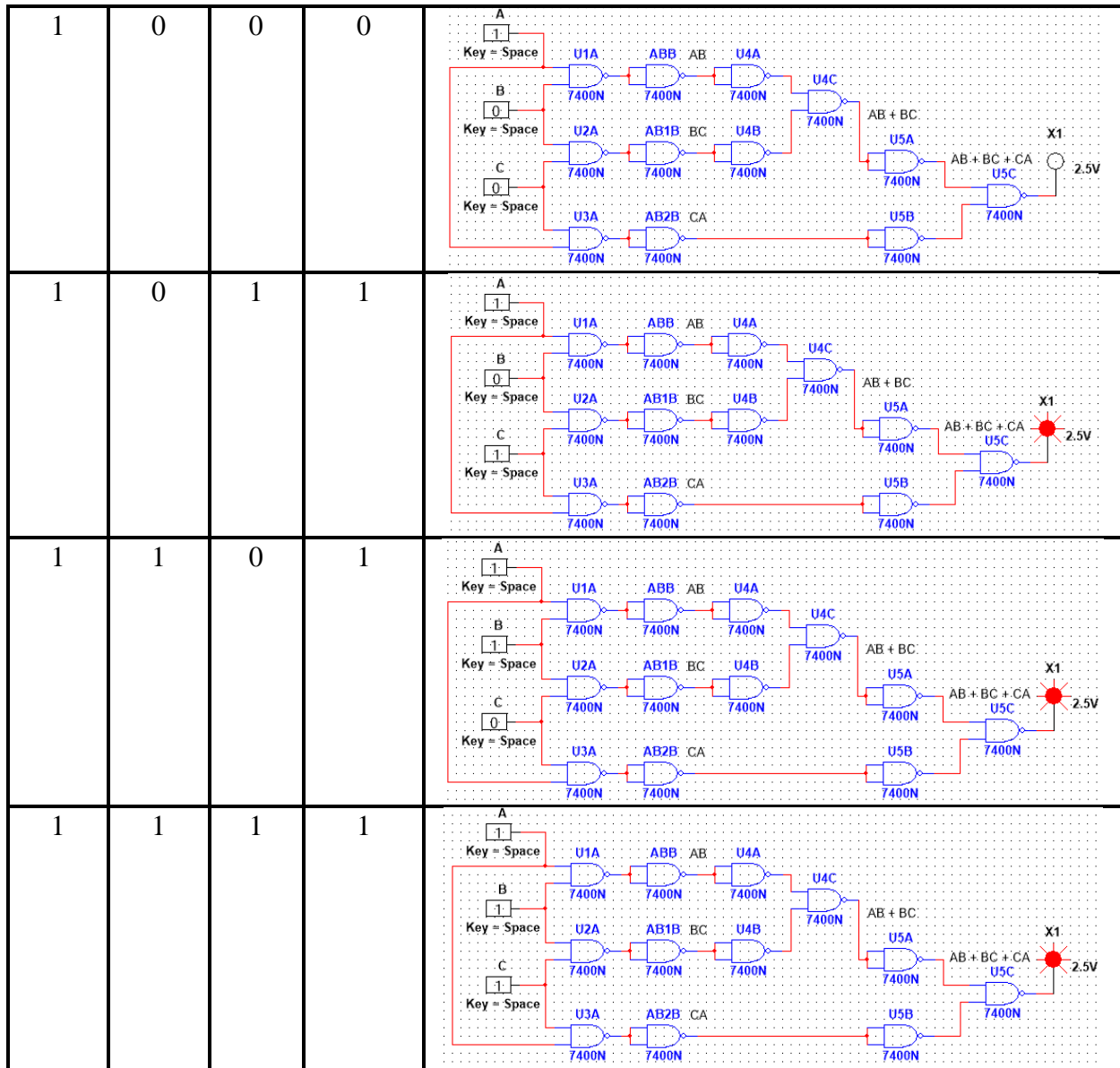
2. What are the ICs required in this experiment?

Ans: To implement the circuit only universal gates are used. So, in experiment IC-74HC00N (NAND) and IC-74HC02N (NOR) ICs are used to implement AND, OR, X-OR, X-NOR and other gates.

3. Construct a circuit of output F, where  $F=AB + BC + CA$ , by using NAND gates only and show the output states for each of the available conditions.

Ans: Output for different input for the Boolean expression.

Input A	Input B	Input C	Output X1	Simulation
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	



## Discussion:

During the experiment we encountered some difficulties such as bread board have some issue all the pin holes weren't working. The pin arrangement of NAND gate and NOR gate were not same which also cause some issue but after checking the PIN arrangement of the ICs twice before assembling the circuit will help to avoid this problem. Some NAND gate also cause some issue, after changing the ICs solve the problem. Incorrect connections can also be very likely to happen



as there are lots of connection to make. To solve the problem all the connection should check more than once.

### **Conclusion:**

Logic gates are used in electronic devices to perform logical operations. There are seven basic logic gates. The objective of this lab is to compare all the logic gates and using universal gates to implement all fundamental gates. All the simulation and experimental results matches accurately.

## **References**

- [1] “logic gate (AND, OR, XOR, NOT, NAND, NOR and XNOR),” December 2020. [Online]. Available: <https://www.techtarget.com/whatis/definition/logic-gate-AND-OR-XOR-NOT-NAND-NOR-and-XNOR#:~:text=Basic%20logic%20gates,the%20logical%20%22and%22%20operator..>
- [2] Z. Tucaković, “Technical Diagnosis of Basic Logic Gates,” in *The 39th international convention on information and communication technology, electronics and microelectronics.*, Opatija, Croatia, 2016.
- [3] “Operations of logic gates,” Tutorials Point, April 2021. [Online]. Available: [https://www.tutorialspoint.com/computer\\_logical\\_organization/logic\\_gates.htm](https://www.tutorialspoint.com/computer_logical_organization/logic_gates.htm). [Accessed September 2022].