

AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH

Faculty of Engineering

Lab Report Cover Page

Assignment Title:	Studying different digital logic gates and designing of basic logic gates us Universal gates		logic gates using
Assignment No:	01	Date of Submission:	27 September 2022
Course Title:	DIGITAL LOGIC AND CIRCUITS LAB		
Course Code:	00868 Section: N		N
Semester:	Fall 2022-23	Course Teacher:	RETHWAN FAIZ

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3	MD. OLI ULLAH RAFI	20-42934-1	BSc [CSE]
4	PARTHA MALAKAR	20-42908-1	BSc [CSE]
5	MD. ATIKUR RAHMAN ATIK	19-40033-1	BSc [CSE]

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	Total Marks

(A4.5)

1289/22



AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH

Faculty of Engineering

Lab Report Cover Page

Assignment Title:	Studying different digital logic gates Universal gates	Studying different digital logic gates and designing of basic logic gates using Universal gates		
Assignment No:	01	Date of Submission:	26 October 2022	
Course Title:	DIGITAL LOGIC AND CIRCUITS LAB	DIGITAL LOGIC AND CIRCUITS LAB		
Course Code:	00868 Section: N			
Semester:	Fall 2022-23 Course Teacher: RETHWAN FA			

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Abstract:

To learn about different logic gate and how to implement them using training board and digital integrated circuits.

Introduction:

Logic gates are used in electronic devices to perform logical operations. There are seven basic logic gates and two universal logic gates. In this lab the goal is to understand the gates and to implement all the basic gates with universal gates.

Theory and Methodology:

Logic gate implements a Boolean function, which is a logical operation on one or more binary inputs that results in a single binary output. Transistors, diodes, and resistors can all be used to create logic gates. Commonly, resistors are utilized as pull-up or pull-down resistors. When there are any unconnected logic gate inputs that need to be connected to a logic level 1 or 0, pull-up and pull-down resistors are utilized. This stops any erroneous gate switching. Pull-down resistors are wired to ground (0 V), and pull-up resistors are wired to Vcc (+5V) [1].

Basic logic gates are usually NOT, AND, OR, NAND and NOR gates [2] [Figure 1].

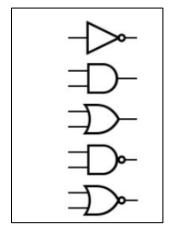


Figure 1 Common symbols of logic gates.

The reason the AND gate is thus named is because it behaves just like the logical "and" operator if 0 is labelled "false" and 1 is labelled "true." The OR gate takes its name from the way it functions, which is like the inclusive "or" in logic. If one or both of the inputs are "true," the result will also be "true." The output is "false" if both inputs are "false." In other words, at least one OR both of the inputs must be 1 for the output to be 1. Logical inverter has a single input and is occasionally referred to as a NOT gate to distinguish it from other kinds of electronic inverter devices. The NAND gate functions as a pair of AND gates and NOT gates. An inverter comes after the NOR gate, which is a combination OR gate [3].

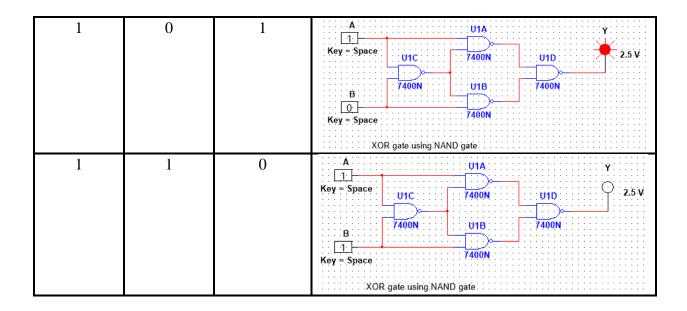
Simulation:

All the simulation are done using NI Multisim.

1. Construct an X-OR and X-NOR gate in your trainer board by using NAND gates only. Use required IC to construct the circuit.

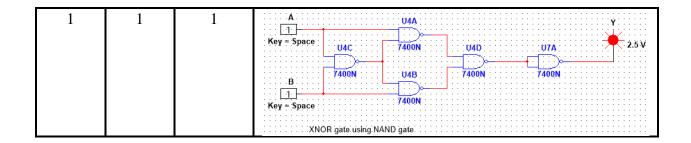
X-OR gate using NAND gate:

Input A	Input B	Output Y	Simulation
0	0	0	A U1A Y Key = Space U1C 7400N U1D 2.5 V B 7400N U1B 7400N Key = Space 7400N XOR gate using NAND gate
0	1	1	A



X-NOR gate using NAND gate:

Input A	Input B	Output Y	Simulation
0	0	1	A
0	1	0	A
1	0	0	A U4A Y Key = Space U4C 7400N U4D U7A 2.5 V B 7400N U4B 7400N 7400N Key = Space 7400N XNOR gate using NAND gate



2. Find out the equivalent NOT, OR and AND gate by using NOR gates only. Now construct an X-OR and X-NOR gate in your trainer board by using NOR gates only. Use required IC to construct the circuit.

NOT gate using NOR gate:

Input A	Output Y	Simulation
0	1	· · · · · · · · · · · · · · · · · · ·
		A U1A 2.5 V
		Key = Space 7402N
		NOT gate using NOR gate
1	0	Y
		A U1A 2.5 V
		Key = Space 7402N
		NOT gate using NOR gate

OR gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	0	A
0	1	1	A O Key = Space D T T T T T T T T T T T T
1	0	1	A 1 Key = Space B 7402N Key = Space OR gate using NOR gate
1	1	1	A 1 Key = Space B 7402N Key = Space OR gate using NOR gate

AND gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	0	A U3A Y 0
0	1	0	A U3A Y O
1	0	0	A U3A Y 1
1	1	1	A U3A Y Key = Space 7402N U3C 2.5 V B U3B 7402N Key = Space 7402N AND gate using NOR gate

X-OR gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	0	A U9A 0 Key = Space 7402N U9C Y B U9B 7402N V 2.5 V Key = Space 7402N V 2.5 V XOR gate using NOR gate
0	1	1	A U9A O V9C Key = Space 7402N U9C U12A 2.5 V T402N XOR gate using NOR gate V9C V12A 7402N XOR gate using NOR gate
1	0	1	A U9A 1
1	1	0	A U9A 1

X-NOR gate using NOR gate:

Input A	Input B	Output Y	Simulation
0	0	1	Markey = Space U13A 7402N U13D 2.5 V B 7402N U13C 7402N Key = Space 7402N XNOR gate using NOR gate
0	1	0	A U13B Y O WI3A 7402N U13D 2.5 V B 7402N U13C 7402N Key = Space 7402N XNOR gate using NOR gate
1	0	0	Note
1	1	1	A U13B Key = Space U13A 7402N U13D 2.5 V B 7402N U13C 7402N Key = Space 7402N XNOR gate using NOR gate

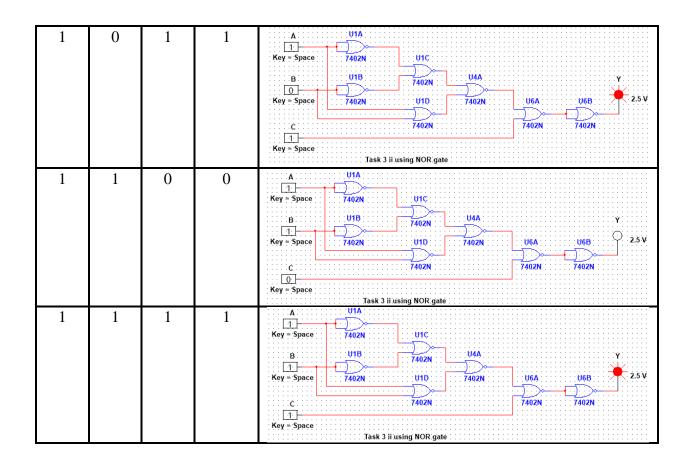
- 3. Convert the following expressions using universal gates and implement them in the trainer board. Compare the results with the truth table of the equations.
 - i) A (+) B
 - ii) (A(+)B) + C
 - **iii**) (AB +CD)'

Implementation of A (+) B

Input A	Input B	Output Y	Simulation
0	0	0	A U9A O V9C Y B U9B 7402N U12A 2.5 V Key = Space 7402N U9D 7402N XOR gate using NOR gate
0	1	1	A U9A O V9C Key = Space 7402N U9C U12A 2.5 V T402N U9D 7402N XOR gate using NOR gate
1	0	1	A U9A 1
1	1	0	A U9A 1

Implementation of (A(+)B) + C

Input	Input	Input	Output	Simulation
Ā	B	Ĉ	Ý	
0	0	0	0	A U1A O
0	0	1	1	A U1A O V1A Key = Space 7402N U1C B U1B 7402N U4A Y O V4A V6B 2.5 V C 7402N U1D 7402N V6A U6B C 7402N 7402N 7402N Task 3 ii using NOR gate
0	1	0	1	A U1A O
0	1	1	1	A U1A O
1	0	0	1	A U1A 1



Implementation of (AB +CD)'

Inpu	Inpu	Inpu	Inpu	Outpu	Simulation
t A	t B	t C	t D	t Y	
0	0	0	0	1	A U7A

0	0	0	1	1	A U7A O
0	0	1	0	1	A U7A O V7C B U7B 7402N Key = Space 7402N U17A U17A U17B U2A 2.5 V Key = Space 7402N U14C D U14B 7402N Task 3 iii using NOR gate.
0	0	1	1	0	A U7A O
0	1	0	0	1	A U7A O
0	1	0	1	1	A U7A O V7A New = Space 7402N U7C B U7B 7402N U17A U17B U2A C U14A 7402N 7402N 7402N 7402N New = Space 7402N U14C D U14B 7402N Key = Space 7402N Task 3 iii using NOR gate

0	1	1	0	1	A U7A 0
					ή 17R
					1 7402N U17A U17B U2A 2.5 V Key = Space 7402N
					C U14A 7402N 7402N 7402N
					1 7902N 7902N 7902N 1114C
					h HAR
					0 7402N Key = Space 7402N
					Task 3 ili using NQR gate
0	1	1	1	0	M U7A
					Key = Space 7402N U7C
					B 07B 7402N
					Key = Space 7402N 017A 017B 02A 2.5 V
					C U14A 7402N 7402N 7402N
					Key = Space 7402N U14C
					D U14B 7402N
					Key = Space 7402N Task 3 iii using NOR gate
1	0	0	0	1	<u>A</u> <u>u</u> TA
1	U	U	U	1	1 (17C) Key = Space 7402N (17C)
					y y
					B 7402N O 7402N Key = Space 7402N U17A U17B U2A 2.5 V
					C U14A 7402N 7402N 7402N
					0
					D U14B 7402N
					0 (Key = Space 7402N
					Task 3 iii úsing NOR gate
1	0	0	1	1	A: U7A
					Key = Space 7402N U7C
					B: U7B 7402N Y
					Key = Space 7402N
					C U14A 7402N 7402N 7402N
					Key = Space 7402N U14C
					D: U14B: 7402N
					Key = Space 7402N Task 3 iii using NOR gate
1	0	1	0	1	A
					1
					B. U7B 7402N
					0 U17A U17B U2A 2.5 V
					C U14A 7402N 7402N 7402N
					Key = Space 7402N U14C
					D U14B 7402N
					0
					Task 3 jii using NOR gate

1	0	1	1	0	A U7A T
					1
1	1	0	0	0	A UTA 1
1	1	0	1	0	D U14B 7402N O V17A Task 3 iii using NOR gate A U7A
					Key = Space 7402N UTC B UTB 7402N Y L1 VITA UTTB UZA 2.5 V Key = Space 7402N UTA 7402N 7402N 7402N C UT4A 7402N 7402N 7402N Ey = Space 7402N UT4C D UT4B 7402N Task 3 III using NOR gate.
1	1	1	0	0	A U7A 1
1	1	1	1		A U7A 1

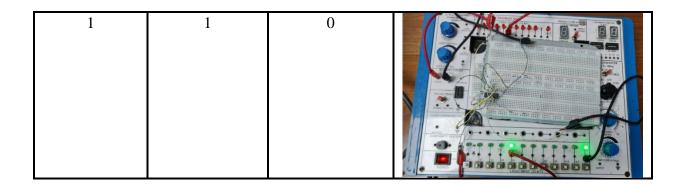
Experiment

Experiments are done in lab using training board and different ICs.

1. Construct an X-OR and X-NOR gate in your trainer board by using NAND gates only. Use required IC to construct the circuit.

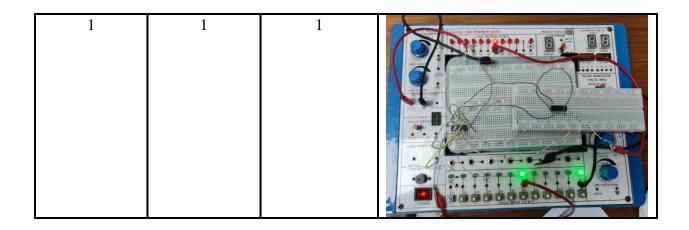
X-OR gate using NAND gate:

Input A	Input B	Output Y	Experiment
0	0	0	TANADA DE LES CONTROLES
0	1	1	
1	0	1	



X-NOR gate using NAND gate:

Input A	Input B	Output Y	Experiment
0	0	1	TOTAL LAB TRANSFEREN
0	1	0	TOTAL LIAS TRANSPORT (DIT) HOUSE TOTAL
1	0	0	THE STATE OF THE S



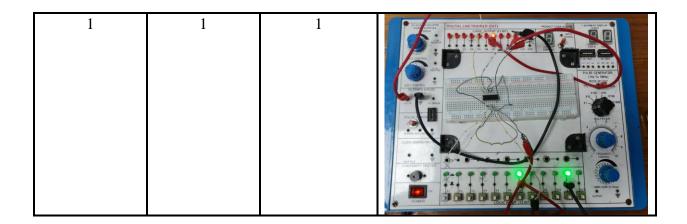
2. Find out the equivalent NOT, OR and AND gate by using NOR gates only. Now construct an X-OR and X-NOR gate in your trainer board by using NOR gates only. Use required IC to construct the circuit.

NOT gate using NOR gate:

Input A	Output Y	Experiment
0	1	THE THE PARTY OF T
1	0	PLAN ESTATE OF THE PROPERTY OF

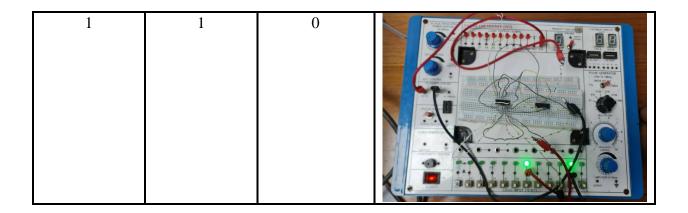
AND gate using NOR gate:

Input A	Input B	Output Y	Experiment
0	0	0	SCHOOL SECTION
0	1	0	CHECKEL COLUMN TO THE PROPERTY OF THE PROPERTY
1	0	0	DICTAL LAS TRANS (QT) THE CONTROL OF THE CONTROL O



X-OR gate using NOR gate:

Input A	Input B	Output Y	Experiment
0		0	THE RESIDENCE OF THE PARTY OF T
0	1	1	THE RESERVE OF THE PARTY OF THE
1	0	1	The state of the s



Results:

The simulation is done using NI Multisim and the experiment is done in lab in training board and different ICs.

In simulation all the gates and logical expression are implemented using NAND gate and NOR gate. In experiment IC-74HC00N (NAND) and IC-74HC02N (NOR) ICs are used to implement AND, OR, X-OR, X-NOR gates.

The simulation results and the experimental results are accurate according to truth table. Both simulation and experiment match perfectly.

Report Question & answer:

1. What do you mean by universal gate?

Ans: A universal gate is a logic gate by which any Boolean function can be implemented without the need to use any other type of logic gate. NOR gate and NAND gate are universal gates.

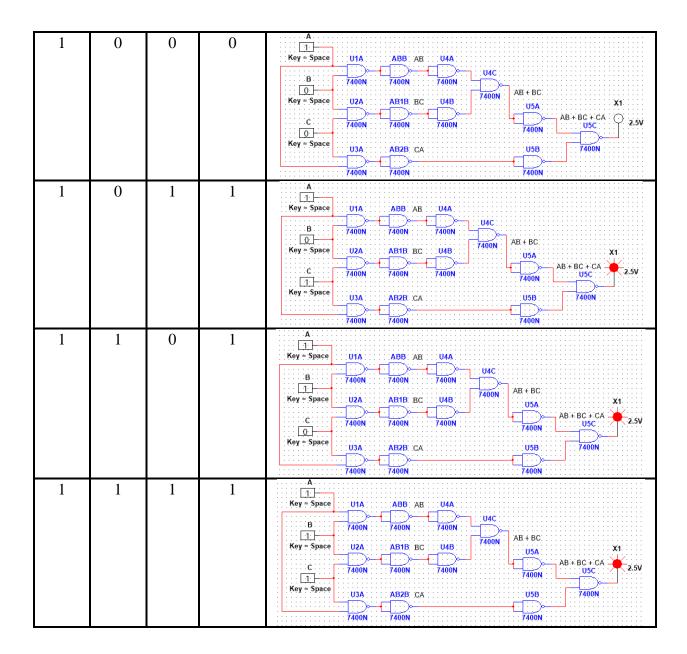
2. What are the ICs required in this experiment?

Ans: To implement the circuit only universal gates are used. So, in experiment IC-74HC00N (NAND) and IC-74HC02N (NOR) ICs are used to implement AND, OR, X-OR, X-NOR and other gates.

3. Construct a circuit of output F, where F=AB+BC+CA, by using NAND gates only and show the output states for each of the available conditions.

Ans: Output for different input for the Boolean expression.

Input	Input	Input	Output	Simulation
\mathbf{A}	В	C	X1	
0	0	0	0	A O Key = Space U1A ABB AB U4A B 7400N 7400N 7400N 7400N AB + BC Key = Space U2A AB1B BC U4B U5A X1 C 7400N 7400N 7400N 7400N U5C 2.5V O Key = Space U3A AB2B CA U5B 7400N
0	0	1	0	A
0	1	0	0	A O O SPACE U1A ABB AB U4A
0	1	1	1	A



Discussion:

During the experiment we encountered some difficulties such as bread board have some issue all the pin holes weren't working. The pin arrangement of NAND gate and NOR gate were not same which also cause some issue but after checking the PIN arrangement of the ICs twice before assembling the circuit will help to avoid this problem. Some NAND gate also cause some issue, after changing the ICs solve the problem. Incorrect connections can also be very likely to happen

as there are lots of connection to make. To solve the problem all the connection should check more than once.

Conclusion:

Logic gates are used in electronic devices to perform logical operations. There are seven basic logic gates. The objective of this lab is to compare all the logic gates and using universal gates to implement all fundamental gates. All the simulation and experimental results matches accurately.

References

- [1] "logic gate (AND, OR, XOR, NOT, NAND, NOR and XNOR)," December 2020. [Online]. Available: https://www.techtarget.com/whatis/definition/logic-gate-AND-OR-XOR-NOT-NAND-NOR-and-XNOR#:~:text=Basic%20logic%20gates,the%20logical%20%22and%22%20operator..
- [2] Z. Tucaković, "Technical Diagnosis of Basic Logic Gates," in *The 39th international convention on information and communication technology, electronics and microelectronics.*, Opatija, Croatia, 2016.
- [3] "Operations of logic gates," Tutorials Point, April 2021. [Online]. Available: https://www.tutorialspoint.com/computer_logical_organization/logic_gates.htm. [Accessed September 2022].