Department of Electrical and Electronic Engineering (EEE)
Faculty of Engineering (FE)
American International University- Bangladesh (AIUB)

Laboratory Experiment Report

Digital Logic And Circuits Laboratory

Semester: Fall 2021-22

Experiment No: 2

Experiment Name: Deriving logic equations and truth table from a given statement or expression and construction of combinational circuits.

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Deriving logic equations and truth table from a given statement or expression and construction of combinational circuits

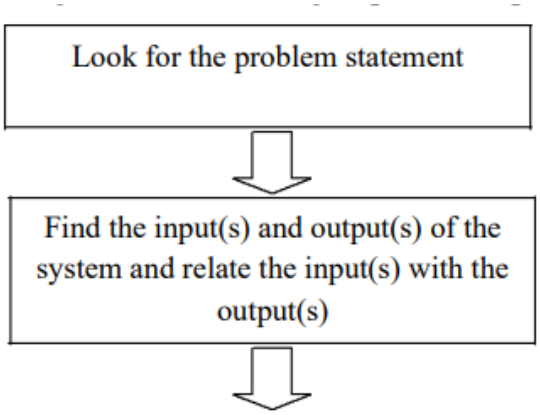
Abstract:
This experiment is designed to-
1. Help students implement the logic circuits derived from a given statement in the breadboard using gate ICs and observe whether the output verifies the truth table of the given logic statement or not.
2. Perform relevant theoretical work by deriving the logic circuit and truth table from the given logic equation/statement and get familiarized with Boolean algebra and De Morgan's law.
3. Simplify the logic expressions with K-Map and verify accuracy by breadboard implementation.

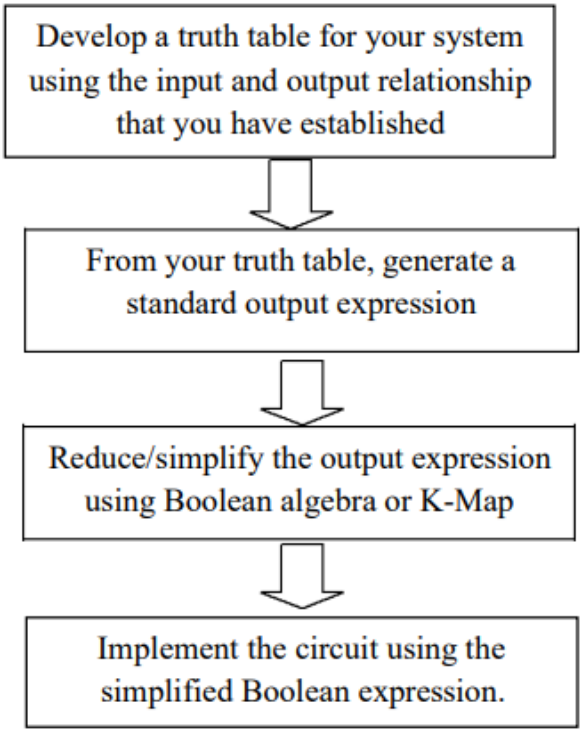
I. Introduction

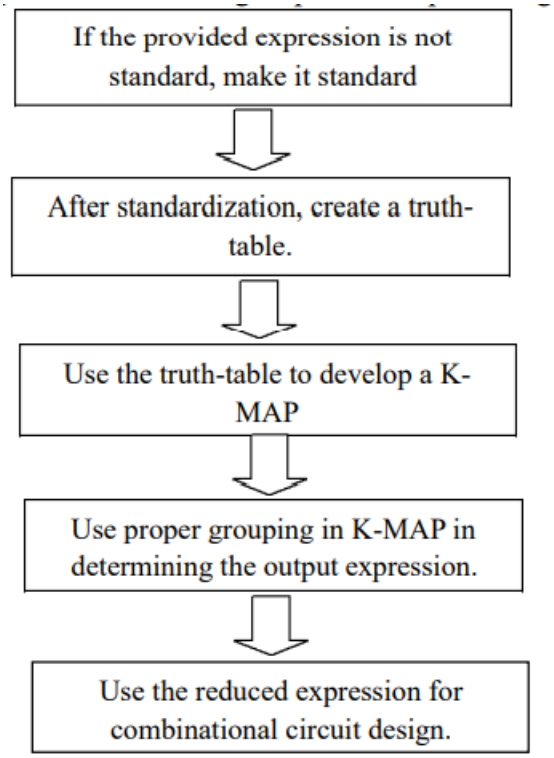
From any given logic statement, it is possible to construct a digital logic circuit. The first step in this process is to construct a truth table and then determine a standard SOP (sum of products) or POS (product of sums). At the same time, it is also possible to derive a logic expression from a given combinational circuit diagram by observing the individual logic operations performed in the circuit and matching them with their corresponding logic gates. Expressions are simplified using Boolean algebra and De Morgan's law or K-Map to reduce the number of gates used. Then the circuit is implemented in the breadboard using gate ICs and observed whether the output verifies the truth table of the given statement. This experiment shows the students a practical verification of deriving logic equations and truth table from combinational circuits. Knowing how to derive logic equations and truth table from combinational circuits helps a person with detecting the output logic expressions from any unknown logic circuit.

II. Theory And Methodology

Combinational circuits are built with logic gates and other components. It does not include any values to be taken from a previous state of the circuit. Designing such a combinational digital system requires use of one of the following methods:




Develop a truth table for your system using the input and output relationship that you have established
From your truth table, generate a standard output expression
Reduce/simplify the output expression using Boolean algebra or K-Map
Implement the circuit using the simplified Boolean expression.


If the provided expression is not standard, make it standard
After standardization, create a truth-table.
Use the truth-table to develop a K-MAP
Use proper grouping in K-MAP in determining the output expression.
Use the reduced expression for combinational circuit design.

III. Experimental Procedure

a) Draw a truth table to represent the output Y.

INPUT A	INPUT B	INPUT C	INPUT D	OUTPUT Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

b) Use the truth table outputs to form standard SOP and POS expressions.

SOP Expression: A’B’C’D + A’B’CD + A’BC’D + A’BCD’ + A’BCD + AB’C’D + AB’CD’ + AB’CD + ABC’D + ABCD’ + ABCD

POS Expression: (A + B + C + D) (A + B + C’ + D) (A + B’ + C + D) (A’ + B + C + D)

c) Minimize the SOP expression using Boolean algebra and K-Map. Perform hardware implementation of the circuit and compare with your truth table output.

Using Boolean algebra:

SOP Expression: A’B’C’D + A’B’CD + A’BC’D + A’BCD’ + A’BCD + AB’C’D + AB’CD’ + AB’CD + ABC’D + ABCD’ + ABCD
= A’B’D (C’+C) + A’BD(C’+C) + AB’D (C+C’) + ACD’(B+B’) + ABD (C+C’) + A’BCD’
=A’B’D+A’BD+AB’D+ACD’+ABD+A’BCD’
=AD’(B+B’) +AD(B’+B) + CD’(A+A’B)

=A'D+AD+CD'(A+D)
=D+CD'A+CD'B
=D+CA+D'CB
=D+CA+BC
=AC+BC+D

Using K-Map:

Expression:

Map

	$\overline{C}.\overline{D}$	$\overline{C}.D$	$C.D$	$C.\overline{D}$
$\overline{A}.\overline{B}$	0	1	1	0
$\overline{A}.B$	0	1	1	1
$A.B$	0	1	1	1
$A.\overline{B}$	0	1	1	1

Map Layout

	$\overline{C}.\overline{D}$	$\overline{C}.D$	$C.D$	$C.\overline{D}$
$\overline{A}.\overline{B}$	0	1	3	2
$\overline{A}.B$	4	5	7	6
$A.B$	12	13	15	14
$A.\overline{B}$	8	9	11	10

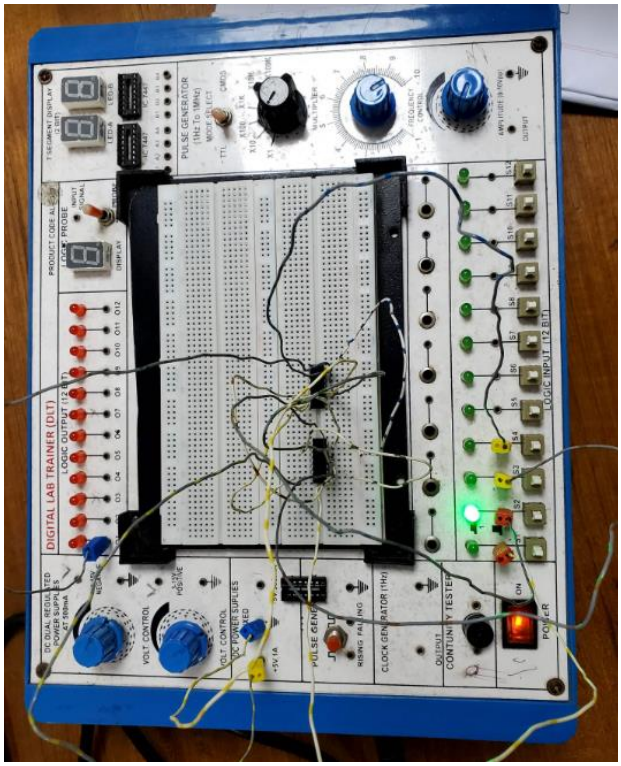
Groups

(1,3,5,7,9,11,13,15)	D
(6,7,14,15)	B.C
(10,11,14,15)	A.C

$y = D + BC + AC$

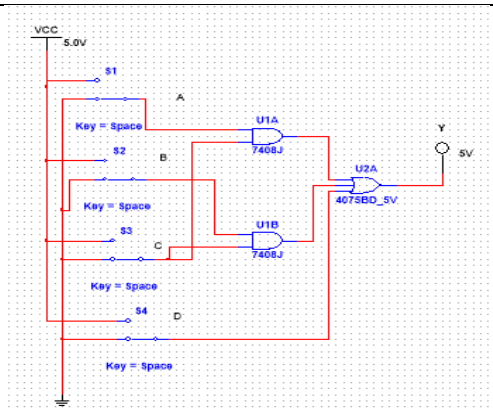
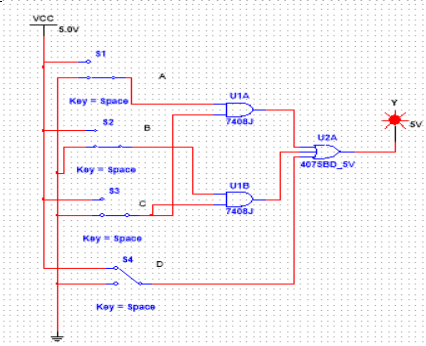
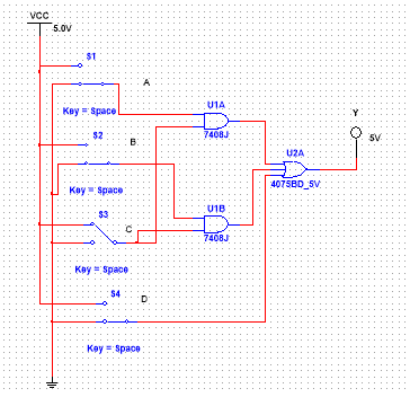
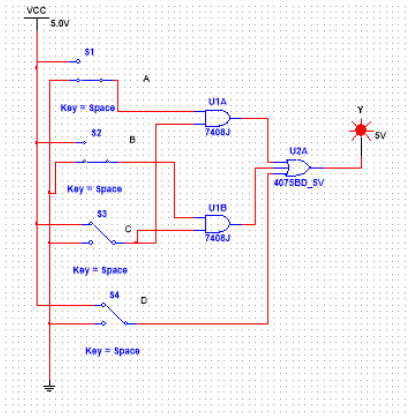
IV. Results

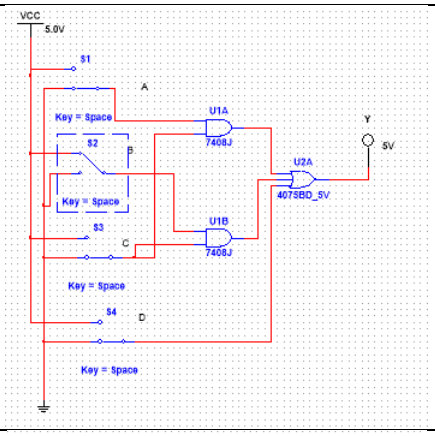
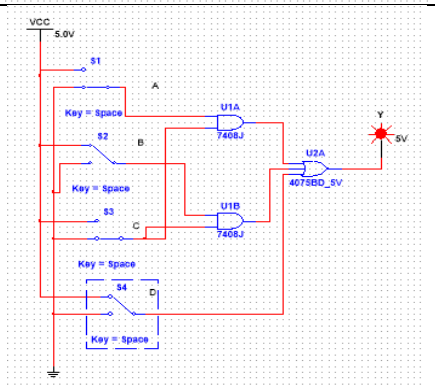
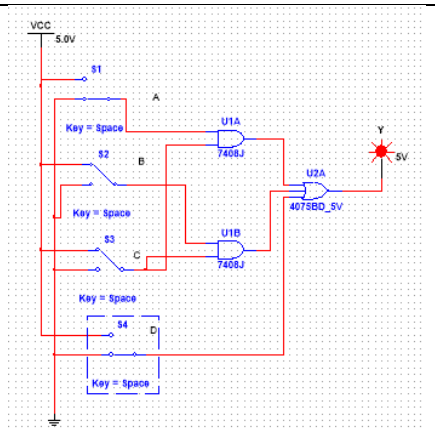
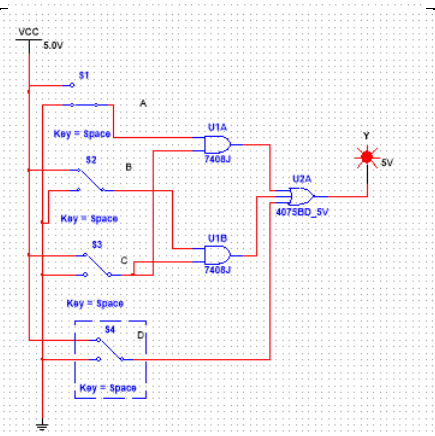
Practical Result:

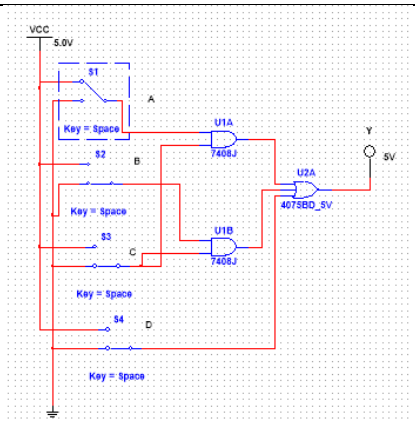
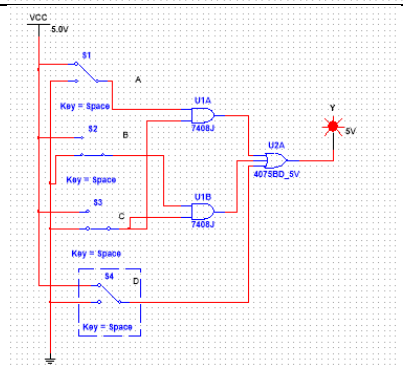
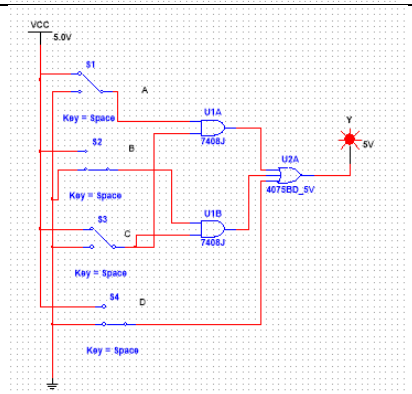
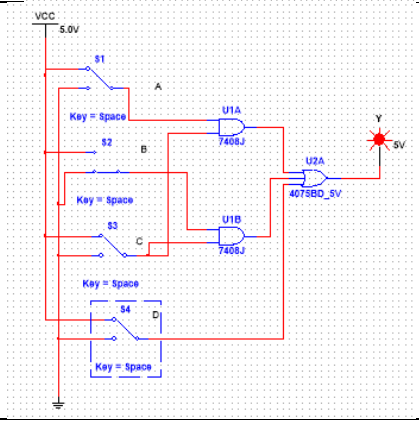


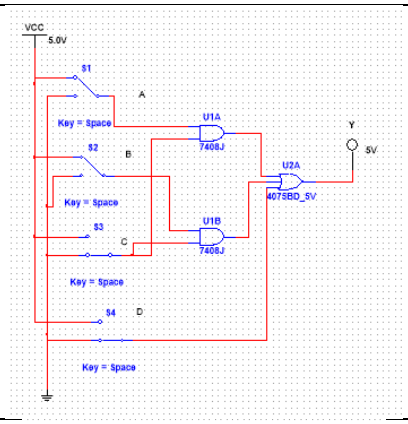
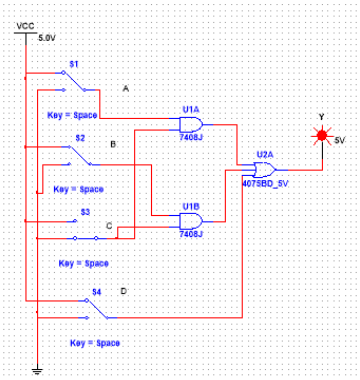
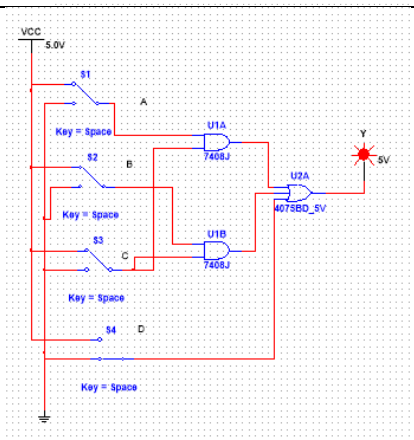
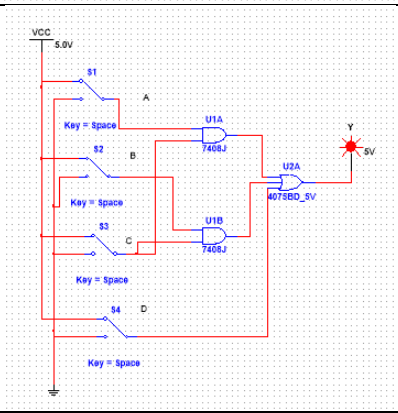
Simulation Result:

INPUT A	INPUT B	INPUT C	INPUT D	OUTPUT Y	SIMULATION

0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	1	1	

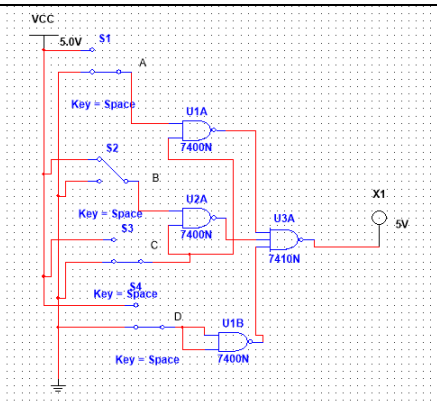
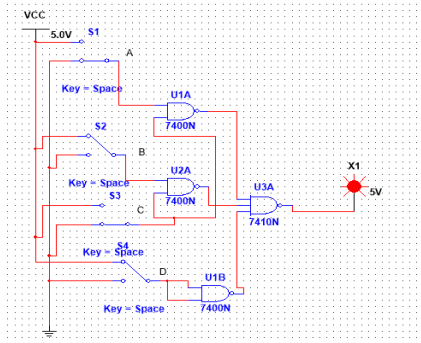
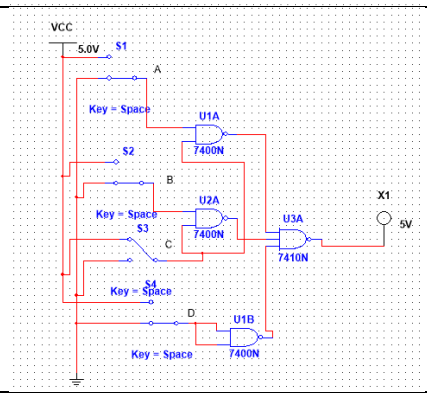
0	1	0	0	0	
0	1	0	1	1	
0	1	1	0	1	
0	1	1	1	1	

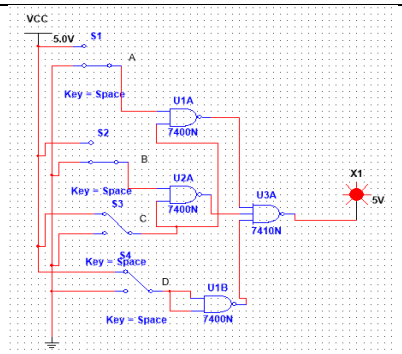
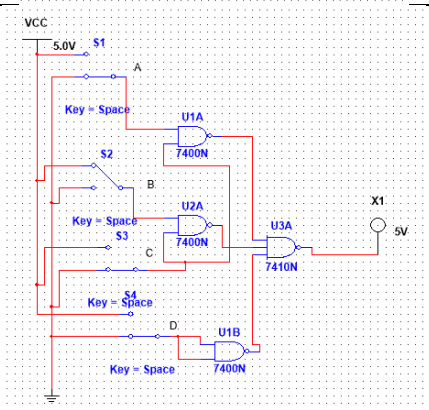
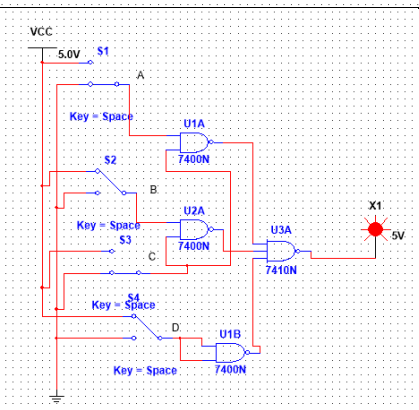
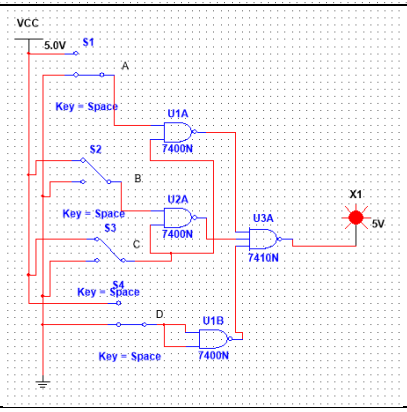
1	0	0	0	0	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	1	

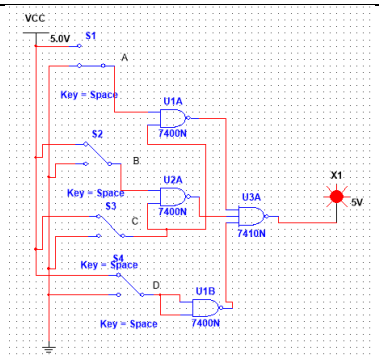
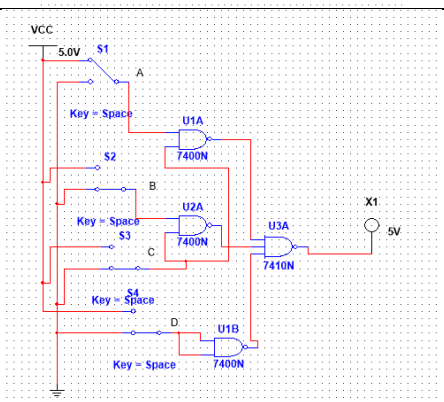
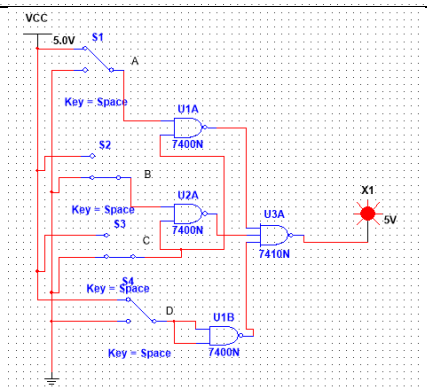
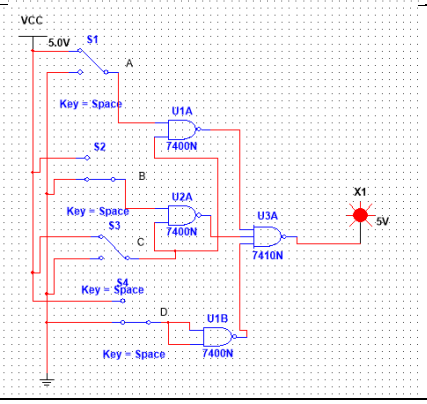
1	1	0	0	0	
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	1	

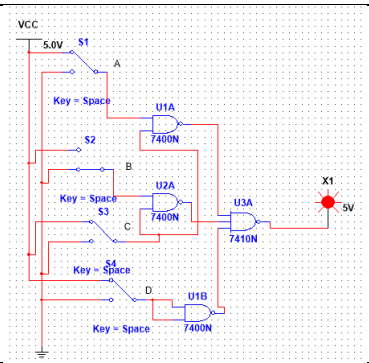
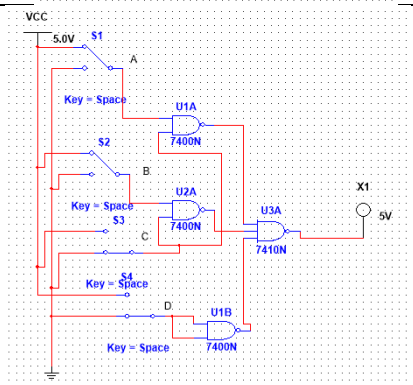
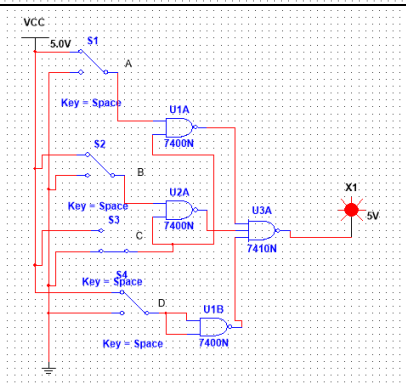
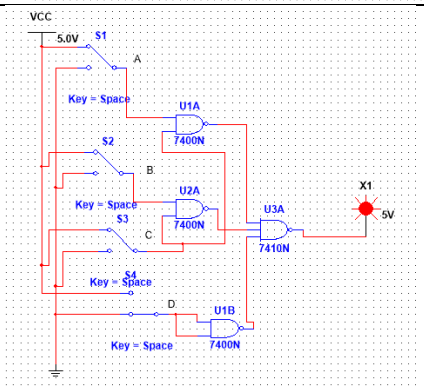
Report Questions:

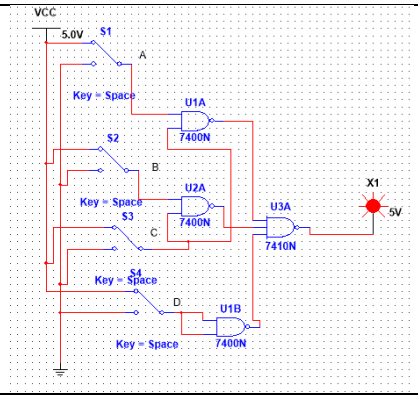
1. Construct the derived equations (i) using Universal gates.
   Ans:

INPUT A	INPUT B	INPUT C	INPUT D	OUTPUT Y	SIMULATION
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	0	

0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	
0	1	1	0	1	

0	1	1	1	1	
1	0	0	0	0	
1	0	0	1	1	
1	0	1	0	1	

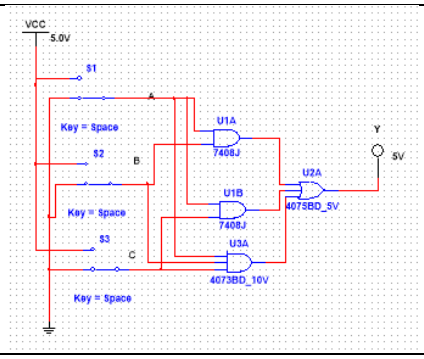
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	1	
1	1	1	0	1	

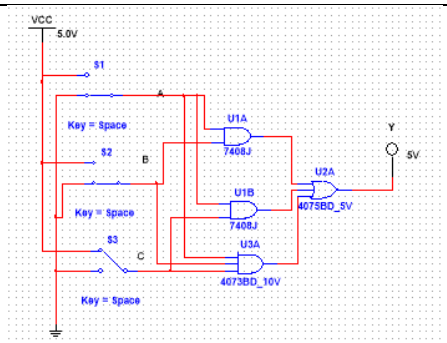
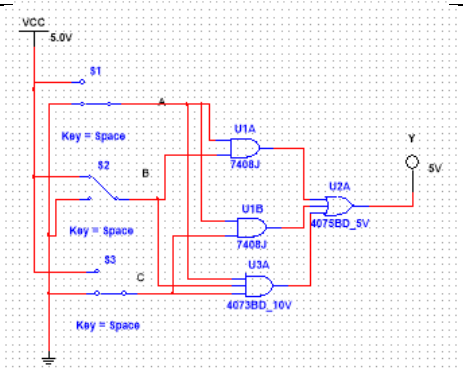
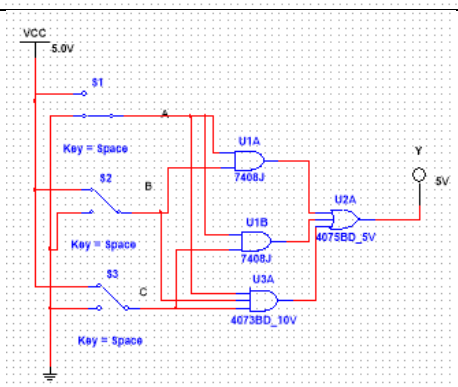
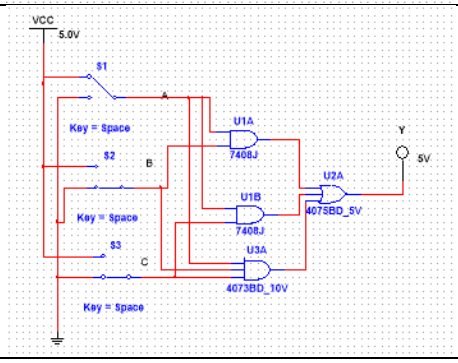
1	1	1	1	1	

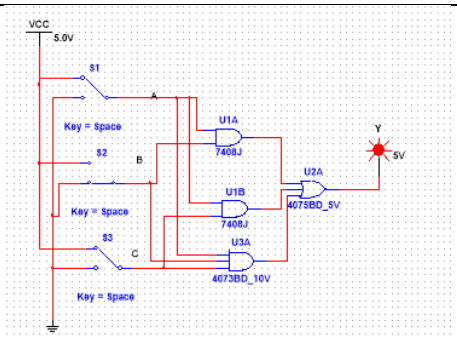
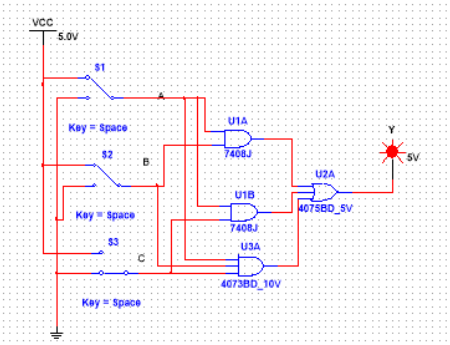
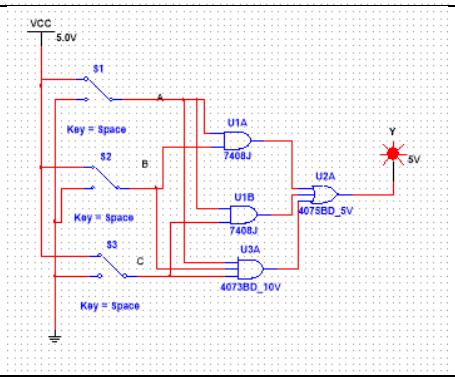
2. Develop the truth table for a certain three-input logic circuit with the output expression Y=ABC+(AB)'C+A'BC+AB'C+A(B'+C).
   Ans:

INPUT A	INPUT B	INPUT C	OUTPUT Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

3. Implement the following logic expressions with logic gates Y=ABC+AB+AC
   Ans:

INPUT A	INPUT B	INPUT C	OUTPUT Y
0	0	0	

0	0	1	
0	1	0	
0	1	1	
1	0	0	

1	0	1	
1	1	0	
1	1	1	

V. Discussion And Conclusion

During the experiment we encountered some difficulties such as bread board have some issue all the pin holes weren't working. The pin arrangement of NAND gate and NOR gate were not same which also cause some issue but after checking the PIN arrangement of the ICs twice before assembling the circuit will help to avoid this problem. Some NAND gate also cause some issue, after changing the ICs solve the problem. Incorrect connections can also be very likely to happen as there are lots of connection to make. To solve the problem all the connection should check more than once.

VI. References

[1] www. tutorialspoint.com
[2] www.electronics-tutorials.ws
[3] faculty.kfupm.edu.sa
[4] "Digital Fundamentals" by Thomas L. Floy