

NYA
SIR

CSE360

MIDOL

1)

3) (4) 0100 = load Ac from I/O

(5) 0101 = store Ac to I/O

7) (6) 0110 = store Ac to device 17

a) program execution for Load Ac from device 14

~~Step 01:-~~

memory		cpu registers	
300	4014		300 PC
301	6940		Ac
302	5017	4014	IR Initialy PC is 300 value 4014 is loaded into IR
:			
940	0020	I/O device	
941	0019	014	4014 → to load device 14 info
		016	
		017	

~~Step 02:-~~

memory		cpu registers	
300	4014	3001	PC
301	6940	0016	Ac PC increment by 1
302	5017	4014	and load value in I/O device
:			
940	0020	014	(014) which 0016 info
941	0019	016	mu acculator
		017	

b) Add contents of memory location 940,-

memory		cpu registers	
300	4014	301	PC
301	6940	0016	Ac The next instruction
302	5017	6940	IR 6940 location 301 and PC is increment
:		I/O device	
940	0020	014	IR work for
941	0019	017	new instruction

step 5: — memory

300 4014

301 6940

302 5017

:

940 0020

941 0019

CPU registers

302 PC

0036 AC

6940 IR

$$PC = PC + 1$$

$$= (301+1)$$

$$= 302$$

$$0016 + 0020 = 0036$$

value of true location

940 is ~~0020~~ 0020

I/O device

add to AC

0014

0017

$$AC = AC + 0020$$

$$= 0020 + 0016$$

$$= 0036$$

c) Store AC to device 17! —

step 6: — memory

CPU registers

300 4014

301 6940

302 5017

302 PC

0036 AC

5017 IR

the next instruction 5017

location is 302 and

I/O device IR work for new instruction

940 0020

014

941 0019

017

step 6: — memory

CPU register

300 4014

301 6940

302 5017

303 PC

0036 AC

5017 IR

PC is 1 increment is

memory. The content of

I/O device

AC stored in device

940 0020

017

941 0019

017

0036

017. 6

so, value 0036 to I/O

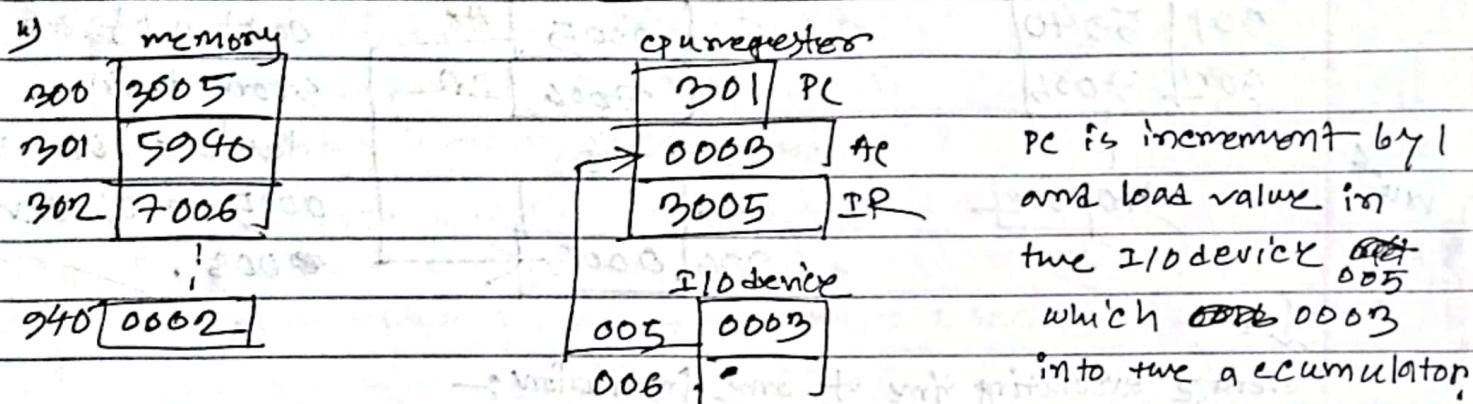
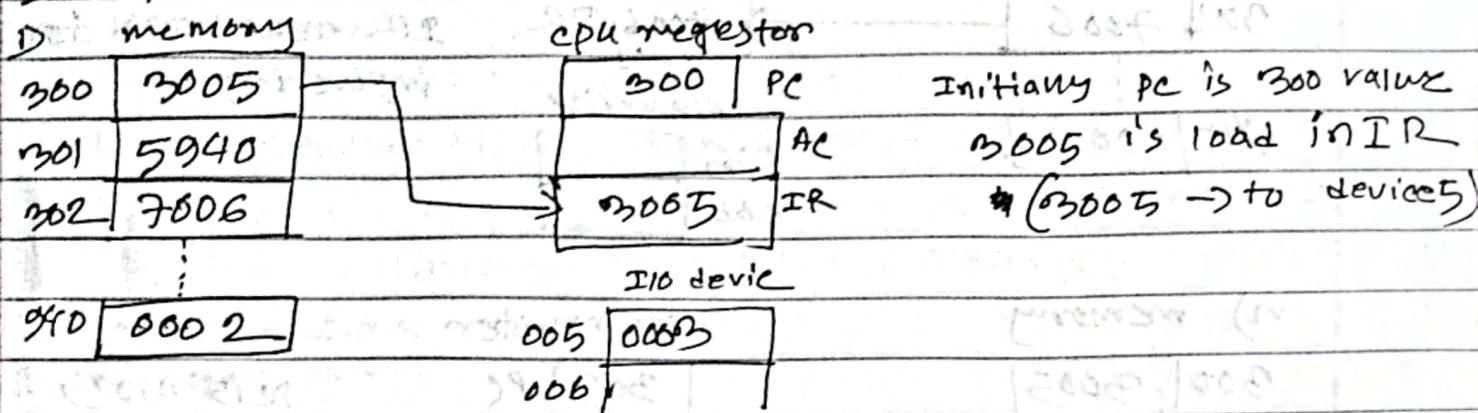
device is 017

2)

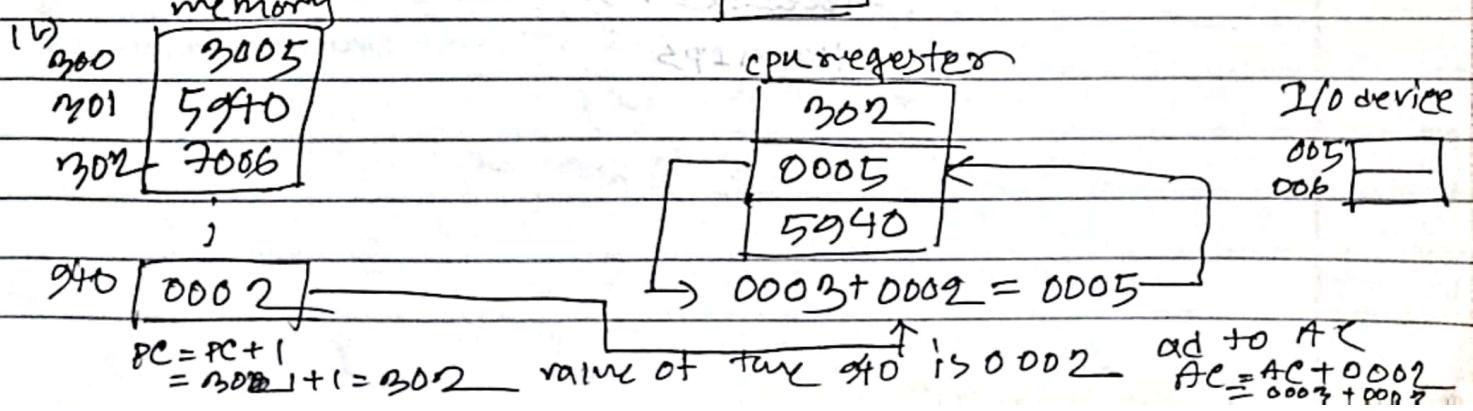
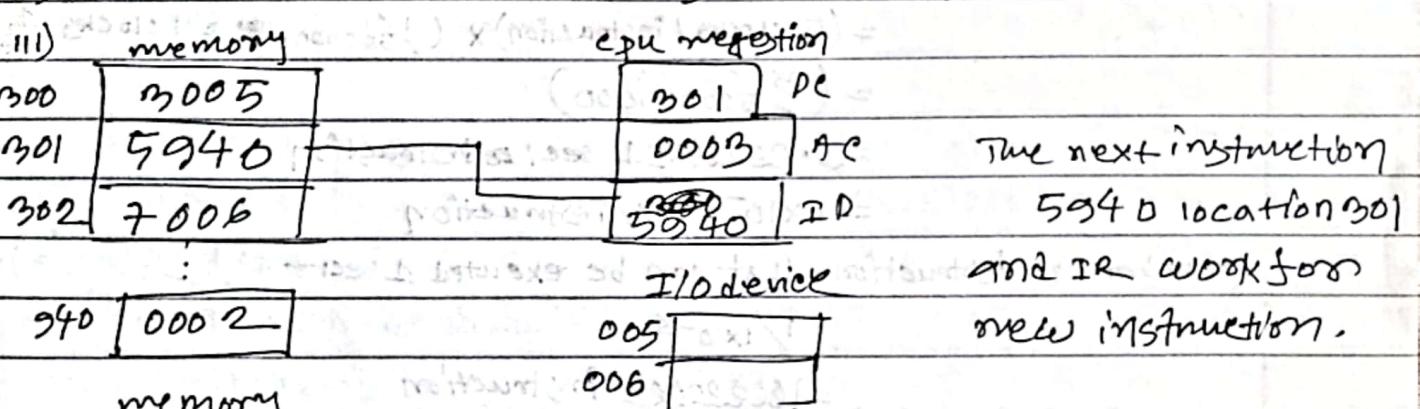
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Mim

(3) 0011 \Rightarrow load AC from I/O(3) 0111 \Rightarrow store AC to I/O(5) 0101 \Rightarrow Add AC to memory

a) program execution to load AC from device 59:-



b) Add contents of memory location 940:-



c) Store AC to device 6 :

i) memory

300	3005
301	5940
302	7006

940 | 0002

cpu register

302	PC
0005	AC
7006	IR

I/O device

005	
006	

The next instruction 3006
location is 302 and
IR new word for
instruction.

ii) memory

300	3005
301	5940
302	7006

940 | 0002

cpu register

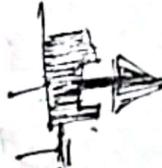
303	PC
0005	AC
7006	IR

I/O

005	
006	0005

pc is 303. The
content of AC
stored in
device 006. Value
0005 to I/O device
006.

~~1000000 KHz~~



④ Average time of execution one instruction:—

CPI x clock time

$$= \{ (10 \text{ clock/instruction}) \times (1/1000000000) \}$$

$$= \frac{10}{1000000000}$$

$$= 1 \times 10^{-9}$$

$$= 0.0000001 \text{ sec/instruction}$$

$$1 \text{ KHz} = 1000 \text{ Hz}$$

$$1000000 = 1000000000$$

$$1000000000 \text{ clock} \rightarrow 1 \text{ sec}$$

Number of instruction can be executed 1 sec = $\frac{1}{1 \times 10^{-9}}$

$$= 1000000000 \text{ instruction}$$

$$= 10 \text{ MIPS } \underline{\text{Ans}}$$

④ $125 \text{ MHz} = 125000000000$

$$125000000000 \text{ clock } 1 \text{ sec}$$

CPI x clock time

$$= (77 \text{ clock/instruction}) \times (1/125000000000)$$

$$= \frac{77}{125000000000}$$

$$= 6.16 \times 10^{-10} \text{ sec/instruction}$$

Hossain min

Number of instruction can be executed 1 sec $\frac{1}{6.16 \times 10^{-10}}$

$$1.25 \times 10^{11}$$

$$1000000000000$$

$$= 1.25 \times 10^{11} \text{ instruction}$$

$$= 125000 \text{ MIPS}$$

a) CPI = $\{ (65000 \times 2) + (52000 \times 3)$

$$+ (18000 \times 4) + (12000 \times 5) \}$$

$$= 418000 / 1000000000$$

$$90000 \text{ KHz}$$

$$40 \text{ MHz}$$

$$\therefore = 0.418$$

$$90000000 \text{ Hz}$$

b) MIPS = $f / \text{CPI} \times 10^6$

$$= 90000000 / 0.418 \times 10^6$$

$$= 2.15 \times 10^{14}$$

c) program executed time $T = I_c \times \text{CPI} \times t$

$$= \{ (1000000 \times 0.418) \times (1/900000000) \}$$

$$= 465 \times 4.65 \times 10^{-3}$$

Ans)

Ans to the question no: 8

x) Average time of execution one instruction:

CPI x clock time

$$\{ (77 \text{ clock/instruction}) \times \left(\frac{1}{125000000 \text{ Hz}} \right) \} = \frac{77}{125000000} \text{ sec}$$

$$= 6.16 \times 10^{-10} \text{ sec/instruction}$$

Number of instruction can be executed for 1 sec:

$$\frac{1}{6.16 \times 10^{-10}}$$

$$= 1623376623 \text{ Instruction}$$

$$= 1623.37 \text{ MIPS } (\text{Ans})$$

Ans to the question no: 9

Average time execution one col) instruction:

CPI x col clock times

$$\{ (10 \text{ clock/instruction}) \times \left(\frac{1}{10000000 \text{ Hz}} \right) \} = \frac{10}{10000000} \text{ sec}$$

$$= 1 \times 10^{-7} \text{ sec/instruction}$$

Number of instruction can be executed for 1 sec:

$$= 10000000 \text{ instruction}$$

$$= 10000 \text{ MIPS } (\text{Ans})$$

Ans to the question no: 02

a) CPI = $\{ (65000 \times 2) + (52000 \times 3) + (18000 \times 4) + (12000 \times 5) \} / 1000000$

$$= \frac{418000}{1000000}$$

$$= 0.418 \text{ MIPS } (\text{Ans})$$

b) MIPS = $1 / \text{CPI} \times 10^6$

$$= \frac{10000000}{0.418 \times 10^6}$$

$$= 215.31 \text{ MIPS } (\text{Ans})$$

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c) program execution time T: $I_c \times \text{CPI} \times t$

$$= 1000000 \times 0.418 \times \frac{1}{4}$$

$$= 1000000 \times 0.418 \times 1$$

$$= 3000000$$

$$= 4.65 \times 10^{-3} \text{ s}$$

$$= 4.65 \text{ ms } \text{ Ans//}$$

Hossain
Ans

Ans to the question no: 02

a) 1st microprocessor data transfer per cycle 16 bit or 2 bytes
and " " " " " " " " = 32 bit or 4 bytes

16 bits wide external data bus transfer rate (300 instruction $\times 16$)
 $= 4800 \text{ bits/cycle}$

32 bits wide external data bus transfer rate (300 instruction $\times 32$)
 $= 9600 \text{ bits/cycle}$

maximum data transfer differ by a factor $9600/4800$
 $= 2 \text{ bits/cycle}$

Thus that the 32 bits microprocessor has twice the data transfer rate

b)

Half of the operands and instructions are two byte long
 $= 16 \text{ bits}$

Assume we have to perform 300 transfers of operands and instruction
which 150 are two bytes long and 150 four bytes long.

For the 16 bit microprocessor require $150 + (2 \times 150) \frac{1}{2} = 32 \text{ bits}$
 $= 450 \text{ bus cycle}$

For the 32 bit microprocessor require $(150 + 150) \frac{1}{2} = 300 \text{ bus cycle}$

The data transfer rate differ by a factor $450/300$

$= 1.5 \text{ bus cycle}$

Half of the operands and instructions two byte long

Assume we have to perform 300 transfer of operands
which 150 are two byte long and 150 four byte

For 16 bit mp require $150 + (2 \times 150) \frac{1}{2}$

a)

Ans to the question no: 05

64 bit microprocessor

External data bus 64 bit

Clock input 64 MHz

six(6) input clock cycle = one bus cycle

64 MHz 1 sec

6400000 clock cycle 1 sec

$$1 \text{ sec} = 1/6400000 \text{ sec}$$

$$= 1.5625 \times 10^{-8} \text{ sec}$$

$$= 1.5625 \times 10^{-8} \times 1000000000$$

$$= 15.625 \text{ ns}$$

one bus cycle takes (6 × 15.625)

$$= 93.75 \text{ ns}$$

93.75 ns data transfer 8 bytes

$$1 \text{ " } " " " \frac{8}{93.75} \text{ "}$$

$$10^9 \text{ " } " " " \frac{8 \times 10^9}{93.75}$$

$$= 8333333.33$$

$$= \frac{8333333.33}{10^6}$$

$$= 8.33 \text{ MB/sec}$$

(Ans)

b) To increased performance,

External data bus 128 bit

double clock frequency 64 to 128 MHz

128 MHz 1 sec

128000000 clock cycle / sec

$$1 \text{ sec} = 1/128000000$$

$$= 7.8125 \times 10^{-9} \text{ sec}$$

$$= 7.8125 \times 10^{-9} \times 10^9$$

$$= 7.8125 \text{ ns}$$

46.875 ns data transfer 8 bytes

$$1 \text{ ns} = \frac{8}{46.875} \text{ "}$$

$$10^9 \text{ " } " " " \frac{8 \times 10^9}{46.875}$$

$$= 170.666666 \cdot 7$$

$$= 170.67 \text{ MB/sec}$$

(x)

one bus cycle takes (6 × 7.8125)

$$= 46.875 \text{ ns}$$

so, increasing clock freq, memory will double the data transfer rate but increasing to 128 bits external data bus not effect performance but bus width

Also,

Assume Bus cycle rate $16/\frac{6}{\text{MHz}}$

$$= 2.67 \text{ MHz}$$

(Ans)

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Amstotur question no: 03

two wait state

in each memory read and four bus wait state write

9)

without wait states $(3+5+7+6+4)$ bus clock cycle
 $= 25$ bus clock cycle

The instruction requires one of memory access $(2+2+2+4)$

$= 10$ bus wait states

The duration increased $\{ \text{Total wait state} / \text{without state} \} \times 100\% \}$
 $\Rightarrow \{ (10/25) \times 100\% \}$
 $= 40\%$ Answ

6)

without wait state $(3+5+7+12+4)$ bus clock cycle
 $= 31$ bus clock cycle

The instruction requires one of four memory access $(2+2+2+4)$
 $= 10$ bus wait states

with wait state $(31+10)$

$= 41$ bus with state

The duration increased $\{ \frac{\text{Total wait states}}{\text{No of without state}} \} \times 100\% \}$

$$= \left\{ \frac{(41-31)}{31} \right\} \times 100\% \}$$

$= 32.25\%$ Answ

Xrossrain

Ans to the question no:- 6T

64 bits long 20%

32 bits long 40%

16 bits long 40%

consider 64 bit microprocessor the number of require $(20+40+40)$

$$= 100$$

consider 32 bit microprocessor the number of require $(2 \times 20) + 40 + 40$

$$= (40 + 40 + 40)$$

$$= 120$$

thus the improvement of $\{ (120 - 100) \times \frac{100}{120} \}$

$$= \frac{20 \times 100}{120}$$

$$= 16.68\% \quad (\text{Ans})$$

thus the improvement

$$\{ (120 - 100) \times \frac{100}{120} \}$$

$$= \frac{100 \times 20}{120}$$

Ans to the question no. 5

a) Instruction 64 Bits

opcode 16 Bits

operand address 48 bits

maximum addressable memory 2^{48}

$$= 2.82 \times 10^{14} \text{ Bytes}$$

$$= 2.82 \times 10^{14} / 10^9$$

$$= 282000 \text{ GB}$$

b)

- i) The local address bus 32 bits the whole address can be transfer at require two cycle to fetch a 64 bit instruction or operand.
- ii) The local address bus 64 bits the whole address can be transfer at once and decoded in the memory.

48

c) The program counter (PC) must be at least 2⁴ bit

Instruction Register (IR) contain the whole memory

instruction, it will to be 32 bit. the opcode part
it will have to be 8 bit; 16

16

~~which is 40 MB/s~~

Q) Consider the hit ratio is 0.7 and the access time for cache memory and main memory are 150ns and 1800ns respectively. what is the average memory access time in ns of CPU?

(Ans)

$$\begin{aligned} T_{avg} &= (H \times T_c) + (1 - H) \times (T_c + T_m) \\ &= (0.7 \times 150) + (1 - 0.7) \times (150 + 1800) \\ &= (105) + (1 - 0.7) \times 1950 \\ &= 105 + 1950 - 1365 \\ &= 2055 - 1365 \\ &= 690 \text{ ns} \end{aligned}$$

(Ans)



1st Binary number : 10.110110101×2^7

2nd Binary number : 111.0010×2^6

1st Binary number normalized : 1.0110110101×2^8

2nd Binary number normalized : 1.1100100000×2^8

$+ 11.0011010101 \times 2^8$

Normalized $\Rightarrow 1.0011010101 \times 2^9$

Sign bit 0 [It is positive number]

Exponent : $9 + 127$

$= 136$

$= \underline{1}000\ 1\underline{000}$

Mantissa : 100010000000000000000000

1 bit → 8 bit
↓ ↓

23 bit →
↓

0 | 10001000 | 100010000000000000000000

(AM)

TWO way

$$1KB = 1000B$$

TWO way set-associative mapping

size of cm times of 16 byte

size of cm of 8 KB

$$= 8000 \text{ byte}$$

$$= 2^{13}$$

$$= 8192$$

number of the block at cm $\frac{8192}{16}$

$$= 512 \text{ block}$$

Each sets of consists $\frac{512}{2}$

$$= 256 \text{ sets}$$

$$= 2^8$$

$$= 8 \text{ set}$$

main memory 64 MByte

$$= 2^{26}$$

number of block at mm $\frac{64}{16} \text{ MB}$

$$= 4 \text{ MB block}$$

$$= 2^{22}$$

the number of block 22

Tag = Block - Set

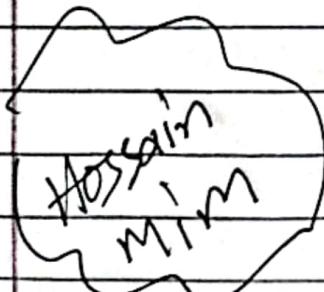
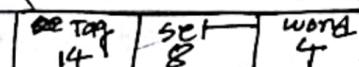
$$= 22 - 8$$

$$= 14$$

Block size = 16 byte

$$= 2^4$$

word 4 \leftarrow 26 \rightarrow



TWO way set associative

size of cache \rightarrow size 64 byte

size of cache memory of 32 KB

$$= 32000 \text{ byte}$$

$$= 2^{15}$$

$$= 32768$$

number of the block at cm $\frac{32768}{64}$

$$= 512 \text{ block}$$

Each sets of consists $\frac{512}{2}$

$$= 256 \text{ set}$$

$$= 2^8$$

$$= 8 \text{ set}$$

main memory 128 MB

$$= 128000000$$

$$= 2^{27}$$

$$= 4 \text{ MB block}$$

main memory size 27

$$= 2^{22}$$

number of block at mm $\frac{128}{64}$

$$= 2 \text{ MB/loc}$$

$$= 2000000$$

$$= 2^{21}$$

the number of block 21

$$\text{Tag} = 21 - 8$$

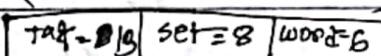
$$= 13$$

Block size 64 byte

$$= 2^6$$

$$\text{word} = 6$$

word 6 \leftarrow 27 \rightarrow



(Any)

Index bit:- set + word

$$= 13 + 6$$

cache size: 2^{Index}

$$= 19$$

$$= 2^5 \times (13 + 6 + 1 + 1) = 256$$

$$\frac{2^{9-1}}{2} = 1 \quad 128^{-1}$$

1st number:- $10.110110101 \times 2^7 \rightarrow$ normalized: 1.0110110101×2^8

2nd n :- $111.00010 \times 2^6 \rightarrow$ normalized: 1.1100010000×2^8

normalize: 1.0110110101×2^8

-normalized: 1.1100010000×2^8

$$11.0011000101 \times 2^8$$

normalized 1.10011000101×2^9

sign Bit : 0 It's positive number

Exponent: $9 + 127$

$$= 136$$

$$= \underline{\underline{10001000}}$$

$$\text{Mantissa} = 100010000000000000000000$$

1st number:- 10.10101×2^7

$$1.010101 \times 2^8$$

2nd number:- $\underline{\underline{11.10010}} \times 2^7$

$$1.110010 \times 2^8$$

$$11.000111 \times 2^8$$

$$\text{Normalize} \Rightarrow 1.1000111 \times 2^9$$

$$\Rightarrow 1.1\underline{\underline{000111}} \times 2^9$$

sign bit : 0 It's positive number

Exponent: $9 + 127$

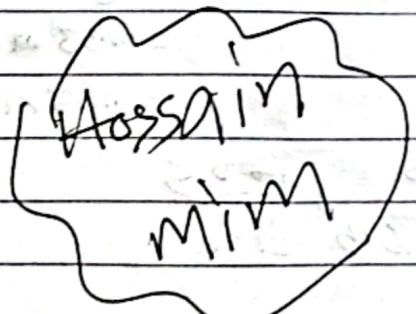
$$= 136$$

$$= \underline{\underline{10001000}}$$

$$\text{Mantissa} = 100010000000000000000000$$

\leftarrow	32	\rightarrow
0	10001000100010000000000000000000	

(Ans)



~~1367.98~~

An to the question no: 02

g)

maximum memory address space 2^{128}

$$= 3.40 \times 10^{38}$$

(Ans)

b) maximum memory address 3.40×10^{38}

But different thing between them is that is that
the access 64 bit memory will transfer a 64. and
the access of 128bit memory will transfer a 64. or
128 bit.

(Ans)

If the 16 bit assigned for I/O port number then microprocessor
can support 2^{16} numbers 16 bit I/O port for input →
 2^{16} for output.

In the case of I/O mapped I/O hardware can
support $2 \times 2^{16} = 2^{17}$ numbers of 16 bit I/O port
Similarly for 32 I/O port it can $2 \times 2^{32} = 2^{33}$
numbers of 32 bit I/O port.