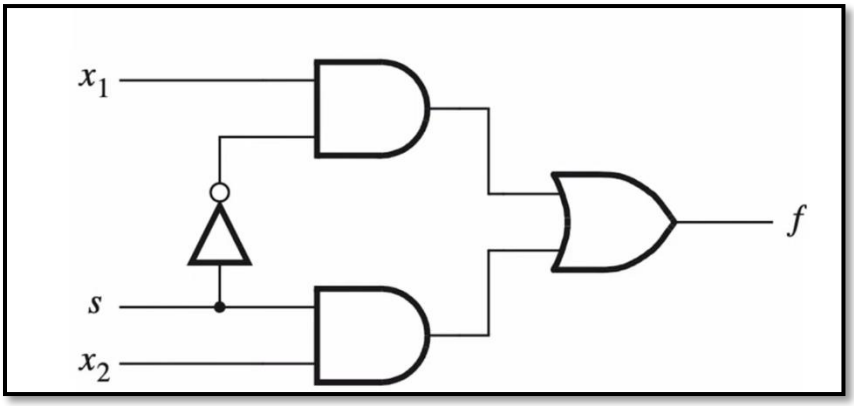
2to1 Mux data flow modeling 1,2

- Design Diagram:



- RTL Code:

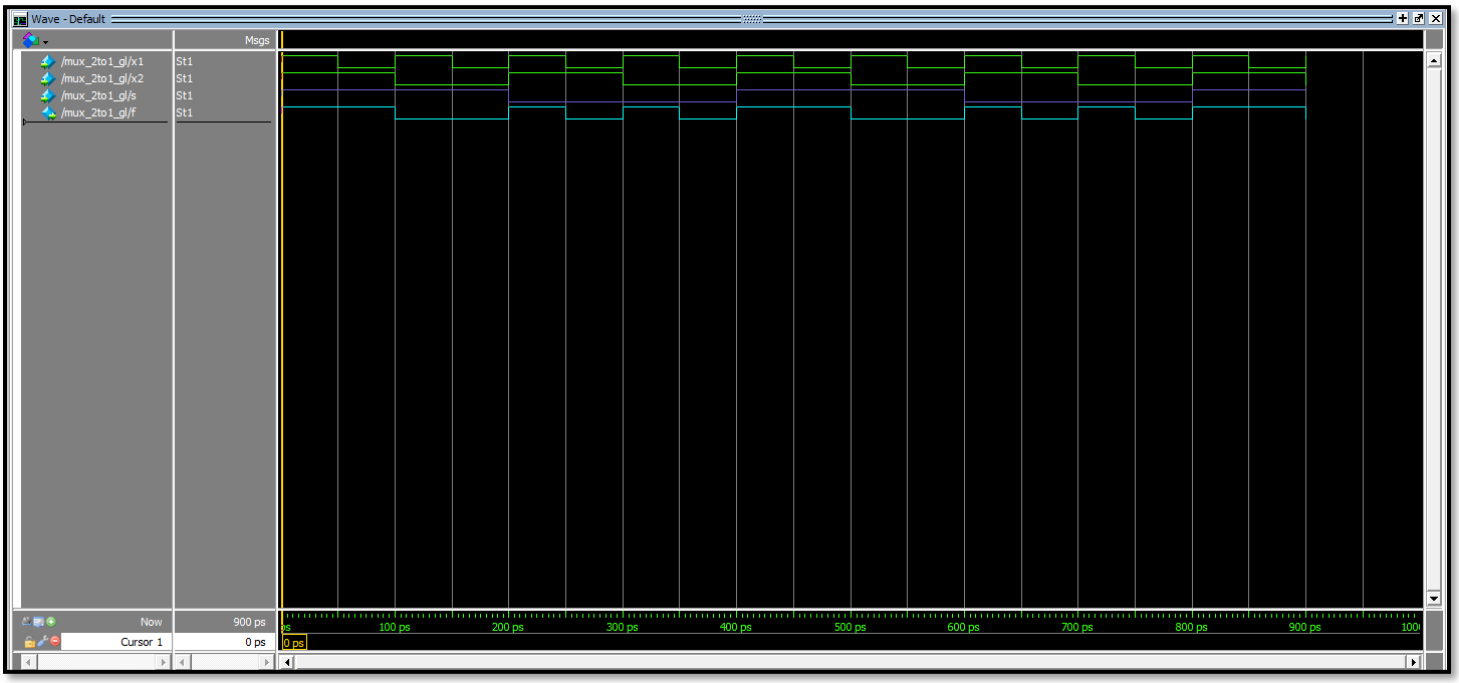
```
`timescale 1ns / 1ps

/*Hossam Ahmed Seyam*/
/*This code is illustrating How to design 2*1 mux in structural modelling especially data flow modeling */

module mux_2to1_df1(x1, x2, s, f);

    input wire x1, x2, s;   // x1,x2 are mux inputs , s is the selector of the 2*1 mux
    output wire f;          //mux output

    assign f = (x1 & ~s)|(x2 & s); //f =( x1.not(s) +  x2.s )

endmodule
```

```
`timescale 1ns / 1ps

/*Hossam Ahmed Seyam*/
/*This code is illustrating How to design 2*1 mux in structural modelling especially data flow modeling */

module mux_2to1_df2(x1, x2, s, f);

    input wire x1, x2, s;   // x1,x2 are mux inputs , s is the selector of the 2*1 mux
    output wire f;          //mux output

    assign f = s?x2:x1;     //if s acheived f = x2 ,if not then f =x1
endmodule
```

Made By : Hossam Ahmed Seyam

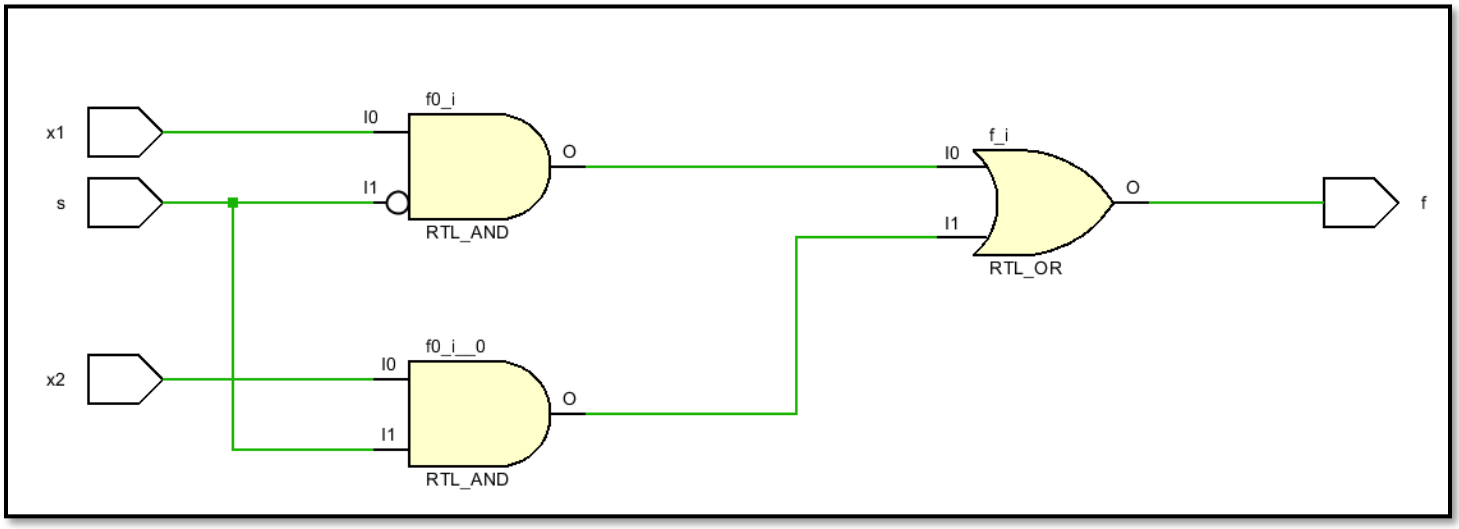
➢ Simulation:

They give the same simulation results.



➢ Elaborated Design:

They give the same Elaborated Design.



➢ **About:**

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