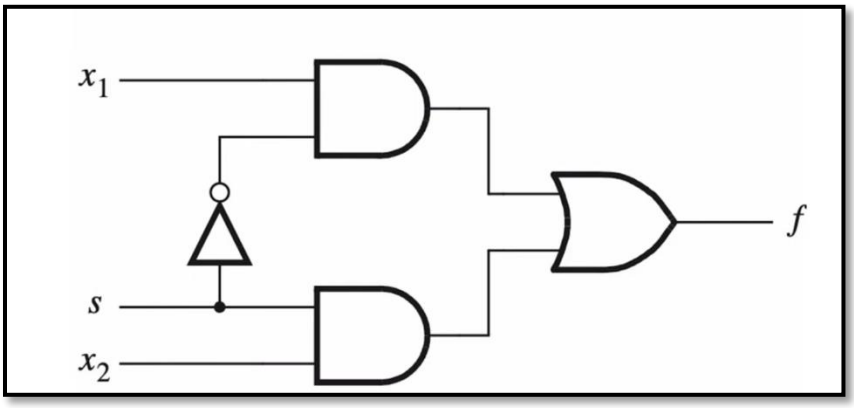
2to1 Mux gate level Modeling

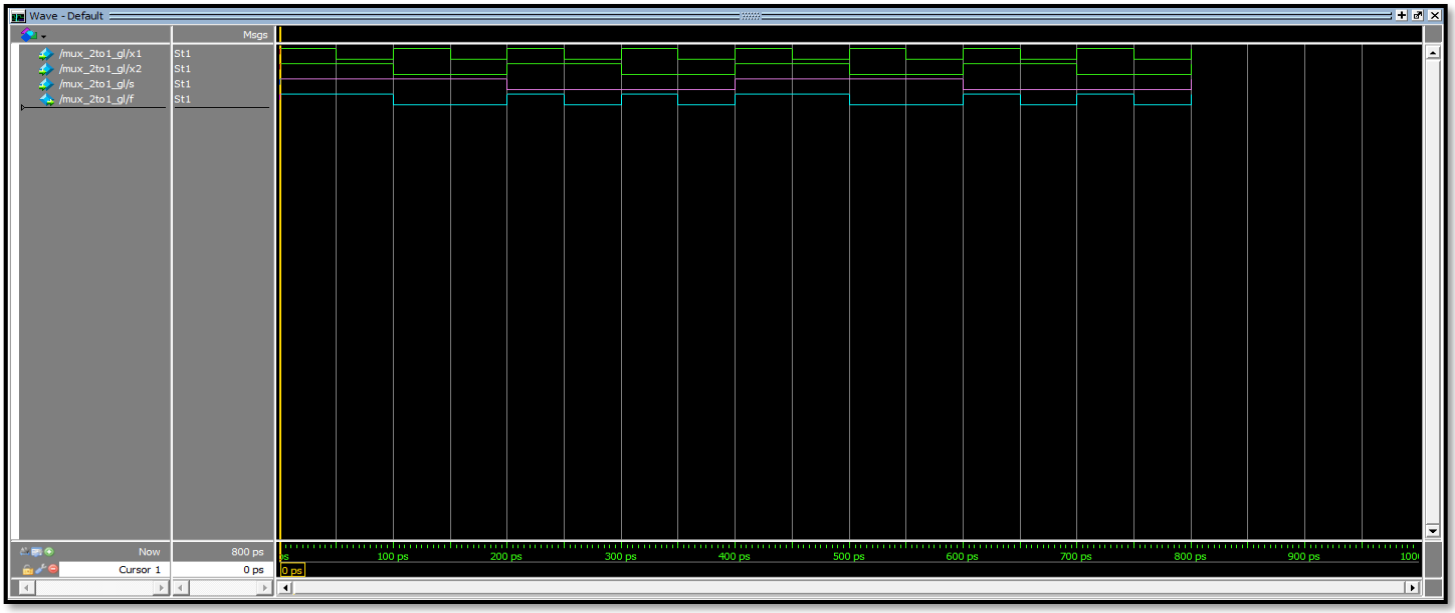
➢ Design Diagram:



➢ RTL Code:

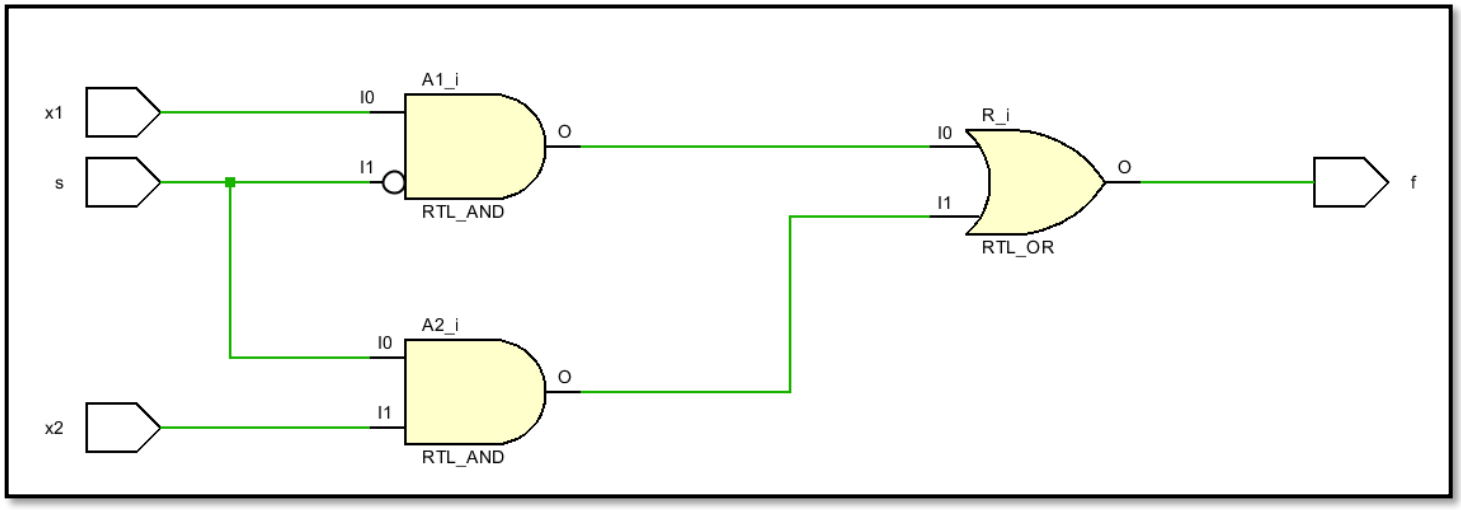
```
1   `timescale 1ns / 1ps
2
3   /*Hossam Ahmed Seyam*/
4   /*This code is illustrating How to design 2*1 mux in structural modelling especially gate level modeling */
5
6   module mux_2to1_gl(x1, x2, s, f);
7
8       input wire x1, x2, s;    // x1,x2 are mux inputs , s is the selector of the 2*1 mux
9       output wire f;           //mux output
10
11      wire w1, w2, ns;         // Declare the internal signals
12
13      and A1(w1, x1, ns);
14      and A2(w2, s, x2);
15      not N(ns, s);
16      or R(f, w1, w2);
17
18  endmodule
```

➢ Simulation:



Made By : Hossam Ahmed Seyam

➢ Elaborated Design:



➢ **About :**

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