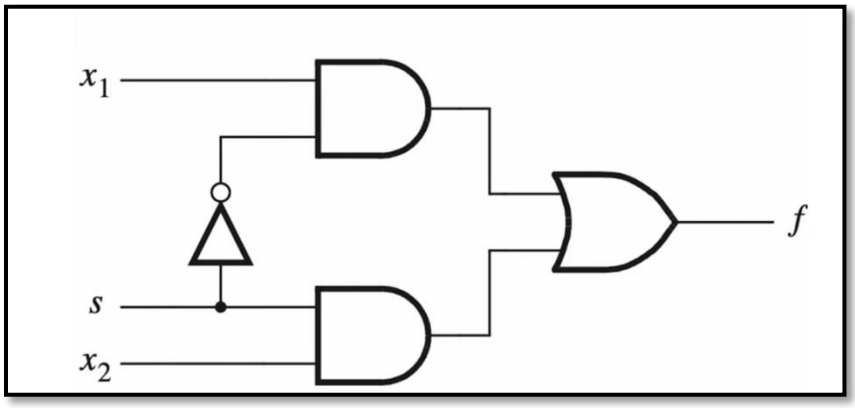
2to1 Mux behavioral Modeling 1,2

- Design Diagram:



- RTL Code:

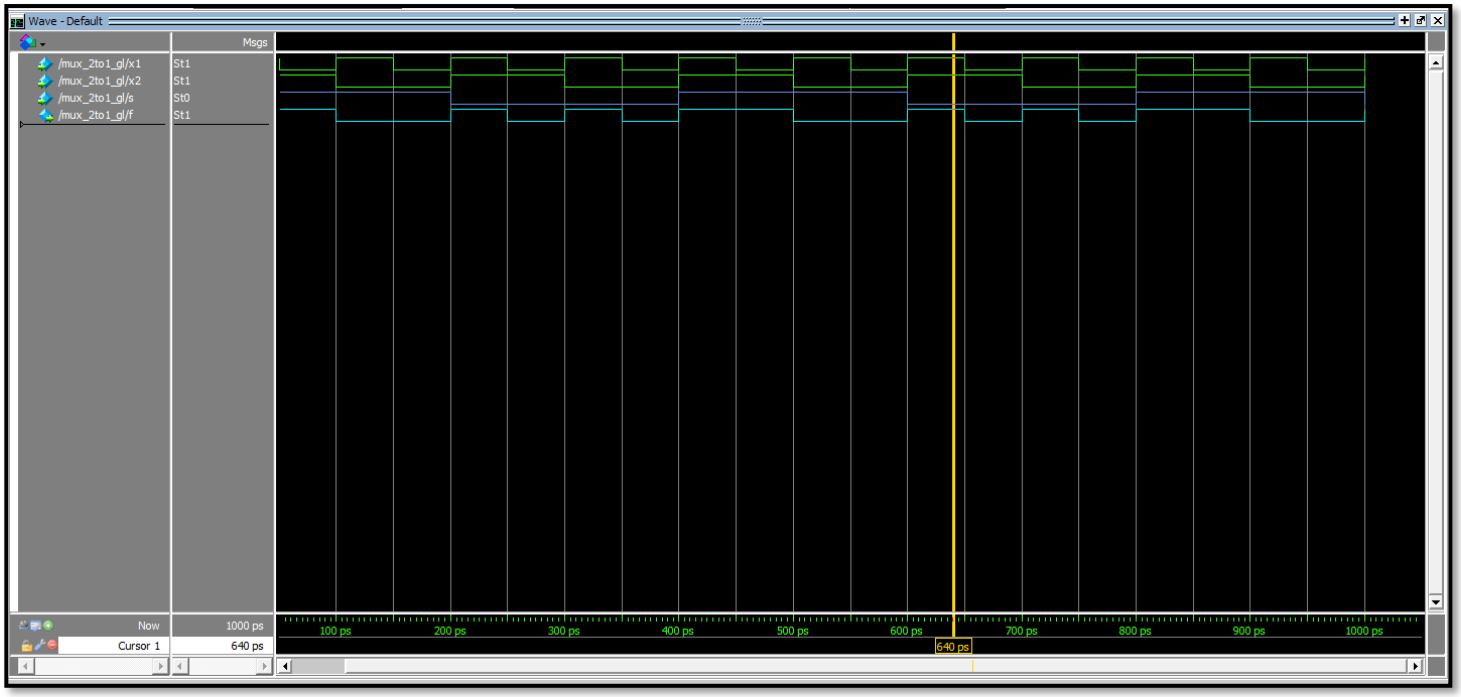
```
`timescale 1ns / 1ps

/*Hossam Ahmed Seyam*/
/*This code is illustrating How to design 2*1 mux in behavioral modelling */

module mux_2to1_bh1(x1, x2, s, f);

    input wire x1, x2 ,s;        // x1,x2 are mux inputs , s is the selector of the 2*1 mux
    output reg f;                //mux output

    always @(x1, x2 or s)
        begin
        if(s)
            begin
            f = x2;
            end
        else
            begin
            f = x1;
            end
        end
endmodule
```

```
`timescale 1ns / 1ps

/*Hossam Ahmed Seyam*/
/*This code is illustrating How to design 2*1 mux in behavioral modelling */

module mux_2to1_bh2(x1, x2, s, f);

    input wire x1, x2 ,s;        // x1,x2 are mux inputs , s is the selector of the 2*1 mux
    output reg f;                //mux output

    always @(x1, x2 , s)
        begin
        case(s)
            0: f = x1;
            1: f = x2;
            default: f = 0;
        endcase
        end
endmodule
```

Made By : Hossam Ahmed Seyam

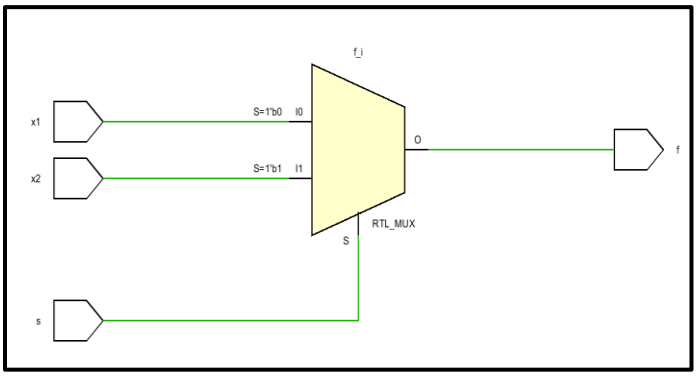
➢ Simulation:

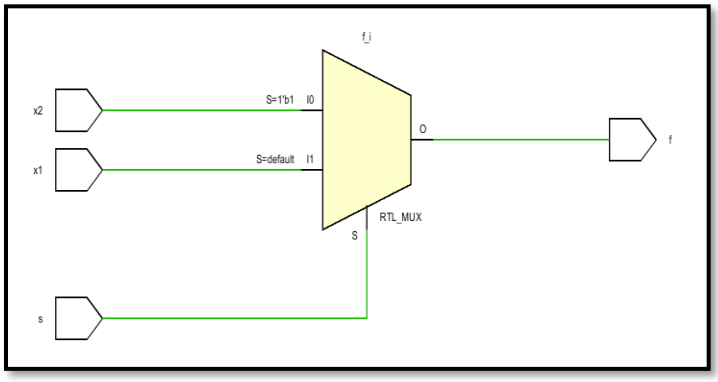
They give the same simulation results.



➢ Elaborated Design:

They give the same Elaborated Design.





➢ **About :**

Name : Hossam Ahmed Seyam

LinkedIn : https://www.linkedin.com/in/hossam-seyam-digital-design/

GitHub : https://github.com/HossamSeyam-Hub/Verilog_Projects

Made By : Hossam Ahmed Seyam