Novel Electromagnetic Bandgap Array Structure on Power Distribution Network for Suppressing Simultaneous Switching Noise and Minimizing Effects on High-Speed Signals

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***Abstract*—To supply high-speed digital circuits with stable power, power/ground noise, such as simultaneous switching noise (SSN) and ground bounce noise caused in multilayer printed circuit boards (PCBs) and packages need to be sufficiently suppressed. The electromagnetic bandgap (EBG) is widely recognized as a good solution for suppressing the propagation of SSN in the gigahertz range. However, a typical coplanar EBG structure etched onto the power and ground planes may degrade the quality of high-speed signals passing over the perforated reference plane. In this paper, a novel method of arranging EBG unit cells on both the power/ground planes in multilayer PCBs and packages is proposed, not only as a means of sufficiently suppressing the propagation of power noise, but also as a means of minimizing the effect of EBG-patterned reference planes on a high-speed signal. On the assumption that noise sources and noise-sensitive devices exist only in specific areas, the proposed method partially positions EBG unit cells only near these critical areas. The SSN suppression performance of the proposed structure is verified by conducting simulations and measurements in the time and frequency domains. Furthermore, signal quality is investigated to verify whether the proposed EBG-patterned reference planes are superior to conventional EBG-patterned planes in terms of signal integrity.**

***Index Terms*—Electromagnetic bandgap (EBG), power integrity (PI), signal integrity (SI), simultaneous switching noise (SSN).**

I. Introduction

GENERALLY speaking, a power distribution network (PDN) consisting of both a power plane and a ground plane (P/G) in multilayer printed circuit boards (PCB) and packages is used to deliver power to the core digital and analog/RF circuits in high-speed mixed mode systems. One of the major obstacles to build a stable PDN is known to be power/ground noise, such as simultaneous switching noise (SSN), ground bounce noise (GBN), and delta-I noise, which mainly occur in high-speed digital systems because of the rapid changes, which take place in the flow of current through an inductive PDN within a very short period of time. As such, SSN is mainly generated by fast switching devices, such as a CPU chip connected to a PDN. SSN can excite the cavity resonance modes within the parallel-plate waveguide-type P/G planes found in multilayer PCBs and packages. The resonance modes generated by SSN are transferred outwardly through the P/G planes, and finally, affect the critical signal lines or other noise-sensitive analog/RF devices, as shown in Fig. 1. As a result, SSN can lead to significant problems with signal/power integrity (SI/PI) as well as electromagnetic interference (EMI) issues [1]–[3]. To build a stable PDN for high-speed digital systems, SSN in multilayer PCBs and packages should be significantly suppressed.

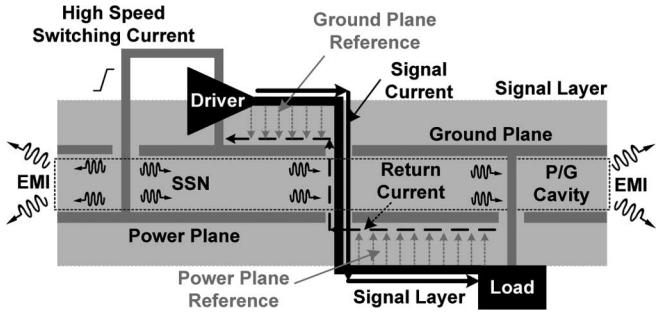

Fig. 1. Generation and propagation mechanism of SSN in a high-speed multilayer package and PCB structure.

Various studies attempting to address the problem of SSN have been conducted by a number of researchers [1]–[5]. Recently, electromagnetic bandgap (EBG) structures have been proposed as a solution capable of sufficiently eliminating SSN. In the initial stage of EBG-related studies, a forbidden frequency band was achieved using mushroom-shaped EBG structures [6]–[8]. However, these multilayer EBG structures with blind vias are difficult to implement using a conventional package and PCB manufacturing process. Furthermore, they require an additional layer to achieve the EBG patches, thereby making the EBG structures an expensive solution. To overcome the mechanical defects of these multilayer EBG structures, coplanar EBG structures [9]–[14], which are single-layer EBG structures, were proposed. However, P/G planes with slots etched periodically to form coplanar EBG structures could degrade the signal quality in the high-speed system because of the imperfect reference plane [15]–[18]. Thus, to remove this defect of the

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coplanar EBG, the ground plane was kept continuous and the EBG pattern etched only onto the power plane in order to reduce the effect of a discontinuous EBG-patterned reference plane on the return path of the current from the SI point of view [9], [10]. However, the return currents of high-speed signals do not always use the ground plane, as shown in Fig. 1. Strictly speaking, they always use the path of least impedance as the return path, so sometimes the power plane may be used as the current's return path. In this case, the quality of the signals may significantly deteriorate due to the EBG-patterned power plane [15]–[18].

In this paper, a novel array method of locating EBG unit cells partially on both the power and ground planes is proposed for multilayer PCBs and packages, it not only sufficiently eliminates the propagation of SSN, but also minimizes the effect of EBG-patterned reference planes on high-speed signals. Actually, most SSN is generated by devices, which use a fast clock, such as the CPU chip, and critical noise-sensitive analog/RF devices generally tend to be located in a specific area. On the assumption that these noise sources and noise-sensitive devices exist only in specific areas, the proposed method partially arranges EBG unit cells only near the critical areas. In this case, an EBG unit cell array located only partially in those critical areas of both P/G planes can sufficiently suppress SSN without any loss of signal quality in high-speed systems. In addition, the proposed structures can use the well-known filter property of EBG structures to broaden the forbidden frequency range by incorporating different sizes of EBG unit cells in the P/G planes [8]. The SSN suppression performance of the proposed structure is verified by conducting simulations and measurements in the time and frequency domains. Also, signal quality is investigated to verify that the proposed EBG-patterned reference planes are superior to conventional EBG-patterned planes in terms of SI.

II. Design of Novel EBG Arrangement

A. Effect of Partial EBG Structure

The EBG structures have periodic structures in which the propagation of electromagnetic waves is forbidden in certain frequency bands. Concerning the microwave region, the coplanar-type EBG structures [9]–[14] can be considered as a combination of lots of filters [19]. A couple of bridges and gaps function as a parallel *LC* resonance circuit, or bandstop filter. And a series of square patterns and narrow bridges function as a stepped-impedance low-pass filter [20]. The combination of them suppresses the propagation of the surface wave in the broad frequency range, aptly named the stopband.

Generally, P/G plane pairs are embedded in the substrate of multilayer PCB and package structures. In the conventional coplanar EBG structure [9], [10], the ground plane is kept continuous and the EBG pattern is etched onto only the power plane. However, in this paper, both planes are used to partially locate the EBG unit cells in a specific area in order to prevent the propagation of SSN generated by noisy digital devices and to protect the noise-sensitive devices. Furthermore, signal quality can be improved in comparison with conventional coplanar EBG methods because the solid part on each side of the power and ground planes is suitable for use as the stable return current path for high-speed signals.

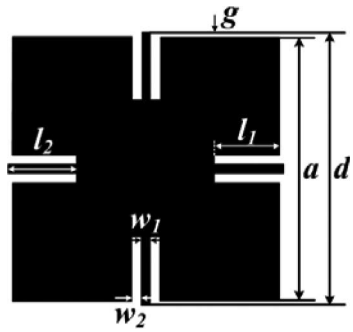

Fig. 2. Coplanar EBG unit cell structure and parameters.

TABLE I
Unit Cell's Structural Parameters and Their Values

Parameter	d	a	g	l_1	l_2	w_1	w_2
Small Unit Cell	30	28.5	1	6.5	7.5	1.5	1.5
Large Unit Cell	60	58	1	14	15	2	2

TABLE II
Effect of the Number of EBG Cells on Noise Suppression Property

Number of Unit Cell	-30dB Bandgap [f_{min} -f_{max}] [GHz]	Average Suppression Level [dB]
1	1.95 [1.36 – 3.31]	-39.5
2	3.36 [0.99 – 4.35]	-57.9
3	3.51 [4.58 – 1.07]	-75.6
4	3.49 [4.59 – 1.1]	-99.7

Next, we investigated the effect of the number of EBG unit cells on the noise suppression property in order to obtain the design guidelines for the partial EBG structure. The main objective of this study is to investigate the effects of the partially located EBG unit cells on both the P/G planes only near the noise source and the noise-sensitive devices. Thus, a well-known coplanar EBG unit cell [9], [10] was used, as shown in Fig. 2. The structural parameters and their values are shown in Table I. The dimensions of the two-layer PCB were 180 mm $\times$ 180 mm, with a 1.0 mm FR4 ($\varepsilon_r = 4.5$) substrate.

As the number of EBG unit cells between the observation ports was increased, the noise suppressing characteristic was examined by 3-D simulation. From Table II, it was confirmed that as the number of EBG unit cells increased, the average suppression level could be magnified while the suppression frequency band was equally maintained. That is, the average noise suppression level within the stopband increased by about 15$\sim$20 dB as the number of EBG unit cells existing between the observation ports increased. Consequently, it was confirmed from the simulation results that the EBG structure partially located on the P/G plane with 2$\sim$3 unit cells between the observation points could be said to be the optimum EBG application method, it cannot only sufficiently eliminate the propagation of SSN, but also minimize the effects of the EBG-patterned reference planes on high-speed signals.

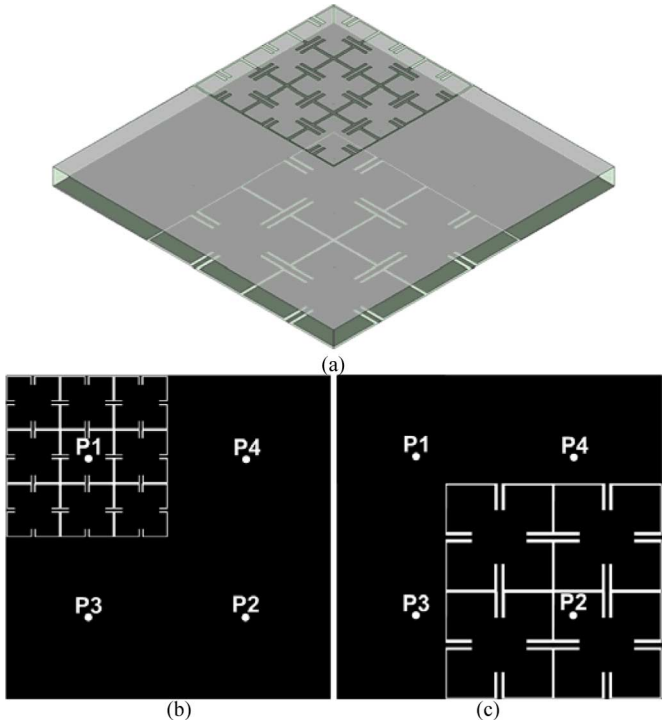

Fig. 3. Proposed EBG unit cell array on both the power and ground planes. (a) 3-D view, partial EBG array with (b) small unit cells etched onto the top layer, and (c) large unit cells etched onto the bottom layer.

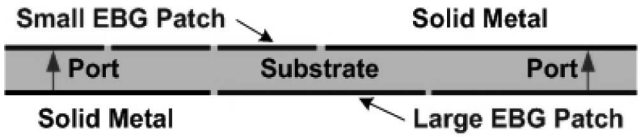

Fig. 4. Side view of partially positioned EBG unit cells on PCB.

B. Design Concept of Partial EBG Structure

Fig. 3 shows a 3-D view of the proposed EBG-patterned P/G planes. Fig. 3(b) and (c) shows the proposed partial placement of two differently sized EBG unit cells on the power and ground planes, respectively. As such, the proposed PDN structures, each with differently sized unit cells, were able to suppress SSN over a broadband frequency range equivalent to the superposition of each stopband, based on the filter theory and the fact that the EBG structures behave like a bandstop filter [8]. To more clearly illustrate the proposed structure, the side view of the PCB is shown in Fig. 4. The dimensions of the two-layer PCB are 180 mm $\times$ 180 mm, with a substrate thickness of 0.4 mm FR4 ($\varepsilon_r = 4.3$) substrate thickness.

For this study, four test samples were designed and fabricated to verify the performance of the proposed structure: a reference board without an EBG structure (Case 1), an EBG board whose entire power plane is filled with large EBG unit cells (Case 2), and small EBG unit cells (Case 3), respectively, and a partially placed EBG board on both planes (Case 4). As shown in Fig. 3, the four ports are located at P1 (45, 135, and 0 mm), P2 (135, 45, and 0 mm), P3 (45, 45, and 0 mm), and P4 (135, 135, and 0 mm), respectively. The origin point is located in the left-hand corner of the PCB, as shown in Fig. 3. These ports were used to evaluate the insertion loss of the structure between the ports by conducting a simulation and taking measurements.

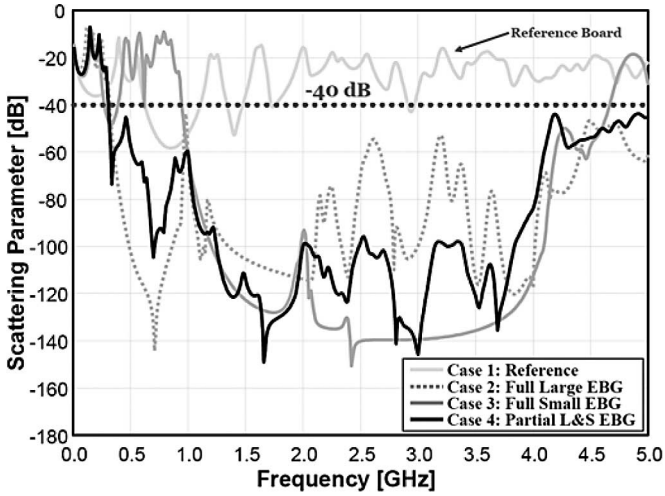

Fig. 5. Results of comparison of insertion loss S_{21} between the proposed EBG boards and the reference board by simulation.

III. Results of Simulation and Measurement

A. Frequency-Domain Analysis

First, the bandstop property of the proposed partially EBG-patterned P/G planes for eliminating SSN was investigated in the frequency domain.

Fig. 5 shows the simulated insertion loss S_{21} for the test PCB boards with EBG-patterned planes. The insertion loss of the reference board with solid power and ground planes is also included in Fig. 5 for comparison. A commercial 3-D full-wave EM simulator, high-frequency structure simulator (HFSS) (Ansoft, Pittsburgh, PA, U.S.A.) [21], was used to simulate the SSN behavior of the structures.

To verify the performance of the simulated structures, the two-layer PCB boards with the proposed EBG patterns were fabricated via a typical PCB process, as shown in Fig. 6. The fabricated test boards were fully EBG-patterned boards with small and large unit cells on the entire power plane, and a partially EBG-patterned board on both P/G planes with two differently sized EBG unit cells. Fig. 7 shows the results of the measurements S_{21} for the four PCB boards. A vector network analyzer (Agilent 8236B) was used to measure the scattering parameters among the ports. The measured insertion loss of the proposed structure shows a very wide bandgap with a sufficient degree of suppression. As shown in Fig. 7, the insertion loss within the bandgap reached the sensitivity limit ($-90\sim -100$ dB) of the vector network analyzer (VNA) used in a frequency range from 1.7 to 3.2 GHz.

As shown in Figs. 5 and 7, reasonable agreement was obtained between the measurements and the simulations. Because the exact values of the dispersion properties of the test PCBs were not considered in the simulation and some errors occurred in the measurement process, slight differences between the measured result and the simulated one are seen at higher frequencies. Also,

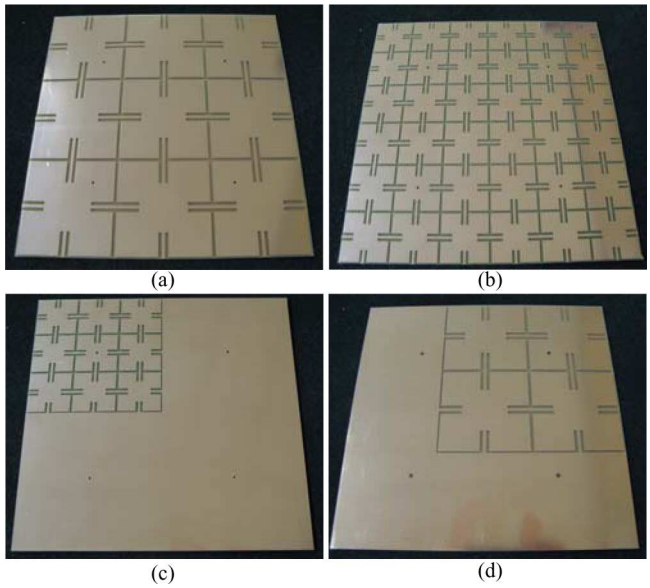

Fig. 6. Fabricated test boards with partial allocations of two differently sized EBG unit cells. Fully EBG-patterned power plane with (a) large unit cells (Case 2) and (b) small unit cells (Case 3), respectively, and a partially EBG-patterned board with (c) small EBG unit cells on the top layer (Case 4) and (d) large EBG unit cells on the bottom layer (Case 4), respectively.

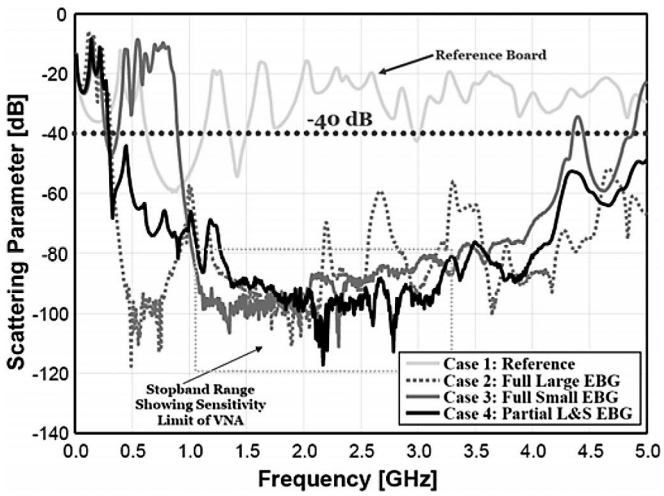

Fig. 7. Results of the comparison of insertion loss S_{21} between the proposed EBG boards and the reference board by measurement.

the discrepancy between the simulations and the measurements is due to the sensitivity limit of the vector network analyzer in the forbidden frequency range.

As shown in Figs. 5 and 7, the noise suppression property of the proposed P/G board with EBG unit cells partially located on both the power and ground planes superimposes the properties of the two differently sized EBG-patterned power planes. That is, the stop bandwidth of the proposed structure is equal to the sum of the stop bandwidth of each EBG unit cell structure, and the average level of suppression within the forbidden bandgap is higher than those of the other samples. From the figure, one can find that SSN is suppressed from 380 MHz to 5 GHz, which is almost the entire noise band defined in [7]

TABLE III
STOP FREQUENCY BANDWIDTH AND RATIO OF OCCUPATION

EBG Placement	Stop Freq. Band [GHz]		Ratio of Occupation
	Simulation	Measurement	
Full Large EBG	0.33~5.0 [4.67]	0.31~5.0 [4.69]	50 %
Full Small EBG	0.95~4.66 [3.71]	0.90~4.87 [3.97]	50 %
Partial EBG	0.32~5.0 [4.68]	0.29~5.0 [4.71]	34.7 %

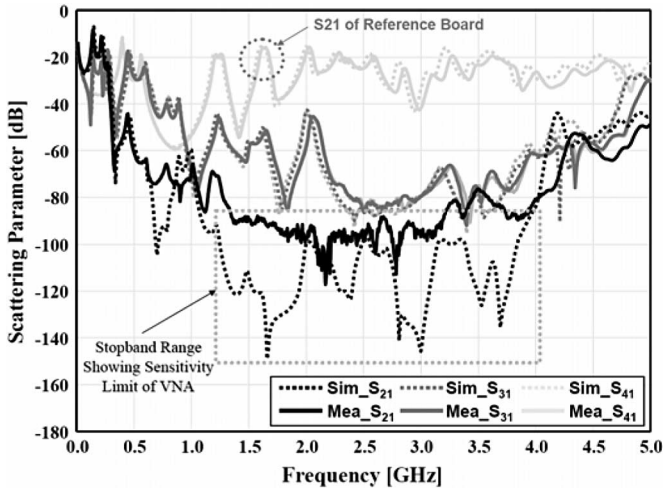

Fig. 8. Simulated and measured insertion loss in Case 4 (partial EBG model) for noise excitation located in different locations.

and [8]. The bandwidth in this study is defined by S_{21} lower than -40 dB.

In the PCB of Cases 2 and 3, only one side of the P/G planes (that is, the power plane) was used to adopt the EBG patterns, so the ratio of EBG unit cell occupation on both P/G planes was 50%. Although the proposed EBG structure uses only 34.7% of the entire power and ground planes, it can be confirmed based on the results of both simulation and measurement that the SSN suppression properties of the proposed structure can be improved as shown in Table III.

Fig. 8 shows the measured SSN suppression behavior in the case of the partially EBG-patterned model (Case 4) for the noise excitation ports located in different positions, i.e., Port 2, Port 3, and Port 4, respectively. The receiving port is Port 1. The insertion loss in Port 2 for the reference board, namely S_{21}, is also presented in this figure for comparison. Although the coplanar-type EBG unit cells do not exist in the positions of Ports 3 and 4, it can be seen in Fig. 8 that SSN was still suppressed over a wide noise band due to the small-sized EBG partially located on Port 1. Even if the noise source were located at Port 2, the SSN will be sufficiently suppressed at Ports 3 and 4 due to the large-sized EBG unit cells located on Port 2.

B. Time-Domain Analysis

Next, the SSN suppression characteristics of the proposed EBG-patterned PDN were investigated by carrying out a time-domain measurement.

Fig. 9 shows the experimental setup for a PI analysis in the time domain. To demonstrate the noise elimination

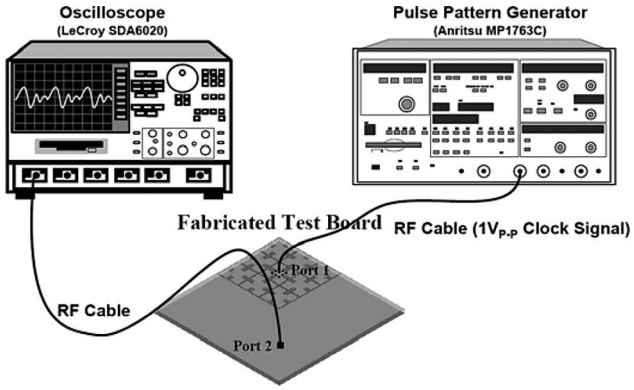

Fig. 9. Experimental setup for a time-domain analysis on power noise isolation of fabricated test boards.

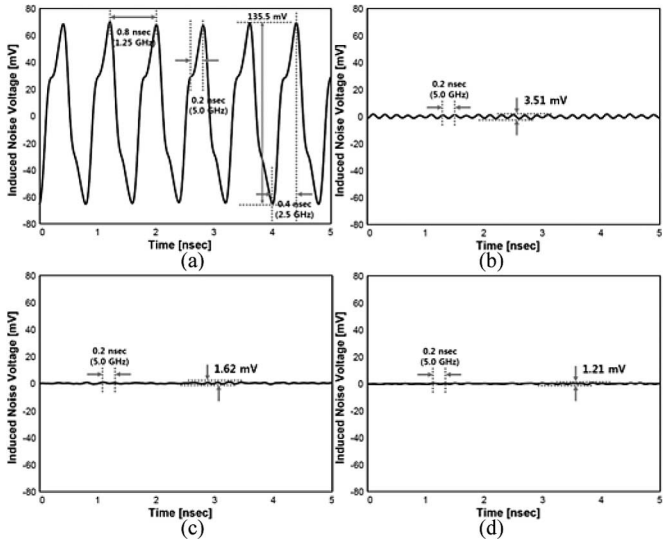

Fig. 10. Measured SSN waveforms at Port 2 with 1.25 GHz clock noise input at Port 1. (a) Reference board, fully EBG-patterned power plane (b) with small unit cells and (c) large unit cells, and (d) partially EBG-patterned P/G boards with small and large unit cells.

performance of the proposed partially EBG-patterned structures against broadband SSN, the P/G planes of the fabricated test boards were excited with 1 $V_{p\text{-}p}$, 1.25 GHz clock signals as a cavity noise source using a pulse pattern generator (Anritsu MP1763C) at Port 1, and the coupling noise at the receiving port (Port 2) was measured in the time domain using an oscilloscope (LeCroy SDA6020), as shown in Fig. 9. The induced noise voltages at Port 2 of all the test boards including the reference board were measured.

Before measuring the SSN waveforms, the results of the time-domain measurement of the 1.25 GHz clock noise based on the SSN suppression characteristics in the frequency domain were predicted. Since the 1.25 GHz clock signal was excited as a P/G noise, the frequency components of the coupled SSN waveform would be the harmonics of the 1.25 GHz clock. They were 1.25, 2.5, 3.75, and 5.0 GHz within 5 GHz.

First, the reference P/G plane without an EBG structure shows the high value of the SSN coupling ratio at all the fundamental and harmonic frequencies of the excited clock noise, as shown in Fig. 7. Therefore, the mostly coupled SSN noise for the reference plane will be 1.25, 2.5, 3.75, and 5.0 GHz. As shown in Fig. 7, all the fundamental and harmonic components of the fabricated EBG-patterned test boards had lower SSN coupling ratios. Therefore, one could easily predict that all SSN would be sufficiently suppressed in the proposed EBG-patterned boards. In the case of both fully EBG-patterned cases, it was observed that all fundamental and harmonic components had lower SSN coupling ratios, which are below –30 dB, as shown in Fig. 7, except the fourth harmonic component (5.0 GHz) in the full EBG-patterned board with small-sized unit cells. Therefore, one could predict that the mostly coupled SSN noise in the full EBG board with small-sized unit cells would be 5.0 GHz. In the case of the full EBG board with large unit cells, all SSN could be suppressed sufficiently. Finally, in the case of the proposed partially EBG-patterned structure on both the power and ground planes, it was observed that all components had lower SSN coupling ratios, which were below –50 dB, as shown in Fig. 7. Therefore, one could predict that all SSN would be suppressed for the proposed partially EBG-patterned PDN.

The observed coupled SSN waveforms in the time domain are compared in Fig. 10. For the reference P/G plane with no EBG structure, the coupled SSN waveform at Port 2 had a peak-to-peak voltage of 135.5 mV, and contained almost all the components of the excited clock noise. In the case of both the EBG-patterned boards, i.e., one with a small and one with a large unit cell on the entire power plane, the coupled SSN waveforms at Port 2 had a peak-to-peak voltage of 3.51 and 1.62 mV, respectively. And they mainly contained high-frequency (5.0 GHz) components.

By using the proposed EBG structures with small and large unit cells on both the P/G planes, all components of the clock signal were suppressed sufficiently below -50 dB, as shown in Fig. 7. In the case of the partially EBG-patterned board, the coupled SSN had a peak-to-peak voltage of 1.21 mV, with only a higher frequency component (5.0 GHz) with a period of 200 ps.

From the results of the measurement of SSN suppression in the time domain, it is clearly shown that the proposed partially EBG-patterned PCB with small and large unit cells on both the P/G planes is a better solution than any other structure.

In Fig. 11, the measured peak-to-peak magnitudes of the induced power noise are compared with the clock frequencies from 50 MHz to 5 GHz in steps of 50 MHz. Three test boards were used in these measurements, which are the fully EBG-patterned boards with small and large unit cells and the partial EBG-patterned board with both a small and a large unit cell. The reference board is measured for comparison. From the results, it is seen that power plane noise has a tendency to increase much more at the resonance-mode frequencies than at other frequencies, since the insertion loss S_{21} of the PDN becomes higher at the resonant modes.

Comparing the magnitude of peak-to-peak power noise propagated through the partial EBG board with that propagated through the reference board, much of the power plane noise is reduced over all frequencies owing to its broad bandgap. In the

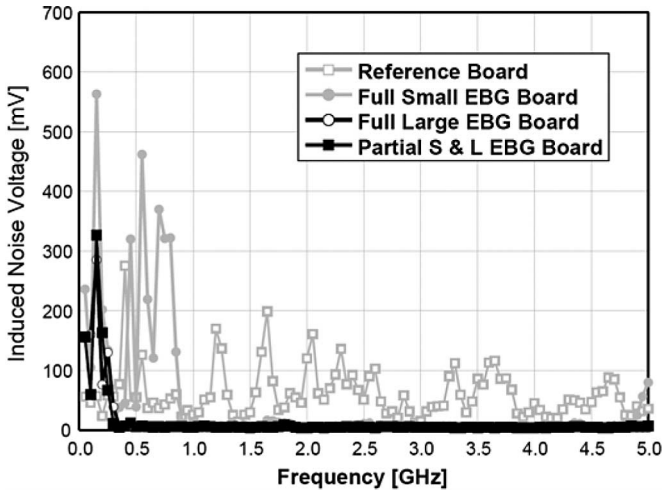

Fig. 11. Magnitude of peak-to-peak power plane noise with the clock frequencies.

case of the fully EBG-patterned board, the magnitude of peak-to-peak SSN is suppressed within the EBG's stopband, but the fully EBG-patterned board moves the resonance frequencies to a lower frequency range, which is outside the EBG's bandgap. Therefore, the full EBG board may make it worse at a lower frequency range than the proposed partial EBG board, as shown in Fig. 11. As shown in Fig. 11, the proposed partial EBG structure in this study provides a broader stopband than any other EBG-patterned boards, which used the entire power plane to array the EBG unit cells.

In the case of the partially EBG-patterned board, it has a sufficient noise suppression property in spite of the EBG structure being only partially located in a specific area of the entire P/G plane. That is, in the case of having the same SSN suppression performance, the partial EBG structure has an advantage in comparison with the full EBG structure in terms of SI. If the solid portion of the partially EBG-patterned PDN is used as the return current path for a high-speed signal, SSN can be sufficiently suppressed, and the signal quality can be improved further than in the case of the fully EBG-patterned PDN.

C. Effect on Signal Quality

Although a P/G plane with typical coplanar EBG unit cells demonstrates wideband suppression of SSN with a cost-effective design using only two metal layers, P/G planes with slots etched periodically to form coplanar EBG structures could degrade the signal quality in a high-speed system because of the imperfect reference plane.

To verify that the quality of the high-speed signal passing over the proposed P/G planes with an EBG unit cell array partially located on both the power/ground planes is superior to that of the conventional full EBG boards, the four-layer test boards with a signal line and transition via over the P/G planes were designed and fabricated, as shown in Fig. 12. The fabricated test boards are as follows: 1) reference board; fully EBG-patterned board on a power plane with 2) large unit cells; and 3) small unit cells; and 4) a partially EBG-patterned board with large and small unit cells on both the power and ground planes.

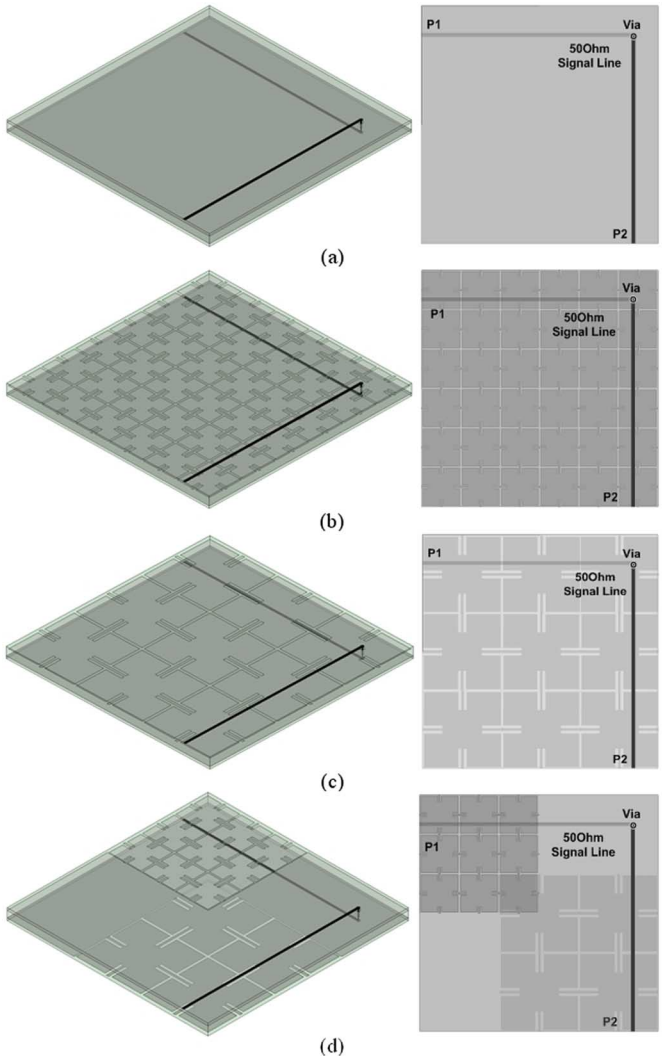

Fig. 12. 3-D and top view for four-layer test boards of signal line with via over EBG-patterned power/ground planes. (a) Reference board, full EBG board with (b) small EBG unit cells and (c) large EBG unit cells, and (d) partial EBG board on both P/G planes.

The four-layer stackup and via structure of the test boards are shown in Fig. 13, which consisted of a signal layer, a ground plane, a power plane, and a signal layer. A signal trace changes its reference from ground plane to power plane using a through-hole signal via, as shown in Fig. 13(b). To evaluate the effect of the EBG-pattern on signal quality, a 50-Ω signal trace of 315 mm passing over the EBG-patterned power plane was considered. Signal lines lie on both the top and bottom layers. The second and third layers are the fully or partially EBG-patterned power plane and the solid ground plane, respectively. The dimensions of the four-layer PCB were 180 mm $\times$ 180 mm, with a 1.4 mm FR4 ($\varepsilon_r = 4.5$) substrate.

An experimental setup in the time domain, as shown in Fig. 9, was used to evaluate the impact of the coplanar EBG-patterned power plane on the quality of the signal, referring to the perforated reference plane. To obtain the eye pattern diagram, the

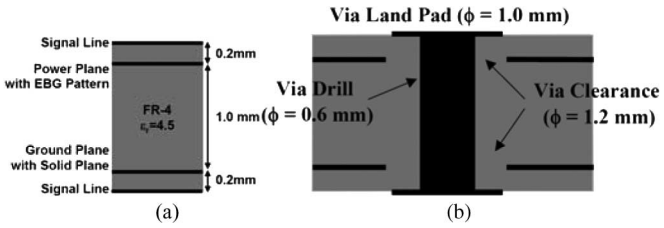

Fig. 13. Four-layer structure with signal line over EBG-patterned board. (a) Stackup. (b) Via structure.

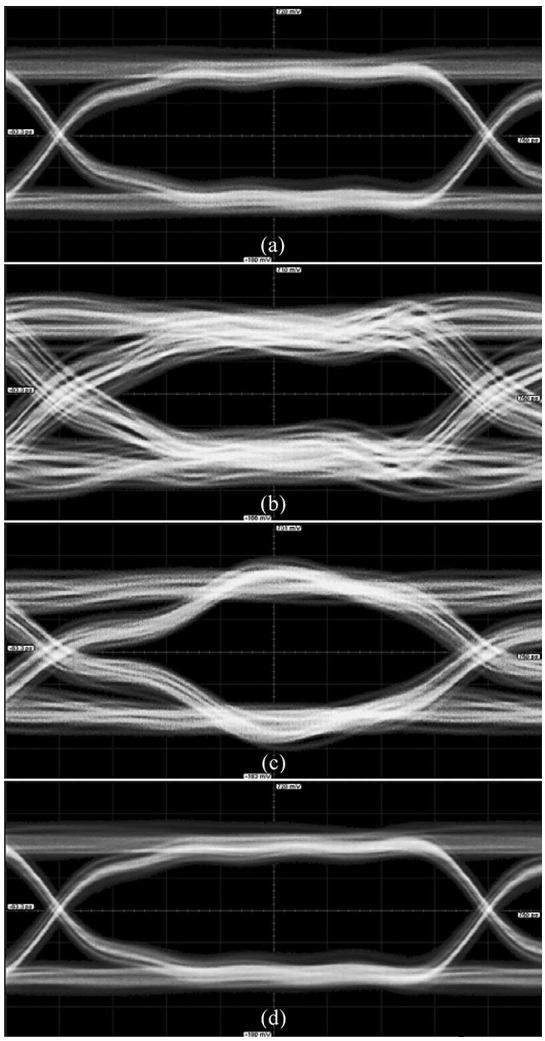

Fig. 14. Measured eye patterns for signal line with $2^7 - 1$ PRBS, NRZ, coded at 1.5 GHz. (a) Reference board. Fully EBG-patterned board with (b) large unit cell and (c) small unit cell. (d) Partially EBG-patterned board with large and small unit cells.

pattern source of 2^7–1 pseudorandom bit sequence (PRBS), nonreturn to zero (NRZ), coded at 1.5 GHz was launched at Port 1 with a pattern generator (Anritsu MP1763C). The bit-sequence swing and the nominal rise/fall time were 500 mV and 120 ps. When launching a pattern source, the eye patterns were measured at the output port (Port 2) with an oscilloscope (LeCroy SDA6020).

Fig. 14 shows the measured eye patterns for the signal quality analysis. In this study, two parameters, maximum eye open (MEO) and maximum eye width (MEW), are used as the metrics of the quality of the eye pattern. Fig. 14(a) shows the measured eye patterns for the reference board with a continuous power plane for comparison. MEO and MEW for the reference board were 352.13 mV and 618.0 ps, respectively. Fig. 14(b) and (c) shows the eye patterns for a fully EBG-patterned PCB board with small and large EBG unit cells. MEO and MEW were 253.85 mV and 464.9 ps for the fully EBG-patterned board with large unit cells, as shown in Fig. 14(b), and 365.46 mV and 516.5 ps for the fully EBG-patterned board with small unit cells, as shown in Fig. 14(c). The degradation of the MEO and MEW for the fully EBG-patterned board with large unit cells was about 27.9% and 24.8%, respectively.

The degradation of the MEO and MEW for the fully EBG-patterned board with small unit cells was about –3.8% and 16.4%. These results show that as the length of the signal line passing over the EBG-patterned boards lengthened, the degradation of the signal quality increased.

The measured eye pattern for the proposed partially EBG-patterned board with small and large unit cells on both the power and ground planes is presented in Fig. 14(d). MEO and MEW for the proposed partial EBG board with small and large unit cells on both the power and ground planes were 350.33 mV and 618.0 ps, which were almost same as the reference board. Compared with the reference board, it is clearly seen that there was no severe degradation of the signal quality for the proposed partial EBG board. Therefore, when the proposed partially EBG-patterned board was used in high-speed digital systems, SSN could be sufficiently suppressed without any significant deterioration of SI.

IV. Conclusion

A novel array method of EBG unit cells located partially on both the power and ground planes is proposed for multilayer PCBs and packages; it not only sufficiently suppresses the propagation of SSN, but also minimizes the effect of the EBG-patterned reference plane on high-speed signals. Actually, most SSN is generated by devices, which use a fast clock, such as the CPU chip, and noise-sensitive analog/RF devices are generally located in a specific area. On the assumption that these noise sources and noise-sensitive devices exist only in specific areas, the proposed method partially arranges the EBG unit cells only near the critical areas. In this case, the EBG unit cell array partially located only in those critical areas of both the P/G planes can sufficiently mitigate SSN without any loss of SI. The SSN suppression performance of the proposed structure is verified by simulations and measurements in the time and frequency domains. Also, the quality of signal is investigated to verify that the proposed EBG-patterned reference planes offer superior signal quality compared to conventional EBG-patterned planes.

Compared with the reference board and conventional EBG-patterned boards, it is clearly seen that the proposed partially EBG-patterned PDN structure not only suppresses SSN with a broader forbidden frequency range, but also provides a continuous return current path to eliminate SI problems. Therefore,

when the proposed partially EBG-patterned board is used in high-speed digital systems, SSN can be sufficiently suppressed without any significant loss of SI.

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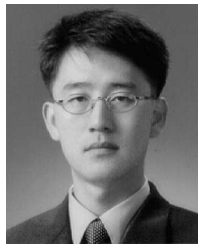

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