

Suppression of Wideband Simultaneous Switching Noise Through Application of a Partial Electromagnetic Band-Gap Structure in Multilayer Printed Circuit Boards

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Abstract—Adding mushroom-like electromagnetic band-gap (EBG) structures to split power planes can produce wideband suppression of ground bounce noise in high-speed printed circuit boards. Practical equations are used to estimate the stop-band performance of EBG structures within parallel power planes. In this article, a mushroom-like EBG and power-bus structure are derived using the modified nodal analysis (MNA) method. Equations calculated using the MNA method are easily programmable. The partial EBG structures developed in this article can suppress noise from electromagnetic (EM) interference within parallel plates in the power bus. Several examples below show that similar results can be obtained in measurements, in EM simulations software, and in derived equations. The proposed structure enhanced the suppression of simultaneous switching noise coupling (≤ -40 dB) within the range of 260 MHz to 10 GHz.

Index Terms—Electromagnetic band gap (EBG), electromagnetic (EM) interference, modified nodal analysis (MNA), power integrity, signal integrity, simultaneous switching noise (SSN), split power plane.

I. INTRODUCTION

AS SHOWN in other studies [1]–[5], simultaneous switching noise (SSN) is a notable aspect of high-speed microprocessors, memory, data buses, mixed-signal systems, integrated sensors, and radio frequency circuits in printed circuit boards (PCBs). In this article, we added decoupling capacitors between the power and ground planes to suppress SSN. To overcome the limitations of the decoupling capacitor, we used a power island array ground and split the power plane.

Although use of a decoupling capacitor is a practical method of inhibiting SSN, noise suppression within the high-frequency

range is often restricted to a maximum of 100 MHz owing to resistance and parasitic inductance. Because of increases in data rates and operating frequencies, the SSN spectral range spans through megahertz and gigahertz frequencies. SSN originates from active components attached to those power/ground planes that are the original sources. When digital signals are in the process of switching, SSN reduces the noise margin and degrades system performance.

Wideband SSN suppression through the application of mixed-mode systems has been demonstrated; simulation electromagnetic (EM) and prediction emphasize the forbidden band cut-off frequency of band-gap structures [1]. To realize wideband suppression within the gigahertz frequency range, researchers have tested the use of EM band-gap (EBG) structures, which apply high-impedance surfaces and stepped impedance [6], [7].

Our article is useful and practical. Based on results of the paper [14], the bandwidth of their EBG shape is narrower than ours. When the frequency is more than 6 GHz, the noise suppression cannot work well. Thus, the shape is fine, not particularly small. Their plane shape is round, but the round shaped plane is not easily practiced in real layout. Usually, the design of layout is divided into two planes in order to place components. Moreover, the effect is quite good, but its size (90 mm \times 90 mm) is bigger than the size of the plane (72 mm \times 72 mm) in this article [15]. Furthermore, its size (90 mm \times 90 mm) is also too big in the paper [16]. In fact, the round shaped plane is not commonly practiced in real layout.

In the article [11], we use the segment method to model the whole structure. Thus, the disadvantage of modeling is that we had to derive the equations without using computers in order to complete the computer programs. In this article, we combine the results with the paper in [12] and use the modified nodal analysis (MNA) to describe the segment method. By applying the MNA method, we can operate the whole derivation process into the computer programs. Moreover, we can input the structure description to produce the MNA matrix that can stimulate the final result.

In this article, we used a partial EBG structure and a Z-shaped power bus in multilayer PCBs to suppress wideband SSN. We then derived a circuit model using the MNA method to replace the transmission line equivalent for a single unit cell or cavity.

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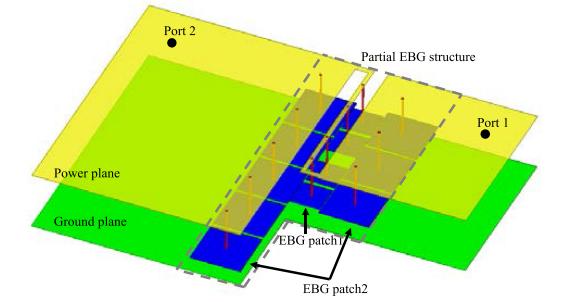


Fig. 1. (a) PCB structure. (b) Segmentation method.

The MNA method can efficiently calculate the result of optimal proximity.

II. USING THE SEGMENTATION METHOD TO ANALYZE PARTIAL EBG STRUCTURES AND Z-SHAPED POWER BUSES

The partial EBG structure shown in Fig. 1(a) contains partial EBG patch1, EBG patch2, and a Z-shaped power bus, all of which are located in the center of the arbitrarily shaped power/ground plane. Moreover, EBG patch1 and EBG patch2 are combined with the Z-shaped power bus in a PCB. We conducted a literature review for analysis [5], [10], [11]. As indicated in Fig. 1(b), we divided the PCB structure into five segments. Segment 3 includes the Z-shaped power bus and the EBG patch1 structure. Segments 2 and 4 contain EBG patch2. Segments 1 and 5 exhibit two rectangular cavities. The current source is located in segments 1 and 5. Two measurement ports,

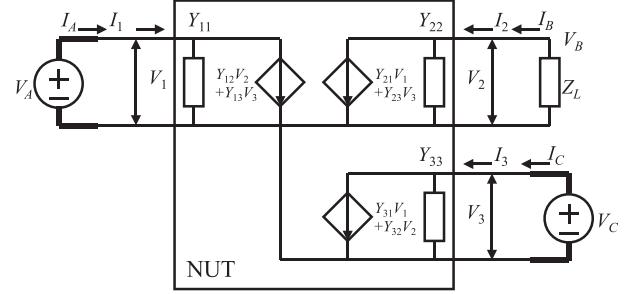


Fig. 2. One component connected at port 2.

namely p_1 and t_6 , represent ports 1 and 2, respectively. Thus, the ports between segments were named “p,” “q,” “r,” “s,” and “t.”

III. IMPEDANCE MATRICES OF SEGMENTS AND MNA

A relevant study [10], [11] employed segmentation for the cavity of a PCB and EBG structure using multiple formulas. Although impedance can be calculated, finding the solution is not easy. For segments 1 and 5, we used the double summation equation [9] to calculate the impedance matrix.

A. Modified Nodal Analysis

To analyze the structure, we employed the MNA method [12], [13]. As demonstrated in Fig. 2, the network under test contained three ports; two were used to measure impedance, and the other was used to connect one external component.

In the network under test, we used ports 1 and 3 to measure impedance. The results are represented by the \mathbf{Y} parameter matrix. To connect with port 2, we deployed an external component (e.g., discrete capacitor). Next, we adopted double summation (1) to calculate the \mathbf{Z} parameter matrix using the formula $\mathbf{Y} = \mathbf{Z}^{-1}$ and then transformed the outcome into the \mathbf{Y} parameter matrix. Meanwhile, external components were analyzed using the MNA method.

We adopted Kirchhoff’s current law to derive each nodal. During calculation of the overall \mathbf{Y} parameter matrix, $\mathbf{Z} = \mathbf{Y}^{-1}$ was transformed into the \mathbf{Z} parameter matrix

$$Z_{ij} = \frac{j\omega\mu h}{W_x W_y} \sum_m \sum_n \frac{C_m C_n P_{mn}(x_i, y_i) P_{mn}(x_j, y_j)}{k_{xm}^2 + k_{yn}^2 - k^2}$$

$$k_{xm} = \frac{m\pi}{W_x}, \quad m = 0.. \infty$$

$$k_{yn} = \frac{n\pi}{W_y}, \quad n = 0.. \infty$$

$$C_m C_n = \begin{cases} 1, & \text{if } m = 0, \quad n = 0 \\ 2, & \text{if } m \neq 0, \quad n = 0 \\ 2, & \text{if } m = 0, \quad n \neq 0 \\ 4, & \text{if } m \neq 0, \quad n \neq 0 \end{cases}$$

$$\begin{aligned} P_{mn}(x, y) = & \cos(k_{xm} T_x) \sin c \left(\frac{k_{xm} L_x}{2\pi} \right) \\ & \times \cos(k_{yn} T_y) \sin c \left(\frac{k_{yn} L_y}{2\pi} \right) \end{aligned} \quad (1)$$

where

W_x and W_y are the width and height of the rectangular cavity, respectively,

h is the thickness of the PCB substrate,

μ is the permeability of the PCB substrate,

k is the wavenumber of the PCB substrate, and

ω is the operating frequency.

$$\begin{aligned} Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3 - I_1 &= 0 \\ Y_{21}V_1 + \left(Y_{22} + \frac{1}{Z_L}\right)V_2 + Y_{23}V_3 &= 0 \\ Y_{31}V_1 + Y_{32}V_2 + Y_{33}V_3 - I_3 &= 0 \\ V_A = V_1, V_C = V_3. \end{aligned} \quad (2)$$

Then, we obtained the following result:

$$\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & -1 & 0 \\ Y_{21} & Y_{22} + \frac{1}{Z_L} & Y_{23} & 0 & 0 \\ Y_{31} & Y_{32} & Y_{33} & 0 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ V_A \\ V_C \end{bmatrix} = \mathbf{Ax} = \mathbf{z}. \quad (3)$$

We shortened $\mathbf{Ax} = \mathbf{z}$ so that $\mathbf{x} = \mathbf{A}^{-1}\mathbf{z}$. In (3), \mathbf{x} symbolizes the unknown current and voltages that run through the voltage sources, and \mathbf{z} represents the independent voltages. A new component was then added to the power bus structure in the \mathbf{A} matrix. In other words, we incorporated component $1/Z_L$ into the equation so that the overall result of the Y parameter could be computed. We set $V_A = 1$ and $V_C = 0$ to calculate the \mathbf{x} vector as follows:

$$\text{Set } \begin{cases} V_A = 1 \\ V_C = 0 \end{cases} \Rightarrow \mathbf{x} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ I_1 \\ I_3 \end{bmatrix} = \mathbf{A}^{-1} \begin{bmatrix} 0 \\ 0 \\ 0 \\ V_A \\ 0 \end{bmatrix} = \mathbf{A}^{-1} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix}. \quad (4)$$

$Y_{11_overall}$ and $Y_{21_overall}$ were then computed as

$$Y_{11_overall} = \left. \frac{I_A}{V_A} \right|_{V_C=0}, \quad Y_{21_overall} = \left. \frac{I_C}{V_A} \right|_{V_C=0},$$

$$I_A = I_1, \quad I_C = I_3. \quad (5)$$

Next, we set $V_A = 0$ and $V_C = 1$ to compute $Y_{12_overall}$ and $Y_{22_overall}$ as

$$Y_{12_overall} = \left. \frac{I_A}{V_C} \right|_{V_A=0}, \quad Y_{22_overall} = \left. \frac{I_C}{V_C} \right|_{V_A=0},$$

$$I_A = I_1, \quad I_C = I_3. \quad (6)$$

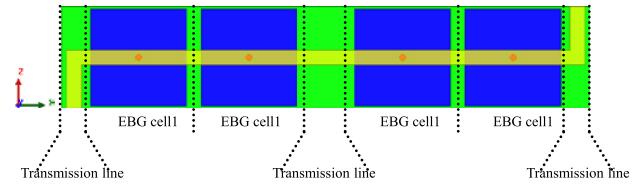


Fig. 3. Top view of the partial EBG structure and Z-shaped power bus.

B. Partial EBG Structure and Z-Shaped Power Bus

The segment 3 structure contained a transmission line and partial EBG. As displayed in Fig. 3, the EBG structure combined the Z-shaped power bus with vertical interconnect access (VIA).

In the EBG structure shown in Fig. 3, the transmission line with VIA was the power line. The bottom of the EBG cell and ground plane consisted of rectangular cavity B. Through the skin effect, the current passes through four edges of EBG cells. Next, we denoted ports A1, A2, B1, B2, C1, and C2. In (7), \mathbf{Z}_A , which is the impedance matrix, is the transmission line with VIA and is computed using the ABCD matrix [10]. In the transmission line, γ exhibited the propagation constant, and Z_0 expressed the characteristic impedance. The impedance matrix of rectangular cavity B consisted of metal plates. Because two structures mean series-series configuration, we were able to use the \mathbf{Z} impedance matrix to calculate the result of the \mathbf{Z}_C impedance matrix easily

$$\begin{aligned} \mathbf{Z}_C &= \begin{bmatrix} \mathbf{Z}_{A,11} + \mathbf{Z}_{B,11} & \mathbf{Z}_{A,12} + \mathbf{Z}_{B,12} \\ \mathbf{Z}_{A,21} + \mathbf{Z}_{B,21} & \mathbf{Z}_{A,22} + \mathbf{Z}_{B,22} \end{bmatrix} \\ \mathbf{Z}_A: \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix} &= \begin{bmatrix} \cosh(\gamma \frac{W_{cell1}}{2}) & Z_0 \sinh(\gamma \frac{W_{cell1}}{2}) \\ \frac{1}{Z_0} \sinh(\gamma \frac{W_{cell1}}{2}) & \cosh(\gamma \frac{W_{cell1}}{2}) \end{bmatrix} \\ &\times \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_{via}} & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma \frac{W_{cell1}}{2}) & Z_0 \sinh(\gamma \frac{W_{cell1}}{2}) \\ \frac{1}{Z_0} \sinh(\gamma \frac{W_{cell1}}{2}) & \cosh(\gamma \frac{W_{cell1}}{2}) \end{bmatrix} \\ Z_{B,ij} &= \frac{j\omega\mu h_1}{W_{patch1}^2} \sum_m \sum_n \frac{C_m C_n P_{mn}(x_{B,i}, y_{B,i}) P_{mn}(x_{B,j}, y_{B,j})}{k_{B,xm}^2 + k_{B,yn}^2 - k^2}. \end{aligned} \quad (7)$$

Fig. 4 displays the result of using MNA to calculate the impedance matrix of EBG cell1. \mathbf{Y}_A refers to transmission line A shown in Fig. 5, \mathbf{Y}_B represents LVia, \mathbf{Y}_C corresponds to transmission line C, \mathbf{Y}_D represents cavity B, and \mathbf{Y}_E is the additional virtual resistance for avoiding a singular matrix.

C. Modeling of EBG Structure

Segments 2 and 4 represent the EBG cell2 structure illustrated in Fig. 6. This structure consisted of cavity B and cavity A of VIA.

Fig. 7 displays the result of using MNA to calculate the impedance matrix of EBG cell2. \mathbf{Y}_A refers to cavity A shown in Fig. 6, \mathbf{Y}_B represents cavity B, \mathbf{Y}_C corresponds to LVia, and \mathbf{Y}_D is the additional virtual resistance for avoiding a singular matrix.

D. Measurement and Simulation

We employed three methods to verify whether the proposed model works well with the EBG structure and Z-shaped power

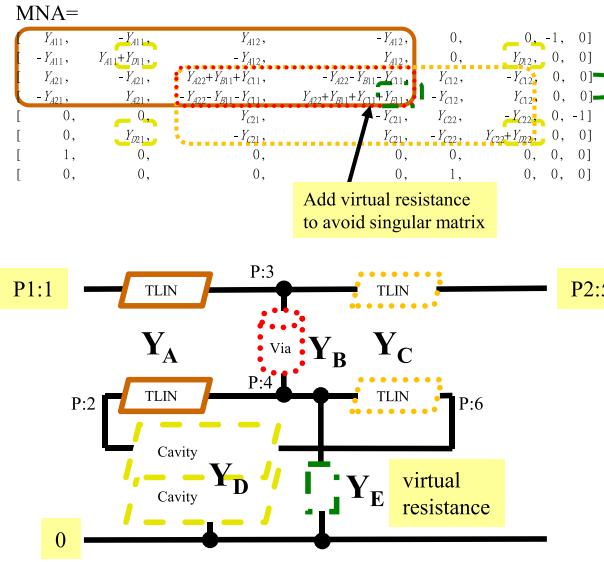


Fig. 4. MNA of EBG cell1.

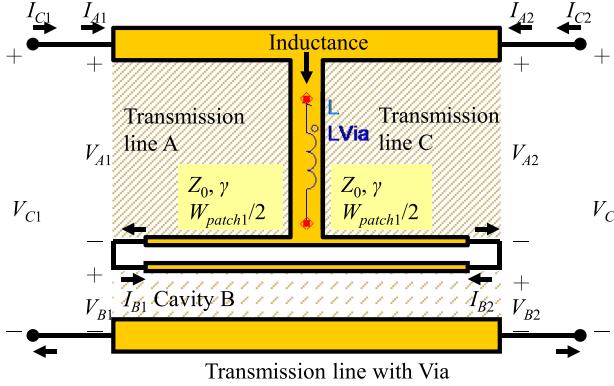


Fig. 5. Side view of the EBG cell1 structure.

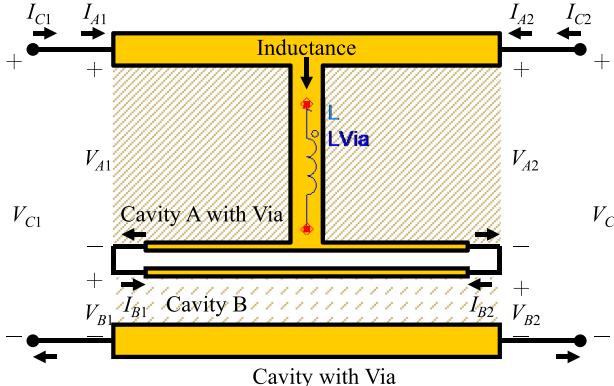


Fig. 6. Side view of the EBG cell2 structure.

bus. These three methods were measurement of a real board, HFSS EM software simulation, and the proposed model calculation. The reference test board conductance of copper was 5.88×10^7 S/m, and the dielectric material was FR-4 (dielectric constant of 4.4, and loss tangent value: 0.02). The structural size of the detailed simulation model is given in Table I, and Fig. 9

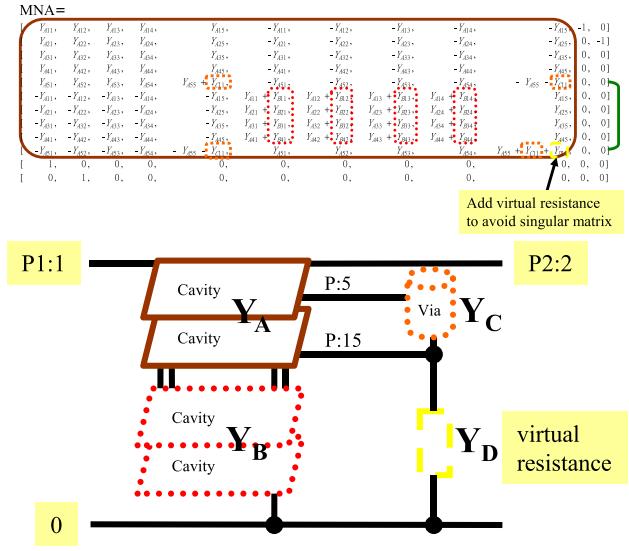


Fig. 7. MNA of EBG cell2.

TABLE I
MODEL DIMENSIONS AND DESIGN PARAMETERS

Dimensions and design parameters (unit: mm)			
W_{x_seg1}	13	W_{y_seg1}	22
W_{x_seg5}	21	W_{y_seg5}	36
W_{px_seg1}	5	W_{py_seg1}	4
W_{px_seg5}	19	W_{py_seg5}	12
W_{cell1}	4.2	W_{patch1}	4
W_{cell2}	7	W_{patch2}	6.8
W_L	0.6	t	0.018
h_1	0.1	h_2	0.9



Fig. 8. (a) Reference board. (b) PCB with Z-shaped power bus, EBG structure, and mushroom-like EBG on the parallel plate.

presents the simulation results. Within the range of 0.1–10 GHz, the noise-coupling effect was performed on S_{21} .

The model EBG structure and Z-shaped power bus were implemented for noise isolation in a multilayer PCB. Fig. 8(a) depicts the two-layer PCB for reference, and Fig. 8(b) reveals part of the EBG structure and Z-shaped power-bus schema, displaying incorporation of the PCB on a parallel plate.

As shown in the Fig. 9, larger deviations will occur when the measurement and the proposed model are more than 2 GHz. Because of using the gap model [17], [18] \mathbf{Z}_u to stimulate

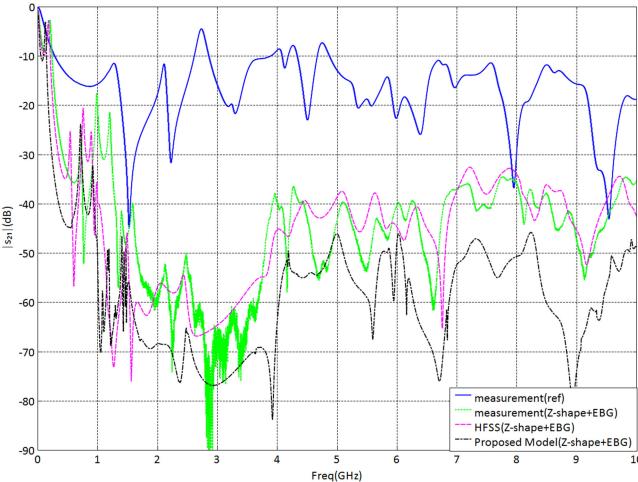


Fig. 9. Measurement and simulation results.

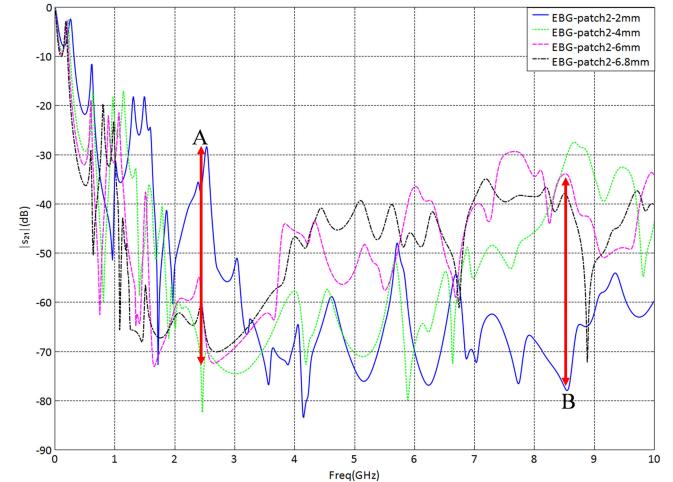


Fig. 10. Modified EBG patch size and simulation results.

(i.e., coupling effect between segment 2 and segment 4), we will get the bigger variation of the coupling coefficient in the high frequencies. However, the curvilinear trend is still similar. Based on the outcome displayed, the proposed model was able to reduce the ground bounce noise (GBN) S_{21} to ≤ -30 dB within the range of 940 MHz to 10 GHz and ≤ -20 dB within 260–940 MHz. In this experiment, we used an Intel(R) Core (TM) i7-4770S CPU with 32 GB of RAM to operate the simulation of HFSS15, which took 15 min to complete. Our proposed model uses a combination of Python and Cython programming languages to calculate the result, and requires only 90 s to complete. Moreover, we attempt to revise the EBG patch which is connected with the ground layer. The simulation result is similar to the EBG patch connected with the power layer. Therefore, this article will discuss the different combinations of EBG patches and power layers.

IV. APPLICATION OF THE MODEL FOR REGULAR STRUCTURE AND ADJUSTMENT

Implementing a local EBG structure and Z-shaped power bus into a multilayer PCB resulted in coupling noise isolation and high band noise suppression. We continued to use the structural element of the EBG structure and Z-shaped power bus to generate reproducible results.

A. Adjustment of EBG Patch Size

The model structure presented in Fig. 6 is based on the cavity model in [11] for adjustment of the number and size of EBG patch2 in the port 2 position. If the EBG patch size is excessive, a lump port cannot be incorporated into the structure. The simulation results of the Z-shaped power bus on both sides of the EBG patch are presented in Fig. 10.

According to the formula, the PCB thickness is fixed and the EBG capacitance increases (i.e., a greater EBG patch is used), causing the cut-off frequency to decrease. Evidently, the low

TABLE II
DIMENSIONS AND DESIGN PARAMETERS FOR VALIDATION OF THE $W_{2 \times 2\text{-cell}}$ MODEL

Dimensions and design parameters (unit: mm)			
$W_{\text{unit_cell}}$	21.2	$W_{2 \times 2\text{-cell}}$	46.6
W_{cell1}	4.2	W_{patch2}	6.8
W_L	0.6	T	0.018
h_1	0.1	h_2	0.9
W_{px1}	7	W_{py1}	7
W_{px2}	7	W_{py2}	7

frequency of isolation point A increased, whereas the high frequency of isolation point B decreased; therefore, no interference occurred for the EBG patch2 size and port 2 positions. We set the EBG patch2 size as 6.8 mm.

Following the aforementioned rule, we were able to adjust the EBG patch size between the PCB layout areas.

B. $W_{2 \times 2\text{-cell}}$ Model

As indicated in Table II, Figs. 11 and 12, we used HFSS EM simulation software to calculate the noise-coupling coefficient and compare S_{21} within the range of 0.1–10 GHz.

C. $W_{3 \times 3\text{-cell}}$ Model

As demonstrated in Table III, and Fig. 13, we modified the number of unit cells in the $W_{2 \times 2\text{-cell}}$ model to develop the $W_{3 \times 3\text{-cell}}$ model. We then used HFSS EM simulation software to compute the noise-coupling coefficient and compare S_{21} within the range of 0.1–10 GHz.

Fig. 14 displays the increase in the repeated structure, where noise isolation within the range of 1.1–10 GHz was improved to ≤ -45 dB; however, within the range of 270 MHz to 1.1 GHz, no improvement was observed in the repeated structure. Consequently, we attempted to adjust the size of EBG patch2 to improve low-frequency isolation.

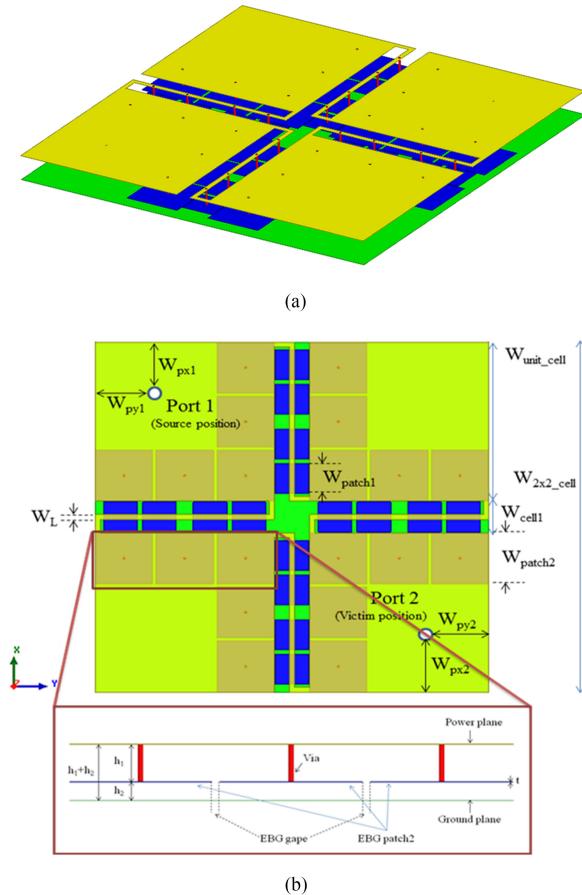


Fig. 11. Model structure. (a) Three-dimensional view of $W_{2X2\text{-}cell}$. (b) Top view and the EBG structure.

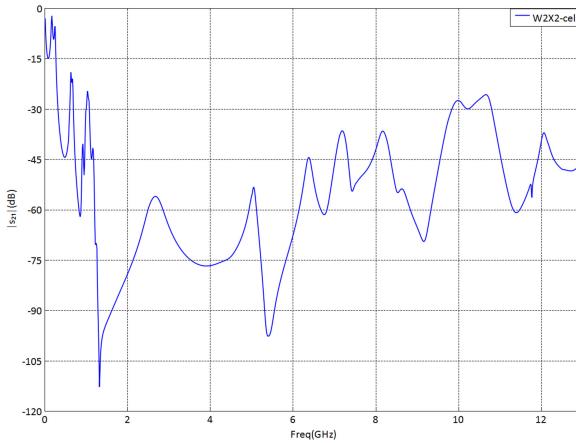


Fig. 12. Electromagnetic simulation of S_{21} for the $W_{2X2\text{-}cell}$ structural model.

D. $W_{2X2\text{-}cell}$ Model (EBG patch3: 10.4 mm)

As described in the preceding section, increasing the size of the structure did not improve noise isolation within the low-frequency range (270 MHz to 1.1 GHz). According to Section IV-A (*Adjustment of EBG Patch Size*) and as shown

TABLE III
DIMENSIONS AND DESIGN PARAMETERS FOR VALIDATION OF THE $W_{3X3\text{-}cell}$ MODEL

Dimensions and design parameters (unit: mm)		
W_{unit_cell}	21.2	$W_{3 \times 3_cell}$
W_{cell1}	4.2	W_{patch2}
W_L	0.6	t
h_1	0.1	h_2
W_{px1}	7	W_{py1}
W_{px2}	7	W_{py2}

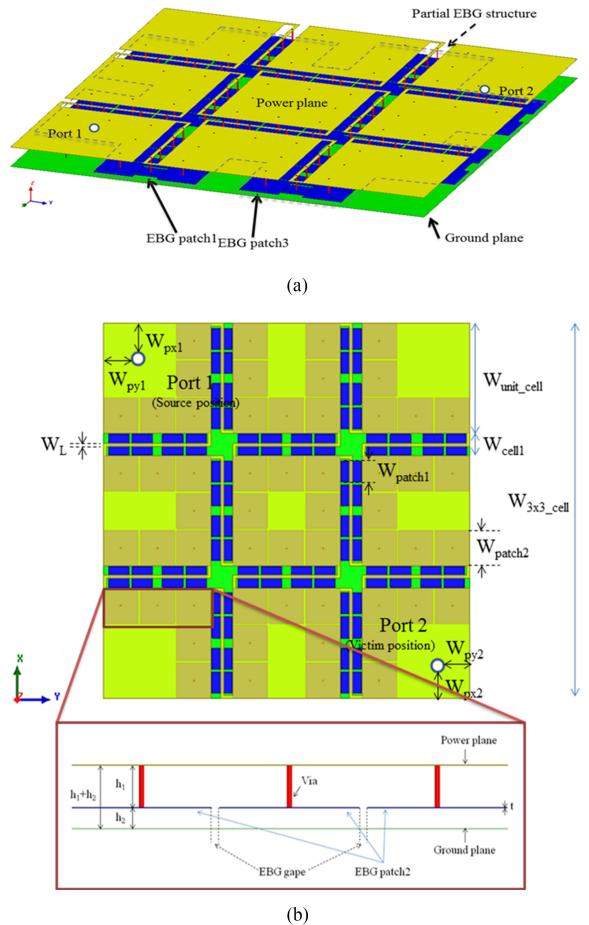


Fig. 13. Model structure. (a) Three-dimensional view of $W_{3X3\text{-}cell}$. (b) Top view and the EBG structure.

in Table IV, Figs. 15 and 16, we adjusted the EBG patch size of W_{patch3} from 6.8 to 10.4 mm to increase the capacitance and improve low-frequency noise isolation. Then, we used the noise-coupling coefficient S_{21} to compare noise isolation within the range of 0.1–20 GHz.

We implemented the $W_{2X2\text{-}cell}$ (EBG patch3: 10.4 mm) model into the practical element of the EBG and Z-shaped power bus for noise isolation in the multilayer PCB. Fig. 17(a) depicts the two-layer PCB for reference, and Fig. 17(b) displays part of the EBG and Z-shaped power-bus schema involving incorporation

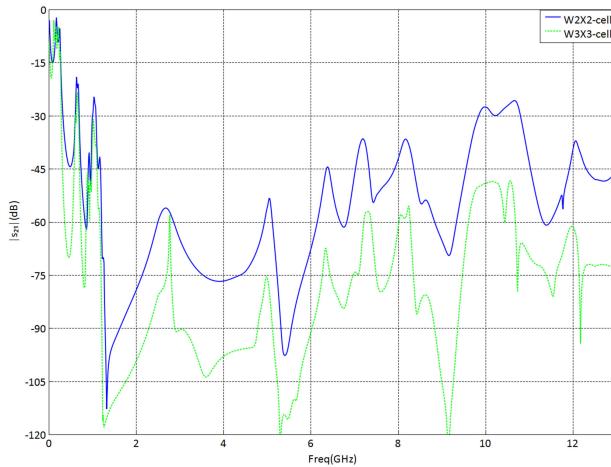


Fig. 14. Comparison of S_{21} electromagnetic simulation for the $W_{2\times 2}$ -cell and $W_{3\times 3}$ -cell structural model.

TABLE IV
DIMENSIONS AND DESIGN PARAMETERS FOR VALIDATION OF THE $W_{2\times 2}$ -CELL MODEL (EBG PATCH3: 10.4 mm)

Dimensions and design parameters (unit: mm)		
$W_{\text{unit_cell}}$	21.2	$W_{2 \times 2_cell}$
W_{cell1}	4.2	W_{patch3}
W_L	0.6	t
h_1	0.1	h_2
W_{px1}	5.2	W_{py1}
W_{px2}	5.2	W_{py2}

of the PCB on a parallel plate. The solid plate was used for FR-4 with a board thickness of 1 mm, dielectric constant of 4.4, and tangential loss of 0.02.

As demonstrated in Fig. 18, the proposed model reduced the GBN S_{21} to ≤ -30 dB within the range of 270 MHz to 10 GHz.

Moreover, $W_{2\times 2}$ -cell (EBG patch3: 10.4 mm) improved noise isolation within the range of 270 MHz to 1.1 GHz, achieving isolation of ≤ -25 dB.

E. $W_{3\times 3}$ -cell Model (EBG patch3: 10.4 mm)

As described in Section IV-C ($W_{3\times 3}$ -cell Model), we continued to increase the number of unit cells in the $W_{3\times 3}$ -cell model to compare its noise isolation coefficient S_{21} with those of the $W_{2\times 2}$ -cell model and reference board within the range of 0.1–10 GHz.

We implemented the $W_{3\times 3}$ -cell (EBG patch3: 10.4 mm) model into the practical element of the EBG structure and Z-shaped power bus for noise isolation of the multilayer PCB. Table V and Fig. 19(a) illustrates the two-layer PCB for reference, and Table V and Fig. 19(b) displays part of the EBG and Z-shaped power-bus schema involving incorporation of the PCB on a parallel plate. An image of the real board is presented in Fig. 20. The solid plate was used for FR-4 with a board thickness of 1 mm, dielectric constant of 4.4, and tangential loss of 0.02.

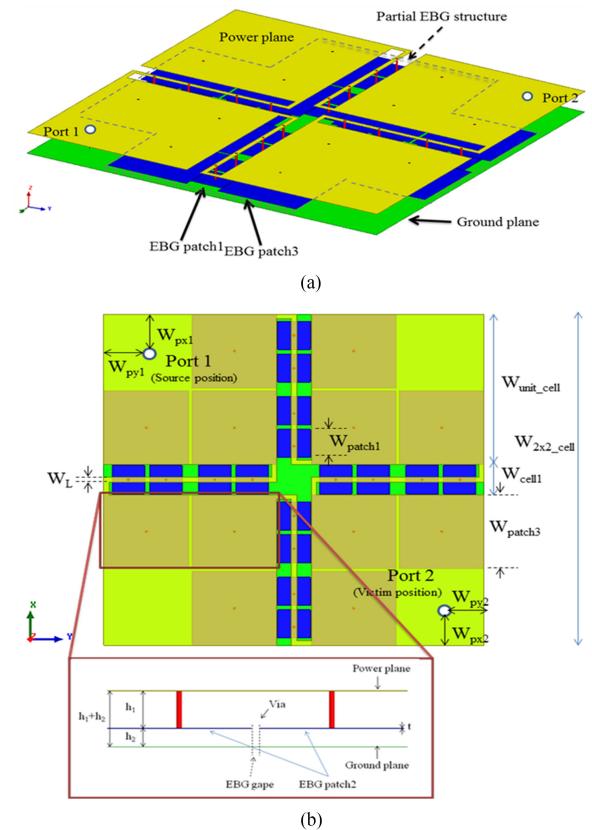


Fig. 15. Model structure. (a) Three-dimensional view of $W_{2\times 2}$ -cell (EBG patch3: 10.4 mm). (b) Top view and EBG structure.

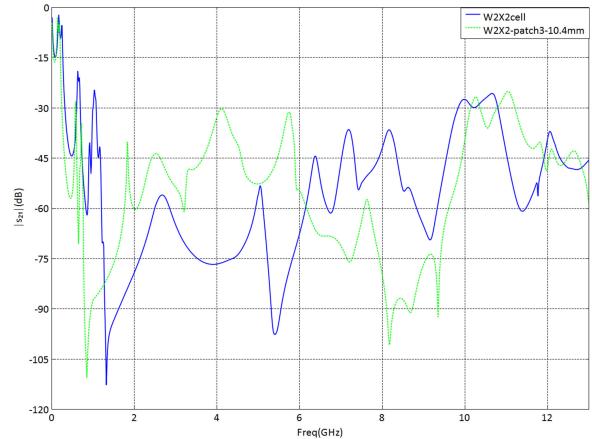


Fig. 16. Electromagnetic simulation of S_{21} for the $W_{2\times 2}$ -cell and $W_{2\times 2}$ -cell (EBG patch3: 10.4 mm) structural model.



Fig. 17. (a) Reference board. (b) PCB with Z-shaped power bus, parts of the EBG structure, and mushroom-like EBG on the parallel plate.

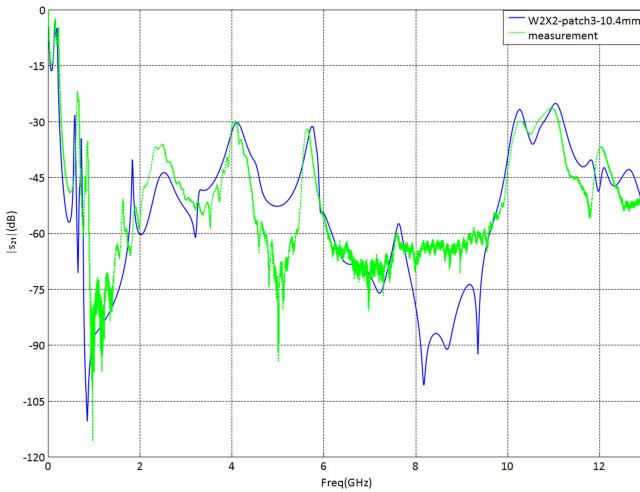


Fig. 18. Electromagnetic simulation and measurement result of S_{21} for the $W_{2 \times 2}$ -cell (EBG patch3: 10.4 mm) structural model.

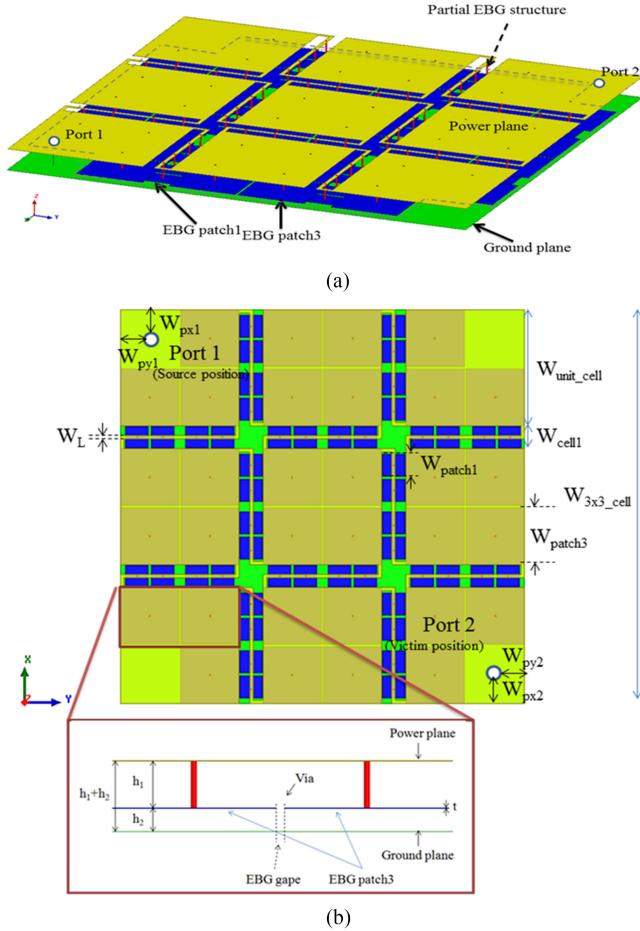


Fig. 19. Model structure. (a) Three-dimensional view of the $W_{3 \times 3}$ -cell (EBG patch3: 10.4 mm) model. (b) Top view and EBG structure.

Fig. 21 depicting the $W_{3 \times 3}$ -cell (EBG patch3: 10.4 mm) model indicates that within the range of 270 MHz to 1.1 GHz, noise isolation was improved to -40 dB. However, at 580 MHz, noise isolation was improved only to -37 dB.

TABLE V
DIMENSIONS AND DESIGN PARAMETERS FOR VALIDATION OF THE $W_{3 \times 3}$ -cell (EBG PATCH3: 10.4 mm) MODEL

Dimensions and design parameters (unit: mm)			
$W_{\text{unit_cell}}$	21.2	$W_{3 \times 3 \text{-cell}}$	72
W_{cell1}	4.2	W_{patch3}	10.4
W_L	0.6	T	0.018
h_1	0.1	h_2	0.9
W_{px1}	5.2	W_{py1}	5.2
W_{px2}	5.2	W_{py2}	5.2



Fig. 20. (a) Reference board. (b) PCB with Z-shaped power bus, parts of the EBG structure, and mushroom-like EBG on the parallel plate.

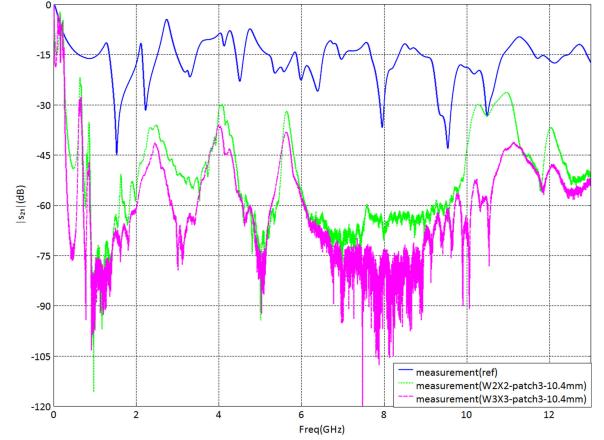


Fig. 21. Electromagnetic measurement of S_{21} for the $W_{3 \times 3}$ -cell (EBG patch3: 10.4 mm) structural model.

V. CONCLUSION

In this article, to enable the setting of individual models, the EBG structure and Z-shaped power bus were separated into five sections to verify whether the proposed method could reduce the calculation time and still provide accurate results. To lower manufacturing costs, we employed three PCB layers of the EBG structure and the Z-shaped power bus. Only a small area (EBG structure and Z-shaped power bus) was required to sufficiently decrease GBN.

We discovered that through the parallel programming designs in the MNA matrix calculator, the calculation speed could be increased. Furthermore, MNA could be incorporated into the segmentation method, and different shapes of discrete capacitors' power-bus structures could be calculated. By deducing the equation in advance, the original calculation could be maintained.

The EBG structure and Z-shaped power bus required only a small space and were able to suppress the GBN S_{21} to ≤ -30 dB within the range of 940 MHz to 10 GHz and ≤ -20 dB within the range of 260–940 MHz. Using repeated structures of differently sized PCBs, GBN suppression reached $S_{21} = -40$ dB within the range of 260 MHz to 10 GHz. Compared with other studies, this article was able to save more space. The proposed structure was completed through the incorporation of three PCB layers of the EBG structure and the Z-shaped power bus to reduce waste and cost.

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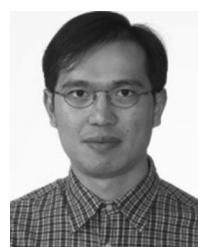
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