

## Charge Transport in Weakly Coupled CoPt<sub>3</sub> Nanocrystal Assemblies

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We report on charge transport through laterally contacted assemblies of weakly coupled, 10.2-nm-diameter CoPt<sub>3</sub> nanocrystals, where the shortest conducting paths consist of fewer than five nanocrystals. High-resolution electron microscopy reveals that the mean inter-nanocrystal separation can be reduced in situ through the use of mild thermal annealing without melting or sintering the nanocrystals. Devices annealed at 150 °C show measured resistances that are several orders of magnitude lower than that for unannealed assemblies, which is attributable to increased inter-nanocrystal tunneling. Variable-temperature dc electrical characterization demonstrates that these devices act as Mott insulators with transport characteristics governed by single-electron charging energies of the electrically isolated nanocrystals. Observed scaling behavior of low-temperature current–voltage characteristics indicates transport through current-carrying networks with dimensionality greater than two dimensions and also reflects the finite geometric disorder in the nanocrystal assembly.

### Introduction

Metal and semiconductor nanocrystals (NCs) with diameters in the range of 1–30 nm are the subject of intense research interest, because these materials can behave as “artificial atoms” or quantum dots, with size-dependent optical and electronic properties bridging those of bulk and molecular materials, e.g., plasmon resonances, single charge tunneling, and quantum confinement.<sup>1,2</sup> The unique self-assembly properties of organically passivated monodisperse nanocrystals offer the promise of artificial atom solids with novel electronic and/or optical properties. Developing a clear understanding of the roles of nanocrystal core size and polydispersity, and of inter-nanocrystal coupling, on the charge-transport characteristics of laterally contacted nanocrystal assemblies represents a critical step toward development of functional nanocrystal architectures with tunable properties.<sup>3–15</sup> Furthermore, the influence of array size and topology on the measured properties must also be considered, because contact effects as well as global and local geometric disorder also impact the electronic properties of each assembly.<sup>15</sup> To this end, we report on the visualization and dc electrical characterization of small assemblies of metal nanocrystals, where the shortest conducting paths contain less than five nanocrystals. We have developed a mild thermal annealing process to manipulate the inter-nanocrystal separation (and coupling) and, hence, control the electronic properties of each assembly while maintaining the structural integrity of the individual nanocrystals. The scaling behavior of low-temperature current–voltage (*I*–*V*) characteristics above the Coulomb Blockade threshold voltage indicates a charge-transport network with dimensionality greater than two dimensions and finite structural disorder.

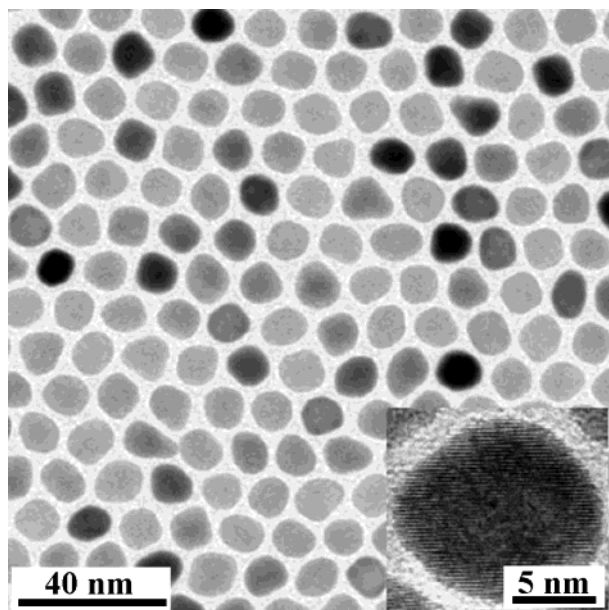
### Experimental Section

CoPt<sub>3</sub> nanocrystals, 10.2 nm in diameter and stabilized by 1-adamantanecarboxylic acid and hexadecylamine ligands, have been synthesized using a solution-phase method, as reported previously.<sup>16</sup> Briefly, CoPt<sub>3</sub> nanocrystals are formed via a modified “polyol” process in a high-boiling-point coordinating solvent.<sup>17</sup> During nanocrystal formation, platinum(II)-acetylacetonate is reduced by a long-chain 1,2-diol and cobalt carbonyl is thermally decomposed. The synthesis is performed using a standard Schlenk line technique under dry argon. As-synthesized nanocrystals are air-stable, monodisperse ( $\sigma = 9\%$ , without post-synthesis size selection), and highly crystalline, possessing a chemically disordered face-centered cubic (fcc) structure. Excess organic stabilizers are removed by addition of a nonsolvent (ethanol) to the nanocrystal solution, centrifugation of the precipitate, and redispersion of the resultant nanocrystal material in toluene. This purification procedure is repeated to ensure complete removal of excess stabilizers. Transmission electron microscopy (TEM) measurements are performed on a Philips model CM-300 microscope system (Philips Electronics N.V.). For measurements of electrical transport through nanocrystal assemblies, finger electrodes 85 nm in width with inter-electrode gaps of  $\sim 45$  nm are fabricated on thermally oxidized silicon wafer chips using electron beam lithography, followed by metal evaporation (Cr 5 nm/Au 25 nm) and liftoff. Multilayer nanocrystal assemblies are deposited between the electrodes by adding  $\sim 5$   $\mu$ L of the purified nanocrystal solution dropwise onto each electrode array under ambient conditions and allowing the solvent to evaporate slowly. Scanning electron microscopy (SEM) data are acquired using a field-emission SEM system (model JSM-6700F, JEOL U.K., Ltd.) operating at beam voltages of 1–10 kV. Post-deposition annealing is performed under reducing conditions (5% H<sub>2</sub>, 95% N<sub>2</sub> for 1 h) at temperatures up to 150 °C. In this regard, previous X-ray diffraction (XRD), TEM, and solubility studies have shown that

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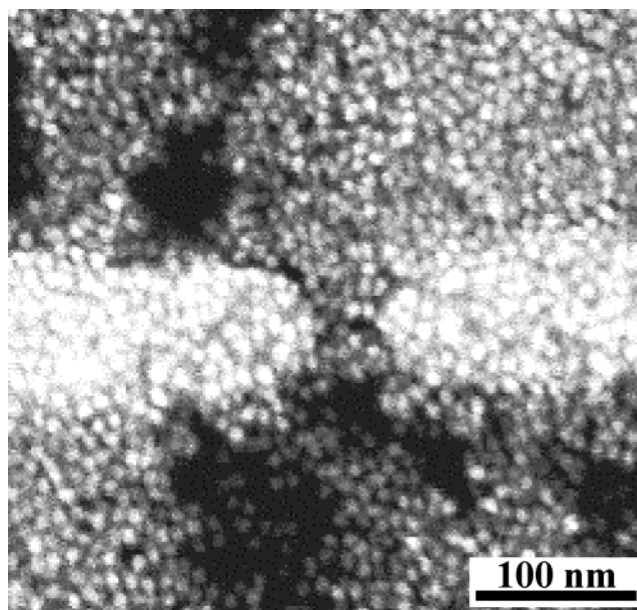
**Figure 1.** Transmission electron microscopy (TEM) image of an array of as-synthesized, 10.2-nm-diameter CoPt<sub>3</sub> nanocrystals on a carbon-coated copper grid. Inset shows a high-resolution TEM image of a single nanocrystal. Lattice fringes indicate a single crystalline domain.

these 10.2-nm-diameter CoPt<sub>3</sub> nanocrystals remain structurally unchanged following anneals of up to 200 °C in air over 2 h with no evidence for nanocrystal oxidation.<sup>16</sup> Electrical measurements of nanocrystal devices are performed using a semiconductor parameter analyzer (model HP4156A, Agilent Technologies, U.K.), with voltage resolution of <100  $\mu$ V and current resolution of <100 fA. For room-temperature measurements, electrode chips are contacted using a probe station (model PML-8000, Wentworth Labs, U.K.). For variable-temperature measurements (3–400 K), electrode chips are mounted in leadless chip carriers, wire-bonded, and inserted into a liquid helium bath cryostat (Spectrostat, Oxford Instruments, U.K.).

## Results and Discussion

Because of their narrow size distribution ( $\sigma = 9\%$ ), the CoPt<sub>3</sub> nanocrystals spontaneously self-organize into two-dimensional (2-D) and three-dimensional (3-D) superlattices when nanocrystal solutions are dropped onto substrates and the toluene solvent is allowed to evaporate in a controlled manner (see Figure 1).<sup>16,18,19</sup> Multilayer CoPt<sub>3</sub> nanocrystal arrays deposited on carbon-coated copper TEM grids pack into cubic close-packed (ccp)-like superlattices that exhibit long-range order.<sup>16</sup> The nanocrystal cores are highly crystalline (see Figure 1, inset) and are separated by the hexadecylamine and bulky 1-adamantanecarboxylic acid ligands that are coordinated to each nanocrystal surface. Values for the mean inter-nanocrystal separation ( $s$ ) are extracted from TEM and SEM data by counting the number of nanocrystals in a defined area (typically  $\sim 65$  nanocrystals in a 100 nm  $\times$  100 nm region of the array shown in Figure 1) and calculating the mean area occupied by a single nanocrystal ( $A_{\text{NC}} = 154 \text{ nm}^2$ ). Assuming hexagonal packing,  $A_{\text{NC}} = (\sqrt{3}/2)(d + s)^2$ , yielding  $s \approx 3.1 \text{ nm}$ .

Measured room-temperature low-bias resistances ( $R_{\text{RT}}$ ) always exceed 1 T $\Omega$  for multilayer nanocrystal arrays self-assembled between electrodes (45 nm gap), which is consistent with similarly large inter-nanocrystal separations. A mild thermal annealing process has been developed to reduce the average inter-nanocrystal separation in situ, through ligand melting and increased ligand interdigitation.<sup>20–23</sup> The maximum anneal

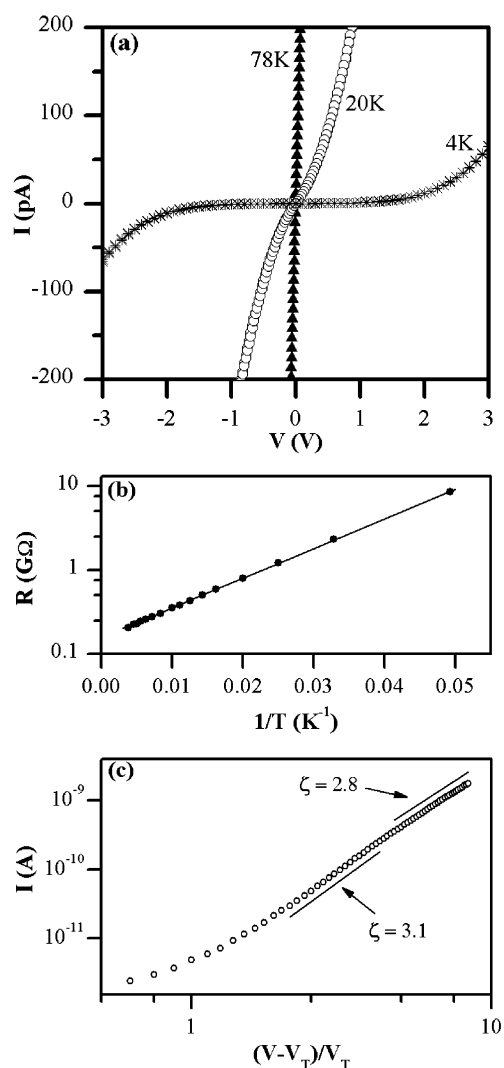


**Figure 2.** Post-anneal (150 °C) scanning electron microscopy (SEM) image of a typical CoPt<sub>3</sub> nanocrystal device with an inter-electrode spacing of 45 nm.

temperature is deliberately limited to 150 °C, to minimize ligand desorption and prevent nanocrystal melting or sintering.<sup>24</sup> In contrast to other reports, we intend to deliberately avoid altering the structure and chemistry of the individual nanocrystals and protecting ligands, so that we can be confident that changes in the charge-transport characteristics are solely due to decreased inter-nanocrystal separation, i.e., increased inter-nanocrystal electronic coupling.<sup>14,17,25</sup>

Figure 2 shows a high-resolution SEM image of a nanocrystal device following post-deposition annealing in forming gas at 150 °C. The annealed nanocrystal assembly is a discontinuous multilayer (void fraction of  $\sim 10\%$ ) that “carpets” over the 30-nm-thick electrodes. The mean post-anneal inter-nanocrystal separation ( $s_{\text{PA}}$ ) can be estimated by counting the number of nanocrystals ( $N_{\text{PA}}$ ) in a defined region (area  $A = 100 \text{ nm} \times 100 \text{ nm}$ ) around the electrodes.<sup>25</sup> We find  $N \approx 69$  for regions of area  $A$  on unannealed devices (data obtained by high-resolution SEM). Similar measurements for the annealed device shown in Figure 2 yield  $N_{\text{PA}} \approx 81$ . Because the nanocrystal diameter ( $d = 10.2 \text{ nm}$ ) is unaffected by the mild thermal anneal temperatures used and  $N \propto A/(d + s)^2$ , the mean post-anneal inter-nanocrystal separation can be calculated from the ratio of  $N_{\text{PA}}/N$ , i.e.,  $s_{\text{PA}} = (s + d)(N_{\text{PA}}/N)^{1/2} - d$ , and by assuming a value of  $s = 3.1 \text{ nm}$ . Using this approach,  $s_{\text{PA}} \approx 2.1 \text{ nm}$  for the device shown in Figure 2, suggesting a substantial reduction in mean inter-nanocrystal distance following mild thermal annealing. In the 45 nm gap between the electrodes, the nanocrystal assembly is not ordered, presumably as a result of structural perturbations that are due to the electrodes. However, the nanocrystals are distinct, with no evidence of sintering, and the shortest apparent conducting paths through the assembly contain only 4–5 nanocrystals.

Figure 3a shows the post-anneal  $I$ – $V$  characteristics for the device shown in Figure 2. All measured  $I$ – $V$  data are symmetric and show no hysteresis. At 300 K, the behavior is ohmic with a low bias resistance:  $R = 130 \text{ M}\Omega$ , which is 4 orders of magnitude lower than values measured for unannealed devices. Assuming that the assembly dimensions are 45 nm  $\times$  45 nm  $\times$  30 nm, the corresponding device resistivity is  $\rho \approx 4 \text{ }\Omega\text{m}$ .  $R$  increases monotonically as the temperature  $T$  decreases. At and



**Figure 3.** (a) Variable-temperature current–voltage ( $I$ – $V$ ) characteristics for the device shown in Figure 2. (b) Semilogarithmic plot of  $R$  vs  $1/T$ ; data (circles) are well fit by an activation model (solid line) for  $k_B T < E_c$  ( $E_c = 7$  meV). (c) Measured low-temperature (4 K) scaling behavior of the device current above the Coulomb blockade threshold voltage ( $V_T$ ); the values of the extracted scaling exponents,  $\zeta$ , suggest conduction through a network with a dimensionality of greater than two dimensions. The crossover behavior from  $\zeta = 3.1$  to  $\zeta = 2.8$  is indicative of structural disorder.

below  $T = 40$  K, pronounced nonlinearity appears in the  $I$ – $V$  curve near zero bias. For  $T \leq 12$  K, complete current suppression is observed at low bias; i.e., a finite threshold voltage ( $V_T$ ) is required to pass current through the array.<sup>14,15</sup> For the device with  $I$ – $V$  data shown in Figure 2, a value of  $V_T = 0.8$  V may be observed over repeated measurements at 4 K.

The temperature dependence of the low-bias resistance ( $R$ ) above 20 K provides strong evidence for the monodispersity of the nanocrystal array and the stability of the protecting ligand monolayer following the anneal. The measured variation in  $R$  vs  $T$  is consistent with the Neugebauer–Webb model for tunnel transport through an array of size-similar nanoscale metallic islands in an insulating matrix, where the tunneling rate is independent of temperature but the carrier density is activated.<sup>26</sup> For such a system, one expects low-bias electrical transport to be dominated by the activation energy required to electrostatically charge individual electrically neutral nanocrystals within the array ( $E_c$ ). Consequently, the  $R$  vs  $T$  characteristics should show activated behavior ( $R \propto \exp[E_c/(k_B T)]$ ) for  $k_B T < E_c$ ,

where  $k_B$  is the Boltzmann constant.<sup>4,8–14</sup> Figure 3b presents a semilogarithmic plot of  $R$  vs  $1/T$  for the device with  $I$ – $V$  data shown in Figure 3a and demonstrates that the device indeed exhibits activated behavior in the temperature range of 20–80 K. For all such measured devices, data fits yield activation energies in the range of 7 meV  $< E_c < 10$  meV, in good agreement with previously measured values for assemblies of 10-nm-diameter cobalt nanocrystals (10 meV  $< E_c < 14$  meV).<sup>14,27</sup> The narrow range of measured activation energies for the CoPt<sub>3</sub> nanocrystal devices also provides further supporting evidence of the monodispersity of the nanocrystals, previously measured by TEM. Although the data can also be fit using the Abeles model first derived for polydisperse metal islands in insulating matrixes,  $R \propto \exp[1/T^{1/2}]$ ,<sup>28</sup> Black et al. estimated that  $R$  vs  $T$  characteristics for assemblies of polydisperse nanocrystals should only deviate significantly from the Neugebauer–Webb model ( $R \propto \exp(1/T)$ ) for nanocrystal size dispersions ( $\sigma > 15\%$ ).<sup>27</sup> Furthermore, they propose that the temperature dependence should only tend toward that of the Abeles model for  $\sigma > 50\%$ .

The total capacitance of a nanocrystal,  $C_\Sigma$ , can be related to the activation energy via the relation  $E_c = e^2/(2C_\Sigma)$ . Assuming an activation energy for nanocrystal charging of  $E_c = 7$  meV, the total capacitance of each nanocrystal is  $C_\Sigma = 11.4$  aF, which results from the inter-nanocrystal capacitance and the nanocrystal self-capacitance,  $C_0 \approx 4\pi\epsilon_0\epsilon r \approx 1.5$  aF, where  $r$  is the nanocrystal radius ( $r = 5.1$  nm) and  $\epsilon$  is the relative permittivity of the ligand, ( $\epsilon \approx 2.7$ ).<sup>29</sup> For a 2-D or 3-D film with fcc packing, each nanocrystal will have between 6 and 12 nearest neighbors. Neglecting the small contribution to  $C_\Sigma$  from  $C_0$ , the pairwise inter-nanocrystal capacitance is estimated to be  $C = C_\Sigma/9 \approx 1.3$  aF. The mean inter-nanocrystal spacing ( $s_{PA}^*$ ) for the device shown in Figure 2 may then be estimated from the pairwise inter-nanocrystal capacitance using  $C \approx 2\pi\epsilon_0\epsilon r \ln(1 + 2r/s_{PA}^*)$ .<sup>14,30</sup> A value of  $s_{PA}^* \approx 2.4$  nm is estimated, based on the measured activation energy for nanocrystal charging ( $E_c = 7$  meV). This is in excellent agreement with the calculated post-anneal mean inter-nanocrystal separation ( $s_{PA} \approx 2.1$  nm) obtained from SEM images of measured devices (see Figure 2). Therefore, both structural and electrical data indicate an anneal-induced reduction in mean inter-nanocrystal separation from the value of  $s \approx 3.1$  nm measured in unannealed nanocrystal arrays.

Concerning the voltage dependence of the current at  $T < 12$  K for the device with  $I$ – $V$  data shown in Figure 2a, complete current suppression is observed for voltages below the threshold voltage ( $V_T = 0.8$  V). Measured values of  $V_T$  are dependent on the device, probably because of local geometric disorder and/or charge disorder arising from random parasitic charges present within the nanocrystal arrays and/or the oxidized silicon substrates. For voltages above  $V_T$ , theory predicts that, for a uniform array of identical nanoscale metallic islands separated by tunnel barriers, the current should follow a power law:  $I \propto [(V/V_T) - 1]^\zeta$ , where the scaling exponent ( $\zeta$ ) is dependent on the dimensionality of the array, i.e., the number of accessible current paths.<sup>31</sup> If one path (or a small number of paths) carries most of the current, then the network is essentially one-dimensional (1-D) and theory predicts  $\zeta = 1$ . For 2-D current-carrying networks, a value of  $\zeta = 5/3$  is predicted, whereas numerical simulations have yielded values of  $\zeta \approx 2 \pm 0.2$ .<sup>31</sup> Figure 3c presents a log–log plot of data measured for the device shown in Figure 2, which demonstrates that the current follows a power law over 3 orders of magnitude with a crossover from  $\zeta = 3.1 \pm 0.05$  to  $\zeta = 2.8 \pm 0.05$  at  $(V/V_T) - 1 = 4.6$ .



The magnitude of the extracted values of  $\zeta$  suggests transport through networks of conduction paths with dimensionality equal to or greater than two dimensions. Indeed, previous experimental data for slightly larger arrays of 10-nm-diameter cobalt nanocrystals have yielded scaling exponents of  $2.2 < \zeta < 2.7$  for multilayer assemblies (1–3 layers).<sup>14</sup> Similar kinks in scaling data have been observed and simulated for geometrically disordered, monolayer assemblies of monodisperse 5-nm-diameter gold nanocrystals with void fractions of  $\sim 15\%$ – $20\%$ .<sup>15</sup> The 2-D assembly is modeled as a set of parallel channels (1 + 1-D system), where only a single channel conducts at voltages just above the Coulomb Blockade threshold  $V_T$ . As the voltage is progressively increased, a growing number of channels conduct and the crossover behavior emerges. For the CoPt<sub>3</sub> nanocrystal device with data shown in Figure 3c, the slight kink is indicative of finite geometric disorder in the assembly, probably due to perturbations from the electrodes which limit the formation of an ordered nanocrystal array during deposition. Therefore, the observed behavior is consistent with the nanocrystal multilayer array deposition conditions used during device fabrication and with the SEM data presented for annealed devices (see Figure 2).

We have demonstrated that in situ thermal annealing can be used to modify the electronic properties of nanocrystal array devices through control of the inter-nanocrystal distance and, hence, inter-nanocrystal electronic coupling for small nanocrystal assemblies where the shortest conducting paths consist of fewer than five nanocrystals. Nanocrystals remain structurally and chemically intact following anneals and the dramatic reduction in device resistance permits measurement of the electronic characteristics of the device assemblies. Measured data confirm nanocrystal monodispersity while yielding single nanocrystal charging energies of  $E_c \approx 7$  meV, corresponding to pairwise inter-nanocrystal capacitances  $C \approx 1.3$  aF. The nanocrystal array devices act as Mott insulators with charging energies governed by nanocrystal size and nearest-neighbor capacitances (arising from reduced inter-nanocrystal separation). Furthermore, the influence of assembly dimensionality and geometric disorder may be clearly identified. Therefore, electrical techniques are powerful tools for characterization of the electronic properties of nanocrystal assemblies, and in situ mild thermal processing offers a novel method to modify inter-nanocrystal electronic coupling from Mott insulating through to metallic regimes. These experiments are underway.

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