# Fabrication of Sub-10-nm Silicon Nanowire Arrays by Size Reduction Lithography

**Yang-Kyu Choi,[†] Ji Zhu,[‡,§] Jeff Grunes,[‡,§] Jeffrey Bokor,[†] and Gabor. A. Somorjai*[,‡,§]**

*Department of Electrical Engineering and Computer Sciences, UC Berkeley, Berkeley, California 94720, Department of Chemistry, UC Berkeley, Berkeley, California 94720, Material Science and Chemistry Division, Lawrence Berkeley National Lab, Berkeley, California 94720*

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A photolithography-based method capable of size reduction to produce sub-10-nm Si nanowire arrays on a wafer scale is described. By conformally depositing a material (silicon oxide or silicon) that has a different etching property over a lithographically defined sacrificial sidewall and selectively removing the sacrificial material, the sidewall material is preserved and can serve as nanopattern mask for further processing. The resolution of this method is not limited by photolithography but by the thickness of the material deposited. The application of size reduction nano-patterning method can range from the fabrication of biosensors to model catalyst systems.

## Introduction

The fabrication of nanoscale patterns with dimensions of 10 nm or less has been the goal of many researchers for potential applications as sensors,[1] soft X-ray optical device components,[2] electronic circuit elements, or catalysts,[3] to name a few. Electron beam lithography, with a finely focused electron beam, is the most commonly used technique for nanometer pattern generation by decomposing a polymer (usually PMMA) in a desired pattern. However, the generation of secondary electrons during electron bombardment makes it difficult to achieve sub-10-nm patterning.[4] Electron beam lithography is also a sequential pattern producing technique and is very time-consuming compared to photolithography-based processes that produce the whole pattern at once using a mask. This is also the case for other scanning probe based lithography techniques.[5] One of the promising directions is to start with a pattern that is produced by photolithography that has spatial definition of the order of the wavelength of visible light (~600 nm) and then find ways to reduce the size of the elements that make up the pattern that is produced using a mask. There is a US patent that reports on a method of "reducing the pitch of line and space dimensions" from polysilicon (polycrystalline silicon) and a metal oxide by etching one of the materials that leaves the other material intact.[6] Using similar techniques, the doubling of the frequency of lines in a grating made of silicon is reported to obtain a 100 nm pitch.[7]

Using siloxane self-assembled monolayers, "edge transfer lithography" was reported that managed size reduction of patterns to 100 nm.[8] Choi et al. carried out what they called "spacer lithography" to produce electronic devices in silicon with sub-40-nm structures starting from 600 nm structures produced by photolithography.[9−11] The quality of their size-reduced structures were superior to those made by electron beam lithography.

Using the techniques of size reduction reported by Choi et al., we produced 20 nm wide single-crystal silicon nanowire arrays starting with wires 600 nm wide. Further oxidation of the silicon nanowires and etching in HF reduced the dimensions to sub-10 nm. This paper describes the method in detail. We have chosen to produce $7 \times 10^8$ nanowires on a 4 in. silicon (100) wafer to obtain a total patterned surface area of ~1 $cm^2$. For chemical applications as sensors or catalysts, the number of product molecules detected or produced is proportional to the surface area. Thus, the ~1 $cm^2$ nanowire area of the $7 \times 10^8$ nanowires ensures a large signal-to-noise ratio in the detection of chemical products.

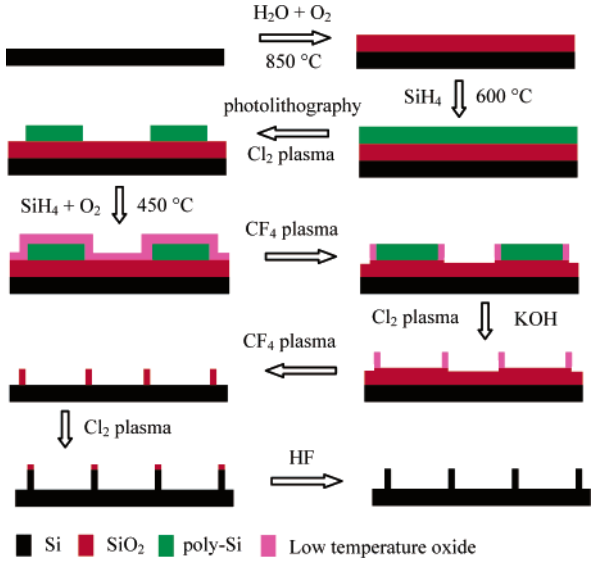


**Figure 1.** Schematic drawing of the size reduction lithography process.

## Fabrication of 10 nm Si Wire Array by Size Reduction Starting from 600 nm Wide Wires

**A. Scheme of Size Reduction Lithography.** The scheme is provided in Figure 1. A thermal oxide is grown on the 4 in. silicon (100) wafer, and polysilicon is then deposited on top of the oxide by silane decomposition. Photoresist is spin coated on the polysilicon film, and it is exposed to UV light through a mask that makes the exposed polymer soluble in basic developer solution. The 600 nm wide wires are plasma-etched

* To whom correspondence should be addressed. E-mail: somorjai@socrates.berkeley.edu.
[†] Department of Electrical Engineering and Computer Sciences, UC Berkeley.
[‡] Department of Chemistry, UC Berkeley.
[§] Lawrence Berkeley National Lab.

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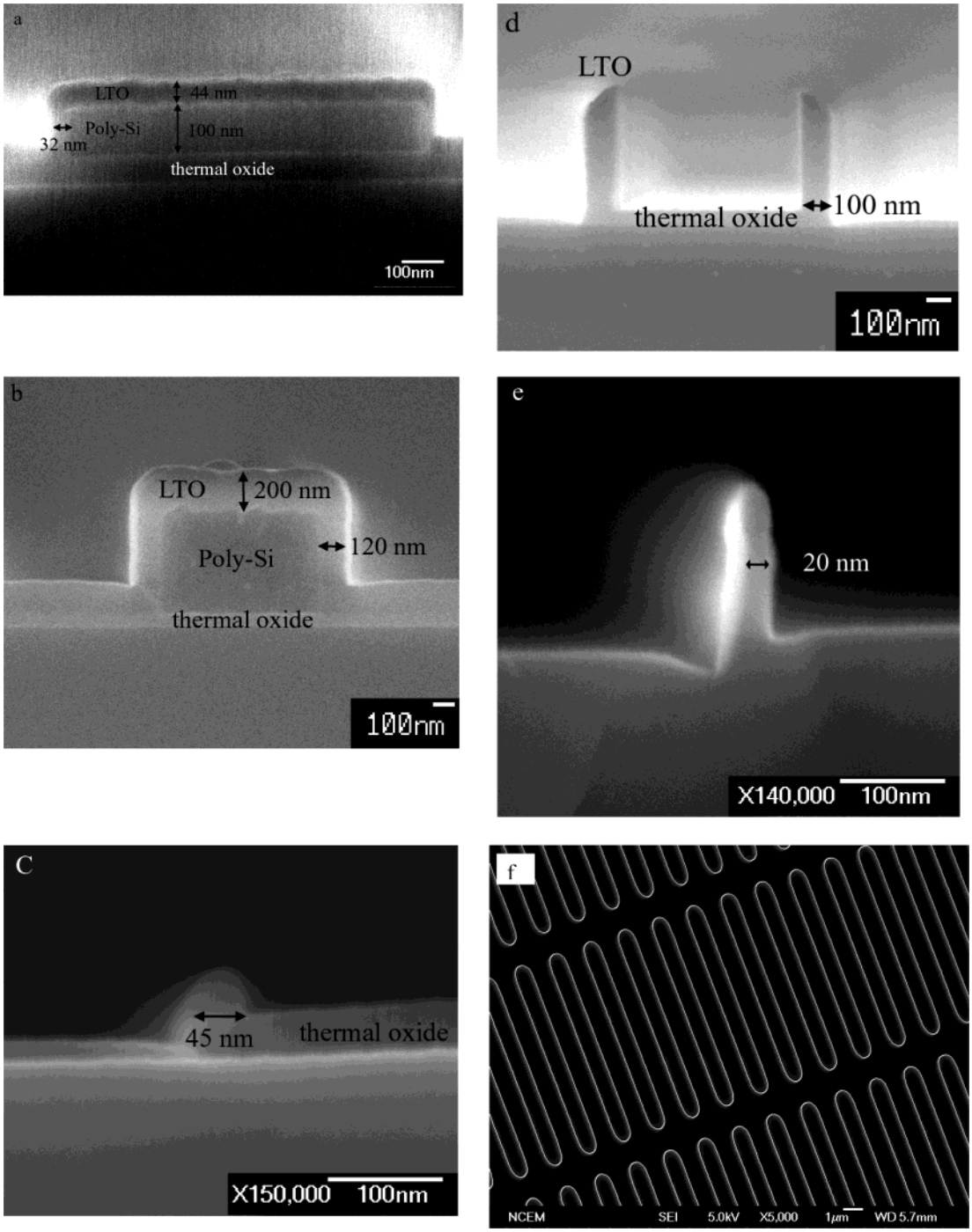


**Figure 2.** (a) Cross section view after thin LTO deposition (44 nm). (b) Cross section view after thick LTO deposition (200 nm). (c) Cross section view after the top LTO layer and poly-Si layer have been etched away from the structure in part a. Notice the broadening of feature size from 32 to 45 nm. (d) Cross section view after the top LTO layer and poly-Si layer have been etched away from the structure in part b. Notice the undercut of the feature size at the bottom of the LTO hard mask. (e) Cross section of 20-nm Si nanowire array made from size reduction lithography. (f) Top view of the 20-nm Si nanowire array.

with $Cl_2$ and HBr that remove the polysilicon not covered by the photoresist. The next step is to deposit silicon oxide on top of the polysilicon followed by a $CF_4$ plasma etch to expose the polysilicon and its silicon oxide sidewalls. Using plasma etching ($Cl_2$ and HBr) again, the polysilicon is removed, leaving behind silicon oxide wires less than 200 nm wide. By employing $CF_4$ plasma etching again, the silicon oxide between the silicon oxide wires is etched away. The silicon wafer is etched with $Cl_2$ and HBr plasma until the desired height of the silicon wire is obtained. Finally, the remaining $SiO_2$ is removed by HF (optional). The procedure described above produces 20 nm silicon nanowires, which is more than an order of magnitude reduction as compared to the 600 nm wire width we started with. The thermal oxide grown initially serves as the hard mask for Si etching, the polysilicon deposited serves as a sacrificial layer, and the low temperature oxide (LTO) deposited is what determines the final pattern size. The essence of the technique is based on the fact that material deposited during low-pressure chemical vapor deposition covers the step edge as well as the top of the step, which is known as conformal deposition. In contrast, plasma etching is an anisotropic technique, removing materials preferentially in the direction perpendicular to the surface. Therefore, by depositing a material that has a different etching property than the sacrificial layer and directionally

etching the material on the top of the step, the sacrificial layer can be removed selectively, leaving only the material deposited on the sacrificial structure sidewall. The feature size thus generated is determined by the thickness of the deposited material not by the photolithography, but the pattern pitch is determined by the minimum pattern obtainable with photolithography. Because the thickness of the deposited film can be controlled to 10 nm or less with high precision, this method is capable of generating nanopattern far smaller than possible by optical lithography.

**B. Experimental Details.** The fabrication steps are carried out in UC Berkeley Microfabrication Laboratory (Microlab), and a field emission scanning electron microscope (JEOL JSM-6340F) was used to characterize the obtained features in every step of the process. Si(100) was used as the starting material. A 50∼70 nm thermal oxide layer was grown on the Si wafers in a water stream and oxygen (Figure 1b). The optimal thickness of the thermal oxide was chosen from these two functional considerations. The layer should be thick enough to protect the substrate during the removal of the sacrificial polysilicon layer, while a thin layer is desired to minimize pattern broadening when forming the hard mask for subsequent silicon etching. A thin layer of polysilicon was deposited by low-pressure chemical vapor deposition at 600 °C as the sacrificial layer (Figure 1c). For improved mechanical stability, the layer thickness is 100 nm for generating Si features with sizes less than 30 and 400 nm for larger Si nanowires. The polysilicon layer was then patterned by photolithography with a GCA 6200 wafer stepper, the resolution of which was around 600 nm. The pattern was transferred from the photoresist layer to the polysilicon layer by plasma etching in a Lam Research 9400 TCP etcher (Figure 1d). The conditions were 50 sccm $Cl_2$, 150 sccm HBr, pressure 15 mTorr, electrode temperature 50 °C, 300 W top electrode power, and 150 W bottom electrode power with a bias of −160 V. This recipe etched polysilicon with a speed of ∼7 nm/s and produced a nearly vertical sidewall profile with an angle >89.5°. It is also important to remove the polymers after the polysilicon etching. The estimated residue polymer thickness was 20∼30 nm, which would significantly enlarge the nanometer pattern desired. The post etch step for the removal of the polymer was to dip the wafer in (100:1) HF for 10 s, strip the photoresist with oxygen plasma, followed by (100:1) HF 10 s then piranha [(4:1) $H_2SO_4$: $H_2O_2$] treated at 120 °C. Low-temperature oxide (LTO) was deposited by low-pressure chemical vapor deposition over the patterned polysilicon layer (Figure 1e). The conditions were 5 sccm $SiH_4$ and 70 sccm $O_2$ at 450 °C. The deposition rate was ∼3 nm/min. The step coverage is ∼70% for thin films (<50 nm) and ∼60% for thicker films, as shown in Figure 2, parts a and b, respectively. The thickness of the deposited LTO on the sidewall determines the minimum feature size. Anisotropic plasma etching was used to remove the LTO on the top of the sacrificial structure and open the polysilicon structure (Figure 1f). The conditions were 100 sccm $CF_4$, pressure 13 mTorr, 200 W top electrode power, and 40 W bottom electrode power with a bias of −80 V. The etching speed was ∼2 nm/s for LTO. This recipe also etches polysilicon and single-crystal silicon with almost the same speed as for LTO. The polysilicon sacrificial layer was then removed with either wet etching or plasma etching (Figure 1g). Wet etching was conducted in $1{:}2_w$ KOH aqueous solution at 80 °C; the etching speed was around 17 nm/s for polysilicon and 0.1 nm/s for LTO. Because of the etching nonuniformity, the complete removal of polysilicon is generally not achieved until 2 min and this will severely undercuts the LTO spacer at 10 nm scale. Therefore, wet etching is not used for spacers smaller than 30 nm, and plasma etching is used instead. The polysilicon plasma etching process is the same as the process for transferring the pattern from photoresist into polysilicon layer and the etching selectivity of polysilicon to LTO is 22. The LTO pattern was then transferred to the thermal oxide layer by plasma etching with conditions 100 sccm $CF_4$, pressure 13 mTorr, 200 W top electrode power, and 40 W bottom electrode power (Figure 1h). The resulting oxide pattern sidewall profile after this etching is not ideally vertical, showing some broadening for smaller spacers (<30 nm, Figure 2c) and a noticeable undercut for larger spacers (>50 nm, Figure 2d). The oxide pattern was transferred to silicon by plasma etching with conditions 50 sccm $Cl_2$, 150 sccm HBr, pressure 15 mTorr, electrode temperature 50 °C, 300 W top electrode power, and 150 W bottom electrode power (Figure 1i). 20 nm silicon nanowires can be routinely fabricated with this process, as shown in Figure 2, parts e and f. The 6 nm silicon feature has also been defined with this method.[10]

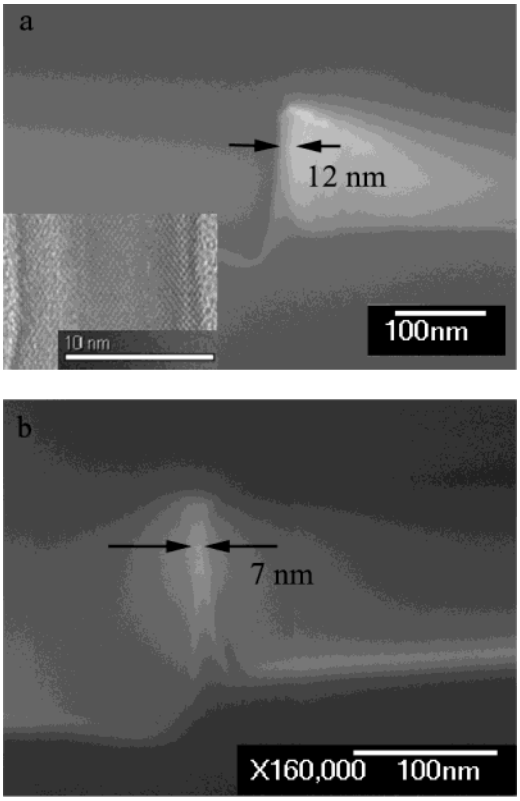


**Figure 3.** (a) Cross section of 12-nm Si nanowire array made after thermal oxide trimming. Inset HRTEM image shows the single crystalline nature of the Si nanowire. (b) Cross section of 7-nm Si nanowire array made after further thermal oxide trimming.

To reduce the silicon size further, the resulting 20 nm silicon nanowires were oxidized at 800 °C for 20 min followed by HF dipping to remove the oxide. This treatment reduced the silicon dimension to ∼12 nm, as shown in Figure 3a. A high-resolution transmission electron microscopy image also shows the single crystalline nature of the Si nanowire. Further oxidation at 800 °C for 10 min reduced the silicon dimension to ∼7 nm, as shown in Figure 3b. The concave shape of the cross section of Si nanowire is due to lower oxidation rate for concave and convex surfaces (top and bottom) than planar surface (middle).[12,13]

The size-reduction process can be repeated by alternating poly-Si and $SiO_2$ as the sidewall and sacrificial materials, doubling the pitch with each cycle. Figure 4 shows dense 70 nm nanowires with 80 nm spacing which were fabricated over

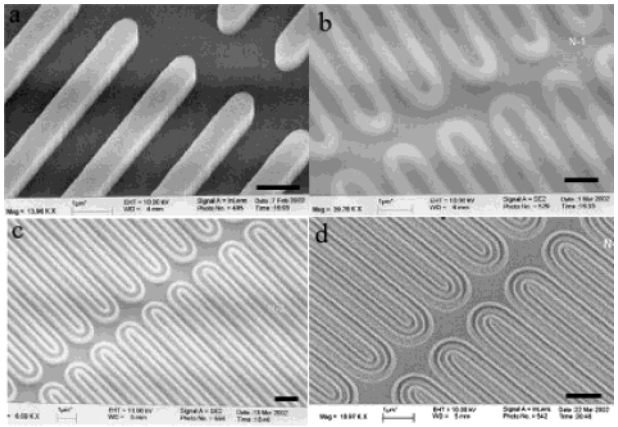


**Figure 4.** Multiplication of pattern density by size reduction lithography. (a) After patterning sacrificial poly-Si layer, (b) after LTO deposition, LTO spacer etched by $CF_4$ plasma, and removal of sacrificial poly-Si by KOH, (c) after poly-Si deposition, poly-Si spacer etched by $Cl_2$ and HBr, and removal of LTO by HF, and (d) after LTO deposition, LTO spacer etched by $CF_4$ plasma, and removal of sacrificial poly-Si by KOH. For an etch stop, nitride was deposited before starting size reduction lithography. 8 ($=2^3$) lines were generated from one line after three cycles of size reduction lithography. Line width was 70 nm and space was 80 nm in (d). The scale bars are 1 $\mu$m.

a full 4″ wafer, after three size-reduction repetitions starting with 0.6 $\mu$m optical lithography.

This size reduced Si nanowire structure can then be used as a mask for producing high surface area devices by nanoimprint lithography. Nanowire arrays of metals can be produced, and works are in progress in our laboratory to fabricate Pt nanowires for catalysis studies and will be reported in a forthcoming publication.

## Conclusion

A photolithography-based process was described here to produce silicon nanowire arrays on silicon wafers. By combining the conformal deposition and anisotropic etching processes, 20 nm silicon nanowire arrays can be routinely produced. Oxidation and HF trimming further reduce the structure size into sub-10-nm regime. By using photolithography techniques, size reduction lithography permits us to make 10-nm spatial features starting from the 600-nm range, achieving more than an order of magnitude reduction.

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