# Organic Thin Film Transistors Based on *N*-Alkyl Perylene Diimides: Charge Transport Kinetics as a Function of Gate Voltage and Temperature

**Reid J. Chesterfield,[†] John C. McKeen,[†] Christopher R. Newman,[†] Paul C. Ewbank,[‡] Demétrio A. da Silva Filho,[§] Jean-Luc Brédas,[§] Larry L. Miller,[‡] Kent R. Mann,[‡] and C. Daniel Frisbie*,[†]**

*Department of Chemical Engineering and Materials Science, University of Minnesota, 421 Washington Avenue SE, Minneapolis, Minnesota 55455, Department of Chemistry, University of Minnesota, 207 Pleasant Street SE, Minneapolis, Minnesota 55455, and School of Chemistry and Biochemistry, Georgia Institute of Technology, Atlanta, Georgia 30332-0400*

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We report structural and electrical transport properties of a family of $\pi$-stacking soluble organic semiconductors, *N,N′*-dialkyl-3,4,9,10-perylene tetracarboxylic diimides (alkyl − pentyl [**1**], octyl [**2**], and dodecyl [**3**]). The structures of evaporated polycrystalline films of **1**−**3** were studied using X-ray diffraction and atomic force microscopy. Films of **1**−**3** pack similarly with the direction of $\pi-\pi$ overlap in the substrate plane. Organic thin film transistors (OTFTs) based on **1**−**3** deposited on $SiO_2$ gate dielectric showed linear regime electron mobilities of 0.1, 0.6, and 0.2 $cm^2/(V\ s)$, respectively, corrected for contact resistance. OTFTs of **2** had saturation electron mobilities as high as 1.7 $cm^2/(V\ s)$ with on-to-off current ratios of $10^7$. Variable temperature measurements were used to examine the charge transport kinetics in the range 80−300 K and revealed (1) thermally activated electron mobilities with activation energies dependent on gate voltage and (2) the presence of well-defined isokinetic points, i.e., temperatures at which Arrhenius plots at different gate voltages intersect for a given film. Isokinetic points indicate a common charge transport mechanism and can be explained in terms of the multiple trapping and release (MTR) transport model. MTR assumes trap-limited band transport, and quantum chemical calculations were used to verify that delocalized transport is likely in **1**−**3**; a conduction bandwidth of 0.58 eV was calculated for **1**. Using MTR, the trap concentrations were estimated to be $\sim 10^{12}$ $cm^{-2}$ for deep traps, and $\sim 6 \times 10^{13}$ $cm^{-2}$ for shallow traps. However, a nonmonotonic dependence of the electron mobility on gate voltage was also observed, which is not predicted by MTR and suggests that the transport mechanism is more complicated, perhaps due to the discrete layered structure of these materials. The high values for the electron mobility and on-to-off current ratio suggest that substituted perylene diimides represent a promising class of n-channel conductors for OTFTs.

## Introduction

Organic semiconductors are an important class of electronic materials that offer intriguing prospects for high throughput, low-temperature processing of electronic circuitry on flexible substrates.[1−4] Developing new organic semiconductors with improved performance in specific devices (e.g., thin film transistors, light-emitting diodes, photovoltaic cells) is an important goal for materials chemistry.[5−8] In the case of organic thin film transistors (OTFTs), there is a particular need for n-channel (electron conducting) organic semiconductors with performance comparable to p-channel (hole conducting) materials, in order for organic electronics to realize the benefits of complementary circuit design. In complementary circuits, both positive and negative gate voltages are used to switch transistors, resulting in simpler circuits and lower power consumption than if only p-channel or n-channel devices are employed. In the last several years there has been increased attention to n-channel TFT materials with corresponding improvements in the field effect mobility, the on-to-off current ratio, and the threshold voltage.[9−15] Still, the performance of the best n-channel materials is not quite as good as the best p-channel materials, such as pentacene,[2] which is the current benchmark organic semiconductor for OTFT applications.

Here we present a detailed structural and electrical characterization of polycrystalline films based on a homologous series of *N*-alkyl perylene diimides, molecules **1**−**3** (Figure 1), which behave as n-channel conductors in OTFTs. Perylene diimides are good candidates for n-channel conductors because (1) they have relatively large electron affinities, which facilitate electron accumulation in the TFT structure, (2) they typically assemble in $\pi$-stacks in the solid state which enhances the intermolecular $\pi$-orbital overlap and facilitates charge transport, and (3) the nature of the $\pi$-orbital interactions can be tuned with high precision by changing the substituents on the imide N atoms, offering the opportunity to optimize transport properties by systematic structural variations. Indeed, the subtle interplay between molecular structure, crystal packing, and intermolecular $\pi$-orbital interactions in perylene diimides gives rise to their well-known crystallochromic behavior (i.e., the dependence of color on structure and crystal packing) and is important in their application as commercial paint pigments (e.g., perylene

* To whom correspondence should be addressed. E-mail. frisbie@cems.umn.edu. Telephone: 612-625-0779.
[†] Department of Chemical Engineering and Materials Science, University of Minnesota.
[‡] Department of Chemistry, University of Minnesota.
[§] Georgia Institute of Technology.

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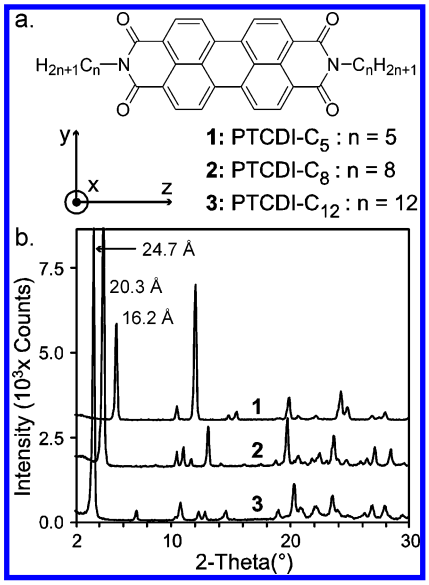


**Figure 1.** (a) Structures of perylene diimides (**1**−**3**) studied in this work. (b) XRD powder patterns of **1**−**3**. The (001) peak has been labeled with the corresponding *d* spacing.

red).[16,17] More recently, perylene diimides have been evaluated as electron transporters in organic photovoltaic cells,[18] and several N-substituted derivatives have been shown to have liquid crystalline phases.[19−21]

The potential of perylene diimides for OTFT applications has been recognized previously. In 2002, Malenfant, Dimitrakopoulos, and co-workers reported n-channel OTFTs based on **2** with saturation electron mobilities of 0.6 $cm^2/(V\ s)$, a remarkably high value.[13] In earlier work, Horowitz showed that an *N*-phenyl-substituted perylene diimide showed weak n-channel field effect conduction,[22] and the group at Lucent made TFTs from perylene tetracarboxylic dianhydride (PTCDA) and naphthalene diimides, close analogues to perylene diimide.[23] We recently reported an examination of contact resistance and air-stability for n-channel OTFTs based on **1**.[24] In that work, films of **1** displayed electron mobilities of 0.1 $cm^2/(V\ s)$ and on-to-off current ratios of $10^6$ under vacuum; the performance degraded in air. While these earlier studies established the n-channel activity of perylene diimides and related compounds, there was no systematic exploration of OTFT behavior as a function of structure for a homologous series of perylene diimides. Detailed studies of structure−property relationships and the mechanism of charge transport are of critical importance to the broader goal of designing organic semiconductors with better performance in OTFTs.

Here we show that by paying careful attention to film growth conditions, it is possible to achieve saturation electron mobilities under vacuum or reducing atmospheres as high as 1.7 $cm^2/(V\ s)$ in OTFTs based on **2**, which is the highest electron mobility reported so far for a polycrystalline organic semiconductor. Linear mobilities, which we feel are a better figure of merit, are routinely 0.3−0.6 $cm^2/(V\ s)$ for **2** with on-to-off current ratios better than $10^6$. The large electron mobilities are supported by electronic structure calculations detailed here that show that **1**−**3** have LUMO bandwidths consistent with substantial $\pi$-orbital overlap and intermolecular charge delocalization.

A central goal of this study was to probe the conduction mechanism in perylene diimide OTFTs based on **1**−**3** and to correlate the transport parameters with structural characteristics. Consequently, we have performed detailed examinations of the electron mobility as a function of gate voltage and temperature. For this work we have made use of a 4-terminal TFT structure that allows extraction of the contact-corrected mobility from the transistor current−voltage ($I-V$) characteristics. We have found that the TFT electron mobility is thermally activated, and that the activation energies are systematically gate voltage dependent. In addition, we observe isokinetic points in Arrhenius plots of mobility vs temperature at different gate voltages, which indicate a common charge transport mechanism with kinetics that can be tuned by the applied gate voltage. Isokinetic points are well-known in chemical kinetics studies of homologous gas- or solution-phase reactants and have been used to demonstrate common reaction pathways.[25,26] While isokinetic points have been observed in carrier transport studies of a-Si:H TFTs,[27] they have not been extensively reported for organic semiconductor films. The significance of these points is that they offer insight into the charge transport mechanism. We argue that the isokinetic points and most of our other observations can be explained in terms of the multiple trapping and release (MTR) model of charge transport[28,29] combined with the presence of a shallow distribution of electron trap states beginning at the conduction band edge. We use the model to extract trap concentrations and average trap depths, parameters that are critical to an overall understanding of the transport mechanism.

A central prediction of MTR is that the charge mobility should increase monotonically with gate-induced charge density. In contrast, we observe a peak in mobility vs gate-induced charge indicating that a simple MTR model coupled with a shallow trap distribution is not an adequate description of the transport. To our knowledge, the nonmonotonic dependence of mobility vs gate voltage is not widely appreciated for organic TFTs, and it is clearly important to the overall picture of the charge transport kinetics. More work will need to be done to clarify the dependence of the electron mobility on gate voltage. Nevertheless, we have demonstrated that transport in perylene diimides is dominated by electron trapping and that despite prevalent trapping, these films have exceptionally good n-channel behavior in TFTs. Furthermore, because of the ease with which their molecular and crystal structures can be modified, these materials offer excellent opportunities both for optimization of transport behavior and for systematic exploration of structure−property relationships that are critical to organic semiconductor design.

## Experimental Methods

**Semiconductor Synthesis and Purification.** *N*,*N*′-Dialkyl-3,4,9,10-perylene tetracarboxylic diimides (alkyl = pentyl [**1**], octyl [**2**], and dodecyl [**3**]) were synthesized according to the published procedure.[16] Source material for thin film growth was initially purified by removing volatile components in the crude product by Kugelrohr distillation at 200 °C in a 7 mT vacuum. Subsequent purification was achieved by temperature gradient sublimation in a flowing stream (∼100 mL/min) of 99.999% Ar. The gradient sublimation apparatus was modeled after the design of Kloc et al.[30] Mass transport was improved by application of a milliTorr vacuum to the outlet of the sublimation tube. At atmospheric pressure, single crystals of **1** were observed to grow in a platelike morphology with typical dimensions of 5 mm × 5 mm × 0.01 mm. Single crystals were extremely fragile, and they were not good candidates for structure determination by normal X-ray sources. **2** and **3** tended to grow in microcrystalline films at all pressures. Source material for thin film growth was purified by sublimation several times.

**Substrate Preparation.** Two types of insulating substrates were used for film growth, hydrophilic thermally grown silicon

oxide ($SiO_2$) and hydrophobic polymer coated $SiO_2$. These substrates served as the surface for thin film growth and as the insulating layer of the TFT. Initially, the untreated $SiO_2$ was cleaned by sonication in acetone and 2-propanol, followed by a short oxygen plasma or ozone exposure. Upon removal from the oxidizing environment, the substrate had a high surface energy (static water contact angle $\sim 0°$). This high surface energy $SiO_2$ served as the hydrophilic substrate. To retain the high surface energy, the hydrophilic substrates were periodically recleaned and stored under 2-propanol prior to loading for film growth. Hydrophobic $SiO_2$ (static water contact angle $\sim 101°$) was made by spin-coating an extremely thin layer of poly(α-methylstyrene) onto the high surface energy substrate, according to the patent published by 3M Company.[31] Further reference to substrates will use $SiO_2$ for the as prepared hydrophilic substrate and PS−$SiO_2$ for the as prepared hydrophobic substrate.

**Film Growth and Characterization.** Thin films of the **1**−**3** were prepared by thermal evaporation (from an alumina (or quartz) crucible) onto substrates held at constant temperature by a resistively heated and water-cooled copper block. The base pressure in the evaporation system was $2 \times 10^{-7}$ Torr. Film thickness was measured by a calibrated quartz crystal monitor. The initial growth rate was held between 0.01 and 0.02 Å/s up to a thickness of 60 Å, and then the rate was increased to 0.2−0.3 Å/s for another 300 Å. Substrate temperature ($T_S$) for film growth was investigated from 25 to 205 °C. The crystallinity of the thin films was studied by wide-angle X-ray diffraction (XRD) using a Siemens D5005 system with a Cu Kα ($\lambda$ = 1.5418 Å) source. Powder patterns of **1**−**3** were also taken on the D5005 system.

Film grain structure and morphology were examined using optical and atomic force microscopy (AFM). An Olympus (1000×) optical microscope with bright-field, dark-field, and differential interference contrast (DIC) capability was used to study grain size/structure and cracks in the thin films. A Digital Instruments Multimode AFM was used in tapping mode to study morphology and grain size on the sub-5-$\mu$m scale.

**TFT Fabrication.** A bottom gate, inverted staggered transistor structure was used to make thin film transistors of **1**−**3**. The gate and insulator layers consisted of 3000 Å of thermally grown oxide on a highly doped (0.01−0.1 Ωcm) ⟨100⟩ n-Si wafer. Wafers with thermally grown $SiO_2$ were obtained from Silicon Valley Microelectronics (San Jose, CA). Ohmic contact to the n-Si gate was made by thermal evaporation of 300 Å of Al capped with 1500 Å of Au, followed by a rapid thermal anneal in air at 450 °C. The measured dc-capacitance of the $SiO_2$ was 11.4 nF/cm$^2$ for both hydrophilic and hydrophobic substrates, which compares well with the ideal value of 11.45 nF/cm$^2$. Thin films of **1**−**3** were thermally evaporated onto the substrates up to a thickness of 350 Å. To minimize parasitic leak, the semiconductor film area was defined by shadow masking. Source and drain electrodes were defined by thermal evaporation of 500 Å of Ag through a shadow mask onto the semiconductor film. Puratronic (99.999%) grade Ag was obtained from Alfa Aesar (Ward Hill, MA). The base pressure in the metal evaporation chamber was $8 \times 10^{-8}$ Torr, and stayed below $2 \times 10^{-7}$ Torr during deposition. The transistor channel widths ($W$) were 1000 $\mu$m and the lengths ($L$) were 100 $\mu$m.

**Electrical Characterization.** Electrical characterization was performed in a Desert Cryogenics (Tucson, AZ) vacuum probe-station with a $5 \times 10^{-7}$ Torr base pressure. All electrical measurements were made in the dark. Variable temperature experiments were performed over the temperature range 80−300 K. Source and drain currents were measured independently using Keithley 236 Source/Measure units. Four-probe measurements were performed by measuring the floating potential of two mid-channel sense probes using Keithley 6517A electrometers; all units have input impedance $>10^{14}$ Ω. The parasitic leak to the gate electrode was never more than 10 pA in all reported devices. Linear ($\mu_{lin}$) and saturation ($\mu_{sat}$) regime mobilities were calculated based on standard metal-oxide-semiconductor field-effect transistor (MOSFET) equations.[32] $\mu_{lin}$ was calculated using the transconductance ($g_M$) at a specific drain voltage. $\mu_{sat}$ was calculated from the slope of a drain current$^{1/2}$ vs gate voltage plot, which was also used to find the threshold voltage $V_T$. The onset voltage ($V_0$) was determined from a logarithmic plot of the subthreshold drain current (log $I_D$) vs gate voltage ($V_G$) extrapolated to the $x$-axis intercept. For most devices, output/transfer curves were taken in 1.0 V drain/gate steps from −25 up to +100 V, respectively, with a dwell time of 0.3 s per step. Previously reported transistor instability mechanisms (observed as a hysteresis between forward/reverse sweeps and subsequent voltage sweeps) were minimized by removing oxygen from the cryostat and characterizing under hydrogen gas ($10^{-4}$ Torr).[33,34] Trap distribution calculations were performed using MATLAB and Mathcad codes developed at the University of Minnesota.

**Quantum Chemical Calculations.** Bandwidth and reorganization (molecular polaron binding) energy calculations were performed using the semiempirical intermediate neglect of differential overlap (INDO) method and density functional theory, respectively. In the framework of Hückel or tight-binding theory, the bandwidth of a one-dimensional stack is equal to $4t\cos(\pi/(N+1))$, where $t$ is the intermolecular transfer integral and $N$ is the number of molecular units in the stack. On the basis of the single-crystal structure of **1** (from the Cambridge database),[35] a small three-dimensional cluster of molecules was generated, and calculation of the transfer integrals on all dimers within the third nearest neighbor shells was performed with the help of the INDO Hamiltonian developed by Zerner et al.[36,37]

The reorganization energy is a relevant parameter in the case of hopping transport; it is defined as the sum of the geometrical relaxation energies of the two molecules involved in the hopping process (one molecule relaxes after going from a charged state to a neutral state, and vice versa). The reorganization energy for **1** was calculated from the potential energy surface and from a normal-mode analysis.[38,39] The quantum-mechanical geometry optimizations and frequency calculations were performed at the DFT-B3LYP level using the 6-31G(d,p) basis set. The reliability of the DFT-B3LYP method to describe the relaxation energy and vibrational properties of organic systems has been established previously.[39,40]

## Results

The single-crystal structure of **1** has been published, and it reveals $\pi$-stacking in a triclinic lattice.[31] The inset to Figure 1a shows the $x$, $y$, and $z$ directions used to characterize the dominant $\pi-\pi$ dimer interaction between molecules in the solid. The interdimer offsets of **1** are 3.34, 1.31, and 3.11 Å for $\Delta x$, $\Delta y$, and $\Delta z$, respectively, reported at 295 K.[35] Figure 1b shows X-ray powder patterns for **1**−**3**, with the first (001) peak labeled with its corresponding $d$ spacing. We will show below that thin films of **1**−**3** pack similarly and adopt a thin film ordering comparable to the packing in the single-crystal structure of **1**.

**Film Morphology.** The film morphology of **1**−**3** was characterized for substrate growth temperatures ($T_S$) from 25 to 205 °C. All three molecules were observed to grow films in a similar manner, with grain size proportional to $T_S$. In films

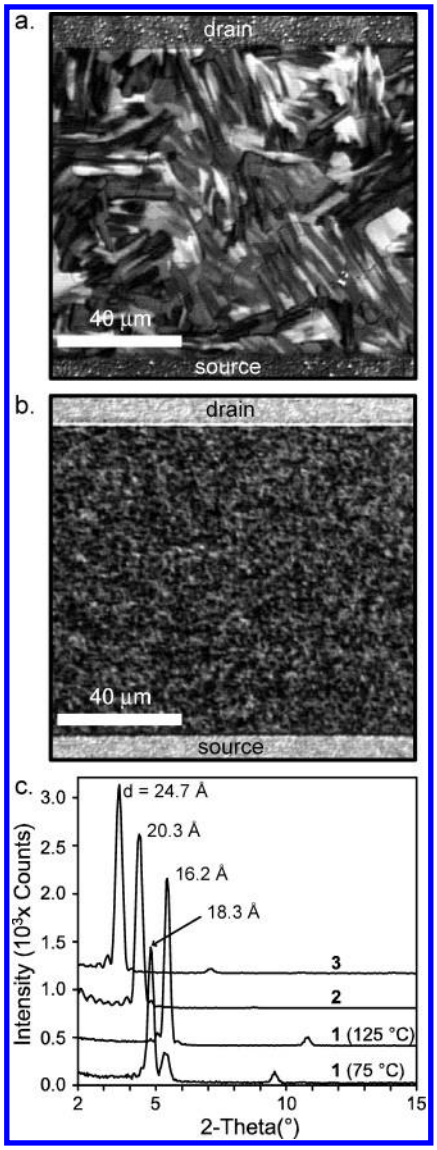


**Figure 2.** (a) Optical micrograph of a film of **2** grown at $T_S = 165$ °C. (b) Optical micrograph of a film of **2** grown at $T_S = 75$ °C. (c) Thin film XRD of **1**−**3** grown at $T_S = 75$ °C. A second trace for **1** grown at $T_S = 125$ °C is also shown.

grown above ∼180 °C the sticking coefficient of the molecules began to decrease significantly, and it was difficult to obtain consistent film growth and TFT performance. In films grown with $T_S = 75$ °C grain sizes were ∼1 $\mu$m. Films grown at elevated $T_S$ included grains as large as 50 $\mu$m. Parts a and b of Figure 2 show differential interference contrast (DIC) optical images of **2** grown at $T_S = 165$ and 75 °C, respectively. Also shown at the top and bottom of the image are the source and drain electrodes of the TFT. In Figure 2a, there is a layered texture that is typical of crystalline organic semiconductor films. Previously reported AFM images of films of **1** established that these layers correspond to molecular terraces in the film, with a terrace height of 16 ± 1 Å.[24] Similar measurements were done for films of **2** and **3** yielding terrace heights of 20 ± 1 and 25 ± 1 Å, respectively.

Films grown with $T_S = 150$ °C revealed significant crack formation. The thermal expansion coefficient for the organic film is more than an order of magnitude greater than the $SiO_2$ substrate. Consequently, upon cooling the film is put under tension and this can cause crack formation. Films with severe cracking yielded TFTs with diminished carrier mobility and significant threshold instability. Film cracking was greatly reduced by slowly cooling (∼1 °C/min) the substrate block to room temperature; the film shown in Figure 2a was tempered in this manner. The liquid crystalline nature of **1**−**3** may allow films to release thermally induced tension and self-heal small cracks.[20] There was no observable morphology, grain size, or packing difference for films grown on $SiO_2$ or PS−$SiO_2$ substrates. The glass transition temperature ($T_g$) of polystyrene films is reported to be ∼110 °C.[41] This may lead to some intermixing of the polystyrene and perylene diimide layers. However, TFTs on both substrates showed equivalent characteristics.

Figure 2c shows typical thin film XRD patterns for **1**−**3** illustrating the crystalline order in the films. XRD patterns for films of **1** grown at $T_S = 75$ and 125 °C are shown in order to illustrate the occurrence of a thin film phase at lower $T_S$. **2** and **3** exhibit no thin film phase at all substrate temperatures investigated. For each molecule **1**−**3** there is a sharp primary peak with a *d* spacing of 16.2, 20.3, and 24.7 Å, respectively, which is very close to the first powder pattern (001) peak, as shown in Figure 1b. **1** and **3** also show a second smaller peak, which is consistent with a second-order reflection (002) of the primary peak.

In thicker films, more high order ⟨00*k*⟩ peaks were observed for **1** and **3**. The AFM determined grain terrace heights of **1**−**3**, which are 16 ± 1, 20 ± 1, and 25 ± 1 Å, respectively, agree closely with the XRD primary peaks for **1**−**3**.

The published single-crystal structure of **1** reveals $\pi$-stacking in a triclinic lattice with a *c*-axis length of 16.3 Å,[35] which corresponds well to the ⟨00*k*⟩ *d* spacing of 16.2 Å we find for thin films of **1**. Therefore, in **1**−**3**, we propose that the ⟨00*k*⟩ film ordering corresponds to single crystal-like packing, with the *c*-axis parallel to the surface normal. In this packing scheme the long axis of the perylene diimide core (*z*-axis) is oriented roughly parallel to the substrate normal, meaning $\pi$-stacking occurs parallel to the substrate surface. This is the optimal packing scheme for charge transport in the OTFT structure.

As previously mentioned, films of **1** grown with $T_S \leq 125$ °C revealed another set of XRD peaks ⟨00*k*′⟩ with *d* spacing = 18.3 Å. In films grown between 20° and 125 °C there was a mixture of both ⟨00*k*⟩ and ⟨00*k*′⟩ peaks, and above 125 °C only ⟨00*k*⟩ peaks were observed. We attribute the ⟨00*k*′⟩ peaks observed at $T_S < 125$ °C to a "thin film" phase of **1**. The thin film phase may be a metastable growth-limited phase or a thermodynamically stable polymorph. Polymorphism and liquid crystalline phase behavior are well documented in the perylene diimide family of molecules,[35,42] and so it is not surprising to observe polymorphism in films of **1**. Similar thin film polymorphs have also been observed in the organic semiconductor pentacene.[43,44] TFTs based on mixed phase films of **1** exhibited slightly inferior transistor performance. For the purposes of this comparative study, $T_S = 75$ °C was used for all films of **1**−**3**, except for $T_S = 165$ °C used to compare large vs small grain TFTs of **2**.

**TFT Characterization.** Top contact, bottom gate TFTs (geometry shown in the inset of Figure 3b) of **1**−**3** (grown at $T_S = 75$ °C) revealed n-channel conduction with linear regime electron mobilities up to 0.1, 0.6, and 0.2 $cm^2/(V\,s)$, respectively. No p-channel conduction was observed to occur for **1**−**3**, even up to −150 V applied gate potential. Figure 3a shows a typical output trace for a TFT based on **2** acquired under a partial pressure of $H_2$ ($10^{-4}$ T). Note the slight hysteresis between the forward and reverse traces (shown by arrows), which indicates a small threshold instability. Figure 3b shows the transfer

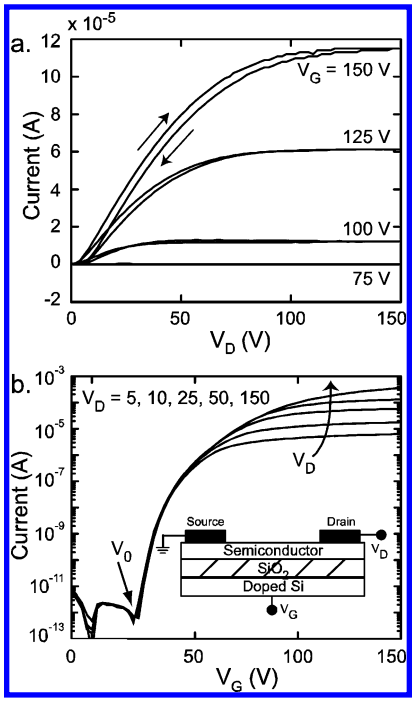


**Figure 3.** (a)Typical output traces ($I_D - V_D$) for a TFT of **2** on PS−$SiO_2$ substrate under $10^{-4}$ Torr of $H_2$. Note the small amount of hysteresis between the forward and reverse trace. Each trace was acquired in ∼2 min. (b) Corresponding (typical) transfer traces ($I_D - V_G$) for various $V_D$. Note the neglible shift in onset voltage ($V_0$) between successive sweeps. Again each trace was acquired in ∼2 min. The inset shows the top contact, bottom gate TFT geometry used for all OTFTs in this work.

characteristics of the same TFT for several drain voltages ($V_D$). The identical onset voltages ($V_0$) in Figure 3b indicate good sweep-to-sweep threshold stability. The large value of the onset voltage (∼25 V) for this particular device is likely due to oxygen induced trap states, which have been studied previously.[24] With careful preparation and quick sample transfer (brief air exposure), it is possible to prepare equivalent devices with a stable onset near 0 V.[24]

TFTs of **1**−**3** with a $SiO_2$ or PS−$SiO_2$ substrate showed equivalent device performance when grown optimally as described in the Experimental Methods section. Initially, TFTs based on $SiO_2$ displayed lower mobility and more device-to-device variation than TFTs on PS−$SiO_2$. We determined this was because the film was being deposited too quickly (0.2−0.3 Å/s) in the early stages of deposition. As it turns out, when a lower deposition rate (∼0.01−0.02 Å/s) is used for the first three monolayers, both $SiO_2$ and PS−$SiO_2$ yield equivalent TFTs. Perhaps these observations reflect a difference in the surface diffusivity of **1**−**3** on PS−$SiO_2$ vs $SiO_2$, which would impact the crystal packing in the first few *critical* layers which form the OTFT channel.

Films of **2** grown at $T_S = 165$ °C show grains as large as 30 $\mu$m with an average grain size of ∼ 15 $\mu$m (Figure 2a), whereas for $T_S = 75$ °C the average grain size is ∼1 $\mu$m (Figure 2b). Intuitively, we would predict that TFTs based on the large grain films would have a higher mobility; however, this is not the case. Typical large grain TFTs of **2** had lower mobility (0.1−0.2 $cm^2/(V\ s)$) and more device-to-device variation than small grain TFTs. Similar results were obtained with **1** and **3**. Knipp et al. also observed that room temperature mobility was not significantly affected by large grain size differences in pentacene TFTs made in their lab.[45]

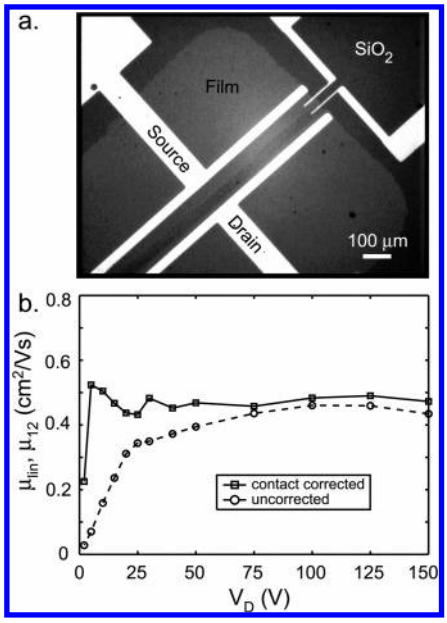


**Figure 4.** (a) Optical microscope image of a four-probe TFT based on **2**. (b) Linear regime mobility ($\mu_{lin}$) and contact corrected linear regime mobility ($\mu_{12}$) as a function of $V_D$, calculated from the data shown in Figure 3b.

**Mobility Corrected for Contact Resistance.** Four-probe transistor measurements may be used to determine the effect of contact resistance on device performance in both amorphous silicon[46] and organic semiconductor TFTs.[4,24,47,48] Figure 4a shows an optical micrograph of the four-probe TFT geometry (actual device) used to estimate contact resistance in this paper. The sense probes float at voltages ($V_1$, $V_2$) corresponding to the channel voltage at the probe positions; thus, the voltage drop at the source and drain electrodes (due to carrier injection barriers or access resistance through the film thickness) can be determined by extrapolating the channel voltage gradient back to the source and drain. Recently, this technique has been used to thoroughly characterize TFT contact resistance in films of **1** as a function of temperature and contact metallurgy.[37] Sense probe data are only valid for characterizing contact resistance in the linear regime of TFT operation; in the saturation regime, the pinch-off effect (nonuniform channel electric field) makes the voltage profile nonlinear.

Correcting the linear regime mobility for contact resistance is possible using a method similar to that of Kanicki et al.,[49] which starts with the linear regime source-drain current equation

$$I_D = \mu_{lin}\frac{W}{L}C_i(V_G - V_T)V_D - \frac{V_D^2}{2} \qquad (1)$$

where $C_i$ is the insulator capacitance per unit area, $W$ is the channel width, and $L$ is the channel length. This equation is mapped into terms parametrized in channel probe variables

$$\frac{I_D}{V_{12}} = \mu_{12}\frac{W}{L_{12}}C_i(V_G' - V_T), \qquad (2)$$

where $V_{12} = V_2 - V_1$, $L_{12} = L_2 - L_1$ (the distance between the sense probes), $\mu_{12}$ is the contacted corrected linear mobility, and $V_G' = V_G - (V_1 + V_2)/2$ (i.e., $V_G'$ is the average gate voltage between the sense probes). The corrected mobility $\mu_{12}$ is found

directly from the derivative of eq 2 with respect to $V_G'$ according to eq 3,

$$g_M' = \frac{d\left(\frac{I_D}{V_{12}}\right)}{dV_G'} = \mu_{12}\frac{W}{L_{12}}C_i. \quad (3)$$

Figure 4b presents a comparison of the uncorrected and corrected linear regime mobilities as a function of drain voltage for the transfer curves corresponding to Figure 3b (some $V_D$'s omitted for clarity).[50] The uncorrected mobility $\mu_{lin}$ is observed to increase steadily with increasing $V_D$ up to $\sim 0.45$ cm$^2$/(V s), whereas $\mu_{12}$ is $\sim 0.5$ cm$^2$/(V s) and is basically invariant with $V_D$. We attribute the increase in $\mu_{lin}$ with $V_D$ to contact resistance effects due to Schottky barrier lowering and/or space charge injection through the ungated semiconductor between the top contacts and the channel. In a top contact TFT, the ungated semiconductor resistance (also called access resistance) can be far greater than the Schottky barrier resistance. The access resistance is generally reduced by space charge transport induced by extremely high fields (1 V/30 nm $\sim 3 \times 10^6$ V/cm). Because $\mu_{lin}$ and $\mu_{12}$ agree well at high $V_D$ we conclude the contact correction is not as important at high $V_D$ as compared to low $V_D$.

When $V_D \geq (V_G - V_T)$, the TFT current is observed to saturate upon increasing $V_D$, as shown in the high $V_D$ portion of Figure 3a. The saturation regime current is described by the following

$$I_{D,sat} = \frac{W}{2L}C_i\mu_{sat}(V_G - V_T)^2 \quad (4)$$

where all values are defined as in eq 1, and $\mu_{sat}$ is the saturation regime mobility. We have found that $\mu_{sat}$ can be as high as 1.7 cm$^2$/(V s) in our best device, and typically (but not always) $\mu_{sat}$ is greater than $\mu_{lin}$. Dimitrakopoulos et al. point out the often overlooked discrepancy between saturation and linear regime mobility in OTFTs[48] and attribute the discrepancy to a breakdown in the assumptions used to derive the TFT equations. Understanding this in detail will require further work, but it is common to ascribe increased $\mu_{sat}$ values to the effects of contact resistance which is less likely to limit the drain current in the saturation regime than in the linear (fully on) regime (i.e., at high gate voltages, the ratio of the channel resistance to contact resistance decreases so the current depends more heavily on the contact properties). Contact resistance is not accounted for in any of the equations above. However, in our experience the discrepancy in the two types of mobility values cannot be attributed to contact effects, because the contact corrected linear mobility, $\mu_{12}$, is still often lower than $\mu_{sat}$. Unfortunately, using our current four probe geometry, we cannot also accurately correct the saturation mobility because the potential profile is not linear.

**Dependence of Mobility on Gate Voltage.** Figure 5a shows both the contact corrected channel conductance ($I/V_{12}$) and the square-root of the drain current vs $V_G$ for a TFT of **2** with a PS−$SiO_2$ insulating layer. The mobilites $\mu_{12}$ and $\mu_{sat}$ are proportional to the local slope of these two traces, respectively. Figure 5b shows mobility vs gate voltage for the corresponding curves in Figure 5a. In both cases, the mobility peaks at ~0.55 cm$^2$/(V s) just above threshold, and proceeds to fall by more than a factor of 2. The nonmonotonic behavior is indicative of the curvature in the traces in Figure 5a. Both of these traces should be linear if the mobility were gate voltage independent. Importantly, the peak in the mobility plots did not depend on the precise value of $V_D$, which eliminates ohmic heating of the film as the cause of the unusual dependence. Nor can the peak be attributed to threshold voltage shift during device operation. Over the 2 min time scale of an $I_D - V_G$ trace, the current hysteresis we observed was less than 10%. The gate voltage dependence of the mobility will be considered in more detail in the Discussion section.

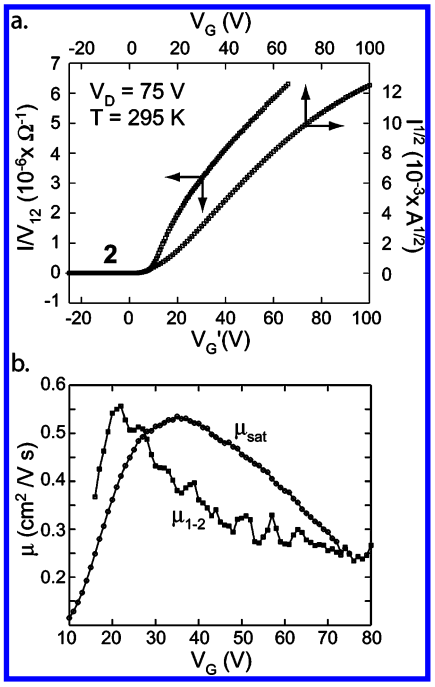


**Figure 5.** (a) Left and bottom axes showing a plot of contact corrected channel conductance ($I/V_{12}$) vs channel gate voltage ($V_G'$) for a TFT of **2**. This entire data set is in the linear regime. The right and top axes show a plot of $(I_D)^{1/2}$ vs $V_G$. This entire data set is in the saturation regime. The local slope of each plot is proportional to the corresponding linear and saturation regime mobility. (b) Plot of contact corrected linear and (uncorrected) saturation regime mobility vs gate voltage for the data in Figure 5a, calculated from the local slopes. In both cases, the mobility increases to a maximum at low gate voltage and then decreases with increasing gate voltage.

**TABLE 1: Summary of Room-Temperature TFT Mobility ($\mu_{12}$, $\mu_{Lin}$, $\mu_{Sat}$) and Contact Resistance ($R_CW$) Data for 1−3 on PS−$SiO_2$ Substrate**

| TFT | $\mu_{12}$[a] (cm$^2$/Vs) | $\mu_{lin}$[a] (cm$^2$/Vs) | $\mu_{sat}$[b] (cm$^2$/Vs) | $R_CW$[c] (Ω cm) |
|---|---|---|---|---|
| **1** | 0.073 | 0.044 | 0.055 | $1.30 \times 10^5$ |
| **2** (75 °C) | 0.55 | 0.14 | 1.3 | $1.60 \times 10^4$ |
| **2** (165 °C) | 0.12 | 0.075 | 0.22 | $4.70 \times 10^4$ |
| **3** | 0.23 | 0.14 | 0.52 | $3.20 \times 10^4$ |

[a] Linear regime mobility ($\mu_{12}$ and $\mu_{lin}$) calculated for $V_D = 10$ V. [b] Saturation regime mobility ($\mu_{sat}$) calculated for $V_D = 75$ V. [c] Contact resistance calculated for $V_D = 10$ V and $V_G = 100$ V.

Table 1 summarizes the room-temperature mobility ($\mu_{12}$, $\mu_{lin}$, and $\mu_{sat}$) values and corresponding specific contact resistances ($R_CW$) for OTFTs based on **1**−**3** with PS−$SiO_2$ substrates. TFTs of **1**−**3** generally follow the trend that $\mu_{sat} > \mu_{12} > \mu_{lin}$, despite the contact resistance correction used to calculate $\mu_{12}$. However, in some devices at smaller drain voltages $\mu_{12}$ was greater than $\mu_{sat}$. The mobility values reported in Table 1 are the maximum observed values (in $V_G$) for a set of four devices of each type (molecule/$T_S$). Table 1 shows specific results that are consistent with the typical trend of $\mu_{12} = 0.1$, 0.6, and 0.2 cm$^2$/(V s) for **1**−**3**, respectively, mentioned in the Introduction. This trend was found for many (~20) devices of each type characterized in our laboratory. Similar to previous results on pentacene TFTs,

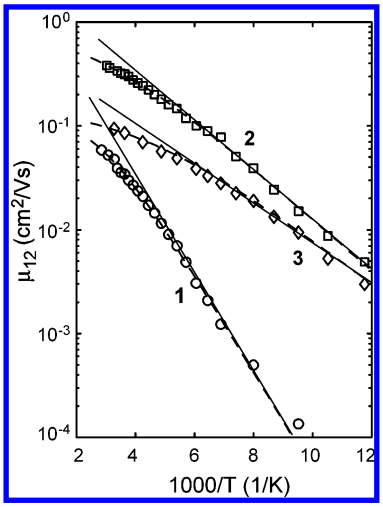


**Figure 6.** Arrhenius plot of contact corrected linear regime mobility ($\mu_{12}$) vs $1/T$ for **1**−**3**. The corrected linear mobilities were determined at large gate voltages where the gate voltage dependence is weak. The dashed lines are least-squares fits to eq 9, which assumes the MTR transport model and a single trap level.

the specific contact resistance ($R_C W$) of **1**−**3** is lower in TFTs with higher carrier mobility.[52]

**Variable Temperature TFT Characterization.** Variable temperature mobility measurements are a well-established method for examining the mechanism of charge transport in semiconductors. In highly ordered, covalently bound semiconductors such as single-crystal silicon, it is widely accepted that charge carriers move in a delocalized manner (band transport); the dominant temperature effect on charge transport is scattering via lattice phonons, which produces a $T^{-m}$ dependence in mobility ($\mu \propto T^{-m}$), where $1 \leq m \leq 3$.[53] For weakly bound solids (most organic semiconductors) like **1**−**3**, the mechanism of charge transport is not as clear.[54,55] Ignoring any extrinsic (physical/impurity) defects, the nature of the charge carrier, whether localized by intrinsic (traplike) polarons, or delocalized in classic bands and/or polaron bands is still a disputed subject.[56,57] Adding the inevitable existence of extrinsic trap states within the band gap complicates the picture even more. Extrinsic traps especially complicate the interpretation of temperature-dependent conduction data because of their effect on the free charge carrier concentration.

Organic TFTs generally yield mobilities that are activated as a function of temperature with characteristic activation energies of tens to hundreds of millielectronvolts.[34,58−61] Recently, two models have been used to explain variable temperature transport in OTFTs: (1) variable range hopping (VRH)[62] and (2) multiple trapping and release (MTR) based on bandlike transport with a shallow distribution of trap states.[58,63] It should be noted that neither model explicitly defines the nature of the charge carrier or trap state (extrinsic, intrinsic). Figure 6 presents contact corrected linear regime mobility ($\mu_{12}$) vs inverse temperature for TFTs of **1**−**3** (grown with $T_S = 75$ °C). At low temperature the TFTs are thermally activated, as indicated by the straight line on the Arrhenius plot. Using the Arrhenius fit (not shown) over the entire data set yields $E_A$ of 85, 44, and 39 meV, for **1**−**3**, respectively. Yet, these $E_A$ values are underestimated because we have ignored the roll-off in $\mu_{12}$ at high temperature. A better Arrhenius fit is shown for the low-temperature data only, and it yields values of 91, 50, and 44 meV, respectively. Both VRH and MTR predict activated transport ($\mu \propto \exp[-E_A/kT]$). However, the observed high-temperature roll-off has also been reported and explained in

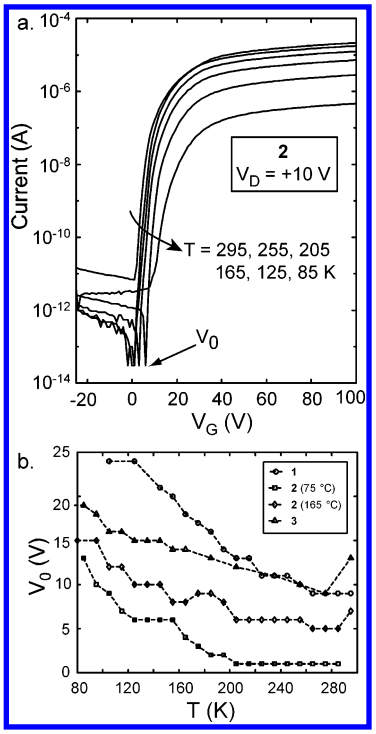


**Figure 7.** (a) Transfer curves for a TFT of **2** as a function of temperature. Note the shift toward more positive onset voltage ($V_0$) with decreasing temperature. (b) Summary of onset shift with temperature for TFTs of **1**−**3**, corresponding to the devices in Table 1.

p-channel OTFTs using the MTR model with shallow traps ($E_A < 100$ meV).[45]

**Shift of Onset Voltage with Temperature.** Figure 7a shows transfer curves for variable temperature TFT measurements of **2**, using a PS−$SiO_2$ substrate. There is a significant shift in the onset voltage ($V_0$) with decreasing temperature. Figure 7b shows the onset voltage as a function of temperature for the TFTs summarized in Table 1. Each device displays a positive onset shift ($\Delta V_0$) from its room-temperature $V_0$. In the framework of MTR, at lower temperature there is less thermal energy available to promote trapped carriers into delocalized (mobile) states.

Consequently, at lower temperature, more carriers remain trapped and the TFT requires an increased gate voltage to achieve the onset of conduction. It should be noted that onset voltage shifts would only affect traps located furthest from the conduction band edge, i.e., deep traps. A quick calculation of $\Delta V_0 C_i$ yields a value of $\sim 1 \times 10^{12}$ trapped carriers/cm$^2$, using a value $\Delta V_0 = 15$ V. This is a significant number of traps, particularly when considering that the areal density of perylene diimide molecules in the TFT plane is $\sim 2 \times 10^{14}$/cm$^2$.

**Dependence of Activation Energy on Gate Voltage.** To investigate the gate voltage dependence of the activation energy, we use the transconductance ($g_M$)

$$g_M = \left.\frac{\partial I}{\partial V_G}\right|_{V_D} \propto \mu_{lin} \qquad (5)$$

defined at constant $V_D$. $g_M$ is directly proportional to the device mobility in the linear regime, and provides a convenient quantity to investigate the gate voltage dependence of TFT activation energy. Figure 8a shows an Arrhenius plot of $g_M$ at various gate voltages for a TFT based on **1**, which can be used to determine $E_A$ as a function of gate voltage. The lines shown are least-squares fits used to extract the activation energy. Figure 8b shows activation energy as a function of gate voltage (from

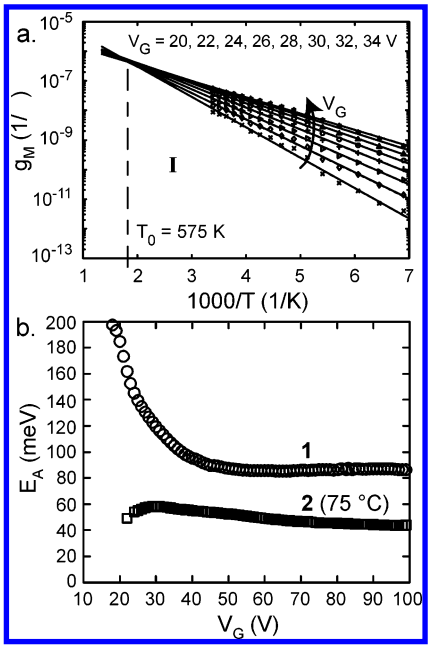


**Figure 8.** (a) Arrhenius plot of the transconductance ($g_M$) of **1** at $V_D$ = 10 V for gate voltages between 20 and 34 V. (b) Activation energy as a function of gate voltage for TFTs of **1** and **2**.

$g_M$) for the corresponding data for **1** (Figures 8a) and a TFT based on **2**. For both **1** and **2**, the activation energies are greatest just above threshold and fall monotonically toward limits of 87 and 48 meV, respectively, in good agreement with the activation energy values extracted from Figure 6.

Further inspection of Figure 8a reveals an isokinetic point with a characteristic temperature ($T_0$) of 575 K, which is illustrated by extending the least-squares lines back to a single intersection point. Typically, TFTs of **1** and **2** displayed isokinetic temperatures at gate voltages just above threshold. We did not observe a clear isokinetic temperature for **3**, though the measured activation energies did decrease with $V_G$.

**Quantum Chemical Calculations.** To better understand the conditions for bandlike (delocalized) or hopping (localized) conduction to occur in **1**−**3**, we have performed calculations to provide quantitative estimates of important parameters governing each regime. For simplicity, we have used **1** as a model compound, which is well justified given the similar chemical structure and thin film packing adopted by **1**−**3**.

The key parameters governing hole and electron transport in the band regime are the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) transfer integrals, $t_{HOMO}$ and $t_{LUMO}$, respectively.[64,65] Using the tight binding approximation, we find that significant electronic splitting is obtained along the **a** and **d** directions, which are shown in the inset of Figure 9 (**a** and **b** are the unit cell axes for **1**).

Interestingly, these two directions define a plane that is identical to the plane of transport in TFTs of **1**−**3**. By calculating the valence and conduction bandwidths for a group of N molecules we are able to estimate the full bandwidth for an infinite stack. Figure 9 is a plot of the calculated HOMO and LUMO bandwidths for the **a** and **d** directions. The excellent linear match to $\cos(\pi/(N+1))$ indicates that the splitting calculated for large clusters at the INDO level is dominated by interactions between adjacent molecules (dimers). From the fit, we can estimate the bandwidth along the **a** and **d** directions and for the two-dimensional plane which includes **a** and **d**.[66] Table 2 summarizes the bandwidth calculation results.

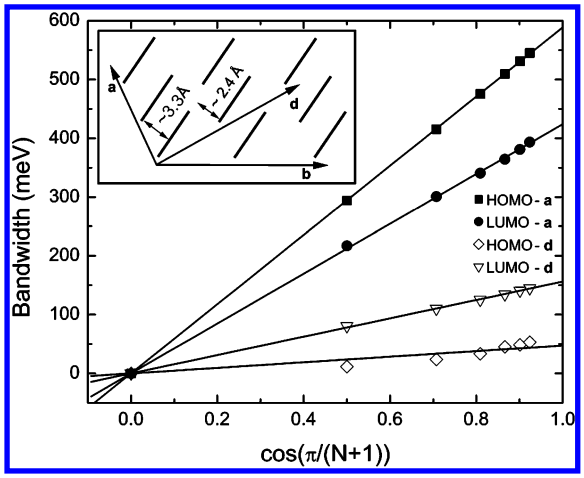


**Figure 9.** Evolution of the bandwidths formed by the HOMO and LUMO levels of **1** along the **a** and **d** directions as a function of $\cos(\pi/(N+1))$. $N$ is the number of interacting molecules in a stack, and the maximum bandwidth occurs at $\cos(\pi/(N+1)) = 1$ (very large $N$). Bandwidths calculated in other directions are vanishingly small. The inset shows the **d** direction with respect to the crystallographic unit cell directions **a** and **b**.

**TABLE 2: Bandwidth along the a and d Directions, and in the Plane Including a and d (Total)**

| direction | valence bandwidth (meV) | conduction bandwidth (meV) |
|---|---|---|
| **a** | 589 | 422 |
| **d** | 47 | 155 |
| total | 636 | 577 |

The total bandwidth exactly corresponds to the sum of bandwidths in the **a** and **d** directions, and indicates that the large overlap between molecules in these directions is the most important overlap in the plane. We note that these bandwidth values are close to those obtained for pentacene (608 and 588 meV for the valence and conduction bandwidths, respectively) using the same approach.[65] The valence bandwidth is similar to the conduction bandwidth, which suggests that in the absence of traps, holes should be as mobile as electrons. However, TFTs of **1**−**3** show only n-channel mobility, so it seems likely that traps play a major role in the conduction.

Figure 9 shows that the HOMO (valence) bandwidth is larger than the LUMO (conduction) bandwidth in the **a** direction, while the reverse holds true in the **d** direction. This result was studied in detail by Kazmaier and Hoffmann for perylene diimide dimers using the extended Hückel semiempirical molecular orbital method.[67] In fact, the bandwidth is determined not only by the degree of overlap between adjacent molecules but also by the nodal characteristics of the HOMO and LUMO orbitals of the individual molecules.[64,67] By studying the effect of the translations along the long molecular axis (Figure 1a, *z*-axis), Kazmaier and Hoffmann concluded that some intermolecular orientations can lead to small valence and/or conduction bandwidths. We used the INDO method to do an analogous study and obtained similar trends.

In the hopping (localized) regime the interchain transfer integral remains important, but another parameter starts playing a major role, the reorganization energy ($\lambda$). We have calculated the intramolecular contributions to $\lambda$ for electrons and holes using density functional theory at the B3LYP level (see Experimental Methods). The reorganization energies of **1** are 272 and 163 meV for electrons and holes, respectively. In the case of electrons, the vibrational analysis indicates that 11% of the total reorganization energy is associated with low-frequency

modes (frequency smaller than 500 $cm^{-1}$), whereas for holes the corresponding value is 20%. It is worth noting that the reorganization energy for electrons is nearly twice as small as the one we have calculated for silole derivatives considered as good electron transport material.[68]

The large bandwidth calculated for electrons (577 meV) in **1** indicates that intermolecular overlap is significant and the bandlike MTR model of transport can be suitable for describing TFTs of **1**−**3**. The following discussion section will interpret the previous TFT results in terms of MTR transport.

## Discussion

**Effects of Grain-Size, Surface Chemistry, Contact Resistance, and Air Exposure.** Comparison of TFTs of **2** grown at 165 and 75 °C (large vs small grains, Figure 2, parts a and b, respectively) reveals that small grained films have larger room-temperature electron mobility than large grained films, even though the activation energies are similar ($E_A \sim 50$ meV). We attribute the decreased room temperature mobility in large grain films to thermally induced cracking, despite our best efforts to minimize crack formation. The presence of cracks in large grained films prevents us from making firm conclusions about the role of grain boundaries on conduction in OTFTs based on **1**−**3**.

Films of **1**−**3** grown on $SiO_2$ and PS−$SiO_2$ revealed no significant difference in TFT performance, though at moderate deposition rates (∼0.5 Å/s) growth on PS−$SiO_2$ was more favorable and led to a larger fraction of better performing TFTs. Initially, TFTs grown on $SiO_2$ showed inferior performance; however, a slower growth procedure (Experimental Methods) led to equivalent performance on the two substrates. We conclude that interfacial trap states due to specific chemical interactions at the semiconductor−dielectric interface are not a major factor in charge transport in our devices, although carrier trapping due to some other mechanism clearly occurs, as discussed below.

Figure 4b shows typical drain voltage dependences of $\mu_{lin}$ and $\mu_{12}$. It makes sense that increasing the drain voltage improves the apparent device mobility, $\mu_{lin}$, by reducing the effective contact resistance. The conclusion that contact resistance plays a role in these devices is supported by the observation that $\mu_{12}$ is roughly equivalent to $\mu_{lin}$ at high drain voltage, and $\mu_{12}$ is relatively unaffected by increasing drain voltage as shown in Figure 4b.

Characterizing TFTs of **1**−**3** under a reducing atmosphere ($10^{-4}$ Torr of $H_2$) greatly improved the threshold voltage stability. This effect was reported previously and attributed to trap formation in TFTs of **1** due to oxygen exposure.[24] A similar effect is likely to occur in TFTs of **2** and **3**, and we have directly observed air induced threshold shifts (tens of volts over ∼5 min) in TFTs of **2** and **3**. Further study is needed to quantify the changes in transport properties as a function of $O_2$ partial pressure and exposure time.

**Temperature-Dependent Transport and Multiple Trapping and Release.** As shown in Figure 6, TFTs of **1**−**3** exhibit activated transport at low temperature, which deviates (rolls-off) from the Arrhenius fit at higher temperature. Similar results on other organic semiconductors have been reported and attributed to shallow traps.[45,69] As shown in Figure 7, there is a significant onset voltage shift with decreasing temperature. This shift is indicative of carrier trapping in deep trap states, which screens the gate field and consequently results in more gate voltage required to achieve the onset of conduction. Because of these obvious indications that traps play a major role in TFTs of **1**−**3**, and because of the relatively large electronic bandwidth we obtained from quantum chemical calculations, we chose the MTR model for describing transport in TFTs of **1**−**3**.

MTR supposes that charge transport in the semiconductor is dominated by recurrent trapping into localized (zero mobility) band-tail "trap" states below the conduction band edge followed by thermal release of the carriers into delocalized states. MTR was used extensively to describe the dispersion of transit times observed in time-of-flight measurements on amorphous materials[28,70] and is an important model used to describe conduction in amorphous silicon TFTs.[27] The present manifestation of MTR originated from a model described as "trap-limited band transport",[29] which is a more apt description for the type of steady-state transport that occurs in TFTs.

MTR proposes that the effective mobility ($\mu_{eff}$) of a TFT is the free carrier mobility ($\mu_0$) multiplied by the ratio ($\Theta$) of free charge density ($N_C$) to total ($N_C + N_T$) induced charge ($N_T$ is the concentration of trapped charges), which leads to

$$\mu_{eff} = \mu_0\Theta = \mu_0\frac{N_C}{N_C + N_T} = \mu_0\frac{1}{1 + \frac{N_T}{N_{C0}}\exp\left(\frac{E_C - E_F}{kT}\right)} \quad (6)$$

where $N_C$ is defined by

$$N_C = N_{C0}\exp\left(\frac{-(E_C - E_F)}{kT}\right). \quad (7)$$

$N_{C0}$ is the effective density of states at the conduction band edge ($E_C$), and $E_F$ is the Fermi level. Here we have assumed Boltzmann statistics which is correct provided that $(E_c - E_F) > \sim 3kT$.

For the sake of simplicity, let us assume a single trap state at energy $E_T$ that captures electrons according to Boltzmann statistics. The trap occupation is then

$$N_T = N_{T0}\exp\left(\frac{-(E_T - E_F)}{kT}\right) \quad (8)$$

where $N_{T0}$ is the density of available trap states (no./$cm^2$). Combining eqs 6 and 8 yields an Arrhenius-like form for the temperature dependence of the effective mobility:

$$\mu_{eff} = \mu_0\frac{1}{1 + \frac{N_{T0}}{N_{C0}}\exp\left(\frac{E_C - E_T}{kT}\right)} \approx \mu_0\exp\left(\frac{-E_A}{kT}\right) \quad (9)$$

where $E_A$ is the difference in energy between the discrete trap state and the conduction band edge ($E_C - E_T$). In the approximation, we have assumed that $E_A \gg kT$ (Boltzmann-like assumption) and $N_{C0} \sim N_{T0}$. This simple, single trap level interpretation of the MTR model predicts activated behavior for the effective mobility, with an activation energy equal to the trap depth, ($E_C - E_T$).

The dashed lines shown in Figure 6 correspond to a least-squares fit of the data to eq 9, where $\mu_0$, $N_{T0}/N_{C0}$, and ($E_C - E_T$) are fitting parameters. Equation 9 yields a reasonable fit to the high-temperature roll-off from Arrhenius behavior (Figure 6), which supports our use of the MTR transport model. In the MTR picture, the reason the roll-off occurs is that at high temperatures the thermal energy ($kT$) becomes comparable to the trap depth, $E_C - E_T$. Table 3 summarizes values obtained from fits of eq 9 to the variable temperature TFT results on

**TABLE 3: Summary of Fit Parameters Using Eq 9 for TFTs of 1−3 on $SiO_2$, and Observed Meyer−Neldel Energies ($E_{MN}$)**

| TFT | $\mu_0$ ($cm^2$/Vs) | $E_A$ (meV) | $N_{T0}/N_{C0}$ | $E_{MN}$ (meV) |
|---|---|---|---|---|
| **1** | 0.39 | 91 | 0.31 | 54 |
| **2** | 1.05 | 50 | 0.33 | 67 |
| **3**[a] | 0.55 | 44 | 0.22 | 6.8[b] |

[a] Measurements for **3** were taken down to 50 K. [b] The isokinetic point ($kT_0 = E_{MN}$) for **3** was not evident using 1 V transfer ($V_G$) steps. However, the $V_0$ shift in Figure 7a (below) implies the existence of trap states because of the positive shift with decreasing temperature.

**1**−**3**. We note that the $E_{MN}$ energy for films of **1** is somewhat larger than the value (25 meV) we reported previously for films of **1** on $Al_2O_3$ gate dielectric.[24] We attribute the different $E_{MN}$ values to differences in trap distributions for **1** on $Al_2O_3$ vs the $SiO_2$ used here.

It is interesting that the ratio of trap to conduction band states ($N_{T0}/N_{C0}$) is as high as 0.33, as this implies there is one trap for every three conduction states in a TFT of **2** (i.e., $\sim 6 \times 10^{13}$/$cm^2$). However, eq 9 is an oversimplification because it assumes a single level trap, and so trap densities derived in this manner are suspect. The fit to eq 9 does provide an explanation for the high-temperature roll-off in $\mu_{12}$ and indicates the shallow trap densities are high. A more detailed analysis that incorporates a more realistic trap distribution and degenerate statistics is in progress.

**Gate Voltage Dependence of the Activation Energy and Isokinetic Temperature.** In Figure 8b, there is an interesting decrease in the transport activation energy with increasing gate voltage for TFTs of **1** and **2**, and a similar dependence was also observed for **3**. The MTR transport model is able to explain this effect if there is a distribution of traps within the band gap of the organic semiconductor. Typically, an exponential distribution ($n_T$) of traps is assumed

$$n_T(E) = \frac{N_{t0}}{kT_0} \exp\left(\frac{-(E_C - E)}{kT_0}\right) \tag{10}$$

where $N_{t0}$ is the density of traps states at $E = E_C$ (no./$cm^2$), and $kT_0$ characterizes the width of the distribution. In this case, the observed activation energy in the TFT is a convolution of both trap depth and distribution. The applied gate voltage in the TFT moves the Fermi level through the trap distribution, closer to the band edge, and so the thermal energy required to hop into the conduction band decreases with increasing gate voltage. This leads to a gate voltage dependence of the activation energy.

A consequence of assuming the MTR model with an exponential distribution of trap states is that the Meyer−Neldel relationship (MNR) will hold.[71] The MNR is the relationship between a thermally activated quantity ($X$, e.g., mobility or conductance), its activation prefactor ($X_0$), and its activation energy

$$X = X_0 \exp\left(-\frac{E_A}{kT}\right) \tag{11}$$

$$X_0 = X_{00} \exp\left(\frac{E_A}{kT_0}\right) \tag{12}$$

where $kT_0$ is the width of the trap distribution and is often called the Meyer−Neldel energy ($E_{MN} = kT_0$). The MNR is observed in a wide variety of materials for a number of different physical quantities.[72] Several authors have observed an MNR for TFT derived transport related quantities.[73−75]

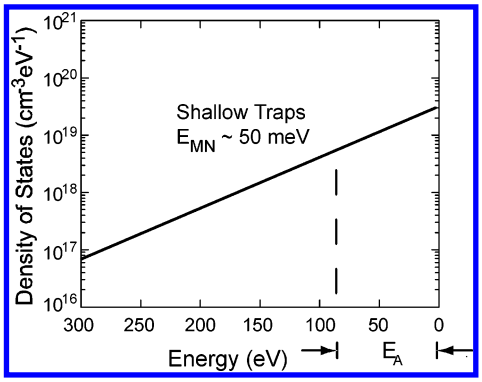


**Figure 10.** Estimated density of localized states (traps) near the conduction band edge (at $E = 0$ eV) for TFTs of **1**−**3**. A gate voltage sweep moves the Fermi-level through the trap distribution.

The MNR is observed graphically by extrapolating the Arrhenius lines to a point of intersection, which is the isokinetic temperature shown in Figure 8a. An isokinetic point indicates a well-defined charge transport mechanism in which the gate voltage modulates the effective activation barrier for transport. In this case, we have assumed (as seems reasonable) that there is an exponential distribution of trap states and, as indicated above, increasing the gate voltage lowers the activation energy by systematically moving the Fermi level higher in the distribution. Table 3 summarizes the trap distribution widths ($E_{MN}$) obtained for TFTs of **1** and **2**. It is likely that TFTs of **3** also contain a trap distribution, however, we did not observe a well-defined isokinetic point and so we do not have an estimate of $E_{MN}$. Figure 7b shows the onset voltage shift (deep trap indicator) with temperature is less than 10 V for **3**, the smallest shift in all TFTs studied.

Figure 10 is a schematic of a postulated exponential trap distribution for films of **1**−**3**. This distribution has been estimated using a representative trap width, $E_{MN}$, and an estimate of $N_{t0}/E_{MN}$ (see eq 10).[76] The true trap distribution is likely to be more complex, and in the case of a-Si:H films, it has often been found that two exponential distributions (shallow and deep) provide a better fit to the transport data.[77] However, our observation of a single isokinetic point suggests that over the temperatures and gate voltages we probed, a single, well-defined trap distribution was sampled. We emphasize that we have assumed that the distribution is exponential, but its true functional form is not determined by our data.

**Dependence of Mobility on Gate Voltage.** In Figure 5 we show data for a TFT of **2** where both the saturation and contact corrected linear regime mobility *increase* and then *decrease* with increasing gate voltage. Similar results are obtained for TFTs of **1** and **3**. MTR is able to explain the observed mobility increase with increasing gate voltage. Increasing the gate voltage moves the Fermi level through the trap distribution, which increases the ratio of free carriers to total carriers ($\Theta$), and consequently increases the effective mobility ($\mu_{eff} = \Theta(V_G)\mu_0$). Shur et al. have used MTR to explain the increasing mobility in amorphous silicon TFTs.[78] Interestingly, a similar dependence is also predicted by the VRH transport model.[62]

In contrast, the observed decrease in mobility with increasing gate voltage is an interesting result, and to the best of our knowledge has only been mentioned by two other groups.[79,80] It is important to note that without a contact resistance correction, it is possible to interpret a decrease in mobility with increasing gate voltage as a symptom of large contact resistance,

which becomes more important as the channel becomes less resistive at high gate voltages. However, we still observe a decrease in the contact-corrected $\mu_{12}$, which eliminates contact resistance as the cause of the $\mu - V_G$ behavior. Furthermore, heating effects can also be discounted because Figure 5b plots are independent of drain voltage; i.e., increasing $V_D$ may increase the film temperature by ohmic heating, but this does not change the mobility vs $V_G$ dependence. Finally, we have noted already that the peak in mobility vs gate voltage data is not the result of threshold voltage shifts (gate bias stress) during device operation as we observed current hysteresis of less than 5% between the forward and reverse gate voltage sweeps.

Although it appears that nonmonotonic variation of mobility with $V_G$ in OTFTs is not widely recognized, it is well-known in single-crystal silicon metal-oxide-semiconductor field effect transistors (MOSFETs).[32] In MOSFETs, the decrease of mobility with increasing gate voltage is attributed to enhanced scattering of carriers resulting from their confinement to a progressively thinner channel at the semiconductor-dielectric interface as the gate field becomes large. A somewhat different mechanism may be operative in TFTs of **1**−**3**. Horowitz has postulated that the layer of molecules adjacent to the insulator has the most traps, and subsequent molecular layers have improved packing and hence fewer traps.[80] As the gate voltage increases, the first layer closest to the insulator has a higher proportion of the induced charge. Charge confined to the first layer will encounter more traps than charge moving in layers further from the insulator interface, and consequently, the average effective mobility for the device will be lower as the gate voltage increases.

The nonmonotonic dependence of mobility with gate voltage illustrates that the basic MTR transport model must be modified to describe operation of OTFTs based on **1**−**3**. However, the MTR transport model explains several experimental observations: (1) the increase in mobility with increasing gate voltage just above threshold (Figure 5); (2) the high-temperature roll-off in the Arrhenius plot of mobility vs temperature for **1**−**3** (Figure 6); (3) the significant positive shift of onset voltage with decreasing temperature for **1**−**3** (Figure 7); (4) the decrease in $E_A$ with increasing gate voltage (Figure 8c); (5) the presence of isokinetic temperatures in Arrhenius plots of the tranconductance (Figure 8a,b).

## Conclusion

We have studied variable temperature transport in a family of high electron mobility perylene diimide based thin film transistors. We observed similar molecular packing in thin films of **1**−**3**, with molecules oriented so that $\pi$-stacking occurs in the plane of TFT conduction. We have observed room-temperature saturation electron mobility ($\mu_{sat}$) up to 1.7 cm$^2$/(V s) in TFTs based on **2**; however, because of deep trapping and contact resistance we caution against using $\mu_{sat}$ as the sole measure of semiconductor quality. Instead, we used a four-probe technique to measure the contact corrected linear regime mobility ($\mu_{12}$), which is approximately 0.6 cm$^2$/(V s) for TFTs based on **2**.

We used the multiple trapping and release (MTR) transport model to analyze our results and find it convincingly explains several gate voltage and temperature related TFT phenomena. The MTR model assumes trap-limited band transport, and quantum chemical calculations verified that delocalized transport is likely in perylene diimides; the estimated conduction bandwidth is 577 meV for **1**. However, the MTR model does not account for all of our observations, in particular the nonmonotonic dependence of mobility on gate induced charge density.

Overall, we have shown that perylene diimide based n-channel OTFTs yield mobilities competitive with pentacene p-channel OTFTs. Because the perylene diimide family of molecules are soluble in many organic solvents, they offer the prospect of high mobility solution deposited TFTs. Future work will focus on characterization of solution deposited films, thorough analysis of air sensitivity, and determination of structure-transport relationships in this family of compounds.

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