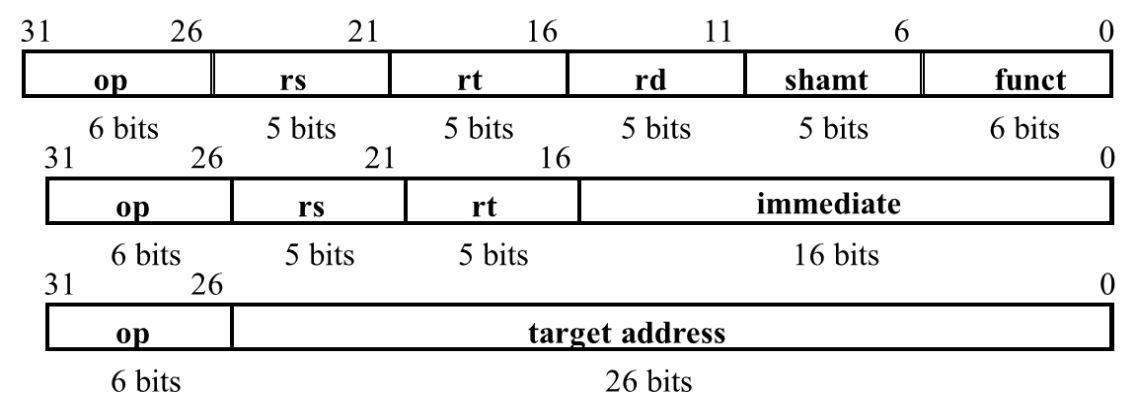
CSC3050 – Computer Architecture Final Examination

1. (25%) Consider the following three instruction formats, R, I and J types, for MIPS.



1. For R-type instruction, why is 5-bit used for the field of *rs*? (5%)
2. Consider the following MIPS I-type instruction. Let $17 = 0x000003A7 (in base 16) and the instruction is stored at the memory address 0x00003338 (in base 16). If it is a *beq* instruction and the target address to jump is 0x00003320, what value is stored in *A*? (5%)

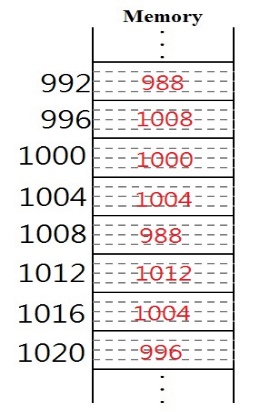
31 opcode 26 25 rs 21 20 rt 16 15 immediate 0

|  |  |  |  |
| --- | --- | --- | --- |
| opcode | 17 | 18 | A |

1. If the above instruction is a *store* instruction, what is the address of stored data in memory? (5%)
2. If the above instruction is an *addi* instruction, what constant is added? Please give your constant in 32-bit form. (5%)
3. If the above instruction is a *Jump* instruction, what is the target *Jump* address? Please give the target address in 32-bit form. (5%)
4. Answer TRUE or FALSE. You need to justify your answer.
   1. There is at least one MIPS instruction that can directly store the result of an ALU calculation into memory. (3%)
   2. In a recursive program, it is not always necessary to store$*ra* onto the stack. (3%)
   3. Overflow will never occur if two signed numbers of different signs are added. (3%)
   4. An integer multiplication by a power of 2 can be replaced by a left shift and an integer division by a power of 2 can be replaced by a right shift. (3%)
   5. A processor with more powerful instructions can always run a job using less CPU time. (3%)
5. Suppose that you have a computer with the following execution time for each stage and each pipeline register takes 20ps to store data.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| IF | ID | EX | MEM | WB |
| 200ps | 300ps | 250ps | 300ps | 200ps |

1. For a single-cycle processor, what are the clock cycle time and the throughput? (5%)
2. For a 5-stage pipelined processor, what are the clock cycle and the throughput? (5%)
3. let the Initial values of the following registers be $0=0, $4=992, $5=1004, and $6=1000. Let we have the following codes and memory state. What are the values in $4 $5 and $6 after the above codes are being executed? (10%)



**Code:**

addi $0, $0, 4,

lw $5, 8($4)

add $4, $5, $0

sw $4, 4($5)

lw $6, 8($4)

1. Which of the following operation(s) is (are) not performed in CPU (Assume that there is no cache in CPU)? Explain your answers: (a) fetching instruction (b) operation of Boolean logic (c) loading/storing data (d) data transfer among registers (e) arithmetic operation. (15%)
2. What is “speculation” used in processor designs? Give two examples of executing instructions that use speculation in a processor. (10%)
3. Consider a memory of 26 words and an 8-block direct-mapped cache. Let a sequence of memory references are shown as following using their word addresses 8(001000), 16(010000), 24(011000), 21(010101). What are the values in A, B, C, D, E? (15%)

|  |  |  |  |
| --- | --- | --- | --- |
| **index** | **v** | **tag** | **data** |
| 000 |  |  | E |
| 001 |  |  |  |
| 010 |  | C |  |
| 011 |  |  |  |
| 100 | A | D |  |
| 101 | B |  |  |
| 110 |  |  |  |
| 111 |  |  |  |