2025 Digital IC Design

Homework 5: Max Convex Hull

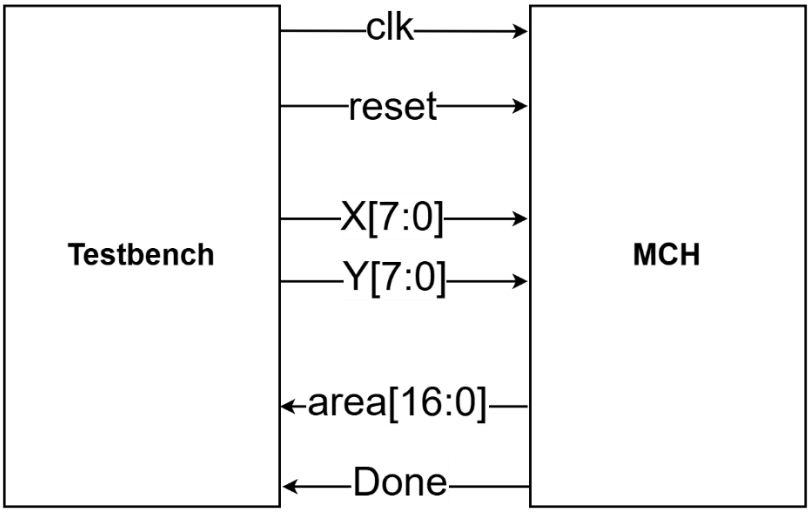
1. Introduction:

This homework focuses on designing an algorithm to compute the area of the largest convex polygon that can be formed from a fixed set of 20 points in 2D space.

You are required to read in 20 distinct 2D coordinates, determine the convex polygon that encloses all the points (i.e., the convex hull), and calculate the area of that polygon.

2. Specification:

2.1 Block Diagram



2.2 I/O Interface

Signal Name	I/O	Width	Description
clk	Input	1	System clock signal. System should be triggered by the positive edge of clock.

reset	Input	1	System reset signal. Active high, asynchronous reset.
X	Input	8	Input horizontal coordinate.
Y	Input	8	Input vertical coordinate.
Done	Output	1	When the MCH circuit finish calculating area of the polygon, it sets done to high to indicate completion.
area	Output	17	Output area port.

2.3 Algorithm

Graham Scan

- Steps:

I. Find the point with the lowest y-coordinate (and leftmost if tie). This is the anchor.

II. Sort all other points by the polar angle they make with the anchor.

III. Traverse sorted points and maintained a stack:

A. At each step, check the turn made by the last two points and the new point.

B. If the turn is not a left turn (i.e., it's a right turn or colinear), pop the last point.

IV. The final stack is your convex hull in counterclockwise order.

In this assignment, you can modify the algorithm to improve the performance.

2.4 Area Calculation

Shoelace Formula

Given a polygon with vertices:

$(x_1,\ y_1),\quad (x_2,\ y_2),\ \cdots,\quad (x_n,\ y_n)$

The area is:

$$\boldsymbol{Area} = \frac{1}{2}\left|\sum_{i=1}^{n}(x_i \cdot y_{i+1} - x_{i+1} \cdot y_i)\right|$$

Where:

$$(x_{n+1},\ y_{n+1}) = (x_1,\ y_1)$$

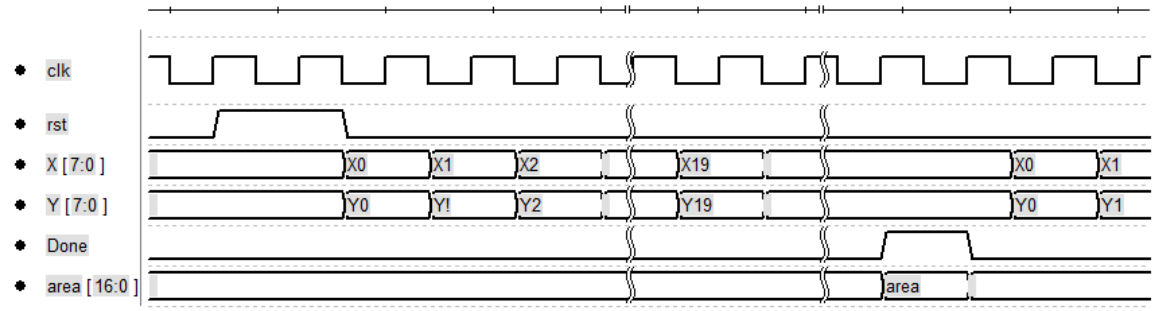
In other words, the last point connects back to the first.

In this assignment, you can modify the algorithm to improve the performance.

2.5 Function Description

- **Input Format:**
  A plain text file or direct function input containing exactly 20 (x, y) coordinate pairs. Each coordinate is a pair of real numbers.
- **Output Format:**
  A single floating-point number representing the area of the convex polygon, rounded to 1 decimal places.

After the reset signal pulled down, the coordinates of the first pattern will be sent into MCH module. After you finish the area calculation of a pattern, the done signal should be pulled high with the area value output at the same cycle. As the done signal is set to high, the testbench will begin to send other 20 coordinates of the other pattern.



3. File Description:

File Name	Description
./MCH.v	Top module of the Max Convex Hull.
./testfixture.sv	Testbench file. You can only modify the "CYCLE" and "MAX_CYCLE" definition.
./MCH.sdc	Constraints file for synthesis. You can modify the cycle width of this file. Note that the cycle used in this file should be equivalent to the clock period of pre-layout simulation.
./dat/goldenX.dat	Test patterns and golden data of each pattern.
./img/goldenX.png	Images of each pattern which is provided for you when needed.

4. Scoring:

4.1 Functional Simulation [40%]

All of the result should be generated correctly, and you will get the following message in ModelSim simulation.

```
# 
# ================ Running pattern 8 ================
# 
# [PASS] Pattern 8: area = 01066
# 
# ================ Running pattern 9 ================
# 
# [PASS] Pattern 9: area = 15e7a
# 
# ====================== RESULT ======================
# 
# All 10 patterns passed!
# 
# Cycle: 1585
# 
# ** Note: $finish    : C:/Users/M18131507/Documents/DICLAB/DIC_2025/2025/h
#    Time: 15855 ns  Iteration: 0  Instance: /testfixture
```

4.2 Pre-Layout Simulation [30%]

- ✓ **Synthesis:**

  Your code should be synthesizable. After it is synthesized in Quartus, a file named MCH.vo will be obtained.

DEVICE：Cyclone IV E –EP4CE55F23A7

✓ **Simulation:**

All of the results should be generated correctly using MCH.vo, and you will get the following message in ModelSim simulation.

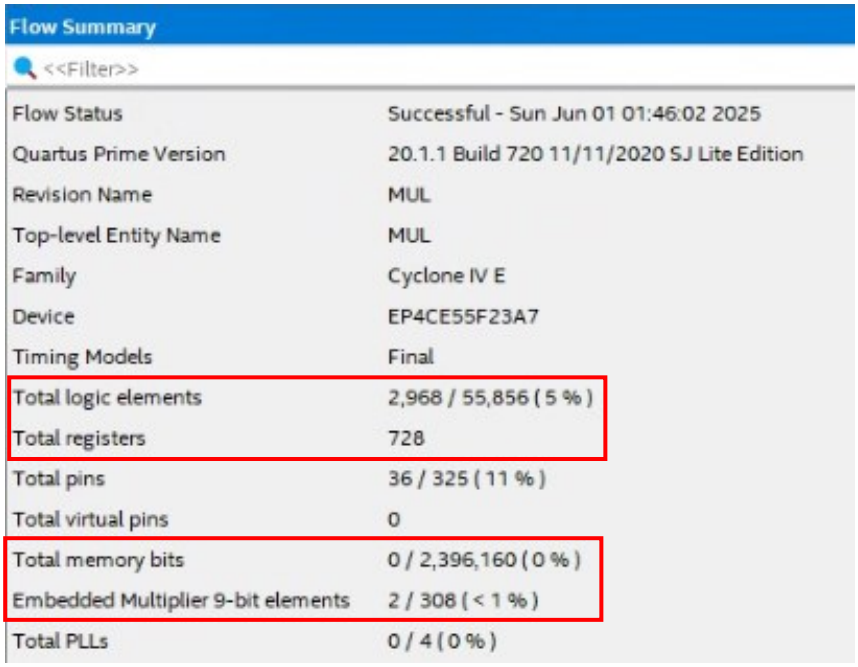
```
# ================ Running pattern 8 ================
#
# [PASS] Pattern 8: area = 01066
#
# ================ Running pattern 9 ================
#
# [PASS] Pattern 9: area = 15e7a
#
# ====================== RESULT ======================
#
# All 10 patterns passed!
#
# Cycle: 1585
#
# ** Note: $finish    : C:/Users/M18131507/Documents/DICLAB/DIC_2025/2025/h
#    Time: 15855 ns  Iteration: 0  Instance: /testfixture
```

4.3 Performance [30%]

The performance is scored by the total logic elements, total registers, total memory bits, and embedded multiplier 9-bit elements your design used in pre-layout simulation and the total cycles your design takes to finish the simulation. The performance score will be decided by your ranking in all received homework. Only designs that passed Pre-Layout Simulation and meet resource limitations will be considered in the ranking. Otherwise, you can't get performance score.

The scoring standard: (The smaller, the better)

Scoring = (Total logic elements + Total register + Total memory bits + 200*Embedded multiplier 9-bit elements) × (Total cycle × Clock width)



Flow Summary

<<Filter>>

Flow Status	Successful - Sun Jun 01 01:46:02 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MUL
Top-level Entity Name	MUL
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	2,968 / 55,856 (5 %)
Total registers	728
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

5. Submission

5.1 File Submission

You should classify your files into three directories and compress them to .zip format. The naming rule is StudentID.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL
*.v	All of your Verilog RTL code
	Pre-Layout
*.vo	Gate-Level netlist generated by Quartus
*.sdo	SDF timing information generated by Quartus
*.sdc	Constraint file when synthesize in Quartus
	Documentary
Report.pdf	The report file of your design (in pdf)

5.2 Report file

In this assignment, if you use different algorithm to implement the circuit, please explain the method in detail. Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the flow summary result is necessary in the report. Please fill the field of total logic elements, total register, total memory

bits, embedded multiplier 9-bit elements according to the flow summary of your synthesized design. And fill the field of clock cycle used and clock width according to the pre-layout simulation results that ModelSim shows if the design passes pre-layout simulation. If the filled-in values don't match your synthesized design or pre-layout simulation results, you will lose 5 points.

5.3 Notes

a. Please submit your .zip file to folder HW5 in Moodle.
   Deadline: 2025/06/22 23:55
b. Late submissions will result in a penalty of 5 points per day.
c. You should fill in a Google form of your performance and the PA ranking will be opened to the public.
d. The clock period in MCH.sdc file should match the pre-layout simulation clock period. TA will use the clock cycle of the MCH.sdc file to verify the pre-layout simulation.