Hao-Wei Liang

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Education

National Taiwan University — Taipei, Taiwan

B.S. in Electrical Engineering, GPA: 4.23/4.3, Last 60: 4.28/4.3, Major: 4.25/4.3 — *September 2018 – Present*

- Double Major in Physics, Minor in Philosophy
- Related Coursework:
  Computer-Aided VLSI System Design, Integrated Circuit Design, Computer Architecture, Digital Circuit Lab Electronics (I) and (II), Switching Circuit and Logic Design, Electronic Circuits, Signals and Systems, Algorithm Networking and Multimedia, Machine Learning, Linear Algebra, Probability and Statistics, Discrete Mathematics

Research Experience

Lab for Data Processing Systems — EE Dept., National Taiwan University, Taiwan

Undergraduate Research Program — *February 2021 – Present*

- Designed a hardware accelerator for Heston Model option pricing with Monte Carlo simulation.
  - Implemented Uniform and correlated/uncorrelated bivariate Gaussian distribution random number generators.
  - Designed four stage pipeline for each of the Heston Model MC core data path.
- Studied and improved neural network basecaller for Oxford Nanopore Technology raw data.

Energy-Efficient Circuits and Systems Lab — EE Dept., National Taiwan University, Taiwan

Undergraduate Research Program — *September 2021 – Present*

- Researched for keyword spotting and digital speech processing on edge device.
  - Studied and evaluated the pros and cons of various machine learning models for hardware implementation.
  - Assisted in and learned from the tape-out flow of the keyword spotting module.
- Built and optimized a framework for VAD algorithms simulation, evaluation, and analysis.

Professional Experience

Research Center for Information Technology Innovation — Academia Sinica, Taiwan

Part-Time Research Assistant — *April 2022 – Present*

- Researched for hardware accelerator for artificial intelligence.
- Studied research papers for in-memory and near-memory processing systems.

Project Experience

Digital Audio Tape Recorder | *System Verilog, FPGA* — November – December 2021

- A device that records sound with a microphone and can play and pause the recorded audio.
- The recorded audio can be played normally and switched to fast, slow, and reversed motion at any time.
- Supports simple signal processing filters for the recorded audio.
- Experienced in communicating with other IP modules such as memory devices and Audio CODEC on FPGA.

Image Processing Filter | *Verilog, Design Compiler, Innovus* — June 2021 – July 2021

- A device that stores the input image in on-chip SRAM and processes it with various kinds of operations such as median filter with zero padding, census transform, and moving or scaling up/down the desired filtering region.
- After every operation is completed, the circuit displays the filtering region of the image in raster-scan order.
- Implemented pipeline design to improve throughput and AT performance.

RISC-V Processor | *Verilog* — May 2021 – June 2021

- A hardware implementation of single cycle simplified version RISC-V processor.
- Supports basic instructions such as mathematical operations, branching, and communication with memory.
- Experienced in system design and hardware optimization techniques.

Additional Information

Programming Languages: Verilog, System Verilog, Python, C++, RISC-V
Related Tools: Design Compiler, Innovus, PrimeTime, Virtuoso, SPICE, Lint, EPS
Developer Tools: Git, Visual Studio
Standardized Test: GRE 330, TOEFL 105
Honors: Dean's List Award (top 5% students in a semester) * 4 semesters