Hao-Wei (Howard) Liang

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Education

University of California, Berkeley — Berkeley, CA
M.Eng. in Electrical Engineering and Computer Sciences — Aug. 2023 – May 2024
- Coursework: Digital Integrated Circuit Design, Integrated Circuit Devices

National Taiwan University (NTU) — Taipei, Taiwan
B.S. in Electrical Engineering, GPA: 4.23/4.3, Major: 4.25/4.3 — Sep. 2018 – Jan. 2023
- Coursework: Computer-aided VLSI System Design, Digital Integrated Circuit Design, Computer Architecture FPGA Lab, Electronics, Switching Circuit and Logic Design, Signals and Systems, Algorithms, Machine Learning

Experience

Lab for Data Processing Systems — EE Dept., NTU, Taiwan
Undergraduate Research Program, advised by Prof. Yi-Chang Lu — Feb. 2021 – Sep. 2022
- Designed an ASIC accelerator to speed up Monte Carlo (MC) simulations for Heston Model option pricing.
  - Implemented Uniform and correlated/uncorrelated bivariate Gaussian distribution random number generators.
  - Designed four-stage pipeline for each of the Heston Model MC core data path.
- Applied Stochastic Weight Averaging, improving the Pytorch basecaller, Bonito, accuracy from 97.98% to 98.18%.

Energy-Efficient Circuits and Systems Lab — EE Dept., NTU, Taiwan
Undergraduate Research Program, advised by Prof. Tsung-Te Liu — Sep. 2021 – Jan. 2023
- Researched for keyword spotting and digital speech processing on edge devices.
  - Studied and evaluated the pros and cons of various machine learning models for hardware implementation.
  - Assisted in and experienced the tape-out flow of the keyword spotting module.
- Built and optimized a framework for voice activity detection algorithms simulation, evaluation, and analysis.

Research Center for Information Technology Innovation — Academia Sinica, Taiwan
Part-Time Research Assistant, advised by Prof. Hsiang-Yun Cheng — Apr. 2022 – Feb. 2023
- Studied and briefed research papers for in-memory and near-memory processing systems.
- Developed near-memory processing architecture for recommendation system training accelerator.
  - Utilized heterogeneous memory hierarchy (HBM and DIMM) to leverage data locality.
  - Proposed to address workload imbalance between processing elements by optimizing data allocation.

Project

Digital Audio Tape Recorder | *System Verilog, FPGA* — Nov. – Dec. 2021
- A device that records sound with a microphone and can play and pause the recorded audio.
- The recorded audio can be played normally and switched to fast, slow, and reversed motion at any time.
- Supports simple signal processing filters for the recorded audio.
- Experienced in communicating with other IP modules such as memory devices and Audio CODEC on FPGA.

Image Processing Filter | *Verilog, Design Compiler, Innovus* — Jun. – Jul. 2021
- A device that stores the input image in on-chip SRAM and processes it with various kinds of operations such as median filter with zero padding, census transform, and moving or scaling up/down the desired filtering region.
- After every operation is completed, the circuit displays the filtering region of the image in raster-scan order.
- Implemented pipeline design to improve throughput and AT performance.

RISC-V Processor | *Verilog, Design Compiler* — May – Jun. 2021
- A hardware implementation of single cycle RISC-V processor.
- Supports basic instructions such as mathematical operations, branching, and interaction with memory.
- Experienced in system design and hardware optimization techniques.

Additional Information

Programming Languages: Verilog, System Verilog, Python, C++, MATLAB, RISC-V Assembly
VLSI Related Tools: NC-Verilog, Design Compiler, Innovus, PrimeTime, Virtuoso, SPICE, Lint, EPS
Awards: NTU Dean's List Award (top 5% students in a semester) * 5 semesters
Honor: Graduate Representative (top ten students of four years in NTU EE)