Winner-Take-All circuit and modifications

Hao-An Her, *Student Member, IEEE*

***Abstract*—This paper introduces the Lazzaro winner-take-all (WTA) circuit which is a configuration commonly used in recurrent neural networks and the computational models in brain. Aside from the simple winner-take-all circuit, this paper also introduces a method to improve the resolution during the transition of output current changes, which is to increase the evaluation node voltage by inserting a cascode transistor in each cell. While this is very simple, this can effectively improve the resolution of the circuit. Lastly, this paper introduces a way that can implement a loser-take-all circuit by using a current mirror, push-pull configuration, and a feedback loop. While the resolution of the circuit can still be improved, this gives a general idea of how a loser-take-all circuit can be implemented.**

***Index Terms*— analog circuits, MOSFET circuits, neurofeedback, neural networks**

I. Introduction

WINNER-TAKE-ALL circuits are one of the most commonly used circuit components to solve neural network architecture problems, which are mostly related to complex engineering classifications, optimization, and control. During the operation of a WTA process, the most preeminent element among all the input is selected. One of the most commonly used circuit configurations used to serve this purpose is Lazzaro's CMOS WTA circuit. [1] This circuit includes a bias current source, and multiple cells with an input current together with an inhibitory feedback loop. Whichever cell that has the largest input current will result in the output current being almost the same as bias current. In contrast, the inferior cells then will be basically shut down and takes no current. The primary deficiency with this simple WTA circuit proposed by Lazzaro is the limitation of resolution during the transition stage because each cell architecture pretty much consist of only an inhibitory feedback system.

B. Sekerkiran and U. Cilingiroglu [2] described a modified version of Lazzaro's winner-take-all circuit, which is done by adding a cascode transistor within each cell. By doing this, it can effectively raise the evaluation node voltage for the output current, thus increasing the rate of current change during and the resolution during the transition stage.

Other than the implementation of winner-take-all, I have found some situations [4], [5] in which the inverse function of the winner-take-all algorithm is needed. A loser-take-all then is needed for this kind of application. This loser-take-all circuit [3] is used to select the input with minimum magnitude from an array of inputs. The cell with minimum magnitude of input current will have its corresponding output current being non-zero while that of the other cells being zero.

II. Circuit description and analysis

A. The Simple Winner-Take-All Circuit

The simple winner-take-all circuit proposed by Lazzaro [1] is shown in Fig. 1. This circuit is composed of n interacting cells and a tail current source. To manifest how this winner-take-all circuit works, we will have n set to 2 in this case for simplicity and suppose that the two input currents $I_{IN,1}$ and $I_{IN,2}$ have the same magnitude. When $I_{IN,1}$ starts to increase, the gate voltage of M2 in cell 1 will increase. Because of the source follower type of configuration at M1 in cell 1, the evaluation node voltage at cell 1 in this case will also increase. Thus, the M1 transistor in cell 1 operates in subthreshold saturation region. For the losing cell (cell 2), while the common source node voltage is increasing, its input current source stays at the same magnitude. In order to draw the same amount of input current at M2 of cell 2, this will largely decrease the evaluation node voltage of cell 2 and will result in M1 transistor of cell 2 operating in subthreshold ohmic region. Applying this rule, the winner cell operates in subthreshold saturation region while the loser cells operate in subthreshold ohmic region. Therefore, the output current of the winner cell will be basically equal to the tail source current while other loser cells will have 0 output current.

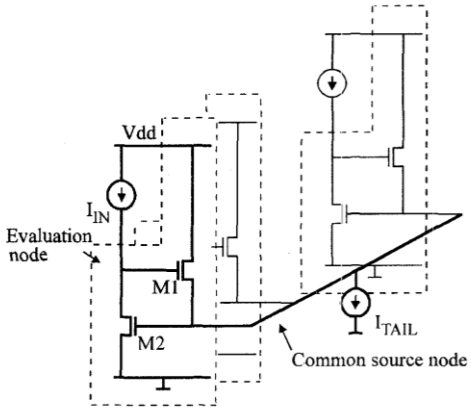

Fig. 1. Lazzaro WTA circuit

B. The Cascoded Winner-Take-All Circuit

The cascoded winner-take-all circuit proposed by B. Sekerkiran and U. Cilingiroglu [2] is shown in Fig. 2. The circuit pretty much resembles the simple winner-take-all circuit proposed by Lazzaro [1]. The only difference in this circuit is the addition of a cascode transistor M3 in each cell. When looking at each cell, we can consider the input voltage as being the gate voltage of transistor M2, which is induced by the input current. For the output voltage, we can consider the evaluation node voltage to be that role because it is the

primary factor that may cause the change in output current in each cell. When the cascode transistor is added into the cell, the cascode transistor configuration can effectively increase the output resistance at the evaluation node, which induces faster transition of the output current, improving the resolution at the transition stage. Lastly, to make sure that both M2, and M3 transistors operate in saturation, we need to properly set the gate voltage V_{GM3}. This can be done by calculating the gate voltage using the following formula:

$$V_{GM3} = V_{DS,SAT2} + V_{DS,SAT3} + V_{TH} + \Delta V \quad (\Delta V \approx 0.1V) \quad (1)$$

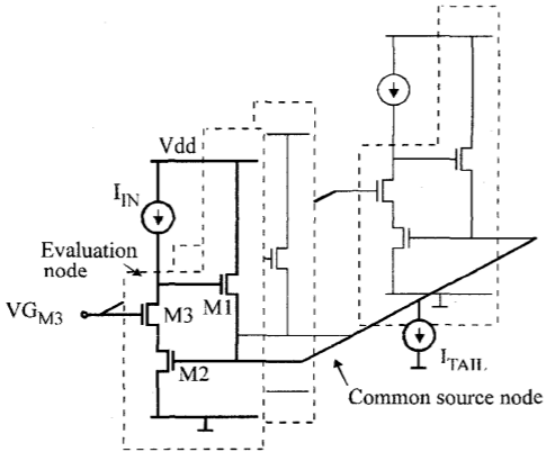

Fig. 2. Cascoded WTA

C. *The Cascoded Winner-Take-All Circuit with Step Input*

For this cascoded winner-take-all circuit in Fig. 3., the circuit configuration does not have any significant changes. The only change being made is the use of a step input current for $I_{IN,2}$ to manifest how the output current changes when one input current is larger than the other.

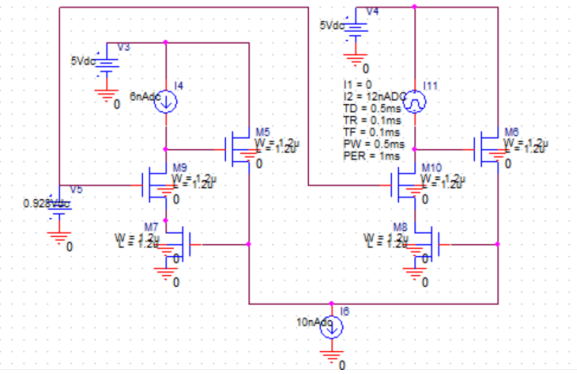

Fig. 3. Cascoded WTA with Step Input

D. *The Loser-Take-All Circuit*

The loser-take-all circuit proposed by G. N. Patel and S. P. DeWeerth [3] is shown in Fig. 4. Each cell in each circuit consists of a current mirror, a push-pull configuration, and a feedback loop. To manifest how the circuit works, we will assume that there's only two cells, and initially their input currents $I_{IN,1}$ and $I_{IN,2}$ are the same. Suppose $I_{IN,2}$ starts to decrease. This will cause the evaluation node voltage V_2 to increase because M1 in cell 2 will try to source more current than M2 can sink. The rise in V_2 will increase the output current flow $I_{OUT,2}$, and partially rob some bias current from the common node. The common mode voltage V_{COM} in this case will also increase because of the source follower type of configuration at M2. The rise in common mode voltage V_{COM} will decrease the current flow over M1 of cell 1. This will further cause M2 in cell 1 to shut down, and thus cell 1 will account for even less current. As a result, when $I_{IN,2}$ is less then $I_{IN,1}$, $I_{OUT,2}$ will account for most part of the bias current while $I_{OUT,1}$ is virtually 0.

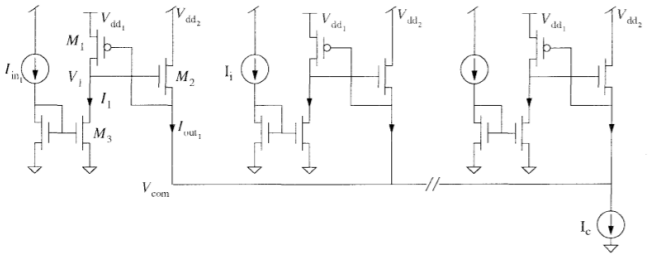

Fig. 4. The Loser-Take-All Circuit

III. Simulation Result

A. *The Simple Winner-Take-All Circuit*

The simple winner-take-all circuit used in my simulation is shown in Fig. 5. Every NMOS that I used within the circuit is of model NMOS05. Each of them has equal width and length of 1.2μm. Vdd is set to 5V. For this simulation, I set I_1 equals to a constant current source of 6nA while I_2 sweeps from 0nA to 10nA, with an increment of 0.01nA. The corresponding result of the simulation is shown in Fig. 6. The result shows that when I_2 exceeds the value of I_1, I_{OUT2} exceeds I_{OUT1} at the same time. The transition starts when I_2 is about 5.8333nA while it ends when I_2 is about 6.1754nA, so the transition in this case can be done within a current change of 0.3421nA.

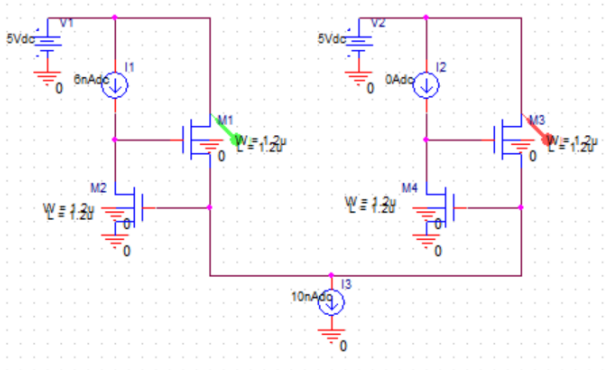

Fig. 5. Simulation Circuit for the simple WTA

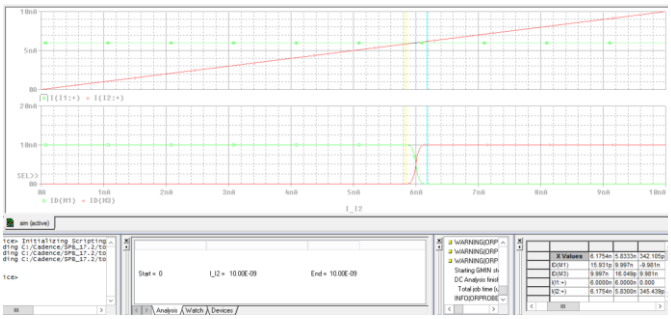

Fig. 6. Simulation Result for the Simple WTA

B. *The Cascoded Winner-Take-All Circuit*

The cascoded winner-take-all circuit used is done by adding cascode transistors M3 and M6 into the original simple WTA circuit. To avoid the "V-min" problem, we need to properly set the bias voltage V_{GM3} at the gate of M3 and M6 transistors. V_{GM3} can be calculated using (1) with the given process parameters $K_n' = 60\mu A/V^2$, $V_{TH} = 0.8V$. The simulation result in Fig. 8 shows that the transition was made from $I_2 = 5.9211nA$ to $I_2 = 6.0877nA$, which indicates that the transition can be made within an input current change of 0.1666nA. In this case, the transition rate is about twice as fast as the simple WTA circuit.

$$V_{GM3} = 2 \times \sqrt{\frac{2\times1.2(\mu m)\times6\times10^{-9}(A)}{60\times10^{-6}\left(\frac{A}{V^2}\right)\times1.2(\mu m)}} + 0.8\,(V) + 0.1\,(V) = 0.928\,(V) \quad (2)$$

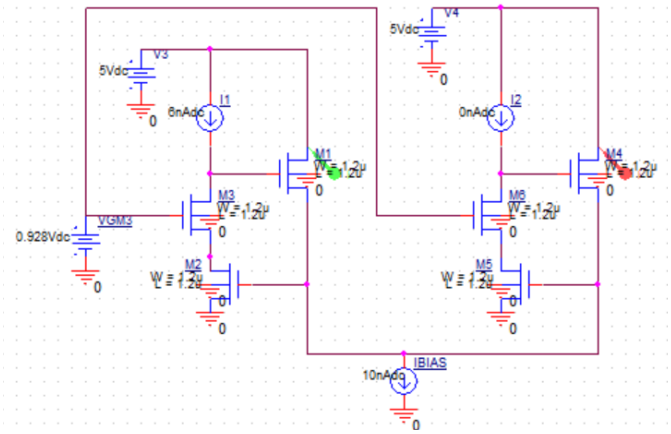

Fig. 7. Simulation Circuit for the Cascoded WTA

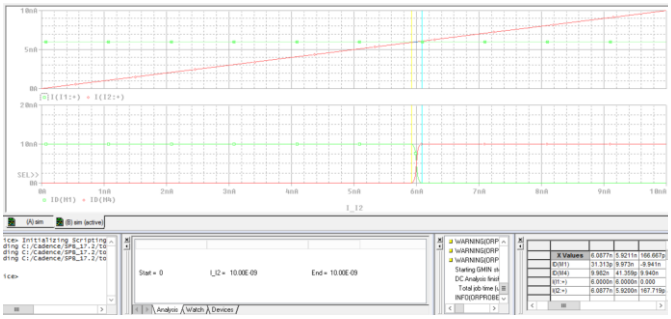

Fig 8. Simulation Result for the Cascoded WTA

C. *The Cascoded Winner-Take-All Circuit with Step Input*

This transient simulation is done by replacing I_2 from a DC sweep current source to an impulse current source. The circuit diagram for this particular circuit is shown in Fig. 9. When we have the input current source I_1 being constant at 6nA and I_2 being an impulse current source that oscillates in between 0 and 12nA, we can expect that the output current I_{OUT2} will be the same as the tail source current I_{BIAS} when I_2 is larger than I_1 with I_{OUT1} being 0. Reversely, when I_2 is less than I_1 and equals to 0, the output current I_{OUT2} will be virtually 0 while I_{OUT1} will account for most portion of I_{BIAS}. The corresponding simulation result with both input and output traces are shown in Fig. 10.

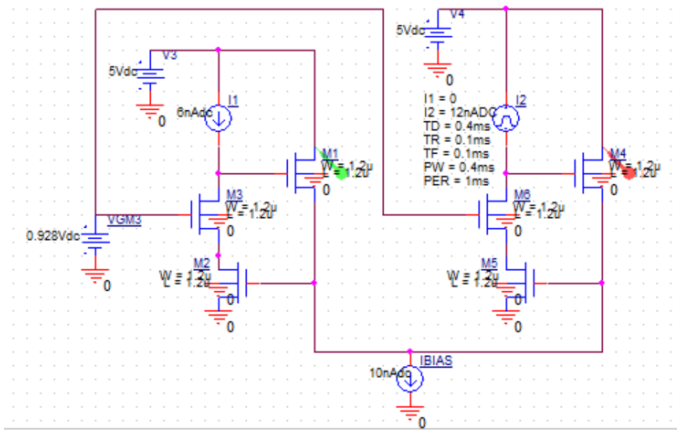

Fig. 9. Cascoded WTA with Step Input

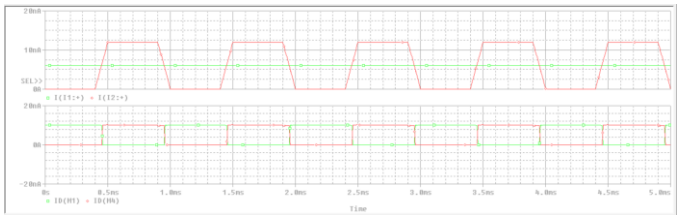

Fig. 10. I/O Relationship of the Cascode WTA with Step Input

D. *The Loser-Take-All Circuit*

The loser-take-all circuit for this simulation is shown in Fig. 11. In order to see how the circuit functions, I set the input current I_1 equals to a constant of 6nA, and I_2 as a DC sweeping current source from 0 to 30nA. The result in Fig. 12 shows that whenever an input current is lower, its corresponding output current will be larger and close to the bias current I_{BIAS} while the corresponding output current for the larger current input being close to 0. The only issue that I had was that the resolution of this loser-take-all circuit is not as ideal as what I have thought of, which takes a bit more time than the winner-take-all current does.

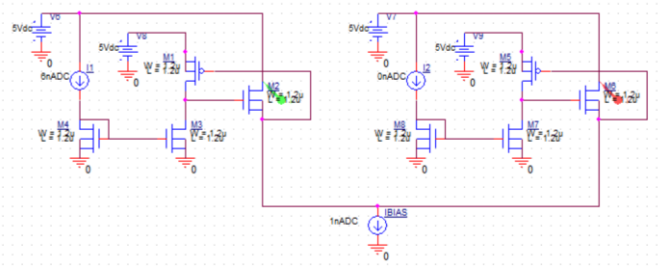

Fig. 11. The Loser-Take-All Circuit

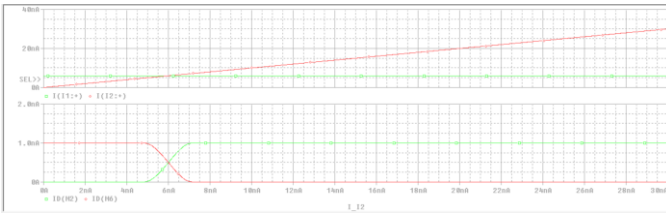

Fig. 12. The I/O Relationship of the Loser-Take-All Circuit

IV. Conclusion

Circuit designs of the simple winner-take-all circuit, the cascoded winner-take-all circuit, and the loser-take-all circuit are presented in this paper. The resolution issue of the simple winner-take-all circuit has been discussed and the cascoded winner-take-all provides a significant improvement in enhancing the resolution of the winner-take-all circuit. Lastly, the loser-take-all circuit was simulated, and its simulation result shows that whenever an input current is lower, its corresponding output current will be higher and close to I_{BIAS}. The only issue encountered was that the resolution doesn't seem to be very ideal compared to the other circuits in this research paper. The resolution of the loser-take-all circuit may be improved by adding a cascode transistor in each cell to improve the overall gain at the evaluation node, just like the simple WTA case. Overall, it was just a basic idea of how to implement a loser-take-all circuit. The circuits within this research paper are all simulated, and their results are same as expected.

References

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