Xilinx Zynq FPGA, TI DSP, MCU 기반의 프로그래밍 및 회로 설계 전문가 과정

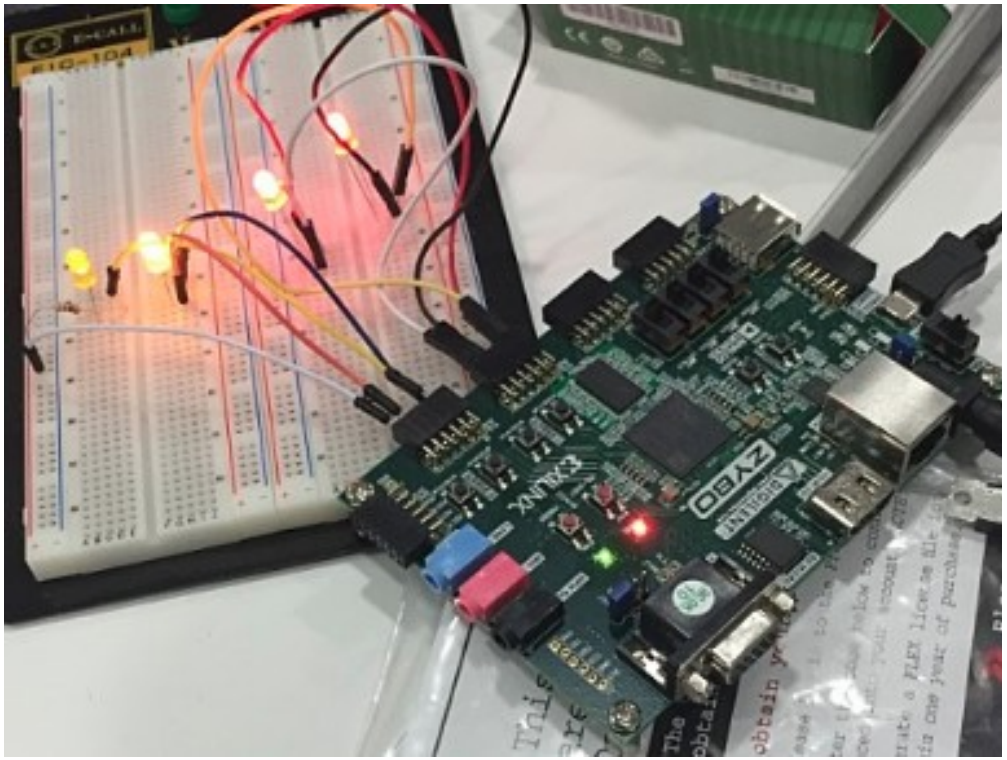
강사 – Innova Lee(이상훈)

gcccompil3r@gmail.com

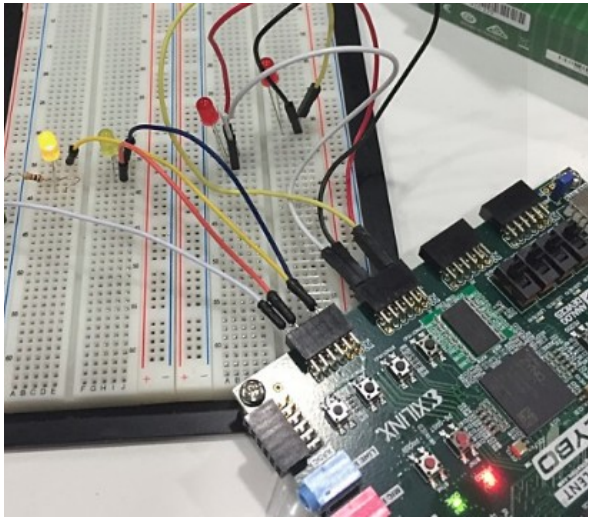
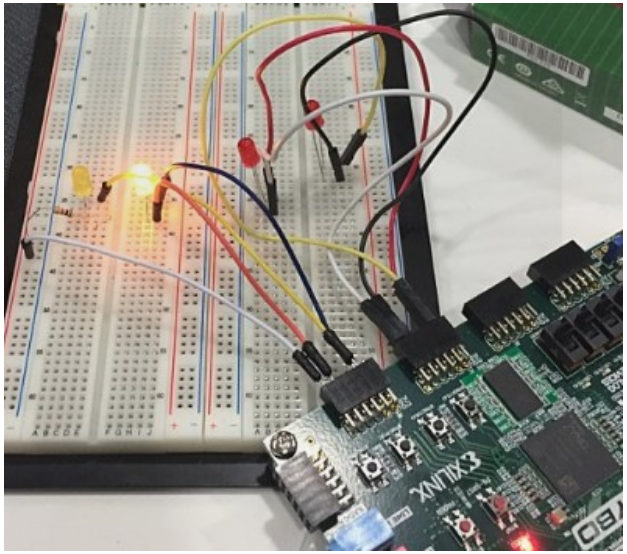
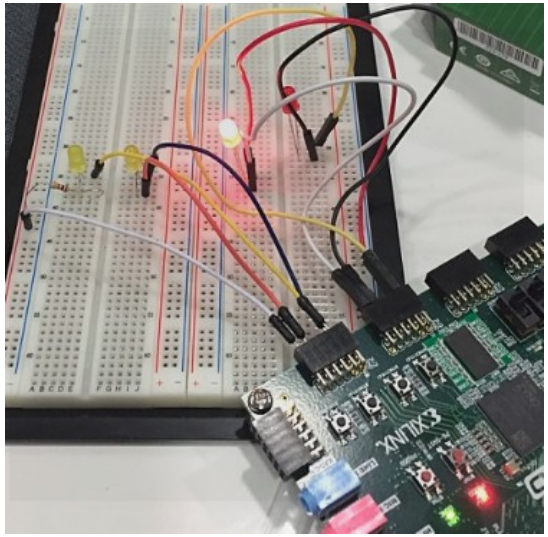
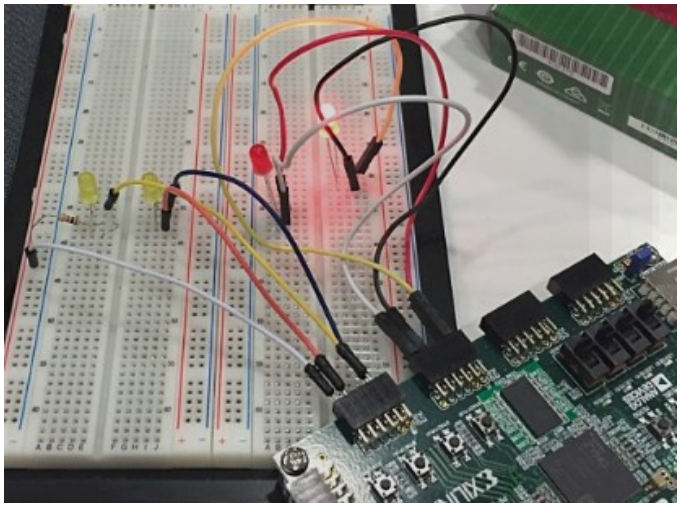
학생 – hoseong Lee(이호성)

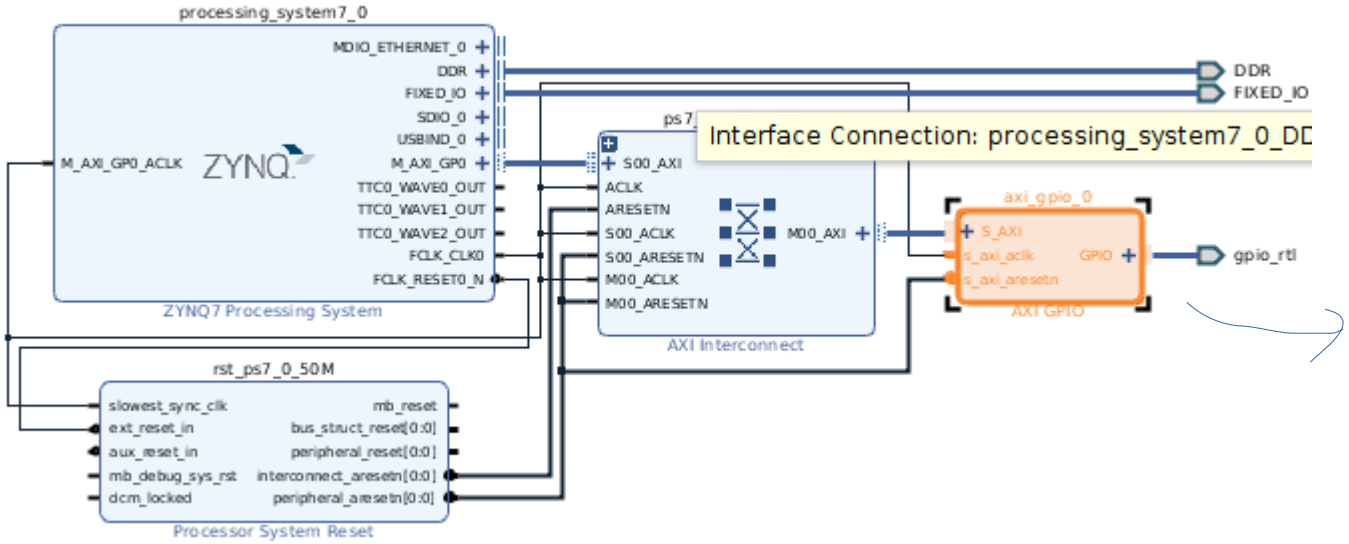
hslee00001@naver.com

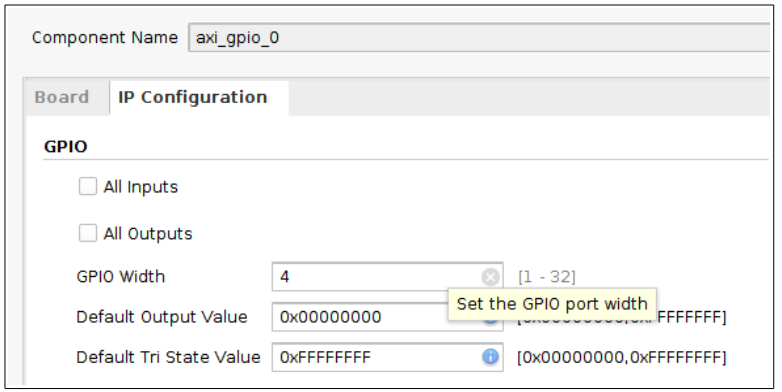
1. FPGA, led 실습

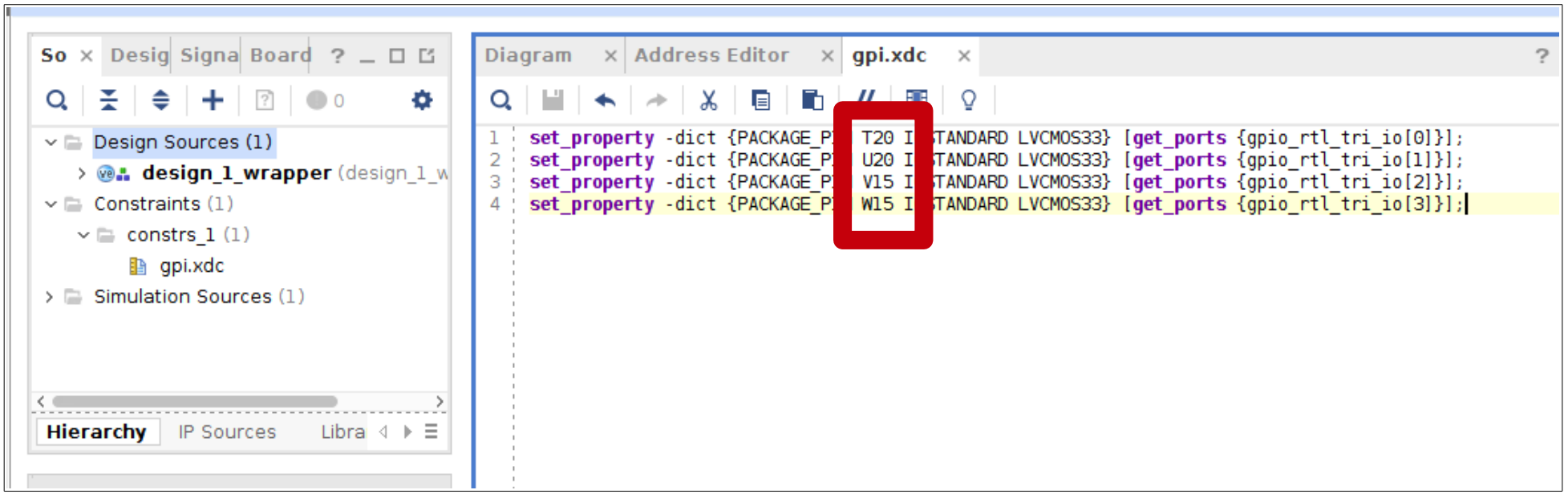


- shift

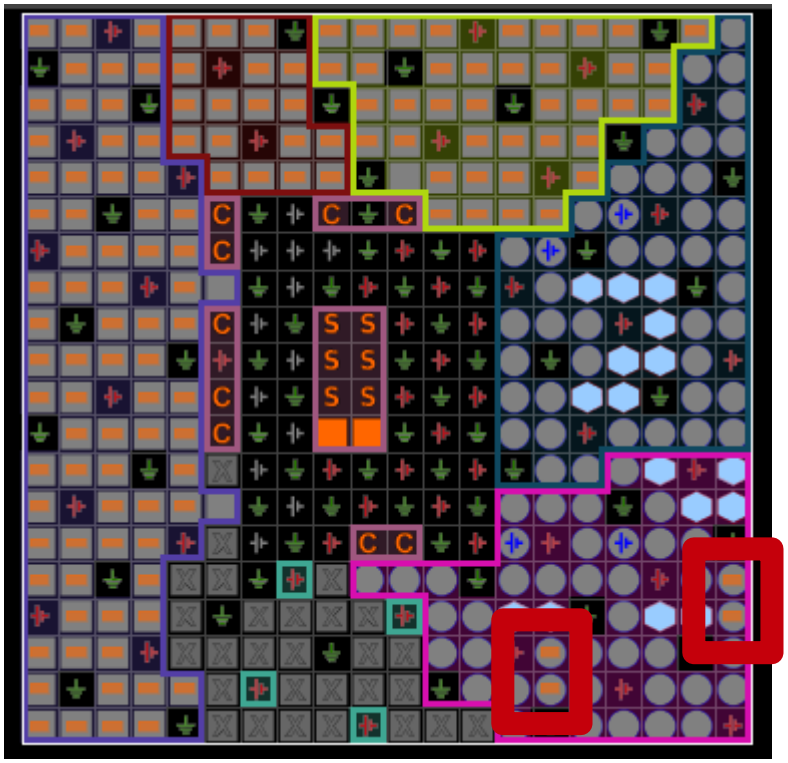
1 	2 
3 	4 


processing_system7_0
MDIO_ETHERNET_0
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0_ACLK
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Interface Connection: processing_system7_0_DD
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
gpio_rtl
rst_ps7_0_50M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset


Component Name
axi_gpio_0
Board
IP Configuration
GPIO
All Inputs
All Outputs
GPIO Width
4
[1 - 32]
Set the GPIO port width
Default Output Value
0x00000000
Default Tri State Value
0xFFFFFFFF
[0x00000000,0xFFFFFFFF]


Design Sources (1)
design_1_wrapper
Constraints (1)
constrs_1 (1)
gpi.xdc
Simulation Sources (1)
Hierarchy
IP Sources
Diagram
Address Editor
gpi.xdc
1 set_property -dict {PACKAGE_PI T20 I STANDARD LVCMOS33} [get_ports {gpio_rtl_tri_io[0]}];
2 set_property -dict {PACKAGE_PI U20 I STANDARD LVCMOS33} [get_ports {gpio_rtl_tri_io[1]}];
3 set_property -dict {PACKAGE_PI V15 I STANDARD LVCMOS33} [get_ports {gpio_rtl_tri_io[2]}];
4 set_property -dict {PACKAGE_PI W15 I STANDARD LVCMOS33} [get_ports {gpio_rtl_tri_io[3]}];

Generate Bitstream



→

gpio 16 개의 포트

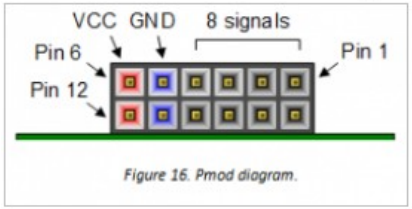


Figure 16. Pmod diagram.

Pmod JA (XADC)	Pmod JB (고속)	Pmod JC (고속)	Pmod JD (고속)	Pmod JE (고속)	Pmod JF (MIO)
JA1 : N15	JB1 : T20	JC1 : V15	JD1 : T14	JE1 : V12	JF1 : MIO-13
JA2 : L14	JB2 : U20	JC2 : W15	JD2 : T15	JE2 : W16	JF2 : MIO-10
JA3 : K16	JB3 : V20	JC3 : T11	JD3 : P14	JE3 : J15	JF3 : MIO-11
JA4 : K14	JB4 : W20	JC4 : T10	JD4 : R14	JE4 : H15	JF4 : MIO-12
JA7 : N16	JB7 : Y18	JC7 : W14	JD7 : U14	JE7 : V13	JF7 : MIO-0
JA8 : L15	JB8 : Y19	JC8 : Y14	JD8 : U15	JE8 : U17	JF8 : MIO-9
JA9 : J16	JB9 : W18	JC9 : T12	JD9 : V17	JE9 : T17	JF9 : MIO-14
JA10 : J14	JB10 : W19	JC10 : U12	JD10 : V18	JE10 : Y17	JF10 : MIO-15

이후 File → Export → Export Hardware , File → Launch SDK → sdk 컴파일 및 디버그

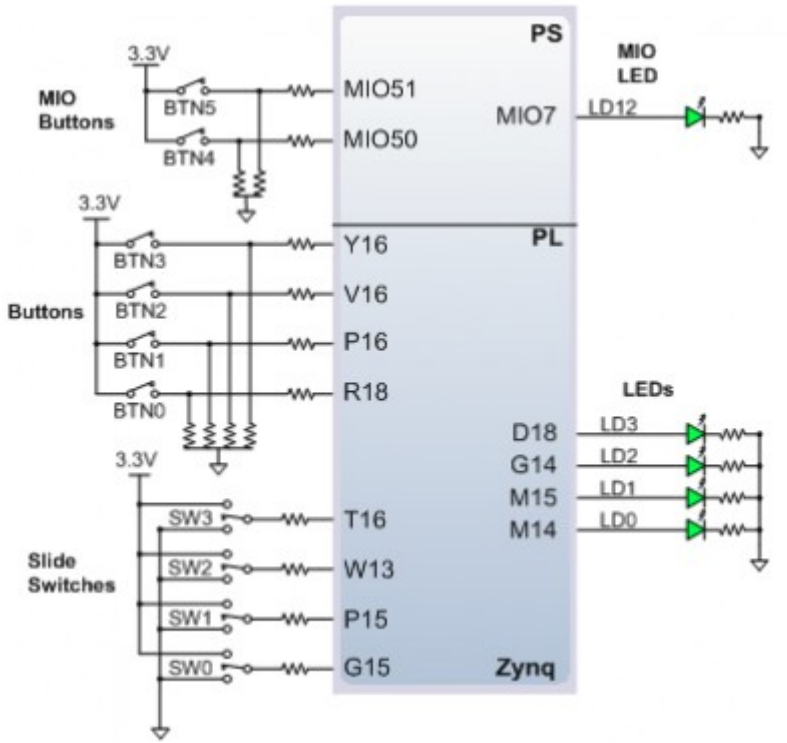
-code

```c
#include <stdio.h>
#include <xgpio.h>
#include "xparameters.h"
#include "sleep.h"

int main(void)
{
    int i=2;
    XGpio out;

    XGpio_Initialize(&out, XPAR_AXI_GPIO_0_DEVICE_ID);
    XGpio_SetDataDirection(&out,1,0x0);
    while(1)
    {
        Xil_Out32(0x41200000, i);
        i= i<<1;
        if(i==16)
            i=1;
        sleep(1);
    }
    return 0;
}
```

- fpga – and gate

Package | Device | ander.vhd

```
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------
20
21
22  library IEEE; -- fpga 는 트랜지스터를 논리적으로 프로그래밍 한 것
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity ander is
26       port(a,b : in std_logic_vector(1 downto 0);
27            result : out std_logic_vector(1 downto 0));
28  end ander;
29
30  architecture Behavioral of ander is
31  begin
32            result <= a and b;
33  end Behavioral;
34
```



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
a (2)	IN			✓	(Multiple)	LVCMOS33*	3.300				NONE	NONE
a[1]	IN		W13	✓	34	LVCMOS33*	3.300				NONE	NONE
a[0]	IN		G15	✓	35	LVCMOS33*	3.300				NONE	NONE
b (2)	IN			✓	34	LVCMOS33*	3.300				NONE	NONE
b[1]	IN		T16	✓	34	LVCMOS33*	3.300				NONE	NONE
b[0]	IN		P15	✓	34	LVCMOS33*	3.300				NONE	NONE
result (2)	OUT			✓	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
result[1]	OUT		M15	✓	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
result[0]	OUT		M14	✓	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_