Xilinx Zynq FPGA, TI DSP, MCU 기반의 프로그래밍 및 회로 설계 전문가 과정

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Cortex-R5F Hercules safety MCU – boot code 분석

1 c_int00() -> systemInit() -> setupFlash

```
void setupFlash(void)
{

/* USER CODE BEGIN (6) */
/* USER CODE END */

    /** - Setup flash read mode, address wait states and data wait states */
    flashWREG->FRDCNTL =  0x00000000U
                       | (uint32)((uint32)3U << 8U)
                       |  3U;

    /** - Setup flash access wait states for bank 7 */
    FSM_WR_ENA_HL     = 0x5U;
    EEPROM_CONFIG_HL = 0x00000002U
                     | (uint32)((uint32)9U << 16U) ;

/* USER CODE BEGIN (7) */
/* USER CODE END */

    /** - Disable write access to flash state machine registers */
    FSM_WR_ENA_HL     = 0x2U;

    /** - Setup flash bank power modes */
    flashWREG->FBPWRMODE = 0x00000000U
                         | (uint32)((uint32)SYS_ACTIVE << 14U) /* BANK 7 */
                         | (uint32)((uint32)SYS_ACTIVE << 2U)  /* BANK 1 */
                         | (uint32)((uint32)SYS_ACTIVE << 0U); /* BANK 0 */
```

1.1 FlashWREG -> FRDCNTL

0011 0000 0011

7.10.1 Flash Read Control Register (FRDCNTL)

FRDCNTL supports prefetch mode. This register controls Flash timings for the main Flash banks. For the equivalent register that controls Flash timings for the EEPROM Emulation Flash bank (bank 7), see Section 7.10.32.

Figure 7-11. Flash Read Control Register (FRDCNTL) (offset = 00h)

31 – 16	15 – 12	11 – 8	7 – 2	1	0
Reserved	Reserved	RWAIT	Reserved	PFUENB	PFUENA
R-0	R-0	R/WP-1	R-0	R/WP-1	R/WP-1

LEGEND: R/W = Read/Write; R = Read only; WP = Write in Privilege Mode; -n = value after reset

Table 7-13. Flash Read Control Register (FRDCNTL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reads return 0. Writes have no effect.
11-8	RWAIT	0-Fh	Random/data Read Wait State The random read wait state bits indicate how many wait states are added to a Flash read access. Address wait state is fixed to 1 HCLK cycle. **Note:** The required wait states for each HCLK frequency can be found in the device-specific data sheet.
7-2	Reserved	0	Reads return 0. Writes have no effect.
1	PFUENB		Prefetch Enable for Port B
		0	Prefetch Mode is disabled.
		1	Prefetch Mode is enabled. (Recommended)
0	PFUENA		Prefetch Enable for Port A
		0	Prefetch Mode is disabled.
		1	Prefetch Mode is enabled. (Recommended)

➔ RWAIT – 주소 wait 상태 (1사이클) , FPFUENA: 프레페치 모드 인에이블

1.2 FSM_WR_ENA_HL

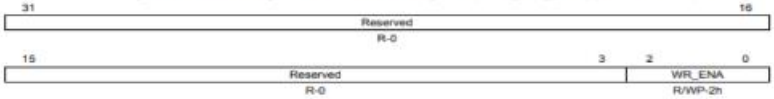
8bit 0000 0101

EEOROM_CONFIG_HL

8bit 0000 0010

7.10.31 FSM Register Write Enable Register (FSM_WR_ENA)

Figure 7-41. FSM Register Write Enable Register (FSM_WR_ENA) (offset = 288h)



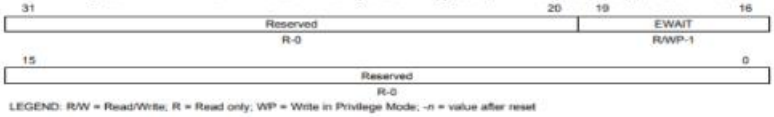
LEGEND: R/W = Read/Write; R = Read only; WP = Write in Privilege Mode; -n = value after reset

Table 7-43. FSM Register Write Enable Register (FSM_WR_ENA) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reads return 0. Writes have no effect.
2-0	WR_ENA		FSM Write Enable
		5h	This register must contain 5h in order to write to any other register in the range FFF8 7200h to FFF8 72FFh. This is the first register to be written when setting up the FSM.
		All other values	For all other values, the FSM registers cannot be written.

7.10.32 EEPROM Emulation Configuration Register (EEPROM_CONFIG)

Figure 7-42. EEPROM Emulation Configuration Register (EEPROM_CONFIG) (offset = 2B8h)



LEGEND: R/W = Read/Write; R = Read only; WP = Write in Privilege Mode; -n = value after reset

Table 7-44. EPROM Emulation Configuration Register (EEPROM_CONFIG) Field Descriptions

Bit	Field	Value	Description
31-20	Reserved	0	Reads return 0. Writes have no effect.
19-16	EWAIT	0-Fh	EEPROM Wait state Counter Replaces the RWAIT count in the EEPROM register. The same formulas that apply to RWAIT apply to EWAIT in the EEPROM bank.
15-0	Reserved	0	Reads return 0. Writes have no effect.

➔ FSM_WR_ENA 2-0 : 쓰기권한, EEPROM_CONFIG_HL 19-16 : 롬 레지스터에 있는 RWAIT count 형식으로 바꿈.

1.3 FSM_WR_ENA_HL

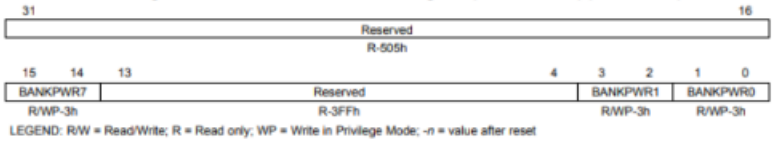
8bit 0000 0010

EEOROM_CONFIG_HL

8bit 0000 1111

7.10.14 Flash Bank Power Mode Register (FBPWRMODE)

Figure 7-24. Flash Bank Power Mode Register (FBPWRMODE) (offset = 40h)



LEGEND: R/W = Read/Write; R = Read only; WP = Write in Privilege Mode; -n = value after reset

Table 7-26. Flash Bank Power Mode Register (FBPWRMODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	505h	Do not write to these register bits.
15-14	BANKPWR7		Bank 7 Power Mode.
		0	Bank sleep mode
		1h	Bank standby mode
		2h	Reserved
		3h	Bank active mode
13-4	Reserved	3FFh	Do not write to these register bits.
3-2	BANKPWR1		Bank 1 Power Mode.
		0	Bank sleep mode
		1h	Bank standby mode
		2h	Reserved
		3h	Bank active mode
1-0	BANKPWR0		Bank 0 Power Mode.
		0	Bank sleep mode
		1h	Bank standby mode
		2h	Reserved
		3h	Bank active mode

BANKPWR0 1-0 , BANKWR1 3-2, BANKPWR7 15-14 = 3h, bank 활성화모드

그중 bank 0,1,7 을 파워모드로 설정한다.

1 c_int00() -> systemInit() -> trimLPO

```
void trimLPO(void)
{

/* USER CODE BEGIN (4) */
/* USER CODE END */

    /** @b Initialize Lpo: */
    /** Load TRIM values from OTP if present else load user defined values */
    /*SAFETYMCUSW 139 S MR:13.7 <APPROVED> "Hardware status bit read check" */
    if(LPO_TRIM_VALUE != 0xFFFFU)
    {

        systemREG1->LPOMONCTL  = (uint32)((uint32)1U << 24U)
                               | LPO_TRIM_VALUE;
    }
    else
    {

        systemREG1->LPOMONCTL   =  (uint32)((uint32)1U << 24U)
                                 | (uint32)((uint32)16U << 8U)
                                 | 16U;
    }
```

LPOMONCTL 의 하위 16 bit 에 LPO_TRIM_VALUE 값 대입함

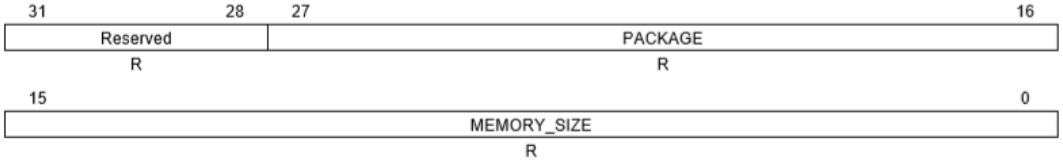
-0Xf0008 01B4 주소의 레지스터

7.5.2.2 Package and Memory Size

Package and memory size information can be determined from the device-specific datasheet, or can be computed by reading locations in the TI OTP Bank 0 registers.

The package and memory size can be read from TI OTP location F008 015Ch as shown in Figure 7-4 and described in Table 7-6.

Figure 7-4. TI OTP Bank 0 Package and Memory Size Information



LEGEND: R = Read only

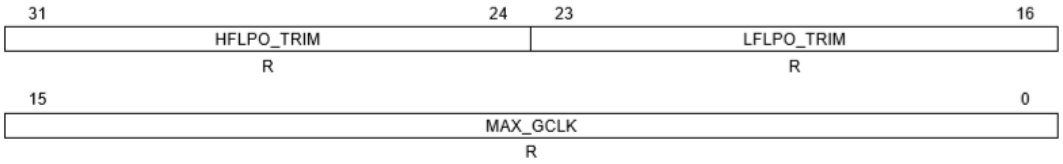
Table 7-6. TI OTP Bank 0 Package and Memory Size Information Field Descriptions

Bit	Field	Description
31-28	Reserved	Reserved
27-16	PACKAGE	Count of pins in the package.
15-0	MEMORY_SIZE	Flash memory size in Kbytes.

7.5.2.3 LPO Trim and Max HCLK

The HF LPO trim solution, LF LPO trim solution and maximum GCLK1 frequency can be read from TI OTP location F008 01B4h as shown in Figure 7-5 and described in Table 7-7.

Figure 7-5. TI OTP Bank 0 LPO Trim and Max HCLK Information



LEGEND: R = Read only

➔ Referance manual

패키지 및 메모리 크기 정보는 장치 별 데이터 시트에서 결정하거나 TI OTP Bank 0 레지스터의 위치를 읽음으로써 계산할 수 있습니다.

패키지 및 메모리 크기는 그림 7-4와 같이 TI OTP 위치 F008 015Ch에서 읽을 수 있으며 표 7-

HF LPO 트림 솔루션, LF LPO 트림 솔루션 및 최대 GCLK1 주파수는 그림 7-5와 표 7-7에서 설명한대로 TI OTP 위치 F008 01B4h에서 읽을 수 있습니다

/

›mparison clock for the crystal oscillator failure detection circu

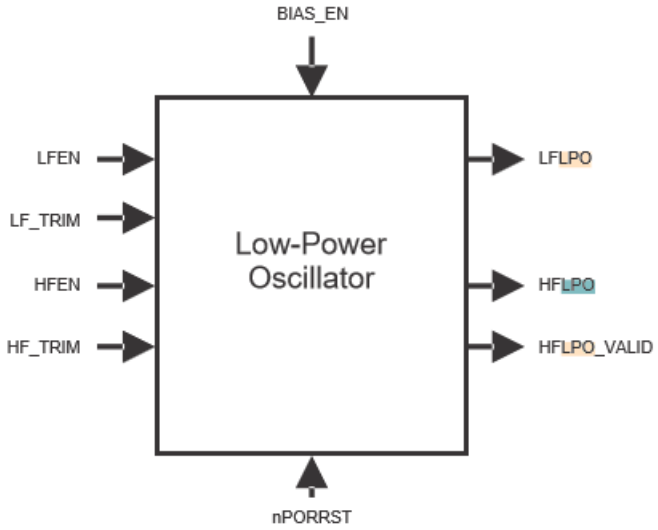


Figure 6-4. LPO Block Diagram

s a block diagram of the internal reference oscillator. This is

➔ Datasheet

```
/** - Wait for until clocks are locked */
```

SYS_CSVSTAT 뭘하는넘일까

SYS_CSDIS 는 또 뭘하는넘일까

➔ 이두가지로 비활성화, 활성화 되는 클럭을 구별한다. 신호를 안정화 하는데 시간이 걸리기 때문에 비활성화된 것들이 더 구별하기 쉽다. PLL을 생각해보자

GHVSRC : Clock 들을 어떻게 다룰지

MRC Instruction

명령어	동작	어셈블러
CDP	Data operation	CDP{cond} <cp_num>, <op1>, <CRd>, <CRn>, <CRm>{, <op2>}
MRC	코프로세스 레지스터의 정보를 ARM레지스터로 읽어 온다.	MRC{cond} <cp_num>, <op1>, <Rd>, <CRn>, <CRm>{, <op2>}
MCR	ARM레지스터의 정보를 코프로세스 레지스터로 읽어 온다.	MCR{cond} <cp_num>, <op1>, <Rd>, <CRn>, <CRm>{, <op2>}
MRRC	코프로세스의 정보를 한 쌍의 ARM 레지스터들에 전송한다.	MRRC{cond} <cp_num>, <op1>, <Rd>, <Rn>, <CRm>
MCRR	한 쌍의 ARM 레지스터들의 정보를 코프로세스에 전송한다.	MCRR{cond} <cp_num>, <op1>, <Rd>, <Rn>, <CRm>
LDC	메모리의 내용을 코프로세스 레지스터에 저장한다.	LDC{cond} <cp_num>, <CRd>, <a_mode5>
STC	코프로세스 레지스터의 내용을 메모리에 저장한다.	STC{cond} <cp_num>, <CRd>, <a_mode5>