

TI DSP, MCU, Xilinx Zynq FPGA 프로그래밍 전문가 과정

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Cortex-R5F RTI 분석

```
int main(void)
{
    /* USER CODE BEGIN (3) */
    rtiInit();

    gpioSetDirection(hetPORT1, 0xFFFFFFFF);

    rtiEnableNotification(rtiREG1, rtiNOTIFICATION_COMPARE0);

    _enable_IRQ_interrupt_();

    rtiStartCounter(rtiREG1, rtiCOUNTER_BLOCK0 );
    srand(time(NULL));

    while(1);

    /* USER CODE END */

    return 0;
}
```

먼저, 위와 같이 RTI 코드를 작성해보자.

rtiInit()에서 무엇을 하는지, 분석해보자.

```
75  /** - Setup NTU source, debug options and disable both counter blocks */
76  rtiREG1->GCTRL = (uint32)((uint32)0x5U << 16U) | 0x00000000U;
```

GCTRL의 18,16번 bit에 1을 넣어주고 있다. 데이터시트를 보자.

Table 17-2. RTI Global Control Register (RTIGCTRL) Field Descriptions

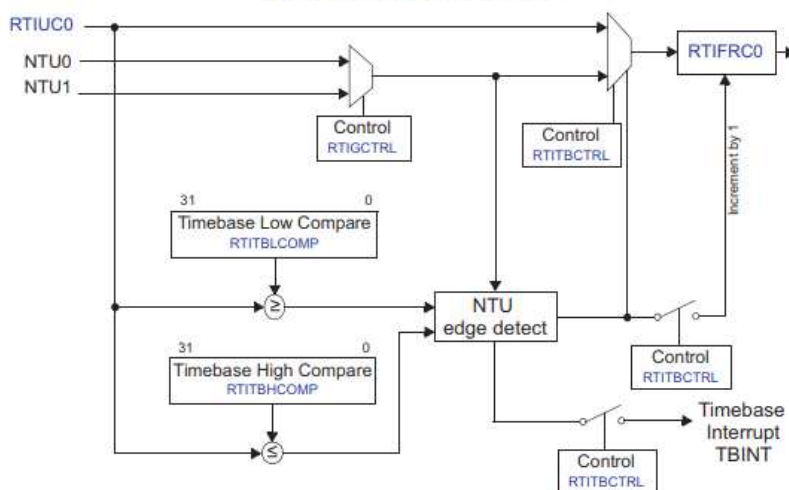
Bit	Field	Value	Description
31-20	Reserved	0	Reads return 0. Writes have no effect.
19-16	NTUSEL	0h 5h Ah Fh All other values	Select NTU signal. These bits determine which NTU input signal is used as external timebase NTU0 NTU1 NTU2 NTU3 Tied to 0
15	COS	0 1	Continue on suspend. This bit determines if both counters are stopped when the device goes into halting debug mode or if they continue counting. Counters are stopped while in halting debug mode. Counters are running while in halting debug mode.
14-2	Reserved	0	Reads return 0. Writes have no effect.
1	CNT1EN	0 1	Counter 1 enable. This bit starts and stops counter block 1 (RTIUC1 and RTIFRC1). Counter block 1 is stopped. Counter block 1 is running.
0	CNT0EN	0 1	Counter 0 enable. This bit starts and stops counter block 0 (RTIUC0 and RTIFRC0). Counter block 0 is stopped. Counter block 0 is running.

19-16번 비트에 5가 들어가니, NTU1이 external timebase로 사용됨을 알 수 있다.

external timebase가 뭔지 알아보자. 하지만, Description을 보니

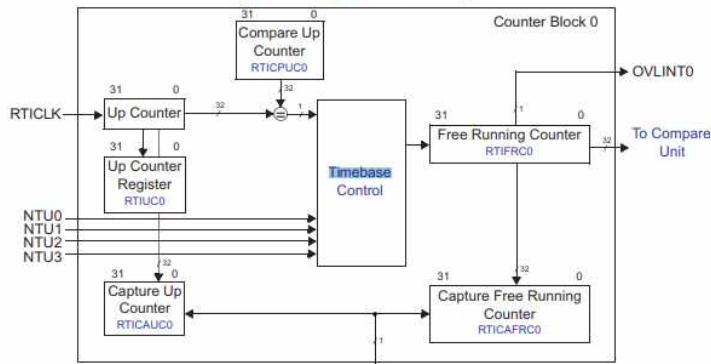
NTU0, NTU1, NTU2, NTU3이 한 mux로 물려있고, 그 중 하나가 선택되는 구조라는 것을 알 수 있다.

Figure 17-4. Timebase Control



NTU0와 NTU1만 물려있어서 이상해서 찾아보니

Figure 17-2. Counter Block Diagram



Block Diagram에서는 다 나와 있는 것을 볼 수 있다.

이 중 NTU1번을 선택한다는 뜻이다.

```
79 rtiREG1->TBCTRL = 0x00000000U;
```

TBCTRL을 알아보자

Table 17-3. RTI Timebase Control Register (RTITBCTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reads return 0. Writes have no effect.
1	INC	0 1	Increment free running counter 0. This bit determines whether the free running counter 0 (RTIFRC0) is automatically incremented if a falling clock on the NTU signal is detected. RTIFRC0 will not be incremented on a falling external clock. RTIFRC0 will be incremented on a falling external clock.
0	TBEXT	0 1	Timebase external. This bit selects whether the free running counter 0 (RTIFRC0) is clocked by the internal up counter 0 (RTIUC0) or from the external signal NTU. Setting the TBEXT bit from 0 to 1 will not increment RTIFRC0, since RTIUC0 is reset. When the timebase supervisor circuit detects a missing clock edge, then the TBEXT bit is reset. Only the software can select whether the external signal should be used. 0 RTIUC0 clocks RTIFRC0. 1 NTU clocks RTIFRC0.

2-31은 의미가 없고, 0, 1번비트 내용만 보자.

RTIUC0 clock을 끌어다가 RTIFRC0에 쓰고,

RTIFRC0 레지스터는 falling external clock일 때, 값이 증가하지 않는다.

```
85 rtiREG1->COMPCTRL = 0x00001000U | 0x00000100U | 0x00000000U | 0x00000000U;
```

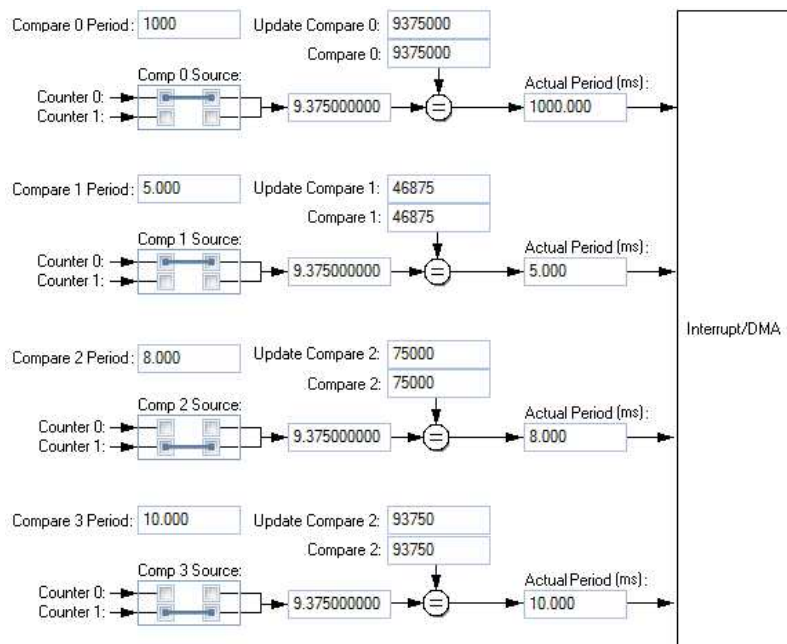
다음 코드는, COMPCTRL에 어떤 값을 넣어주고 있다. compare를 설정하는 레지스터인 듯 하다. 검색해보자.

Table 17-5. RTI Compare Control Register (RTICOMPCTRL) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reads return 0. Writes have no effect.
12	COMPSEL3	0 1	Compare select 3. This bit determines the counter with which the compare value held in compare register 3 (RTICOMP3) is compared. 0 Value will be compared with RTIFRC0. 1 Value will be compared with RTIFRC1.
11-9	Reserved	0	Reads return 0. Writes have no effect.
8	COMPSEL2	0 1	Compare select 2. This bit determines the counter with which the compare value held in compare register 2 (RTICOMP2) is compared. 0 Value will be compared with RTIFRC0. 1 Value will be compared with RTIFRC1.
7-5	Reserved	0	Reads return 0. Writes have no effect.
4	COMPSEL1	0 1	Compare select 1. This bit determines the counter with which the compare value held in compare register 1 (RTICOMP1) is compared. 0 Value will be compared with RTIFRC0. 1 Value will be compared with RTIFRC1.
3-1	Reserved	0	Reads return 0. Writes have no effect.
0	COMPSEL0	0 1	Compare select 0. This bit determines the counter with which the compare value held in compare register 0 (RTICOMP0) is compared. 0 Value will be compared with RTIFRC0. 1 Value will be compared with RTIFRC1.

8,12번 bit가 1이므로, RTICOMP2,3는 RTIFRC1과 비교를 할 것이고, RTICOMP0,1은 RTIFRC0와 비교할 것이다.

FRC는 Free Running Counter이므로, HalCoGen으로 보면,



COMP0,1은 counter0, COMP2,3는 counter1을 사용하는 이것을 말하는 듯 하다.

```
/** - Reset up counter 0 */
rtiREG1->CNT[0U].UCx = 0x00000000U;
```

Table 17-7. RTI Up Counter 0 Register (RTIUC0) Field Descriptions

Bit	Field	Value	Description
31-0	UC0	0-FFFF FFFFh	Up counter 0. This register holds the current value of the up counter 0 and prescales the RTI clock. It will be only updated by a previous read of free running counter 0 (RTIFRC0). This method of updating effectively gives a 64-bit read of both counters, without having the problem of a counter being updated between two consecutive reads on up counter 0 (RTIUC0) and free running counter 0 (RTIFRC0). A read of this counter returns the value of the counter at the time RTIFRC0 was read. A write to this counter presets it with a value. The counter then increments from this written value upwards. Note: If counters must be preset, they must be disabled in the RTIGCTRL register to ensure consistency between RTIUC0 and RTIFRC0. Note: If the preset value is bigger than the compare value stored in register RTICPUC0, then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

RTIFRC0를 0으로 초기화한다.

```
rtiREG1->CNT[0U].FRCx = 0x00000000U;
```

Table 17-6. RTI Free Running Counter 0 Register (RTIFRC0) Field Descriptions

Bit	Field	Value	Description
31-0	FRC0	0-FFFF FFFFh	Free running counter 0. This registers holds the current value of the free running counter 0. A read of this counter returns the current value of the counter. The counter can be preset by writing (in privileged mode only) to this register. The counter increments then from this written value upwards. Note: If counters must be preset, they must be disabled in the RTIGCTRL register to ensure consistency between RTIUC0 and RTIFRC0.

FRC도 0으로 초기화한다. FRC는 현재 UC값을 읽어오는 레지스터이다.

```
rtiREG1->CNT[0U].CPUCx = 7U;
```

Table 17-8. RTI Compare Up Counter 0 Register (RTICPUC0) Field Descriptions

Bit	Field	Value	Description
31-0	CPUC0	0-FFFF FFFFh	Compare up counter 0. This register holds the value that is compared with the up counter 0. When the compare shows a match, the free running counter 0 (RTIFRC0) is incremented. RTIUC0 is set to 0 when the counter value matches the RTICPUC0 value. The value set in this register prescales the RTI clock. If CPUC0 = 0, then $f_{FRC0} = RTICLK/(2^{32}+1)$ (Setting CPUC0 equal to 0 is not recommended. Doing so will hold the Up Counter at 0 for 2 RTICLK cycles after it overflows from FFFF FFFFh to 0.) If CPUC0 ≠ 0, then $f_{FRC0} = RTICLK/(RTICPUC0+1)$ A read of this register returns the current compare value. A write to this register: • If TBEXT = 0, the compare value is updated. • If TBEXT = 1, the compare value is unchanged.

분주비 7+1 = 8 설정

```

/** - Setup compare 0 value. This value is compared with selected free running counter. */
rtiREG1->CMP[0U].COMPx = 9375000U;

/** - Setup update compare 0 value. This value is added to the compare 0 value on each compare match. */
rtiREG1->CMP[0U].UDCPx = 9375000U;

```

Table 17-16. RTI Compare 0 Register (RTICOMP0) Field Descriptions

Bit	Field	Value	Description
31-0	COMP0	0-FFFF FFFFh	<p>Compare 0. This registers holds a value that is compared with the counter selected in the compare control logic. If RTIFRC0 or RTIFRC1, depending on the counter selected, matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>A read of this register will return the current compare value.</p> <p>A write to this register (in privileged mode only) will update the compare register with a new compare value.</p>

Table 17-17. RTI Update Compare 0 Register (RTIUDCP0) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP0	0-FFFF FFFFh	<p>Update compare 0. This register holds a value that is added to the value in the compare 0 (RTICOMP0) register each time a compare matches. This function allows periodic interrupts to be generated without software intervention.</p> <p>A read of this register will return the value to be added to the RTICOMP0 register on the next compare match.</p> <p>A write to this register will provide a new update value.</p>

비교값 설정, 즉, 인터럽트가 발생하는 주기를 설정하는 부분이다(UDCP).

$F = 9.375\text{MHz}$ 이고, $T = 1/9.375\mu\text{s} = 1/0.000009375$ 이므로, 비교값을 9375000으로 설정시, 주기가 1초가 된다.

COMP0의 역할은 compare의 초기값을 설정, 즉, 첫 인터럽트에 관여한다.

비슷한 코드들이 여러 개 준비해 있고 그 다음엔

```

/** - Clear all pending interrupts */
rtiREG1->INTFLAG = 0x0007000FU;

```

Bit	Field	Value	Description
31-19	Reserved	0	Reads return 0. Writes have no effect.
18	OVL1INT	0	Free running counter 1 overflow interrupt flag. This bit determines if an interrupt is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.
17	OVL0INT	0	Free running counter 0 overflow interrupt flag. This bit determines if an interrupt is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.
16	TBINT	0	Timebase interrupt flag. This flag is set when the TBEXT bit is cleared by detection of a missing external clock edge. It will not be set by clearing TBEXT by software. It determines if an interrupt is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.
15-4	Reserved	0	Reads return 0. Writes have no effect.
3	INT3	0	Interrupt flag 3. These bits determine if an interrupt due to a Compare 3 match is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.
2	INT2	0	Interrupt flag 2. These bits determine if an interrupt due to a Compare 2 match is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.
1	INT1	0	Interrupt flag 1. These bits determine if an interrupt due to a Compare 1 match is pending. <i>Read:</i> No interrupt is pending. <i>Write:</i> Bit is unchanged.
		1	<i>Read:</i> Interrupt is pending. <i>Write:</i> Bit is cleared to 0.

0,1,2,3 16,17,18번 bit를 set한다.

초기화 과정이라는 것을 알 수 있다.

```

/** - Disable all interrupts */
rtiREG1->CLEARINTENA = 0x00070F0FU;

```


Table 17-27. RTI Clear Interrupt Control Register (RTICLEARINTENA) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved	0	Reads return 0. Writes have no effect.
18	CLEAROVL1INT	0	Clear free running counter 1 overflow interrupt. <i>Read:</i> Interrupt is disabled. <i>Write:</i> Corresponding bit is unchanged.
		1	<i>Read:</i> Interrupt is enabled. <i>Write:</i> Interrupt is disabled.
17	CLEAROVL0INT	0	Clear free running counter 0 overflow interrupt. <i>Read:</i> Interrupt is disabled. <i>Write:</i> Corresponding bit is unchanged.
		1	<i>Read:</i> Interrupt is enabled. <i>Write:</i> Interrupt is disabled.
16	CLEARTBINT	0	Clear timebase interrupt. <i>Read:</i> Interrupt is disabled. <i>Write:</i> Corresponding bit is unchanged.
		1	<i>Read:</i> Interrupt is enabled. <i>Write:</i> Interrupt is disabled.
15-12	Reserved	0	Reads return 0. Writes have no effect.
11	CLEARDMA3	0	Clear compare DMA request 3. <i>Read:</i> DMA request is disabled. <i>Write:</i> Corresponding bit is unchanged.
		1	<i>Read:</i> DMA request is enabled. <i>Write:</i> DMA request is disabled.
10	CLEARDMA2	0	Clear compare DMA request 2. <i>Read:</i> DMA request is disabled. <i>Write:</i> Corresponding bit is unchanged.
		1	<i>Read:</i> DMA request is enabled. <i>Write:</i> DMA request is disabled.

인터럽트들을 disable하고 있다.

```

679 void rtiEnableNotification(rtiBASE_t *rtiREG, uint32 notification)
680 {
681 /* USER CODE BEGIN (38) */
682 /* USER CODE END */
683
684 rtiREG->INTFLAG = notification;
685 rtiREG->SETINTENA = notification;
686
687 /** @note The function rtiInit has to be called before this function can be used.\n
688 * This function has to be executed in privileged mode.
689 */
690
691 /* USER CODE BEGIN (39) */
692 /* USER CODE END */
693 }

```

인터럽트 0번(compare 0 match)은 다시 활성화한다.

`_enable_IRQ_interrupt_`

```

cpsie i
bx lr

.endasmfunc

```

`*cpsie` 명령어는 인터럽트를 활성화한다.

`cpsie i`를 하면, 인터럽트가 활성화되고, `cpsie if`를 하면 인터럽트와 fiq 모두 활성화됨.

```

void rtiStartCounter(rtiBASE_t *rtiREG, uint32 counter)
{
/* USER CODE BEGIN (4) */
/* USER CODE END */

rtiREG->GCTRL |= ((uint32)1U << (counter & 3U));

/** @note The function rtiInit has to be called before this function can be used.\n
* This function has to be executed in privileged mode.
*/

/* USER CODE BEGIN (5) */
/* USER CODE END */
}

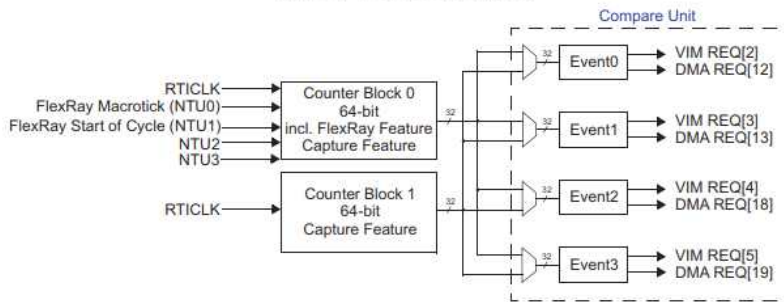
```

Table 17-2. RTI Global Control Register (RTIGCTRL) Field Descriptions

Bit	Field	Value	Description
31-20	Reserved	0	Reads return 0. Writes have no effect.
19-16	NTUSEL	0h 5h Ah Fh All other values	Select NTU signal. These bits determine which NTU input signal is used as external timebase. NTU0 NTU1 NTU2 NTU3 Tied to 0
15	COS	0 1	Continue on suspend. This bit determines if both counters are stopped when the device goes into halting debug mode or if they continue counting. Counters are stopped while in halting debug mode. Counters are running while in halting debug mode.
14-2	Reserved	0	Reads return 0. Writes have no effect.
1	CNT1EN	0 1	Counter 1 enable. This bit starts and stops counter block 1 (RTIUC1 and RTIFRC1). Counter block 1 is stopped. Counter block 1 is running.
0	CNT0EN	0 1	Counter 0 enable. This bit starts and stops counter block 0 (RTIUC0 and RTIFRC0). Counter block 0 is stopped. Counter block 0 is running.

0번 비트가 1이 되므로, Counter block 0 가 실행된다.

Figure 17-1. RTI Block Diagram



수치 해석 시도해보기

```
1  #include <stdio.h>
2  #include <math.h>
3  #define dt      0.000001
4  #define dtheta  0.000001
5  #define w      dtheta/dt
6  #define r      2
7  #define pi     3.14159
8  //각도에 따른 원 위의 x,y 좌표
9  #define posX(rad)  r*cos(rad)
10 #define posY(rad)  r*sin(rad)
11 //현재 각도에서 x성분 속도 구하기(x성분 위치 미분)
12 double v_x(double theta){
13     return (posX(theta + dtheta) - posX(theta))/dt;
14 }
15 //현재 각도에서 y성분 속도 구하기(y성분 위치 미분)
16 double v_y(double theta){
17     return (posY(theta + dtheta) - posY(theta))/dt;
18 }
19 //현재 각도에서 선속력(sqrt x^2+y^2)
20 double v(double theta){
21     return sqrt(pow(v_x(theta),2)+pow(v_y(theta),2));
22 }
23 //현재 각도에서 x성분 가속도 구하기(x성분 속도 미분)
24 double a_x(double theta){
25     return (v_x(theta + dtheta) - v_x(theta))/dt;
26 }
27 //현재 각도에서 y성분 가속도 구하기(y성분 속도 미분)
28 double a_y(double theta){
29     return (v_y(theta + dtheta) - v_y(theta))/dt;
30 }
31 //현재 각도에서 가속도의 크기
32 double a(double theta){
33     return sqrt(pow(a_x(theta),2)+pow(a_y(theta),2));
34 }
35 int main(void){
36     double rad = 0;
37     #if 1
38         //속도 출력
39         while(rad<=2*pi)
40         {
41             printf (".31f radian\tv_x(.31f) : %1fm/s\tv_y(.31f) : %1fm/s\tv(.31f) : %1fm/s\n",
42                     rad,rad,v_x(rad),rad,v_y(rad),rad,v(rad));
43             rad += dtheta;
44         }
45     #endif
46
47     #if 0
48         //가속도 출력
```



```

49
50
51 while(rad<=2*pi)
52 {
53     printf (".3lf radian\ta_x(.3lf) : %lfm/s^2\ta_y(.3lf) : %lfm/s^2\ta(.3lf) : %lfm/s^2\n",
54         rad,rad,a_x(rad),rad,a_y(rad),rad,a(rad));
55     rad += dtheta;
56 }
57 #endif
58 }
59
60

```

Colored by Color Scripter

0 radian

```

howi@ubuntu: ~/HomeworkBackup
0.003 radian v_x(0.003) : -0.005685m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005687m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005689m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005691m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005693m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005695m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005697m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005699m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005701m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005703m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005705m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005707m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005709m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005711m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005713m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005715m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005717m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005719m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005721m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005723m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005725m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005727m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian v_x(0.003) : -0.005729m/s v_y(0.003) : 1.999992m/s v(0.003) : 2.000000m/s
0.003 radian

howi@ubuntu: ~/HomeworkBackup
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006758m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006760m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006762m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -2.000178m/s^2 a_y(0.003) : -0.006765m/s^2 a(0.003) : 2.000189m/s^2
0.003 radian a_x(0.003) : -1.999734m/s^2 a_y(0.003) : -0.006765m/s^2 a(0.003) : 1.999745m/s^2
0.003 radian a_x(0.003) : -2.000178m/s^2 a_y(0.003) : -0.006768m/s^2 a(0.003) : 2.000189m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006771m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006771m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006774m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006776m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006778m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -2.000178m/s^2 a_y(0.003) : -0.006780m/s^2 a(0.003) : 2.000189m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006783m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006784m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006785m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006789m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006790m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -2.000178m/s^2 a_y(0.003) : -0.006791m/s^2 a(0.003) : 2.000189m/s^2
0.003 radian a_x(0.003) : -1.999734m/s^2 a_y(0.003) : -0.006795m/s^2 a(0.003) : 1.999745m/s^2
0.003 radian a_x(0.003) : -2.000178m/s^2 a_y(0.003) : -0.006795m/s^2 a(0.003) : 2.000189m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006798m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006801m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006801m/s^2 a(0.003) : 1.999967m/s^2
0.003 radian a_x(0.003) : -1.999956m/s^2 a_y(0.003) : -0.006804m/s^2

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[illegible][illegible]