TI DSP, MCU 및 Xilinx Zynq FPGA
프로그래밍 전문가 과정

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63 일차

FPGA 이해하기 좋은책들

MCU 에서 했던것을 FPGA 에서

우리가 징크(를 쓰고있음

vdhl 이랑

zynq 란 PL+PS 로 구성되있음
PL 은 프로그램 로직
프로그램로직은 베릴로그랑 vhdl 이 동작하는 영역
즉 트랜지스터가 그만큼 많이박혀있음

PS 는 프로세싱 시스템
한마디로 리눅스가 올라갈수있음

우리는 PL 과 PS 를 묶어서 써야함

절차를 밟으려하는것

아직은 PL

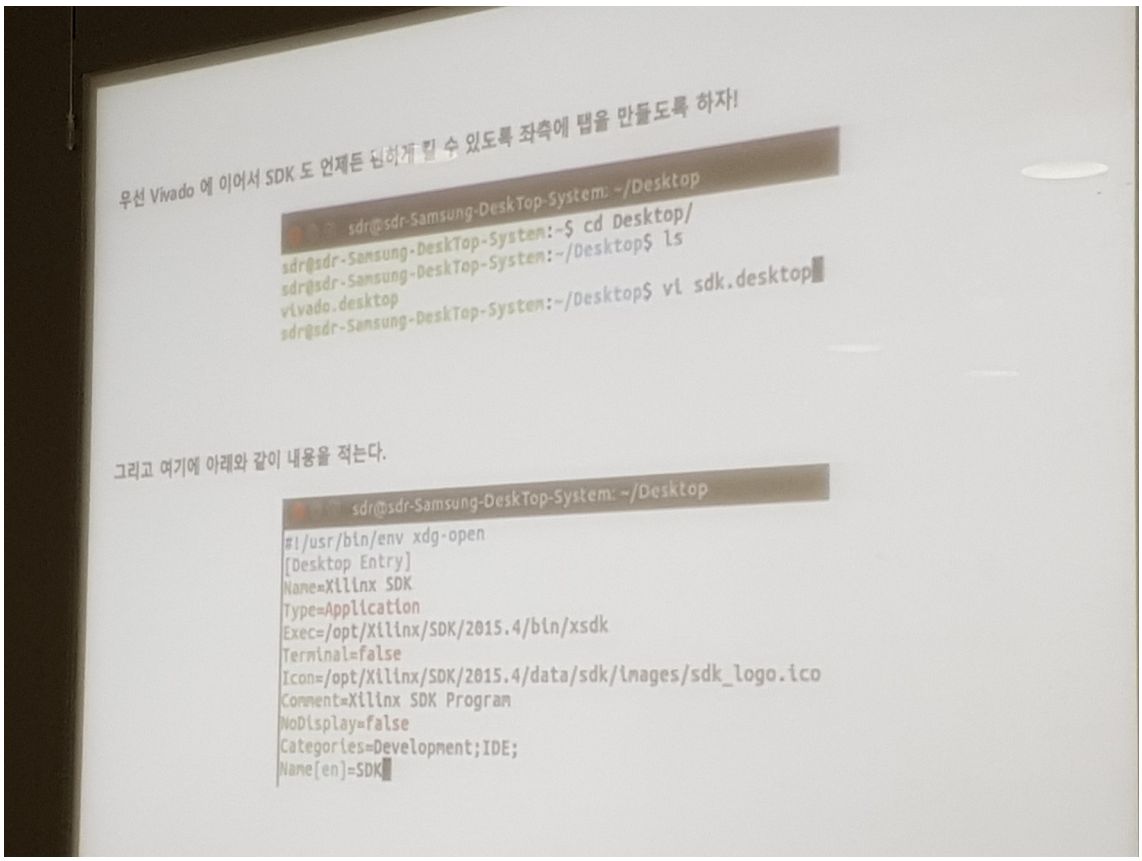
세팅 -
데스크톱에 이런걸 만들것

```
yong@yong-Z20NH-AS51B5U:~/Vivado/2017.1/bin$ ./vivado
CRITICAL WARNING: [Common 17-183] Failed to open handle vivado.jou. Please check
 access permission of directory '/home/yong/Vivado/2017.1/bin'. You should resta
rt the application from a writable working directory.
CRITICAL WARNING: [Common 17-183] Failed to open handle vivado.log. Please check
 access permission of directory '/home/yong/Vivado/2017.1/bin'. You should resta
rt the application from a writable working directory.

****** Vivado v2017.1 (64-bit)
  **** SW Build 1846317 on Fri Apr 14 18:54:47 MDT 2017
  **** IP Build 1846188 on Fri Apr 14 20:52:08 MDT 2017
    ** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

start_gui
```

어디서든 비바도 실행을 하기위해 작업을 세팅하는것



// 이거 문제잇음 수정필요(opt 설정이 나을거같음)
#!/usr/bin/env xdg-open
[Desktop Entry]
Name=xilinx SDK
Type=Application
Exec=/home/SDK/2017.1/bin/xsdk
Terminal=false
Icon=/home/SDK/2017.1/data/sdk/images/sdk_logo.ico
Comment=xilinx SDK Program
NoDisplay=false
Categories=Development;IDE;
Name[en]=SDK

#!/usr/bin/env xdg-open
[Desktop Entry]
Name=Xilinx SDK
Type=Application
Exec=/home/yong/SDK/2017.1/bin/xsdk
Terminal=false
Icon=/home/yong/SDK/2017.1/data/sdk/images/sdk_logo.ico
Comment=Xilinx SDK Program
NoDisplay=false
Categories=Development;IDE;
Name[en]=SDK

sdk 가 됫으면 비바도에도 동일한 작업을 해야함

홈 디렉토리에 Desktop 디렉토리가 바탕화면에 해당한다.

```
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ cd ~/Desktop/
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ vi vivado.desktop
```

그리고 아래와 같이 기록한다.

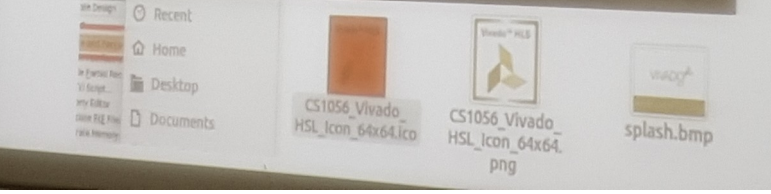
```
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
#!/usr/bin/env xdg-open
[Desktop Entry]
Name=Xilinx Vivado
Type=Application
Exec=/opt/Xilinx/Vivado/2017.4/bin/vivado
Terminal=false
Icon=/opt/Xilinx/Vivado/2017.4/common/icons/CS1056_Vivado_HSL_Icon_64x64.ico
Comment=Xilinx Vivado Program
NoDisplay=false
Categories=Development;IDE;
Name[en]=Vivado
~
~
~
~
~
~
"vivado.desktop" 11L, 300C
```

홈 디렉토리에 Desktop 디렉토리가 바탕화면에 해당한다.

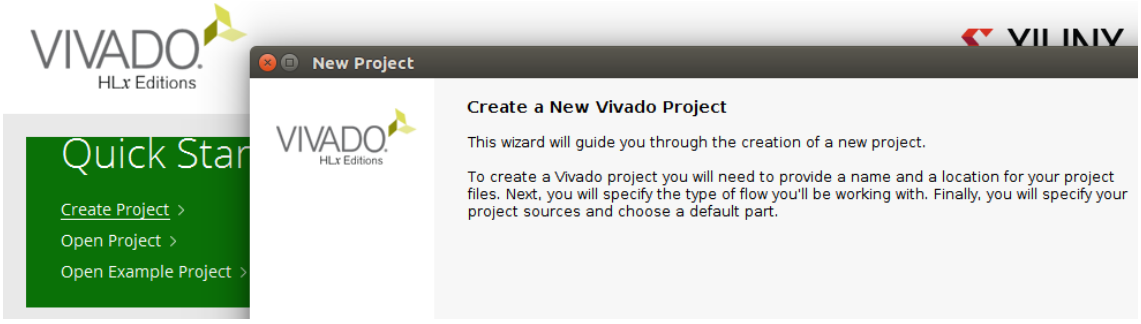
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ cd ~/Desktop/
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ vi vivado.desktop

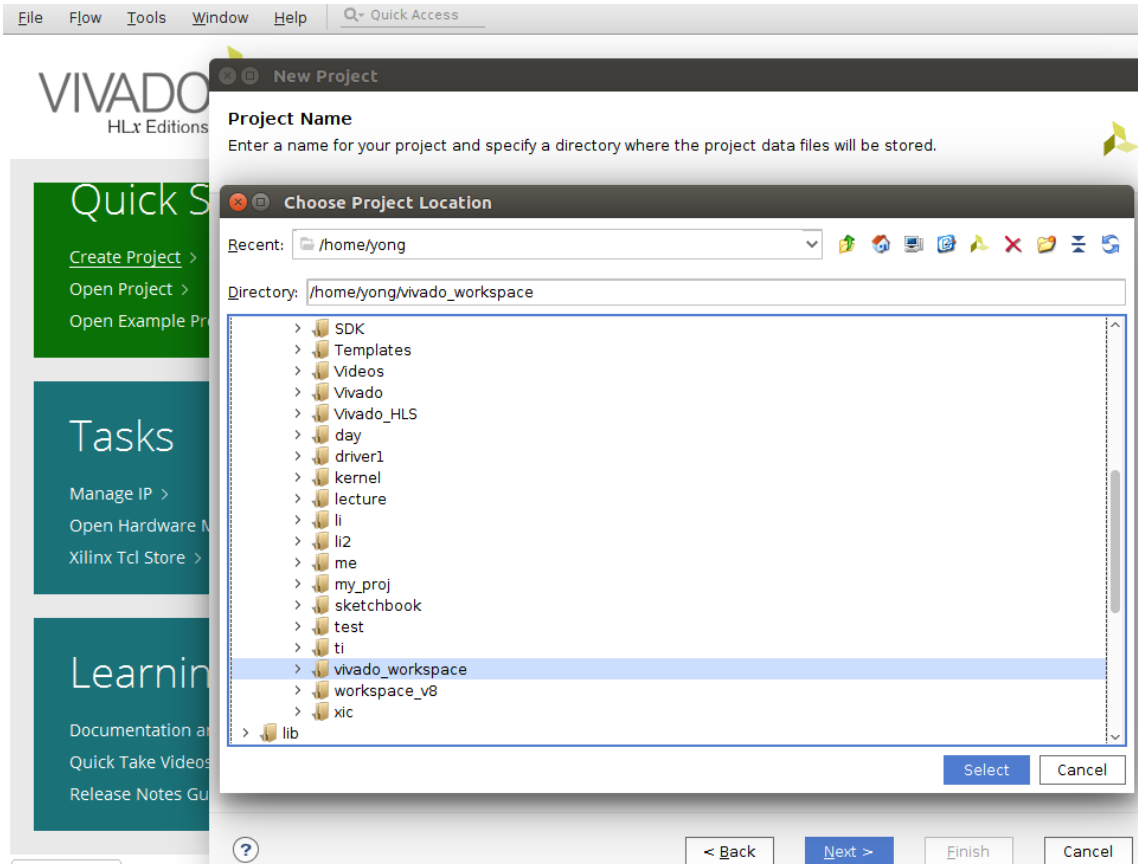
그리고 아래와 같이 기록한다.

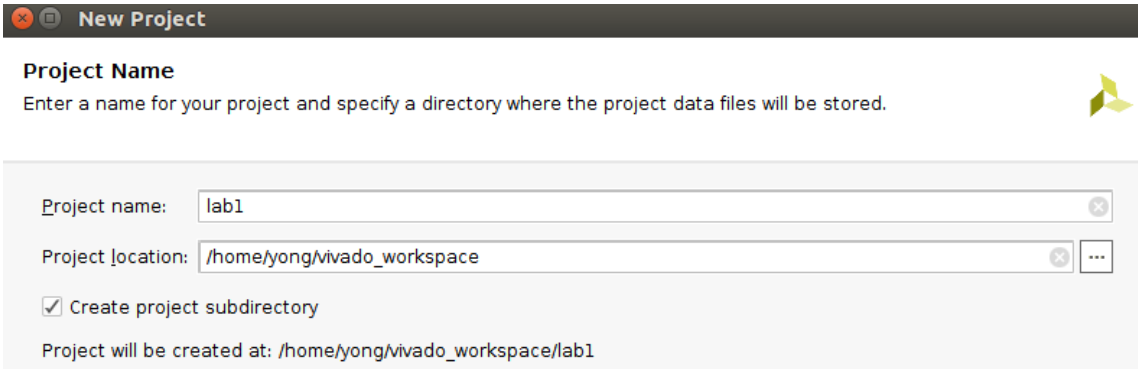
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
#!/usr/bin/env xdg-open
[Desktop Entry]
Name=Xilinx Vivado
Type=Application
Exec=/opt/Xilinx/Vivado/2017.4/bin/vivado
Terminal=false
Icon=/opt/Xilinx/Vivado/2017.4/common/icons/CS1056_Vivado_HSL_Icon_64x64.ico
Comment=Xilinx Vivado Program
NoDisplay=false
Categories=Development;IDE;
Name[en]=Vivado
~
~
~
~
~
~
"vivado.desktop" 11L, 300C



create new vivado

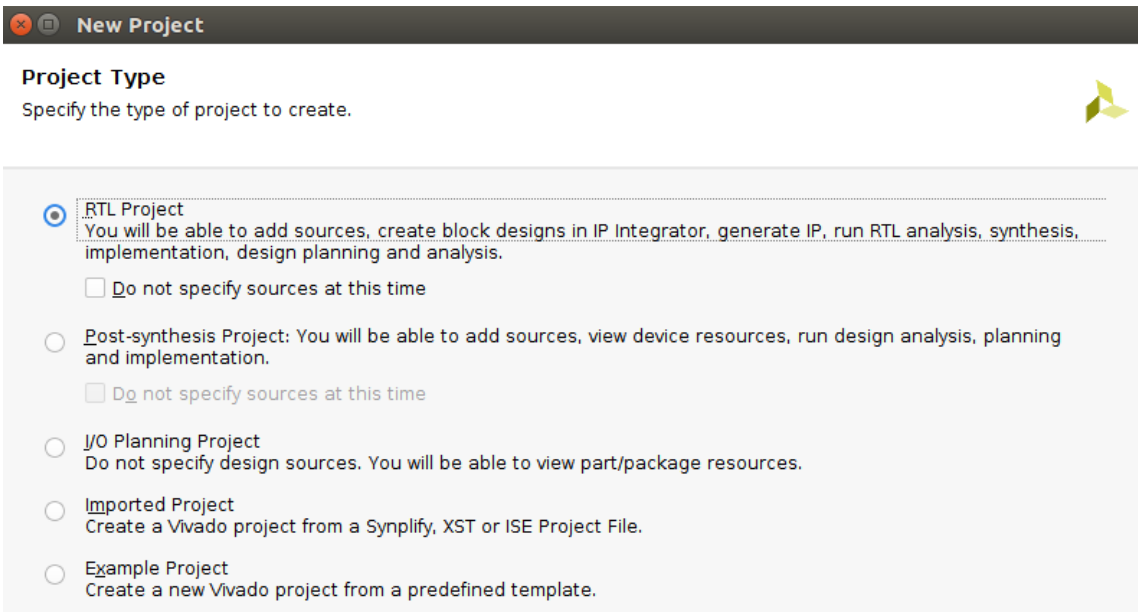






→ Next

//RTL 프로젝트로 설정



verilog(베릴로그), verilog(베릴로그)로 하고 넥트스 넥스트
//보드에서 자이보 선택

cd Vivado/2017.1/data/boards/board_files

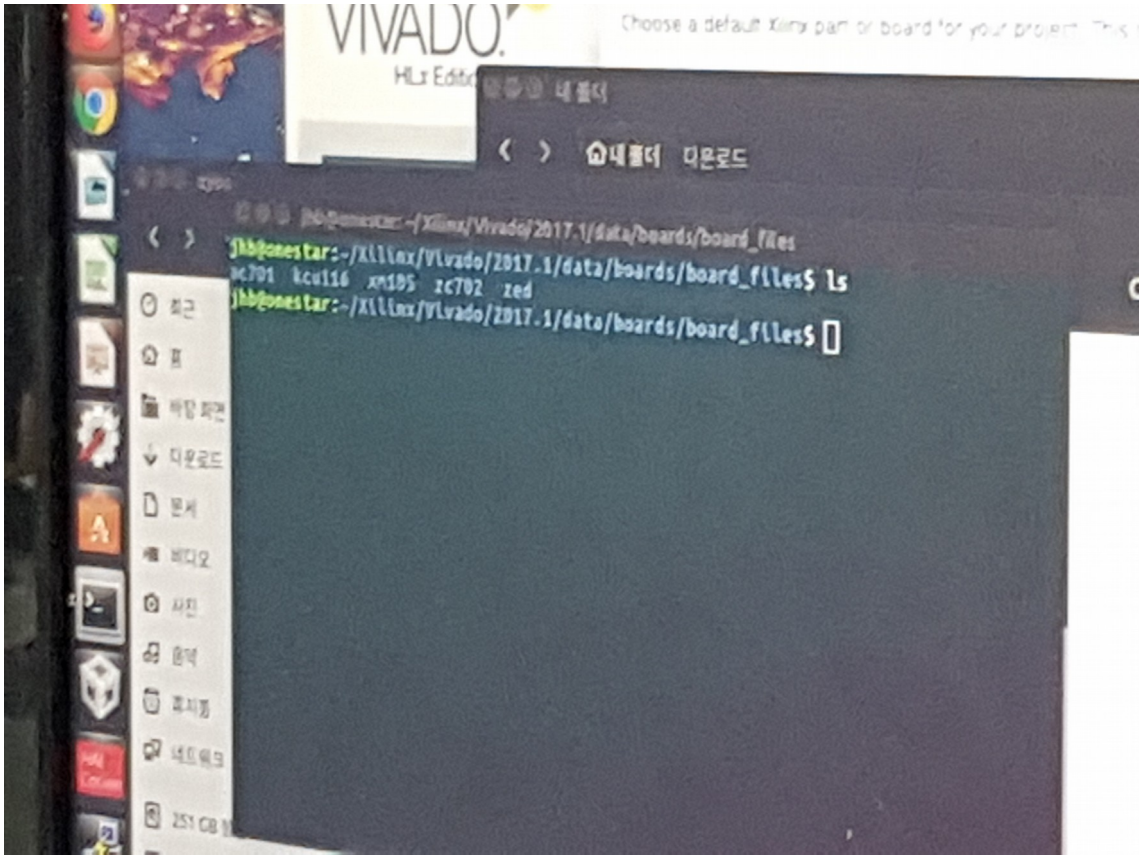
보드가없어?→
https://reference.digilentinc.com/reference/software/vivado/board-files
다운받으면
데이타-보드-보드파일

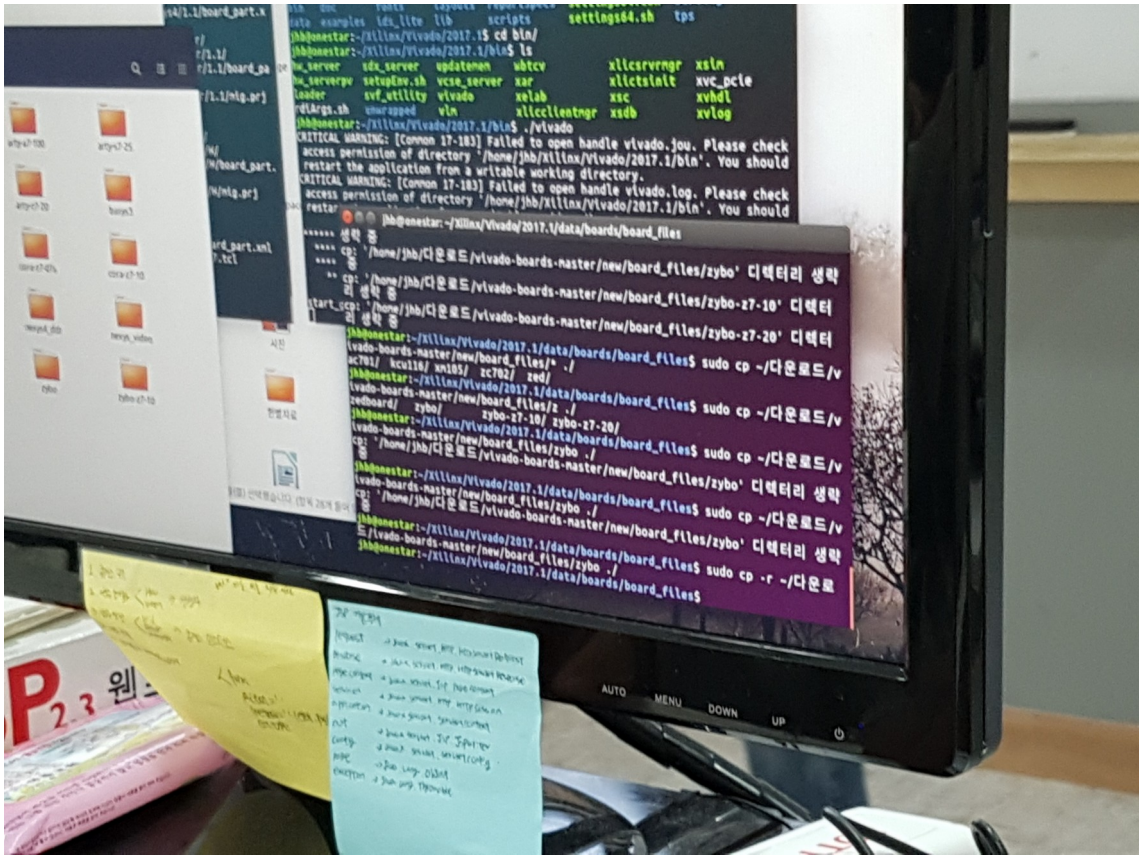
```
yong@yong-Z20NH-AS51B5U:~/Vivado/2017.1/data/boards/board_files$ sudo cp -r ~/Do
wnloads/vivado-boards-master/new/board_files/* ./
[sudo] password for yong:
yong@yong-Z20NH-AS51B5U:~/Vivado/2017.1/data/boards/board_files$ ls
ac701        arty-s7-50   cmod_a7-35t  nexys4       zc702        zybo-z7-20
arty         arty-z7-10   cora-z7-07s  nexys4_ddr   zed
arty-a7-100  arty-z7-20   cora-z7-10   nexys_video  zedboard
arty-a7-35   basys3       genesys2     sword        zybo
arty-s7-25   cmod_a7-15t  kcu116       xm105        zybo-z7-10
```

~/Xilinx/Vivado/2017.1/data/boards/board_files
??// 옮길위치

아까 다운받은거
unzip vivado-boards-master.zip

이거를 저기 데이타 보드파일로 복사옮김
cp ~/Downloads/vivado-boards-master/board_files ./


VIVADO
Choose a default Xilinx part or board for your project. This
네틀더
다운로드
jhb@onestar:~/Xilinx/Vivado/2017.1/data/boards/board_files
jhb@onestar:~/Xilinx/Vivado/2017.1/data/boards/board_files$ ls
zc702 zed
jhb@onestar:~/Xilinx/Vivado/2017.1/data/boards/board_files$
최근
표
바탕 화면
다운로드
문서
비디오
사진
음악
휴지통
네트워크



New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter/ Preview

Vendor: All

Display Name: All

Board Rev: Latest

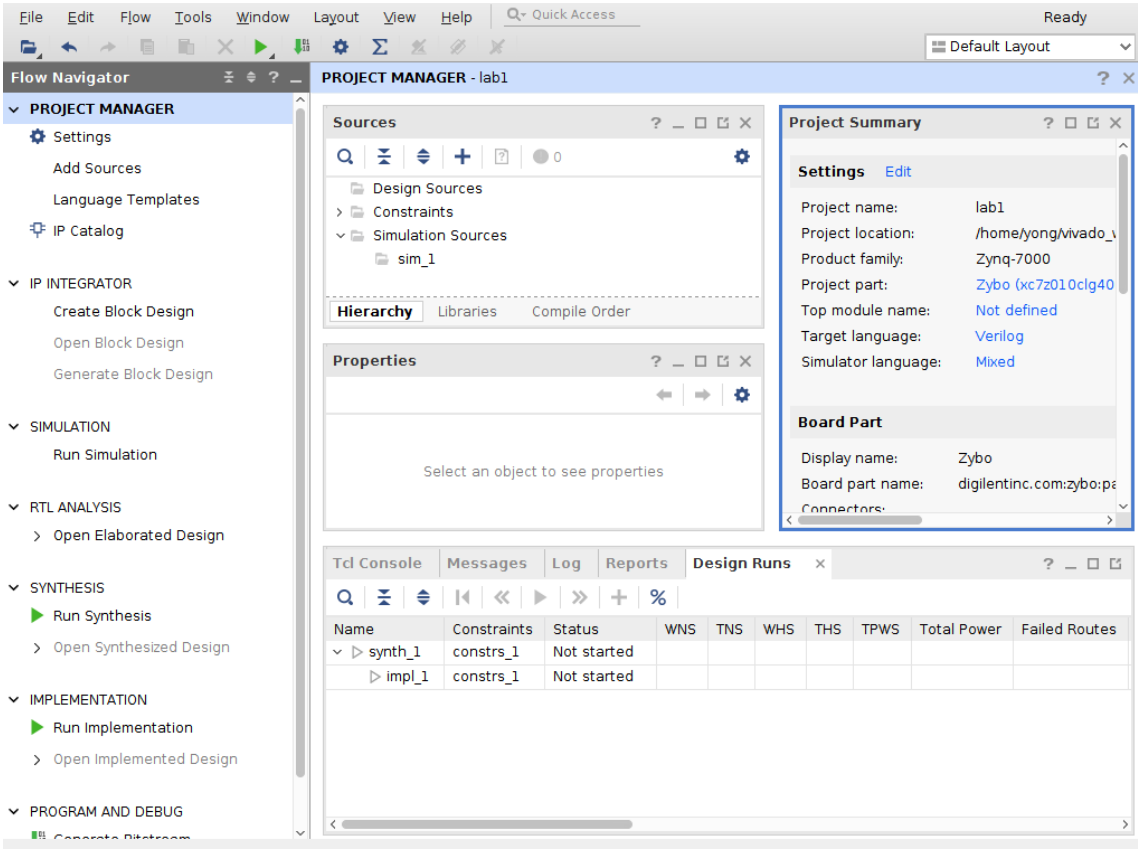
Reset All Filters

Search:

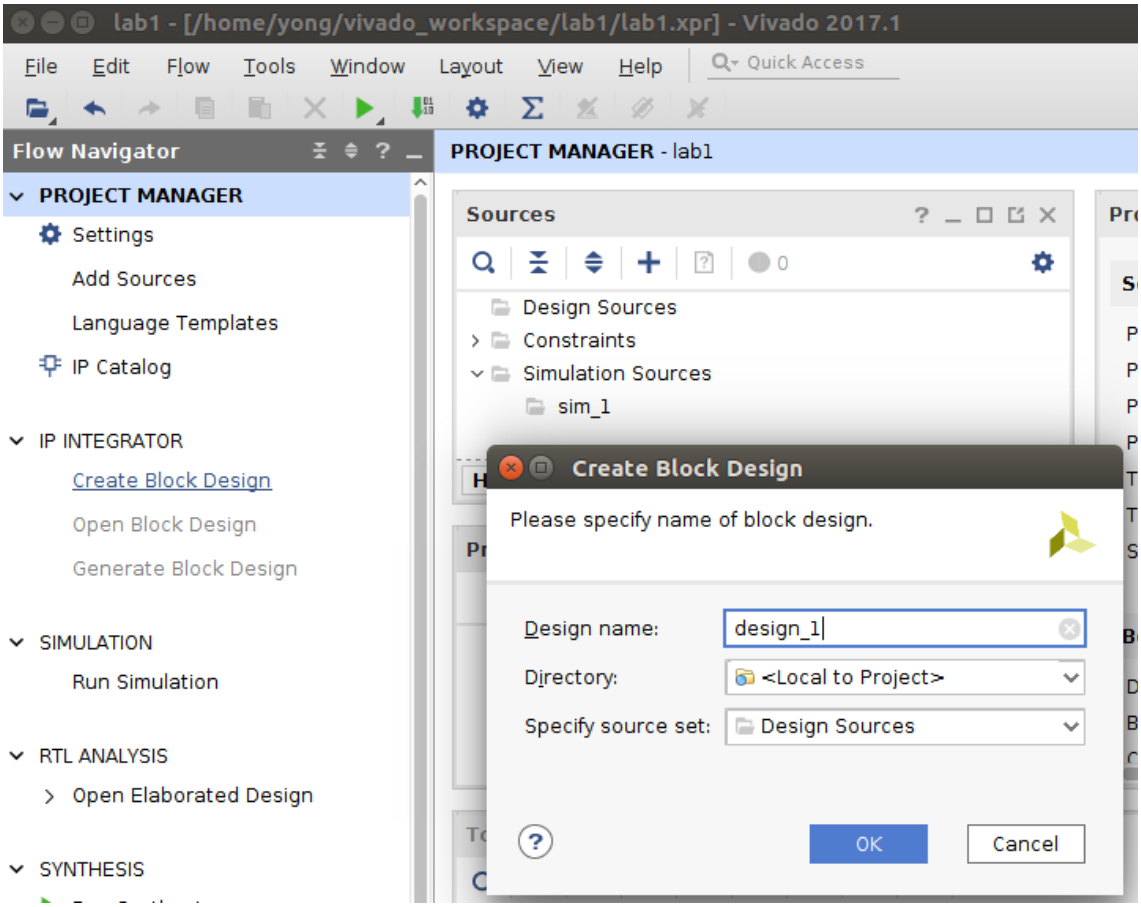
Display Name	Vendor	Board Rev	Part	I/O Pir
Nexys Video	digilentinc.com	A.0	xc7a200tsbg484-1	484
Zedboard	digilentinc.com	D.3	xc7z020clg484-1	484
Zybo Z7-10	digilentinc.com	B.2	xc7z010clg400-1	400
Zybo Z7-20	digilentinc.com	B.2	xc7z020clg400-1	400
Zybo	digilentinc.com	B.3	xc7z010clg400-1	400
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484

No Board Connectors

< Back Next > Finish Cancel

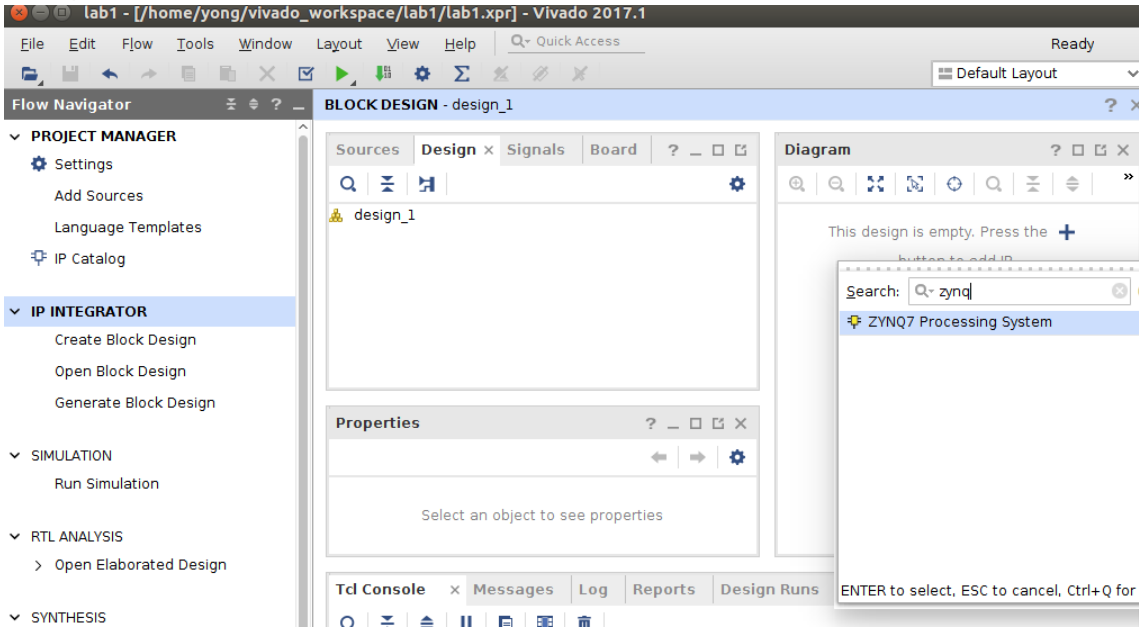


//create block 디자인 누르면 이게 나옴

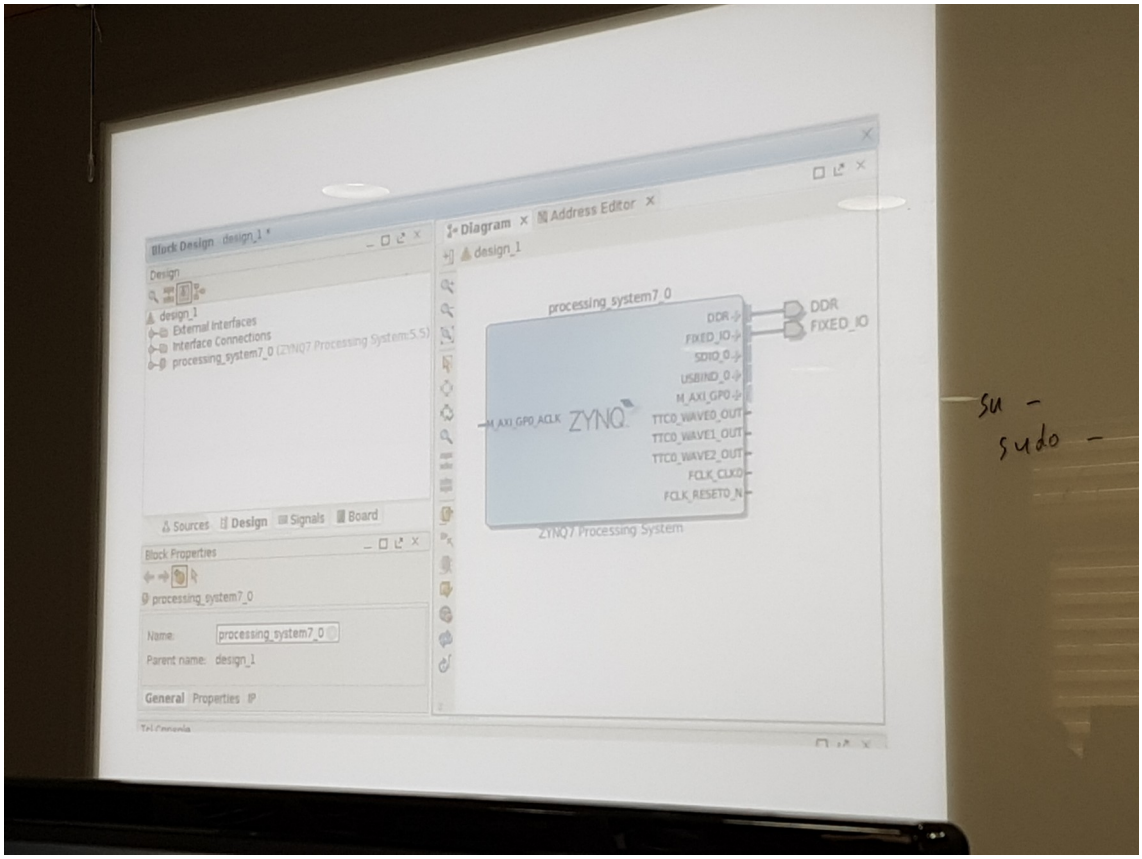


//서치

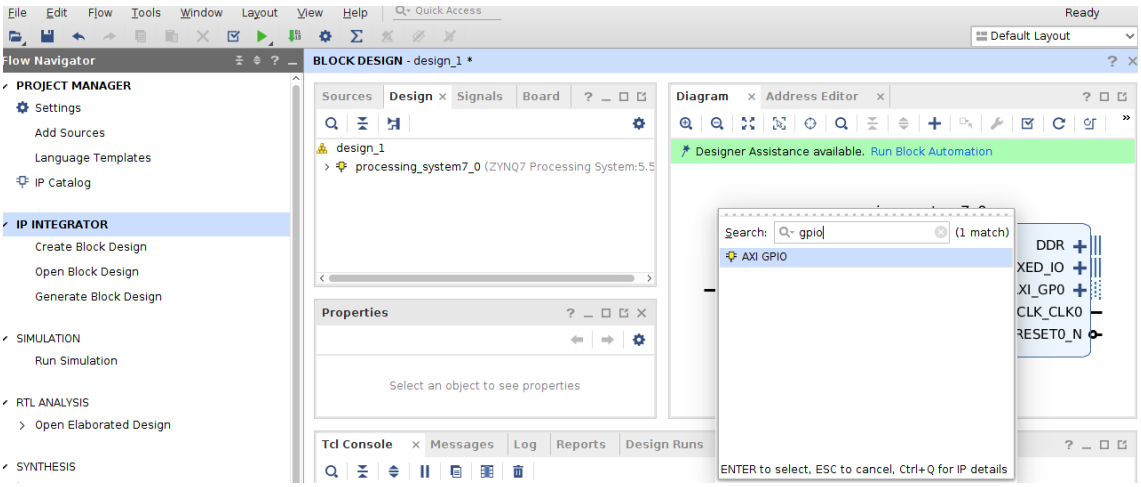
안보이면 + 클릭



//run



//+누르고 gpio



gpio 나왔으면 gpio 더블클릭
custom 으로 바꾸기