

TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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목차

- Cortex-R5F 부트로더 분석

0xF00801B4U & 0xFFFF0000U를 연산하면 0xF0080000이 된다. 이 값을 보겠다는 뜻이 되고 >>16U는 최상위 16비트만 확인 하겠다는 뜻이 된다. HFLPO_TRIM과 LFLPO_TRIM을 확인하면 된다. 그럼 LPO가 무엇인지 알아보도록 한다.

6.6.1.2 Low-Power Oscillator

The Low-Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

6.6.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power to reduce power consumption. This is connected as clock source 4 of the Global Clock Module (GCM).
- Supplies a high-frequency clock for nontiming-critical systems. This is connected as clock source 5 of the GCM.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

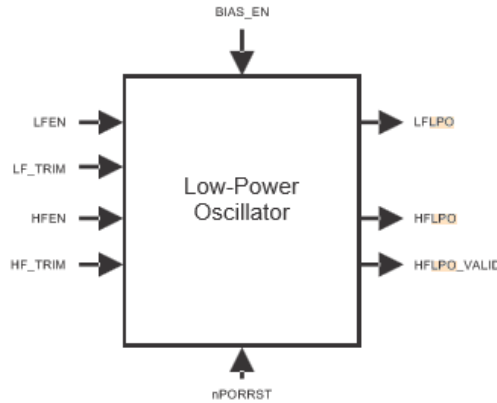


Figure 6-4. LPO Block Diagram

Figure 6-4 shows a block diagram of the internal reference oscillator. This is a low-power oscillator (LPO) and provides two clock sources: one nominally 80 kHz and one nominally 10 MHz.

LPO는 Low-Power Oscillator로 single macro에 HF LPO와 LF LPO 2개의 oscillator로 구성되어 있다. 주요 특징은 전력 소비를 줄이기 위해 매우 낮은 전력으로 클럭을 공급하고 GCM (Global Clock Module)의 클럭 소스 4로 연결된다. 중요하지 않은 시스템에는 고주파 클럭을 공급한다. 이 것은 GCM의 클럭 소스 5로 연결된다. 크리스털 오실레이터 고장 검출 회로의 비교 클럭을 제공한다.

if문을 들어가면 `systemREG1->LPOMONCTL = (uint32)((uint32)1U << 24U)`라는 코드가 나온다.

System and Peripheral Control Registers

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2.5.1.30 LPO/Clock Monitor Control Register (LPOMONCTL)

The LPOMONCTL register, shown in Figure 2-37 and described in Table 2-49, controls the Low Frequency (Clock Source 4) and High Frequency (Clock Source 5) Low Power Oscillator's trim values.

Figure 2-37. LPO/Clock Monitor Control Register (LPOMONCTL) (offset = 088h)

31	25	24	23	17	16
Reserved		BIAS ENABLE	Reserved	OSCFRQCONFIGCNT	
R-0		R/WP-1	R-0	R/WP-0	
15	13	12	8	7	5
Reserved		HFTRIM	Reserved	LFTRIM	0
R-0		R/WP-10h	R-0	R/WP-10h	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -n = value after reset

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Reads return 0. Writes have no effect.
24	BIAS ENABLE	0 1	Bias enable. The bias circuit inside the low-power oscillator (LPO) is disabled. The bias circuit inside the low-power oscillator (LPO) is enabled.
23-17	Reserved	0	Reads return 0. Writes have no effect.
16	OSCFRQCONFIGCNT	0 1	Configures the counter based on OSC frequency. Read: OSC freq is ≤ 20MHz. Write: A write of 0 has no effect. Read: OSC freq is > 20MHz and ≤ 80MHz. Write: A write of 1 has no effect.
15-13	Reserved	0	Reads return 0. Writes have no effect.

여기서 LPOMONCTL의 24비트를 1로 셋팅하고 있는 것이므로 LPOMONCTL이 무엇을 셋팅하고 있는 건지 확인한다. 24비트는 바이어스를 허용하는지에 대한 비트이다. 이를 1로 셋팅해주면 LPO 내부의 바이어스 회로가 활성화된다. 이를 LPO_TRIM_VALUE와 OR 연산을 해주게 되는데

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions (continued)

Bit	Field	Value	Description
12-8	HFTRIM		High-frequency oscillator trim value. This four-bit value is used to center the HF oscillator's frequency. Caution: This value should only be changed when the HF oscillator is not the source for a clock domain, otherwise a system failure could result. The following values are the ratio: f / f_0 in the F021 process.
		0	29.52
		1h	34.24%
		2h	38.85%
		3h	43.45%
		4h	47.99%
		5h	52.55%
		6h	57.02%
		7h	61.46%
		8h	65.92%
		9h	70.17
		Ah	74.55%
		Bh	78.92%
		Ch	83.17%
		Dh	87.43%
		Eh	91.75%
		Fh	95.89%
		10h	100.00% Default at Reset.
		11h	104.09
		12h	108.17