

TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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수학

1) 확률밀도함수 & 감마함수

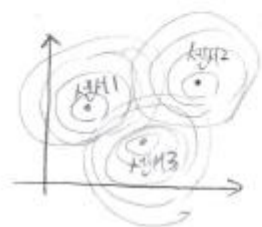
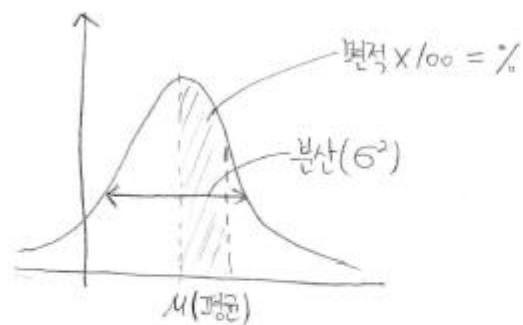
2) 감마함수와 정규분포 1

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1) 확률밀도함수

○ 확률밀도함수



⇒ 랜덤프로세스

★
확률밀도 함수는
절구간에 대해 적분하면
그 결과는 언제나 1이다.

• 서로 다른 정규분포 함수
⇒ • 감마함수
• 칼만 필터

○ 감마함수 - 팩토리얼 실수로 확장

$$\gamma(x) = \int_0^{\infty} e^{-t} t^{x-1} dt, \quad t = -\ln u, \quad du = -e^{-t} dt$$

$$\gamma(x) = \int_0^1 [-\ln(u)]^{x-1} du$$

$$\gamma(x+1) = \int_0^{\infty} e^{-t} t^x dt$$

$$= [-e^{-t} t^x]_0^{\infty} - \int_0^{\infty} -e^{-t} x t^{x-1} dt$$

$$= x \gamma(x)$$

$$\gamma(1) = 1 \quad \bullet \text{ 팩토리얼 함수의 일반화}$$

~~~~~  
• 정규분포 해석용이

## 2) 감마함수와 정규분포 1

○ 감마함수와 정규분포 1

$$y = e^{-ax^2}$$

$$\int_{-\infty}^{\infty} e^{-ax^2} dx = S \times \int_{-\infty}^{\infty} e^{-ay^2} dy = S$$

$$\Rightarrow \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} e^{-a(x^2+y^2)} dx dy = S^2$$

↓  
원의 방정식  $x^2+y^2=r^2$

$$\Rightarrow \int_0^{2\pi} \int_0^{\infty} e^{-ar^2} \cdot r dr d\theta = S^2$$

치환  $t = ar^2 \quad dr = \frac{dt}{2ar}$

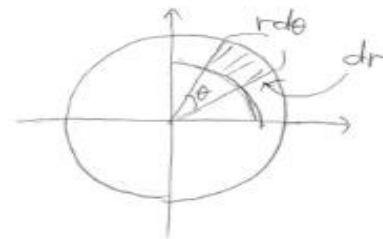
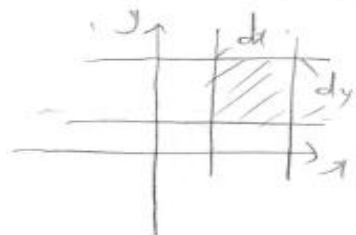
$$= \int_0^{2\pi} \int_0^{\infty} e^{-t} \frac{1}{2a} dt d\theta = \int_0^{2\pi} \left[ e^{-t} \frac{1}{2a} \right]_0^{\infty} d\theta = \int_0^{2\pi} \frac{1}{2a} d\theta = \frac{\pi}{a} = S^2$$

$$\therefore \int_{-\infty}^{\infty} e^{-ax^2} dx = \sqrt{\frac{\pi}{a}}$$

$$\ast \underline{y = \sqrt{\frac{a}{\pi}} e^{-ax^2}} \quad (\text{정규분포})$$

↑  $a$ 가 분산을 결정함.

\* 좌표계  $\rightarrow$  극좌표계



$dx dy$

↓ 극좌표

$r dr d\theta$

- \* 추가 공부
1. 프아싱 곱포
  2. chi-square distribution

### 3) 감마함수와 정규분포 2

○ 감마함수와 정규분포 2

$$y = \sqrt{\frac{a}{\pi}} e^{-ax^2}$$

$$\sigma^2 = \int_{-\infty}^{\infty} (x-m)^2 y \, dx$$

평균 (가우시안 분포의 평균은 0)

$$= \int_{-\infty}^{\infty} x^2 \sqrt{\frac{a}{\pi}} e^{-ax^2} \, dx$$

$$= \sqrt{\frac{a}{\pi}} \int_{-\infty}^{\infty} \frac{x}{g} \frac{x}{f'} e^{-ax^2} \, dx$$

$$= \left[ -\frac{x}{2a} e^{-ax^2} \right]_{-\infty}^{\infty} + \int_{-\infty}^{\infty} \frac{1}{2a} e^{-ax^2} \, dx$$

$$= \sqrt{\frac{a}{\pi}} \cdot \frac{1}{2a} \cdot \sqrt{\frac{\pi}{a}}$$

$$\sigma^2 = \frac{1}{2a}$$

$$\therefore a = \frac{1}{2\sigma^2}$$

$$y = \sqrt{\frac{1}{2\pi\sigma^2}} e^{-\frac{x^2}{2\sigma^2}}$$

$$\star \int_{-\infty}^{\infty} e^{-x^2} \, dx \quad (\text{가우시안})$$

$$= 2 \int_0^{\infty} e^{-x^2} \, dx = \sqrt{\pi}$$

$$x^2 = t \Rightarrow x = \sqrt{t}$$

$$dx = \frac{1}{2} t^{-\frac{1}{2}} \, dt$$



$$= 2 \int_0^{\infty} e^{-t} \frac{1}{2} t^{-\frac{1}{2}} \, dt$$

$$= \int_0^{\infty} e^{-t} t^{-\frac{1}{2}} \, dt$$


$$= \Gamma\left(\frac{1}{2}\right)$$

$$\therefore \int_{-\infty}^{\infty} e^{-x^2} \, dx = \Gamma\left(\frac{1}{2}\right) = \sqrt{\pi}$$


# FPGA 환경설정 (Xilinx) 1

 Applications Products Developer Zone Support About 


*shipment will no longer be available for ordering and will only be available for download at Xilinx.com.*

 [Vivado HLx 2017.1: WebPACK and Editions - Windows Self Extracting Web Installer](#) (EXE - 51.57 MB)

MD5 SUM Value :  
df4c2611b3fdedb8c8f184bf7ee5bbba


 [Vivado HLx 2017.1: WebPACK and Editions - Linux Self Extracting Web Installer](#) (BIN - 85.23 MB)

MD5 SUM Value :  
42fd14f5472de77a54ba1f847c00eec2

 [Vivado HLx 2017.1: All OS Installer Single-File Download](#) (TAR/GZIP - 20.21 GB)

MD5 SUM Value :  
ee351905f061e19751999e69b41f4b22

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# FPGA 환경설정 (Xilinx) 2

Select Edition to Install

XILINX  
ALL PROGRAMMABLE

Select an edition to continue installation. You will be able to customize the content in the next page.

☒ Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.

☐ Vivado HL Design Edition

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.


☐ Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

☐ Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

Vivado HL WebPACK

XILINX  
ALL PROGRAMMABLE

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.

Design Tools

☐ Vivado Design Suite

☒ Software Development Kit (SDK)

☒ DocNav

Devices

☐ Production Devices

☒ SoCs

☐ 7 Series ([limited support](#))

☐ UltraScale ([limited support](#))

☐ UltraScale+ ([limited support](#))

☐ Engineering Sample Devices

☐ Kintex UltraScale+ ES

☐ Virtex UltraScale+ ES

☐ Zynq UltraScale+ MPSoC ES

☐ Zynq UltraScale+ RFSoc ES

Installation Options

☐ NOTE: Cable Drivers are not installed on Linux. Please follow the instructions in UG973 to install Linux cable drivers

☒ Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)

☒ Enable WebTalk for SDK to send usage statistics to Xilinx

# FPGA 환경설정 (Xilinx) 3

## Select Destination Directory

Choose installation options such as location and shortcuts.

### Installation Options

Select the installation directory

/home/hyunwoopark

...

### Installation location(s)

/home/hyunwoopark/Vivado/2017.1

/home/hyunwoopark/Vivado\_HLS/2017.1

/home/hyunwoopark/SDK/2017.1

/home/hyunwoopark/DocNav

### Disk Space Required

|                       |           |
|-----------------------|-----------|
| Download Size:        | NA        |
| Disk Space Required:  | 23.98 GB  |
| Disk Space Available: | 224.36 GB |

### Select shortcut and file association options

☒ Create program group entries

Xilinx Design Tools

☒ Create \_desktop shortcuts

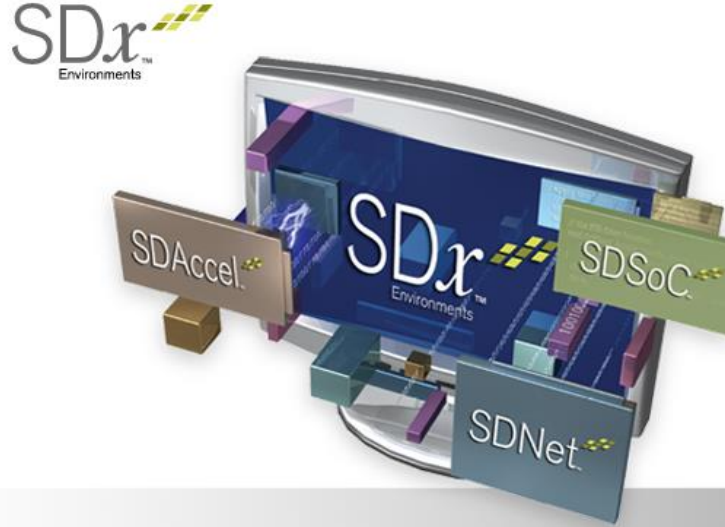
## Installation Progress

Installing files, 0% completed.

Final Processing...

### SDx Family of Development Environments

for Systems and Software Engineers

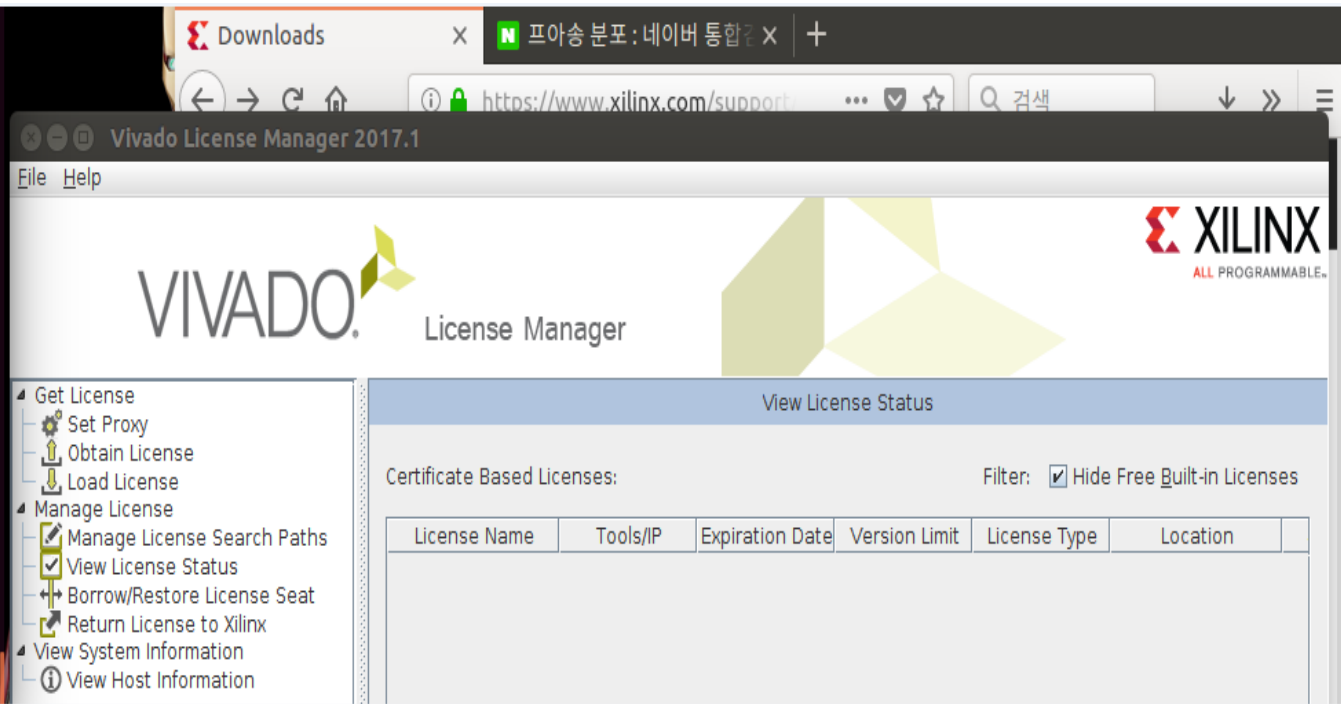


The graphic shows a central monitor displaying the SDx Environments logo. Surrounding the monitor are several floating rectangular blocks, each representing a different development environment: SDAccel (brown), SDSoC (green), SDNet (blue), and SDx Environments (blue). The blocks are arranged in a cluster, suggesting a family of tools.

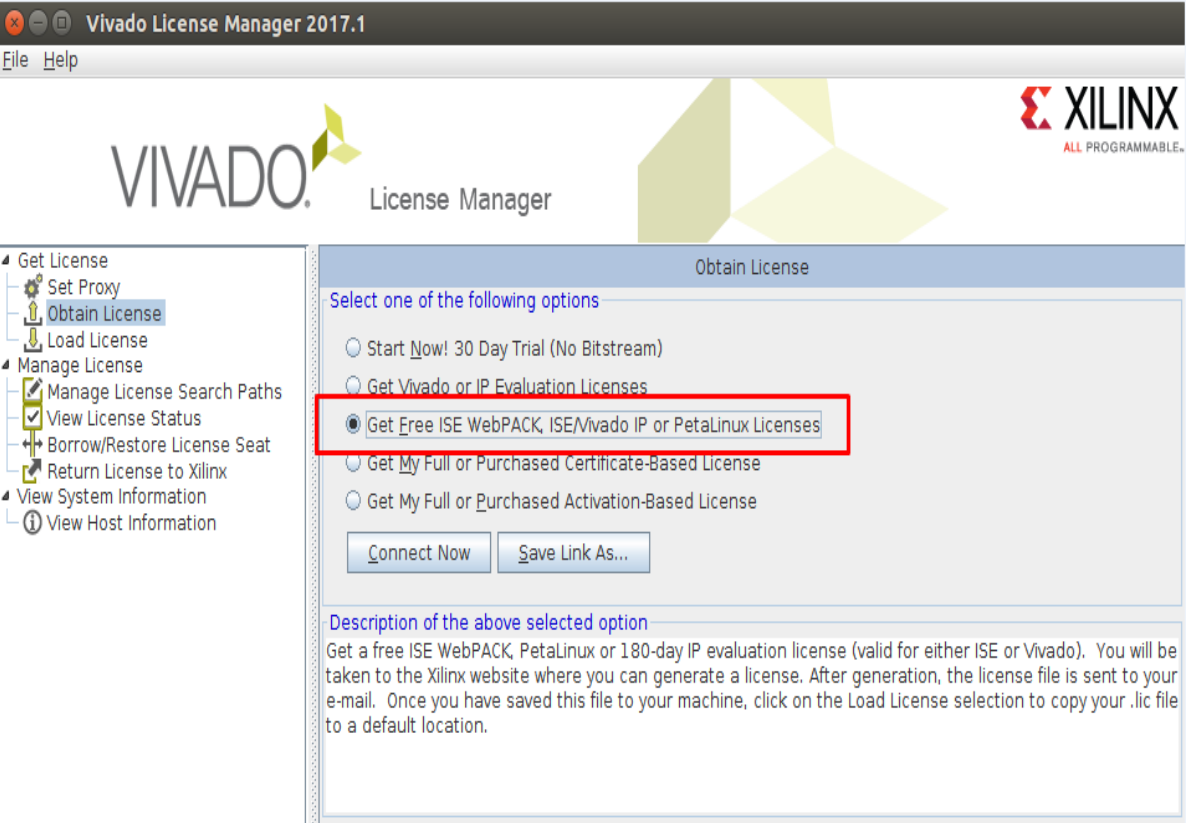


# FPGA 환경설정 (Xilinx) 4

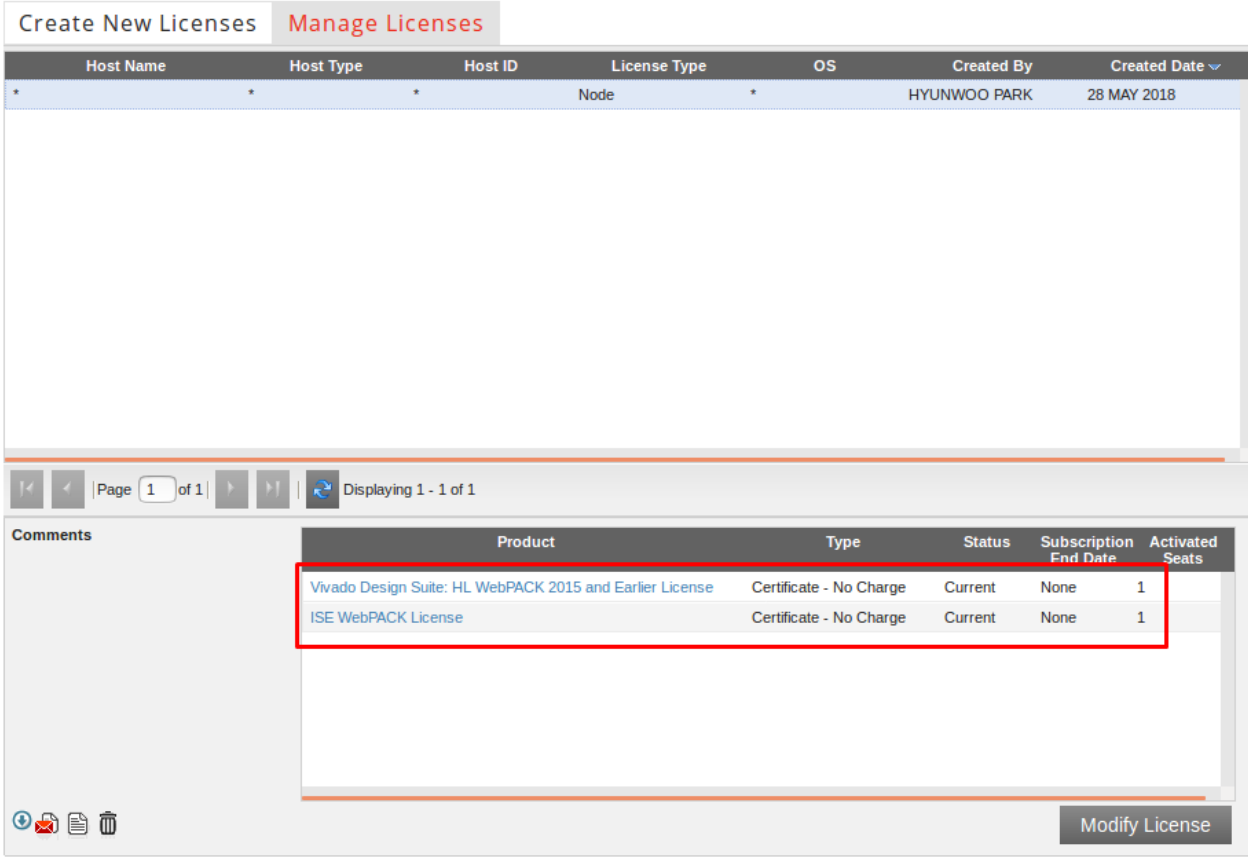
```
hyunwoopark@hyunwoopark-P65-P67SG:~$ ls
DocNav          cscope.files  math           문서
Firefox_wallpaper.png cscope.out    mkcscope.sh   바탕화면
Homework        data_structure second_test    비디오
Release.key     examples.desktop system_programming 사진
SDK             first_test    xic           음악
Vivado          hw            xilinx_vivado 템플릿
Vivado_HLS      kernel        공개
arm_asm         kernel.tar.gz 다운로드
hyunwoopark@hyunwoopark-P65-P67SG:~$ cd Vivado
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado$ ls
2017.1
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado$ cd 2017.1/
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1$ ls
bin doc fonts layouts reportSpecs settings64.csh strategies
data examples ids_lite lib scripts settings64.sh tps
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1$ cd bin
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1/bin$ ls
hw_server sdx_server updatemem wbtcv xlicsrvmgr xsim
hw_serverpv setupEnv.sh vcse_server xar xlictsinit xvc_pcie
loader svf_utility vivado xelab xsc xvhdl
rdiArgs.sh unwrapped vlm xlicclientmgr xsdb xvlog
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1/bin$ ./vlm
```



# FPGA 환경설정 (Xilinx) 5



## Product Licensing



# FPGA 환경설정 (Xilinx) 6



# FPGA 환경설정 (Xilinx) 7

```
hyunwoopark@hyunwoopark-P65-P67SG: ~/Vivado/2017.1/bin
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1$ ls
bin  doc  fonts  layouts  reportSpecs  settings64.csh  strategies
data  examples  ids_lite  lib  scripts  settings64.sh  tps
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1$ cd bin
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1/bin$ ls
hw_server  sdx_server  updatemem  wbtcv  xlicsrvmgr  xsin
hw_serverpv  setupEnv.sh  vcse_server  xar  xlictsint  xvc_pcie
loader  svf_utility  vivado  xelab  xsc  xvhdl
rdiArgs.sh  unwrapped  vlm  xlicclientmgr  xsdb  xvlog
hyunwoopark@hyunwoopark-P65-P67SG:~/Vivado/2017.1/bin$ ./vivado
CRITICAL WARNING: [Common 17-183] Failed to open handle vivado.jou. Please check
access permission of directory '/home/hyunwoopark/Vivado/2017.1/bin'. You should
restart the application from a writable working directory.
CRITICAL WARNING: [Common 17-183] Failed to open handle vivado.log. Please check
access permission of directory '/home/hyunwoopark/Vivado/2017.1/bin'. You should
restart the application from a writable working directory.

***** Vivado v2017.1 (64-bit)
**** SW Build 1846317 on Fri Apr 14 18:54:47 MDT 2017
**** IP Build 1846188 on Fri Apr 14 20:52:08 MDT 2017
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

start_gui
```

