

TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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1) Vivado 환경설정 1

An internal exception error

✓ Re: Vivado 2017.1 Crashed When Opening Implemented Design

Options ▾

04-26-2017 01:14 PM

There are two protobuf JAR files installed with Vivado 2017.1 which can lead to a conflict on some Linux machines. To work around the issue you can rename or remove the protobuf-java-3.1.0.jar file under <Vivado Install Folder>/lib/classes. Removing this file does not have any negative effect on Vivado, and will be fixed in Vivado 2017.2.

Don't forget to reply, kudo, and accept as solution.

진짜 이거 때문에 엄청 고생함... 리눅스 재설치... 환경설정 등등 아오...

에러 원인 : 두 개의 java 파일이 어떤 리눅스 상에서는 충돌이 일어나 에러를 만든다 함.
그래서 lib/classes 밑으로 가서 중복된 거 하나 지워야 됨.

1) Vivado 환경설정 2

Zybo 보드 드라이버 설치

```
hyunwoopark@hyunwoopark-P65-P67SG:~/xilinx/Vivado/2017.1/data/xicom$ cd cable_drivers/lin64/install_script/install_drivers/
hyunwoopark@hyunwoopark-P65-P67SG:~/xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers$ sudo ./install_drivers
[sudo] password for hyunwoopark:
INFO: Installing cable drivers.
INFO: Script name = ./install_drivers
INFO: HostName = hyunwoopark-P65-P67SG
INFO: Current working dir = /home/hyunwoopark/xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers
INFO: Kernel version = 4.13.0-36-generic.
INFO: Arch = x86_64.
Successfully installed Digilent Cable Drivers
--File /etc/udev/rules.d/52-xilinx-ftdi-usb.rules does not exist.
--File version of /etc/udev/rules.d/52-xilinx-ftdi-usb.rules = 0000.
--Updating rules file.
--File /etc/udev/rules.d/52-xilinx-pcusb.rules does not exist.
--File version of /etc/udev/rules.d/52-xilinx-pcusb.rules = 0000.
--Updating rules file.

INFO: Digilent Return code = 0
INFO: Xilinx Return code = 0
INFO: Xilinx FTDI Return code = 0
INFO: Return code = 0
INFO: Driver installation successful.
CRITICAL WARNING: Cable(s) on the system must be unplugged then plugged back in order for the driver scripts to update the cables.
hyunwoopark@hyunwoopark-P65-P67SG:~/xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers$
```

드라이버 설치가 제대로 안될 수 있기 때문에 드라이버 설치 권장.

1) Vivado 환경설정 3

Vivado 이미지 파일 만들기

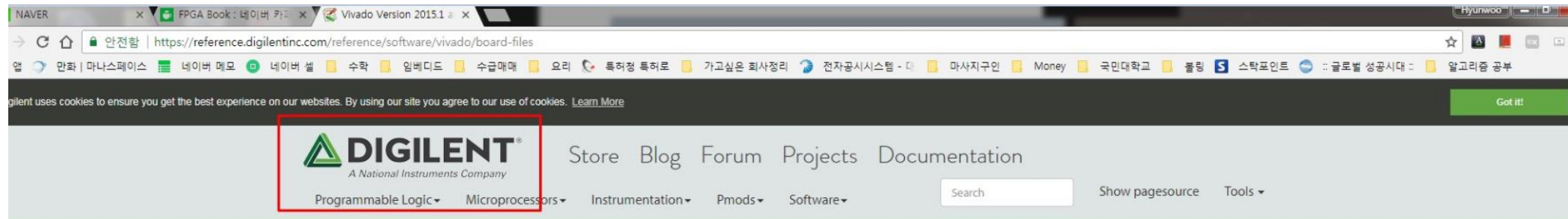
```
1 #! /usr/bin/env xdg-open
2 [Desktop Entry]
3 Name=Xilinx Vivado
4 Type=Application
5 Exec=/home/hyunwoopark/xilinx/Vivado/2017.1/bin/vivado
6 Terminal=false
7 Icon=/home/hyunwoopark/xilinx/Vivado/2017.1/common/icons/CS1056_Vivado_HSL_I
  con_64x64.ico
8 Comment=Xilinx Vivado Program
9 NoDisplay=false
10 Categories=Development;IDE;
11 Name[en]=Vivado
```

Icon 위치 바꿔야 됨.

1) Vivado 환경설정 4

FPGA 회로 프로그래밍 하려면 보드 파일 추가 설치 해야 함. (full version 제외)

https://reference.digilentinc.com/_media/zybo:zybo_rm.pdf (GPIO 핀 확인)



You are here: [Digilent Documentation](#) / [Reference](#) / [Software](#) / [Vivado](#) / Vivado Version 2015.1 and Later Board File Installation (Legacy)

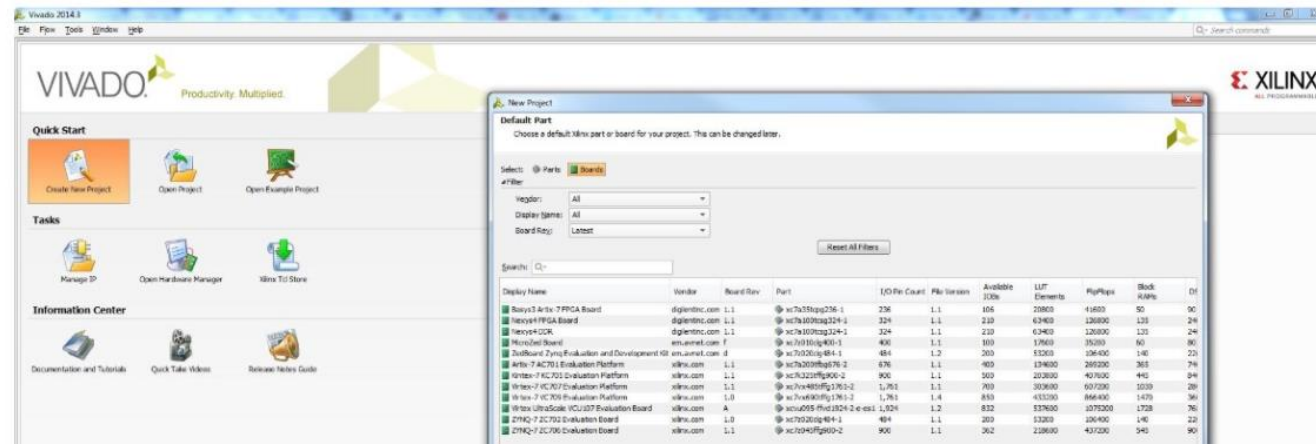
Vivado Version 2015.1 and Later Board File Installation (Legacy)

[Table of Contents](#)

Board Files: [Download](#)

Description

This guide will help you obtain Vivado Board Files for the Nexys 4, Nexys 4 DDR, Basys 3, Arty, Nexys Video, Zedboard and Zybo FPGA Boards.



2) GPIO 프로그래밍 VHDL 1

1

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select:

Parts

Boards

Filter

Product category:

All

Speed grade:

All

Family:

All

Temp grade:

All

Package:

All

Reset All Filters

Search:

xc7z010clg400-1

(1 match)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transc
<div>xc7z010clg400-1</div>	400	100	17600	35200	60	0	80	0	0

< Back

Next >

Finish

Cancel

2

and_gate - [j:/home/nyunwoopark/vivado_workspace/and_gate/and_gate.xpr] - Vivado 2017.1

File Edit Flow Tools Window Layout View Help

Q: Quick Access

Ready

Default Layout

Flow Navigator

PROJECT MANAGER - and_gate

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Open Hardware Manager

Sources

Design Sources

Constraints

Simulation Sources

sim_1

Hierarchy

Libraries

Properties

Select an object to view

Project Summary

Settings Edit

Project name: and_gate

Project location: /home/nyunwoopark/vivado_workspace/and_gate

Product family: Zynq-7000

Not started

No errors or warnings

xc7z010clg400-1

Vivado Implementation Defaults

total compile: None

Run Implementation to see timing results

Run Implementation to see power results

Add Sources

VIVADO HLS Editions

Add Sources

This guides you through the process of adding and creating sources for your project

Add or create constraints

Add or create design sources

Add or create simulation sources

XILINX ALL PROGRAMMABLE

< Back

Next >

Finish

Cancel

Tcl Console

Messages

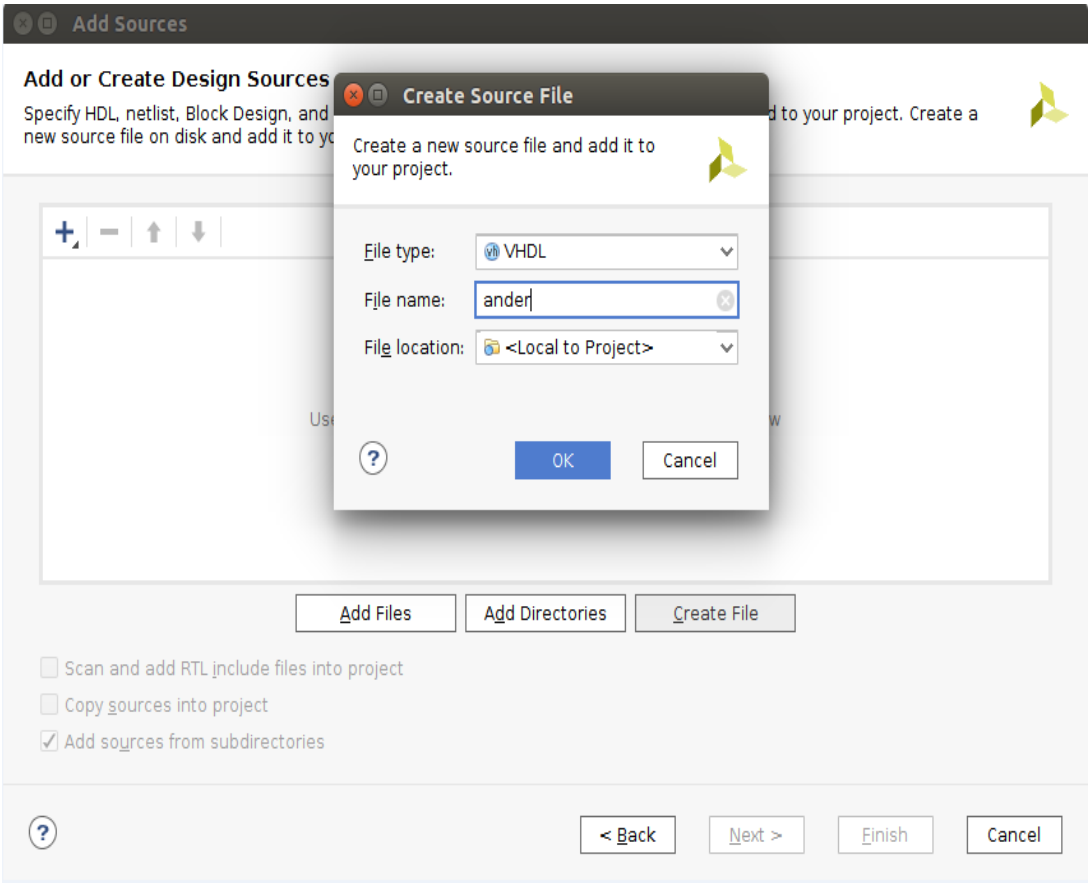
Q: Quick Access

100%

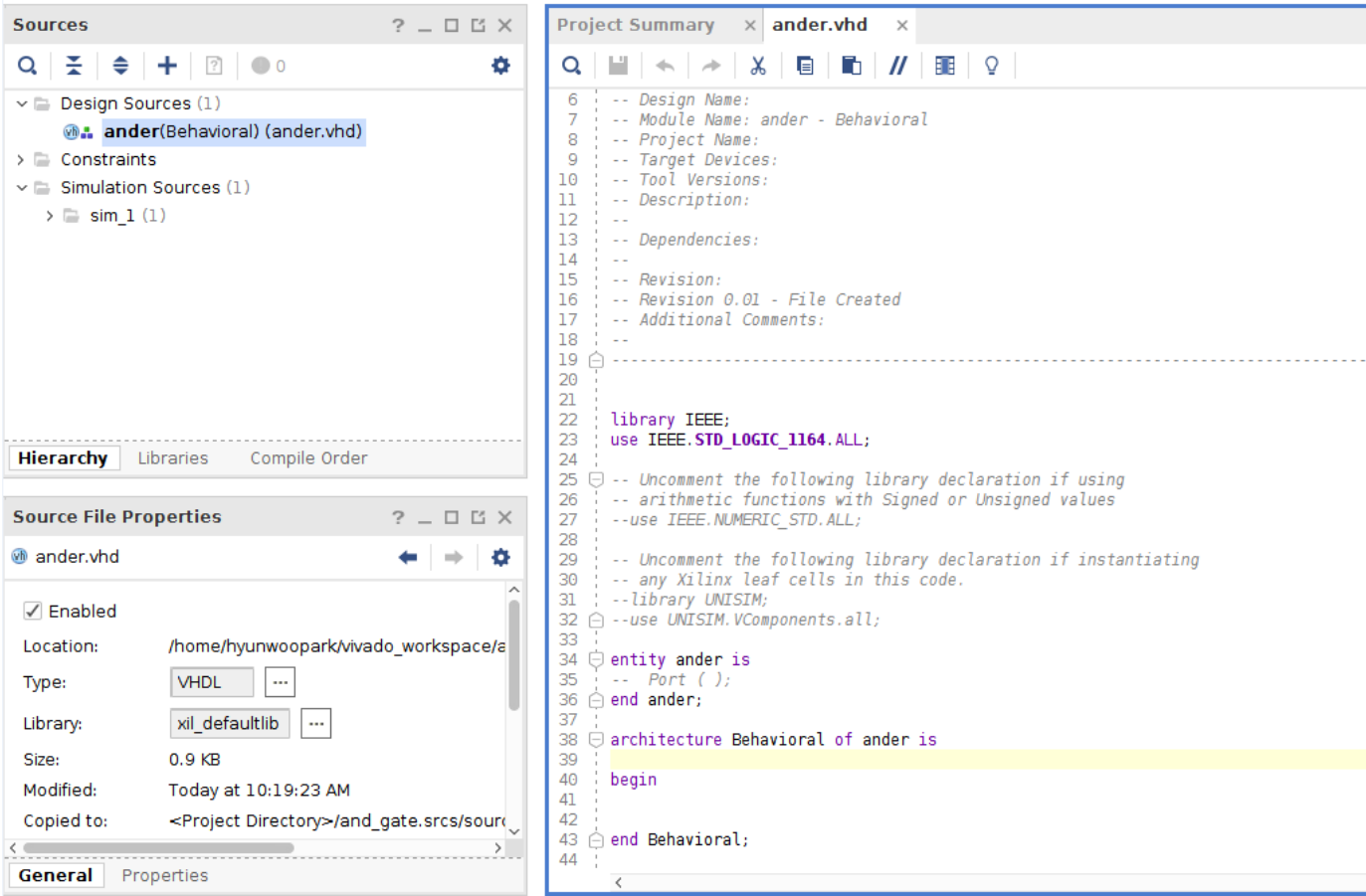
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Ho
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7z010clg400-1	
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7z010clg400-1	

2) GPIO 프로그래밍 VHDL 2

3



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2) GPIO 프로그래밍 VHDL 3

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ELABORATED DESIGN * - xc7z010clg400-1 (active)

Sources

Netlist

Device Constraints

Design Sources (1)

ander(Behavioral) (ander.vhd)

Constraints

constrs_1

Simulation Sources (1)

sim_1 (1)

ander(Behavioral) (ander.vhd)

Hierarchy

Libraries

Compile Order

Constraint Set Properti

Clock Regions

constrs_1

Default directory: /home/hyunwoopark/vivado_workspace

File count: 0

Format: XDC

Target constraint file:

☒ Active

General

Properties

Package

Device

Schematic

ander.vhd

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

T

U

V

W

Y

Tcl Console

Messages

Log

Reports

Design Runs

Find Results

Package Pins

I/O Ports

Name

Direction

Neg Diff Pair

Package Pin

Fixed

Bank

I/O Std

Vcco

Vref

Drive Strength

Slew Type

Pull Type

Off-Chip Termination

IN_TERM

▼ All ports (3)

▼ Scalar ports (3)

a

IN

G15

✓

35

LVC MOS33*

3.300

NONE

NONE

b

IN

P15

✓

34

LVC MOS33*

3.300

NONE

NONE

res

OUT

M14

✓

35

LVC MOS33*

3.300

12

SLOW

NONE

FP_VTT_50

2) GPIO 프로그래밍 VHDL 4

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The screenshot displays the Xilinx Vivado IDE interface. On the left, the **Flow Navigator** pane shows the project workflow. The **IMPLEMENTATION** section is expanded, and the **Run Implementation** button is highlighted with a red box. Below it, the **Open Implemented Design** option is also visible. The **PROGRAM AND DEBUG** section is also expanded, with the **Generate Bitstream** button highlighted with a red box.

The main workspace is divided into several panes. The **HARDWARE MANAGER** pane at the top shows the device **xc7z010_1** is programmed. The **Hardware** pane below it lists the components: **arm_dap_0** (N/A) and **xc7z010_1** (Programmed). The **Hardware Device Properties** pane for **xc7z010_1** shows details such as Name, Part, ID code, IR length, Status, Programming file, Probes file, and User chain count.

The **ander.vhd** file is open in the editor, showing the VHDL code for the **ander** entity. The code includes library declarations for **IEEE** and **UNISIM**, and defines the **ander** entity with two input ports **a** and **b**, and one output port **res**. The architecture **Behavioral** of **ander** is defined as **res <= a and b;**.

The **Tcd Console** pane at the bottom shows the output of the **refresh_hw_device** command. It displays an **INFO** message indicating that the device **xc7z010** is programmed with a design that has no supported debug core(s) in it. A **WARNING** message follows, stating that the debug hub core was not detected. The console also provides a resolution: 1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active. 2. Make sure the **BSCAN_SWITCH_USER_MASK** device property in Vivado Hardware Manager reflects the user scan chain setting in the design and refresh the device. To determine the user scan chain setting in the d, For more details on setting the scan chain property, consult the Vivado Debug and Programming User Guide (UG908).

1

2

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select:

Parts

Boards

Filter/Preview

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search: zybo (3 matches)

Display Name	Vendor	Board Rev	Part	I/O Pin C
<div><div></div> Zybo Z7-10</div>	digilentinc.com	B.2	<div></div> xc7z010clg400-1	400
<div><div></div> Zybo Z7-20</div>	digilentinc.com	B.2	<div></div> xc7z020clg400-1	400
<div><div></div> Zybo</div>	digilentinc.com	B.3	<div></div> xc7z010clg400-1	400

No Board Connectors

?

< Back

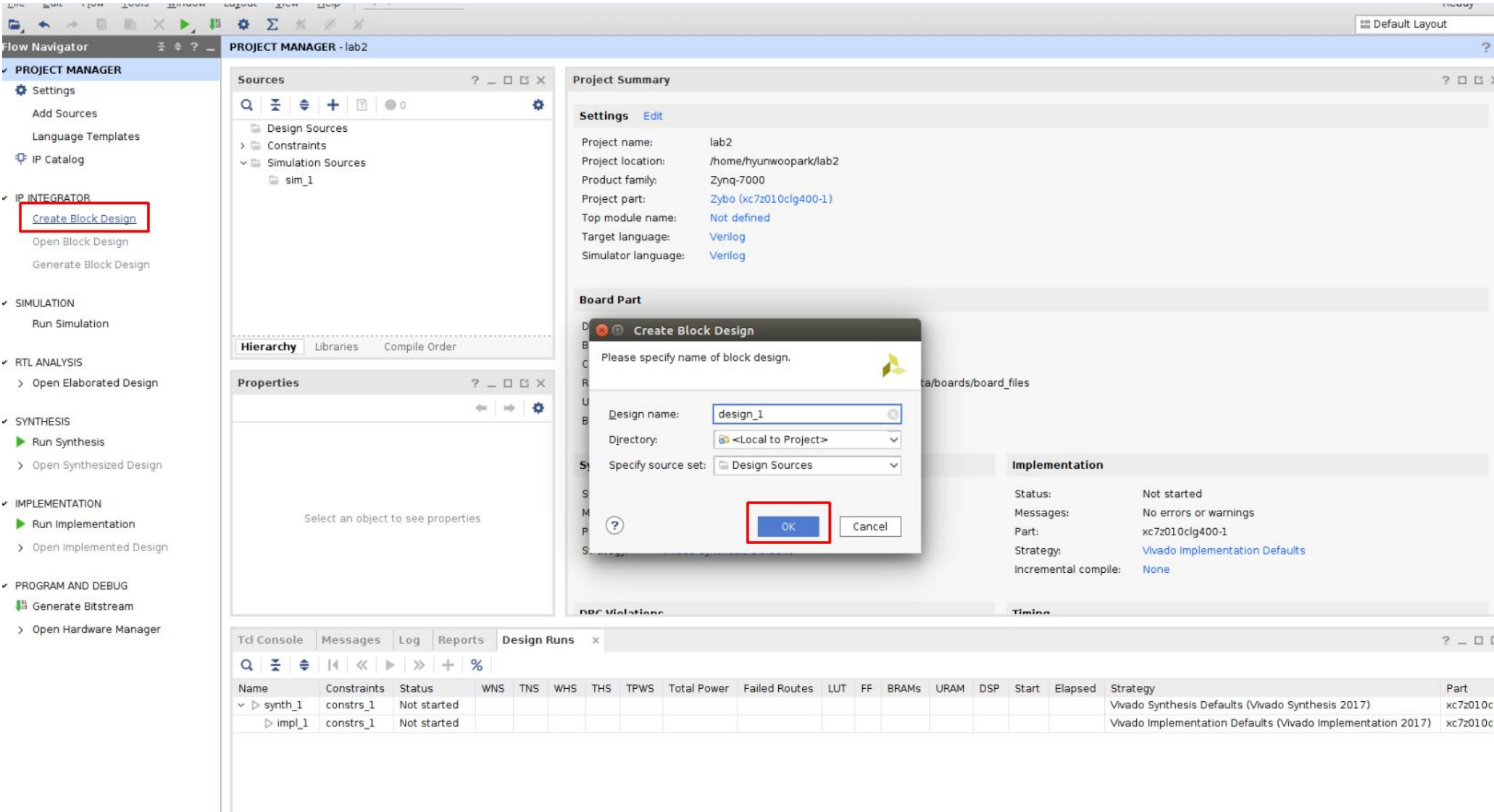
Next >

Finish

Cancel

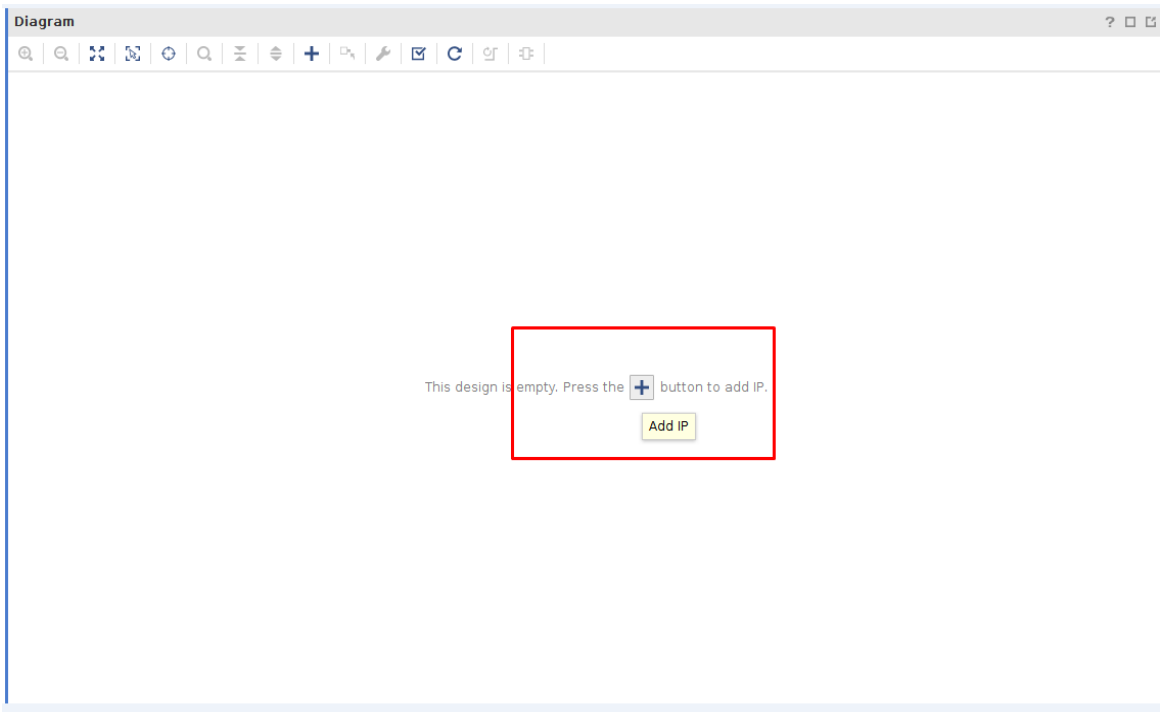
3) GPIO 회로 프로그래밍 Verilog 2

3

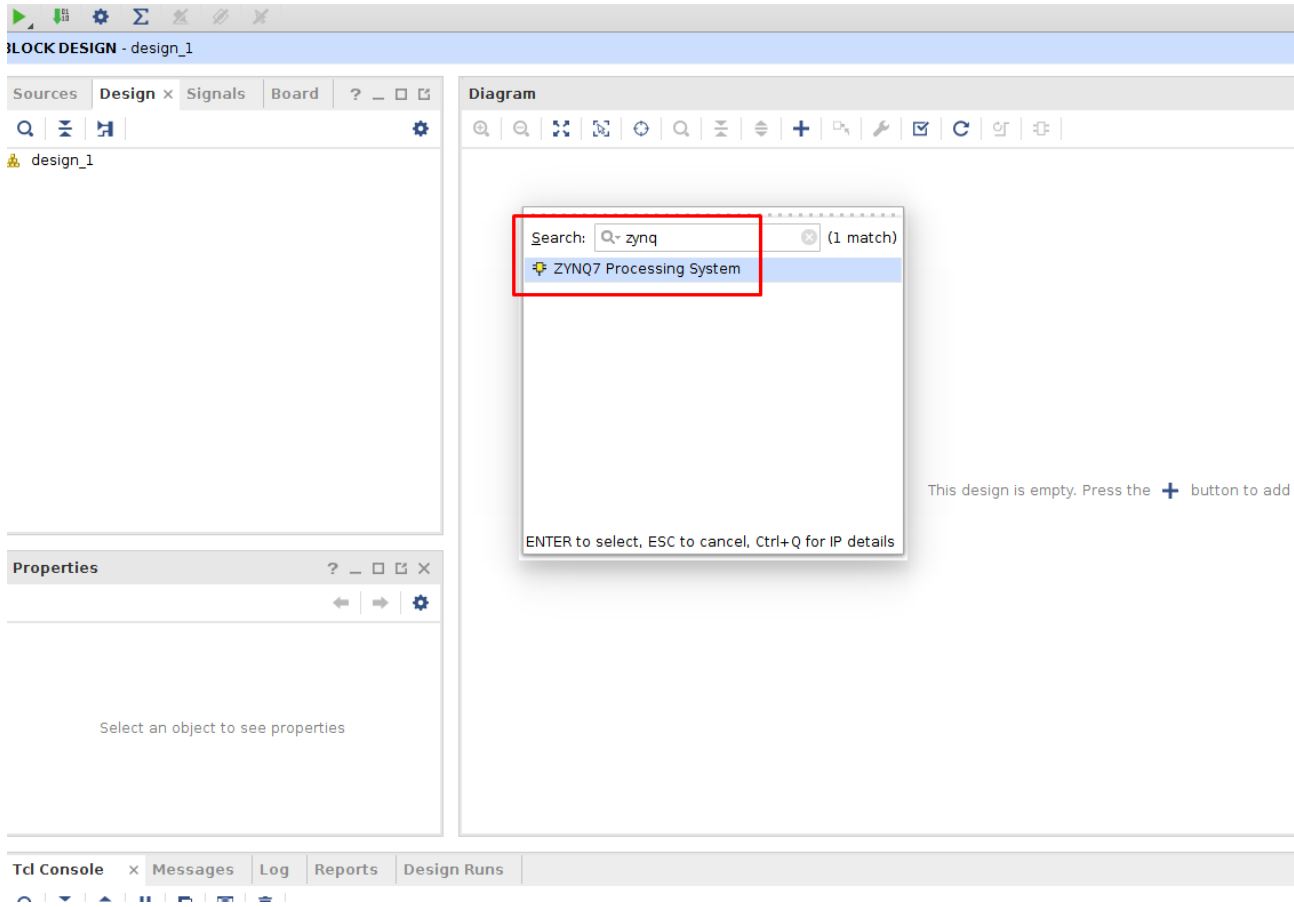


3) GPIO 회로 프로그래밍 Verilog 3

4

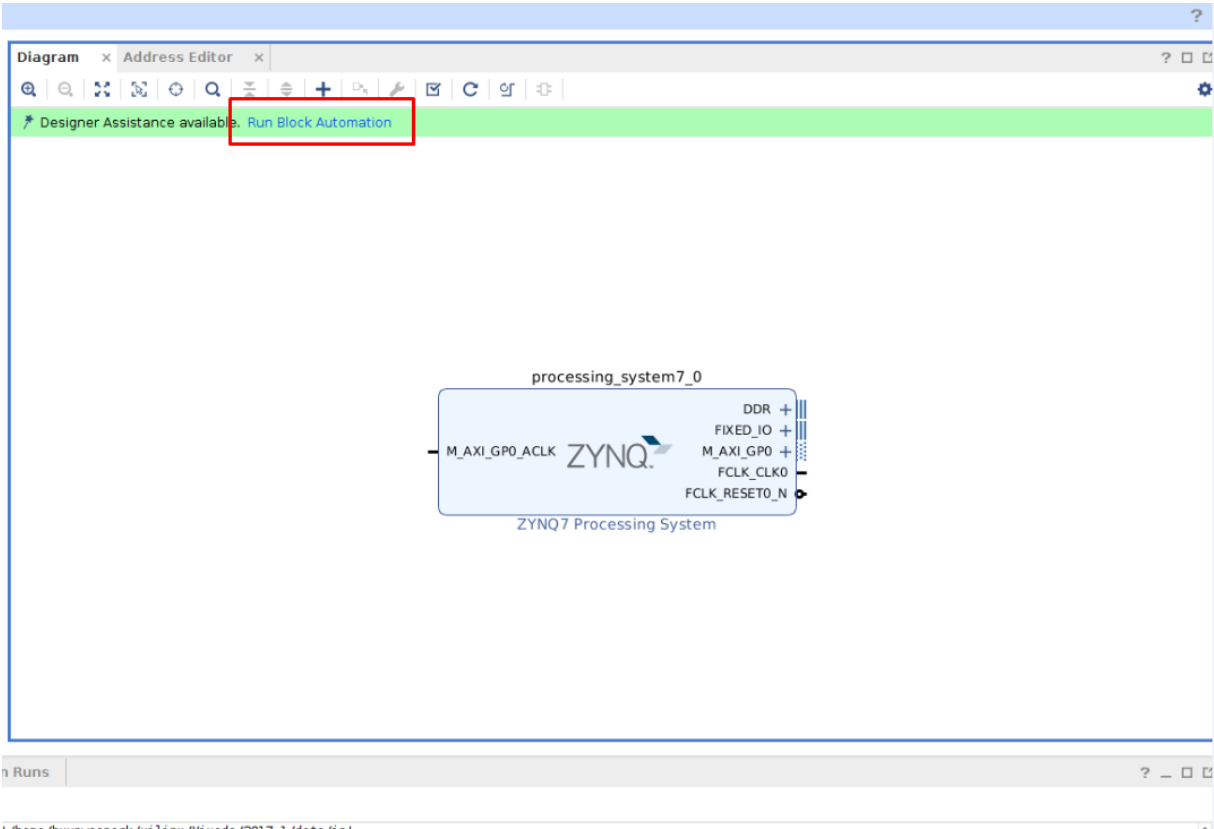


5

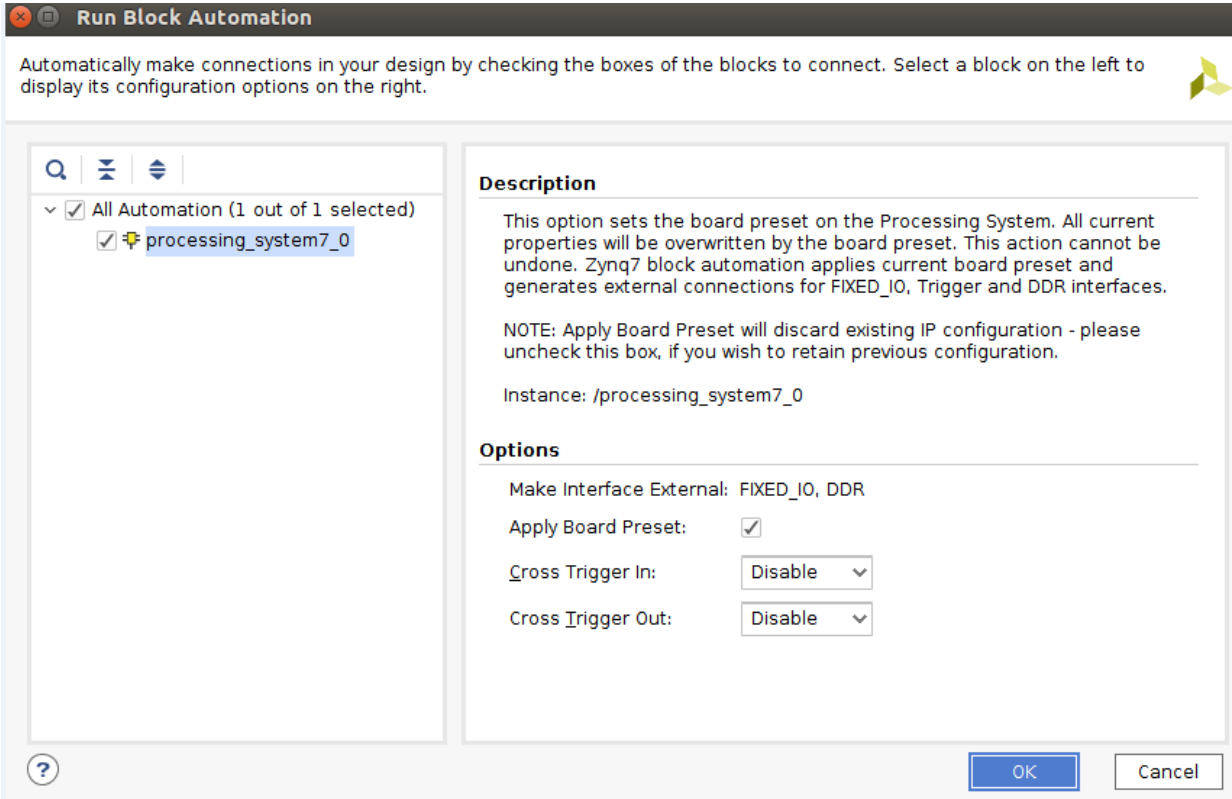


3) GPIO 회로 프로그래밍 Verilog 4

6

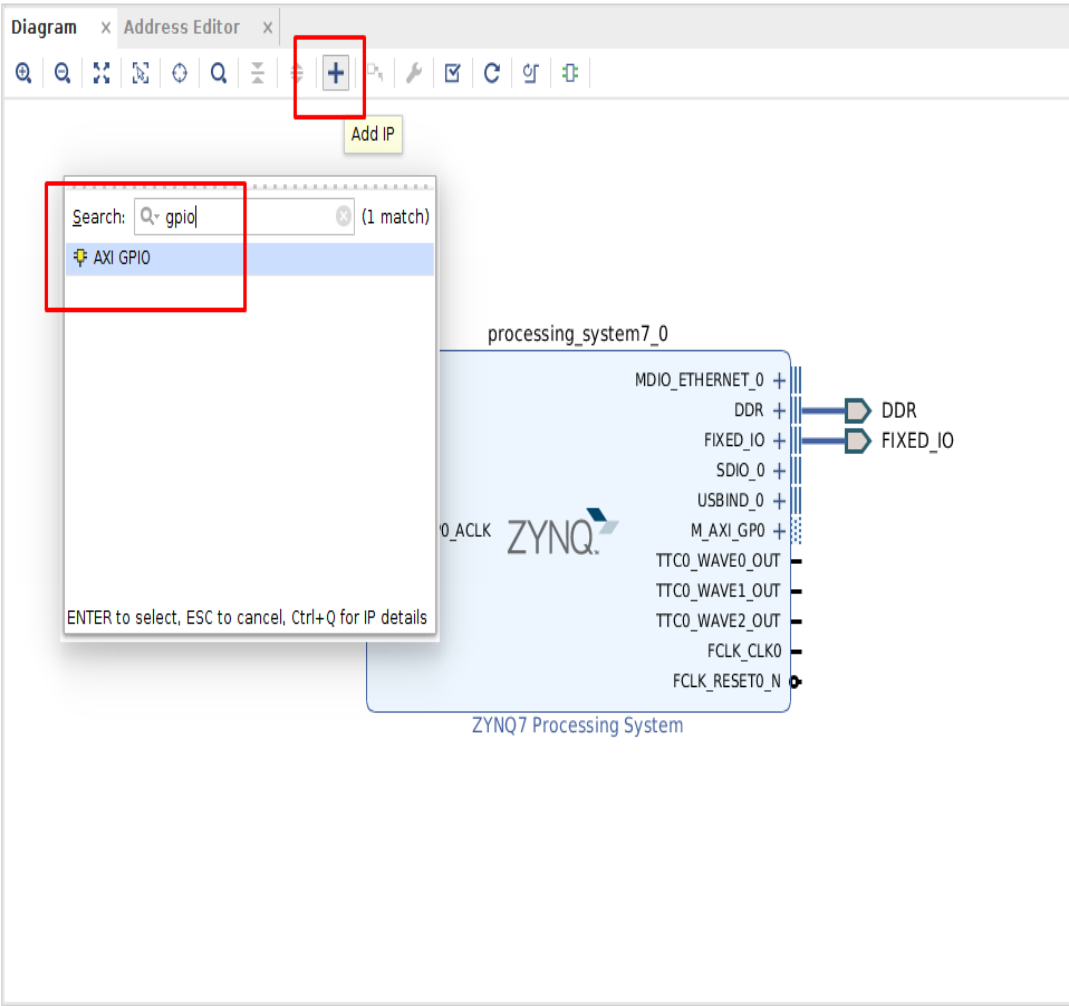


7

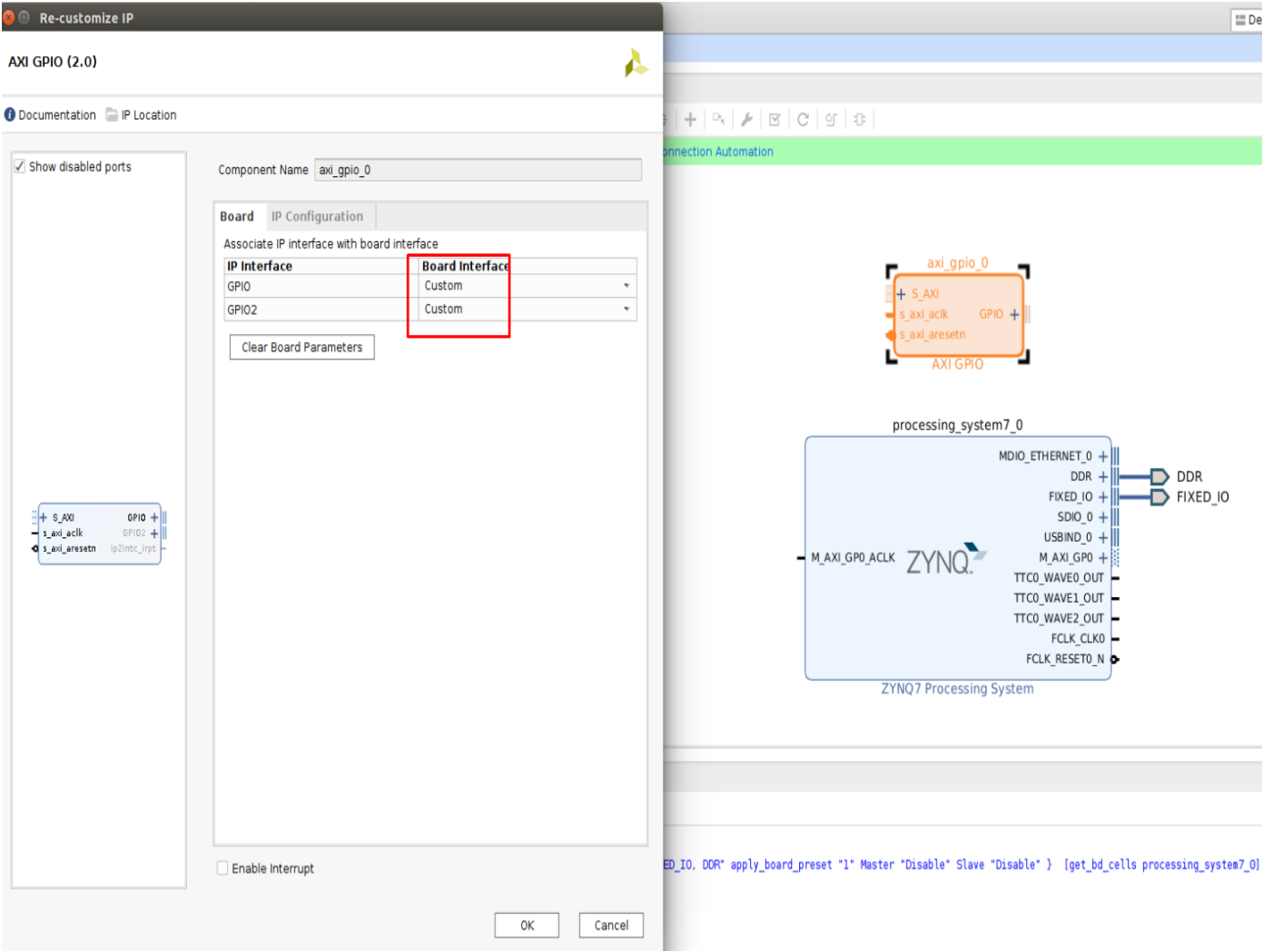


3) GPIO 회로 프로그래밍 Verilog 5

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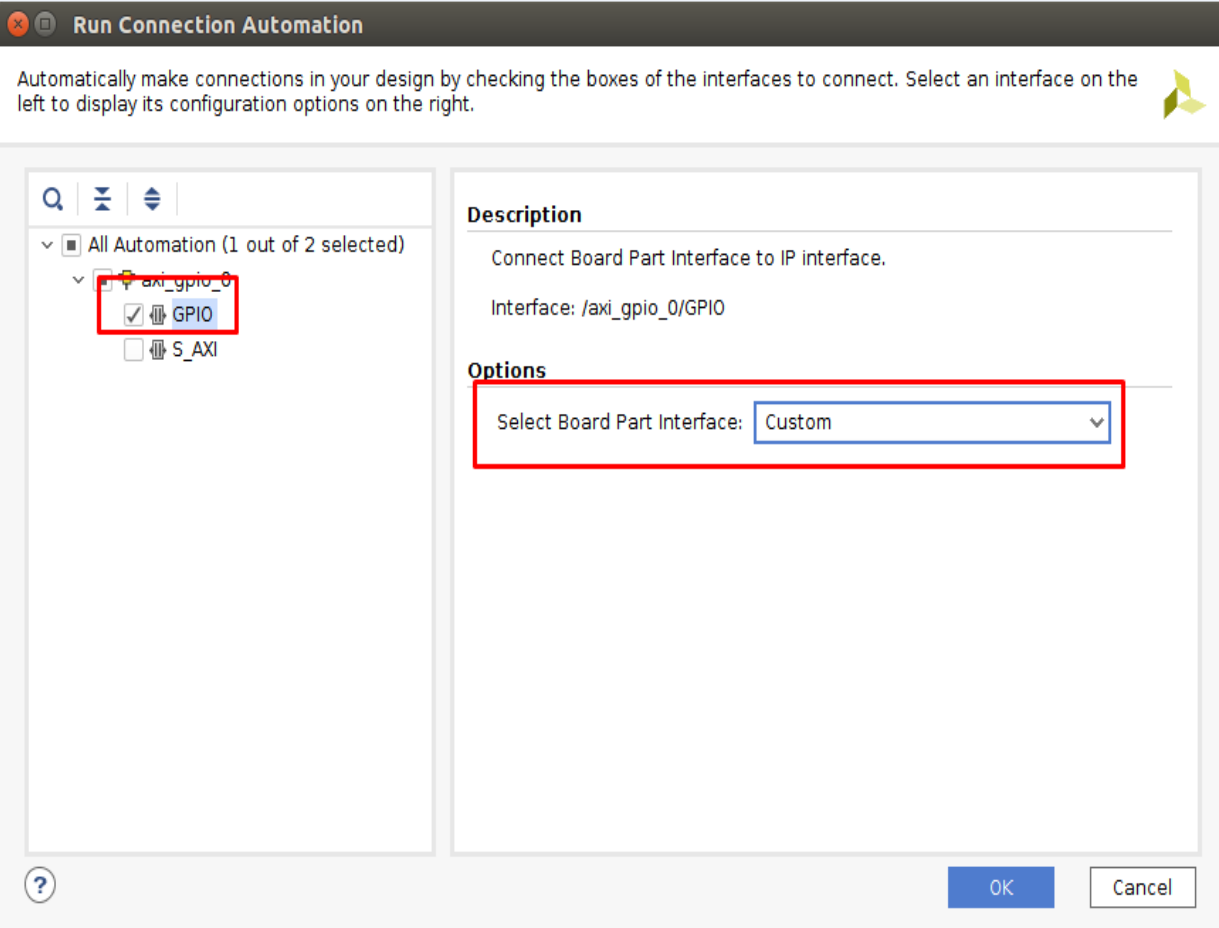


9

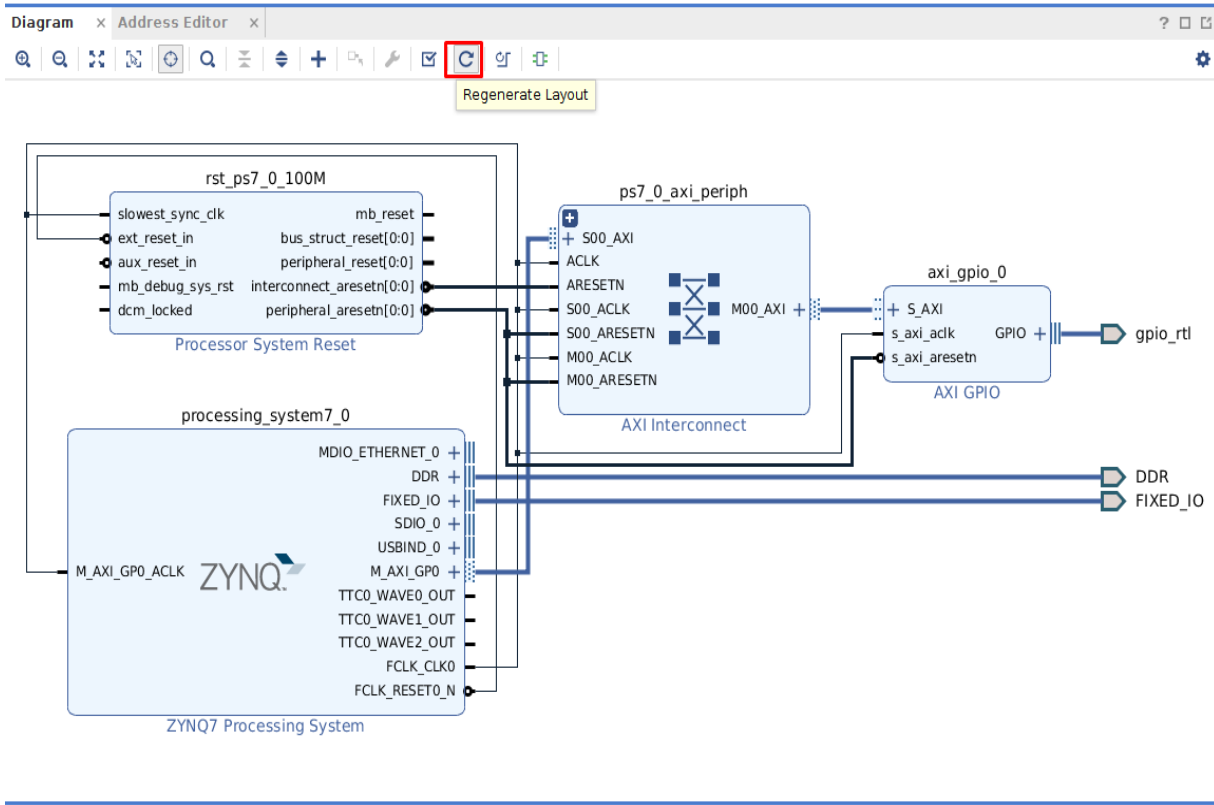


3) GPIO 회로 프로그래밍 Verilog 6

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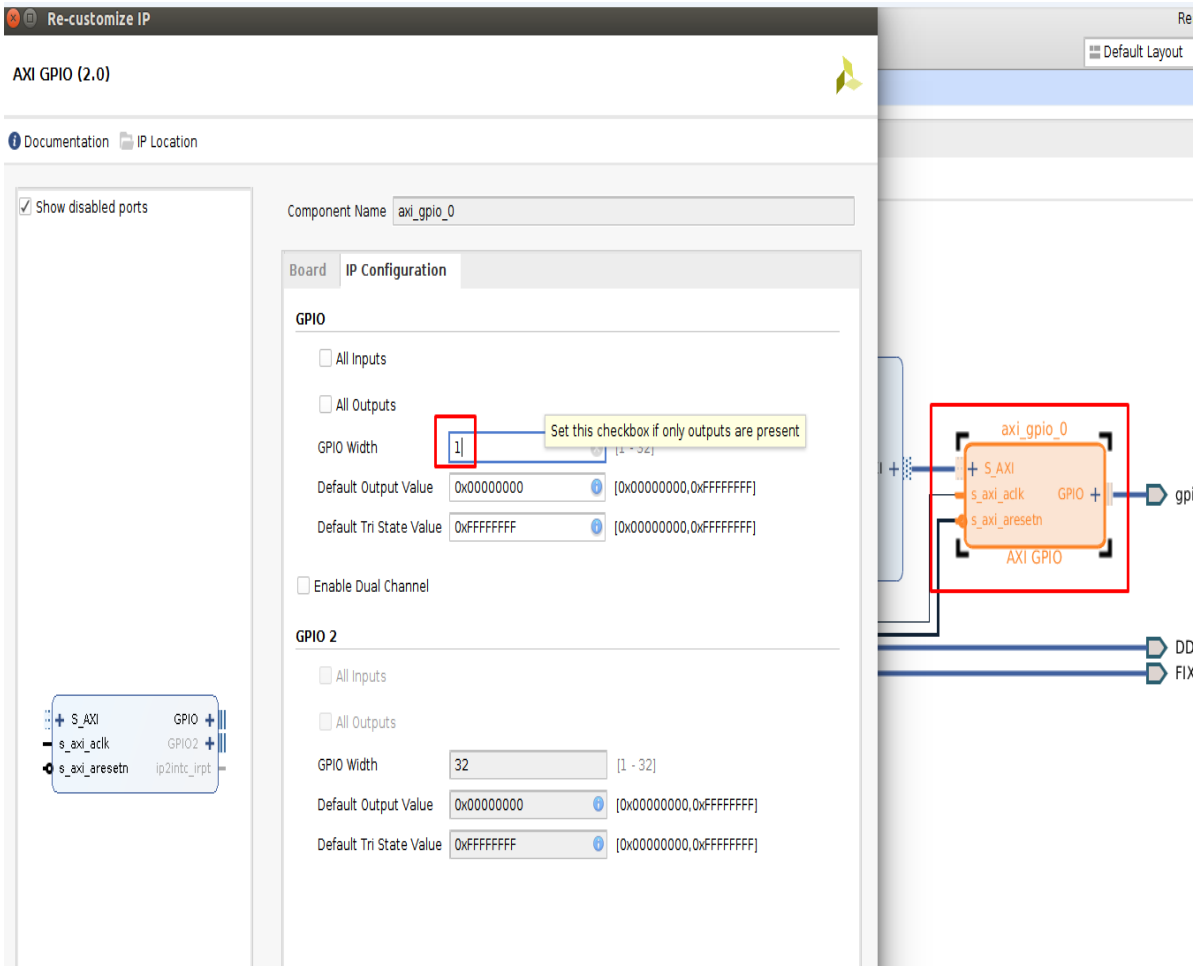


11

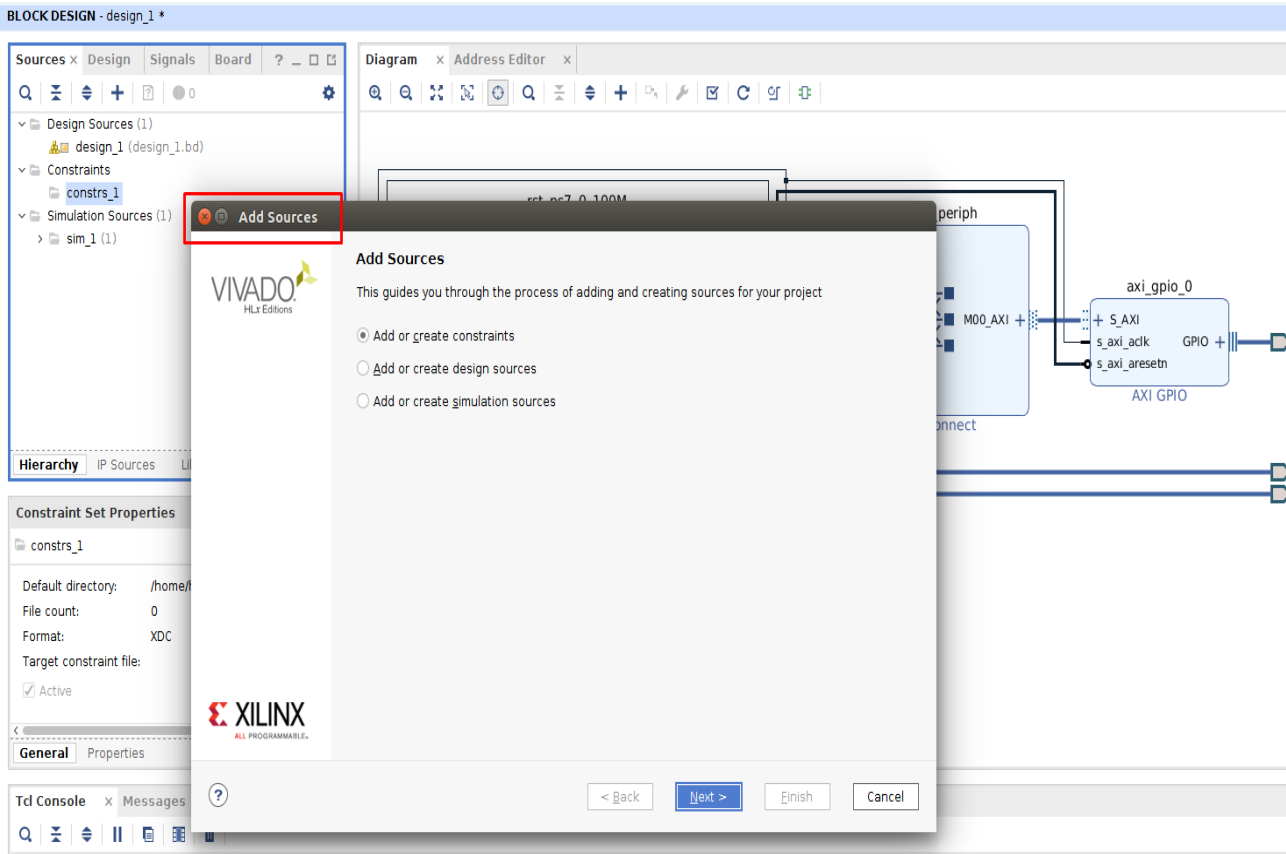


3) GPIO 회로 프로그래밍 Verilog 7

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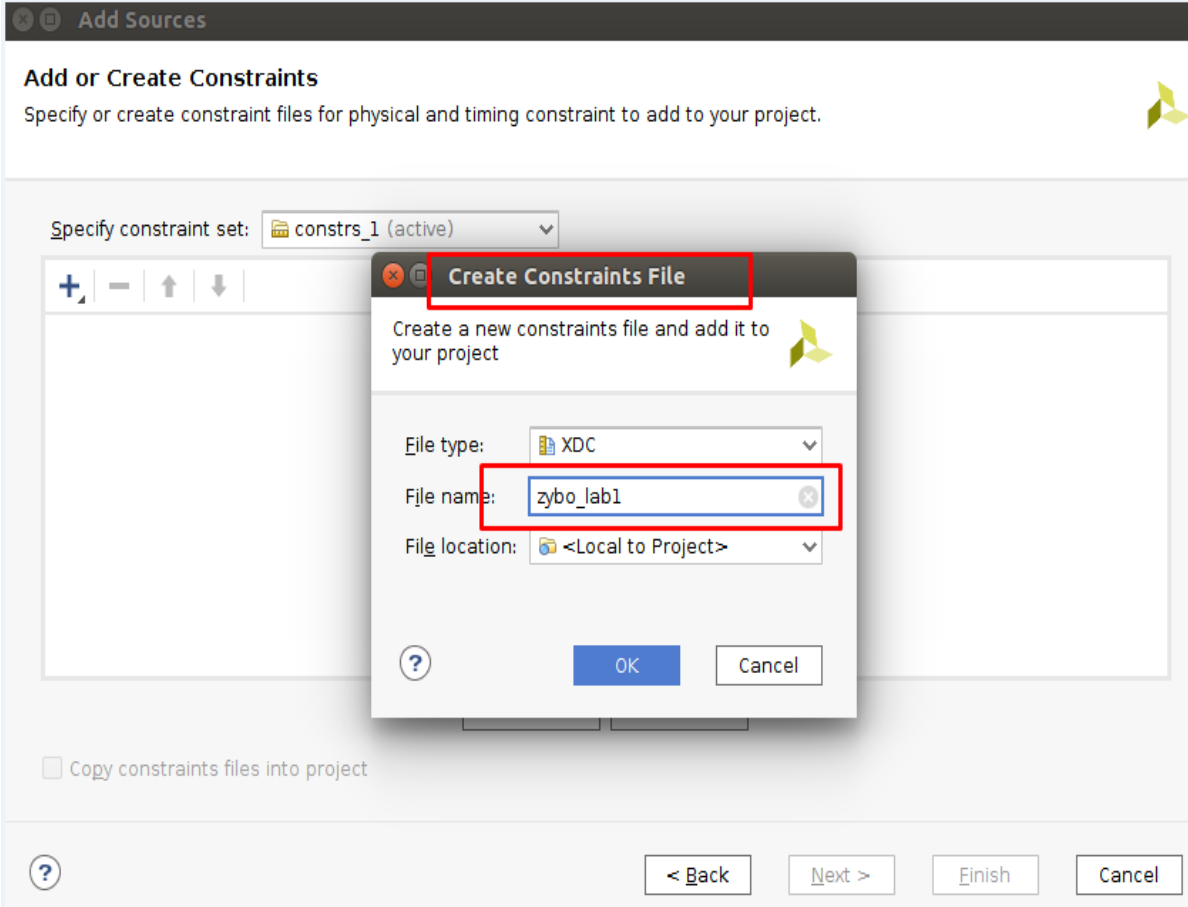


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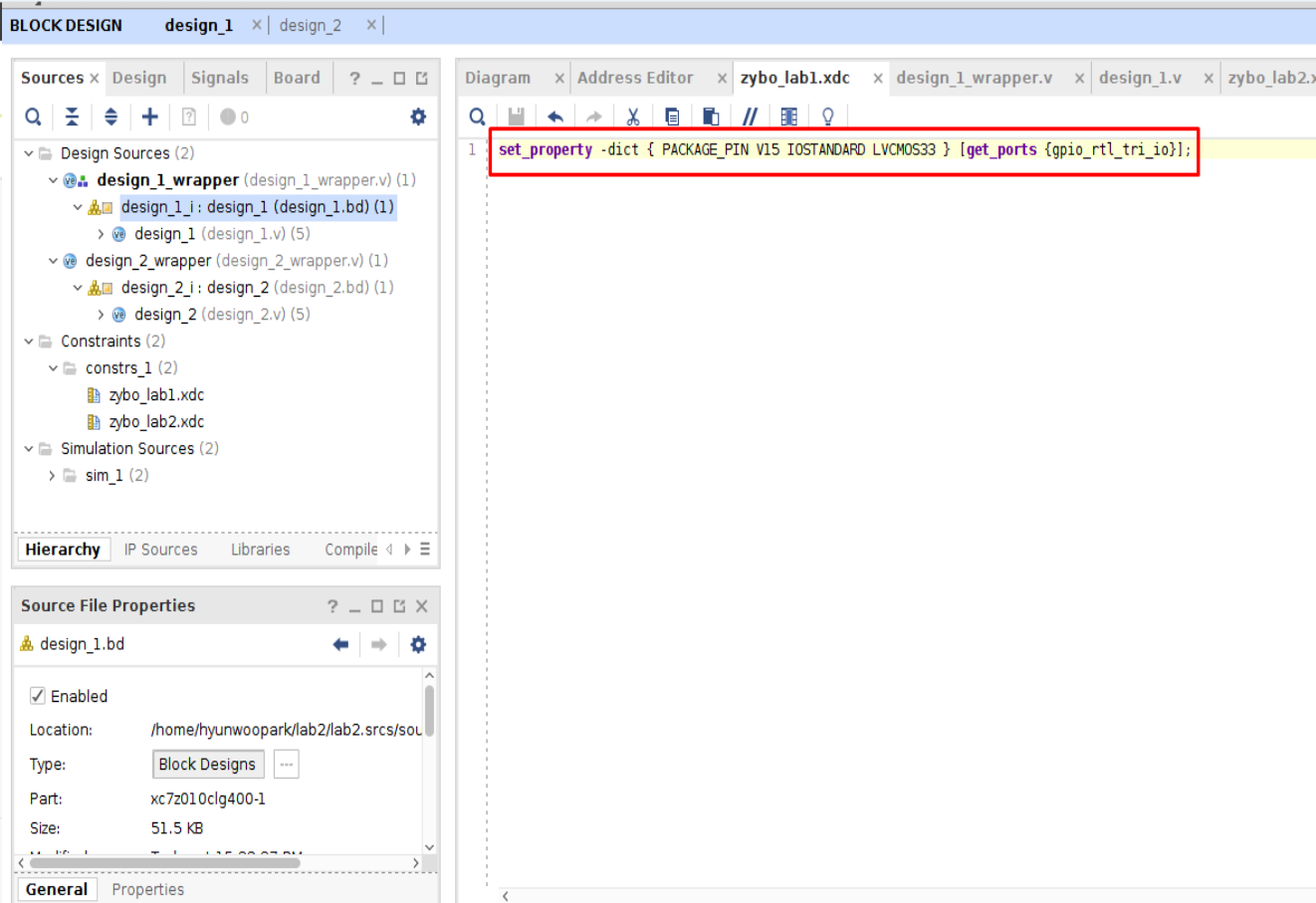


3) GPIO 회로 프로그래밍 Verilog 8

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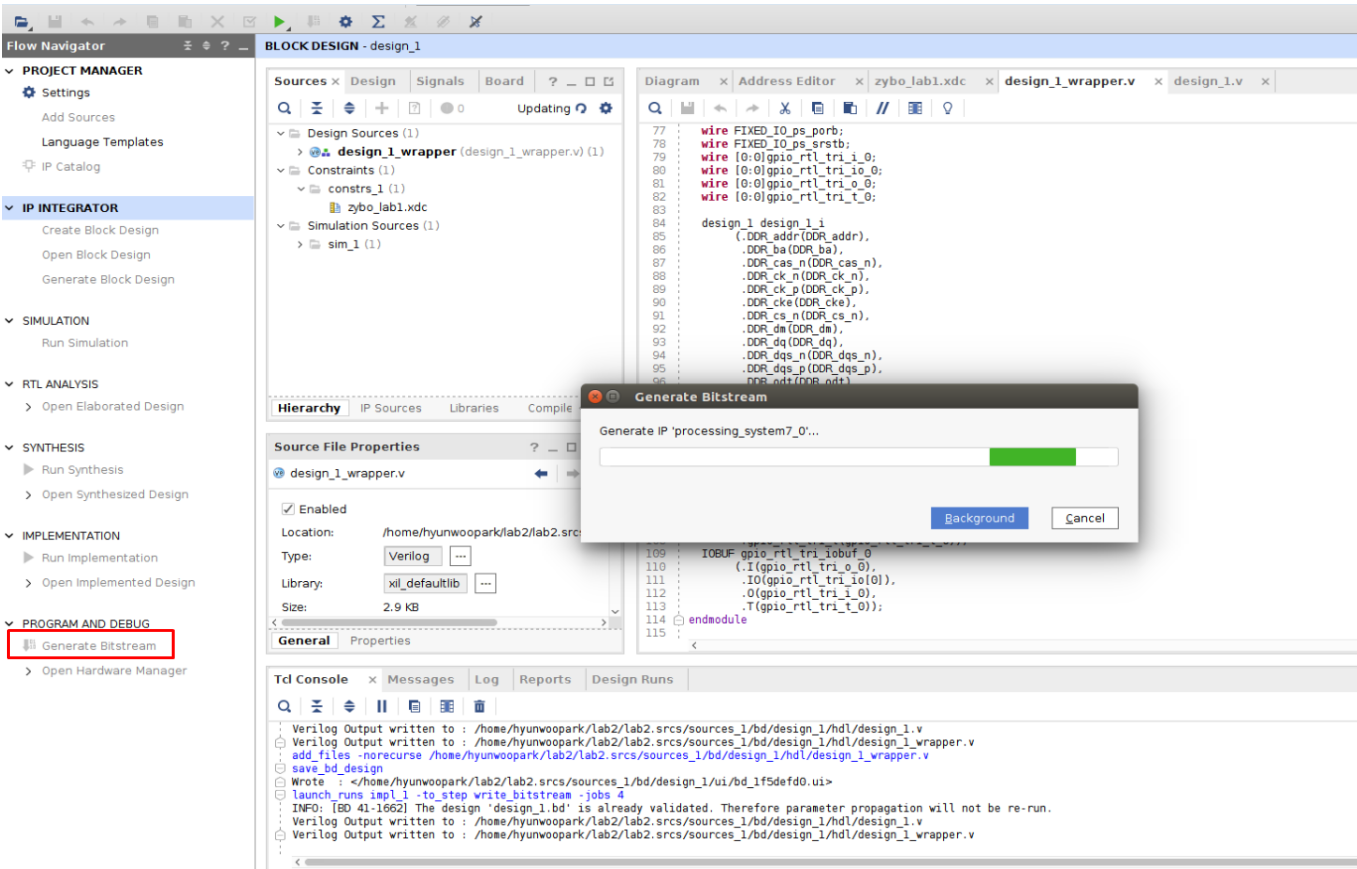
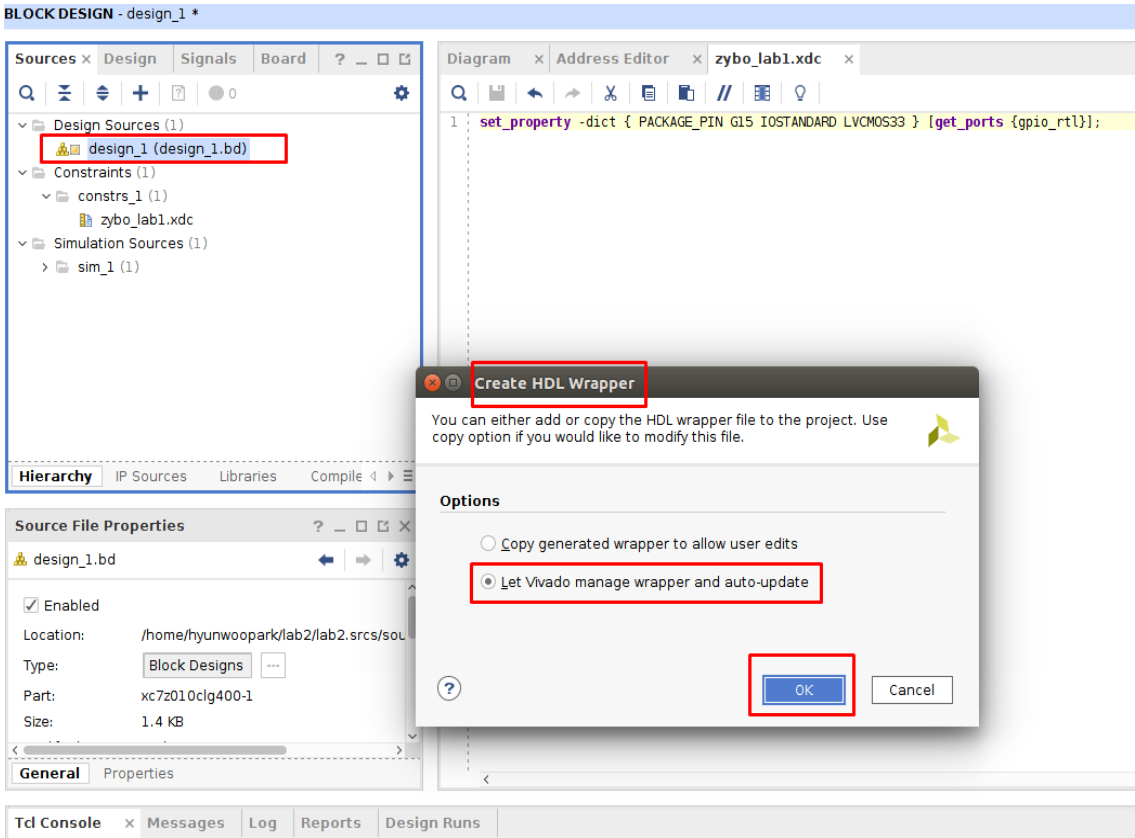
15



3) GPIO 회로 프로그래밍 Verilog 9

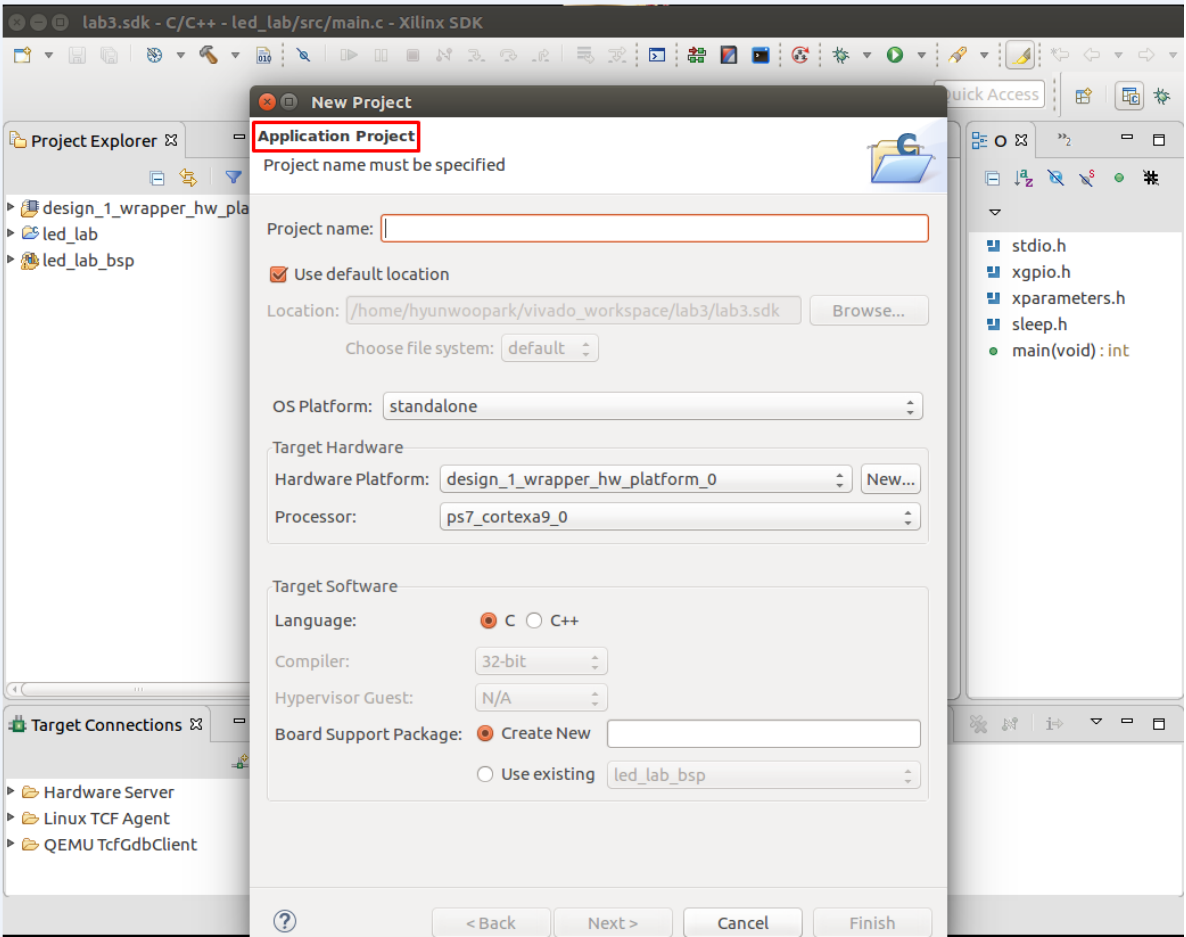
16

17

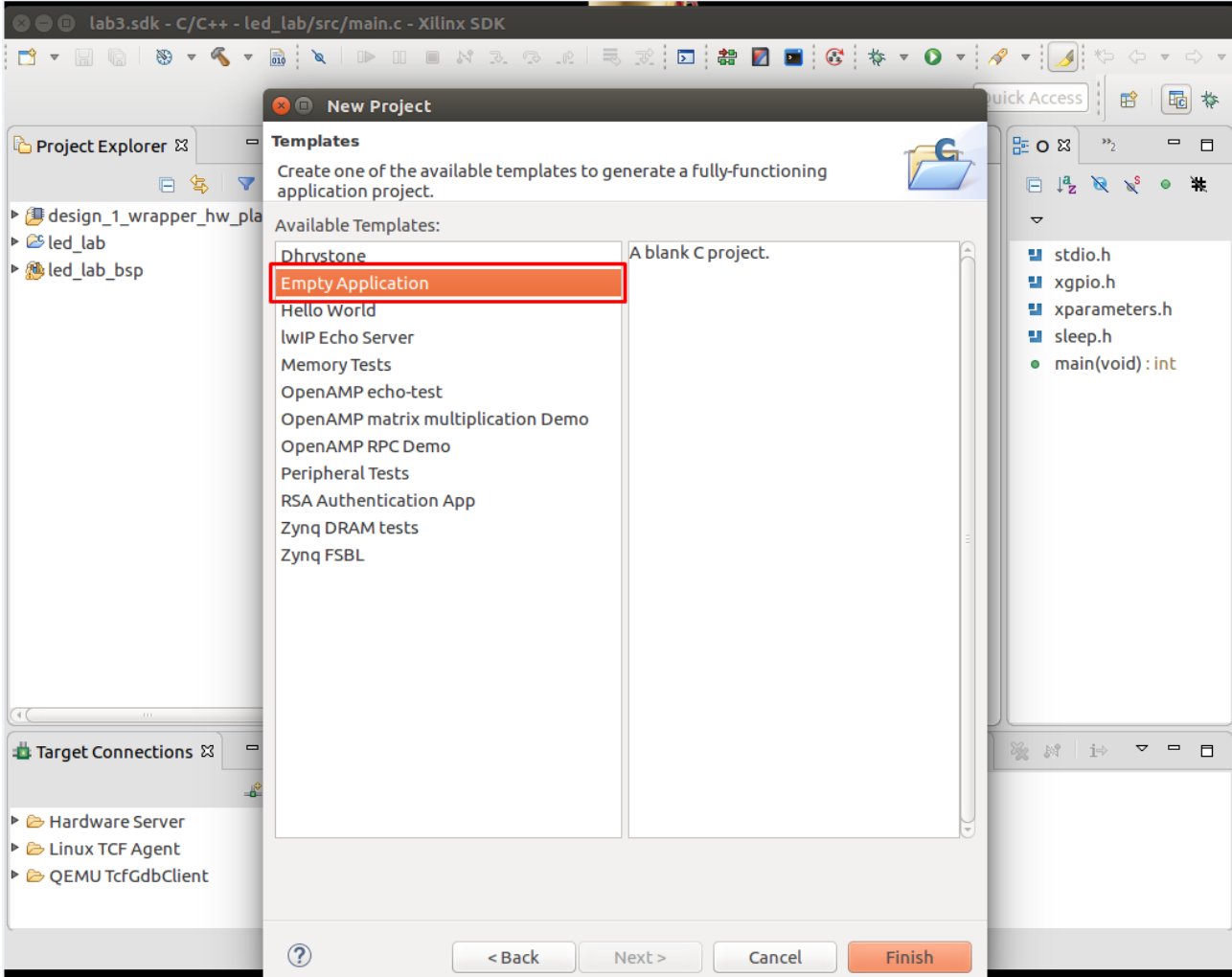


3) GPIO 회로 프로그래밍 Verilog 10

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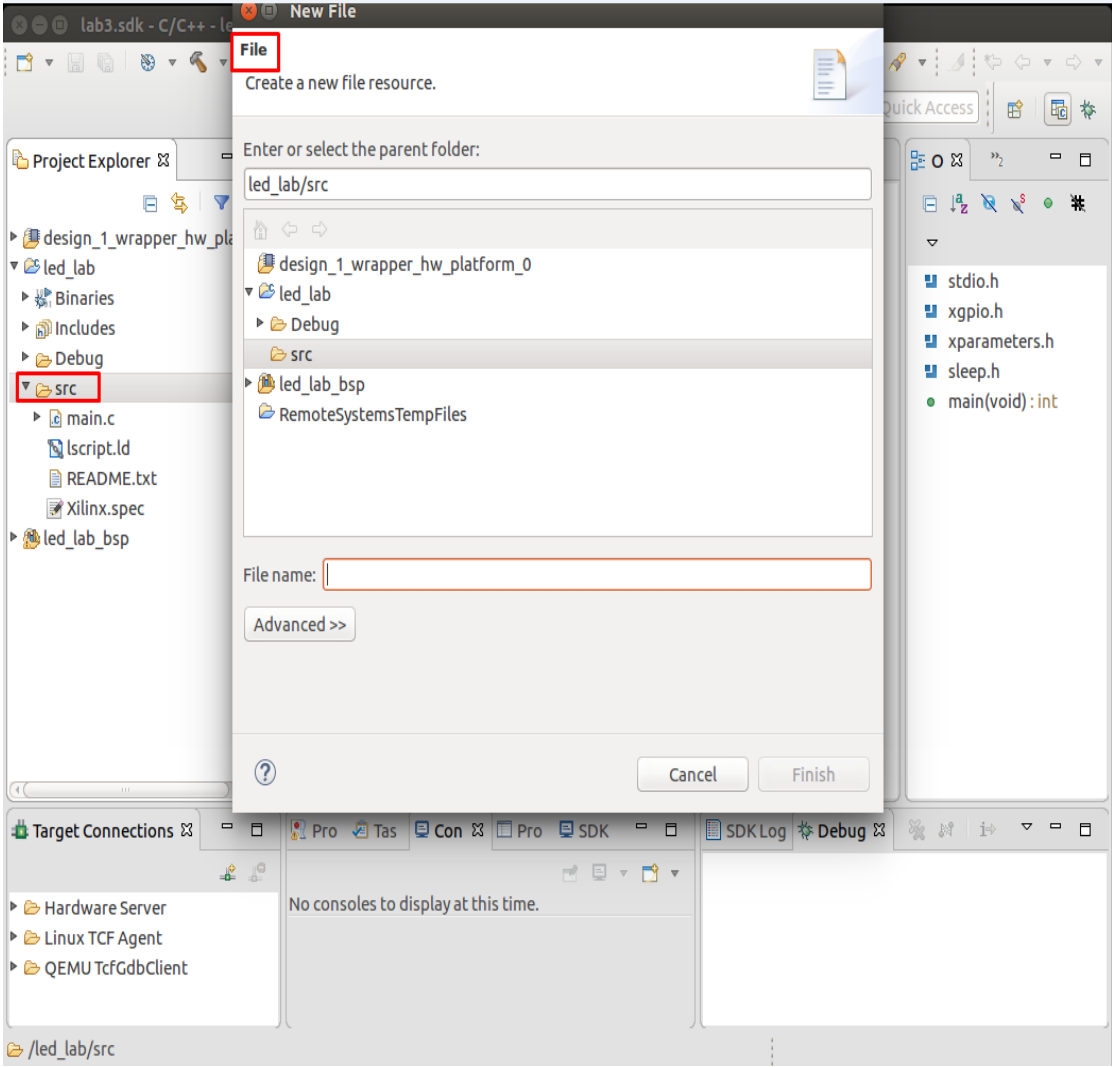


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3) GPIO 회로 프로그래밍 Verilog 11

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