TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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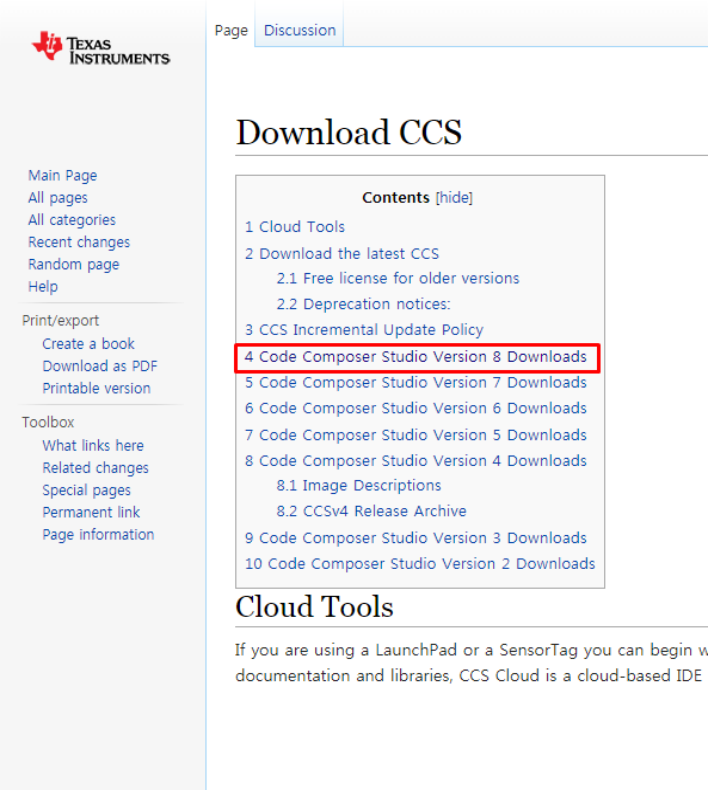
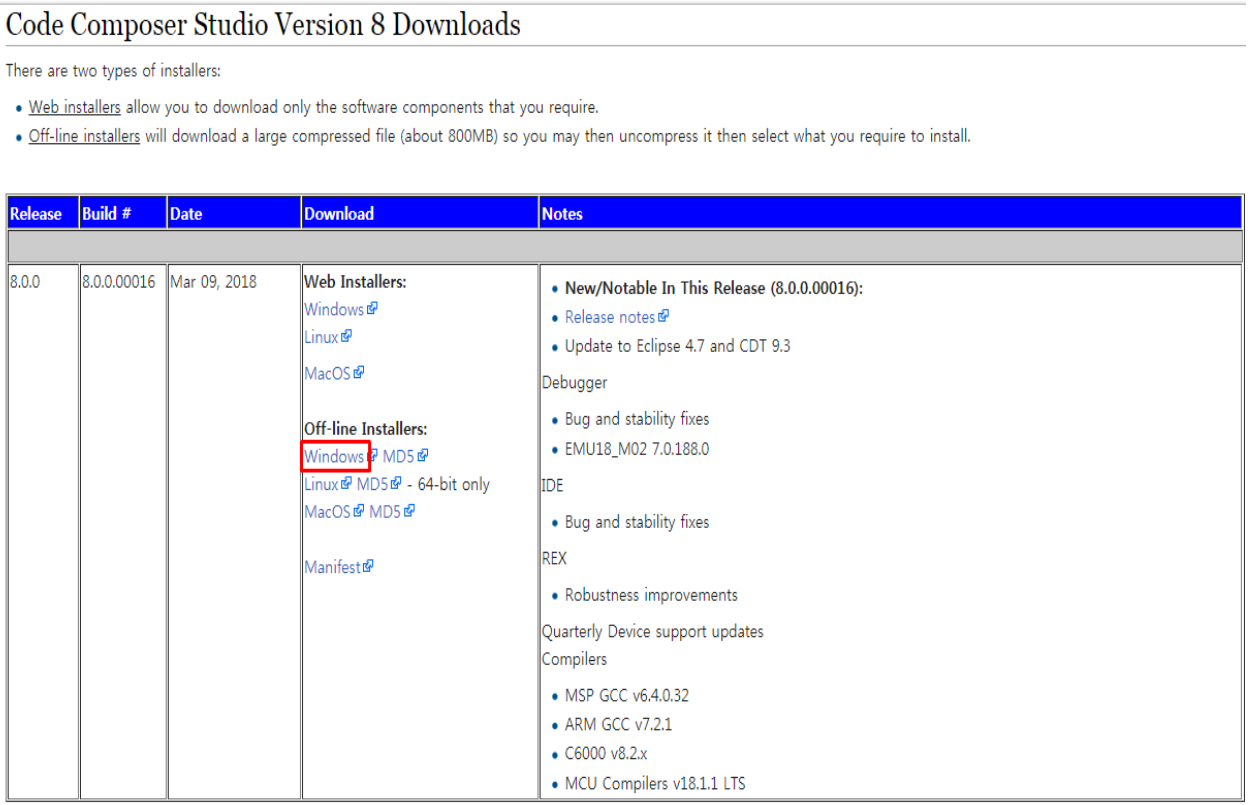
http://processors.wiki.ti.com/index.php/Download_CCS





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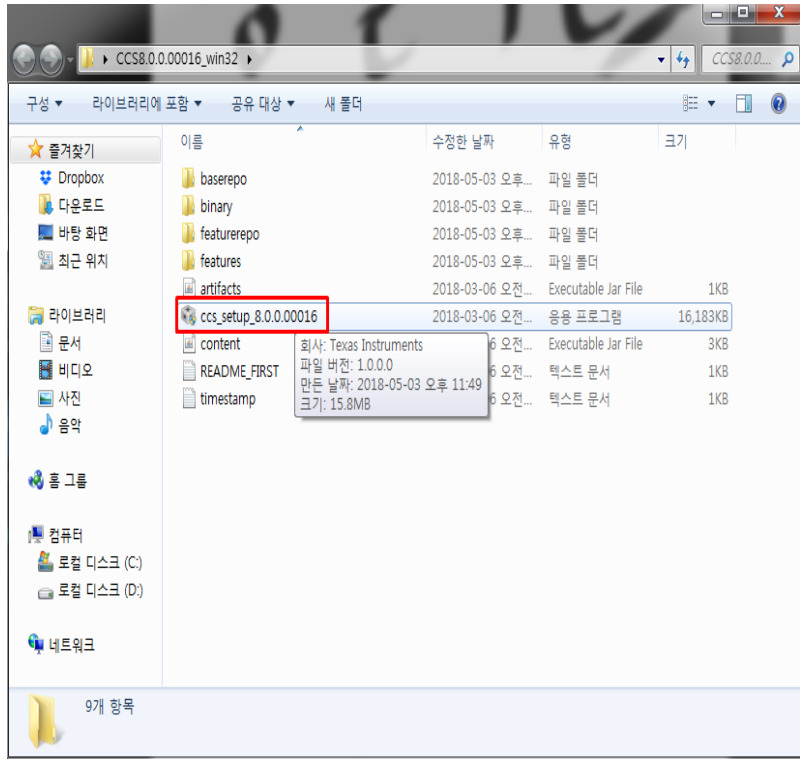

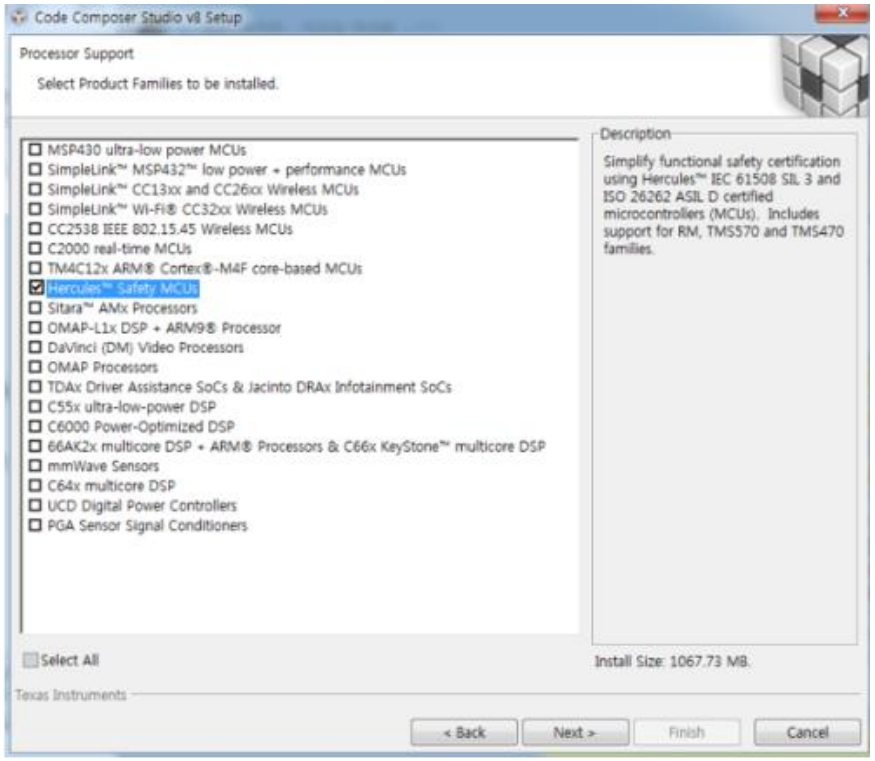

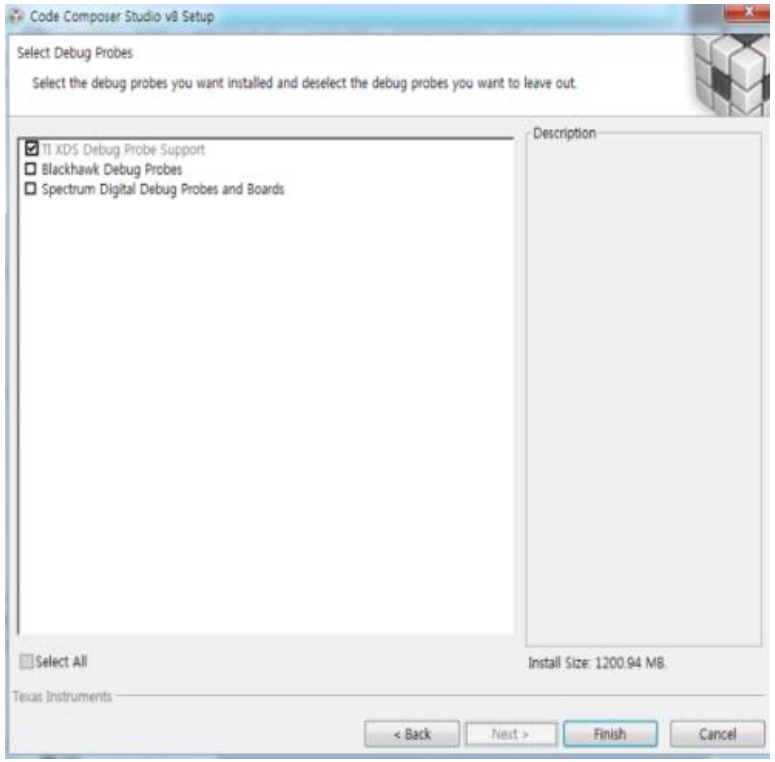

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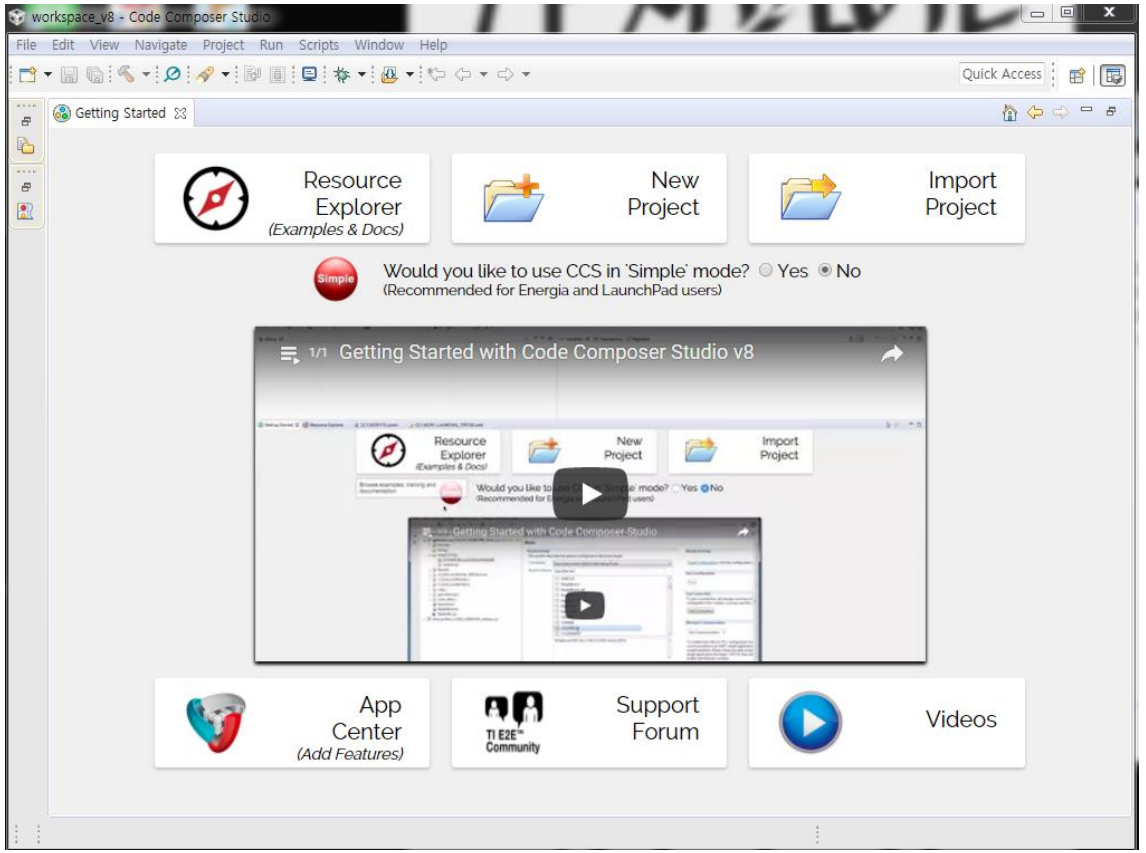

1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - HalCoGen

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HALCOGEN: HAL Code Generator tool	Download	Alert Me	ACTIVE	04.07.00	07-Jul-2017	PC	Vista, Windows 7, XP,
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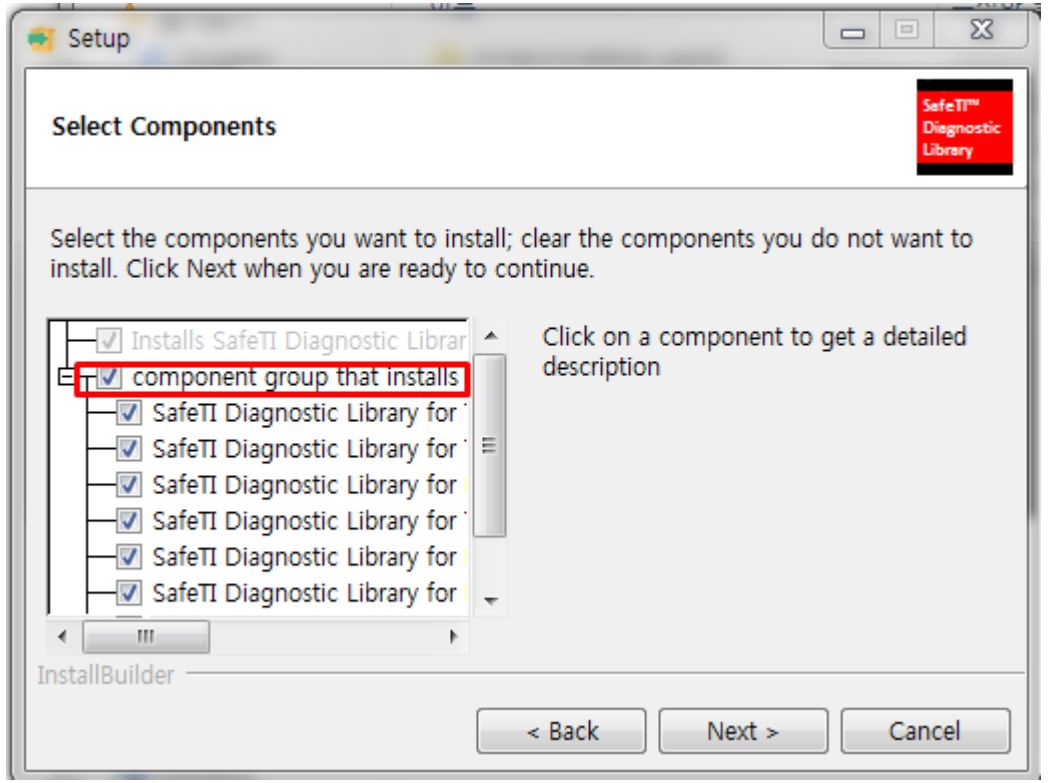

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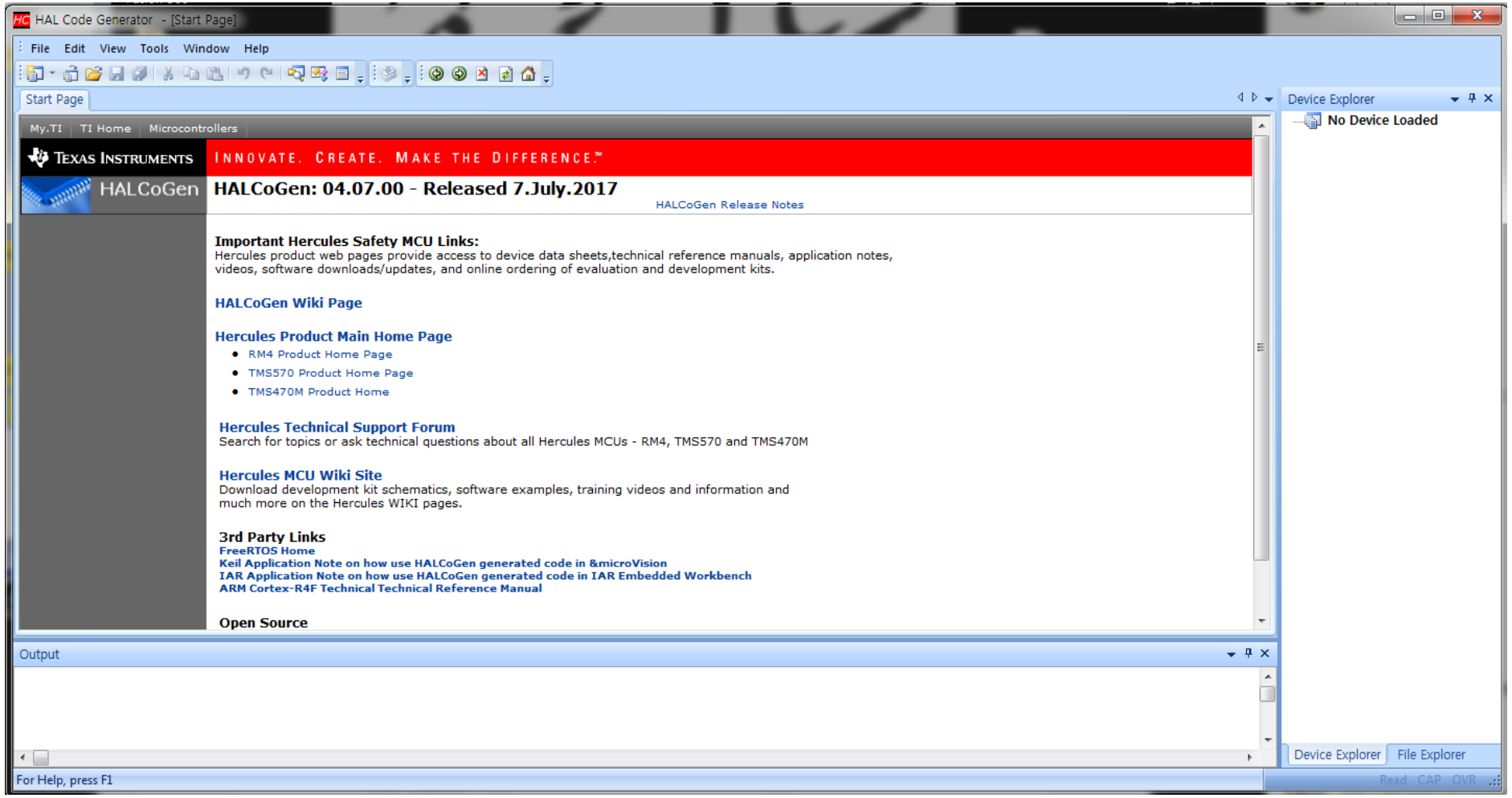
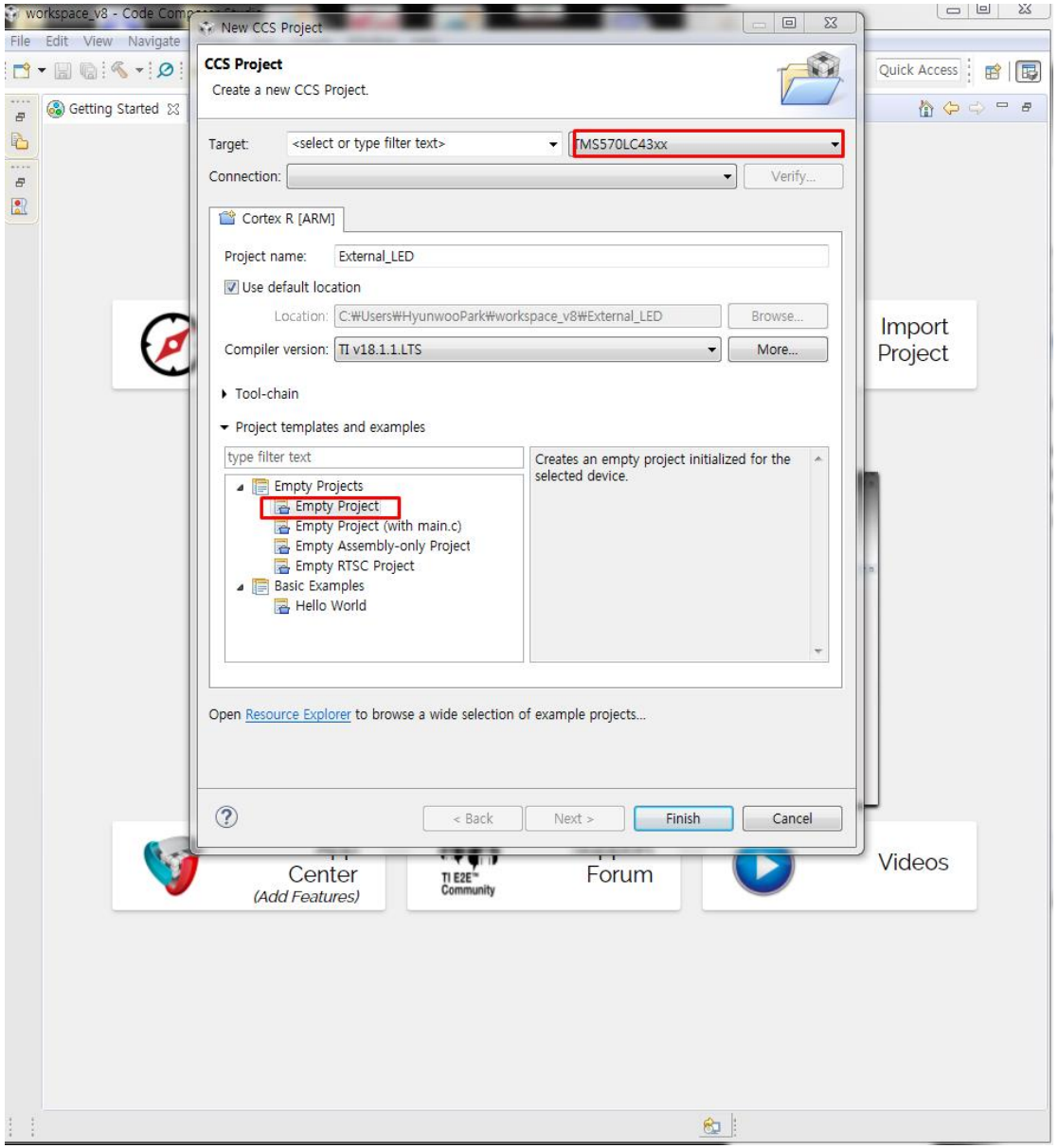
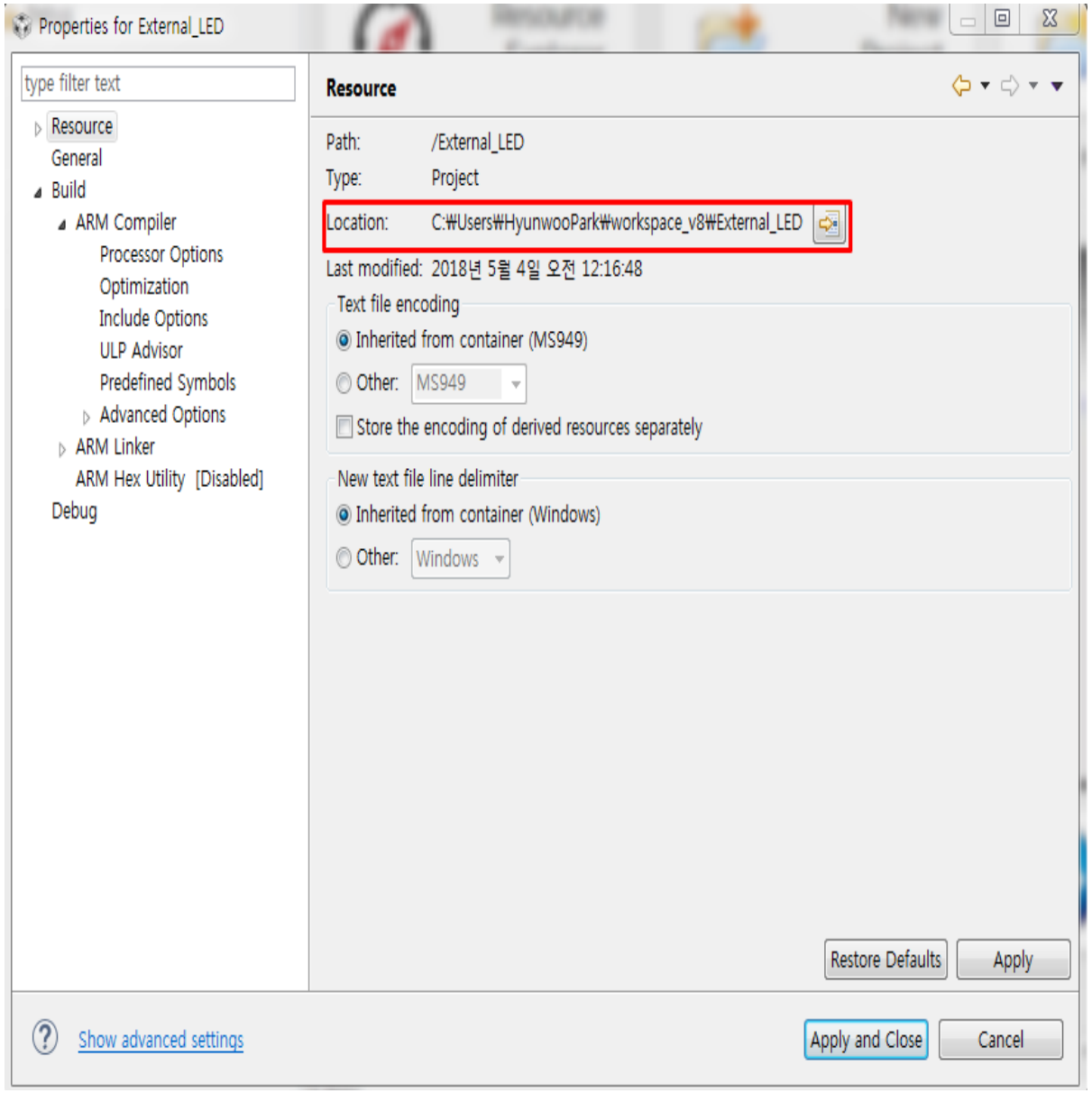


1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 – 연동





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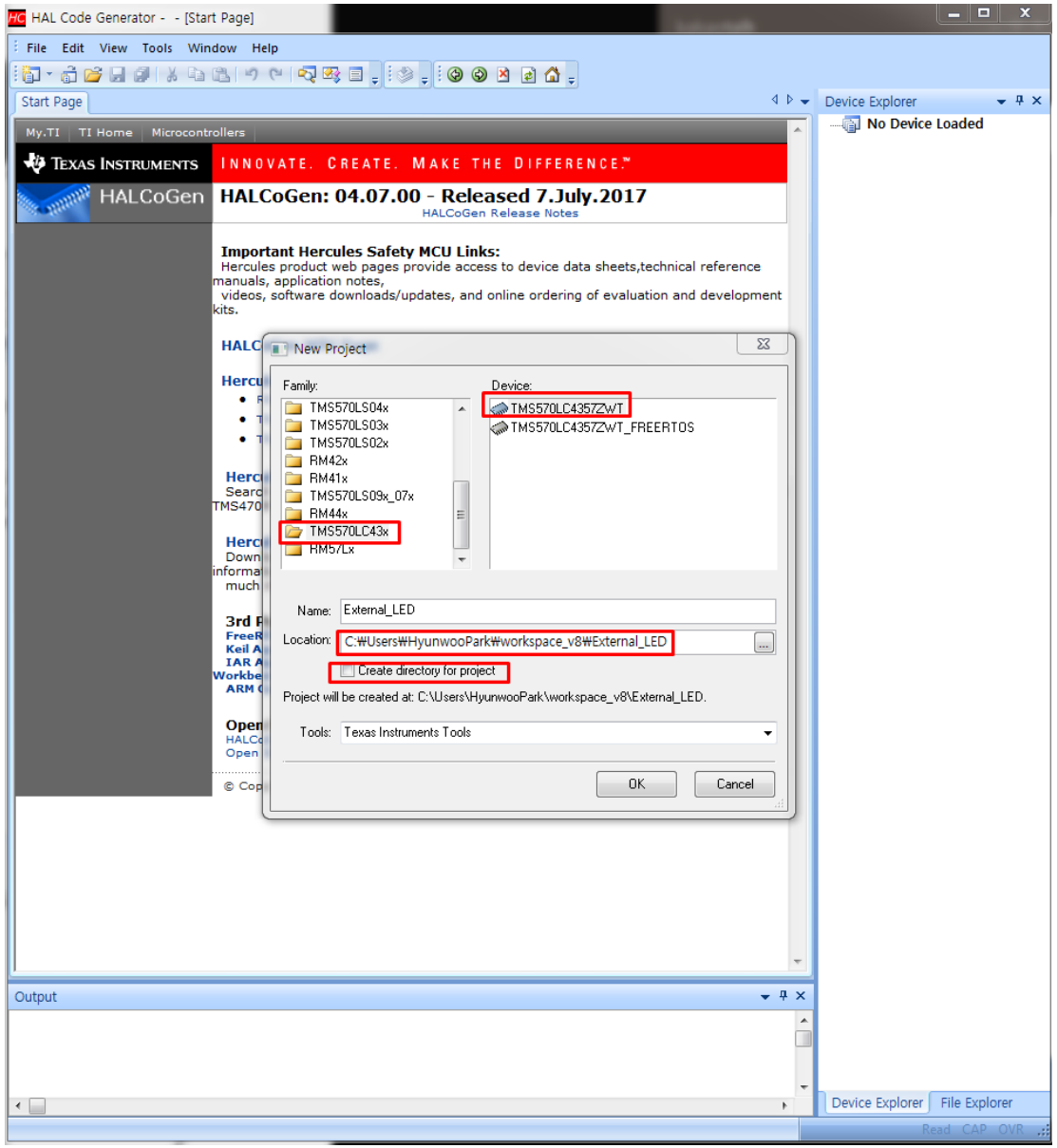

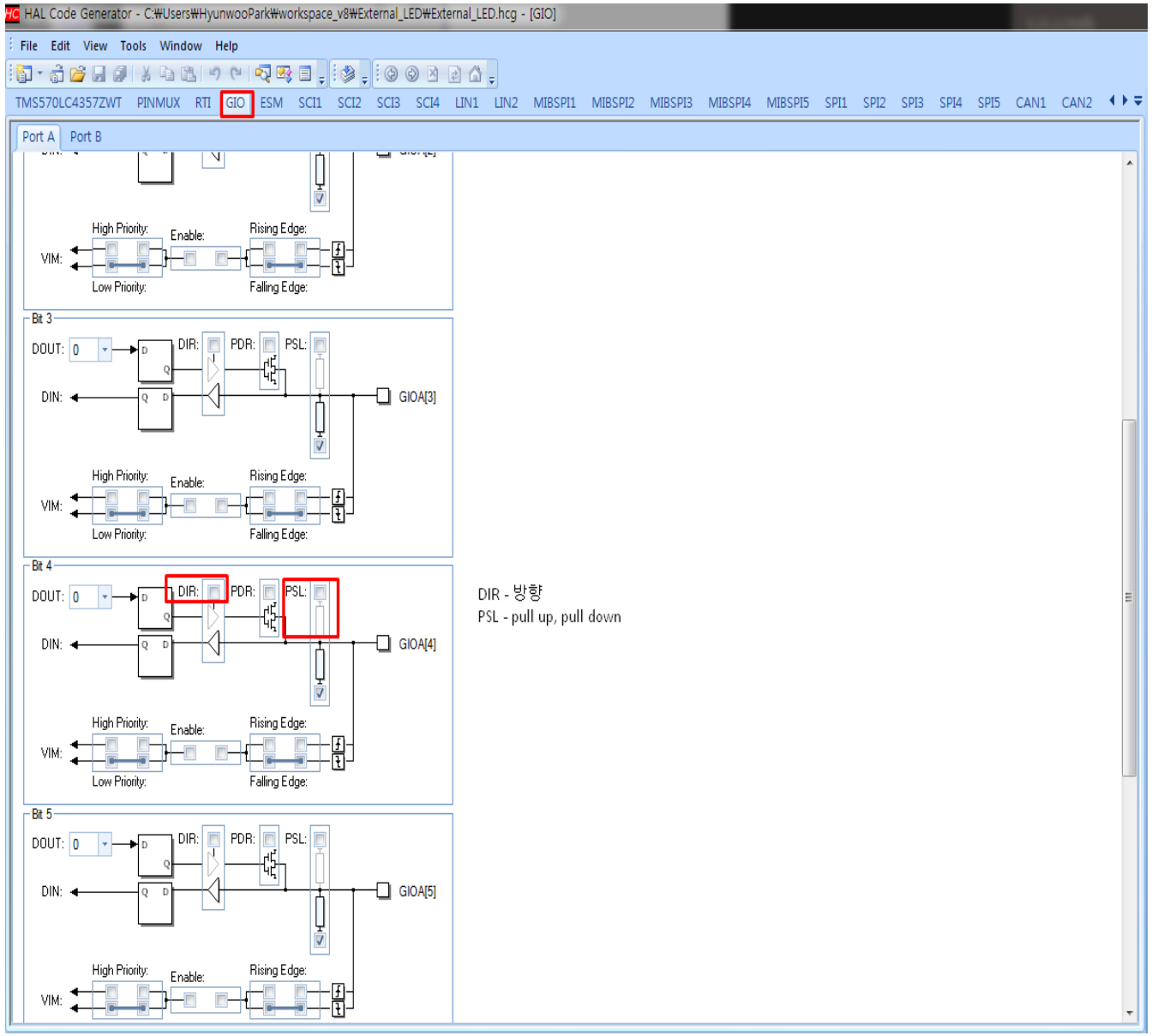

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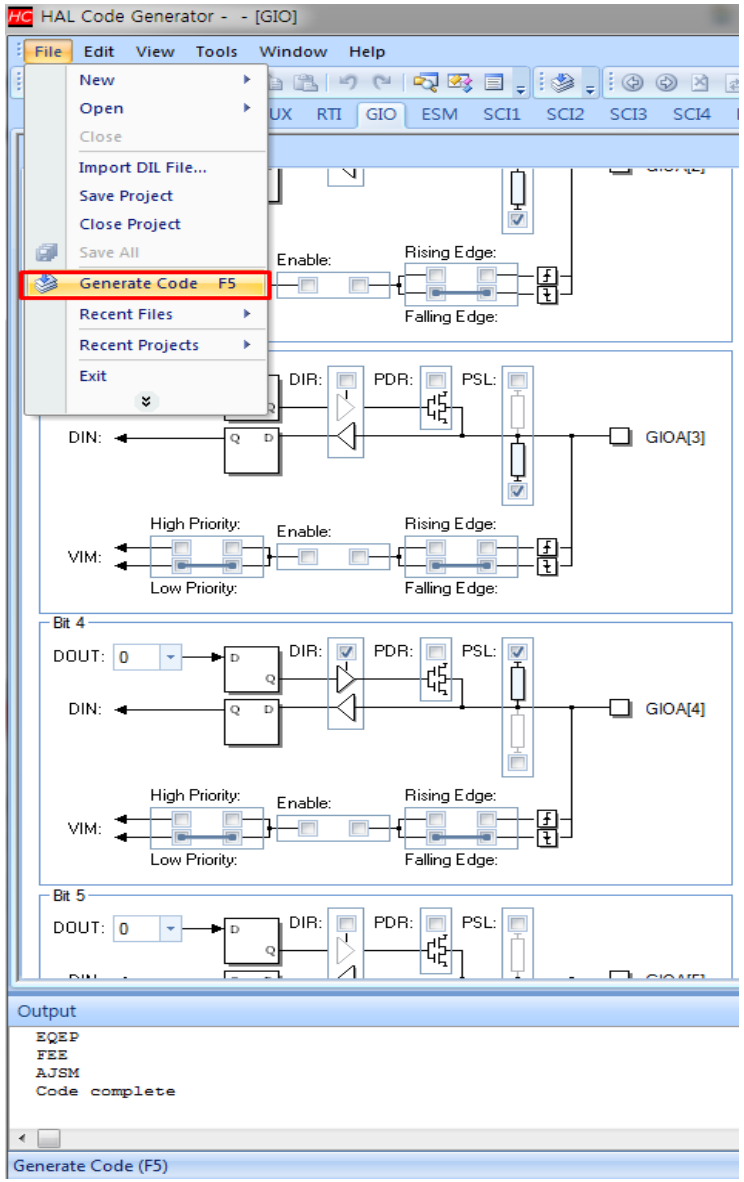

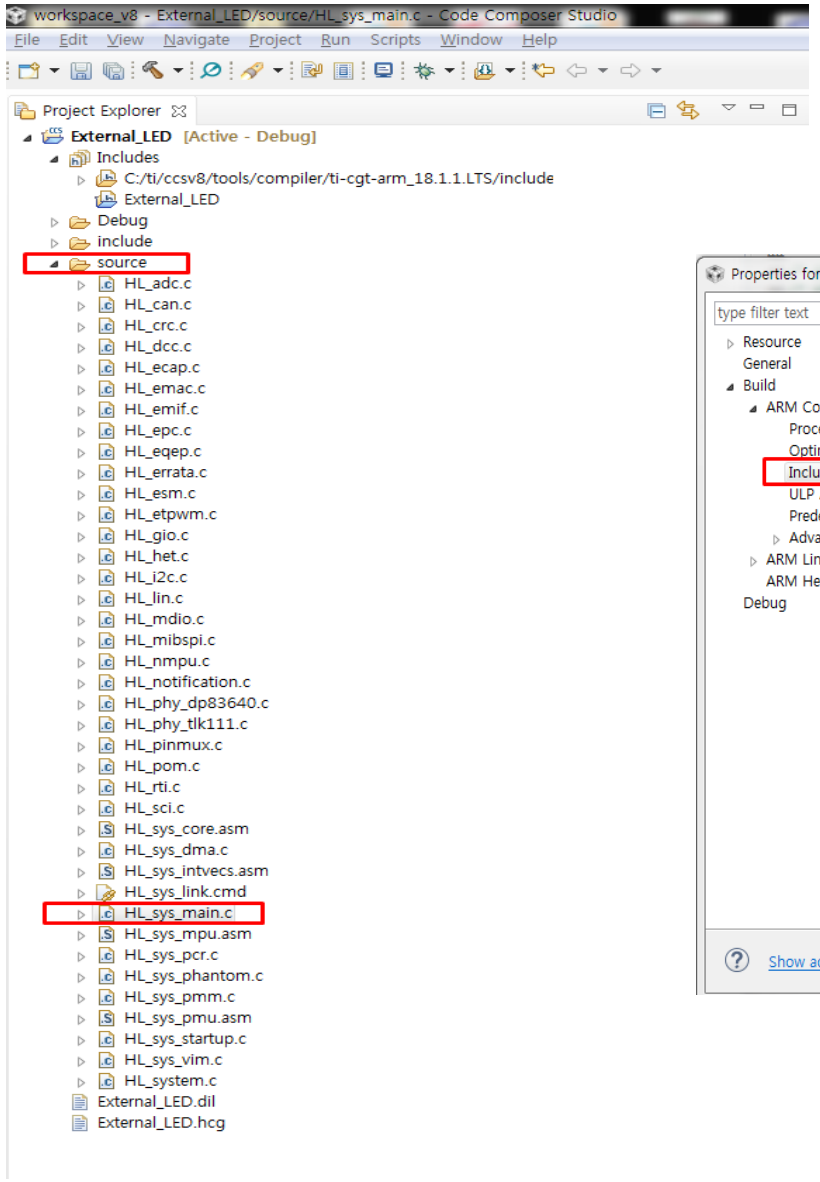

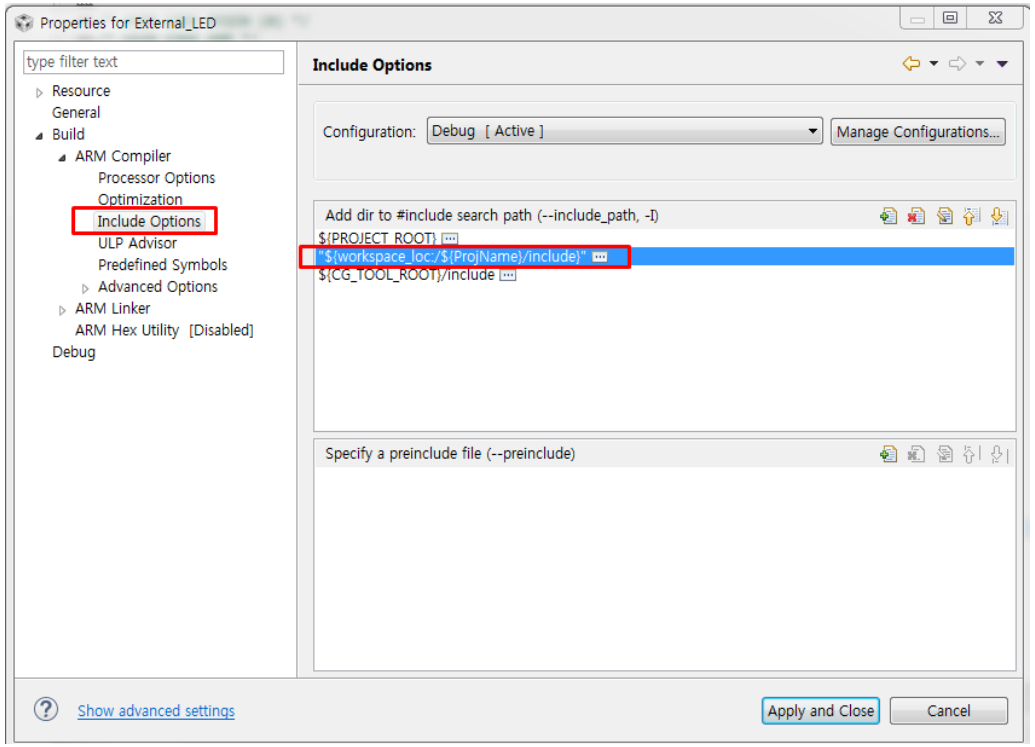

2. External LED GIO 기반 제어 예제

Getting Started | *HL_sys_main.c | HL_gio.c

```
46 /* USER CODE END */
47
48 /* Include Files */
49
50 #include "HL_sys_common.h"
51 #include "HL_gio.h"
52
53 /* USER CODE BEGIN (1) */
54 /* USER CODE END */
55
56 /** @fn void main(void)
57 *   @brief Application main function
58 *   @note This function is empty by default.
59 *
60 *   This function is called after startup.
61 *   The user can use this function to implement the application.
62 */
63
64 /* USER CODE BEGIN (2) */
65 /* USER CODE END */
66
67 uint8   emacAddress[6U] =   {0xFFU, 0xFFU, 0xFFU, 0xFFU, 0xFFU, 0xFFU};
68 uint32  emacPhyAddress  =   1U;
69
70 int main(void)
71 {
72 /* USER CODE BEGIN (3) */
73     gioInit();
74     gioSetPort(gioPORTA, 0xFFU);
75     gioSetDirection(gioPORTA, 0xFFU);
76     gioSetBit(gioPORTA, 4, 1);
77 /* USER CODE END */
78
79     return 0;
80 }
```

F3 – 함수 in

Alt +<- 방향키 – 함수 out

```
/** bring GIO module out of reset */
gioREG->GCR0    = 1U;
gioREG->ENACLR = 0xFFU;
gioREG->LVLCLR = 0xFFU;
```


25.5.1 GIO Global Control Register (GIOGCR0)

The GIOGCR0 register contains one bit that controls the module reset status. Writing a 0 to this bit puts the module in a reset state. After system reset, this bit must be set to 1 before configuring any other register of the GIO module. Figure 25-5 and Table 25-2 describe this register.

Figure 25-5. GIO Global Control Register (GIOGCR0) [offset = 00h]

31	16
Reserved	
R-0	

15	1	0
Reserved		RESET
R-0		R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 25-2. GIO Global Control Register (GIOGCR0) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reads return 0. Writes have no effect.
0	RESET		GIO reset.
		0	The GIO is in reset state.
		1	The GIO is operating normally.

2. External LED GIO 기반 제어 예제

```
/** bring GIO module out of reset */
gioREG->GCR0    = 1U;
gioREG->ENACLR = 0xFFU;
gioREG->LVLCLR = 0xFFU;
```


25.5.4.2 GIOENACLR Register

This register disables the interrupt. Figure 25-9 and Table 25-6 describe this register.

Figure 25-9. GIO Interrupt Enable Clear Register (GIOENACLR) [offset = 14h]

31–24	23–16	15–8	7–0
GIOENACLR 3	GIOENACLR 2	GIOENACLR 1	GIOENACLR 0
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 25-6. GIO Interrupt Enable Clear Register (GIOENACLR) Field Descriptions

Bit	Field	Value	Description
31-24	GIOENACLR 3		Interrupt disable for pins GIOD[7:0]
		0	Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
23-16	GIOENACLR 2		Interrupt disable for pins GIOC[7:0]
		0	Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
15-8	GIOENACLR 1		Interrupt disable for pins GIOB[7:0]
		0	Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
7-0	GIOENACLR 0		Interrupt disable for pins GIOA[7:0]
		0	Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.

25.5.5.2 GIOLVLCLR Register

The GIOLVLCLR register is used to configure an interrupt as a low-level interrupt going to the VIM. An interrupt can be configured as a low-level interrupt by writing a 1 into the corresponding bit of the GIOLVLCLR register. Writing a 0 has no effect. Figure 25-11 and Table 25-8 describe this register.

Figure 25-11. GIO Interrupt Priority Register (GIOLVLCLR) [offset = 1Ch]

31–24	23–16	15–8	7–0
GIOLVLCLR 3	GIOLVLCLR 2	GIOLVLCLR 1	GIOLVLCLR 0
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 25-8. GIO Interrupt Priority Register (GIOLVLCLR) Field Descriptions

Bit	Field	Value	Description
31-24	GIOLVLCLR 3		GIO low-priority interrupt for pins GIOD[7:0]
		0	Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2.
23-16	GIOLVLCLR 2		GIO low-priority interrupt for pins GIOC[7:0]
		0	Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2.
15-8	GIOLVLCLR 1		GIO low-priority interrupt for pins GIOB[7:0]
		0	Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2.
7-0	GIOLVLCLR 0		GIO low-priority interrupt for pins GIOA[7:0]
		0	Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2.