5월 3일 숙제

# Xilinx Zynq FPGA, TI DSP, MCU 기반의 프로그래밍 및 회로 설계 전문가 과정

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TMS570LC4357 Hercules MCU Technical Reference Manual 에서

용어들을 정리해보자

*GIO Global Control Register (GIOGCR0)

GIOGCR0 레지스터는 모듈 리셋 상태를 제어하는 ??1 비트를 포함한다.
이 비트에 0을 쓰면 모듈은 리셋 상태에 있다.
시스템 리셋 후 GIO 모듈의 다른 레지스터를 설정하기 전에 이 비트를 1로 설정해야한다.

**Figure 25-5. GIO Global Control Register (GIOGCR0) [offset = 00h]**

| 31 | | 16 |
|---|---|---|
| Reserved | | |
| R-0 | | |

| 15 | | 1 | 0 |
|---|---|---|---|
| Reserved | | | RESET |
| R-0 | | | R/WP-0 |

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

**Table 25-2. GIO Global Control Register (GIOGCR0) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-1 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 0 | RESET | | GIO reset. |
| | | 0 | The GIO is in reset state. |
| | | 1 | The GIO is operating normally. |

**NOTE:** Note that putting the GIO module in reset state is not the same as putting it in a low-power state.

*GIO Interrupt Enable Clear Register (GIOENACLR)

이 레지스터는 인터럽트를 허용하지 않는다.

**Figure 25-9. GIO Interrupt Enable Clear Register (GIOENACLR) [offset = 14h]**

| 31 | 24 | 23 | 16 |
|---|---|---|---|
| GIOENACLR 3 | | GIOENACLR 2 | |
| R/W-0 | | R/W-0 | |

| 15 | 8 | 7 | 0 |
|---|---|---|---|
| GIOENACLR 1 | | GIOENACLR 0 | |
| R/W-0 | | R/W-0 | |

LEGEND: R/W = Read/Write; -*n* = value after reset

**Table 25-6. GIO Interrupt Enable Clear Register (GIOENACLR) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-24 | GIOENACLR 3 | | Interrupt disable for pins GIOD[7:0] |
| | | 0 | Read: The interrupt is disabled.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is enabled.<br>Write: Disables the interrupt. |
| 23-16 | GIOENACLR 2 | | Interrupt disable for pins GIOC[7:0] |
| | | 0 | Read: The interrupt is disabled.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is enabled.<br>Write: Disables the interrupt. |
| 15-8 | GIOENACLR 1 | | Interrupt disable for pins GIOB[7:0] |
| | | 0 | Read: The interrupt is disabled.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is enabled.<br>Write: Disables the interrupt. |
| 7-0 | GIOENACLR 0 | | Interrupt disable for pins GIOA[7:0] |
| | | 0 | Read: The interrupt is disabled.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is enabled.<br>Write: Disables the interrupt. |

*GIO Interrupt Priority Register (GIOLVLCLR)

GIOLVLCLR 레지스터는 VIM으로 진행하는 로우 레벨 인터럽트로 설정하는 데 사용된다.
인터럽트는 GIOLVLCLR 레지스터의 해당 비트에 1을 기록함으로써 저레벨

인터럽트로 설정 될 수 있다.

**Figure 25-11. GIO Interrupt Priority Register (GIOLVLCLR) [offset = 1Ch]**

| 31 | | 16 |
|---|---|---|
| GIOLVLCLR 3 | | GIOLVLCLR 2 |
| R/W-0 | | R/W-0 |
| **15** | **8** | **7** | **0** |
| GIOLVLCLR 1 | | GIOLVLCLR 0 |
| R/W-0 | | R/W-0 |

LEGEND: R/W = Read/Write; *-n* = value after reset

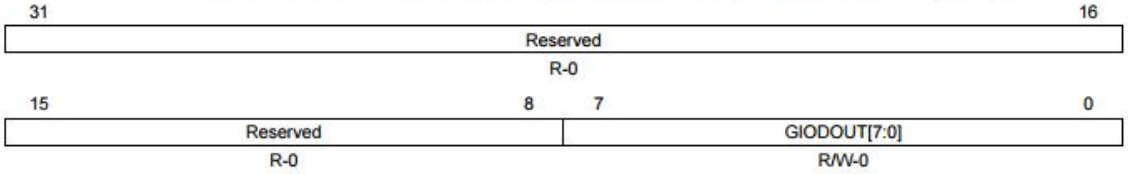
**Table 25-8. GIO Interrupt Priority Register (GIOLVLCLR) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-24 | GIOLVLCLR 3 | | GIO low-priority interrupt for pins GIOD[7:0] |
| | | 0 | Read: The interrupt is a low-level interrupt.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1.<br>Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2. |
| 23-16 | GIOLVLCLR 2 | | GIO low-priority interrupt for pins GIOC[7:0] |
| | | 0 | Read: The interrupt is a low-level interrupt.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1.<br>Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2. |
| 15-8 | GIOLVLCLR 1 | | GIO low-priority interrupt for pins GIOB[7:0] |
| | | 0 | Read: The interrupt is a low-level interrupt.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1.<br>Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2. |
| 7-0 | GIOLVLCLR 0 | | GIO low-priority interrupt for pins GIOA[7:0] |
| | | 0 | Read: The interrupt is a low-level interrupt.<br>Write: Writing a 0 to this bit has no effect. |
| | | 1 | Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOOFF1 and GIOEMU1.<br>Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOOFF2 and GIOEMU2. |

*GIO Data Output Register (GIODOUT[A-B])

GIODOUT 레지스터의 값은 출력으로 설정 될 때 포트 핀의 출력 상태 (high = 1 또는 low = 0)를 지정한다.

**Figure 25-19. GIO Data Output Registers (GIODOUT[A-B]) [offset = 3Ch, 5Ch]**




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

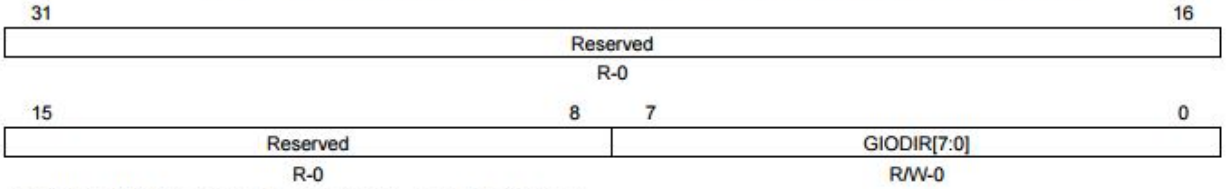
**Table 25-16. GIO Data Output Registers (GIODOUT[A-B]) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-8 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 7-0 | GIODOUT[*n*] | | GIO data output of port n, pins[7:0]. |
| | | 0 | The pin is driven to logic low (0). |
| | | 1 | The pin is driven to logic high (1). |
| | | | **Note: Output is in high impedance state if the GIOPDRx bit = 1 and GIODOUTx bit = 1.** |
| | | | **Note: GIO pin is placed in output mode by setting the GIODIRx bit to 1.** |

*GIO Data Direction Register (GIODIR[A-B])

GIODIR 레지스터는 주어진 포트의 핀이 입력 또는 출력으로 설정되는지 여부를 제어한다.

**Figure 25-17. GIO Data Direction Registers (GIODIR[A-B]) [offset = 34h, 54h]**




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

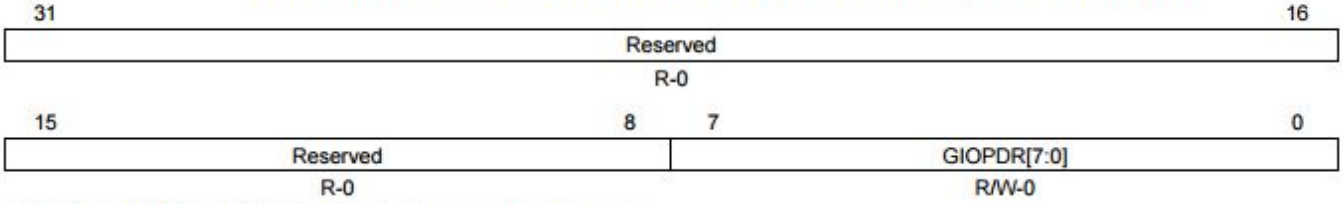
**Table 25-14. GIO Data Direction Registers (GIODIR[A-B]) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-8 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 7-0 | GIODIR[*n*] | | GIO data direction of port n, pins [7:0] |
| | | 0 | The GIO pin is an input. Note: If the pin direction is set as an input, the output buffer is tristated. |
| | | 1 | The GIO pin is an output. |

*GIO Open Drain Register (GIOPDR[A-B])

이 레지스터의 값은 데이터 핀의 오픈 드레인 기능을 활성화 또는 비활성화한다.

**Figure 25-22. GIO Open Drain Registers (GIOPDR[A-B]) [offset = 48h, 68h]**




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

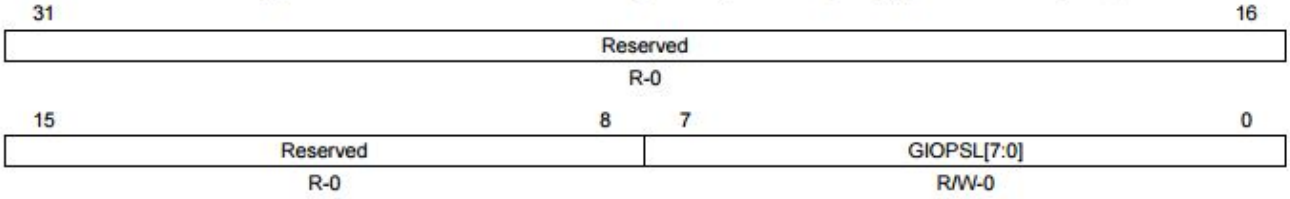
**Table 25-19. GIO Open Drain Registers (GIOPDR[A-B]) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-8 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 7-0 | GIOPDR[*n*] | | GIO open drain for port n, pins[7:0] |
| | | 0 | The GIO pin is configured in push/pull (normal GIO) mode. The output voltage is $V_{OL}$ or lower if GIODOUT bit = 0 and $V_{OH}$ or higher if GIODOUT bit = 1. |
| | | 1 | The GIO pin is configured in open drain mode. The GIODOUTx bit controls the state of the GIO output buffer: GIODOUTx = 0, the GIO output buffer is driven low; GIODOUTx = 1, the GIO output buffer is tristated. |

*GIO Pull Select Register (GIOPSL[A-B])

이 레지스터의 값은 핀의 풀업 또는 풀다운 기능을 선택한다.

**Figure 25-24. GIO Pull Select Registers (GIOPSL[A-B]) [offset = 50h, 70h]**




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

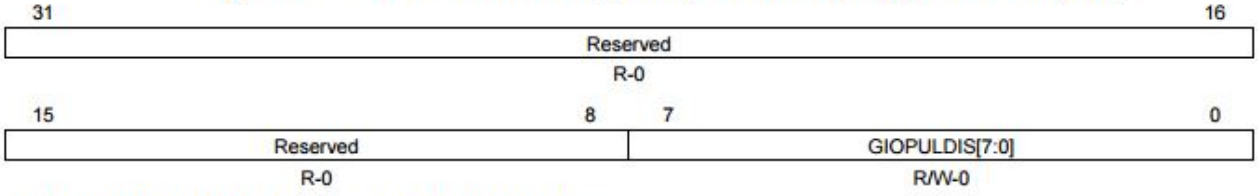
**Table 25-21. GIO Pull Select Registers (GIOPSL[A-B]) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-8 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 7-0 | GIOPSL[*n*] | | GIO pull select for port n, pins[7:0] |
| | | 0 | The pull down functionality is select, when pull up/pull down logic is enabled. |
| | | 1 | The pull up functionality is select, when pull up/pull down logic is enabled. |
| | | | **Note: The pull up/pull down functionality is enabled by clearing corresponding bit in GIOPULDIS to 0.** |

*GIO Pull Disable Register (GIOPULDIS[A-B])

이 레지스터의 값은 핀의 풀 제어 기능을 활성화 또는 비활성화한다.

**Figure 25-23. GIO Pull Disable Registers (GIOPULDIS[A-B]) [offset = 4Ch, 6Ch]**




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 25-20. GIO Pull Disable Registers (GIOPULDIS[A-B]) Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-8 | Reserved | 0 | Reads return 0. Writes have no effect. |
| 7-0 | GIOPULDIS[*n*] | | GIO pull disable for port n, pins[7:0]. Writes to this bit will only take effect when the GIO pin configured as an input pin. |
| | | 0 | The pull functionality is enabled. |
| | | 1 | The pull functionality is disabled. |
| | | | **Note: The GIO pin is placed in input mode by clearing the GIODIRx bit to 0.** |