Xilinx Zynq FPGA, TI DSP, MCU 기반의 프로그래밍 및 회로 설계 전문가 과정

#52

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과제

PWM 제어

sys_main.c

```c
#include "HL_sys_common.h"
#include "HL_system.h"
#include "HL_etpwm.h"

int idx=0;
uint32 value=0;
uint32 duty_arr[6]={1000,1200,1400,1600,1800,2000};



void pwmSet(void);
void delay(uint32);

int main(void)
{
  etpwmInit();
  etpwmStartTBCLK();

  delay(10000000000);

  for(;;)
  {
    pwmSet();

  }

  return 0;
}
```

```c
void delay(uint32 delay)
{
  int i;

  for(i=0; i< delay; i++)
    ;
}
void pwmSet(void)
{
  value=duty_arr[idx % 6];
  etpwmSetCmpA(etpwmREG1,value);
  idx++;

}
```

메인함수를 보면 이렇게 되어있다.

EtpwmInit() 함수를 들여다 보도록 한다.

EtpwmInit

```c
void etpwmInit(void)
{

  /** @b initialize @b ETPWM1 */

  /** - Sets high speed time-base clock prescale bits */
  etpwmREG1->TBCTL = (uint16)5U << 7U;

  /** - Sets time-base clock prescale bits */
  etpwmREG1->TBCTL |= (uint16)((uint16)0U << 10U);

  /** - Sets time period or frequency for ETPWM block both
PWMA and PWMB*/
  etpwmREG1->TBPRD = 19999U;
```

```
  /** - Setup the duty cycle for PWMA */
  etpwmREG1->CMPA = 1000U;

  etpwmREG1->CMPB = 10000U;

  /** - Force EPWMxA output high when counter reaches zero
and low when counter reaches Compare A value */
  etpwmREG1->AQCTLA = ((uint16)((uint16)ActionQual_Set   <<
0U)
         | (uint16)((uint16)ActionQual_Clear << 4U));

  /** - Force EPWMxB output high when counter reaches zero
and low when counter reaches Compare B value */
  etpwmREG1->AQCTLB = ((uint16)((uint16)ActionQual_Set   <<
0U)
         | (uint16)((uint16)ActionQual_Clear << 8U));


  etpwmREG1->DBCTL = ((uint16)((uint16)0U << 5U)
        | (uint16)((uint16)0u << 4U)
        | (uint16)((uint16)0U << 3U)
        | (uint16)((uint16)0U << 2U)
        | (uint16)((uint16)0U << 1U)
        | (uint16)((uint16)0U << 0U));

  etpwmREG1->DBRED = 110U;

  etpwmREG1->DBFED = 110U ;


  etpwmREG1->PCCTL = ((uint16)((uint16)0U << 0U)    /*
Enable/Disable chopper module */
        | (uint16)((uint16)0U << 1U)
        | (uint16)((uint16)3U << 8U)
        | (uint16)((uint16)0U << 5U));

/** - Set trip source enable */
etpwmREG1->TZSEL = 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U;

/** - Set interrupt enable */
etpwmREG1->TZEINT = 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U
       | 0x0000U;

etpwmREG1->ETSEL = (uint16)NO_EVENT;

if ((etpwmREG1->ETSEL & 0x0007U) != 0U)
{
  etpwmREG1->ETSEL |= 0x0008U;
}
etpwmREG1->ETPS = 1U;

etpwmREG1->ETSEL |= ((uint16)(0x0000U)
```

```
        | (uint16)(0x0000U)
        | (uint16)((uint16)DCAEVT1 << 8U)
        | (uint16)((uint16)DCBEVT1 << 12U));

  etpwmREG1->ETPS |= ((uint16)((uint16)1U << 8U)
        | (uint16)((uint16)1U << 12U));

}
```

처음에 나오는 레지스터는 TBCTL 이다.
TBCTL 5<<7 즉 7 번째 비트에 5 를 집어넣는다.

데이터 시트를 확인한다.

35.4.1.2 Time-Base Control Register (TBCTL)

Figure 35-64. Time-Base Control Register (TBCTL) [offset = 02h]

15	14	13	12	11	10	9	8
FREE	SOFT	PHSDIR	CLKDIV			HSPCLKDIV	
R/W-0	R/W-0	R/W-0	R/W-0			R/W-0	

7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W-1	R/W-0	R/W-0		R/W-0	R/W-0	R/W-3h	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 35-24. Time-Base Control Register (TBCTL) Field Descriptions

Bit	Field	Value	Description
15-14	FREE, SOFT		Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events:
		0	Stop after the next time-base counter increment or decrement.
		1h	Stop when counter completes a whole cycle: • Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) • Down-count mode: stop when the time-base counter = 0x0000 (TBCTR = 0x0000) • Up-down-count mode: stop when the time-base counter = 0x0000 (TBCTR = 0x0000)
		2h-3h	Free run
13	PHSDIR		Phase Direction Bit. This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (TBCTR) will count after a synchronization event occurs and a new phase value is loaded from the phase (TBPHS) register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored.
		0	Count down after the synchronization event.
		1	Count up after the synchronization event.
12-10	CLKDIV		Time-base Clock Prescale Bits. These bits determine part of the time-base clock prescale value: TBCLK = VCLK3 / (HSPCLKDIV × CLKDIV)
		0	/1 (default on reset)
		1h	/2
		2h	/4
		3h	/8
		4h	/16
		5h	/32
		6h	/64
		7h	/128
9-7	HSPCLKDIV		High Speed Time-base Clock Prescale Bits. These bits determine part of the time-base clock prescale value: TBCLK = VCLK3 / (HSPCLKDIV × CLKDIV)
		0	/1
		1h	/2 (default on reset)
		2h	/4
		3h	/6
		4h	/8
		5h	/10
		6h	/12
		7h	/14

Table 35-24. Time-Base Control Register (TBCTL) Field Descriptions (continued)

Bit	Field	Value	Description
6	SWFSYNC		Software Forced Synchronization Pulse.
		0	Writing a 0 has no effect and reads always return a 0.
		1	Writing a 1 forces a one-time synchronization pulse to be generated.
			This event is ORed with the EPWMxSYNCI input of the ePWM module.
			SWFSYNC is valid (operates) only when EPWMxSYNCI is selected by SYNCOSEL = 00.
5-4	SYNCOSEL		Synchronization Output Select. These bits select the source of the EPWMxSYNCO signal.
		0	EPWMxSYNC
		1h	CTR = zero: Time-base counter equal to zero (TBCTR = 0x0000)
		2h	CTR = CMPB : Time-base counter equal to counter-compare B (TBCTR = CMPB)
		3h	Disable EPWMxSYNCO signal
3	PRDLD		Active Period Register Load From Shadow Register Select.
		0	The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero.
			A write or read to the TBPRD register accesses the shadow register.
		1	Load the TBPRD register immediately without using a shadow register.
			A write or read to the TBPRD register directly accesses the active register.
2	PHSEN		Counter Register Load From Phase Register Enable.
		0	Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS).
		1	Load the time-base counter with the phase register when an EPWMxSYNCI input signal occurs or when a software synchronization is forced by the SWFSYNC bit, or when a digital compare sync event occurs.
1-0	CTRMODE		Counter Mode.
			The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change.
			These bits set the time-base counter mode of operation as follows:
		0	Up-count mode
		1h	Down-count mode
		2h	Up-down-count mode
		3h	Stop-freeze counter operation (default on reset)

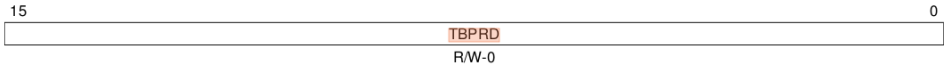
HSPCLKDIV 가 7 번째 비트이다. 이 부분은 VCLK 의 주파수를 TBCLK = VCLK3 / (HSPCLKDIV × CLKDIV) 로 분주해주는 비트이다 여기서 5 는 10 이므로 VCLK3 / 10 분주를 하게된다.

VCLK 는 앞에서 PLL 을 통해 15 분주 되어 10 MHz 로 들어오고 그다음 이 레지스터에 의해 10 분주 되어 1MHz 로 PWM 동작 주파수로 들어오게 된다.
(여기서 CLKDIV 는 default 값이라 1 로 리셋되어있는 상태이다.)

여기서 0 번비트는 카운트 모드를 정해주는데 CTRMODE =0 이기때문에 up 카운트 모드이다.
나머지는 default 기 때문에 리셋 상태가 되거나 사용하지 않는다.

35.4.1.4 Time-Base Period Register (TBPRD)

Figure 35-66. Time-Base Period Register (TBPRD) [offset = 08h]



LEGEND: R/W = Read/Write; *-n* = value after reset

Table 35-26. Time-Base Period Register (TBPRD) Field Descriptions

Bits	Name	Description
15-0	TBPRD	These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. • If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals 0. • If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. • The active and shadow registers share the same memory map address.

PRDLD 의 카운터는 현재 0 이다 이 TBPRD 레지스터는 TBCLT 레지스터의의 PRDLD 를 도와주는 녀석이다.PRDLD 값이 0 이면 Shadow 레지스터인 TBPRD 의 값을 카운터 값으로 가져옵니다.
TBPRD = 19999 이 므로 총 카운터 값이 19999 가 되고 이게 주기가 된다.
현재 PWM 에 들어오는 클럭 주수는 1MHz 이며 이건 0.000001 초의 주기를 갖는 다는 뜻이며 0.000001 초마다 카운터 한개를 주는데 0~19999 를 세면 PWM 이 동작하기 때문에 PWM 의 주기는 0.000001 * 20000 이 되며 이는 20ms 가 된다. 이것을 주파수로 바게 꾸되면 50Hz 인걸 알수 있으며, 모터의 동작 주파수와 일치하는 것을 볼 수 있다.

CMPA 레지스터
우리는 PWM A 를 사용하기 때문에 CMPA 레지스 그리고 이 레지스터와 연결되있는 레지스터만 확인하면 된다.

35.4.2.2 Counter-Compare A Register (CMPA)

Figure 35-69. Counter-Compare A Register (CMPA) [offset = 10h]

15	0
CMPA	
R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 35-29. Counter-Compare A Register (CMPA) Field Descriptions

Bits	Name	Description
15-0	CMPA	The value in the active CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: • Do nothing; the event is ignored. • Clear: Pull the EPWMxA and/or EPWMxB signal low. • Set: Pull the EPWMxA and/or EPWMxB signal high. • Toggle the EPWMxA and/or EPWMxB signal. Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed. • If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. • Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. • If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. • In either mode, the active and shadow registers share the same memory map address.

CMPA 는 카운터가 설정한 값이 되면 어떤 동작을 실행시킨다.
그 동작을 설정하는 레지스터는 AQCTLA 와 AQCT 레지스터이다.
여기서 CMPA = 1000 으로 되어있다. 여기서 예상할 수 있는것은 우리가 HALCOGEN 에서 듀티비를 5%로 설정했는데, 현재 위에 구한 총 카운터의 갯수 19999 의 5%는 10000 인걸 알 수 있고 이 값과 카운터 값이 같아지면 어떤 동작 즉 PWM 의 듀티비를 제어 한다는 것을 예상 할수 있다.
CMPB 는 PWMB 를 제어하는데 우리는 PWMB 를 사용하지 않으므로 확인하지 않겠다.

CMPA = 1000 인걸 기억하고 다음으로 넘어가도록 한다.

```
etpwmREG1->AQCTLA =
        ((uint16)((uint16)ActionQual_Set   << 0U)
        | (uint16)((uint16)ActionQual_Clear << 4U));
```

```
ActionQual_Set      = 2U
ActionQual_Clear    = 1U
```

AQCTLA 의 0 번 비트에 2 를 셋팅하고 , 4 번 비트에 1 을 셋팅한다. 데이터 시트를 통해 어떤 행동인지 확인해본다.

35.4.3.1 Action-Qualifier Output A Control Register (AQCTLA)

Figure 35-71. Action-Qualifier Output A Control Register (AQCTLA) [offset = 14h]

15	12	11	10	9	8
Reserved		CBD		CBU	
R-0		R/W-0		R/W-0	

7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35-31. Action-Qualifier Output A Control Register (AQCTLA) Field Descriptions

Bits	Name	Value	Description
15-12	Reserved	0	Reserved
11-10	CBD		Action when the time-base counter equals the active CMPB register and the counter is decrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
9-8	CBU		Action when the counter equals the active CMPB register and the counter is incrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
7-6	CAD		Action when the counter equals the active CMPA register and the counter is decrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5-4	CAU		Action when the counter equals the active CMPA register and the counter is incrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3-2	PRD		Action when the counter equals the period. Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
1-0	ZRO		Action when counter equals zero. Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

ZRO = 카운터가 0 일때 즉 처음 셋팅을 의미한다 .
현재 2 로 설정되있기 때문에 처음 시작은 High 로 시작된다. 전압으로 이야기 하면 데이터 핀에서 3.3V 의 전압이 나오게된다.

4 번비트 = 1
CAU = 증가하는 카운터 값이 CMP 와 같아졌을 때, 출력을 Low level 로 내립니다.

즉 CMP 는 듀티를 설정해 주는 녀석입니다.

```
uint32 duty_arr[6]={1000,1200,1400,1600,1800,2000};
```

여기까지 해석한 후 위의 배열을 보면 5%~ 10%의 듀티를 나열한 배열인 것을 알 수 있으며, 이 값은 Delay 마다 바뀝니다. 따라서 서서히 변하는 PWM 파형을 오실로스 코프로 관찰할 수 있었습니다.

DBCTL

```
etpwmREG1->DBCTL = ((uint16)((uint16)0U << 5U)
         | (uint16)((uint16)0u << 4U)
         | (uint16)((uint16)0U << 3U)
         | (uint16)((uint16)0U << 2U)
         | (uint16)((uint16)0U << 1U)
         | (uint16)((uint16)0U << 0U));
```

0~5 번까지 0 으로 셋팅한다. 데이터 시트를 확인한다.

35.4.4.1 Dead-Band Generator Control Register (DBCTL)

Figure 35-75. Dead-Band Generator Control Register (DBCTL) [offset = 1Ch]

15	14	13	12	11	10	9	8
HALFCYCLE	Reserved						
R/W-0	R-0						

7	6	5	4	3	2	1	0
Reserved		IN_MODE		POLSEL		OUT_MODE	
R-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35-35. Dead-Band Generator Control Register (DBCTL) Field Descriptions

Bits	Name	Value	Description
15	HALFCYCLE		Half Cycle Clocking Enable Bit.
		0	Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate.
		1	Half cycle clocking enabled. The dead-band counters are clocked at TBCLK × 2.
14-6	Reserved	0	Reserved
5-4	IN_MODE		Dead Band Input Mode Control. Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown in Figure 35-28. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays.
		0	EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.
		1h	EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.
		2h	EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.
		3h	EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.
3-2	POLSEL		Polarity Select Control. Bit 3 controls the S3 switch and bit 2 controls the S2 switch shown in Figure 35-28. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0,0. Other enhanced modes are also possible, but not regarded as typical usage modes.
		0	Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default).
		1h	Active low complementary (ALC) mode. EPWMxA is inverted.
		2h	Active high complementary (AHC). EPWMxB is inverted.
		3h	Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.
1-0	OUT_MODE		Dead-band Output Mode Control. Bit 1 controls the S1 switch and bit 0 controls the S0 switch shown in Figure 35-28. This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay.
		0	Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect.
		1h	Disable rising-edge delay. The EPWMxA signal from the action-qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].
		2h	The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by DBCTL[IN_MODE]. Disable falling-edge delay. The EPWMxB signal from the action-qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule.
		3h	Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].

POLSEL = 엑티브 하이 모드 이다. 내가 알고 있는 엑티브 하이모드는 클럭이 하이레벨일 때 동작하는 것을 말한다.

OUT_MODE - 데드밴드의 하이레벨신호 로우레벨 신호를 바이패스 한다.
바이패스는 신호를 일정 기간동안 지연시킨다는 뜻으로 새로운 신호가 들어오지 않고 마지막 신호를 설정한 시간동안 유지한다는 것을 말합니다.

DBRED 데드라인의 하이레벨 신호를 지연할 카운터를 설정합니다 110 이므로 0.000110 초 동안 지연한다는 것을 말하며 이는 원래 정현파로 들어오는 신호를 구형파로 만들어주는것을 의미합니다.
DBFED 위와 마찬가지로 로우레벨 신호를 지연할 카운터를 설정합니다.

PCCTL (PWM 에 들어가는 클럭 컨트롤인지????)

```
etpwmREG1->PCCTL = ((uint16)((uint16)0U << 0U)     /*
Enable/Disable chopper module */
         | (uint16)((uint16)0U << 1U)
         | (uint16)((uint16)3U << 8U)
         | (uint16)((uint16)0U << 5U));
```

0 번 =0 , 1 번 = 0 , 8 번 = 3, 5 번 = 0
데이터 시트를 확인합니다.

CHPEN = 0
PWM-chopping Enable. 해주는 비트이다 0 으로 되있기 때문에
disable 한다.

OSHTWTH 펄스 즉 하이레벨의 폭을 조정한다.
VCLK3 = 1MHz
1Mhz / 8 wide (100 MHz 에서 80 ns 면 1Mhz 에는서 8 마이크로 세컨드이다)
듀티비는 50 퍼센트로 설정된다.

Figure 35-90. PWM-Chopper Control Register (PCCTL) [offset = 3Eh]

15	11	10	8
Reserved		CHPDUTY	
R-0		R/W-0	

7	5	4	1	0
CHPFREQ		OSHTWTH		CHPEN
R/W-0		R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35-50. PWM-Chopper Control Register (PCCTL) Bit Descriptions

Bits	Name	Value	Description
15-11	Reserved	0	Reserved
10-8	CHPDUTY		Chopping Clock Duty Cycle.
		0	Duty = 1/8 (12.5%)
		1h	Duty = 2/8 (25.0%)
		2h	Duty = 3/8 (37.5%)
		3h	Duty = 4/8 (50.0%)
		4h	Duty = 5/8 (62.5%)
		5h	Duty = 6/8 (75.0%)
		6h	Duty = 7/8 (87.5%)
		7h	Reserved
7-5	CHPFREQ		Chopping Clock Frequency.
		0	Divide by 1 (no prescale, = 12.5 MHz at 100 MHz VCLK3)
		1h	Divide by 2 (6.25 MHz at 100 MHz VCLK3)
		2h	Divide by 3 (4.16 MHz at 100 MHz VCLK3)
		3h	Divide by 4 (3.12 MHz at 100 MHz VCLK3)
		4h	Divide by 5 (2.50 MHz at 100 MHz VCLK3)
		5h	Divide by 6 (2.08 MHz at 100 MHz VCLK3)
		6h	Divide by 7 (1.78 MHz at 100 MHz VCLK3)
		7h	Divide by 8 (1.56 MHz at 100 MHz VCLK3)
4-1	OSHTWTH		One-Shot Pulse Width.
		0	1 x VCLK3 / 8 wide (= 80 nS at 100 MHz VCLK3)
		1h	2 x VCLK3 / 8 wide (= 160 nS at 100 MHz VCLK3)
		2h	3 x VCLK3 / 8 wide (= 240 nS at 100 MHz VCLK3)
		3h	4 x VCLK3 / 8 wide (= 320 nS at 100 MHz VCLK3)
		4h	5 x VCLK3 / 8 wide (= 400 nS at 100 MHz VCLK3)
		5h	6 x VCLK3 / 8 wide (= 480 nS at 100 MHz VCLK3)
		6h	7 x VCLK3 / 8 wide (= 560 nS at 100 MHz VCLK3)
		7h	8 x VCLK3 / 8 wide (= 640 nS at 100 MHz VCLK3)
		8h	9 x VCLK3 / 8 wide (= 720 nS at 100 MHz VCLK3)
		9h	10 x VCLK3 / 8 wide (= 800 nS at 100 MHz VCLK3)
		Ah	11 x VCLK3 / 8 wide (= 880 nS at 100 MHz VCLK3)
		Bh	12 x VCLK3 / 8 wide (= 960 nS at 100 MHz VCLK3)
		Ch	13 x VCLK3 / 8 wide (= 1040 nS at 100 MHz VCLK3)
		Dh	14 x VCLK3 / 8 wide (= 1120 nS at 100 MHz VCLK3)
		Eh	15 x VCLK3 / 8 wide (= 1200 nS at 100 MHz VCLK3)
		Fh	16 x VCLK3 / 8 wide (= 1280 nS at 100 MHz VCLK3)
0	CHPEN		PWM-chopping Enable.
		0	Disable (bypass) PWM chopping function.
		1	Enable chopping function.

그 밑에 Trip 과 interrupt 는 사용하지 않으므로 다 0 으로 셋팅하고 끝난다.