TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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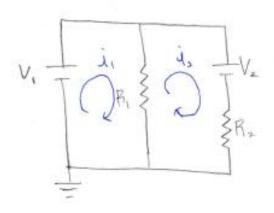
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1~2) 망전류, 마디 전압법

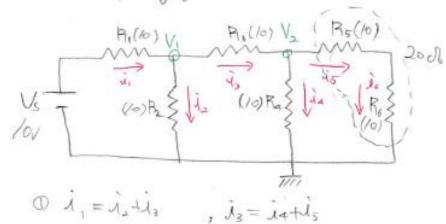
이 망전류



$$\mathbb{O} V_1 = (\tilde{\lambda}_1 - \tilde{\lambda}_2) R_1$$

$$Q - V_2 - \lambda_2 R_2 = \lambda_3 R_1$$

이 와디 전했병



$$\frac{V_1 - V_2}{P_{18}} = \frac{V_2}{P_{18}} + \frac{V_2}{26}$$

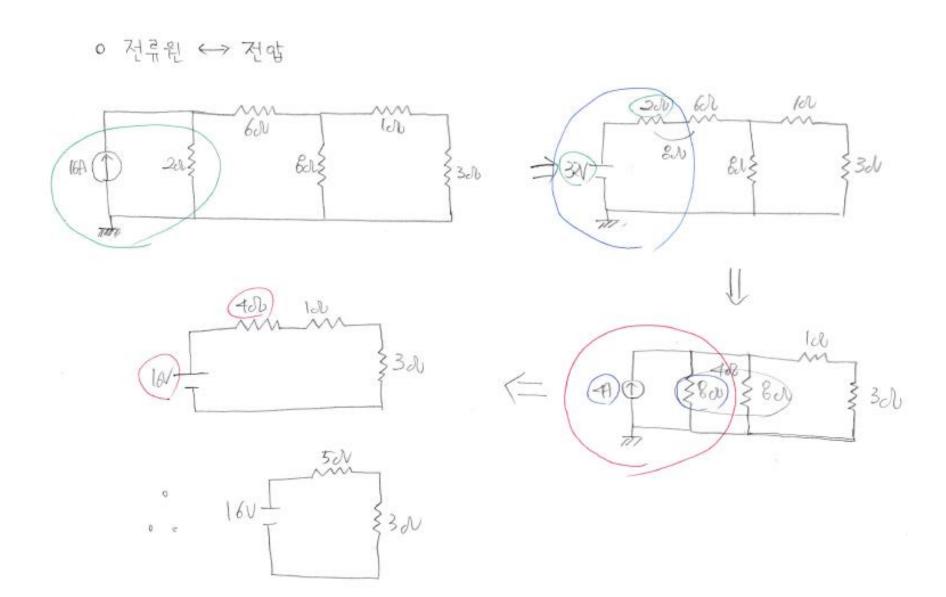
③
$$V_5 = 3U_1 - V_2$$

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$$V_5 = 3V_1 - V_2$$
 , $2V_1 - 2V_2 = 2V_2 + V_2 \Rightarrow V_1 = \frac{5}{2}V_2$

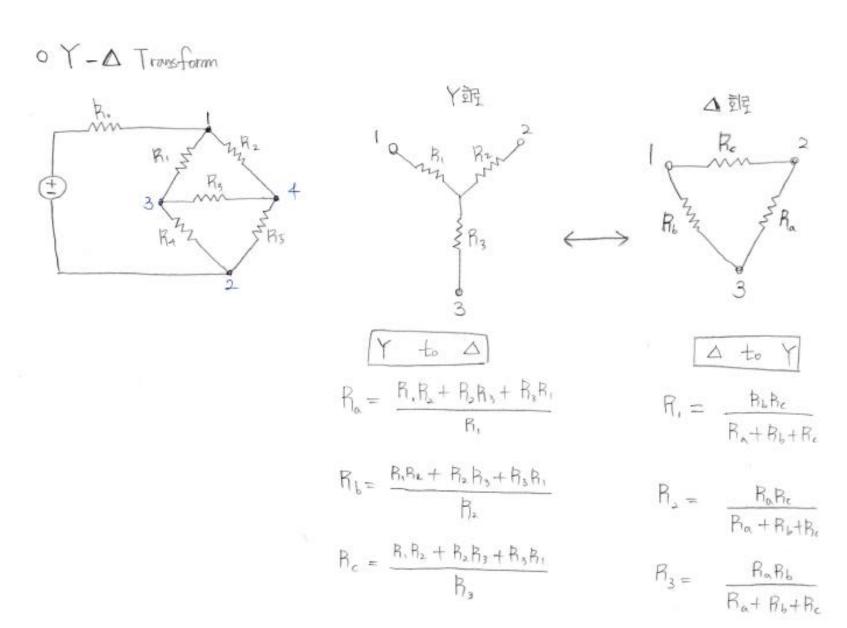
$$0 = \frac{15}{2}V_2 - V_2$$

$$=\frac{13}{2}V_2$$
 ., $V_2 = \frac{26}{13}V$, $V_1 = \frac{50}{13}V$

3) 전류원 <-> 전압원

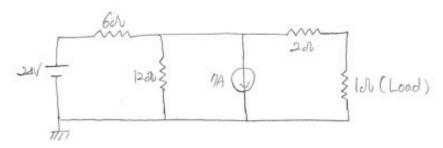


4) Y to Delta Transformation

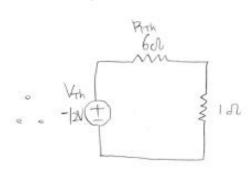


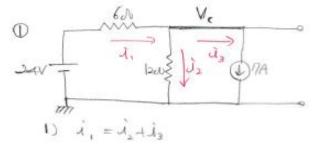
5) Thevenin 등가회로 1

OTherenin 号外强 1



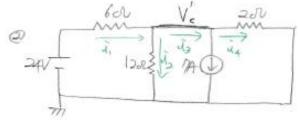
- ① 테브네 전에는 부하되로를 개성하여 연는다.
- @ 테브너 지하은 부터를 지킨 Short 라너 구함





$$\Rightarrow \frac{24 - V_c}{6} = \frac{V_c}{12} + 7$$

3)
$$3V_c = -36$$
 ... $V_c = -12 = V_{Th}$

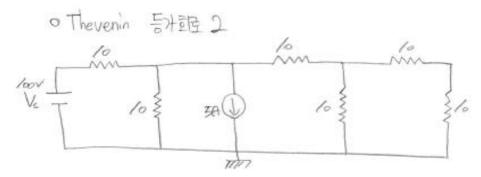


1)
$$\hat{\lambda}_1 = \hat{\lambda}_2 + \hat{\lambda}_3 + \hat{\lambda}_4$$

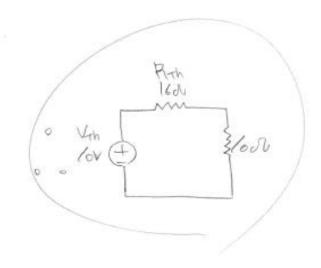
2)
$$\frac{24-V_e'}{6} = \frac{V_e'}{12} + 7 + \frac{V_e'}{2} = 48 - 2V_e' = V_e' + 84 + 6V_e'$$

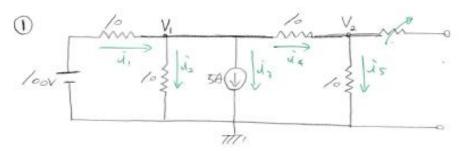
$$^{\circ}$$
. $R_{Th} = \frac{-12}{-2} = 60$

5) Thevenin 등가회로 2

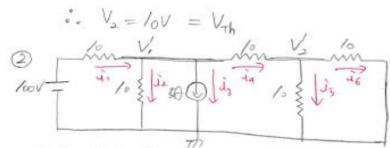


- ① 터브비 진약은 부하起를 개방하여 연는다.
- @ 터보냉 저항은 부터를 지원 Sharl 라이 구함.





2)
$$\frac{100-V_1}{10} = \frac{V_1}{10} + 5 + \frac{V_1 - V_2}{10}$$
, $\frac{V_1 - V_2}{10} = \frac{V_2}{10} \Rightarrow V_1 = 2V_2$
 $\Rightarrow 50 = 3V_1 - V_2$



2)
$$\frac{100-V'_1}{10} = \frac{V'_1}{10} + \frac{5}{10} + \frac{V'_1-V'_2}{10}$$
, $\frac{V'_1-V'_2}{10} = \frac{V'_2}{10} + \frac{V'_2}{10} \Rightarrow V_1 = 3V_2$
=) $50 = 3V_1 - V_2$
 $V_2 = \frac{50}{8}V$ ° $R_{Th} = \frac{8}{5} \times 10 = 160V$