TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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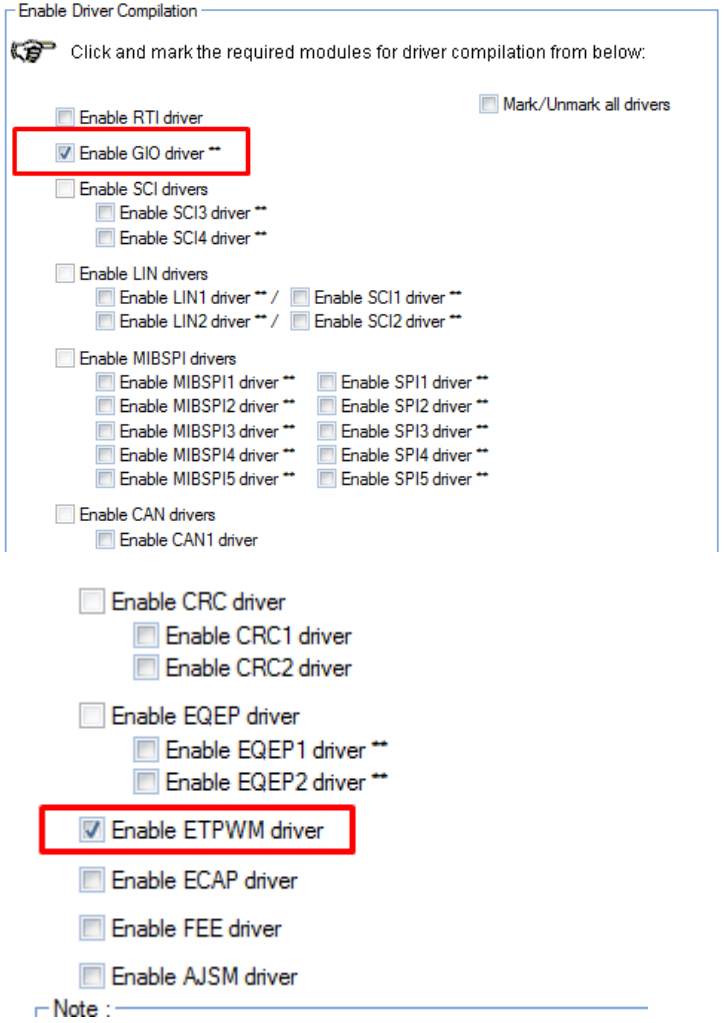
목차

4. Cortex-R5F Hercules Safety MCU - (etPWM 설정)

❖ 모터를 돌리려면 동작 주파수 50hz를 맞추기 위해서 GCM에서 PLL을 조정해야 함.

<1>



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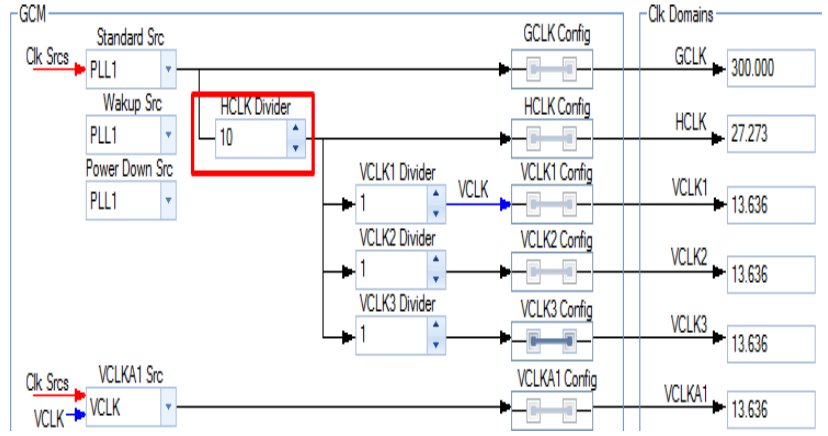
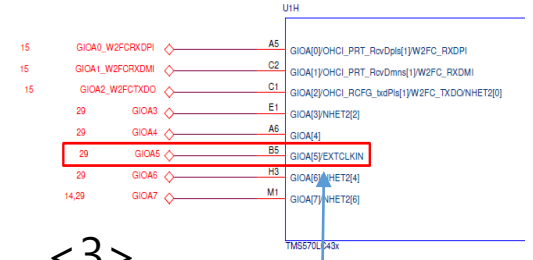
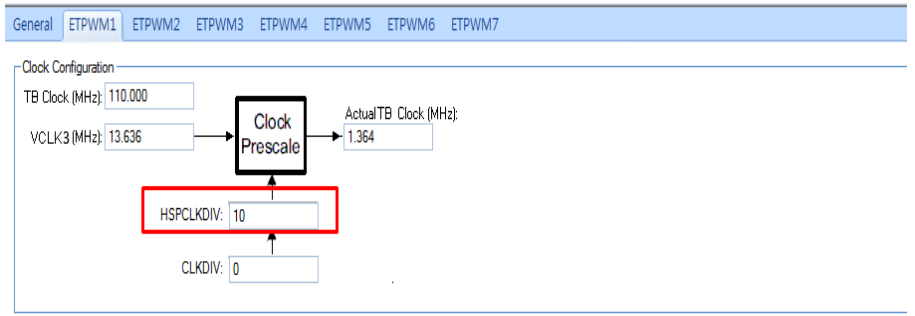
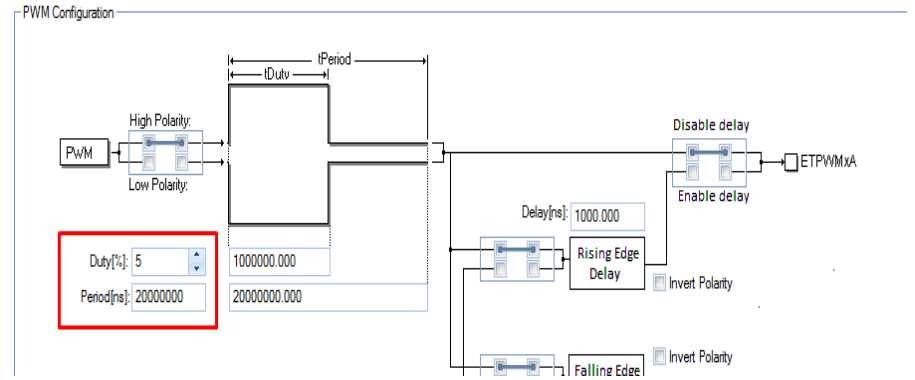


<3>







4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 1)

```c
#include "HL_sys_common.h"
#include "HL_system.h"
#include "HL_etpwm.h"

int idx = 0;
uint32 value =0;
uint32 duty_arr[6] = {1000, 2000, 1400, 1600, 1800, 20000};

void pwmSet(void);
void delay(uint32);

int main(void)
{
    etpwmInit();
    etpwmStartTBCLK();
    delay(10000);
    for(;;){
        pwmSet();
        delay(10000000);
    }
    return 0;
}
void delay(uint32 delay){
    int i;
    for(i =0; i<delay; i++);
}
void pwmSet(void){
    value = duty_arr[ idx % 6 ];
    idx ++;
    etpwmSetCmpA(etpwmREG1, value);
}
```

```c
void etpwmInit(void)
{
/* USER CODE BEGIN (1) */
/* USER CODE END */

    /** @b initialize @b ETPWM1 */

    /** - Sets high speed time-base clock prescale bits */
    etpwmREG1->TBCTL = (uint16)5U << 7U;
```

ePWM Registers www.ti.com

35.4.1.2 Time-Base Control Register (TBCTL)

Figure 35-64. Time-Base Control Register (TBCTL) [offset = 02h]

15	14	13	12	11	10	9	8
FREE	SOFT	PHSDIR	CLKDIV			HSPCLKDIV	
R/W-0	R/W-0	R/W-0	R/W-0			R/W-0	

7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W-1	R/W-0	R/W-0		R/W-0	R/W-0	R/W-3h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 35-24. Time-Base Control Register (TBCTL) Field Descriptions

Bit	Field	Value	Description
15-14	FREE, SOFT		Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events:
		0	Stop after the next time-base counter increment or decrement.
		1h	Stop when counter completes a whole cycle: • Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) • Down-count mode: stop when the time-base counter = 0x0000 (TBCTR = 0x0000) • Up-down-count mode: stop when the time-base counter = 0x0000 (TBCTR = 0x0000)
		2h-3h	Free run
13	PHSDIR		Phase Direction Bit. This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (TBCTR) will count after a synchronization event occurs and a new phase value is loaded from the phase (TBPHS) register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored.
		0	Count down after the synchronization event.
		1	Count up after the synchronization event.
12-10	CLKDIV		Time-base Clock Prescale Bits. These bits determine part of the time-base clock prescale value: TBCLK = VCLK3 / (HSPCLKDIV × CLKDIV)
		0	/1 (default on reset)
		1h	/2
		2h	/4
		3h	/8
		4h	/16
		5h	/32
		6h	/64
		7h	/128
9-7	HSPCLKDIV		High Speed Time-base Clock Prescale Bits. These bits determine part of the time-base clock prescale value: TBCLK = VCLK3 / (HSPCLKDIV × CLKDIV)
		0	/1
		1h	/2 (default on reset)
		2h	/4
		3h	/6
		4h	/8
		5h	/10
		6h	/12
		7h	/14

Table 35-24. Time-Base Control Register (TBCTL) Field Descriptions (continued)

Bit	Field	Value	Description
6	SWFSYNC		Software Forced Synchronization Pulse.
		0	Writing a 0 has no effect and reads always return a 0.
		1	Writing a 1 forces a one-time synchronization pulse to be generated. This event is ORed with the EPWMxSYNCI input of the ePWM module. SWFSYNC is valid (operates) only when EPWMxSYNCI is selected by SYNCOSEL = 00.
5-4	SYNCOSEL		Synchronization Output Select. These bits select the source of the EPWMxSYNCO signal.
		0	EPWMxSYNC
		1h	CTR = zero: Time-base counter equal to zero (TBCTR = 0x0000)
		2h	CTR = CMPB : Time-base counter equal to counter-compare B (TBCTR = CMPB)
		3h	Disable EPWMxSYNCO signal
3	PRDLD		Active Period Register Load From Shadow Register Select.
		0	The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero. A write or read to the TBPRD register accesses the shadow register.
		1	Load the TBPRD register immediately without using a shadow register. A write or read to the TBPRD register directly accesses the active register.
2	PHSEN		Counter Register Load From Phase Register Enable.
		0	Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS).
		1	Load the time-base counter with the phase register when an EPWMxSYNCI input signal occurs or when a software synchronization is forced by the SWFSYNC bit, or when a digital compare sync event occurs.
1-0	CTRMODE		Counter Mode. The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows:
		0	Up-count mode
		1h	Down-count mode
		2h	Up-down-count mode
		3h	Stop-freeze counter operation (default on reset)

9-7 bit set 5h : TBCLK = VCLK3 / 10

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0	
TBCTL:	0000	0000	0000	0000	0010	0010	1000	0000	나머지는 default setting

4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 2)

```
/** - Sets time period or frequency for ETPWM block both PWMA and PWMB*/
etpwmREG1->TBPRD = 27279U;
```

TBPRD의 임계치는 2^16 = 65536

만약에 TBPRD 셋팅을 위에 임계치를 초과하면, 주파수 설정이 이상하게 됨.

```
/** - Setup the duty cycle for PWMA */
etpwmREG1->CMPA = 1364U;

/** - Setup the duty cycle for PWMB */
etpwmREG1->CMPB = 13640U;
```

TBCTR과 계속 비교하고, 값이 같아지면 둘이 같아 졌다는 것을 AQCTLA에게 보낸다.

35.4.1.4 Time-Base Period Register (TBPRD)

Figure 35-66. Time-Base Period Register (TBPRD) [offset = 08h]

15	0
TBPRD	
R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 35-26. Time-Base Period Register (TBPRD) Field Descriptions

Bits	Name	Description
15-0	TBPRD	These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. • If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals 0. • If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. • The active and shadow registers share the same memory map address.

35.4.2.2 Counter-Compare A Register (CMPA)

Figure 35-69. Counter-Compare A Register (CMPA) [offset = 10h]

15	0
CMPA	
R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 35-29. Counter-Compare A Register (CMPA) Field Descriptions

Bits	Name	Description
15-0	CMPA	The value in the active CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: • Do nothing; the event is ignored. • Clear: Pull the EPWMxA and/or EPWMxB signal low. • Set: Pull the EPWMxA and/or EPWMxB signal high. • Toggle the EPWMxA and/or EPWMxB signal. Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed. • If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. • Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. • If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. • In either mode, the active and shadow registers share the same memory map address.

4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 3)

```
/** - Force EPWMxA output high when counter reaches zero and low when counter reaches Compare A v
etpwmREG1->AQCTLA = ((uint16)((uint16)ActionQual_Set   << 0U)  // 2 << 0
                   | (uint16)((uint16)ActionQual_Clear << 4U));  // 1 << 4

/** - Force EPWMxB output high when counter reaches zero and low when counter reaches Compare B v
etpwmREG1->AQCTLB = ((uint16)((uint16)ActionQual_Set   << 0U)
                   | (uint16)((uint16)ActionQual_Clear << 8U));
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
AQCTLA :	0000	0000	0000	0000	0000	0000	0001	0010

1-0 bit : 2h , Set: force EPWMxA output high

5-4 bit : 1h , Clear: force EPWMxA output low

CMPA 값이 1364에 이르면, low
그전까지는 High로 output을 생성~!

35.4.3 Action-Qualifier Submodule Registers

35.4.3.1 Action-Qualifier Output A Control Register (AQCTLA)

Figure 35-71. Action-Qualifier Output A Control Register (AQCTLA) [offset = 14h]

15 ... 12	11	10	9	8
Reserved	CBD		CBU	
R-0	R/W-0		R/W-0	

7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 35-31. Action-Qualifier Output A Control Register (AQCTLA) Field Descriptions

Bits	Name	Value	Description
15-12	Reserved	0	Reserved
11-10	CBD		Action when the time-base counter equals the active CMPB register and the counter is decrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
9-8	CBU		Action when the counter equals the active CMPB register and the counter is incrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
7-6	CAD		Action when the counter equals the active CMPA register and the counter is decrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5-4	CAU		Action when the counter equals the active CMPA register and the counter is incrementing.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3-2	PRD		Action when the counter equals the period. Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
1-0	ZRO		Action when counter equals zero. Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.
		0	Do nothing (action is disabled).
		1h	Clear: force EPWMxA output low.
		2h	Set: force EPWMxA output high.
		3h	Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

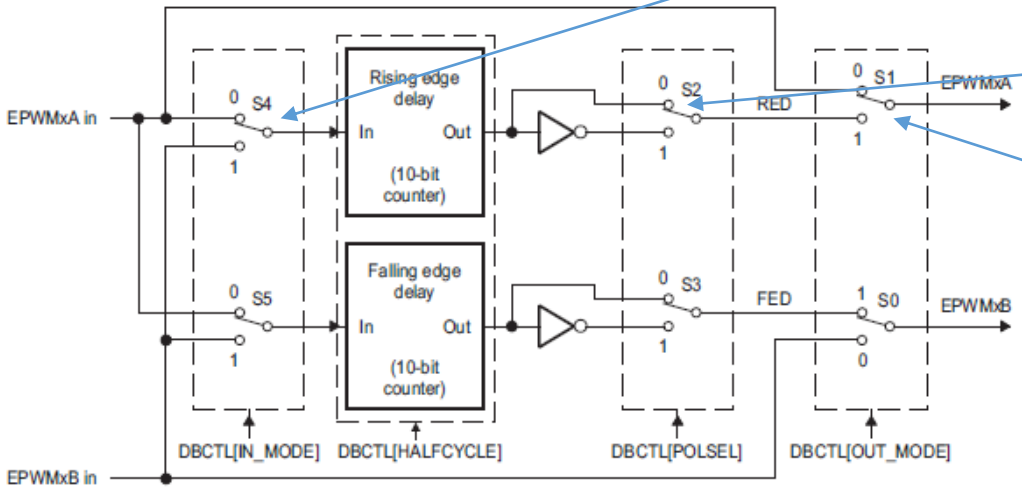
4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 4)

```
/** - Mode setting for Dead Band Module
*     -Select the input mode for Dead Band Module
*     -Select the output mode for Dead Band Module
*     -Select Polarity of the output PWMs
*/
etpwmREG1->DBCTL = ((uint16)((uint16)0U << 5U)    /* Source for Falling edge delay(0-PWMA, 1-PWMB
                  | (uint16)((uint16)0u << 4U)    /* Source for Rising edge delay(0-PWMA, 1-PWMB)
                  | (uint16)((uint16)0U << 3U)    /* Enable/Disable EPWMxB invert       */
                  | (uint16)((uint16)0U << 2U)    /* Enable/Disable EPWMxA invert       */
                  | (uint16)((uint16)0U << 1U)    /* Enable/Disable Rising Edge Delay   */
                  | (uint16)((uint16)0U << 0U));  /* Enable/Disable Falling Edge Delay  */
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
DBCTL :	0000	0000	0000	0000	0000	0000	0000	0000

Dead band 모듈 셋팅

Figure 35-28. Configuration Options for the Dead-Band Submodule



35.4.4 Dead-Band Submodule Registers

35.4.4.1 Dead-Band Generator Control Register (DBCTL)

Figure 35-75. Dead-Band Generator Control Register (DBCTL) [offset = 1Ch]

15	14	8
HALFCYCLE	Reserved	
R/W-0	R-0	

7	6	5	4	3	2	1	0
Reserved		IN_MODE		POLSEL		OUT_MODE	
R-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35-35. Dead-Band Generator Control Register (DBCTL) Field Descriptions

Bits	Name	Value	Description
15	HALFCYCLE		Half Cycle Clocking Enable Bit.
		0	Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate.
		1	Half cycle clocking enabled. The dead-band counters are clocked at TBCLK × 2.
14-6	Reserved	0	Reserved
5-4	IN_MODE		Dead Band Input Mode Control. Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown in Figure 35-28. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays.
		0	EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.
		1h	EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.
		2h	EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.
		3h	EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.
3-2	POLSEL		Polarity Select Control. Bit 3 controls the S3 switch and bit 2 controls the S2 switch shown in Figure 35-28. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0,0. Other enhanced modes are also possible, but not regarded as typical usage modes.
		0	Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default).
		1h	Active low complementary (ALC) mode. EPWMxA is inverted.
		2h	Active high complementary (AHC). EPWMxB is inverted.
		3h	Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.

Table 35-35. Dead-Band Generator Control Register (DBCTL) Field Descriptions (continued)

Bits	Name	Value	Description
1-0	OUT_MODE		Dead-band Output Mode Control. Bit 1 controls the S1 switch and bit 0 controls the S0 switch shown in Figure 35-28. This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay.
		0	Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect.
		1h	Disable rising-edge delay. The EPWMxA signal from the action-qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].
		2h	The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by DBCTL[IN_MODE]. Disable falling-edge delay. The EPWMxB signal from the action-qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule.
		3h	Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].

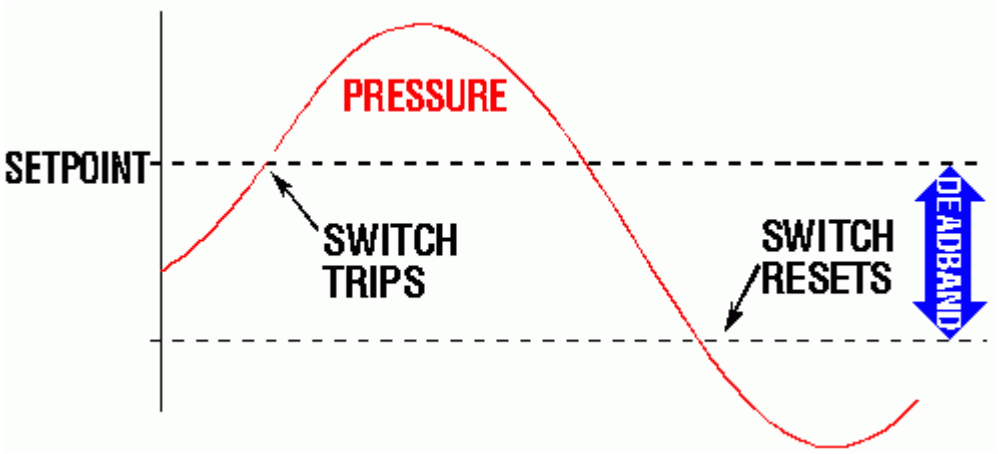
4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 5)

```
/** - Set the rising edge delay  */
etpwmREG1->DBRED = 110U;

/** - Set the falling edge delay  */
etpwmREG1->DBFED = 110U ;
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
DBRED :	0000	0000	0000	0000	0000	0000	0110	1110

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
DBFED :	0000	0000	0000	0000	0000	0000	0110	1110



35.4.4.3 Dead-Band Generator Rising Edge Delay Register (DBRED)

Figure 35-77. Dead-Band Generator Rising Edge Delay Register (DBRED) [offset = 22h]

15	10	9	8
Reserved		DEL	
R-0		R/W-0	

7	0
DEL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35-37. Dead-Band Generator Rising Edge Delay Register (DBRED) Field Descriptions

Bits	Name	Description
15-10	Reserved	Reserved
9-0	DEL	Rising Edge Delay Count. 10-bit counter.

35.4.4.2 Dead-Band Generator Falling Edge Delay Register (DBFED)

Figure 35-76. Dead-Band Generator Falling Edge Delay Register (DBFED) [offset = 20h]

15	10	9	8
Reserved		DEL	
R-0		R/W-0	

7	0
DEL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35-36. Dead-Band Generator Falling Edge Delay Register (DBFED) Field Descriptions

Bits	Name	Description
15-10	Reserved	Reserved
9-0	DEL	Falling Edge Delay Count. 10-bit counter.

- ❖ 10 bit counter로 라이징 엣지와 폴링 엣지의 딜레이 용도로 사용 됨.
- ❖ dead band를 사용하여 사각파를 만듬.

4. Cortex-R5F Hercules Safety MCU – (etpwmInit() 분석 6)

```
/** - Enable the chopper module for ETPWMx
*     -Sets the One shot pulse width in a chopper modulated wave
*     -Sets the dutycycle for the subsequent pulse train
*     -Sets the period for the subsequent pulse train
*/
etpwmREG1->PCCTL = ((uint16)((uint16)0U << 0U)    /* Enable/Disable chopper module */
                  | (uint16)((uint16)0U << 1U)    /* One-shot Pulse Width */
                  | (uint16)((uint16)3U << 8U)    /* Chopping Clock Duty Cycle */
                  | (uint16)((uint16)0U << 5U));  /* Chopping Clock Frequency */
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
PCCTL :	0000	0000	0000	0000	0000	0011	0000	0000

- 10-8 bit set 3h : duty = 50%
- 나머지는 기본 0으로 셋팅

Table 35-50. PWM-Chopper Control Register (PCCTL) Bit Descriptions (continued)

Bits	Name	Value	Description
4-1	OSHTWTH		One-Shot Pulse Width.
		0	1 x VCLK3 / 8 wide (= 80 nS at 100 MHz VCLK3)
		1h	2 x VCLK3 / 8 wide (= 160 nS at 100 MHz VCLK3)
		2h	3 x VCLK3 / 8 wide (= 240 nS at 100 MHz VCLK3)
		3h	4 x VCLK3 / 8 wide (= 320 nS at 100 MHz VCLK3)
		4h	5 x VCLK3 / 8 wide (= 400 nS at 100 MHz VCLK3)
		5h	6 x VCLK3 / 8 wide (= 480 nS at 100 MHz VCLK3)
		6h	7 x VCLK3 / 8 wide (= 560 nS at 100 MHz VCLK3)
		7h	8 x VCLK3 / 8 wide (= 640 nS at 100 MHz VCLK3)
		8h	9 x VCLK3 / 8 wide (= 720 nS at 100 MHz VCLK3)
		9h	10 x VCLK3 / 8 wide (= 800 nS at 100 MHz VCLK3)
		Ah	11 x VCLK3 / 8 wide (= 880 nS at 100 MHz VCLK3)
		Bh	12 x VCLK3 / 8 wide (= 960 nS at 100 MHz VCLK3)
		Ch	13 x VCLK3 / 8 wide (= 1040 nS at 100 MHz VCLK3)
		Dh	14 x VCLK3 / 8 wide (= 1120 nS at 100 MHz VCLK3)
		Eh	15 x VCLK3 / 8 wide (= 1200 nS at 100 MHz VCLK3)
		Fh	16 x VCLK3 / 8 wide (= 1280 nS at 100 MHz VCLK3)
0	CHPEN		PWM-chopping Enable.
		0	Disable (bypass) PWM chopping function.
		1	Enable chopping function.

35.4.7 PWM-Chopper Submodule Register

35.4.7.1 PWM-Chopper Control Register (PCCTL)

Figure 35-90. PWM-Chopper Control Register (PCCTL) [offset = 3Eh]

15	11	10	8
Reserved		CHPDUTY	
R-0		R/W-0	

7	5	4	1	0
CHPFREQ		OSHTWTH		CHPEN
R/W-0		R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35-50. PWM-Chopper Control Register (PCCTL) Bit Descriptions

Bits	Name	Value	Description
15-11	Reserved	0	Reserved
10-8	CHPDUTY		Chopping Clock Duty Cycle.
		0	Duty = 1/8 (12.5%)
		1h	Duty = 2/8 (25.0%)
		2h	Duty = 3/8 (37.5%)
		3h	Duty = 4/8 (50.0%)
		4h	Duty = 5/8 (62.5%)
		5h	Duty = 6/8 (75.0%)
		6h	Duty = 7/8 (87.5%)
		7h	Reserved
7-5	CHPFREQ		Chopping Clock Frequency.
		0	Divide by 1 (no prescale, = 12.5 MHz at 100 MHz VCLK3)
		1h	Divide by 2 (6.25 MHz at 100 MHz VCLK3)
		2h	Divide by 3 (4.16 MHz at 100 MHz VCLK3)
		3h	Divide by 4 (3.12 MHz at 100 MHz VCLK3)
		4h	Divide by 5 (2.50 MHz at 100 MHz VCLK3)
		5h	Divide by 6 (2.08 MHz at 100 MHz VCLK3)
		6h	Divide by 7 (1.78 MHz at 100 MHz VCLK3)
		7h	Divide by 8 (1.56 MHz at 100 MHz VCLK3)

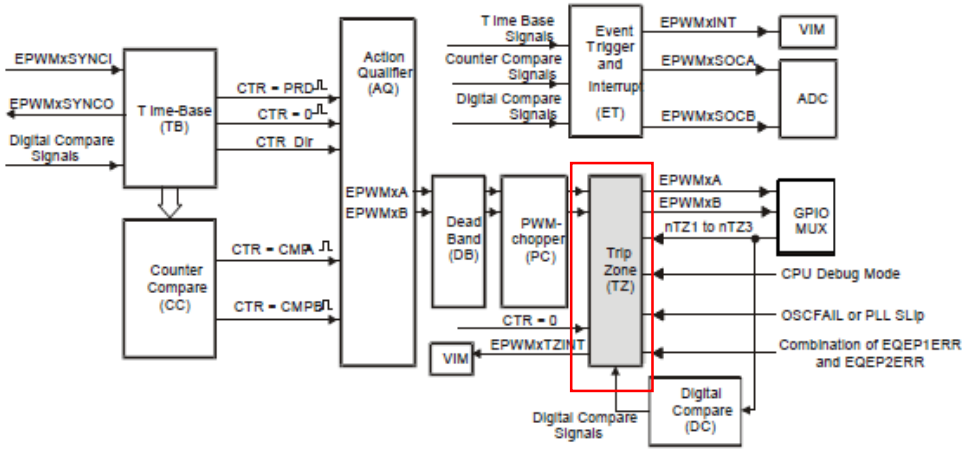
4. Cortex-R5F Hercules Safety MCU – (etpwmInit() 분석 7)

35.2.7 Trip-Zone (TZ) Submodule

Figure 35-35 shows how the trip-zone (TZ) submodule fits within the ePWM module.

Each ePWM module is connected to six TZn signals (TZ1 to TZ6). TZ1 to TZ3 are sourced from the GPIO mux. TZ4 is sourced from a combination of EQEP1ERR and EQEP2ERR signals. TZ5 is connected to the system oscillator or PLL clock fail logic, and TZ6 is sourced from the debug mode halt indication output from the CPU. These signals indicate fault or trip conditions, and the ePWM outputs can be programmed to respond accordingly when faults occur.

Figure 35-35. Trip-Zone Submodule



35.2.7.1 Purpose of the Trip-Zone Submodule

The key functions of the Trip-Zone submodule are:

- Trip inputs TZ1 to TZ6 are mapped to all ePWM modules.
- Upon a fault indication, either no action is taken or the ePWM outputs EPWMxA and EPWMxB can be forced to one of the following:
  - High
  - Low
  - High-impedance
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Support for digital compare tripping (DC) based on state of on-chip analog comparator module outputs and/or TZ1 to TZ3 signals.
- Each trip-zone input and digital compare (DC) submodule DCAEVT1/2 or DCBEVT1/2 force event can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone input.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if it is not required.

Each ePWM module is connected to six TZn signals (TZ1 to TZ6) that are sourced from the general-purpose input/output (GPIO) MUX. These signals indicate external fault or trip conditions, and the ePWM outputs can be programmed to respond accordingly when faults occur.

❖ Trip – Zone 은 epwm신호선들과 맵핑되어 있고

일반적으로는 GPIO MUX 신호선이지만,
외부 fault나 trip상황에 반응하도록 프로그램되어 있다.

4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 8)

```
/** - Set trip source enable */
etpwmREG1->TZSEL = 0x0000U    /** - Enable/Disable TZ1 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ2 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ3 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ4 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ5 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ6 as a one-shot trip source */
                 | 0x0000U    /** - Enable/Disable TZ1 as a CBC trip source      */
                 | 0x0000U    /** - Enable/Disable TZ2 as a CBC trip source      */
                 | 0x0000U    /** - Enable/Disable TZ3 as a CBC trip source      */
                 | 0x0000U    /** - Enable/Disable TZ4 as a CBC trip source      */
                 | 0x0000U    /** - Enable/Disable TZ5 as a CBC trip source      */
                 | 0x0000U;   /** - Enable/Disable TZ6 as a CBC trip source      */
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
TZSEL :	0000	0000	0000	0000	0000	0000	0000	0000

35.4.5.2 Trip-Zone Select Register (TZSEL)

Figure 35-79. Trip-Zone Select Register (TZSEL) [offset = 26h]

15	14	13	12	11	10	9	8
DCBEVT1	DCAEVT1	OSHT6	OSHT5	OSHT4	OSHT3	OSHT2	OSHT1
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 35-39. Trip-Zone Submodule Select Register (TZSEL) Field Descriptions

Bits	Name	Value	Description
One-Shot (OSHT) Trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this ePWM module. When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until the user clears the condition via the TZCLR register.			
15	DCBEVT1		Digital Compare Output B Event 1 Select.
		0	Disable DCBEVT1 as one-shot-trip source for this ePWM module.
		1	Enable DCBEVT1 as one-shot-trip source for this ePWM module.
14	DCAEVT1		Digital Compare Output A Event 1 Select.
		0	Disable DCAEVT1 as one-shot-trip source for this ePWM module.
		1	Enable DCAEVT1 as one-shot-trip source for this ePWM module.
13	OSHT6		Trip-zone 6 ($\overline{TZ6}$) Select.
		0	Disable $\overline{TZ6}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ6}$ as a one-shot trip source for this ePWM module.
12	OSHT5		Trip-zone 5 ($\overline{TZ5}$) Select.
		0	Disable $\overline{TZ5}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ5}$ as a one-shot trip source for this ePWM module.
11	OSHT4		Trip-zone 4 ($\overline{TZ4}$) Select.
		0	Disable $\overline{TZ4}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ4}$ as a one-shot trip source for this ePWM module.
10	OSHT3		Trip-zone 3 ($\overline{TZ3}$) Select.
		0	Disable $\overline{TZ3}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ3}$ as a one-shot trip source for this ePWM module.
9	OSHT2		Trip-zone 2 ($\overline{TZ2}$) Select.
		0	Disable $\overline{TZ2}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ2}$ as a one-shot trip source for this ePWM module.
8	OSHT1		Trip-zone 1 ($\overline{TZ1}$) Select.
		0	Disable $\overline{TZ1}$ as a one-shot trip source for this ePWM module.
		1	Enable $\overline{TZ1}$ as a one-shot trip source for this ePWM module.
Cycle-by-Cycle (CBC) Trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this ePWM module. When the event occurs, the action defined in the TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.			
7	DCBEVT2		Digital Compare Output B Event 2 Select.
		0	Disable DCBEVT2 as a CBC trip source for this ePWM module.
		1	Enable DCBEVT2 as a CBC trip source for this ePWM module.
6	DCAEVT2		Digital Compare Output A Event 2 Select.
		0	Disable DCAEVT2 as a CBC trip source for this ePWM module.
		1	Enable DCAEVT2 as a CBC trip source for this ePWM module.

4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 9)

```
/** - Set interrupt enable */
etpwmREG1->TZEINT = 0x0000U     /** - Enable/Disable Digital Comparator Output A Event 1  */
                  | 0x0000U     /** - Enable/Disable Digital Comparator Output A Event 2  */
                  | 0x0000U     /** - Enable/Disable Digital Comparator Output A Event 1  */
                  | 0x0000U     /** - Enable/Disable Digital Comparator Output A Event 2  */
                  | 0x0000U     /** - Enable/Disable one-shot interrupt generation        */
                  | 0x0000U;    /** - Enable/Disable cycle-by-cycle interrupt generation  */
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
TZEINT :	0000	0000	0000	0000	0000	0000	0000	0000

35.4.5.3 Trip-Zone Enable Interrupt Register (TZEINT)

Figure 35-80. Trip-Zone Enable Interrupt Register (TZEINT) [offset = 28h]

15							8
Reserved							
R -0							

7	6	5	4	3	2	1	0
Reserved	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	Reserved
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 35-40. Trip-Zone Enable Interrupt Register (TZEINT) Field Descriptions

Bits	Name	Value	Description
15-3	Reserved	0	Reserved
6	DCBEVT2		Digital Comparator Output B Event 2 Interrupt Enable.
		0	Disabled
		1	Enabled
5	DCBEVT1		Digital Comparator Output B Event 1 Interrupt Enable.
		0	Disabled
		1	Enabled
4	DCAEVT2		Digital Comparator Output A Event 2 Interrupt Enable.
		0	Disabled
		1	Enabled
3	DCAEVT1		Digital Comparator Output A Event 1 Interrupt Enable.
		0	Disabled
		1	Enabled
2	OST		Trip-zone One-Shot Interrupt Enable.
		0	Disable one-shot interrupt generation.
		1	Enable Interrupt generation; a one-shot trip event will cause a EPWMx_TZINT VIM interrupt.
1	CBC		Trip-zone Cycle-by-Cycle Interrupt Enable.
		0	Disable cycle-by-cycle interrupt generation.
		1	Enable interrupt generation; a cycle-by-cycle trip event will cause an EPWMx_TZINT VIM interrupt.
0	Reserved	0	Reserved

4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 10)

35.2.7.4 Generating Trip Event Interrupts

Figure 35-36 and Figure 35-37 illustrate the trip-zone submodule control and interrupt logic, respectively. DCAEVT1/2 and DCBEVT1/2 signals are described in further detail in Section 35.2.9.

Figure 35-36. Trip-Zone Submodule Mode Control Logic

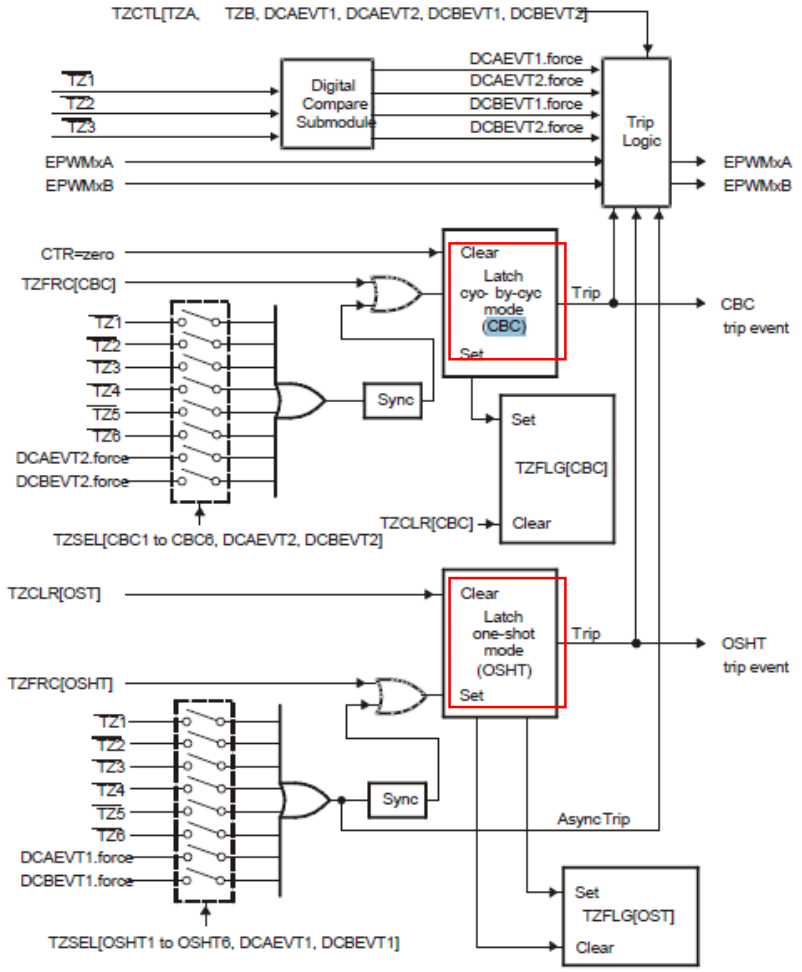
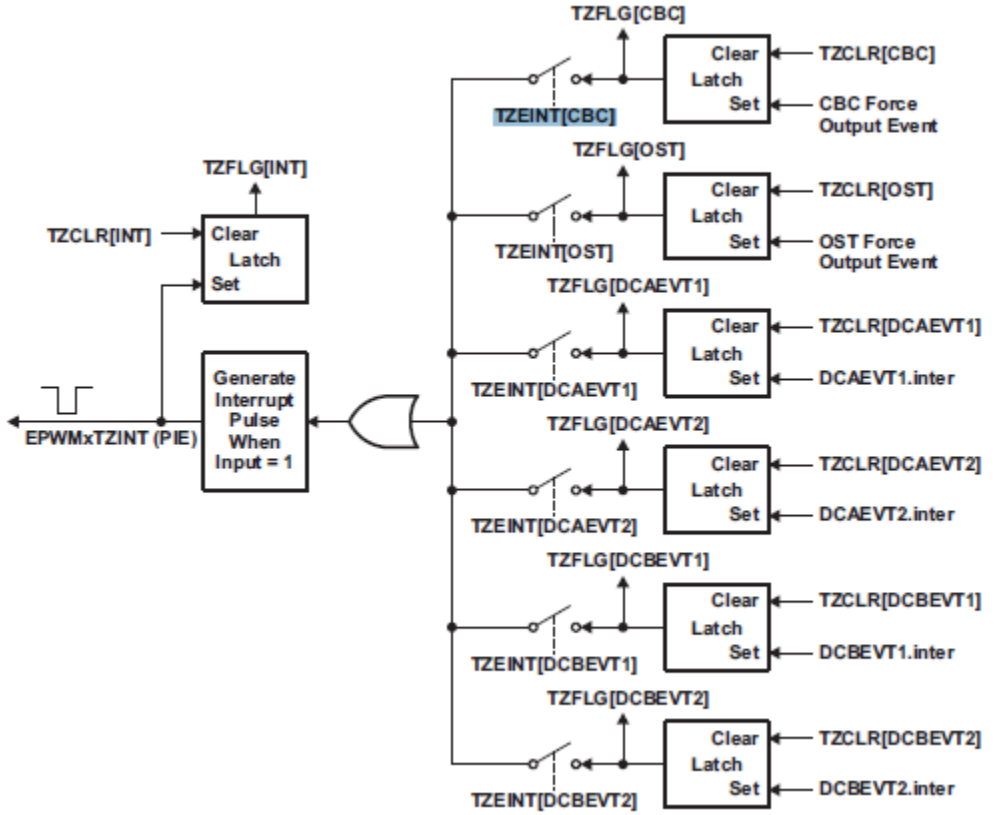


Figure 35-37. Trip-Zone Submodule Interrupt Logic



4. Cortex-R5F Hercules Safety MCU - (etpwmInit() 분석 11)

```
/** - Setup the frequency of the interrupt generation */
etpwmREG1->ETPS = 1U;


/** - Sets up the ADC SOC period */
etpwmREG1->ETPS |= ((uint16)((uint16)1U << 8U)
                 | (uint16)((uint16)1U << 12U));
```

	31~28	27~24	23~20	19~16	15~12	11~8	7~4	3~0
ETPS :	0000	0000	0000	0000	0001	0001	0000	0001

Table 35-47. Event-Trigger Prescale Register (ETPS) Field Descriptions (continued)

Bits	Name	Value	Description
3-2	INTCNT		ePWM Interrupt Event (EPWMx_INT) Counter Register. These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD].
		0	No events have occurred.
		1h	1 event has occurred.
		2h	2 events have occurred.
		3h	3 events have occurred.
1-0	INTPRD		ePWM Interrupt (EPWMx_INT) Period Select. These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled (ETSEL[INT] = 1). If the interrupt status flag is set from a previous interrupt (ETFLG[INT] = 1) then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared. Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented.
		0	Disable the interrupt event counter. No interrupt will be generated and ETFRC[INT] is ignored.
		1h	Generate an interrupt on the first event INTCNT = 01 (first event).
		2h	Generate interrupt on ETPS[INTCNT] = 1,0 (second event).
		3h	Generate interrupt on ETPS[INTCNT] = 1,1 (third event).

35.4.6.3 Event-Trigger Prescale Register (ETPS)

Figure 35-87. Event-Trigger Prescale Register (ETPS) [offset = 36h]

15-14	13-12	11-10	9-8
SOCBCNT	SOCBPRD	SOCACNT	SOCAPRD
R-0	R/W-0	R-0	R/W-0

7-4	3-2	1-0
Reserved	INTCNT	INTPRD
R-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35-47. Event-Trigger Prescale Register (ETPS) Field Descriptions

Bits	Name	Value	Description
15-14	SOCBCNT		ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Counter Register. These bits indicate how many selected ETSEL[SOCBSEL] events have occurred.
		0	No events have occurred.
		1h	1 event has occurred.
		2h	2 events have occurred.
		3h	3 events have occurred.
13-12	SOCBPRD		ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Period Select. These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCBEN] = 1). The SOCB pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCB] = 1). Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared.
		0	Disable the SOCB event counter. No EPWMxSOCB pulse will be generated.
		1h	Generate the EPWMxSOCB pulse on the first event: ETPS[SOCBCNT] = 0,1.
		2h	Generate the EPWMxSOCB pulse on the second event: ETPS[SOCBCNT] = 1,0.
		3h	Generate the EPWMxSOCB pulse on the third event: ETPS[SOCBCNT] = 1,1.
11-10	SOCACNT		ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Counter Register. These bits indicate how many selected ETSEL[SOCASEL] events have occurred.
		0	No events have occurred.
		1h	1 event has occurred.
		2h	2 events have occurred.
		3h	3 events have occurred.
9-8	SOCAPRD		ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Period Select. These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCAEN] = 1). The SOCA pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCA] = 1). Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared.
		0	Disable the SOCA event counter. No EPWMxSOCA pulse will be generated.
		1h	Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 0,1.
		2h	Generate the EPWMxSOCA pulse on the second event: ETPS[SOCACNT] = 1,0.
		3h	Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 1,1.
7-4	Reserved	0	Reserved