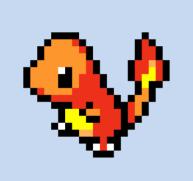
Xilinx Zynq FPGA TI DSP MCU 기반의 프로그래밍 및 회로 설계 전문가



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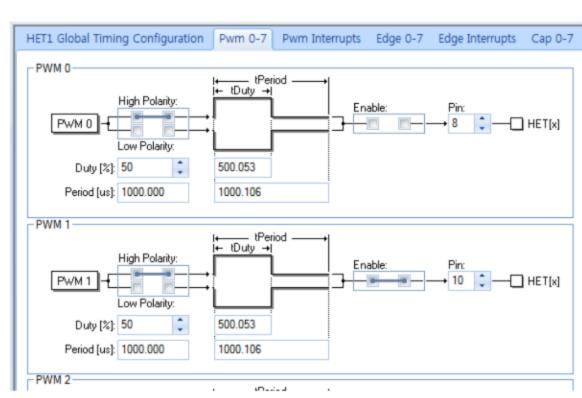
```
1 #include "HL sys common.h"
 2 #include "HL system.h"
 3 #include "HL_het.h"
 5 int main(void)
 6 {
       hetInit();
       while(1);
       return 0;
11 }
12
13
```

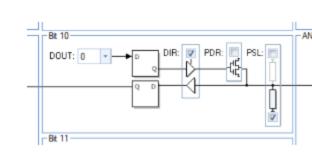
HetPWM

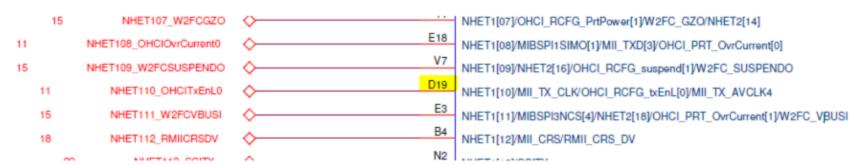
설정

☑ Enable HET drivers
☑ Enable HET1 driver **
⑤ Enable HET2 driver **

driver 설정







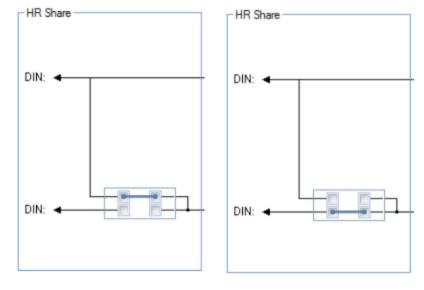


Table 23-73. Instruction Summary

Opcode

Ch

9h

Sub-Opcode

C[25:23] = 111, C[5] = 1

Cycles

1

2

1-3

Instruction Name

Angle Compare

Angle Count

Software Capture Word

Software Capture Word and Event Count

Bitwise Exclusive-Or and Shift

Abbreviation

ACMP

ACNT

WCAP

WCAPE

XOR

ADCNST	Add Constant	5h	-	2	
ADC	Add with Carry and Shift	4h	C[25:23] = 011, C5 = 1	1-3	
ADD	Add and Shift	4h	C[25:23] = 001, C5 = 1	1-3	
ADM32	Add Move 32	4h	C[25:23] = 000, C5 = 1	1-2	
AND	Bitwise AND and Shift	4h	C[25:23] = 010, C5 = 1	1-3	
APCNT	Angle Period Count	Eh	-	1-2	
BR	Branch	Dh	-	1	
CNT	Count	6h		1-2	
DADM64	Data Add Move 64	2h		2	
DJZ	Decrement and Jump if -zero	Ah	P[7:6] = 10	1	
ECMP	Equality Compare	Oh	C[6:5] = 00	1	
ECNT	Event Count	Ah	P[7:6] = 01	1	
MCMP	Magnitude Compare	Oh	C[6] = 1	1	
MOV32	Move 32	4h	C[5] = 0	1-2	
MOV64	Move 64	1h	-	1	
OR	Bitwise OR	4h	C[25:23] = 100, C5 = 1	1-3	
PCNT	Period/Pulse Count	7h	-	1	
PWCNT	Pulse Width Count	Ah	P[7:6] = 11	1	
RADM64	Register Add Move 64	3h		1	
RCNT	Ratio Count	Ah	P[7:6] = 00, P[0] = 1	3	
SBB	Subtract with Borrow and Shift	4h	C[25:23] =110, C[5] = 1	1-3	
SCMP	Sequence Compare	Oh	C[6:5] = 01	1	
SCNT	Step Count	Ah	P[7:6] = 00, P[0] = 0	3	
SHFT	Shift	Fh	C[3] = 0	1	
SUB	Subtract and Shift	4h	C[25:23] = 101, C[5] = 1	1-3	

Bh

8h

4h