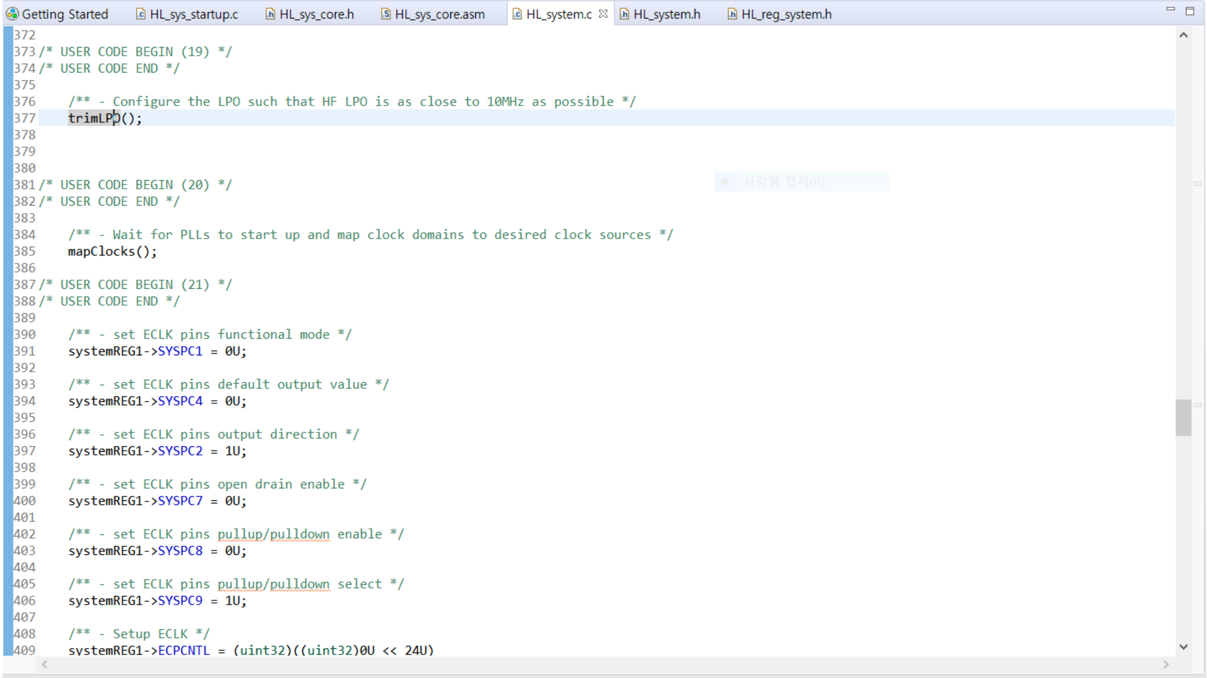
TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

강사 – Innova Lee(이상훈)

gcccompil3r@gmail.com

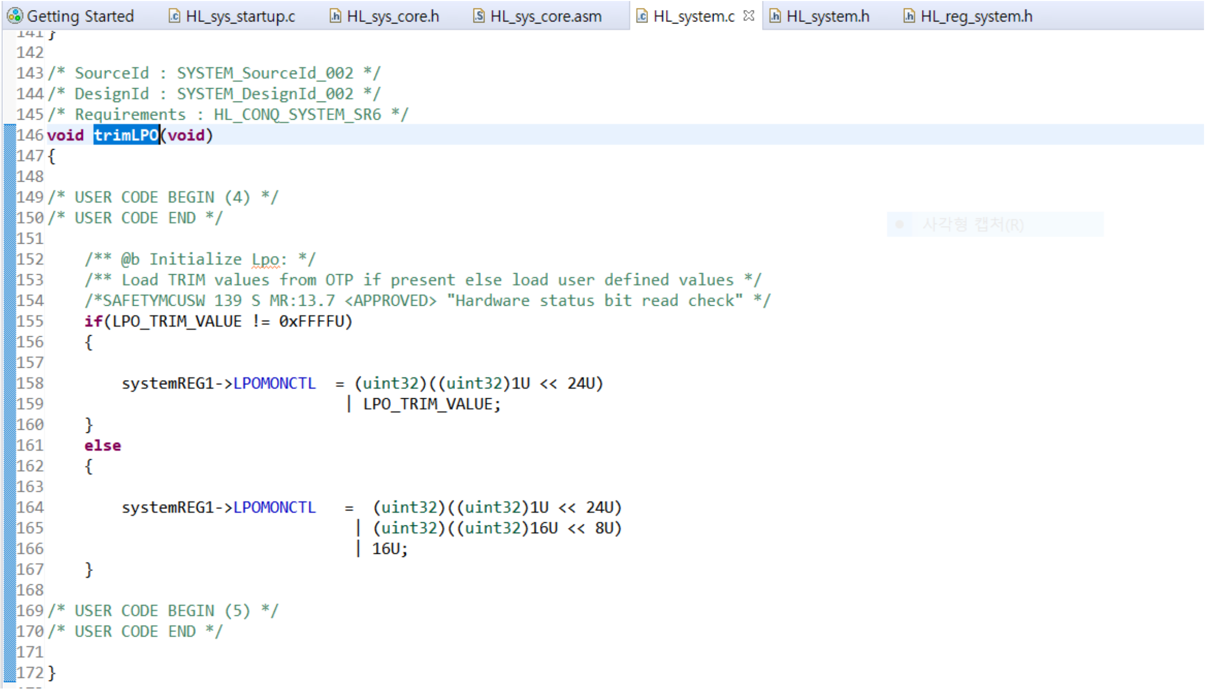
학생 – 문한나

mhn97@naver.com



```

/* USER CODE BEGIN (19) */
/* USER CODE END */

    /** - Configure the LPO such that HF LPO is as close to 10MHz as possible */
    trimLPO();



/* USER CODE BEGIN (20) */
/* USER CODE END */

    /** - Wait for PLLs to start up and map clock domains to desired clock sources */
    mapClocks();

/* USER CODE BEGIN (21) */
/* USER CODE END */

    /** - set ECLK pins functional mode */
    systemREG1->SYSPC1 = 0U;

    /** - set ECLK pins default output value */
    systemREG1->SYSPC4 = 0U;

    /** - set ECLK pins output direction */
    systemREG1->SYSPC2 = 1U;

    /** - set ECLK pins open drain enable */
    systemREG1->SYSPC7 = 0U;

    /** - set ECLK pins pullup/pulldown enable */
    systemREG1->SYSPC8 = 0U;

    /** - set ECLK pins pullup/pulldown select */
    systemREG1->SYSPC9 = 1U;

    /** - Setup ECLK */
    systemREG1->ECPCNTL = (uint32)((uint32)0U << 24U)
```

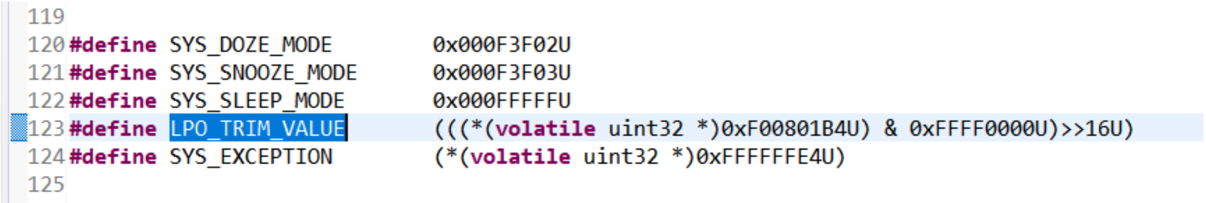
trimLPO();



```
}

/* SourceId : SYSTEM_SourceId_002 */
/* DesignId : SYSTEM_DesignId_002 */
/* Requirements : HL_CONQ_SYSTEM_SR6 */
void trimLPO(void)
{

/* USER CODE BEGIN (4) */
/* USER CODE END */

    /** @b Initialize Lpo: */
    /** Load TRIM values from OTP if present else load user defined values */
    /*SAFETYMCUSW 139 S MR:13.7 <APPROVED> "Hardware status bit read check" */
    if(LPO_TRIM_VALUE != 0xFFFFU)
    {

        systemREG1->LPOMONCTL  = (uint32)((uint32)1U << 24U)
                               | LPO_TRIM_VALUE;
    }
    else
    {

        systemREG1->LPOMONCTL   =  (uint32)((uint32)1U << 24U)
                                 | (uint32)((uint32)16U << 8U)
                                 | 16U;
    }

/* USER CODE BEGIN (5) */
/* USER CODE END */

}
```

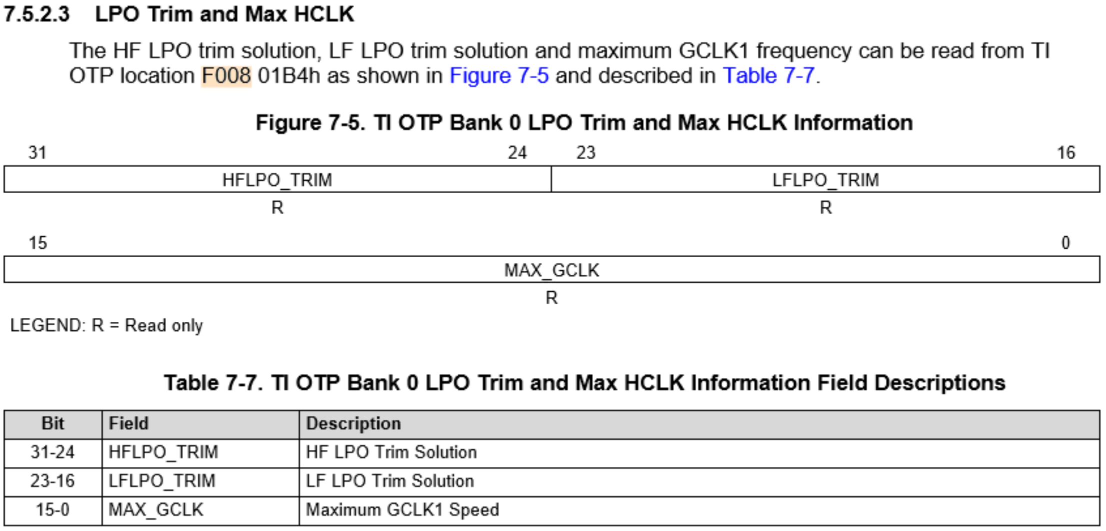
if(LPO_TRIM_VALUE != 0xFFFFU)

LPO_TRIM_VALUE



```
#define SYS_DOZE_MODE        0x000F3F02U
#define SYS_SNOOZE_MODE      0x000F3F03U
#define SYS_SLEEP_MODE       0x000FFFFFU
#define LPO_TRIM_VALUE       (((*(volatile uint32 *)0xF00801B4U) & 0xFFFF0000U)>>16U)
#define SYS_EXCEPTION        (*(volatile uint32 *)0xFFFFFFE4U)
```

F008 검색



7.5.2.3 LPO Trim and Max HCLK

The HF LPO trim solution, LF LPO trim solution and maximum GCLK1 frequency can be read from TI OTP location F008 01B4h as shown in Figure 7-5 and described in Table 7-7.

Figure 7-5. TI OTP Bank 0 LPO Trim and Max HCLK Information

31 — 24	23 — 16
HFLPO_TRIM	LFLPO_TRIM
R	R

15 — 0
MAX_GCLK
R

LEGEND: R = Read only

Table 7-7. TI OTP Bank 0 LPO Trim and Max HCLK Information Field Descriptions

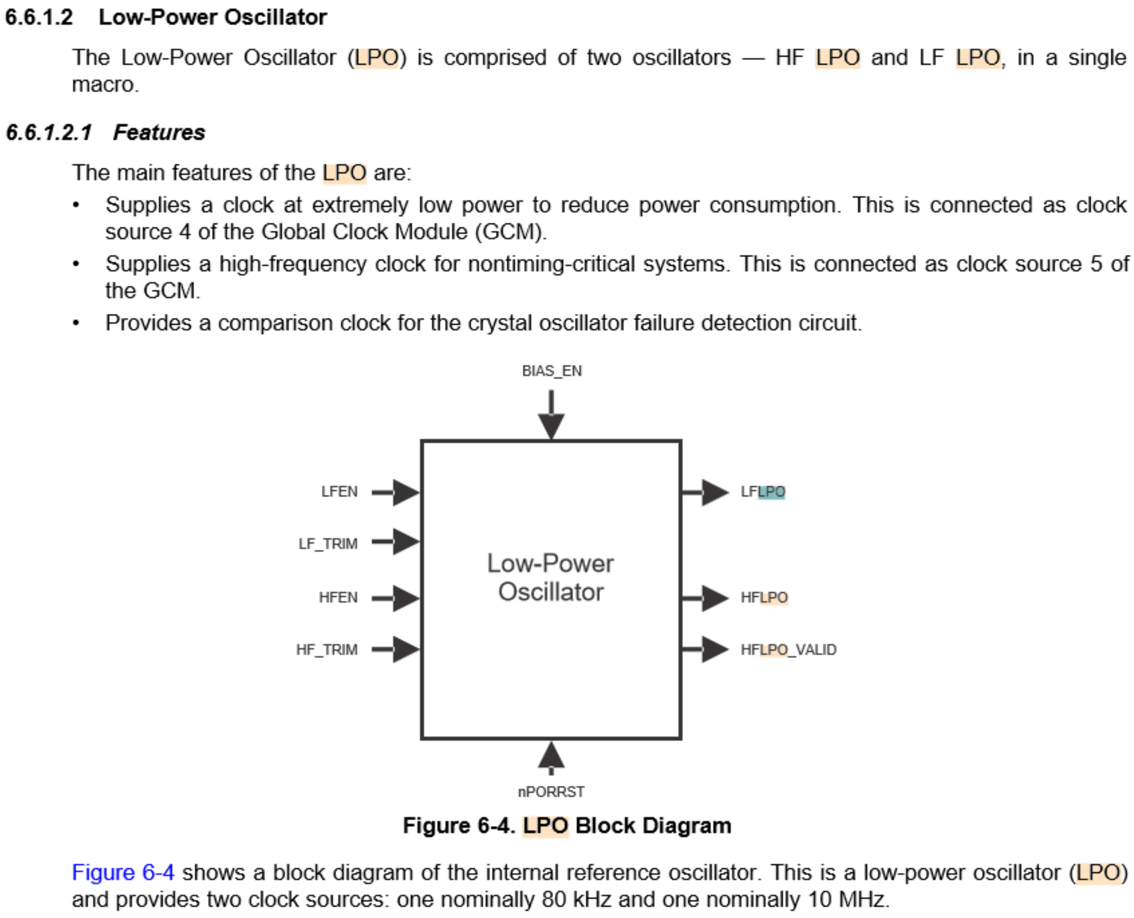
Bit	Field	Description
31-24	HFLPO_TRIM	HF LPO Trim Solution
23-16	LFLPO_TRIM	LF LPO Trim Solution
15-0	MAX_GCLK	Maximum GCLK1 Speed

```
#define LPO_TRIM_VALUE (((*(volatile uint32 *)0xF00801B4U) & 0xFFFF0000U)>>16U)
```

31~16 비트만 봄

HFLPO_TRIM 과 LFLPO_TRIM

LPO TRIM? 저전력 오실레이터



6.6.1.2 Low-Power Oscillator

The Low-Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

6.6.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power to reduce power consumption. This is connected as clock source 4 of the Global Clock Module (GCM).
- Supplies a high-frequency clock for nontiming-critical systems. This is connected as clock source 5 of the GCM.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

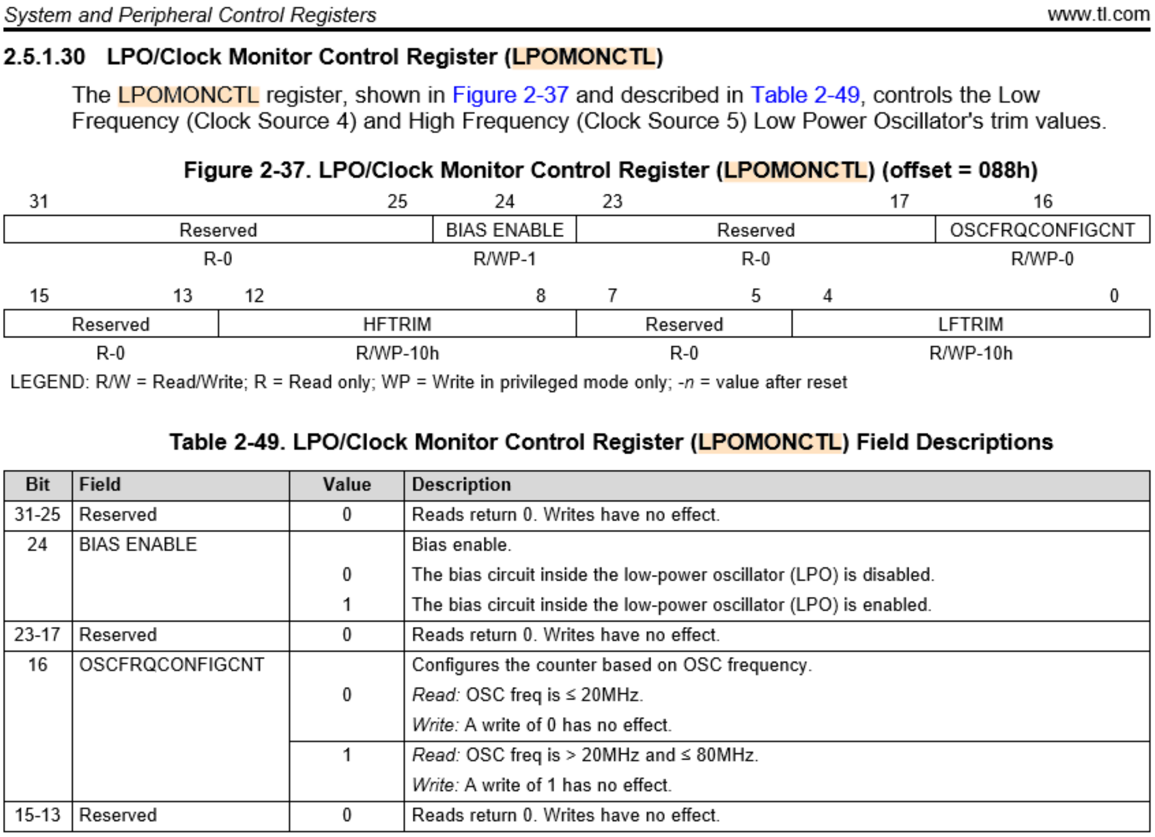
Figure 6-4. LPO Block Diagram

Figure 6-4 shows a block diagram of the internal reference oscillator. This is a low-power oscillator (LPO) and provides two clock sources: one nominally 80 kHz and one nominally 10 MHz.

상위 16 비트가 아니라면

```
if(LPO_TRIM_VALUE != 0xFFFFU)
    {

        systemREG1->LPOMONCTL  = (uint32)((uint32)1U << 24U)
                               | LPO_TRIM_VALUE;
    }
```

24 번비트 확인



System and Peripheral Control Registers www.ti.com

2.5.1.30 LPO/Clock Monitor Control Register (LPOMONCTL)

The LPOMONCTL register, shown in Figure 2-37 and described in Table 2-49, controls the Low Frequency (Clock Source 4) and High Frequency (Clock Source 5) Low Power Oscillator's trim values.

Figure 2-37. LPO/Clock Monitor Control Register (LPOMONCTL) (offset = 088h)

31 25	24	23 17	16
Reserved	BIAS ENABLE	Reserved	OSCFRQCONFIGCNT
R-0	R/WP-1	R-0	R/WP-0

15 13	12 8	7 5	4 0
Reserved	HFTRIM	Reserved	LFTRIM
R-0	R/WP-10h	R-0	R/WP-10h

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions

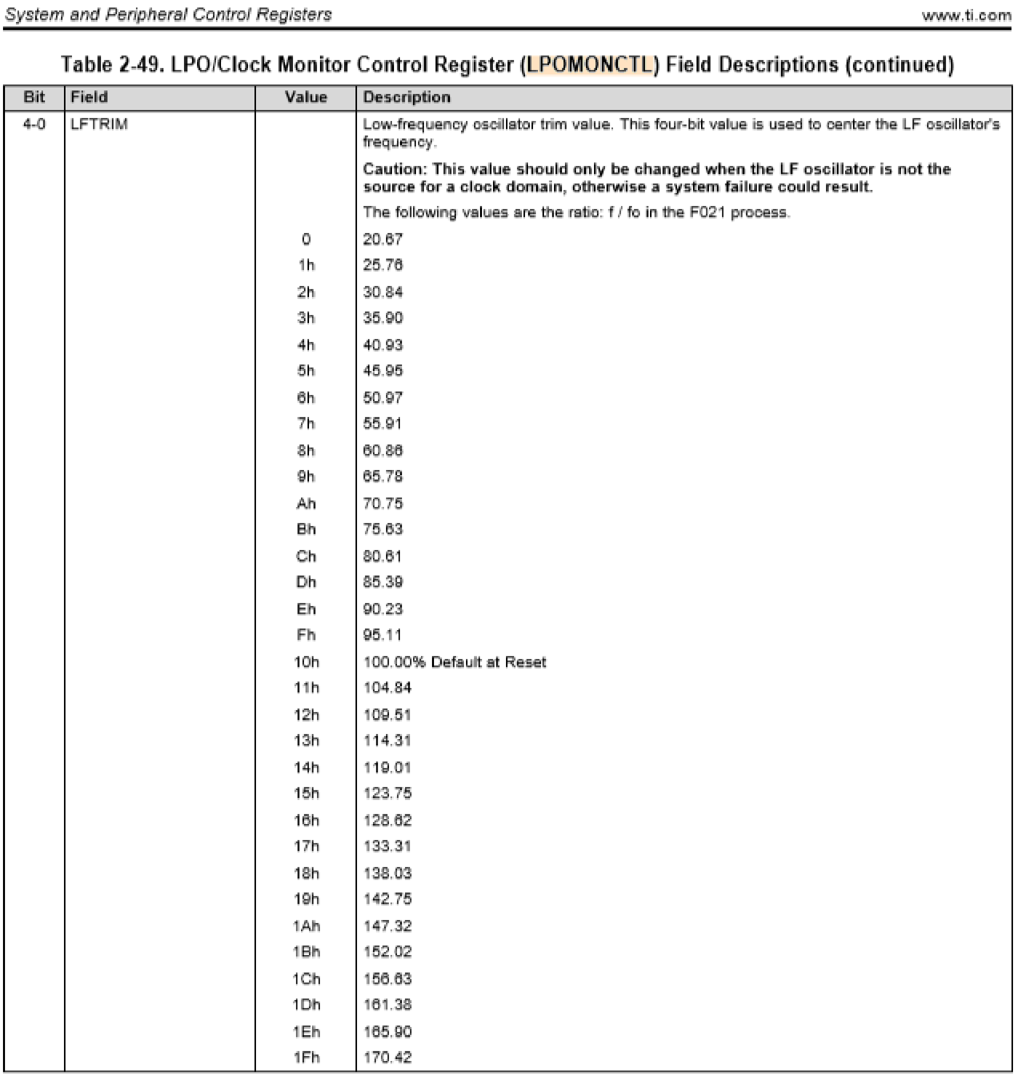
Bit	Field	Value	Description
31-25	Reserved	0	Reads return 0. Writes have no effect.
24	BIAS ENABLE		Bias enable.
		0	The bias circuit inside the low-power oscillator (LPO) is disabled.
		1	The bias circuit inside the low-power oscillator (LPO) is enabled.
23-17	Reserved	0	Reads return 0. Writes have no effect.
16	OSCFRQCONFIGCNT		Configures the counter based on OSC frequency.
		0	*Read:* OSC freq is ≤ 20MHz. *Write:* A write of 0 has no effect.
		1	*Read:* OSC freq is > 20MHz and ≤ 80MHz. *Write:* A write of 1 has no effect.
15-13	Reserved	0	Reads return 0. Writes have no effect.

The bias circuit inside the low-power oscillator (LPO) is enabled.

오실레이터 내부 바이오스 회로 동작

8~12 5비트 -> HFTRIM 로 동작이 바뀔 수 있음

High-frequency oscillator trim value. This four-bit value is used to center the HF oscillator's frequency.



System and Peripheral Control Registers www.ti.com

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions (continued)

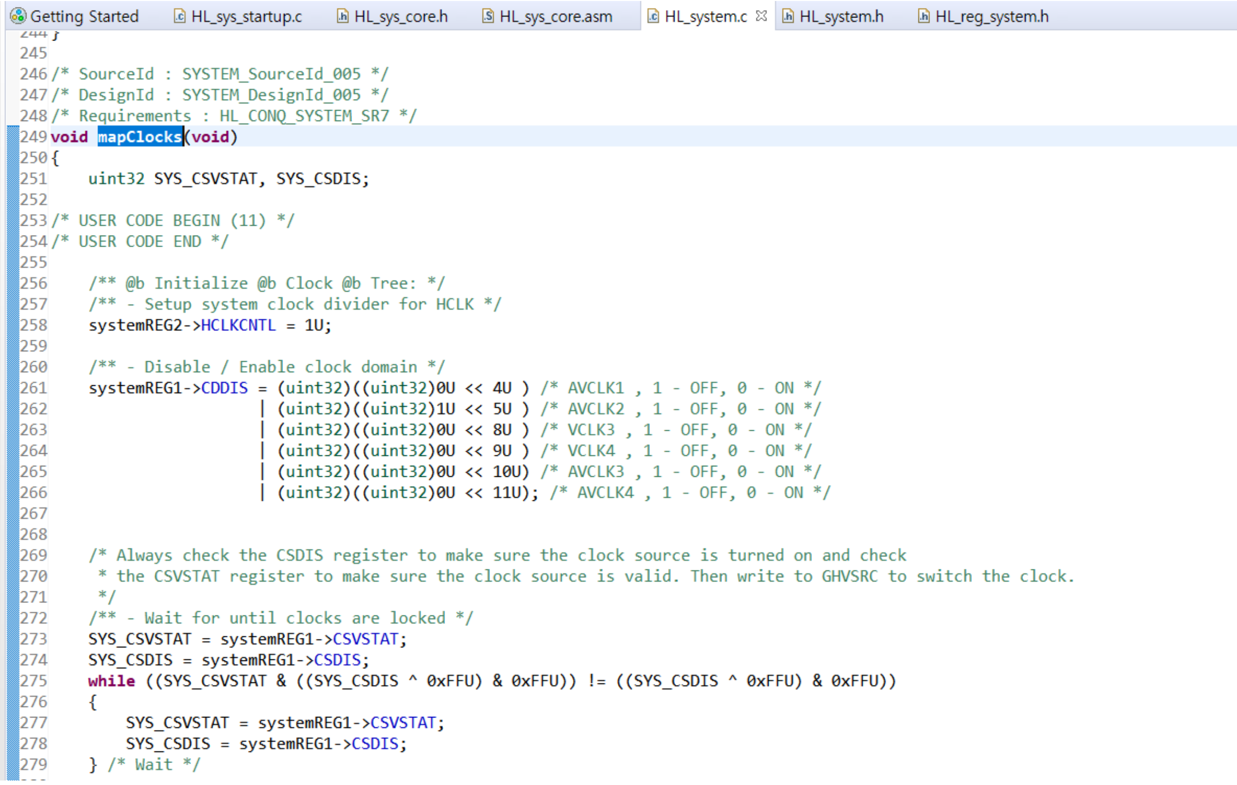
Bit	Field	Value	Description
4-0	LFTRIM		Low-frequency oscillator trim value. This four-bit value is used to center the LF oscillator's frequency. **Caution: This value should only be changed when the LF oscillator is not the source for a clock domain, otherwise a system failure could result.** The following values are the ratio: f / fo in the F021 process.
		0	20.67
		1h	25.76
		2h	30.84
		3h	35.90
		4h	40.93
		5h	45.95
		6h	50.97
		7h	55.91
		8h	60.88
		9h	65.78
		Ah	70.75
		Bh	75.63
		Ch	80.61
		Dh	85.39
		Eh	90.23
		Fh	95.11
		10h	100.00% Default at Reset
		11h	104.84
		12h	109.51
		13h	114.31
		14h	119.01
		15h	123.75
		16h	128.62
		17h	133.31
		18h	138.03
		19h	142.75
		1Ah	147.32
		1Bh	152.02
		1Ch	156.63
		1Dh	161.38
		1Eh	165.90
		1Fh	170.42

10h 100.00% Default at Reset. -> 주파수 감소가 없다

Reset 시 디폴트 값이 1 0 이므로 else 일 수 없음(ffff 일 수 없음)

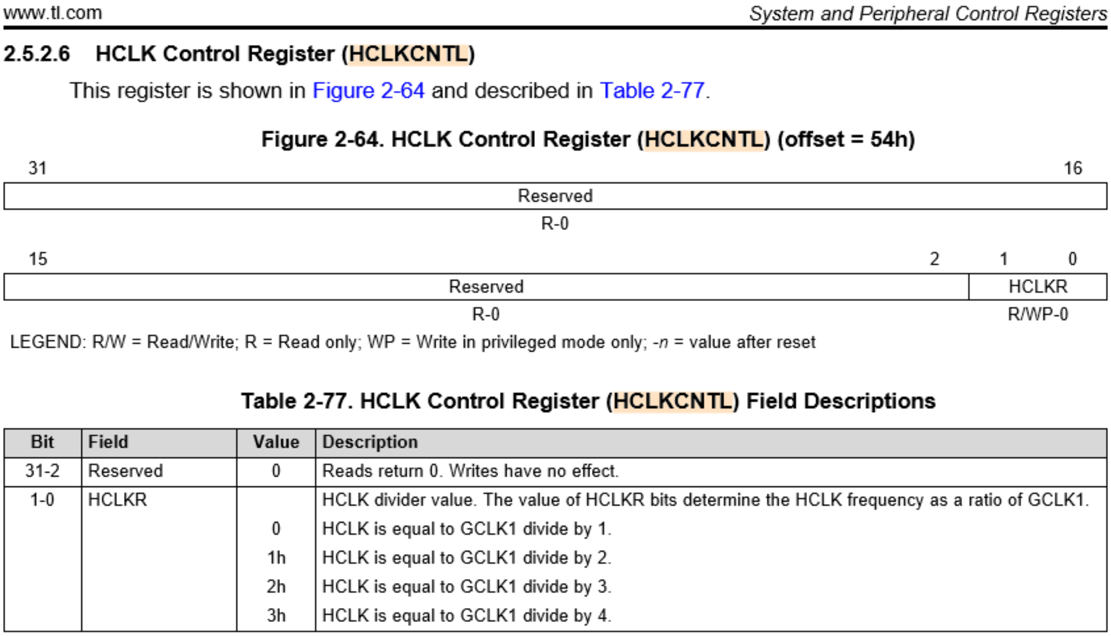
TRIM? 파형성형회로

mapClocks();



```c

/* SourceId : SYSTEM_SourceId_005 */
/* DesignId : SYSTEM_DesignId_005 */
/* Requirements : HL_CONQ_SYSTEM_SR7 */
void mapClocks(void)
{
    uint32 SYS_CSVSTAT, SYS_CSDIS;

/* USER CODE BEGIN (11) */
/* USER CODE END */

    /** @b Initialize @b Clock @b Tree: */
    /** - Setup system clock divider for HCLK */
    systemREG2->HCLKCNTL = 1U;

    /** - Disable / Enable clock domain */
    systemREG1->CDDIS = (uint32)((uint32)0U << 4U ) /* AVCLK1 , 1 - OFF, 0 - ON */
                      | (uint32)((uint32)1U << 5U ) /* AVCLK2 , 1 - OFF, 0 - ON */
                      | (uint32)((uint32)0U << 8U ) /* VCLK3 , 1 - OFF, 0 - ON */
                      | (uint32)((uint32)0U << 9U ) /* VCLK4 , 1 - OFF, 0 - ON */
                      | (uint32)((uint32)0U << 10U) /* AVCLK3 , 1 - OFF, 0 - ON */
                      | (uint32)((uint32)0U << 11U); /* AVCLK4 , 1 - OFF, 0 - ON */


    /* Always check the CSDIS register to make sure the clock source is turned on and check
     * the CSVSTAT register to make sure the clock source is valid. Then write to GHVSRC to switch the clock.
     */
    /** - Wait for until clocks are locked */
    SYS_CSVSTAT = systemREG1->CSVSTAT;
    SYS_CSDIS = systemREG1->CSDIS;
    while ((SYS_CSVSTAT & ((SYS_CSDIS ^ 0xFFU) & 0xFFU)) != ((SYS_CSDIS ^ 0xFFU) & 0xFFU))
    {
        SYS_CSVSTAT = systemREG1->CSVSTAT;
        SYS_CSDIS = systemREG1->CSDIS;
    } /* Wait */
```

HCLKCNTL



www.ti.com *System and Peripheral Control Registers*

2.5.2.6 HCLK Control Register (HCLKCNTL)

This register is shown in Figure 2-64 and described in Table 2-77.

Figure 2-64. HCLK Control Register (HCLKCNTL) (offset = 54h)

31 … 16
Reserved
R-0

15 … 2	1 … 0
Reserved	HCLKR
R-0	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-77. HCLK Control Register (HCLKCNTL) Field Descriptions

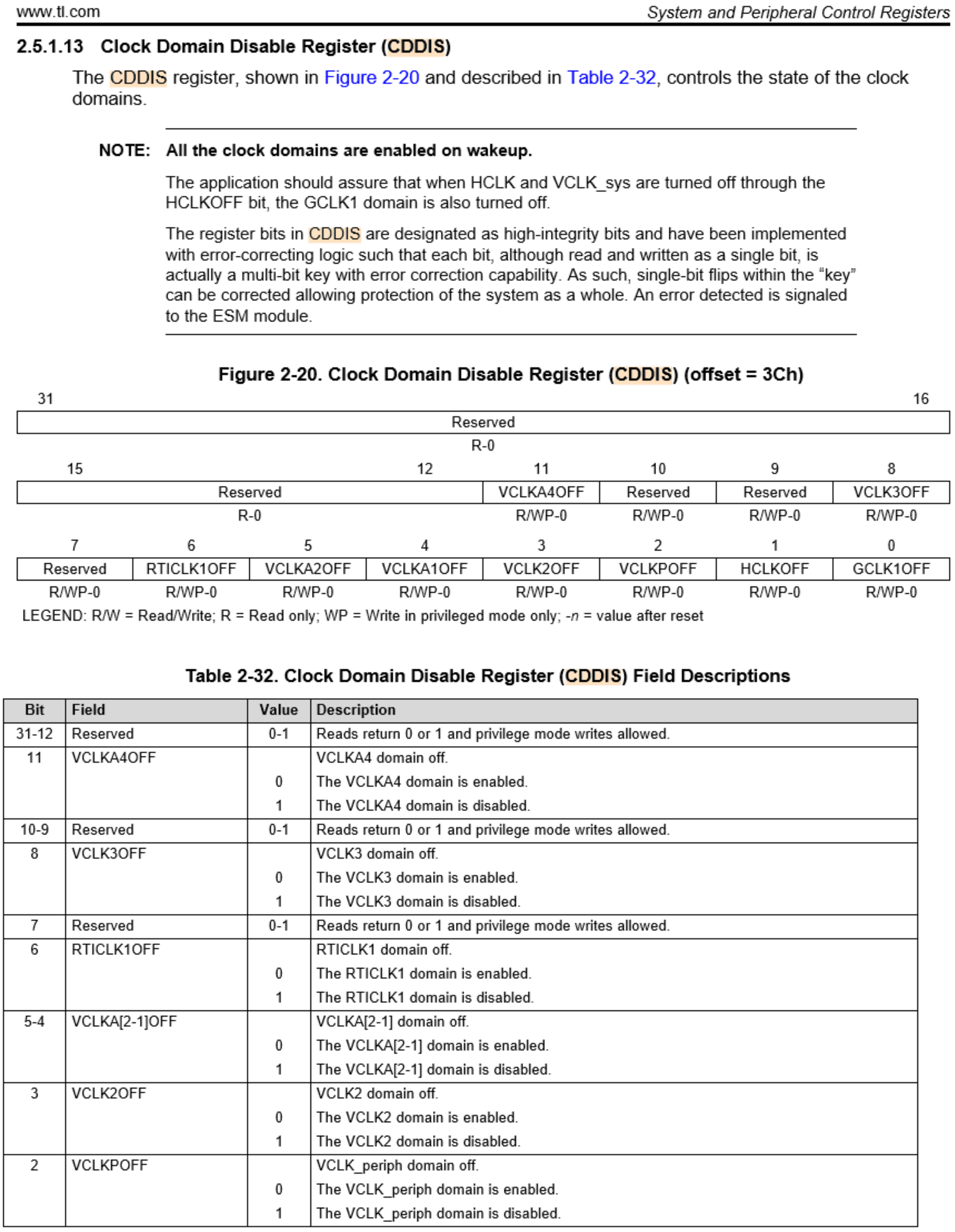
Bit	Field	Value	Description
31-2	Reserved	0	Reads return 0. Writes have no effect.
1-0	HCLKR		HCLK divider value. The value of HCLKR bits determine the HCLK frequency as a ratio of GCLK1.
		0	HCLK is equal to GCLK1 divide by 1.
		1h	HCLK is equal to GCLK1 divide by 2.
		2h	HCLK is equal to GCLK1 divide by 3.
		3h	HCLK is equal to GCLK1 divide by 4.

1h: HCLK is equal to GCLK1 divide by 2.

1 이 들어오니까 2 분주 하겠다.

```
systemREG1->CDDIS = (uint32) ((uint32)0U << 4U) /* AVCLK1, 1 - OFF, 0 - ON */
```

4 번비트를 0으로



www.ti.com — *System and Peripheral Control Registers*

2.5.1.13 Clock Domain Disable Register (CDDIS)

The CDDIS register, shown in Figure 2-20 and described in Table 2-32, controls the state of the clock domains.

NOTE: All the clock domains are enabled on wakeup.

The application should assure that when HCLK and VCLK_sys are turned off through the HCLKOFF bit, the GCLK1 domain is also turned off.

The register bits in CDDIS are designated as high-integrity bits and have been implemented with error-correcting logic such that each bit, although read and written as a single bit, is actually a multi-bit key with error correction capability. As such, single-bit flips within the “key” can be corrected allowing protection of the system as a whole. An error detected is signaled to the ESM module.

Figure 2-20. Clock Domain Disable Register (CDDIS) (offset = 3Ch)

31-16
Reserved
R-0

15-12	11	10	9	8
Reserved	VCLKA4OFF	Reserved	Reserved	VCLK3OFF
R-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0

7	6	5	4	3	2	1	0
Reserved	RTICLK1OFF	VCLKA2OFF	VCLKA1OFF	VCLK2OFF	VCLKPOFF	HCLKOFF	GCLK1OFF
R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-32. Clock Domain Disable Register (CDDIS) Field Descriptions

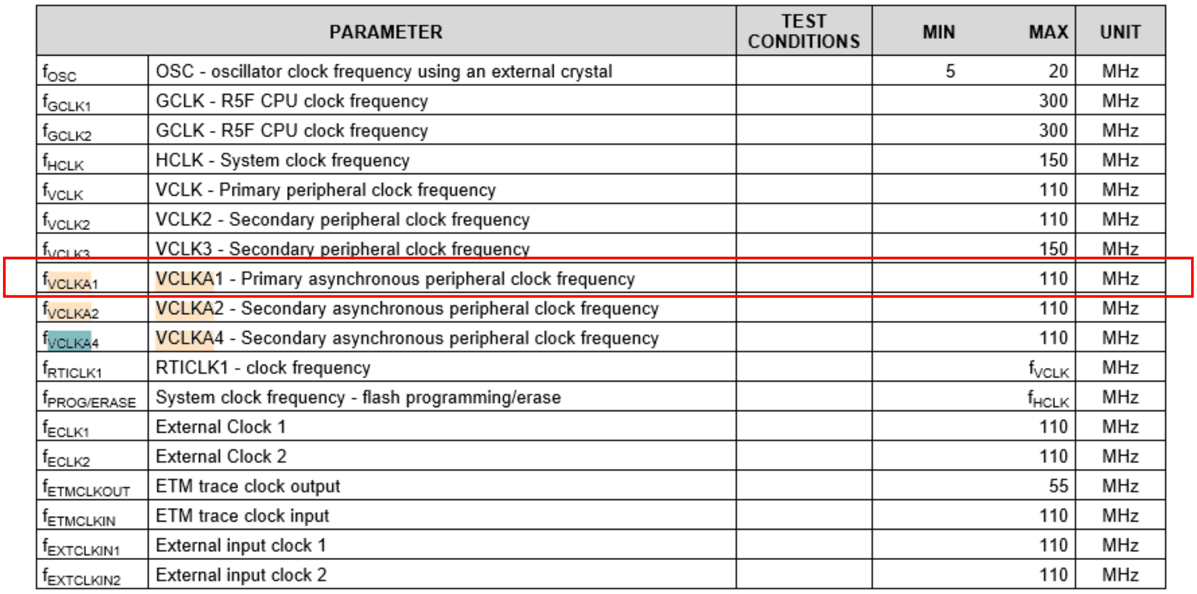
Bit	Field	Value	Description
31-12	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
11	VCLKA4OFF		VCLKA4 domain off.
		0	The VCLKA4 domain is enabled.
		1	The VCLKA4 domain is disabled.
10-9	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
8	VCLK3OFF		VCLK3 domain off.
		0	The VCLK3 domain is enabled.
		1	The VCLK3 domain is disabled.
7	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
6	RTICLK1OFF		RTICLK1 domain off.
		0	The RTICLK1 domain is enabled.
		1	The RTICLK1 domain is disabled.
5-4	VCLKA[2-1]OFF		VCLKA[2-1] domain off.
		0	The VCLKA[2-1] domain is enabled.
		1	The VCLKA[2-1] domain is disabled.
3	VCLK2OFF		VCLK2 domain off.
		0	The VCLK2 domain is enabled.
		1	The VCLK2 domain is disabled.
2	VCLKPOFF		VCLK_periph domain off.
		0	The VCLK_periph domain is enabled.
		1	The VCLK_periph domain is disabled.

The VCLKA[1] domain is enabled.

VCLKA1 – 동작주파수 110mhz 사용

5.5 Switching Characteristics over Recommended Operating Conditions for Clock Domains

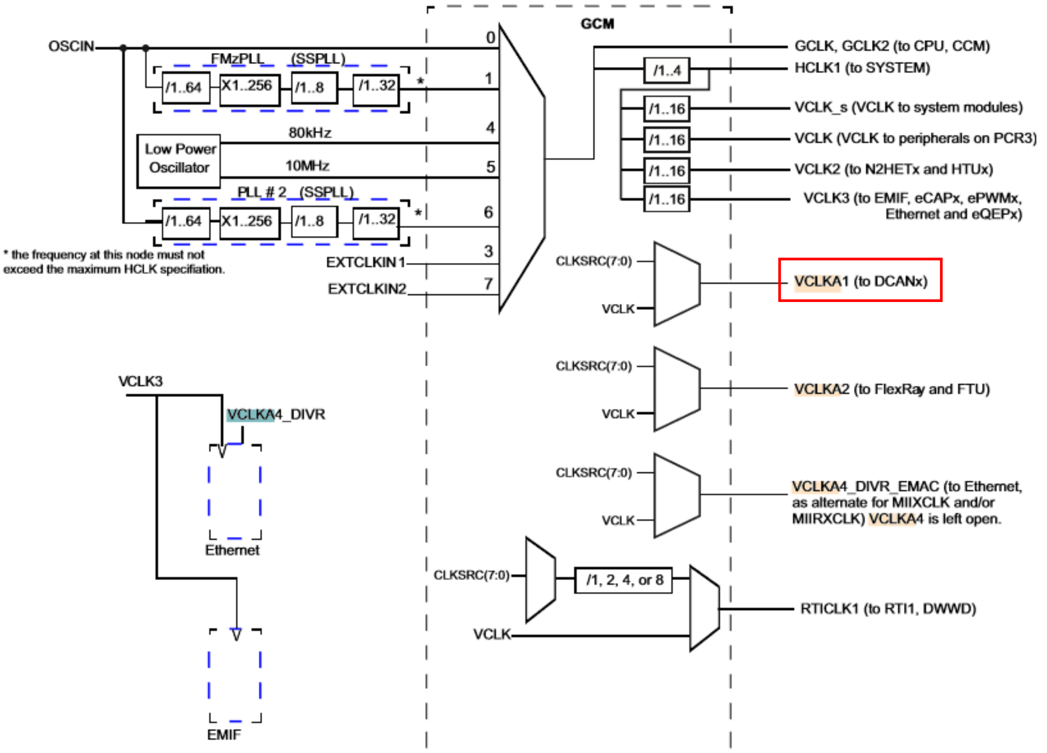
Table 5-2. Clock Domain Timing Specifications



PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{OSC}	OSC - oscillator clock frequency using an external crystal		5	20	MHz
f_{GCLK1}	GCLK - R5F CPU clock frequency			300	MHz
f_{GCLK2}	GCLK - R5F CPU clock frequency			300	MHz
f_{HCLK}	HCLK - System clock frequency			150	MHz
f_{VCLK}	VCLK - Primary peripheral clock frequency			110	MHz
f_{VCLK2}	VCLK2 - Secondary peripheral clock frequency			110	MHz
f_{VCLK3}	VCLK3 - Secondary peripheral clock frequency			150	MHz
f_{VCLKA1}	VCLKA1 - Primary asynchronous peripheral clock frequency			110	MHz
f_{VCLKA2}	VCLKA2 - Secondary asynchronous peripheral clock frequency			110	MHz
f_{VCLKA4}	VCLKA4 - Secondary asynchronous peripheral clock frequency			110	MHz
$f_{RTICLK1}$	RTICLK1 - clock frequency			f_{VCLK}	MHz
$f_{PROG/ERASE}$	System clock frequency - flash programming/erase			f_{HCLK}	MHz
f_{ECLK1}	External Clock 1			110	MHz
f_{ECLK2}	External Clock 2			110	MHz
$f_{ETMCLKOUT}$	ETM trace clock output			55	MHz
$f_{ETMCLKIN}$	ETM trace clock input			110	MHz
$f_{EXTCLKIN1}$	External input clock 1			110	MHz
$f_{EXTCLKIN2}$	External input clock 2			110	MHz

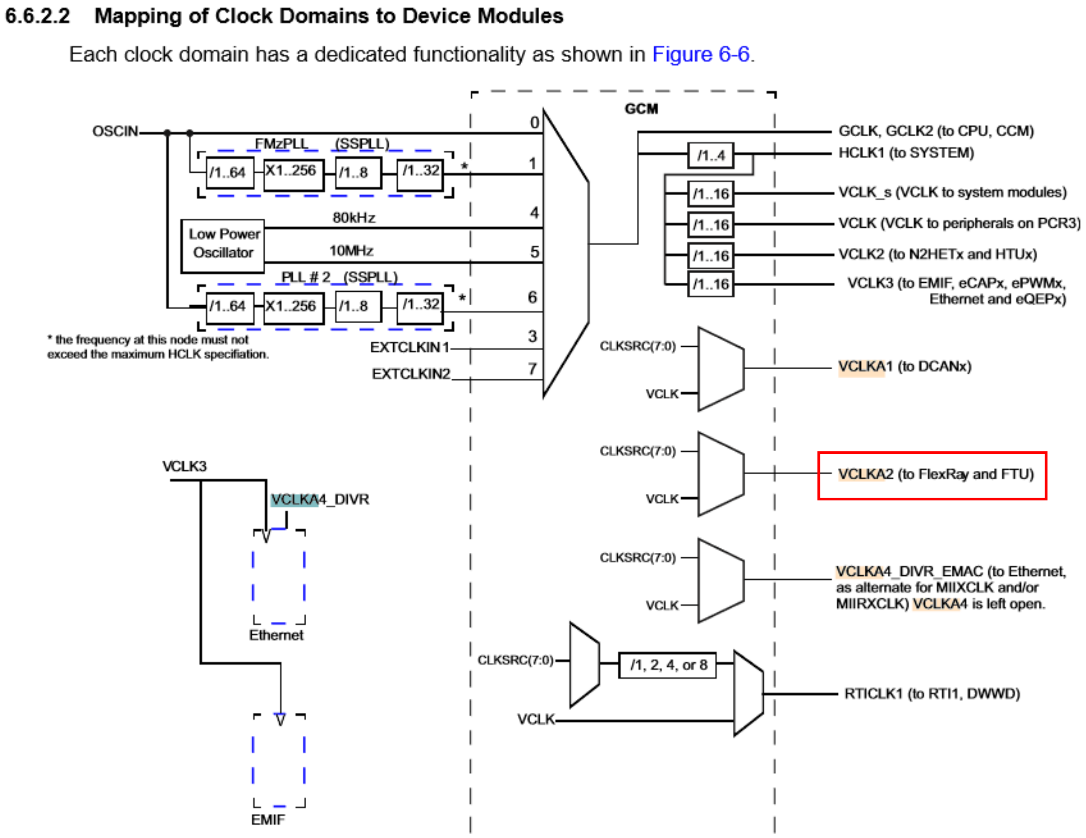
6.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in Figure 6-6.


OSCIN
FMzPLL (SSPLL)
/1..64
X1..256
/1..8
/1..32
*
0
1
4
5
6
3
7
80kHz
Low Power Oscillator
10MHz
PLL # 2 (SSPLL)
* the frequency at this node must not exceed the maximum HCLK specification.
EXTCLKIN1
EXTCLKIN2
GCM
/1..4
/1..16
GCLK, GCLK2 (to CPU, CCM)
HCLK1 (to SYSTEM)
VCLK_s (VCLK to system modules)
VCLK (VCLK to peripherals on PCR3)
VCLK2 (to N2HETx and HTUx)
VCLK3 (to EMIF, eCAPx, ePWMx, Ethernet and eQEPx)
CLKSRC(7:0)
VCLK
VCLKA1 (to DCANx)
VCLKA2 (to FlexRay and FTU)
VCLKA4_DIVR_EMAC (to Ethernet, as alternate for MIIXCLK and/or MIIRXCLK) VCLKA4 is left open.
/1, 2, 4, or 8
RTICLK1 (to RTI1, DWWD)
VCLK3
VCLKA4_DIVR
Ethernet
EMIF

```
| (uint32)((uint32)1U << 5U ) /* AVCLK2 , 1 - OFF, 0 - ON */
```

The VCLKA[2] domain is disabled.



6.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in Figure 6-6.

OSCIN
FMzPLL (SSPLL)
/1..64
X1..256
/1..8
/1..32
*
80kHz
Low Power Oscillator
10MHz
PLL # 2 (SSPLL)
* the frequency at this node must not exceed the maximum HCLK specification.
EXTCLKIN1
EXTCLKIN2
0
1
4
5
6
3
7
GCM
/1..4
/1..16
GCLK, GCLK2 (to CPU, CCM)
HCLK1 (to SYSTEM)
VCLK_s (VCLK to system modules)
VCLK (VCLK to peripherals on PCR3)
VCLK2 (to N2HETx and HTUx)
VCLK3 (to EMIF, eCAPx, ePWMx, Ethernet and eQEPx)
CLKSRC(7:0)
VCLK
VCLKA1 (to DCANx)
VCLKA2 (to FlexRay and FTU)
VCLKA4_DIVR_EMAC (to Ethernet, as alternate for MIIXCLK and/or MIIRXCLK) VCLKA4 is left open.
VCLK3
VCLKA4_DIVR
Ethernet
EMIF
/1, 2, 4, or 8
RTICLK1 (to RTI1, DWWD)

```
| (uint32)((uint32)0U << 8U ) /* VCLK3 , 1 - OFF, 0 - ON */
```

The VCLK3 domain is enabled.

```
| (uint32)((uint32)0U << 9U ) /* VCLK4 , 1 - OFF, 0 - ON */
| (uint32)((uint32)0U << 10U) /* AVCLK3 , 1 - OFF, 0 - ON */
```

Reads return 0 or 1 and privilege mode writes allowed.

이미 Reserved되있음

```
| (uint32)((uint32)0U << 11U); /* AVCLK4 , 1 - OFF, 0 - ON */
```

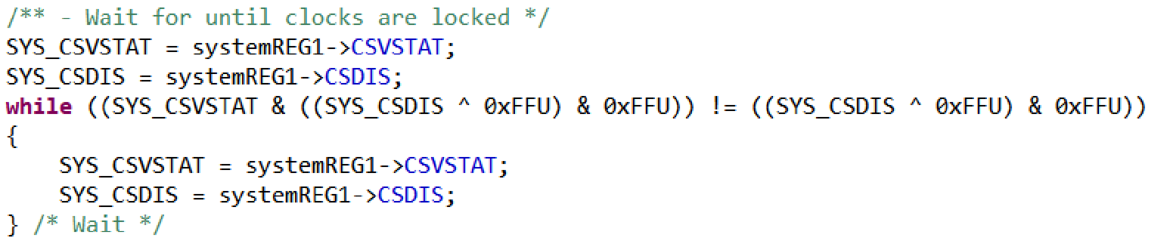
The VCLKA4 domain is enabled.

랜 통신 하는 곳으로 들어가는 클록

VCLKA3 – 동작주파수 150mhz 사용

문제? 주기가 너무 짧음, 150mhz 로 모터를 돌리면 안돌아감

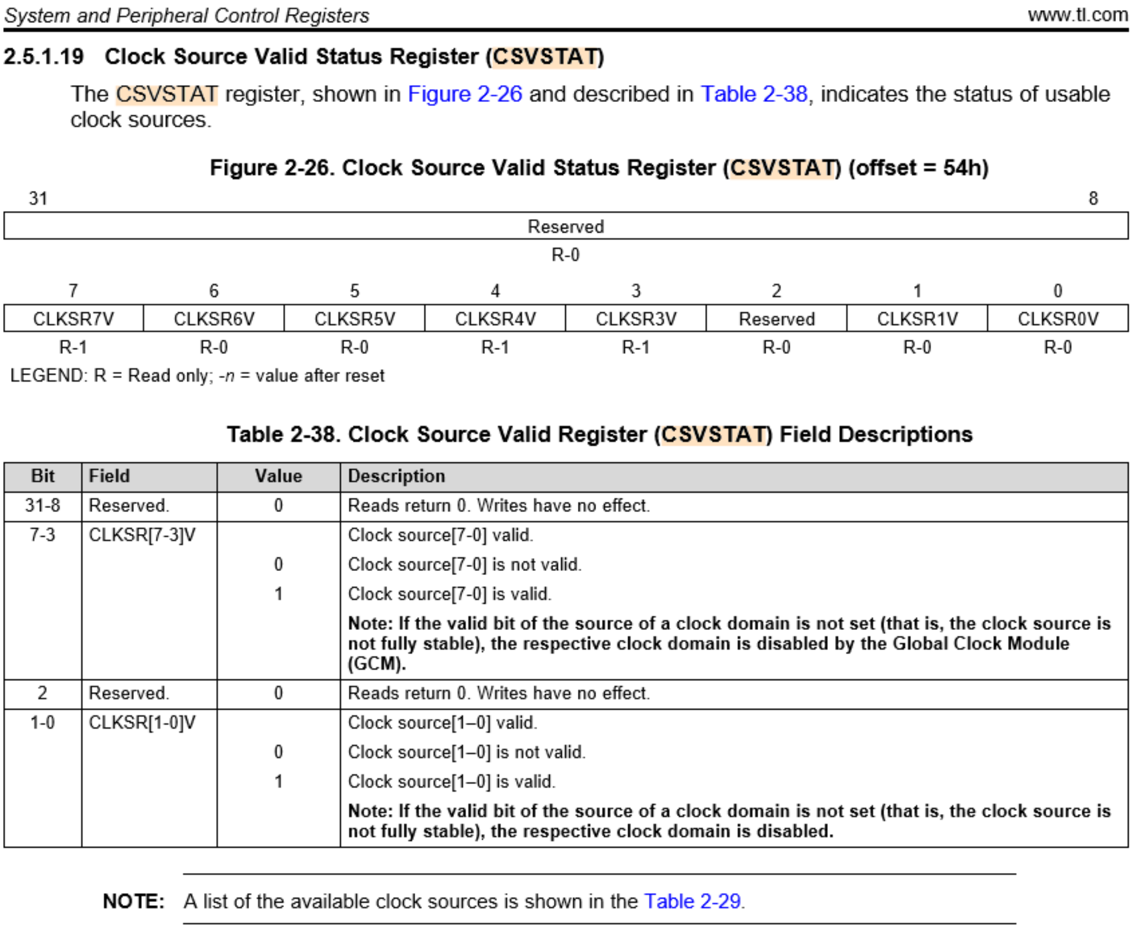
Rc 형 모터는 20ms 라서 맞춰 줘야함(나눠줘야 한다)



```
/** - Wait for until clocks are locked */
SYS_CSVSTAT = systemREG1->CSVSTAT;
SYS_CSDIS = systemREG1->CSDIS;
while ((SYS_CSVSTAT & ((SYS_CSDIS ^ 0xFFU) & 0xFFU)) != ((SYS_CSDIS ^ 0xFFU) & 0xFFU))
{
    SYS_CSVSTAT = systemREG1->CSVSTAT;
    SYS_CSDIS = systemREG1->CSDIS;
} /* Wait */
```

Lock? 클럭주파수 고정

CSVSTAT



2.5.1.19 Clock Source Valid Status Register (CSVSTAT)

The CSVSTAT register, shown in Figure 2-26 and described in Table 2-38, indicates the status of usable clock sources.

Figure 2-26. Clock Source Valid Status Register (CSVSTAT) (offset = 54h)

31–8
Reserved
R-0

7	6	5	4	3	2	1	0
CLKSR7V	CLKSR6V	CLKSR5V	CLKSR4V	CLKSR3V	Reserved	CLKSR1V	CLKSR0V
R-1	R-0	R-0	R-1	R-1	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

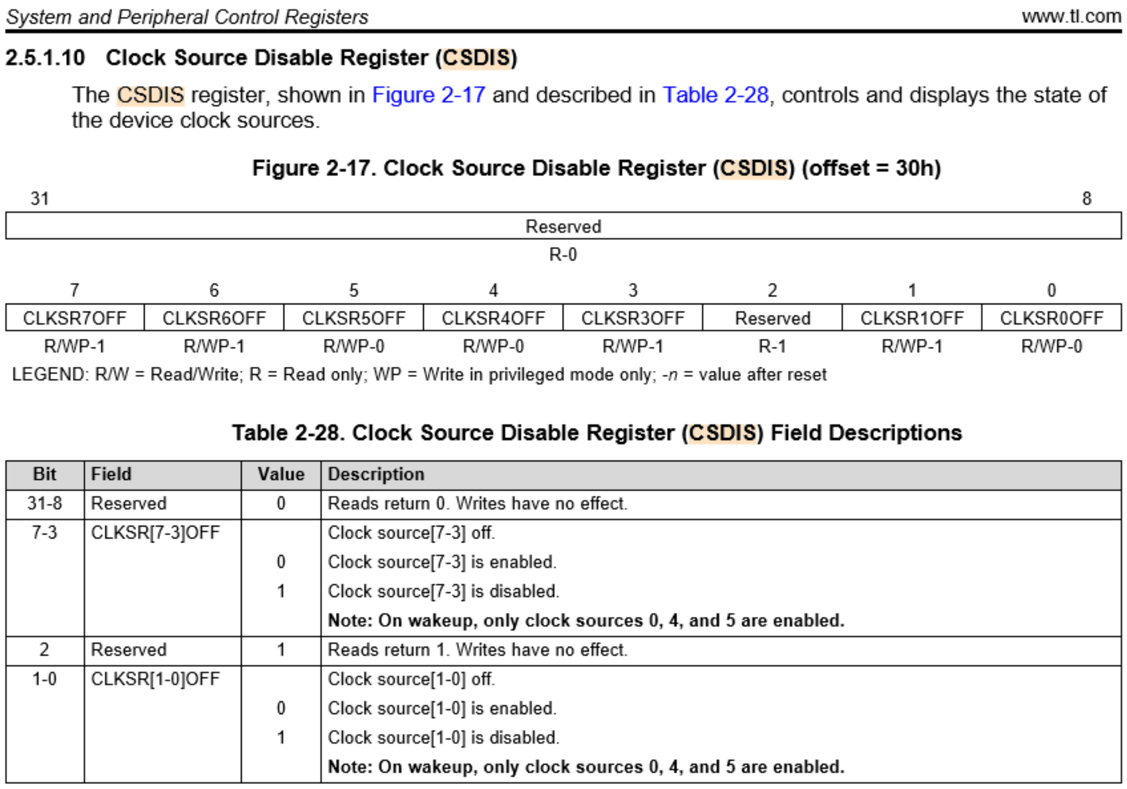
Table 2-38. Clock Source Valid Register (CSVSTAT) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved.	0	Reads return 0. Writes have no effect.
7-3	CLKSR[7-3]V		Clock source[7-0] valid.
		0	Clock source[7-0] is not valid.
		1	Clock source[7-0] is valid.
			Note: If the valid bit of the source of a clock domain is not set (that is, the clock source is not fully stable), the respective clock domain is disabled by the Global Clock Module (GCM).
2	Reserved.	0	Reads return 0. Writes have no effect.
1-0	CLKSR[1-0]V		Clock source[1–0] valid.
		0	Clock source[1–0] is not valid.
		1	Clock source[1–0] is valid.
			Note: If the valid bit of the source of a clock domain is not set (that is, the clock source is not fully stable), the respective clock domain is disabled.

NOTE: A list of the available clock sources is shown in the Table 2-29.

안정화가 되면 1, 아니면 0

CSDIS



2.5.1.10 Clock Source Disable Register (CSDIS)

The CSDIS register, shown in Figure 2-17 and described in Table 2-28, controls and displays the state of the device clock sources.

Figure 2-17. Clock Source Disable Register (CSDIS) (offset = 30h)

31–8
Reserved
R-0

7	6	5	4	3	2	1	0
CLKSR7OFF	CLKSR6OFF	CLKSR5OFF	CLKSR4OFF	CLKSR3OFF	Reserved	CLKSR1OFF	CLKSR0OFF
R/WP-1	R/WP-1	R/WP-0	R/WP-0	R/WP-1	R-1	R/WP-1	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-28. Clock Source Disable Register (CSDIS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reads return 0. Writes have no effect.
7-3	CLKSR[7-3]OFF		Clock source[7-3] off.
		0	Clock source[7-3] is enabled.
		1	Clock source[7-3] is disabled.
			Note: On wakeup, only clock sources 0, 4, and 5 are enabled.
2	Reserved	1	Reads return 1. Writes have no effect.
1-0	CLKSR[1-0]OFF		Clock source[1-0] off.
		0	Clock source[1-0] is enabled.
		1	Clock source[1-0] is disabled.
			Note: On wakeup, only clock sources 0, 4, and 5 are enabled.