# TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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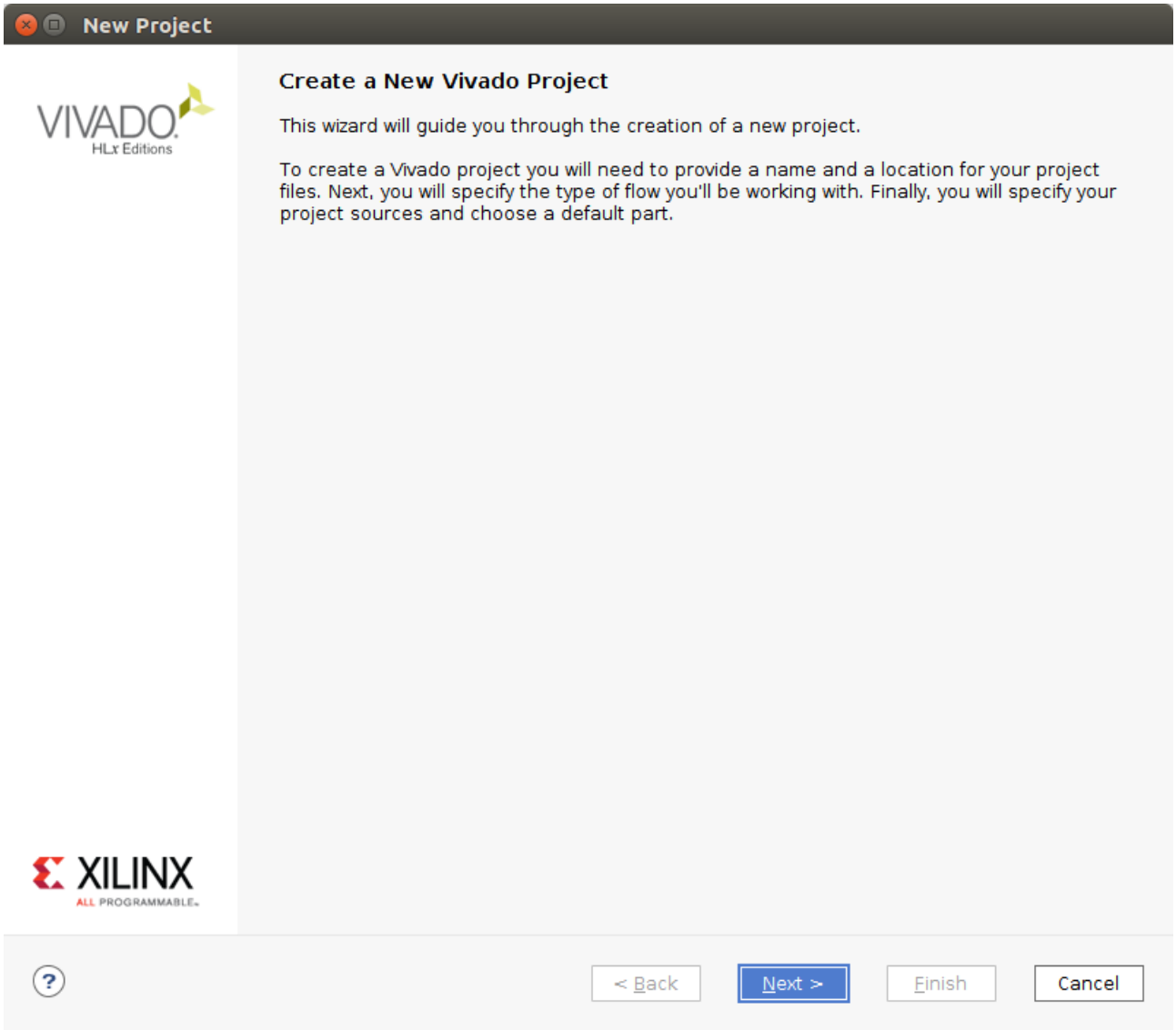
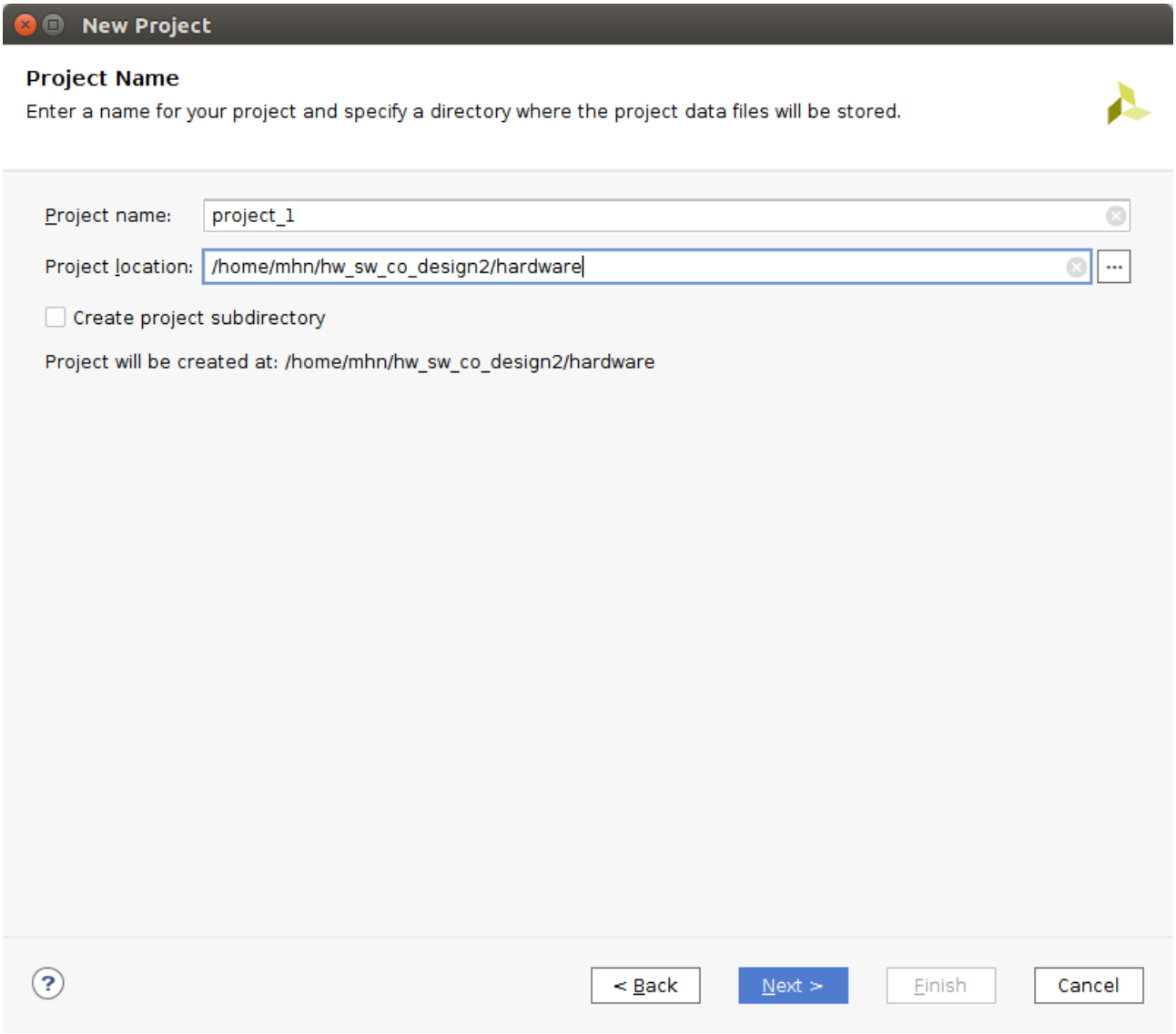
학생 – 문한나

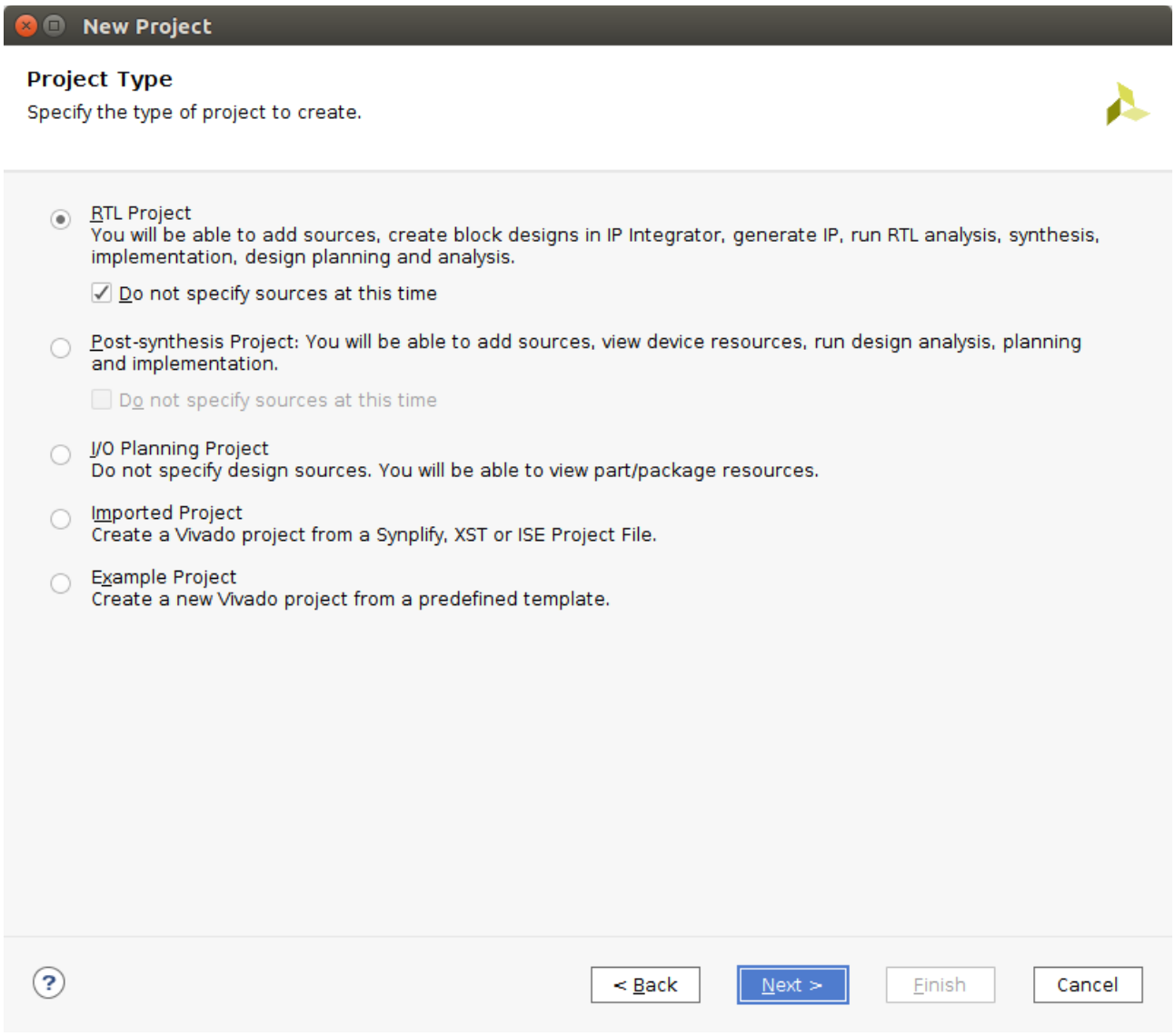
mhn97@naver.com

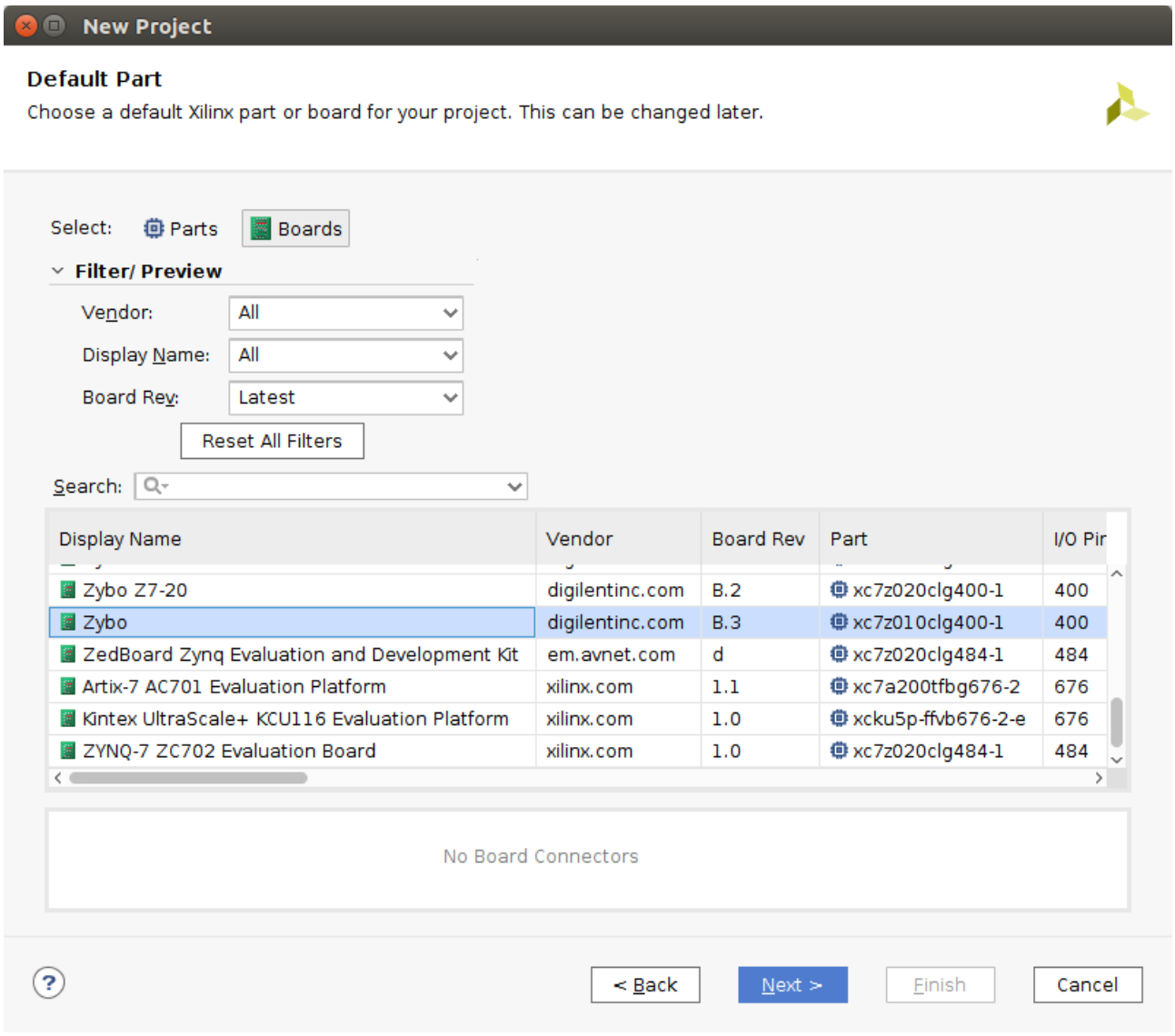
```
mkdir hw_sw_co_design2

cd hw_sw_co_design2

mkdir hardware
```

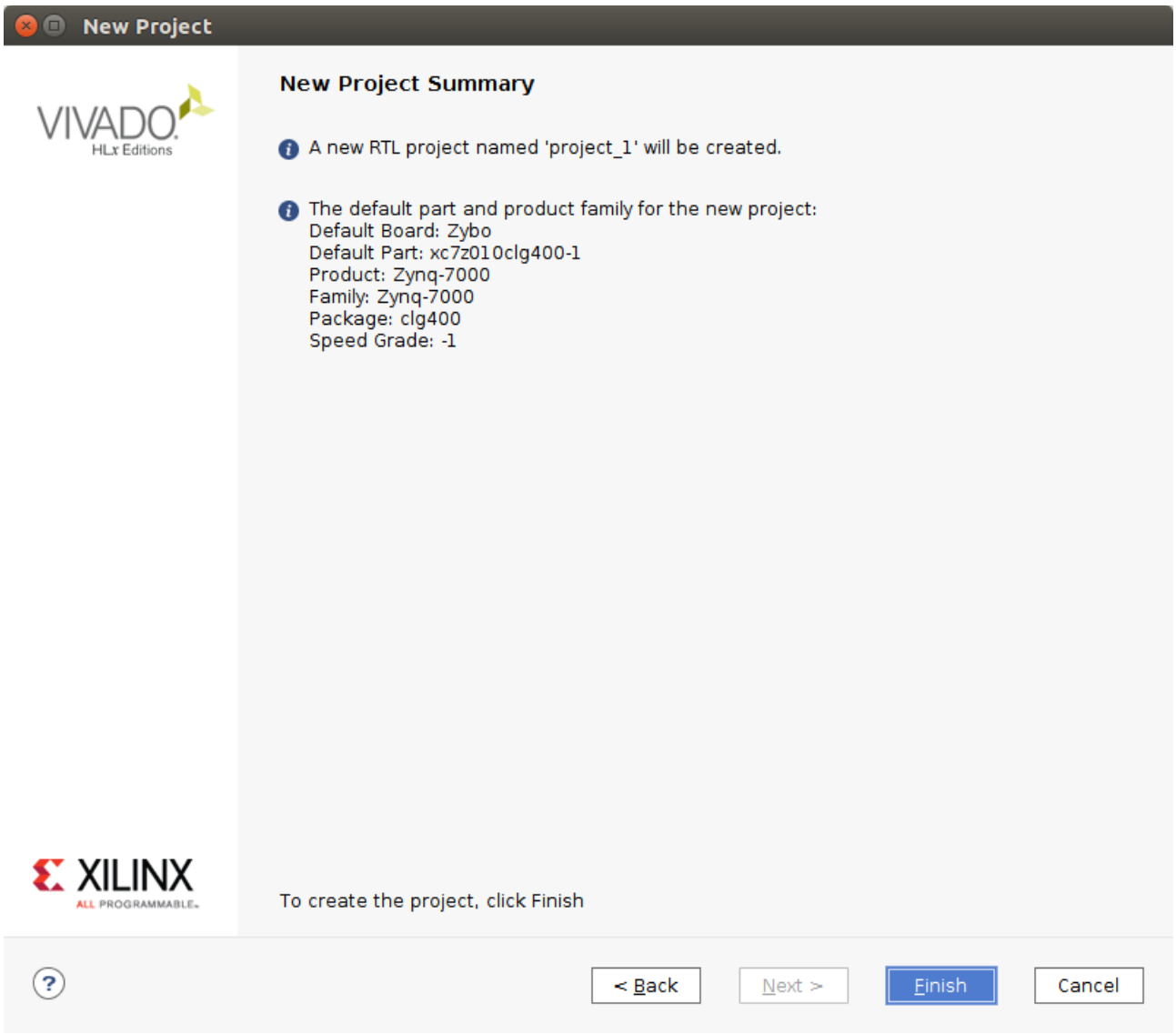
Vivado 실행

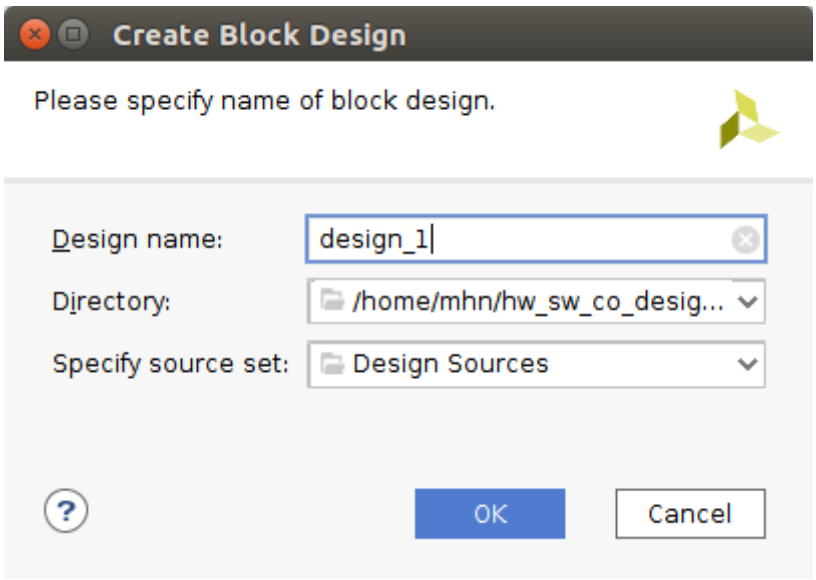


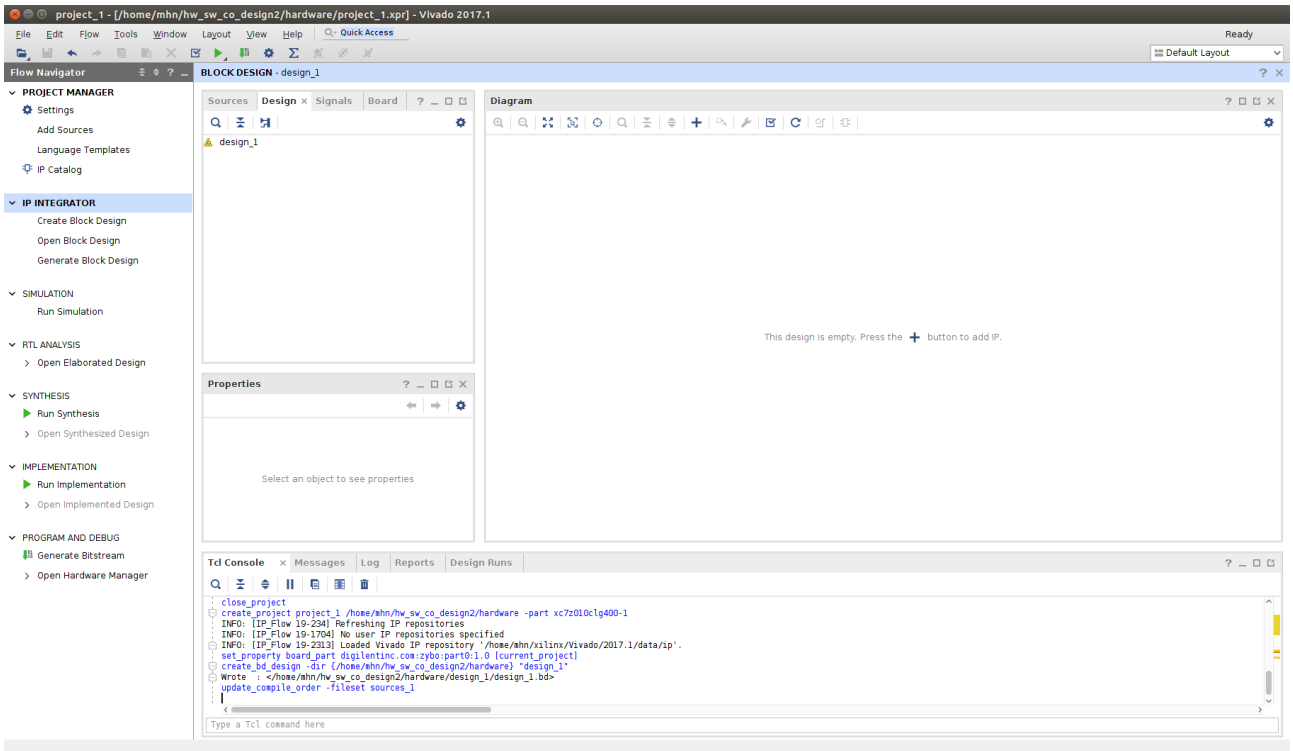

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
project_1
Project location:
/home/mhn/hw_sw_co_design2/hardware
Create project subdirectory
Project will be created at: /home/mhn/hw_sw_co_design2/hardware
< Back
Next >
Finish
Cancel

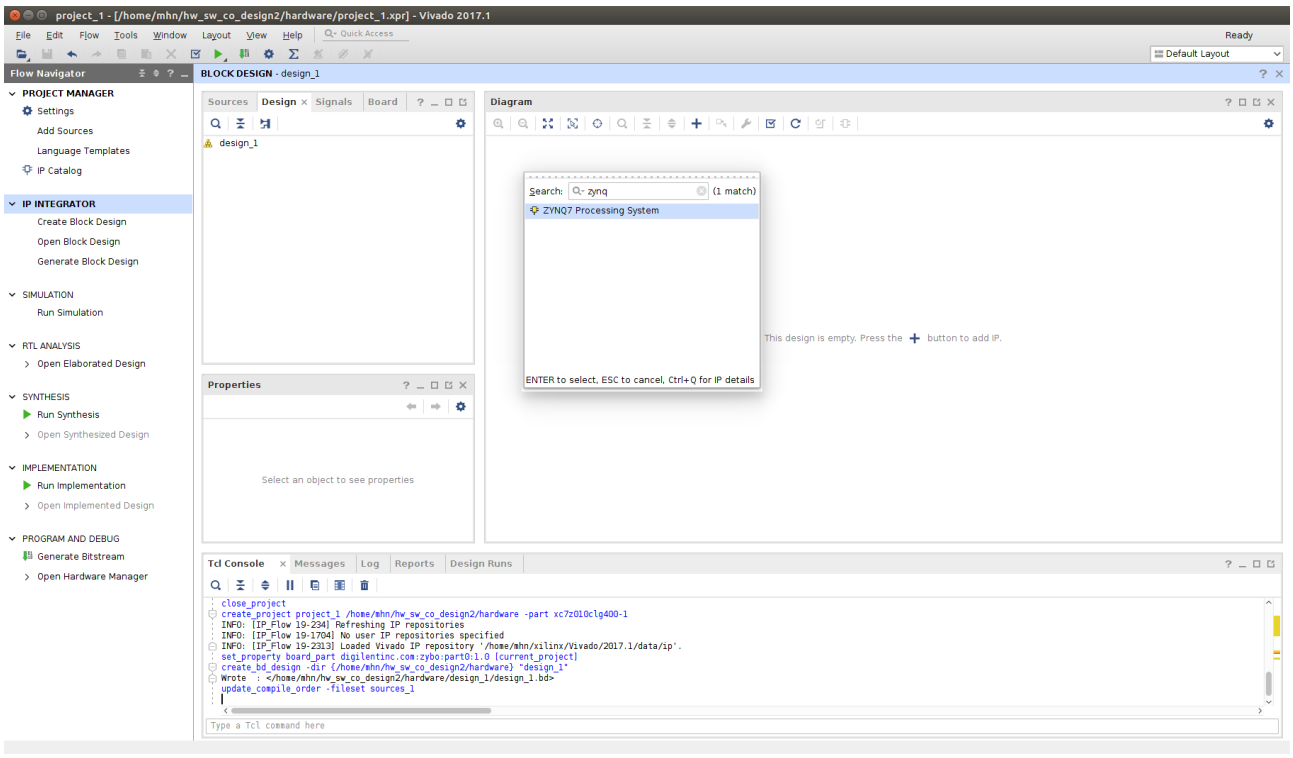

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

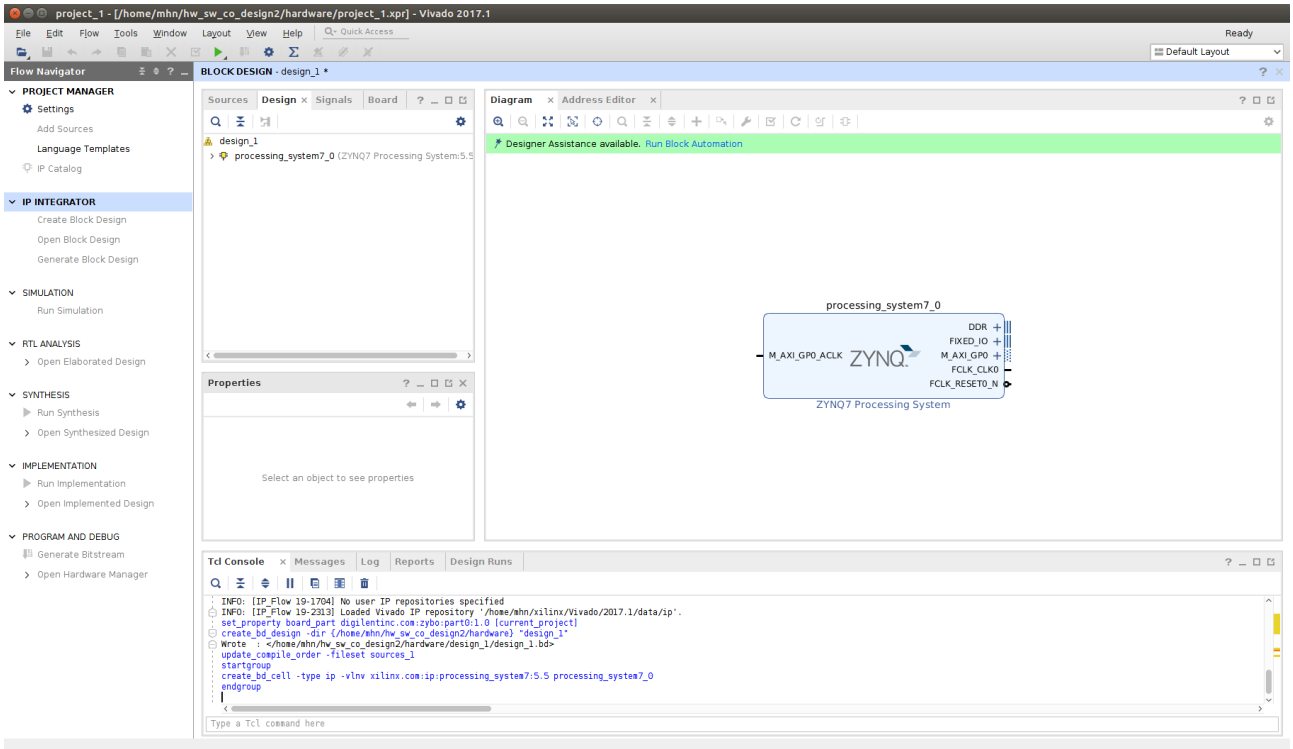

New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Select:
Parts
Boards
Filter/ Preview
Vendor:
All
Display Name:
All
Board Rev:
Latest
Reset All Filters
Search:
Display Name
Vendor
Board Rev
Part
I/O Pir
Zybo Z7-20
digilentinc.com
B.2
xc7z020clg400-1
400
Zybo
digilentinc.com
B.3
xc7z010clg400-1
400
ZedBoard Zynq Evaluation and Development Kit
em.avnet.com
d
xc7z020clg484-1
484
Artix-7 AC701 Evaluation Platform
xilinx.com
1.1
xc7a200tfbg676-2
676
Kintex UltraScale+ KCU116 Evaluation Platform
xilinx.com
1.0
xcku5p-ffvb676-2-e
676
ZYNQ-7 ZC702 Evaluation Board
xilinx.com
1.0
xc7z020clg484-1
484
No Board Connectors
< Back
Next >
Finish
Cancel

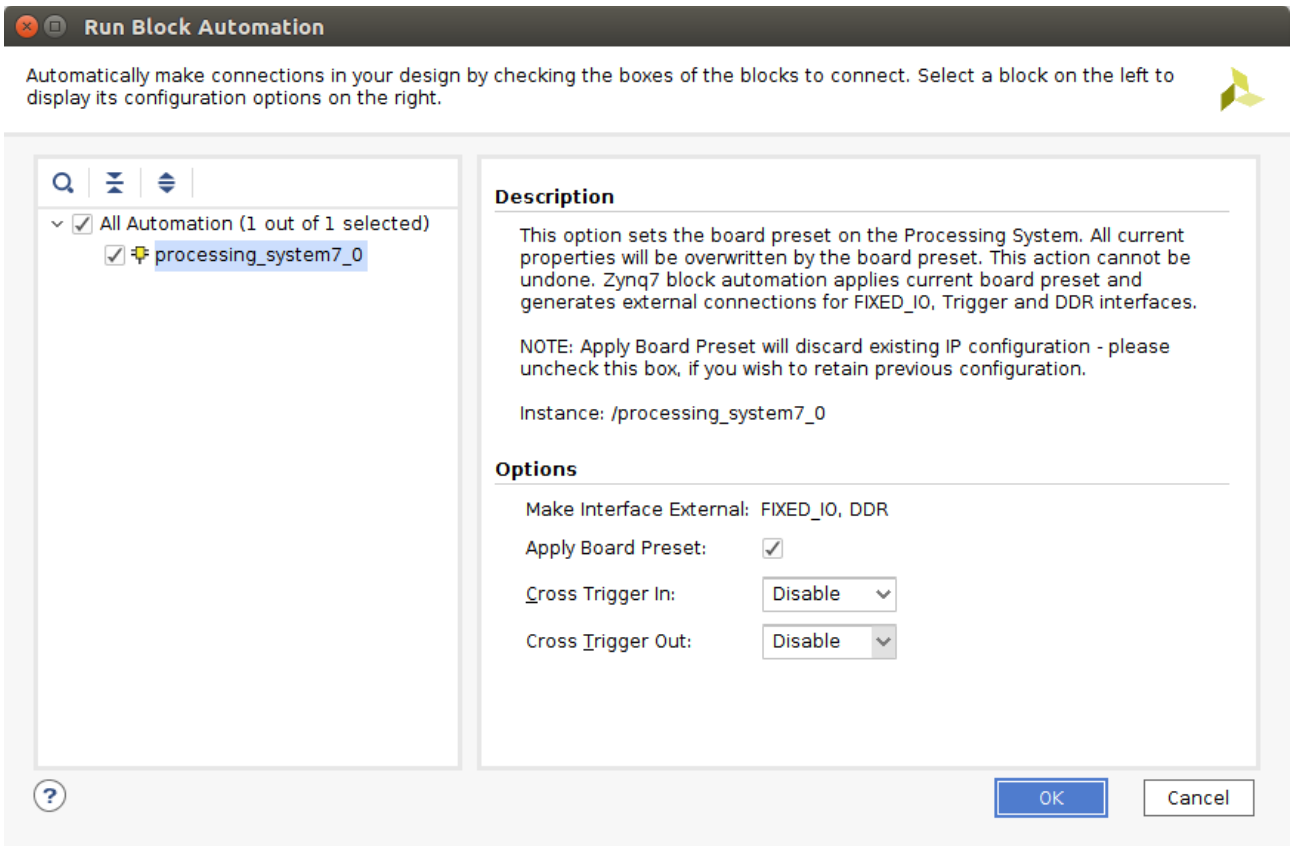

New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'project_1' will be created.
The default part and product family for the new project:
Default Board: Zybo
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1
XILINX
ALL PROGRAMMABLE.
To create the project, click Finish
< Back
Next >
Finish
Cancel

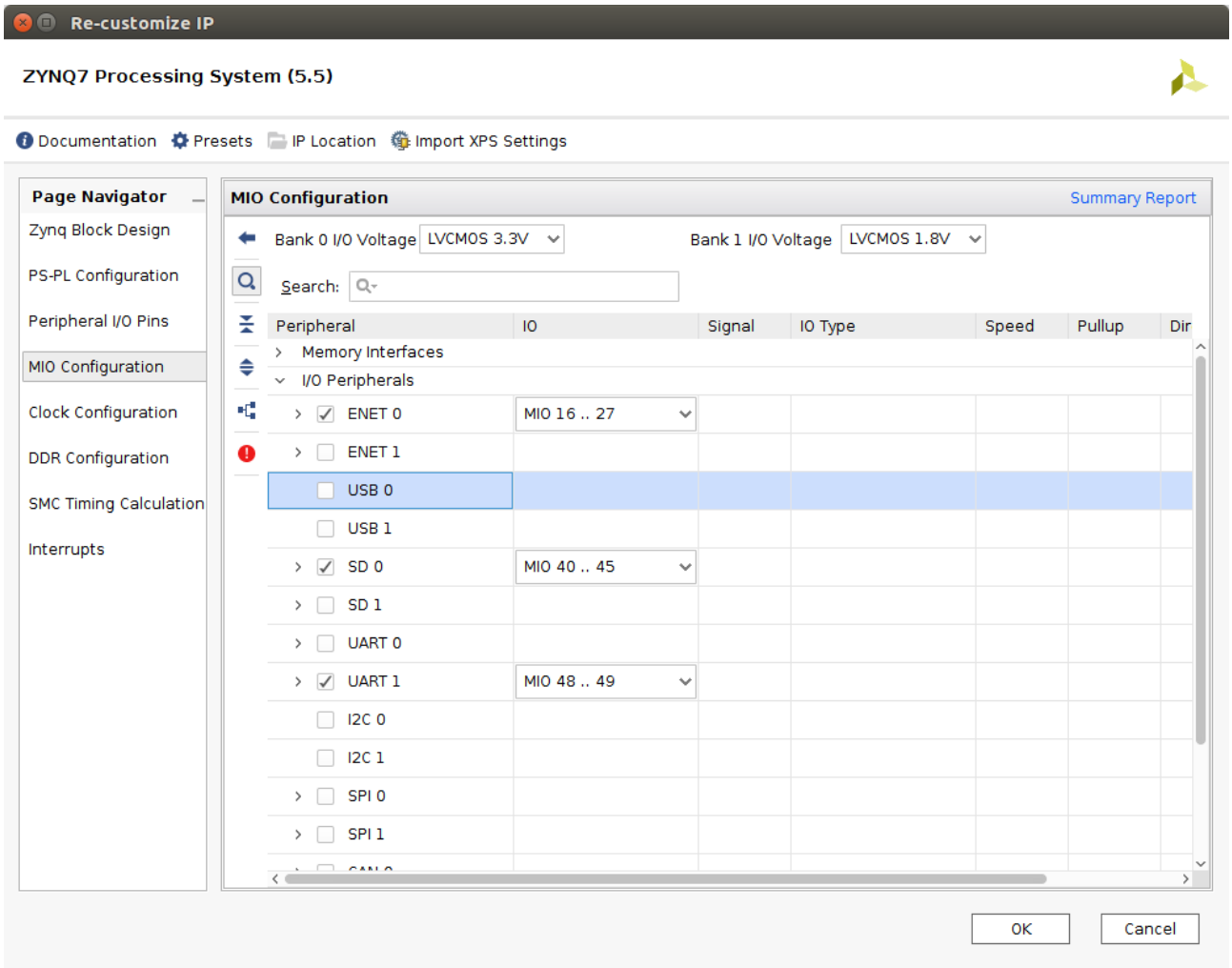

Create Block Design
Please specify name of block design.
Design name:
design_1
Directory:
/home/mhn/hw_sw_co_desig...
Specify source set:
Design Sources
OK
Cancel

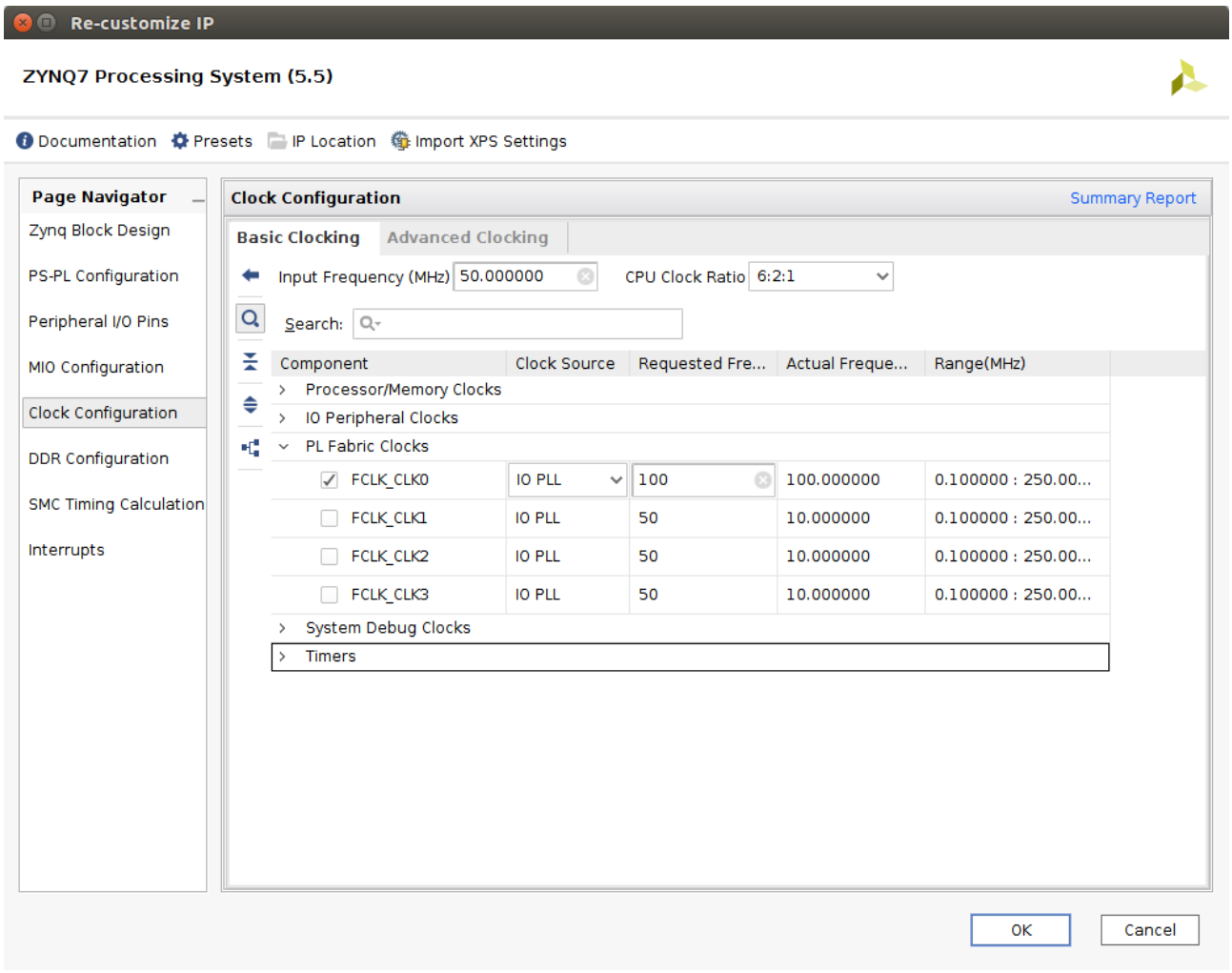

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1
Sources
Design
Signals
Board
design_1
Diagram
This design is empty. Press the + button to add IP.
Properties
Select an object to see properties
Tcl Console
Messages
Log
Reports
Design Runs
close_project
create_project project_1 /home/mhn/hw_sw_co_design2/hardware -part xc7z010clg400-1
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/home/mhn/xilinx/Vivado/2017.1/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
create_bd_design -dir {/home/mhn/hw_sw_co_design2/hardware} "design_1"
Wrote : </home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd>
update_compile_order -fileset sources_1
Type a Tcl command here

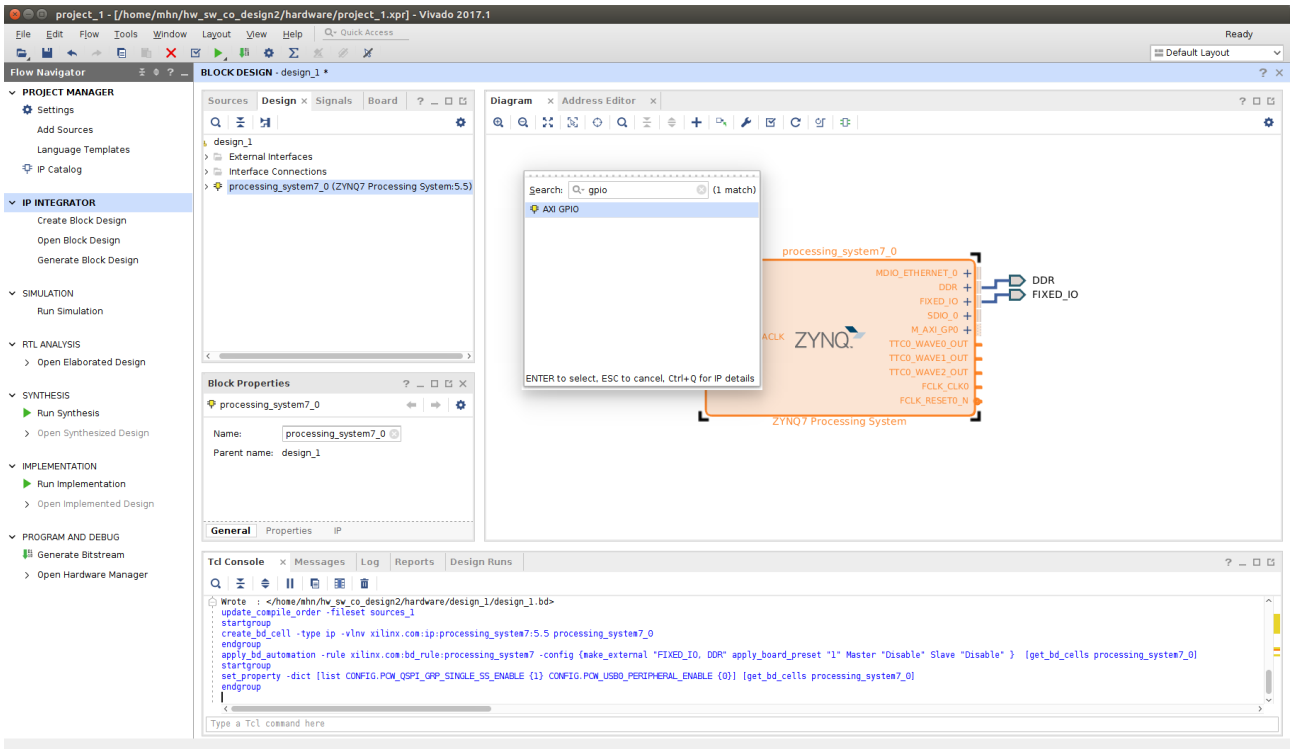

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - design_1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Design
Signals
Board
design_1
Diagram
Search: zynq (1 match)
ZYNQ7 Processing System
ENTER to select, ESC to cancel, Ctrl+Q for IP details
This design is empty. Press the + button to add IP.
Properties
Select an object to see properties
Tcl Console
Messages
Log
Reports
Design Runs
close_project
create_project project_1 /home/mhn/hw_sw_co_design2/hardware -part xc7z010clg400-1
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/home/mhn/xilinx/Vivado/2017.1/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
create_bd_design -dir {/home/mhn/hw_sw_co_design2/hardware} "design_1"
Wrote : </home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd>
update_compile_order -fileset sources_1
Type a Tcl command here

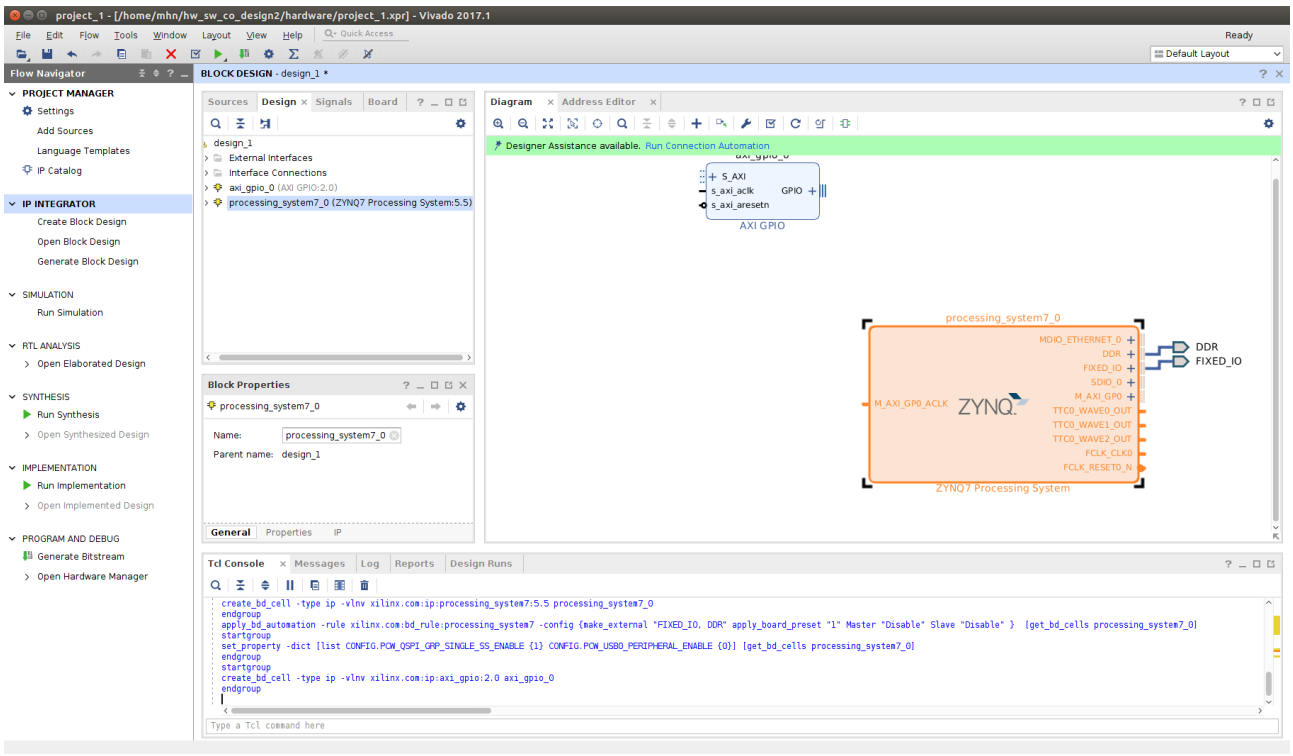

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - design_1 *
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Design
Signals
Board
design_1
processing_system7_0 (ZYNQ7 Processing System:5.5
Diagram
Address Editor
Designer Assistance available. Run Block Automation
processing_system7_0
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ7
ZYNQ7 Processing System
Properties
Select an object to see properties
Tcl Console
Messages
Log
Reports
Design Runs
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/home/mhn/xilinx/Vivado/2017.1/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
create_bd_design -dir {/home/mhn/hw_sw_co_design2/hardware} "design_1"
Wrote : </home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd>
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
Type a Tcl command here

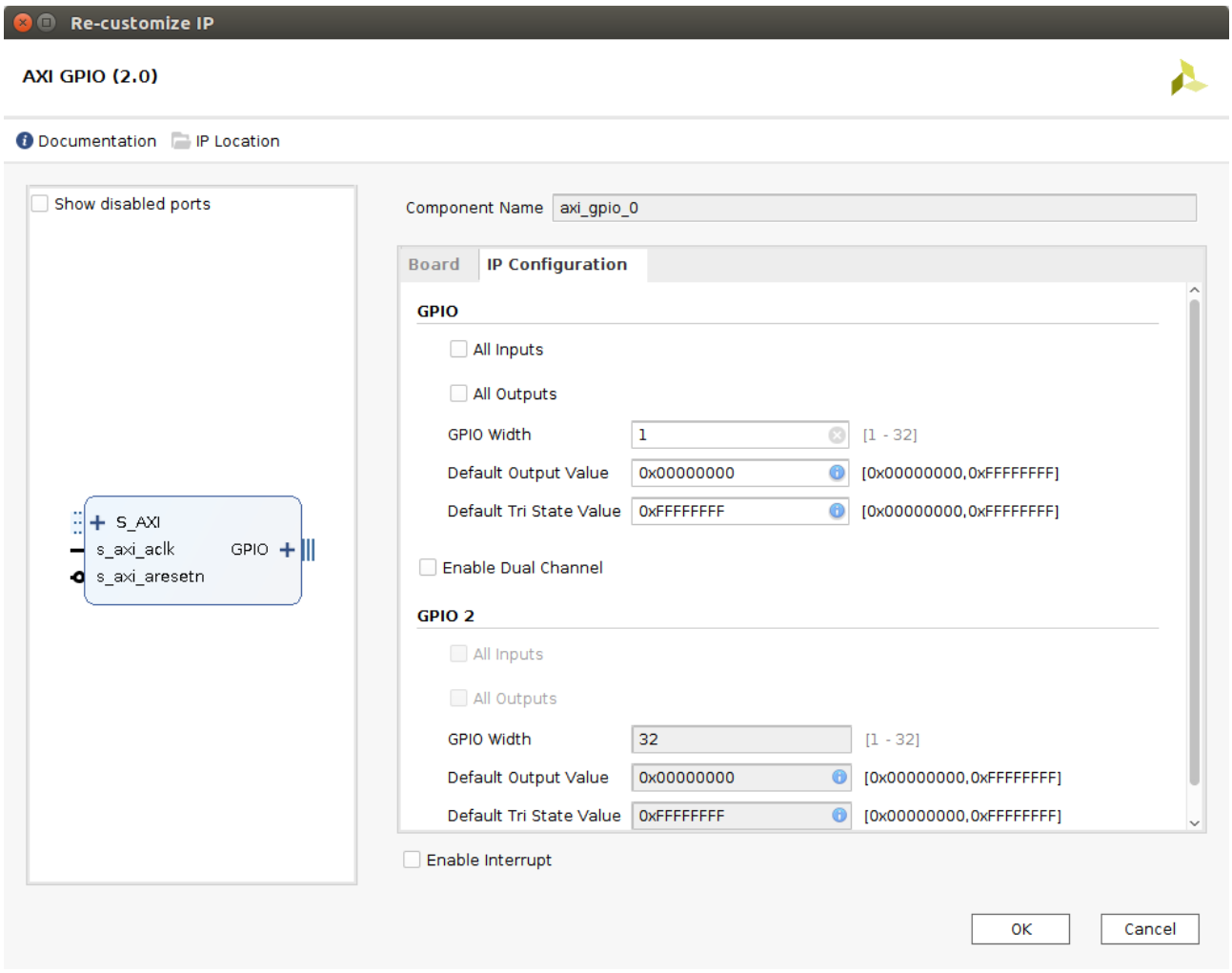

Run Block Automation
Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.
All Automation (1 out of 1 selected)
processing_system7_0
Description
This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone. Zynq7 block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.
NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.
Instance: /processing_system7_0
Options
Make Interface External: FIXED_IO, DDR
Apply Board Preset:
Cross Trigger In: Disable
Cross Trigger Out: Disable
OK
Cancel

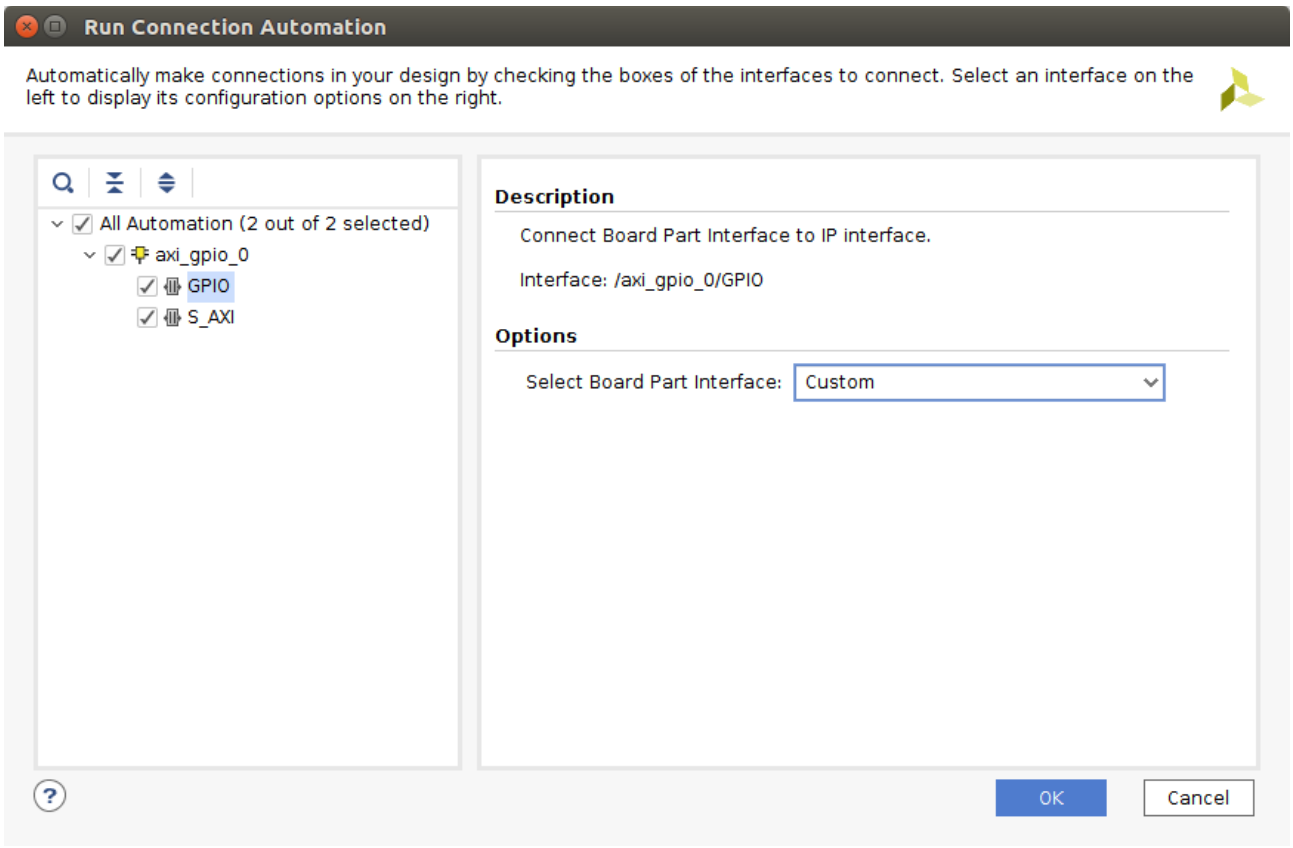

Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
MIO Configuration
Summary Report
Bank 0 I/O Voltage LVCMOS 3.3V
Bank 1 I/O Voltage LVCMOS 1.8V
Search:
Peripheral
IO
Signal
IO Type
Speed
Pullup
Dir
Memory Interfaces
I/O Peripherals
ENET 0
MIO 16 .. 27
ENET 1
USB 0
USB 1
SD 0
MIO 40 .. 45
SD 1
UART 0
UART 1
MIO 48 .. 49
I2C 0
I2C 1
SPI 0
SPI 1
OK
Cancel

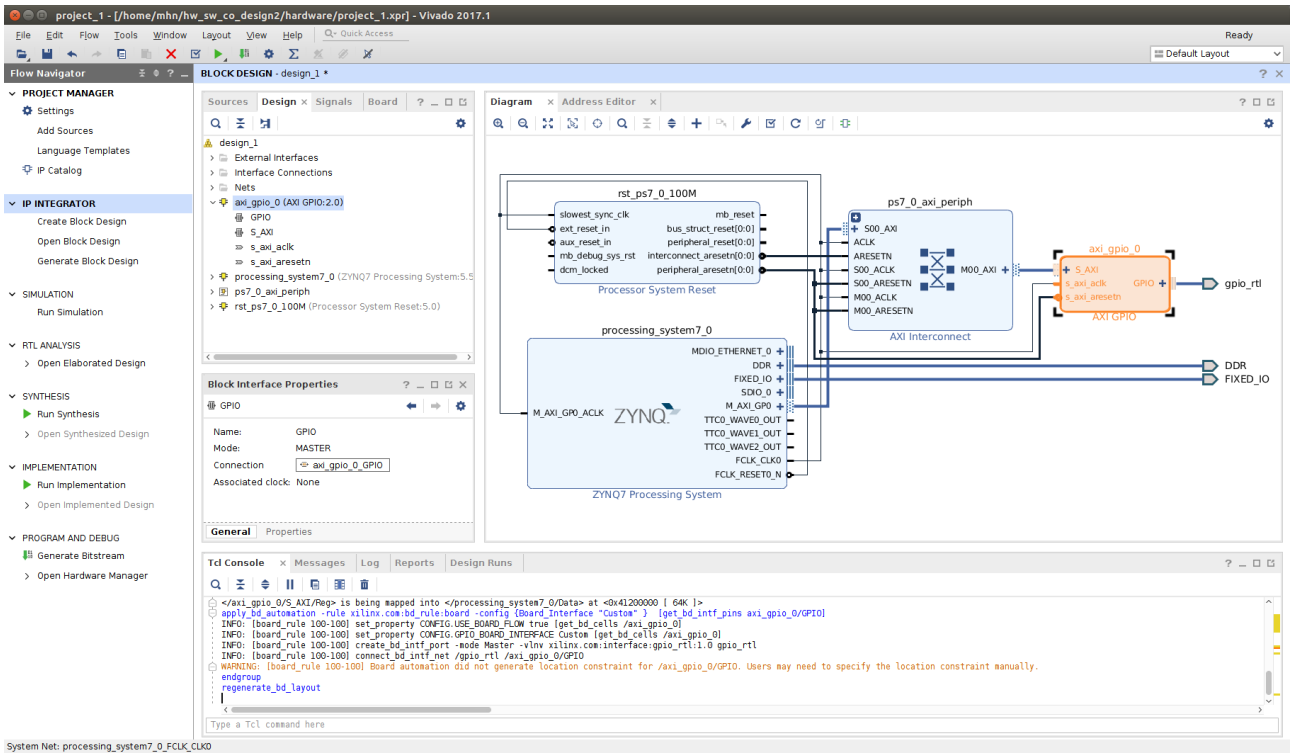

Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Clock Configuration
Summary Report
Basic Clocking
Advanced Clocking
Input Frequency (MHz) 50.000000
CPU Clock Ratio 6:2:1
Search:
Component
Clock Source
Requested Fre...
Actual Freque...
Range(MHz)
Processor/Memory Clocks
IO Peripheral Clocks
PL Fabric Clocks
FCLK_CLK0 IO PLL 100 100.000000 0.100000 : 250.00...
FCLK_CLK1 IO PLL 50 10.000000 0.100000 : 250.00...
FCLK_CLK2 IO PLL 50 10.000000 0.100000 : 250.00...
FCLK_CLK3 IO PLL 50 10.000000 0.100000 : 250.00...
System Debug Clocks
Timers
OK
Cancel

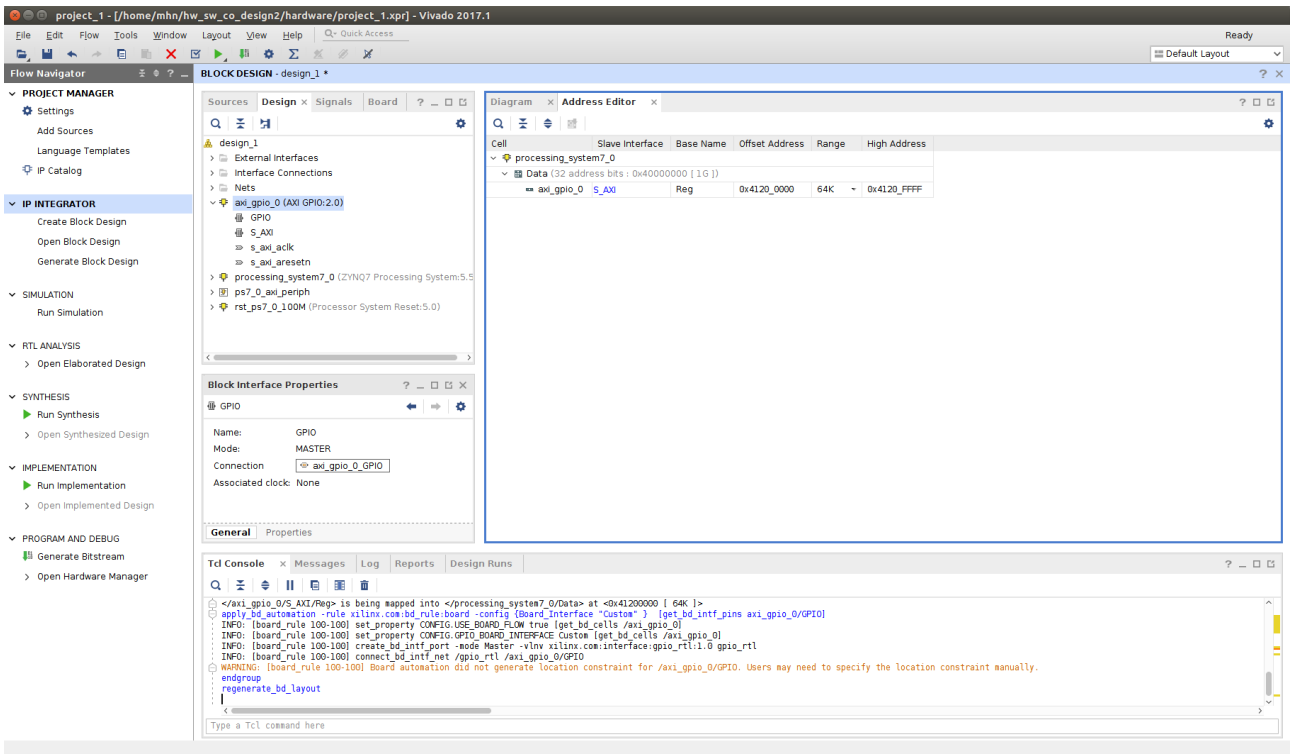

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
Flow Navigator
PROJECT MANAGER
IP INTEGRATOR
SIMULATION
RTL ANALYSIS
SYNTHESIS
IMPLEMENTATION
PROGRAM AND DEBUG
BLOCK DESIGN - design_1
Sources
Design
Signals
Board
Diagram
Address Editor
design_1
External Interfaces
Interface Connections
processing_system7_0 (ZYNQ7 Processing System:5.5)
Search: gpio (1 match)
AXI GPIO
ENTER to select, ESC to cancel, Ctrl+Q for IP details
processing_system7_0
ZYNQ7 Processing System
DDR
FIXED_IO
Block Properties
Name: processing_system7_0
Parent name: design_1
Tcl Console
Messages
Log
Reports
Design Runs
Type a Tcl command here

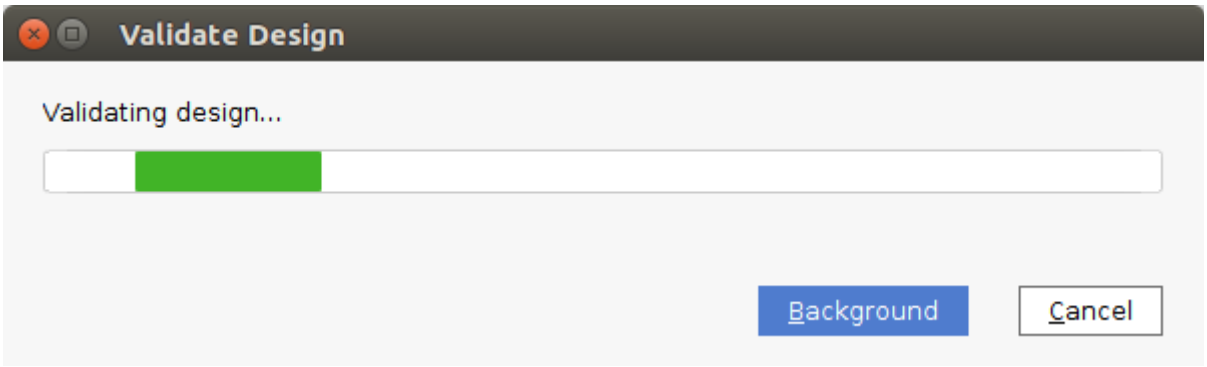

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Board
design_1
External Interfaces
Interface Connections
axi_gpio_0 (AXI GPIO:2.0)
processing_system7_0 (ZYNQ7 Processing System:5.5)
Block Properties
processing_system7_0
Name: processing_system7_0
Parent name: design_1
General
Properties
IP
Diagram
Address Editor
Designer Assistance available. Run Connection Automation
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
processing_system7_0
MDIO_ETHERNET_0
DDR
FIXED_IO
SDIO_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ7
ZYNQ7 Processing System
DDR
FIXED_IO
Tcl Console
Messages
Log
Reports
Design Runs
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
startgroup
set_property -dict [list CONFIG.PCW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.PCW_USB0_PERIPHERAL_ENABLE {0}] [get_bd_cells processing_system7_0]
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_gpio:2.0 axi_gpio_0
endgroup
Type a Tcl command here

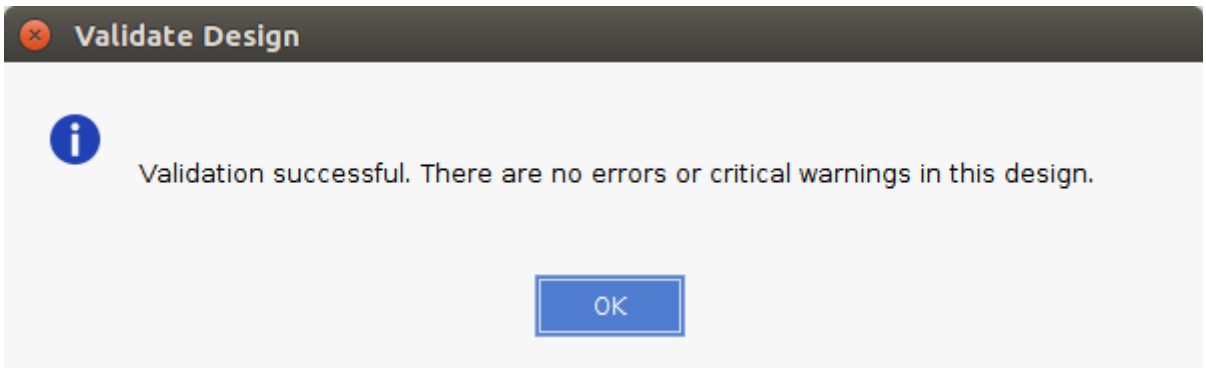

Re-customize IP
AXI GPIO (2.0)
Documentation
IP Location
Show disabled ports
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
Component Name
axi_gpio_0
Board
IP Configuration
GPIO
All Inputs
All Outputs
GPIO Width
1
[1 - 32]
Default Output Value
0x00000000
[0x00000000,0xFFFFFFFF]
Default Tri State Value
0xFFFFFFFF
[0x00000000,0xFFFFFFFF]
Enable Dual Channel
GPIO 2
All Inputs
All Outputs
GPIO Width
32
[1 - 32]
Default Output Value
0x00000000
[0x00000000,0xFFFFFFFF]
Default Tri State Value
0xFFFFFFFF
[0x00000000,0xFFFFFFFF]
Enable Interrupt
OK
Cancel

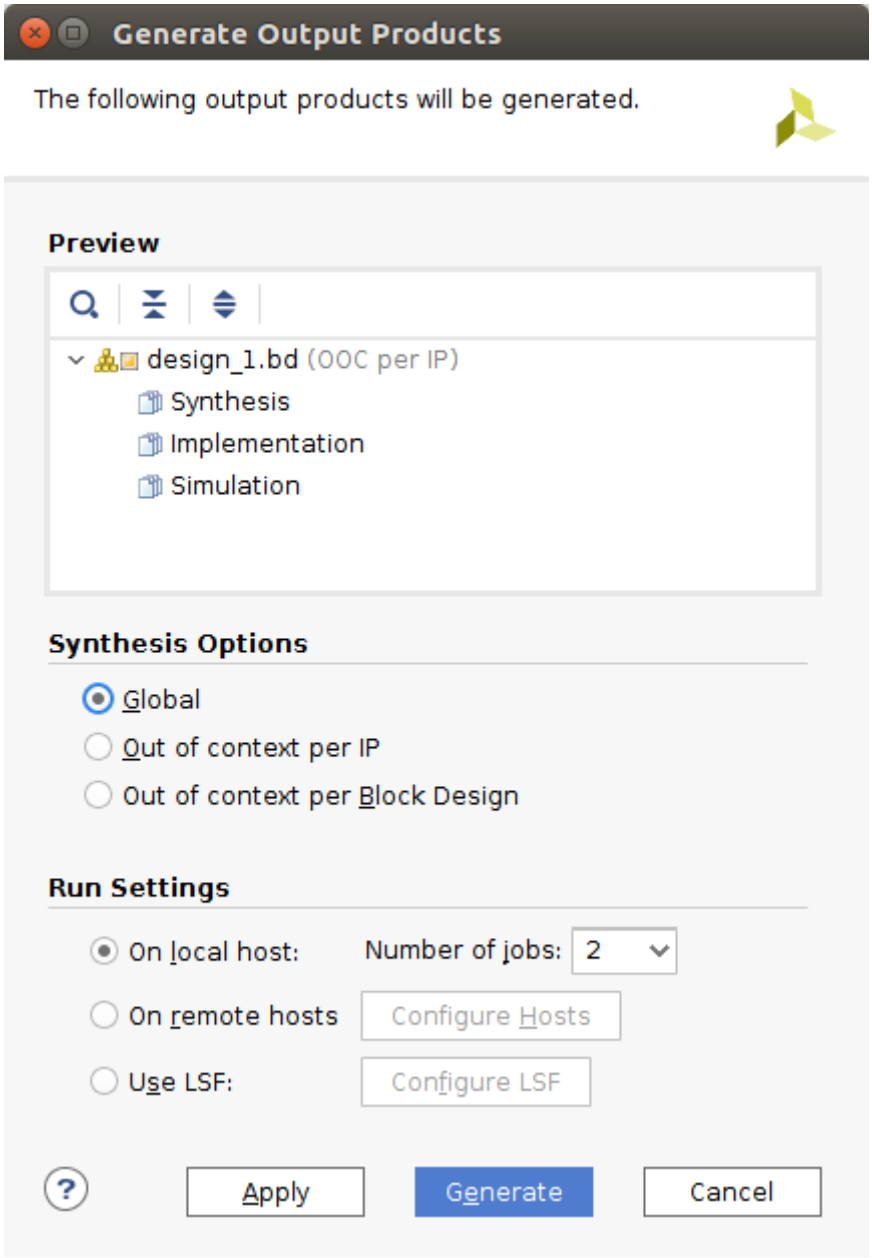

Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (2 out of 2 selected)
axi_gpio_0
GPIO
S_AXI
Description
Connect Board Part Interface to IP interface.
Interface: /axi_gpio_0/GPIO
Options
Select Board Part Interface:
Custom
OK
Cancel

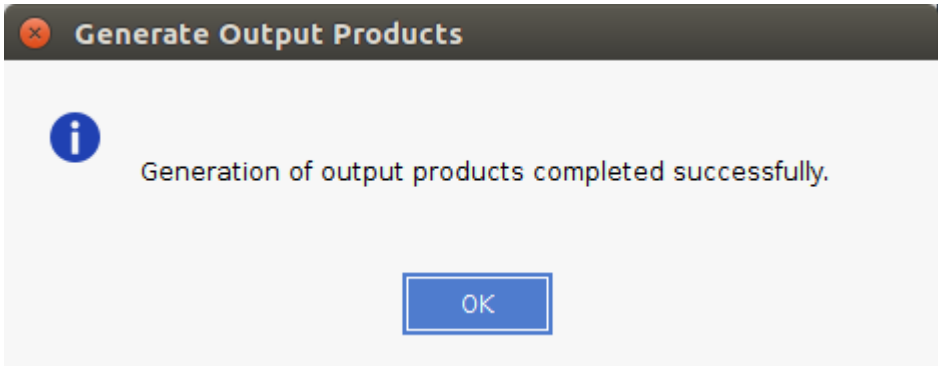

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources Design Signals Board
design_1
External Interfaces
Interface Connections
Nets
axi_gpio_0 (AXI GPIO:2.0)
GPIO
S_AXI
s_axi_aclk
s_axi_aresetn
processing_system7_0 (ZYNQ7 Processing System:5.5
ps7_0_axi_periph
rst_ps7_0_100M (Processor System Reset:5.0)
Block Interface Properties
GPIO
Name: GPIO
Mode: MASTER
Connection axi_gpio_0_GPIO
Associated clock: None
General Properties
Diagram Address Editor
rst_ps7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
gpio_rtl
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
MDIO_ETHERNET_0
DDR
FIXED_IO
SDIO_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO
Tcl Console Messages Log Reports Design Runs
</axi_gpio_0/S_AXI/Reg> is being mapped into </processing_system7_0/Data> at <0x41200000 [ 64K ]>
apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "Custom" } [get_bd_intf_pins axi_gpio_0/GPIO]
INFO: [board_rule 100-100] set_property CONFIG.USE_BOARD_FLOW true [get_bd_cells /axi_gpio_0]
INFO: [board_rule 100-100] set_property CONFIG.GPIO_BOARD_INTERFACE Custom [get_bd_cells /axi_gpio_0]
INFO: [board_rule 100-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl:1.0 gpio_rtl
INFO: [board_rule 100-100] connect_bd_intf_net /gpio_rtl /axi_gpio_0/GPIO
WARNING: [board_rule 100-100] Board automation did not generate location constraint for /axi_gpio_0/GPIO. Users may need to specify the location constraint manually.
endgroup
regenerate_bd_layout
Type a Tcl command here
System Net: processing_system7_0_FCLK_CLK0

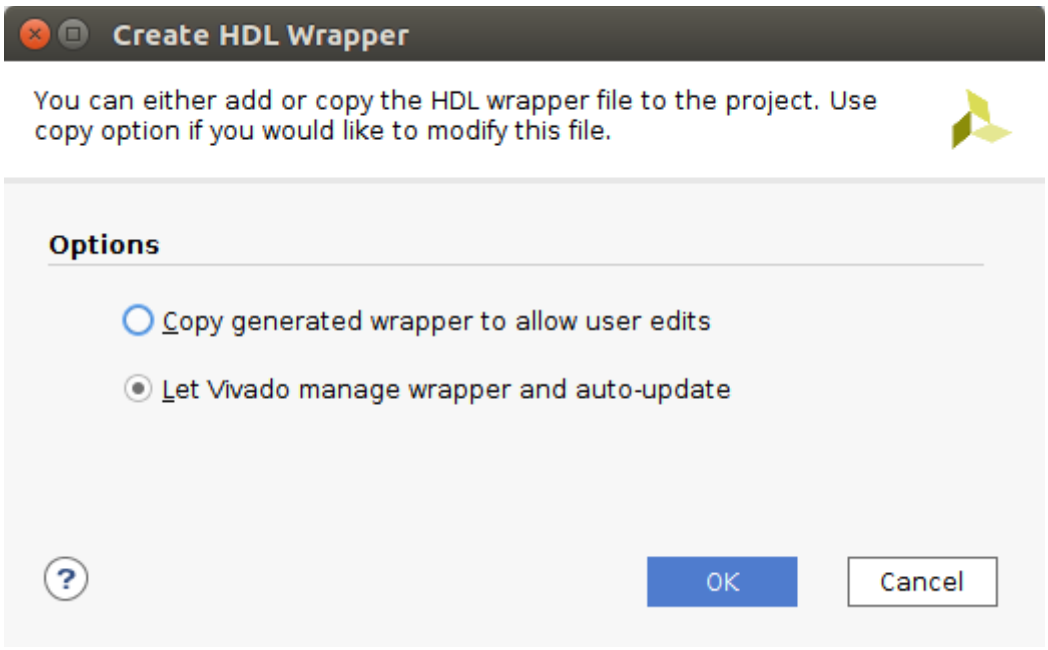

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Board
design_1
External Interfaces
Interface Connections
Nets
axi_gpio_0 (AXI GPIO:2.0)
GPIO
S_AXI
s_axi_aclk
s_axi_aresetn
processing_system7_0 (ZYNQ7 Processing System:5.5
ps7_0_axi_periph
rst_ps7_0_100M (Processor System Reset:5.0)
Block Interface Properties
GPIO
Name: GPIO
Mode: MASTER
Connection axi_gpio_0_GPIO
Associated clock: None
General
Properties
Diagram
Address Editor
Cell
Slave Interface
Base Name
Offset Address
Range
High Address
processing_system7_0
Data (32 address bits : 0x40000000 [ 1G ])
axi_gpio_0
S_AXI
Reg
0x4120_0000
64K
0x4120_FFFF
Tcl Console
Messages
Log
Reports
Design Runs
</axi_gpio_0/S_AXI/Reg> is being mapped into </processing_system7_0/Data> at <0x41200000 [ 64K ]>
apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "Custom" } [get_bd_intf_pins axi_gpio_0/GPIO]
INFO: [board_rule 100-100] set_property CONFIG.USE_BOARD_FLOW true [get_bd_cells /axi_gpio_0]
INFO: [board_rule 100-100] set_property CONFIG.GPIO_BOARD_INTERFACE Custom [get_bd_cells /axi_gpio_0]
INFO: [board_rule 100-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl:1.0 gpio_rtl
INFO: [board_rule 100-100] connect_bd_intf_net /gpio_rtl /axi_gpio_0/GPIO
WARNING: [board_rule 100-100] Board automation did not generate location constraint for /axi_gpio_0/GPIO. Users may need to specify the location constraint manually.
endgroup
regenerate_bd_layout
Type a Tcl command here

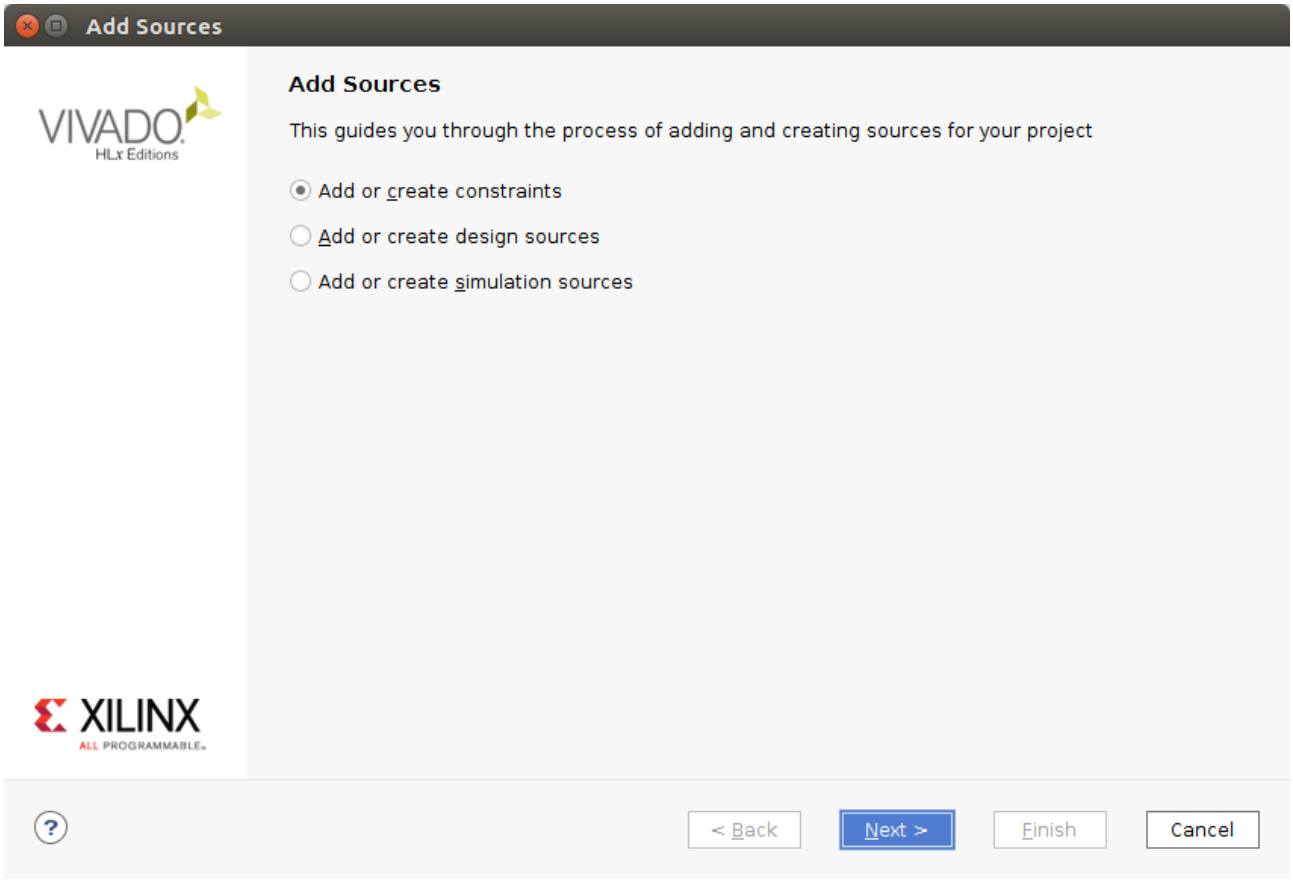

Validate Design
Validating design...
Background
Cancel

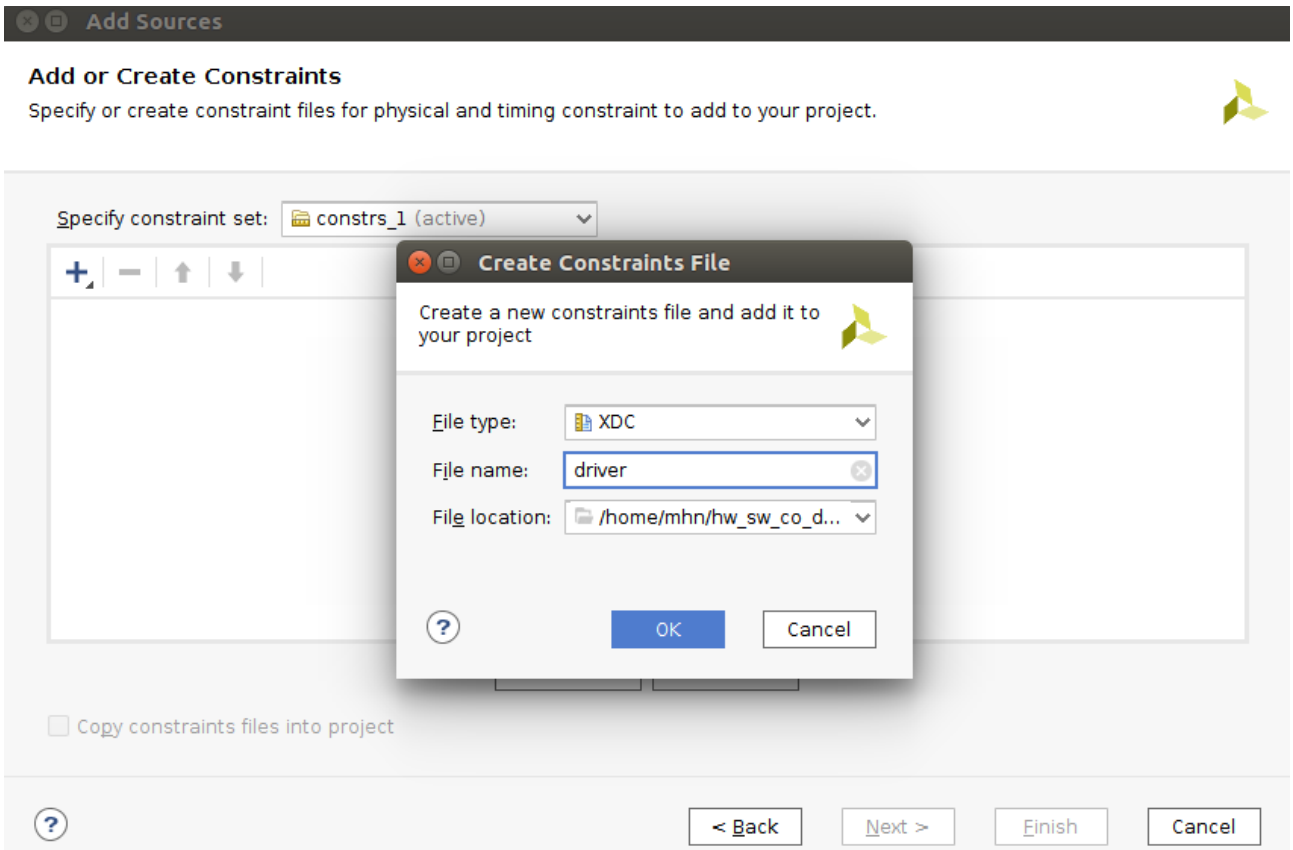

Validate Design
Validation successful. There are no errors or critical warnings in this design.
OK

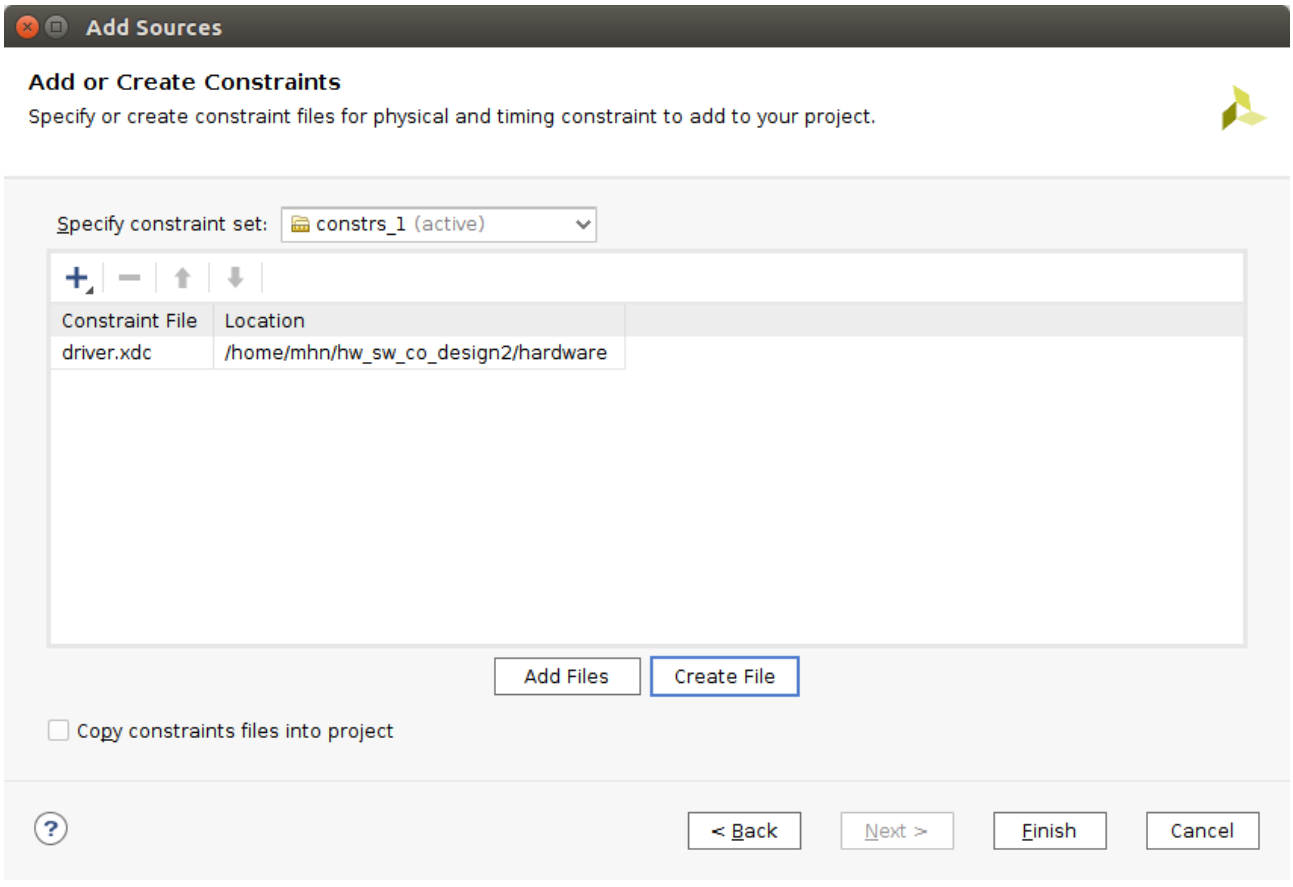

Generate Output Products
The following output products will be generated.
Preview
design_1.bd (OOC per IP)
Synthesis
Implementation
Simulation
Synthesis Options
Global
Out of context per IP
Out of context per Block Design
Run Settings
On local host:
Number of jobs:
2
On remote hosts
Configure Hosts
Use LSF:
Configure LSF
Apply
Generate
Cancel

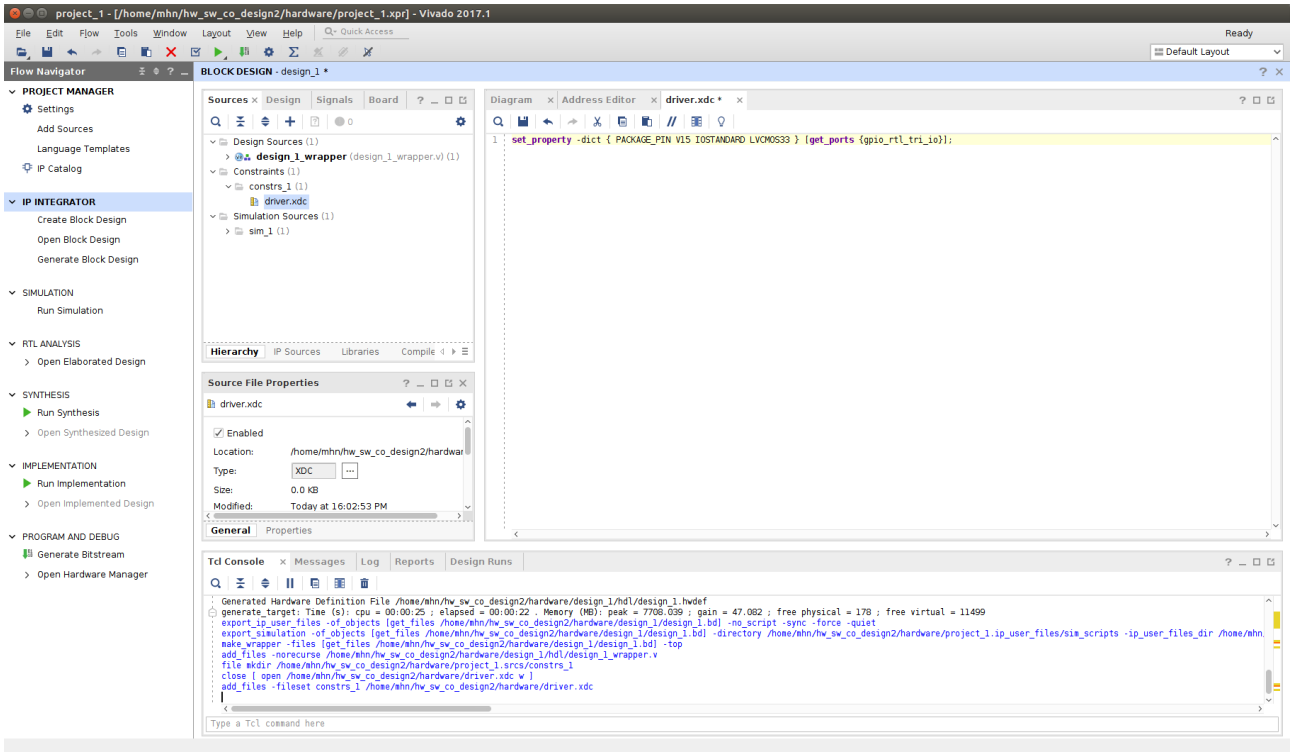

Generate Output Products
Generation of output products completed successfully.
OK

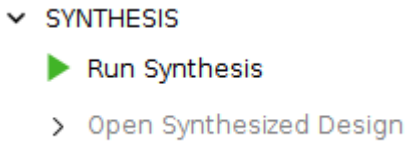

Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
OK
Cancel

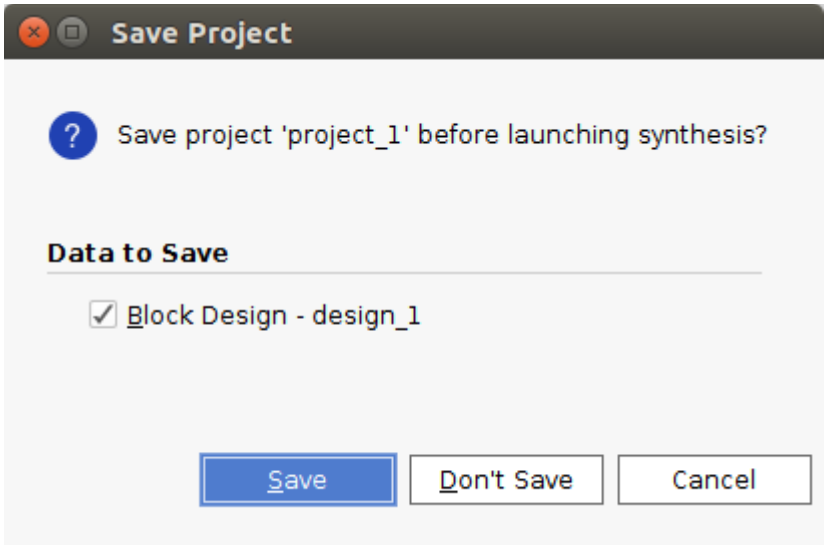

Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
ALL PROGRAMMABLE
< Back
Next >
Finish
Cancel

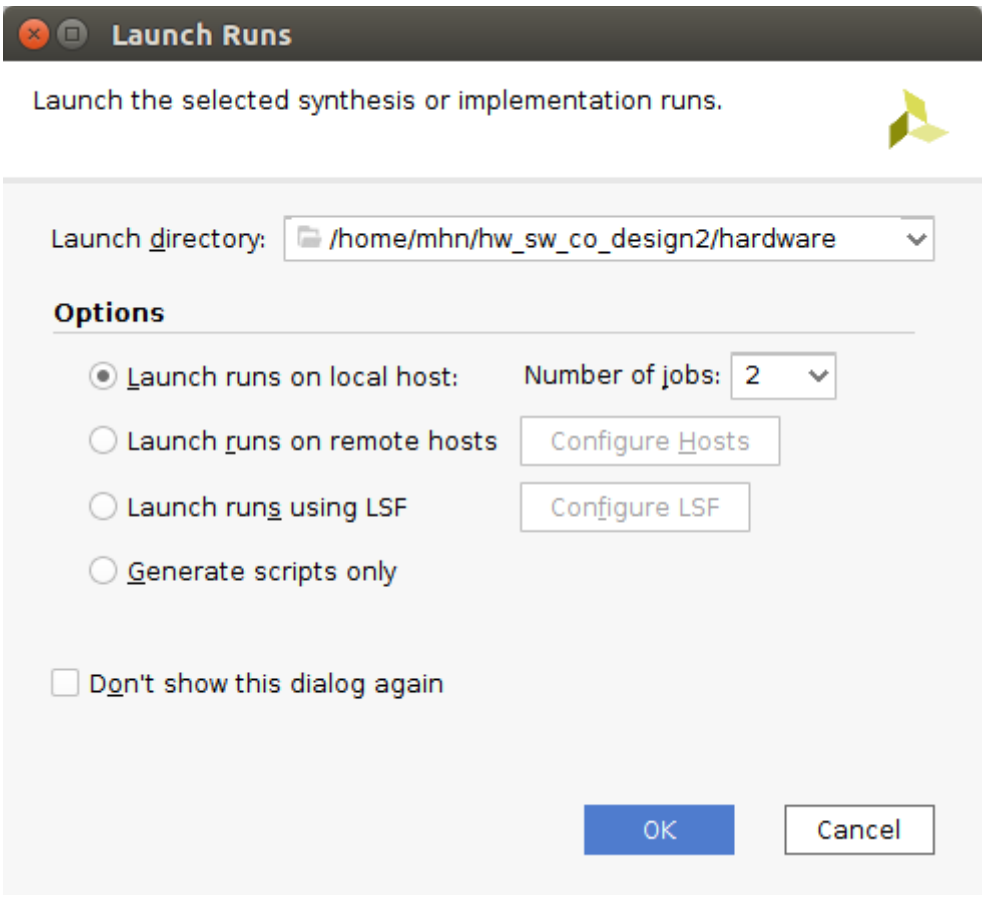

Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
driver
File location:
/home/mhn/hw_sw_co_d...
OK
Cancel
Copy constraints files into project
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Constraint File
Location
driver.xdc
/home/mhn/hw_sw_co_design2/hardware
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

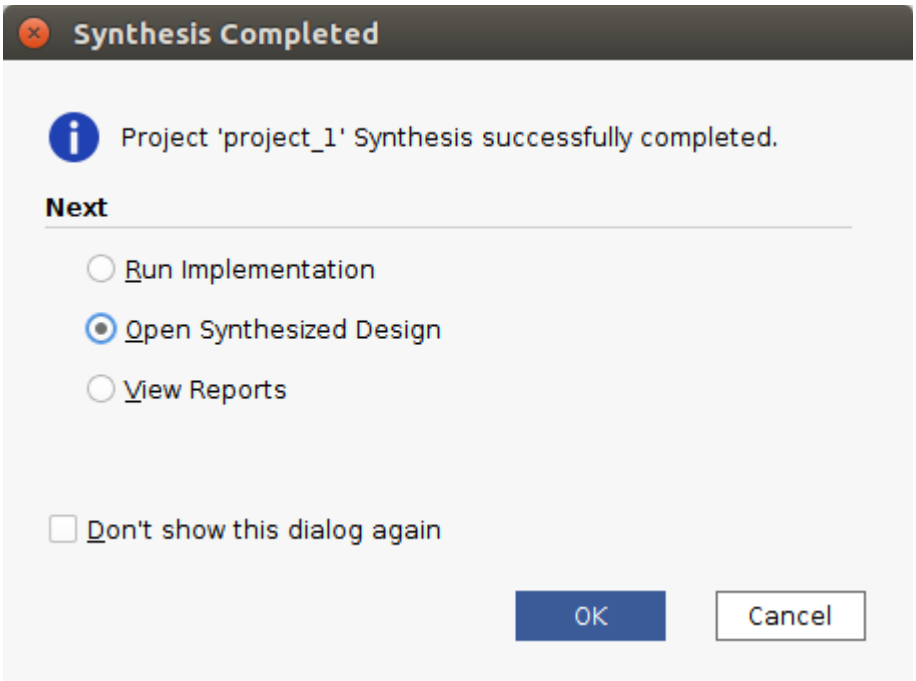

project_1 - [/home/mhn/hw_sw_co_design2/hardware/project_1.xpr] - Vivado 2017.1
File Edit Flow Tools Window Layout View Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1 *
Sources
Design
Signals
Board
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints (1)
constrs_1 (1)
driver.xdc
Simulation Sources (1)
sim_1 (1)
Hierarchy
IP Sources
Libraries
Source File Properties
driver.xdc
Enabled
Location:
Type:
XDC
Size:
0.0 KB
Modified:
Today at 16:02:53 PM
General
Properties
Diagram
Address Editor
driver.xdc *
set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [get_ports {gpio_rtl_tri_io}];
Tcl Console
Messages
Log
Reports
Design Runs
Generated Hardware Definition File /home/mhn/hw_sw_co_design2/hardware/design_1/hdl/design_1.hwdef
generate_target: Time (s): cpu = 00:00:25 ; elapsed = 00:00:22 . Memory (MB): peak = 7708.039 ; gain = 47.082 ; free physical = 178 ; free virtual = 11499
export_ip_user_files -of_objects [get_files /home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd] -no_script -sync -force -quiet
export_simulation -of_objects [get_files /home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd] -directory /home/mhn/hw_sw_co_design2/hardware/project_1.ip_user_files/sim_scripts -ip_user_files_dir /home/mhn
make_wrapper -files [get_files /home/mhn/hw_sw_co_design2/hardware/design_1/design_1.bd] -top
add_files -norecurse /home/mhn/hw_sw_co_design2/hardware/design_1/hdl/design_1_wrapper.v
file mkdir /home/mhn/hw_sw_co_design2/hardware/project_1.srcs/constrs_1
close [ open /home/mhn/hw_sw_co_design2/hardware/driver.xdc w ]
add_files -fileset constrs_1 /home/mhn/hw_sw_co_design2/hardware/driver.xdc
Type a Tcl command here

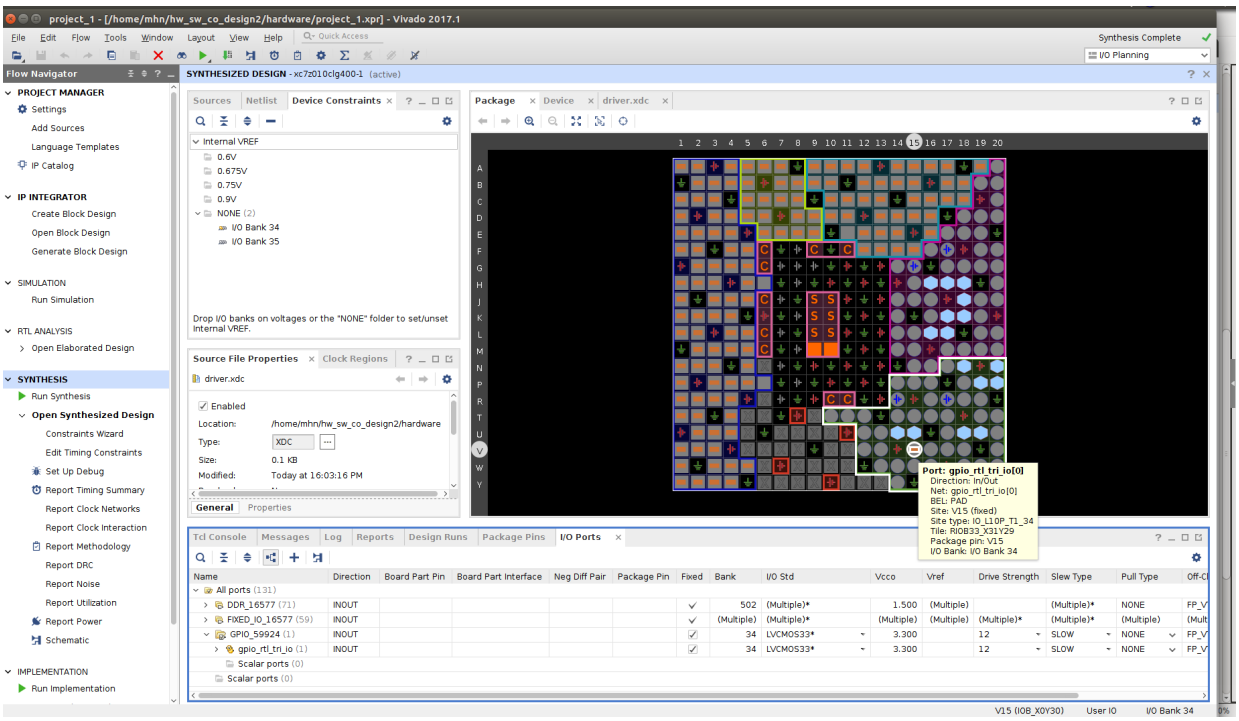

SYNTHESIS
Run Synthesis
Open Synthesized Design


Save Project
Save project 'project_1' before launching synthesis?
Data to Save
Block Design - design_1
Save
Don't Save
Cancel

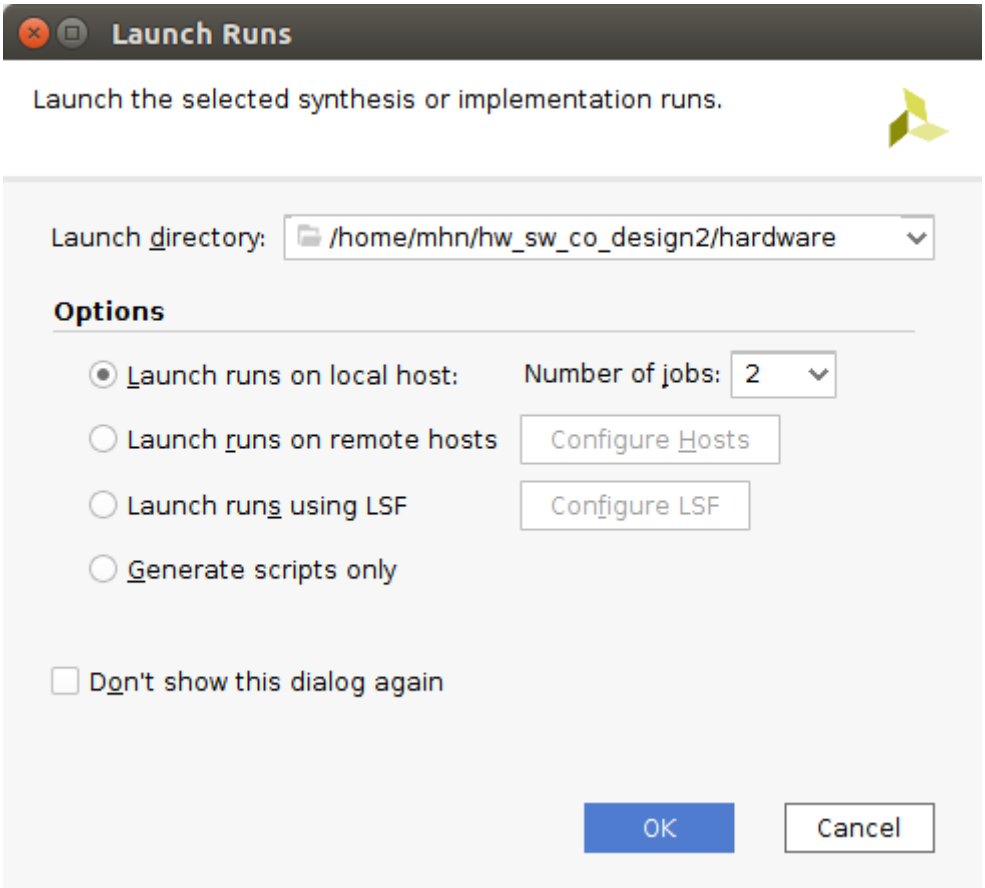

Launch Runs
Launch the selected synthesis or implementation runs.
Launch directory:
/home/mhn/hw_sw_co_design2/hardware
Options
Launch runs on local host:
Number of jobs:
2
Launch runs on remote hosts
Configure Hosts
Launch runs using LSF
Configure LSF
Generate scripts only
Don't show this dialog again
OK
Cancel


Running synth_design
Cancel


Synthesis Completed
Project 'project_1' Synthesis successfully completed.
Next
Run Implementation
Open Synthesized Design
View Reports
Don't show this dialog again
OK
Cancel




Generate Bitstream



cd xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers/

sudo ./install_drivers

```
mhn@mhn-Z20NH-AS51B5U:~/xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers$ sudo ./install_drivers
[sudo] password for mhn:
INFO: Installing cable drivers.
INFO: Script name = ./install_drivers
INFO: HostName = mhn-Z20NH-AS51B5U
INFO: Current working dir = /home/mhn/xilinx/Vivado/2017.1/data/xicom/cable_drivers/lin64/install_script/install_drivers
INFO: Kernel version = 4.13.0-43-generic.
INFO: Arch = x86_64.
USB udev file exists and will not be updated.
--File /etc/udev/rules.d/52-xilinx-ftdi-usb.rules exists.
--File /etc/udev/rules.d/52-xilinx-ftdi-usb.rules version =
--File 52-xilinx-ftdi-usb.rules exists.
--File 52-xilinx-ftdi-usb.rules version =
--File 52-xilinx-ftdi-usb.rules is newer than the destination file.
--Updating rules file.
--File /etc/udev/rules.d/52-xilinx-pcusb.rules exists.
--File /etc/udev/rules.d/52-xilinx-pcusb.rules version = 0002
--File 52-xilinx-pcusb.rules exists.
--File 52-xilinx-pcusb.rules version = 0002
--File 52-xilinx-pcusb.rules is already updated.

INFO: Digilent Return code = 0
INFO: Xilinx Return code = 0
INFO: Xilinx FTDI Return code = 0
INFO: Return code = 0
INFO: Driver installation successful.
CRITICAL WARNING: Cable(s) on the system must be unplugged then plugged back in order for the driver scripts to update the cables.
```

cd ../../../../../../../../../

~/hw_sw_co_design$
petalinux-create -t project -n software --template zynq

~/hw_sw_co_design/hardware/driver_lab.sdk$
petalinux-config --get-hw-description -p ../../software/

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/hardware/driver_lab.sdk$ petalinux-config --get-hw-description -p ../../software/
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename design_1_wrapper.hdf to system.hdf

****** hsi v2015.4 (64-bit)
  **** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
    ** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/mhn/hw_sw_co_design/software/build/linux/hw-description/hw-description.tcl -notrace
INFO: [Common 17-206] Exiting hsi at Thu May 31 11:48:12 2018...
INFO: Config linux
[INFO ] config linux
configuration written to /home/mhn/hw_sw_co_design/software/subsystems/linux/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

[INFO ] generate DTS to /home/mhn/hw_sw_co_design/software/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 3 seconds
WARNING: ps7_ethernet_0: No reset found
INFO: [Common 17-206] Exiting hsi at Thu May 31 11:48:32 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 11:48:51 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 1 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 11:49:10 2018...
[INFO ] oldconfig linux/u-boot
```

~/hw_sw_co_design/software/components/bootloader/zynq_fsbl$ ls

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software/components/bootloader/zynq_fsbl$ ls
fsbl_debug.h    fsbl_hooks.h   main.c    nand.c  pcap.c      ps7_parameters.xml  rsa.h
fsbl.h          image_mover.c  Makefile  nand.h  pcap.h      qspi.c              sd.c
fsbl_handoff.S  image_mover.h  md5.c     nor.c   ps7_init.c  qspi.h              sd.h
fsbl_hooks.c    lscript.ld     md5.h     nor.h   ps7_init.h  rsa.c               zynq_fsbl_bsp
```

FPGA 베이스의 Cortex-A9 부트 코드를 볼 수 있다

~/hw_sw_co_design/software$ petalinux-config -c u-boot

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config -c u-boot
INFO: Checking component...
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
#
# configuration written to .config
#
[INFO ] config linux/u-boot


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

~/hw_sw_co_design/software$ petalinux-build

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build system.dtb
[INFO ] build linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] build zynq_fsbl
[INFO ] build linux/rootfs/fwupgrade
[INFO ] build linux/rootfs/peekpoke
[INFO ] build kernel in-tree modules
[INFO ] modules linux/kernel
[INFO ] post-build linux/rootfs/fwupgrade
[INFO ] post-build linux/rootfs/peekpoke
[INFO ] pre-install linux/rootfs/fwupgrade
[INFO ] pre-install linux/rootfs/peekpoke
[INFO ] install system.dtb
[INFO ] install linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] install linux/u-boot
[INFO ] install sys_init
[INFO ] install linux/rootfs/fwupgrade
[INFO ] install linux/rootfs/peekpoke
[INFO ] install kernel in-tree modules
[INFO ] modules_install linux/kernel
[INFO ] post-install linux/rootfs/fwupgrade
[INFO ] post-install linux/rootfs/peekpoke
[INFO ] package rootfs.cpio to /home/mhn/hw_sw_co_design/software/images/linux
[INFO ] Update and install vmlinux image
[INFO ] vmlinux linux/kernel
[INFO ] install linux/kernel
[INFO ] package zImage
[INFO ] zImage linux/kernel
[INFO ] install linux/kernel
[INFO ] Package HDF bitstream
[INFO ] Failed to copy images to TFTPBOOT /tftpboot
```

~/hw_sw_co_design/software$
petalinux-create -t apps -n device_driver –enable

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-create -t apps -n device_driver --enable
INFO: Create apps: device_driver
INFO: New apps successfully created in /home/mhn/hw_sw_co_design/software/components/apps/device_driver
INFO: Enabling created component...
INFO: It has been enabled to linux/rootfs
```

~/hw_sw_co_design/software$
cd components/apps/device_driver/

```
~/hw_sw_co_design/software/components/apps/device_driver$
vi device_driver.c

/*
 * Placeholder PetaLinux user application.
 *
 * Replace this with your application code
 */
#include <stdio.h>
#include <stdlib.h>
#include <unistd.h>
#include <sys/mman.h>
#include <fcntl.h>


#define IN        0
#define OUT        1

#define GPIO_MAP_SIZE        0x10000

#define GPIO_DATA_OFFSET    0x00
#define GPIO_TRI_OFFSET        0x04
#define GPIO2_DATA_OFFSET    0x00
#define GPIO2_TRI_OFFSET    0x04

void usage(void){

    printf("*argv[0] -d <UIO_DEV_FILE> -i | -o <VALUE>\n");
    printf(" -d UIO device file - ex) /dev/uio0");
    printf(" -i Input from GPIO\n");
    printf(" -o <VALUE> Output to GPIO\n");

}

int main(int argc, char *argv[])
{

    int c, fd, value, direction = IN;
    char *uiod;
    void *ptr;

    printf("GPIO UIO Test\n");

    while( (c = getopt(argc, argv, "d:io:h")) != -1){

        switch(c){
            case 'd':
                uiod = optarg;
                break;
            case 'i':
                direction = IN;
            case 'o':
                direction = OUT;
```

```
                value = atoi(optarg);
                break;
            default :
                printf("Invalid Option: %c\n", (char)c);
                usage();
                return -1;

        }
    }

    fd = open(uiod, O_RDWR);

    if(fd < 1){
        perror(argv[0]);
        printf("Onvalid UIO Device File: %s\n", uiod);
        usage();
        return -1;
    }

    ptr = mmap(NULL, GPIO_MAP_SIZE, PROT_READ|
PROT_WRITE,MAP_SHARED, fd, 0);

    if(direction == IN){
        *((unsigned *)(ptr + GPIO_TRI_OFFSET)) == 255;
        printf("%s:Input: %08x\n", argv[0], value);
    }else{
        *((unsigned *)(ptr + GPIO_TRI_OFFSET)) = 0;
        *((unsigned *)(ptr + GPIO_DATA_OFFSET)) = value;

    }

    munmap(ptr, GPIO_MAP_SIZE);

    return 0;
}
```

/home/mhn/hw_sw_co_design/software/images/linux

여기에 부트 로더와 리눅스 이미지가 있는 것을 볼 수 있을 것이다.

~/hw_sw_co_design/software$ petalinux-config -c rootfs

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config -c rootfs
INFO: Checking component...
INFO: Config linux/rootfs
[INFO ] config linux/rootfs


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

~/hw_sw_co_design/software$ petalinux-config -c kernel

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config -c kernel
INFO: Checking component...
INFO: Config linux/kernel
[INFO ] config linux/kernel


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

~/hw_sw_co_design/software$ cd ../hardware/driver_lab.sdk

~/hw_sw_co_design/hardware/driver_lab.sdk$
petalinux-config --get-hw-description -p ../../software/

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/hardware/driver_lab.sdk$ petalinux-config --get-hw-description -p ../../software/
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename design_1_wrapper.hdf to system.hdf

****** hsi v2015.4 (64-bit)
  **** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
    ** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/mhn/hw_sw_co_design/software/build/linux/hw-description/hw-description.tcl -notrace
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:26:31 2018...
INFO: Config linux
[INFO ] oldconfig linux
[INFO ] generate DTS to /home/mhn/hw_sw_co_design/software/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
WARNING: ps7_ethernet_0: No reset found
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:26:43 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:27:01 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 1 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:27:08 2018...
[INFO ] oldconfig linux/u-boot
```

~/hw_sw_co_design/hardware/driver_lab.sdk$ cd ../../software/

~/hw_sw_co_design/software$ petalinux-config

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config
INFO: Checking component...
INFO: Config linux
[INFO ] config linux


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

[INFO ] generate DTS to /home/mhn/hw_sw_co_design/software/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
WARNING: ps7_ethernet_0: No reset found
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:27:34 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:27:53 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Thu May 31 14:27:59 2018...
[INFO ] oldconfig linux/u-boot
```

~/hw_sw_co_design/software$ petalinux-config -c kernel

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config -c kernel
INFO: Checking component...
INFO: Config linux/kernel
[INFO ] config linux/kernel


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

~/hw_sw_co_design/software$ petalinux-config -c rootfs

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software$ petalinux-config -c rootfs
INFO: Checking component...
INFO: Config linux/rootfs
[INFO ] config linux/rootfs


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

```
~/hw_sw_co_design/software/subsystems/linux/configs/device-tree$
vi system-top.dts

/dts-v1/;
/include/ "system-conf.dtsi"
/ {
};

&clkc {
    ps-clk-frequency = <50000000>;
};

&flash0{
    compatible = "s25fl128s1";
};

&usb0{
    dr_mode = "otg";
};

&gem0{
    phy-handle = <&phy0>;
    mdio{

        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@1{
            compatible = "realtek,RTL8211E";
            device_type = "ethernet-phy";
            reg = <1>;
        };
    };
};

&axi_gpio_0{
    compatible = "generic-uio";
};
```

~/hw_sw_co_design/software/images/linux$ petalinux-build

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software/images/linux$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] Cleaning packages
[INFO ] clean linux/rootfs/device_driver
[INFO ] clean linux/rootfs/fwupgrade
[INFO ] clean linux/rootfs/peekpoke
[INFO ] pre-build linux/rootfs/device_driver
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build system.dtb
[INFO ] build linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] build zynq_fsbl
[INFO ] Setting up stage config
[INFO ] Setting up rootfs config
[INFO ] Updating for cortexa9-vfp-neon
[INFO ] Updating package manager
[INFO ] Expanding stagefs
[INFO ] build linux/rootfs/device_driver
[INFO ] build linux/rootfs/fwupgrade
[INFO ] build linux/rootfs/peekpoke
[INFO ] build kernel in-tree modules
[INFO ] modules linux/kernel
[INFO ] post-build linux/rootfs/device_driver
[INFO ] post-build linux/rootfs/fwupgrade
[INFO ] post-build linux/rootfs/peekpoke
[INFO ] pre-install linux/rootfs/device_driver
[INFO ] pre-install linux/rootfs/fwupgrade
[INFO ] pre-install linux/rootfs/peekpoke
[INFO ] install system.dtb
[INFO ] install linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] install linux/u-boot
[INFO ] Expanding rootfs
[INFO ] install sys_init
[INFO ] install linux/rootfs/device_driver
[INFO ] install linux/rootfs/fwupgrade
[INFO ] install linux/rootfs/peekpoke
[INFO ] install kernel in-tree modules
[INFO ] modules_install linux/kernel
[INFO ] post-install linux/rootfs/device_driver
[INFO ] post-install linux/rootfs/fwupgrade
[INFO ] post-install linux/rootfs/peekpoke
[INFO ] package rootfs.cpio to /home/mhn/hw_sw_co_design/software/images/linux
[INFO ] Update and install vmlinux image
[INFO ] vmlinux linux/kernel
[INFO ] install linux/kernel
[INFO ] package zImage
[INFO ] zImage linux/kernel
[INFO ] install linux/kernel
[INFO ] Package HDF bitstream
[INFO ] Failed to copy images to TFTPBOOT /tftpboot
```

~/hw_sw_co_design/software/images/linux$
petalinux-package --boot --fsbl zynq_fsbl.elf --fpga
../../../hardware/impl_1/design_1_wrapper.bit --uboot –force

```
mhn@mhn-Z20NH-AS51B5U:~/hw_sw_co_design/software/images/linux$ petalinux-package --boot --fsbl zynq_fsbl.elf --fpga ../../../hardware/impl_1/design_1_wrapper.bit --uboot --force
INFO: File in BOOT BIN: "/home/mhn/hw_sw_co_design/software/images/linux/zynq_fsbl.elf"
INFO: File in BOOT BIN: "/home/mhn/hw_sw_co_design/hardware/impl_1/design_1_wrapper.bit"
INFO: File in BOOT BIN: "/home/mhn/hw_sw_co_design/software/images/linux/u-boot.elf"
INFO: Generating zynq binary package BOOT.BIN...
INFO: Binary is ready.
WARNING: Unable to access the TFTPBOOT folder /tftpboot!!!
WARNING: Skip file copy to TFTPBOOT folder!!!
```

if)

```
ERROR: This tool requires 'bootgen' and it is missing. Please source Xilinx Tools settings first
```

export PATH=$PATH:/home/mhn/xilinx/SDK/2017.1/bin/

수업중 제공한 문서를 기반으로 SD 카드에 부트 로더와 리눅스 이미지를 옮긴다.

(sd 카드 파티션 분할을 먼저 하자!)

FPGA 보드의 점퍼를 SD 카드 부팅으로 변경한다.

컴퓨터와 FPGA 보드를 USB 로 연결한다.

전원을 인가한다.

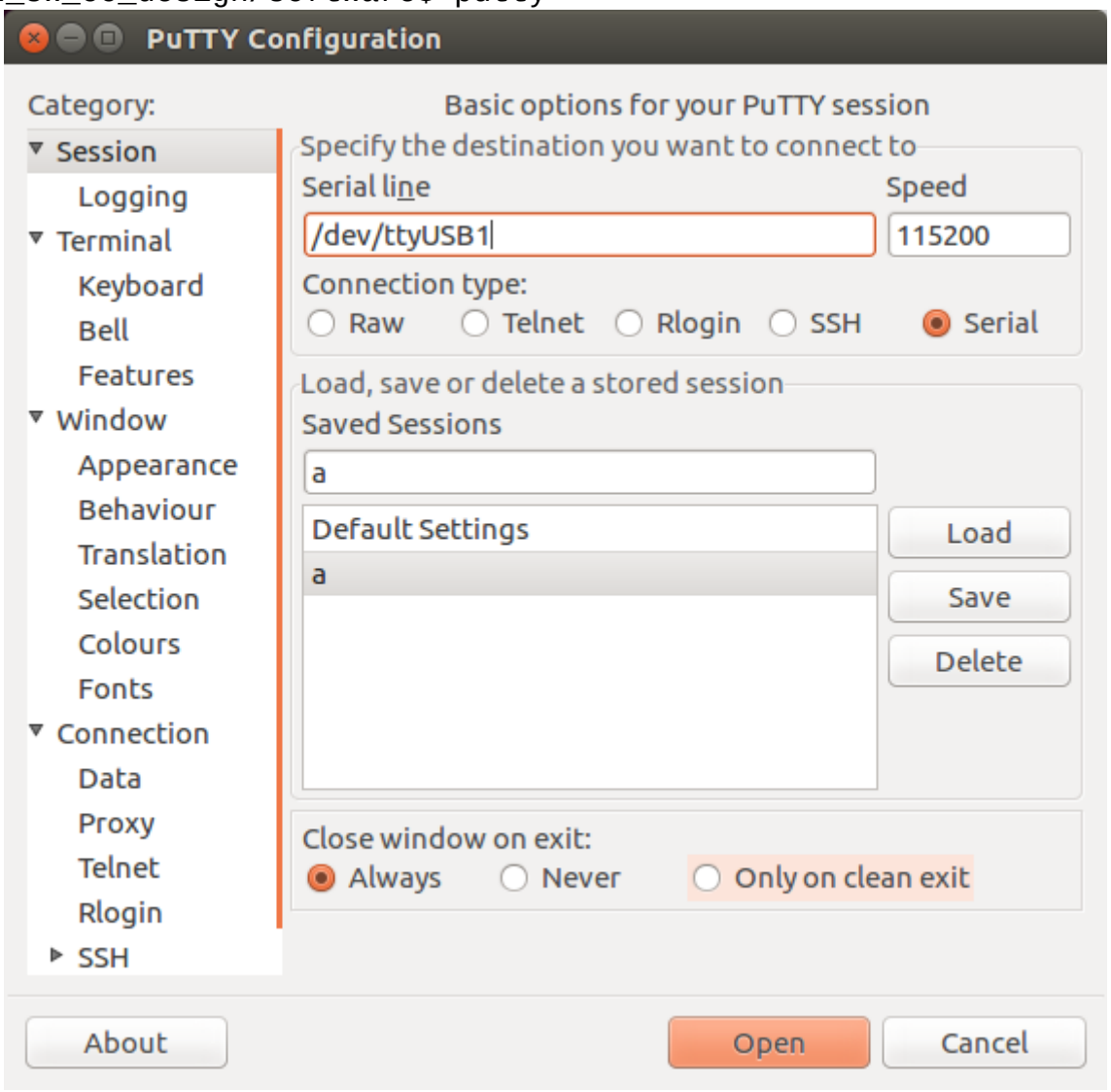
dmesg 를 통해 USB Device Driver 가 잘 잡히는지 확인한다.(노란불!)

sudo apt-get install putty

```
mhn@mhn-Z20NH-AS51B5U:~/petalinux_zynq/petalinux-v2015.4-final/components/apps$ sudo apt-get install putty
Reading package lists... Done
Building dependency tree
Reading state information... Done
The following packages were automatically installed and are no longer required:
  cabextract fonts-horai-umefont libasyncns0:i386 libexif12:i386 libgpm2:i386
  libice6:i386 libieee1284-3:i386 libjpeg-turbo8:i386 libjson-c2:i386
  liblcms2-2:i386 libmspack0 libogg0:i386 libp11-kit-gnome-keyring:i386
  libsamplerate0:i386 libsm6:i386 libwrap0:i386 libx11-6:i386 libxau6:i386
  libxcb1:i386 libxcomposite1:i386 libxdamage1:i386 libxdmcp6:i386
  libxext6:i386 libxfixes3:i386 libxinerama1:i386 libxshmfence1:i386
  libxxf86vm1:i386 linux-headers-4.10.0-28 linux-headers-4.10.0-28-generic
  linux-headers-4.13.0-32 linux-headers-4.13.0-32-generic
  linux-headers-4.13.0-36 linux-headers-4.13.0-36-generic
  linux-headers-4.13.0-37 linux-headers-4.13.0-37-generic
  linux-headers-4.13.0-38 linux-headers-4.13.0-38-generic
  linux-headers-4.13.0-39 linux-headers-4.13.0-39-generic
  linux-image-4.10.0-28-generic linux-image-4.13.0-32-generic
  linux-image-4.13.0-36-generic linux-image-4.13.0-37-generic
  linux-image-4.13.0-38-generic linux-image-4.13.0-39-generic
  linux-image-extra-4.10.0-28-generic linux-image-extra-4.13.0-32-generic
  linux-image-extra-4.13.0-36-generic linux-image-extra-4.13.0-37-generic
  linux-image-extra-4.13.0-38-generic linux-image-extra-4.13.0-39-generic
  ttf-mscorefonts-installer
Use 'sudo apt autoremove' to remove them.
The following additional packages will be installed:
  putty-tools
Suggested packages:
  putty-doc
The following NEW packages will be installed:
  putty putty-tools
0 upgraded, 2 newly installed, 0 to remove and 24 not upgraded.
Need to get 662 kB of archives.
After this operation, 2,713 kB of additional disk space will be used.
Do you want to continue? [Y/n] y
Get:1 http://kr.archive.ubuntu.com/ubuntu xenial/universe amd64 putty-tools amd64 0.67-2 [342 kB]
Get:2 http://kr.archive.ubuntu.com/ubuntu xenial/universe amd64 putty amd64 0.67-2 [321 kB]
Fetched 662 kB in 0s (1,889 kB/s)
Selecting previously unselected package putty-tools.
(Reading database ... 431388 files and directories currently installed.)
Preparing to unpack .../putty-tools_0.67-2_amd64.deb ...
Unpacking putty-tools (0.67-2) ...
Selecting previously unselected package putty.
Preparing to unpack .../putty_0.67-2_amd64.deb ...
Unpacking putty (0.67-2) ...
Processing triggers for man-db (2.7.5-1) ...
Processing triggers for bamfdaemon (0.5.3~bzr0+16.04.20180209-0ubuntu1) ...
Rebuilding /usr/share/applications/bamf-2.index...
Processing triggers for gnome-menus (3.13.3-6ubuntu3.1) ...
Processing triggers for desktop-file-utils (0.22-1ubuntu5.1) ...
Processing triggers for mime-support (3.59ubuntu1) ...
Setting up putty-tools (0.67-2) ...
Setting up putty (0.67-2) ...
```

~/hw_sw_co_design/software$ sudo chmod 666 /dev/ttyUSB1

```
~/hw_sw_co_design/software$ putty
```

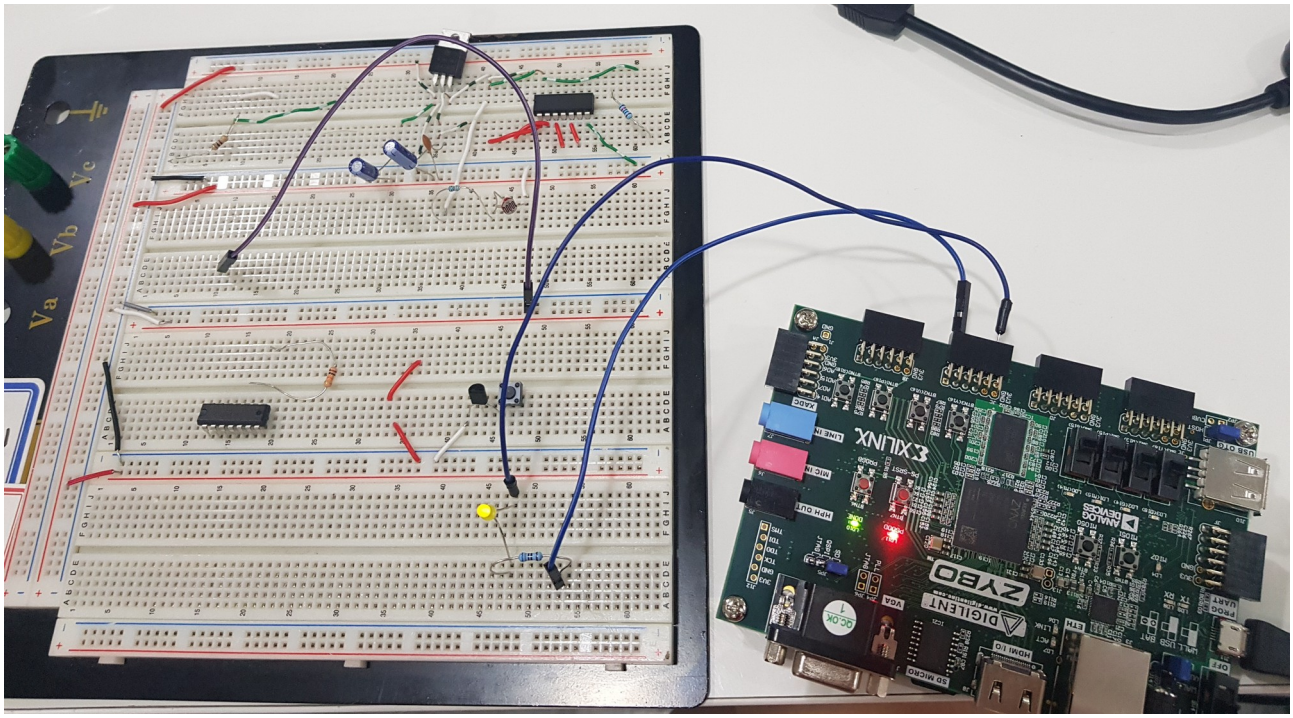


```
Sending discover...
Sending discover...
No lease, forking to background
done.

Built with PetaLinux v2015.4 (Yocto 1.8) software /dev/ttyPS0
software login: root
Password:
login[876]: root login on 'ttyPS0'
root@software:~#
root@software:~#
root@software:~# cd /dev
root@software:/dev# ;s
-sh: syntax error: unexpected ";"
root@software:/dev# ls
console             ram10               tty21               tty50
cpu_dma_latency     ram11               tty22               tty51
flash               ram12               tty23               tty52
full                ram13               tty24               tty53
iio:device0         ram14               tty25               tty54
initctl             ram15               tty26               tty55
input               ram2                tty27               tty56
kmsg                ram3                tty28               tty57
loop-control        ram4                tty29               tty58
loop0               ram5                tty3                tty59
loop1               ram6                tty30               tty6
loop2               ram7                tty31               tty60
loop3               ram8                tty32               tty61
loop4               ram9                tty33               tty62
loop5               random              tty34               tty63
loop6               shm                 tty35               tty7
loop7               snd                 tty36               tty8
mem                 tty                 tty37               tty9
memory_bandwidth    tty0                tty38               ttyPS0
mmcblk0             tty1                tty39               uio0
mmcblk0p1           tty10               tty4                urandom
mmcblk0p2           tty11               tty40               vcs
mtab                tty12               tty41               vcs1
network_latency     tty13               tty42               vcsa
network_throughput  tty14               tty43               vcsa1
null                tty15               tty44               vga_arbiter
port                tty16               tty45               watchdog
psaux               tty17               tty46               watchdog0
ptmx                tty18               tty47               xdevcfg
pts                 tty19               tty48               zero
ram0                tty2                tty49
ram1                tty20               tty5
root@software:/dev# cd ../
```

uio0 이 잘 올라가 있는지 확인하자

```
root@software:/dev# cd ../
root@software:/# ls
bin    dev    home   lib    mnt    run    sys    usr
boot   etc    init   media  proc   sbin   tmp    var
root@software:/# cd bin
root@software:/bin# ls
ash                 getopt              poke
busybox             grep                ps
busybox.nosuid      gunzip              pwd
busybox.suid        gzip                rm
cat                 hostname            rmdir
chattr              kill                run-parts
chgrp               ln                  sed
chmod               login               sh
chown               ls                  sleep
cp                  mkdir               stat
cpio                mknod               stty
date                mktemp              su
dd                  more                sync
device_driver       mount               tar
df                  mountpoint          touch
dmesg               mountpoint.sysvinit true
dnsdomainname       mv                  umount
dumpkmap            netstat             uname
echo                nice                upgrade-firmware
egrep               peek                usleep
false               pidof               vi
fatattr             pidof.sysvinit      watch
fgrep               ping                zcat
fwupgrade           ping6
root@software:/bin# cd ../
root@software:/# device_driver
.stage.apt/       etc/              mnt/              tmp/
.targetroot.apt/  home/             proc/             usr/
bin/              init              run/              var/
boot/             lib/              sbin/
dev/              media/            sys/
root@software:/# device_driver /dev/uio0 -o -0
GPIO UIO Test
device_driver: Bad address
Onvalid UIO Device File: (null)
*argv[0] -d <UIO_DEV_FILE> -i | -o <VALUE>
 -d UIO device file - ex) /dev/uio0 -i Input from GPIO
 -o <VALUE> Output to GPIO
root@software:/# device_driver -d /dev/uio0 -o -0
GPIO UIO Test
root@software:/# device_driver -d /dev/uio0 -o -1
GPIO UIO Test
```

bin에 device_driver가 잘 올라가 있는지 확인한 후
led 불을 껐다 켰다 해보자!


Va
Vb
Vc
XILINX
DIGILENT
ZYBO