

# TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

강사 – Innova Lee(이상훈)  
[gcccompil3r@gmail.com](mailto:gcccompil3r@gmail.com)

학생 – GJ (박현우)  
[uc820@naver.com](mailto:uc820@naver.com)

# 목차


## 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법

- 1) css 설치 (윈도우)
- 2) HalCoGen 설치 (윈도우)
- 3) css와 HalCoGen 연동

## 2. External LED GIO 기반 제어 예제

# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - CSS

http://processors.wiki.ti.com/index.php/Download\_CCS



Page

Discussion

Download CCS

Contents [hide]

1 Cloud Tools

2 Download the latest CCS

2.1 Free license for older versions

2.2 Deprecation notices:

3 CCS Incremental Update Policy

4 Code Composer Studio Version 8 Downloads

5 Code Composer Studio Version 7 Downloads

6 Code Composer Studio Version 6 Downloads

7 Code Composer Studio Version 5 Downloads

8 Code Composer Studio Version 4 Downloads

8.1 Image Descriptions

8.2 CCSv4 Release Archive

9 Code Composer Studio Version 3 Downloads

10 Code Composer Studio Version 2 Downloads

Cloud Tools

If you are using a LaunchPad or a SensorTag you can begin v documentation and libraries, CCS Cloud is a cloud-based IDE

Main Page

All pages

All categories

Recent changes

Random page

Help

Print/export

Create a book

Download as PDF

Printable version

Toolbox

What links here

Related changes

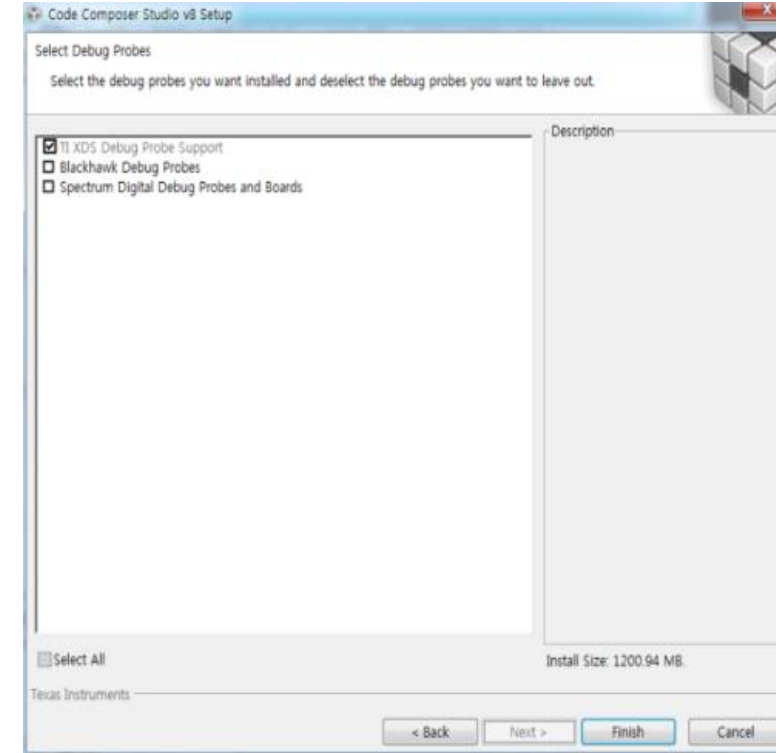
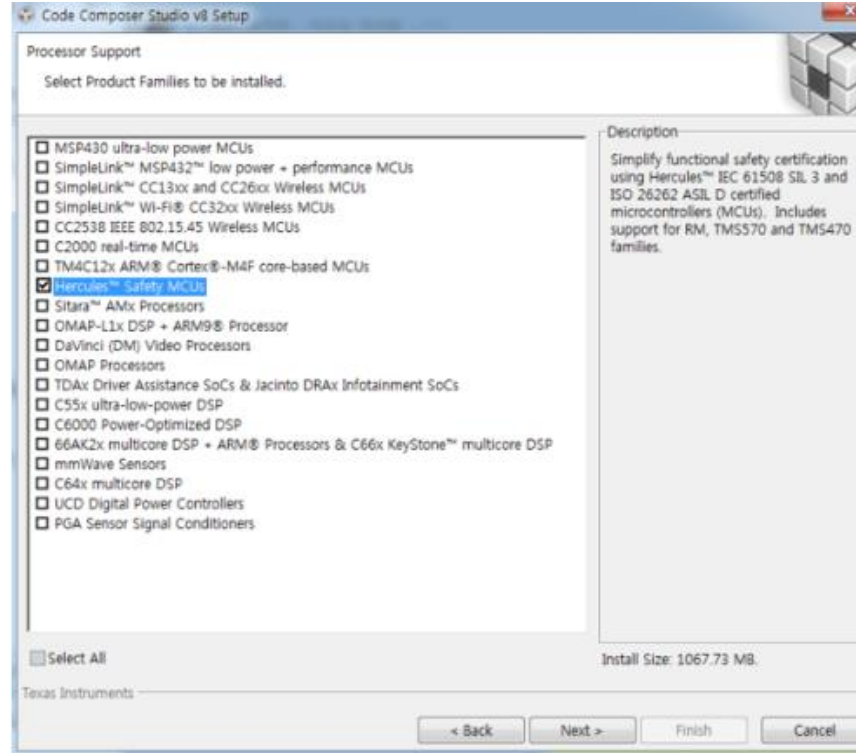
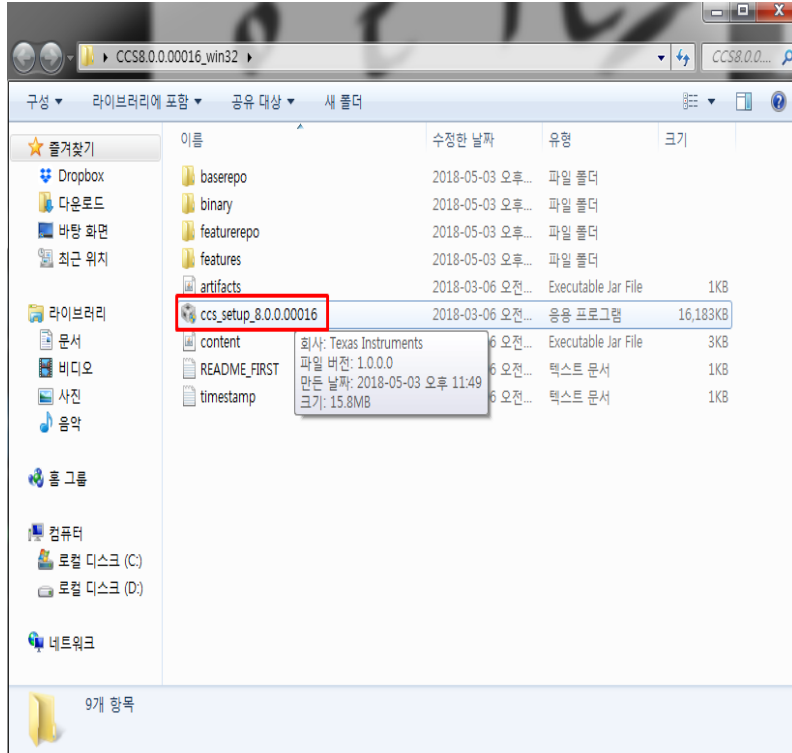
Special pages

Permanent link

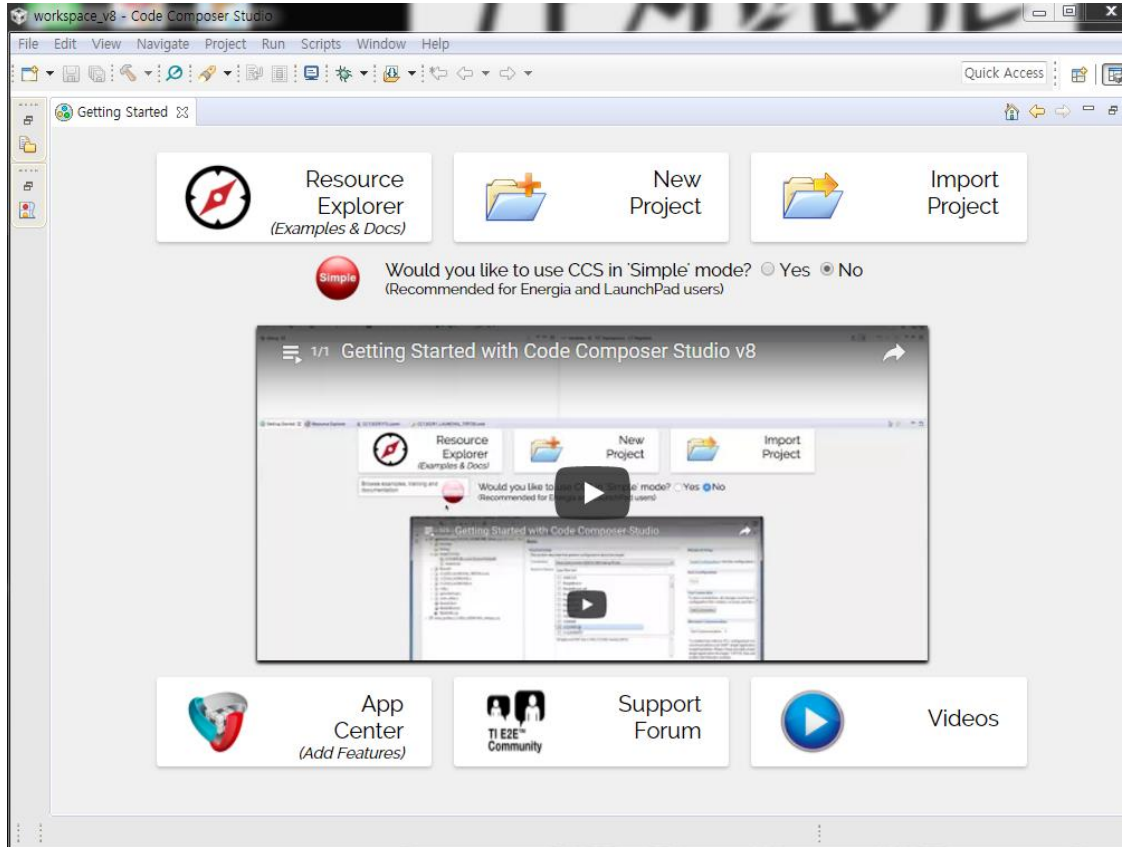
Page information

Code Composer Studio Version 8 Downloads				
There are two types of installers:				
<ul style="list-style-type: none"><li>• <a href="#">Web installers</a> allow you to download only the software components that you require.</li><li>• <a href="#">Off-line installers</a> will download a large compressed file (about 800MB) so you may then uncompress it then select what you require to install.</li></ul>				
Release	Build #	Date	Download	Notes
8.0.0	8.0.0.00016	Mar 09, 2018	<div>Web Installers: <a href="#">Windows</a> <a href="#">Linux</a> <a href="#">MacOS</a>  Off-line Installers: <a href="#">Windows</a> <a href="#">MD5</a> <a href="#">Linux</a> <a href="#">MD5</a> - 64-bit only <a href="#">MacOS</a> <a href="#">MD5</a>  <a href="#">Manifest</a></div>	<ul style="list-style-type: none"><li>• <b>New/Notable In This Release (8.0.0.00016):</b></li><li>• <a href="#">Release notes</a></li><li>• Update to Eclipse 4.7 and CDT 9.3</li></ul> <div>Debugger<ul style="list-style-type: none"><li>• Bug and stability fixes</li><li>• EMU18_M02 7.0.188.0</li></ul>IDE<ul style="list-style-type: none"><li>• Bug and stability fixes</li></ul>REX<ul style="list-style-type: none"><li>• Robustness improvements</li></ul>Quarterly Device support updatesCompilers<ul style="list-style-type: none"><li>• MSP GCC v6.4.0.32</li><li>• ARM GCC v7.2.1</li><li>• C6000 v8.2.x</li><li>• MCU Compilers v18.1.1 LTS</li></ul></div>

# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - CSS



# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - CSS

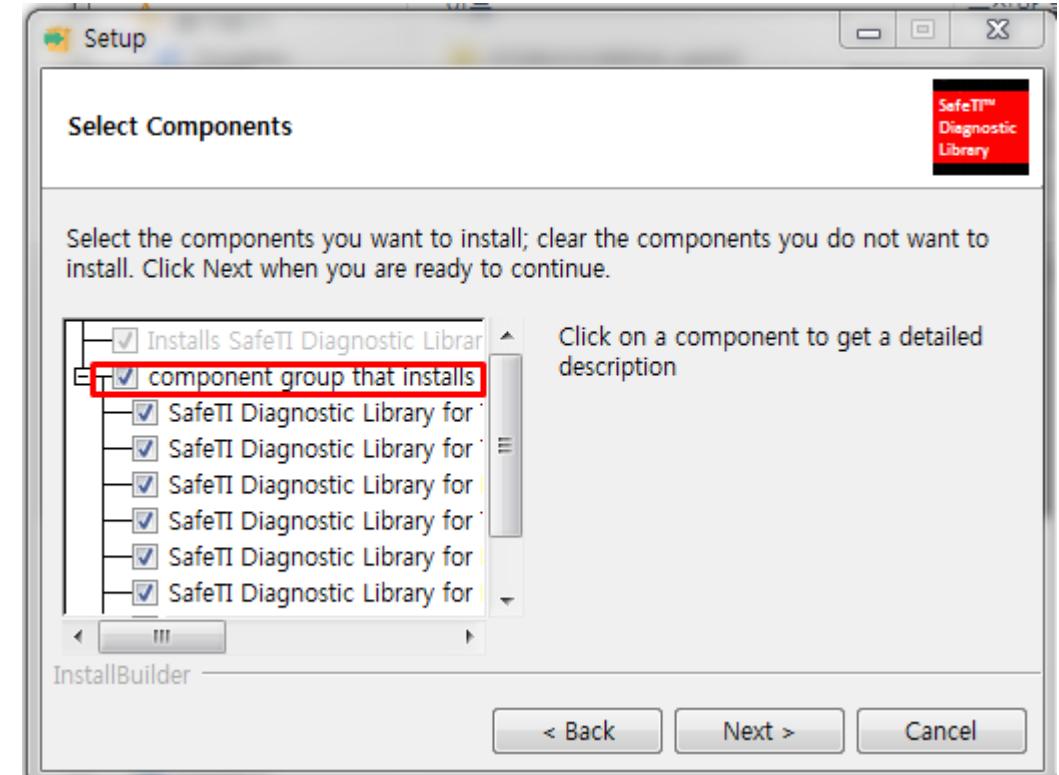
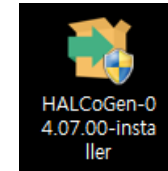


# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - HalCoGen

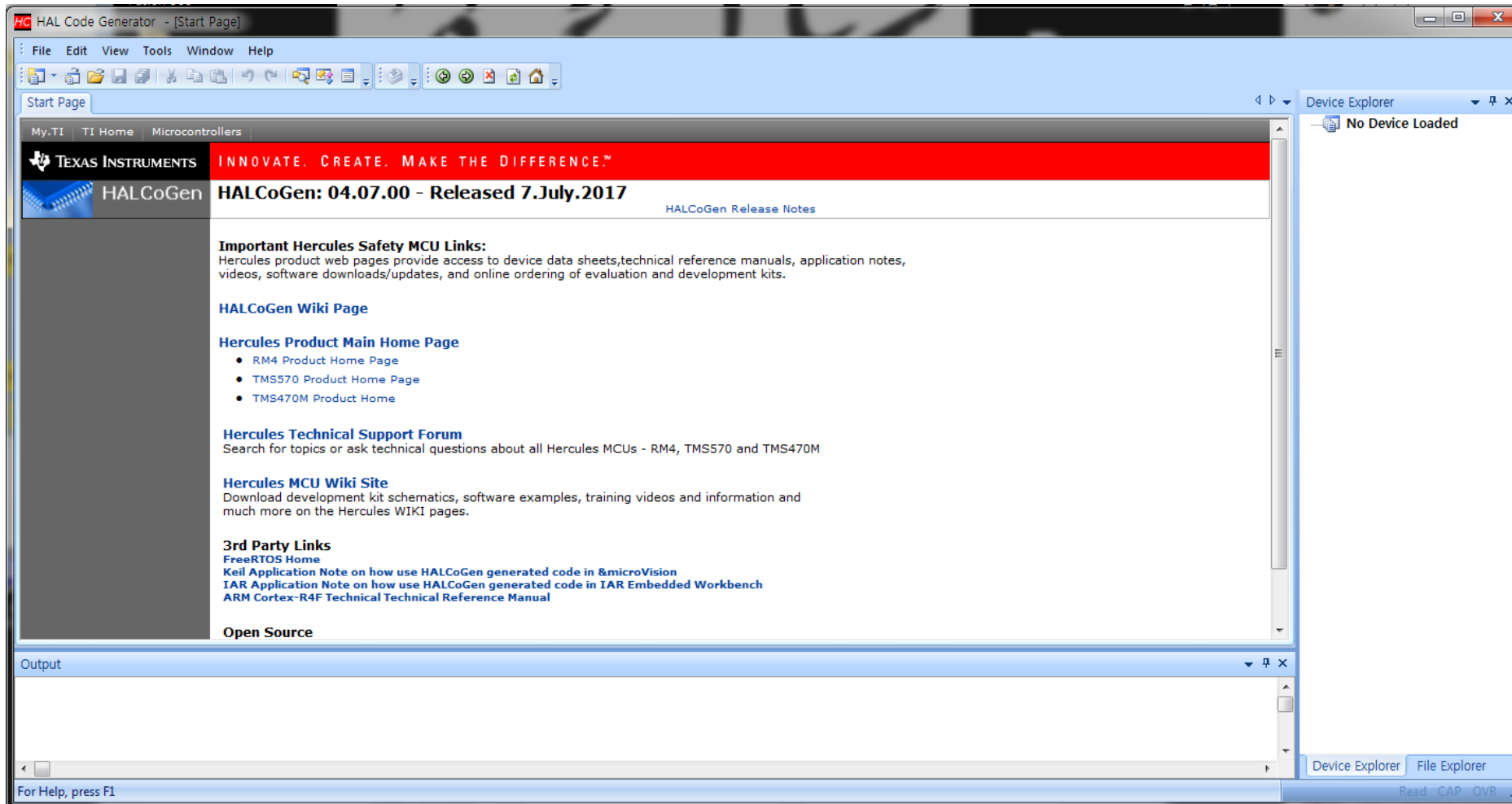
<http://www.ti.com/tool/halcodegen>

Order Now

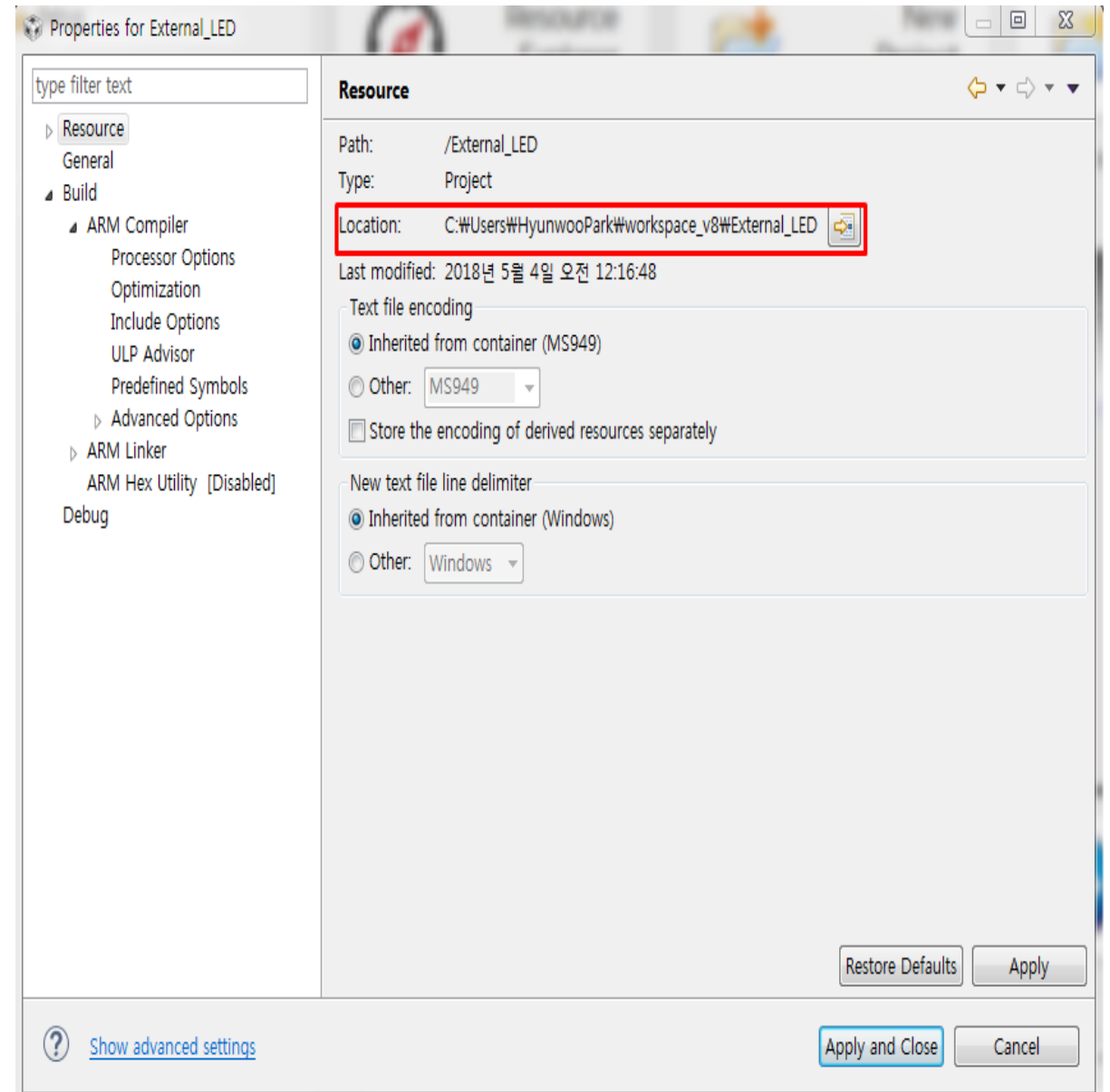
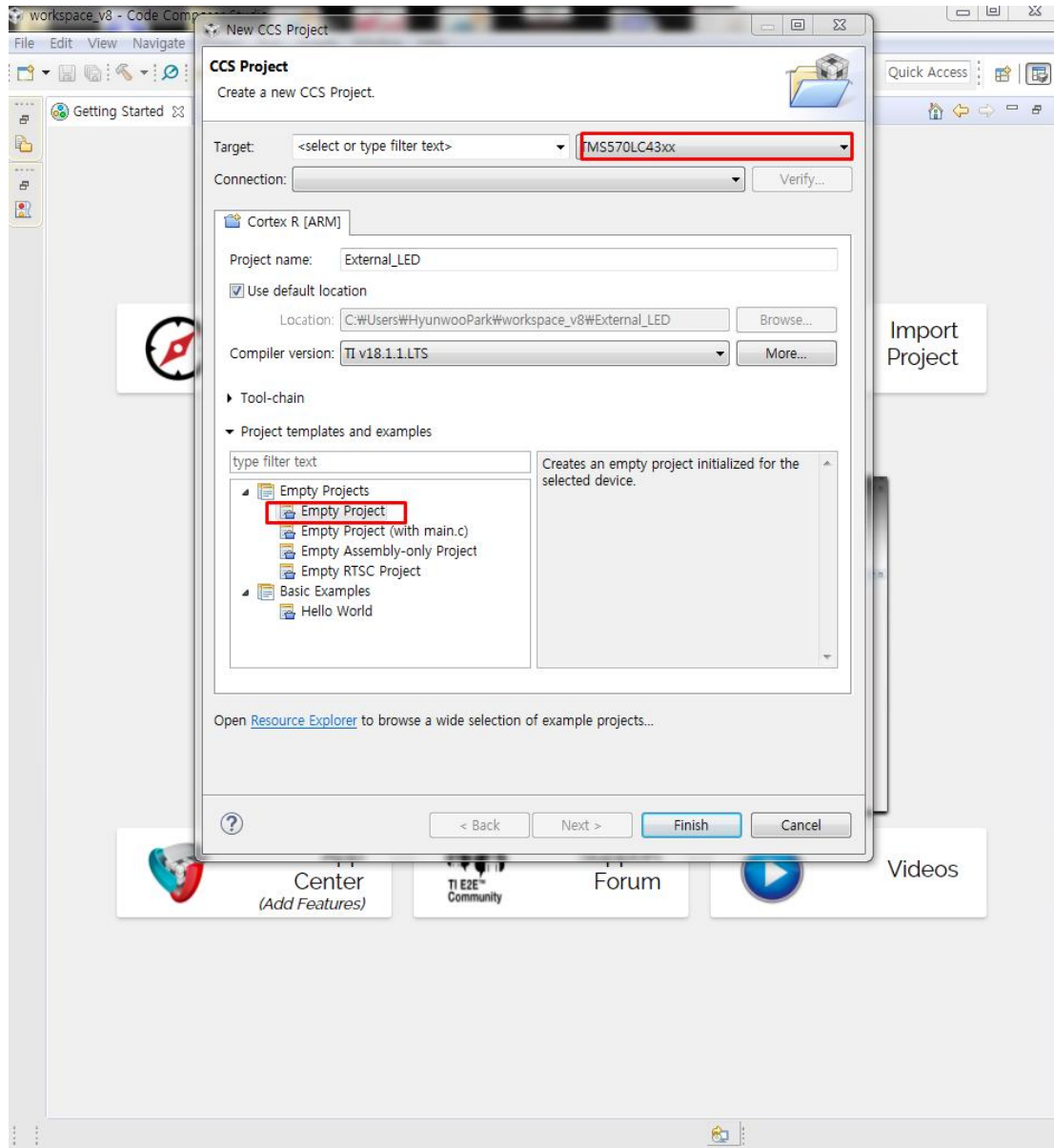
Part Number	Buy from Texas Instruments or Third Party	Alert Me	Status	Current Version	Version Date	Host	OS
HALCOGEN: HAL Code Generator tool	<b>Download</b>	<b>Alert Me</b>	ACTIVE	04.07.00	07-Jul-2017	PC	Vista, Windows 7, XP,
SAFETI-HALCOGEN-CSP: SafeTI HALCoGen Compliance Support Package	<b>Request</b>	<b>Alert Me</b>	ACTIVE	01.00.00	30-Jan-2015		



# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - HalCoGen

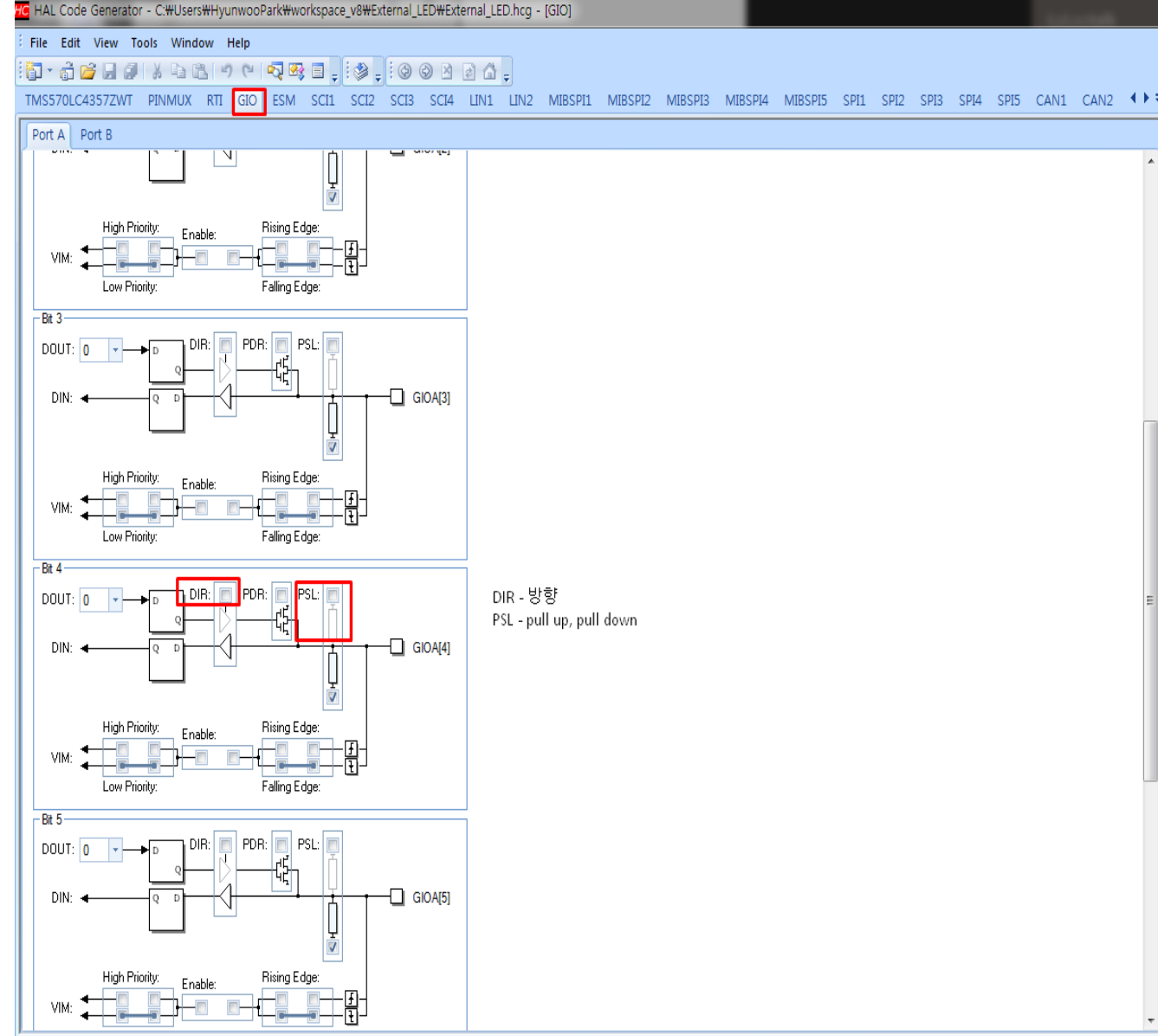
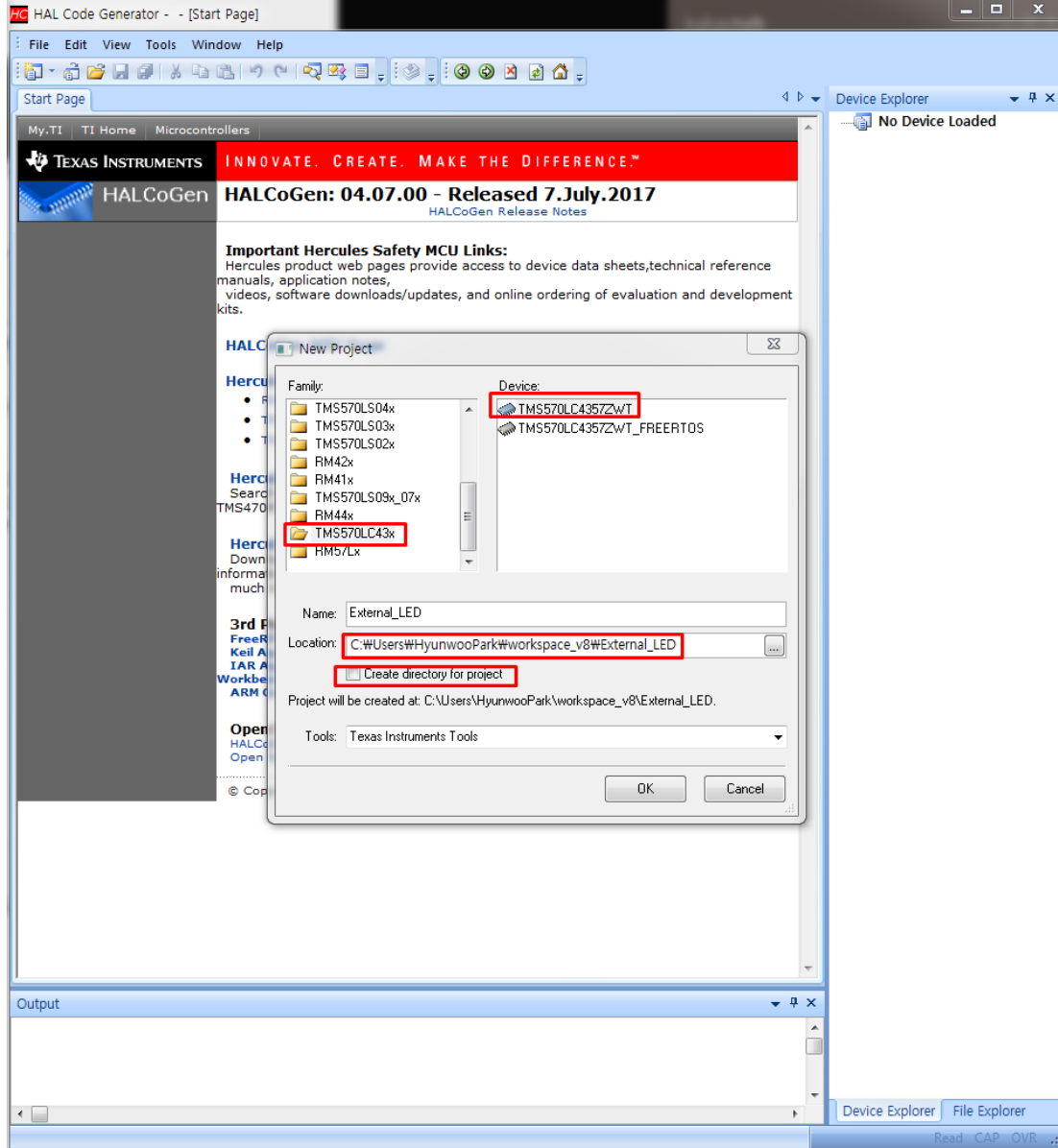


# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - 연동

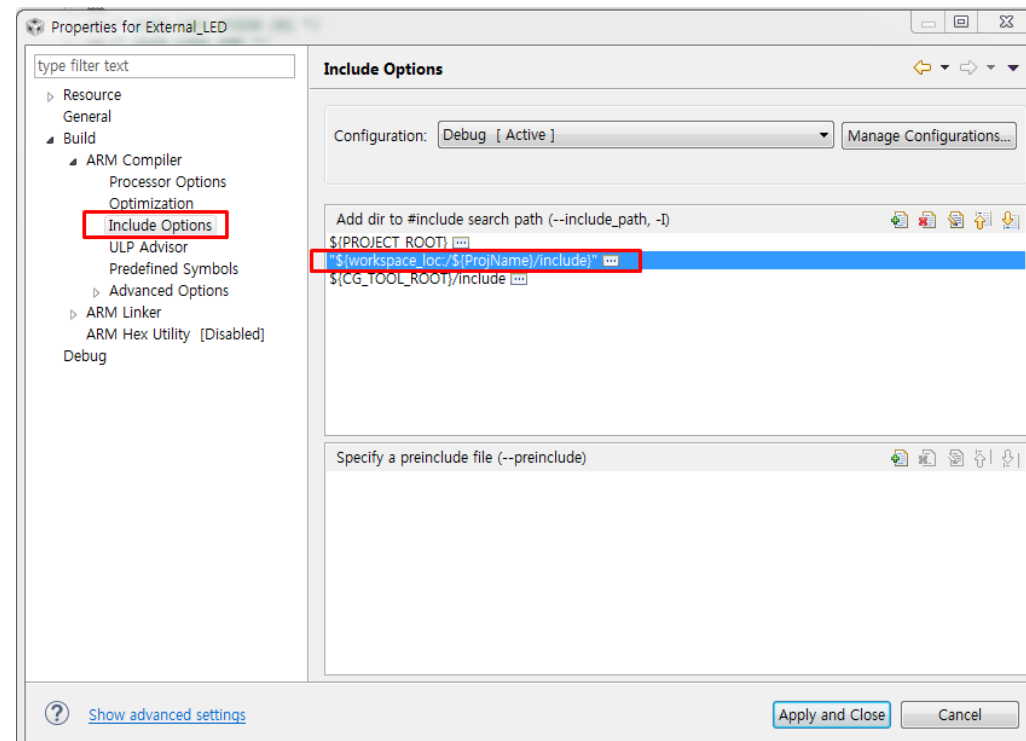
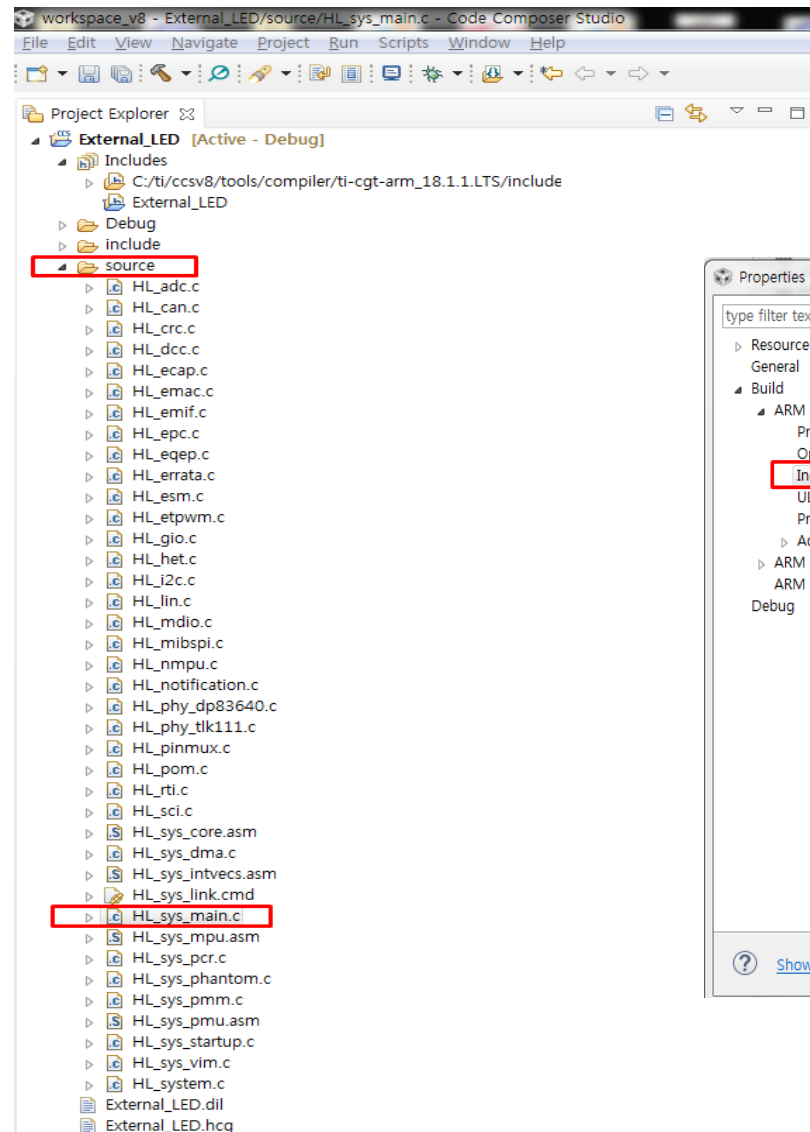
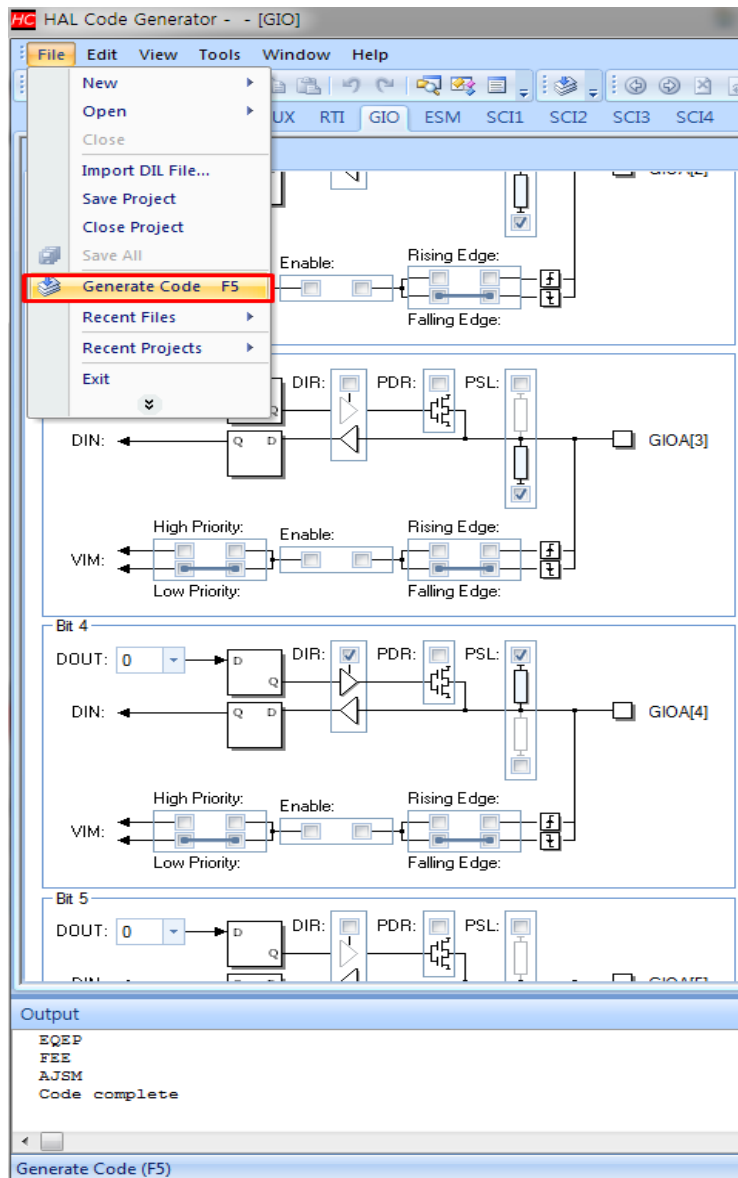




# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - 연동



# 1. Cortex-R5F Hercules Safety MCU를 위한 툴 다운로드 방법 - 연동



## 2. External LED GPIO 기반 제어 예제

Getting Started \*HL\_sys\_main.c HL\_gpio.c

```
46 /* USER CODE END */
47
48 /* Include Files */
49
50 #include "HL_sys_common.h"
51 #include "HL_gpio.h"
52
53 /* USER CODE BEGIN (1) */
54 /* USER CODE END */
55
56 /** @fn void main(void)
57 * @brief Application main function
58 * @note This function is empty by default.
59 *
60 * This function is called after startup.
61 * The user can use this function to implement the application.
62 */
63
64 /* USER CODE BEGIN (2) */
65 /* USER CODE END */
66
67 uint8_t emacAddress[6U] = {0xFFU, 0xFFU, 0xFFU, 0xFFU, 0xFFU, 0xFFU};
68 uint32_t emacPhyAddress = 1U;
69
70 int main(void)
71 {
72 /* USER CODE BEGIN (3) */
73     gpioInit();
74     gpioSetPort(gioPORTA, 0xFFU);
75     gpioSetDirection(gioPORTA, 0xFFU);
76     gpioSetBit(gioPORTA, 4, 1);
77 /* USER CODE END */
78
79     return 0;
80 }
```

F3 – 함수 in

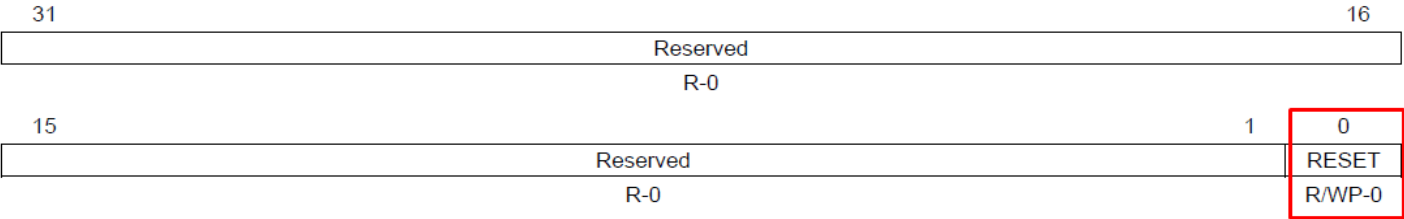
Alt + <- 방향키 – 함수 out

```
/** bring GPIO module out of reset */
gioREG->GCR0 = 1U;
gioREG->ENACLR = 0xFFU;
gioREG->LVLCLR = 0xFFU;
```

### 25.5.1 GIO Global Control Register (GIOGCR0)

The GIOGCR0 register contains one bit that controls the module reset status. Writing a 0 to this bit puts the module in a reset state. After system reset, this bit must be set to 1 before configuring any other register of the GIO module. Figure 25-5 and Table 25-2 describe this register.

Figure 25-5. GIO Global Control Register (GIOGCR0) [offset = 00h]



LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -n = value after reset

Table 25-2. GIO Global Control Register (GIOGCR0) Field Descriptions

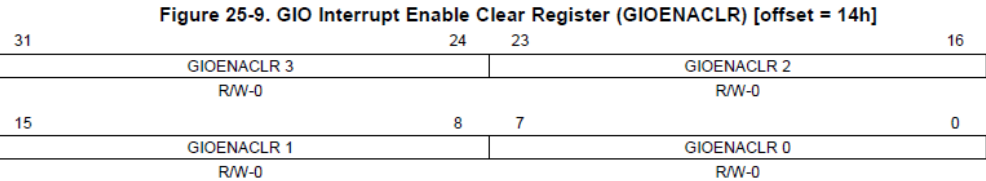
Bit	Field	Value	Description
31-1	Reserved	0	Reads return 0. Writes have no effect.
0	RESET	0	GIO reset. The GIO is in reset state.
		1	The GIO is operating normally.

## 2. External LED GIO 기반 제어 예제

```
/** bring GIO module out of reset */
gioREG->GCR0 = 1U;
gioREG->ENACLR = 0xFFU;
gioREG->LVLCLR = 0xFFU;
```

### 25.5.4.2 GIOENACLR Register

This register disables the interrupt. Figure 25-9 and Table 25-6 describe this register.

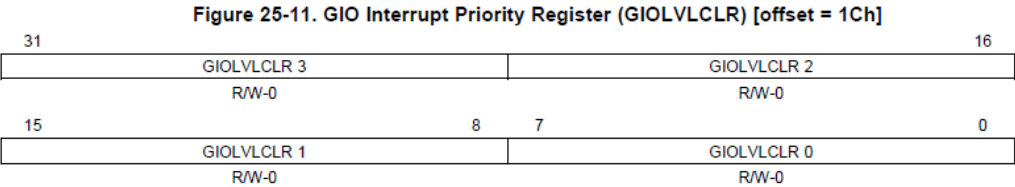


LEGEND: R/W = Read/Write; -n = value after reset

Table 25-6. GIO Interrupt Enable Clear Register (GIOENACLR) Field Descriptions			
Bit	Field	Value	Description
31-24	GIOENACLR 3	0	Interrupt disable for pins GIOD[7:0] Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
23-16	GIOENACLR 2	0	Interrupt disable for pins GIOC[7:0] Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
15-8	GIOENACLR 1	0	Interrupt disable for pins GIOB[7:0] Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.
7-0	GIOENACLR 0	0	Interrupt disable for pins GIOA[7:0] Read: The interrupt is disabled. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is enabled. Write: Disables the interrupt.

### 25.5.5.2 GIOLVLCLR Register

The GIOLVLCLR register is used to configure an interrupt as a low-level interrupt going to the VIM. An interrupt can be configured as a low-level interrupt by writing a 1 into the corresponding bit of the GIOLVLCLR register. Writing a 0 has no effect. Figure 25-11 and Table 25-8 describe this register.



LEGEND: R/W = Read/Write; -n = value after reset

Table 25-8. GIO Interrupt Priority Register (GIOLVLCLR) Field Descriptions			
Bit	Field	Value	Description
31-24	GIOLVLCLR 3	0	GIO low-priority interrupt for pins GIOD[7:0] Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOFF2 and GIOEMU2.
23-16	GIOLVLCLR 2	0	GIO low-priority interrupt for pins GIOC[7:0] Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOFF2 and GIOEMU2.
15-8	GIOLVLCLR 1	0	GIO low-priority interrupt for pins GIOB[7:0] Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOFF2 and GIOEMU2.
7-0	GIOLVLCLR 0	0	GIO low-priority interrupt for pins GIOA[7:0] Read: The interrupt is a low-level interrupt. Write: Writing a 0 to this bit has no effect.
		1	Read: The interrupt is set as a high-level interrupt. The high-level interrupts are recorded to GIOFF1 and GIOEMU1. Write: Sets the interrupt as a low-level interrupt. The low-level interrupts are recorded to GIOFF2 and GIOEMU2.