

TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

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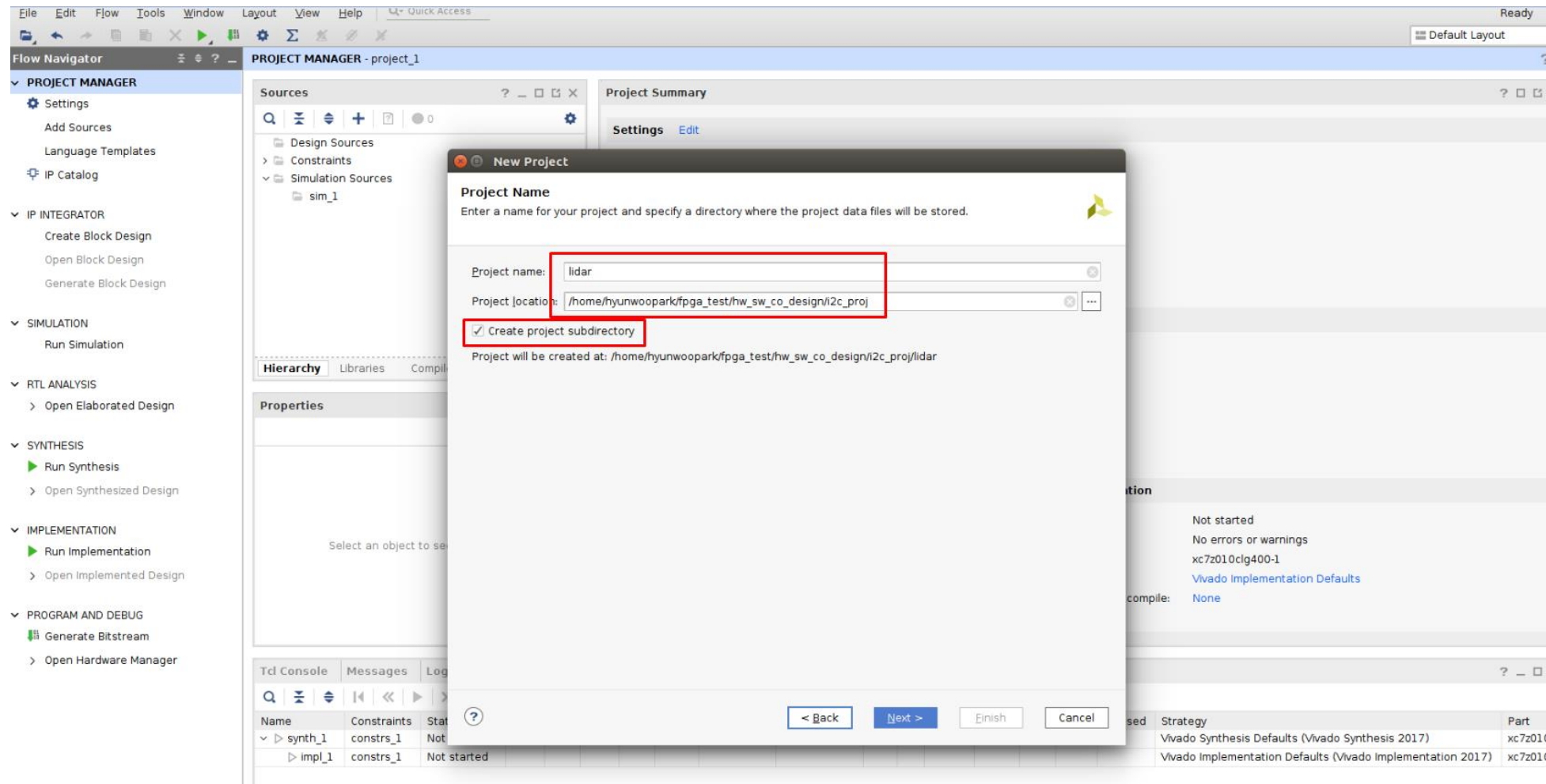
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목차

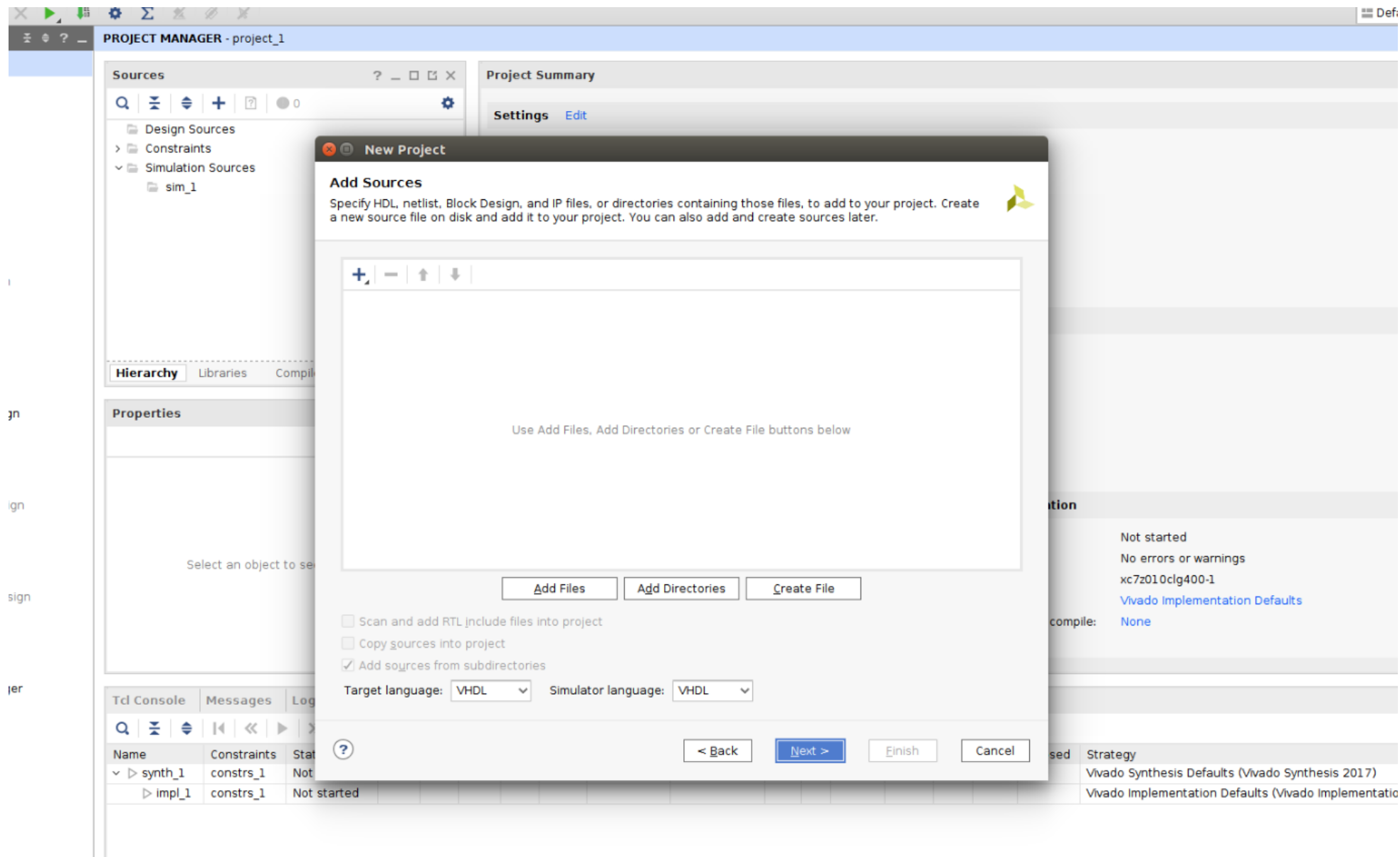
Zynq FPGA on Petalinux for PWM

- 1) Vivado I2C 설계
- 2) LIDAR 센서 제어 C Code
- 3) LIDAR 제어 결과물

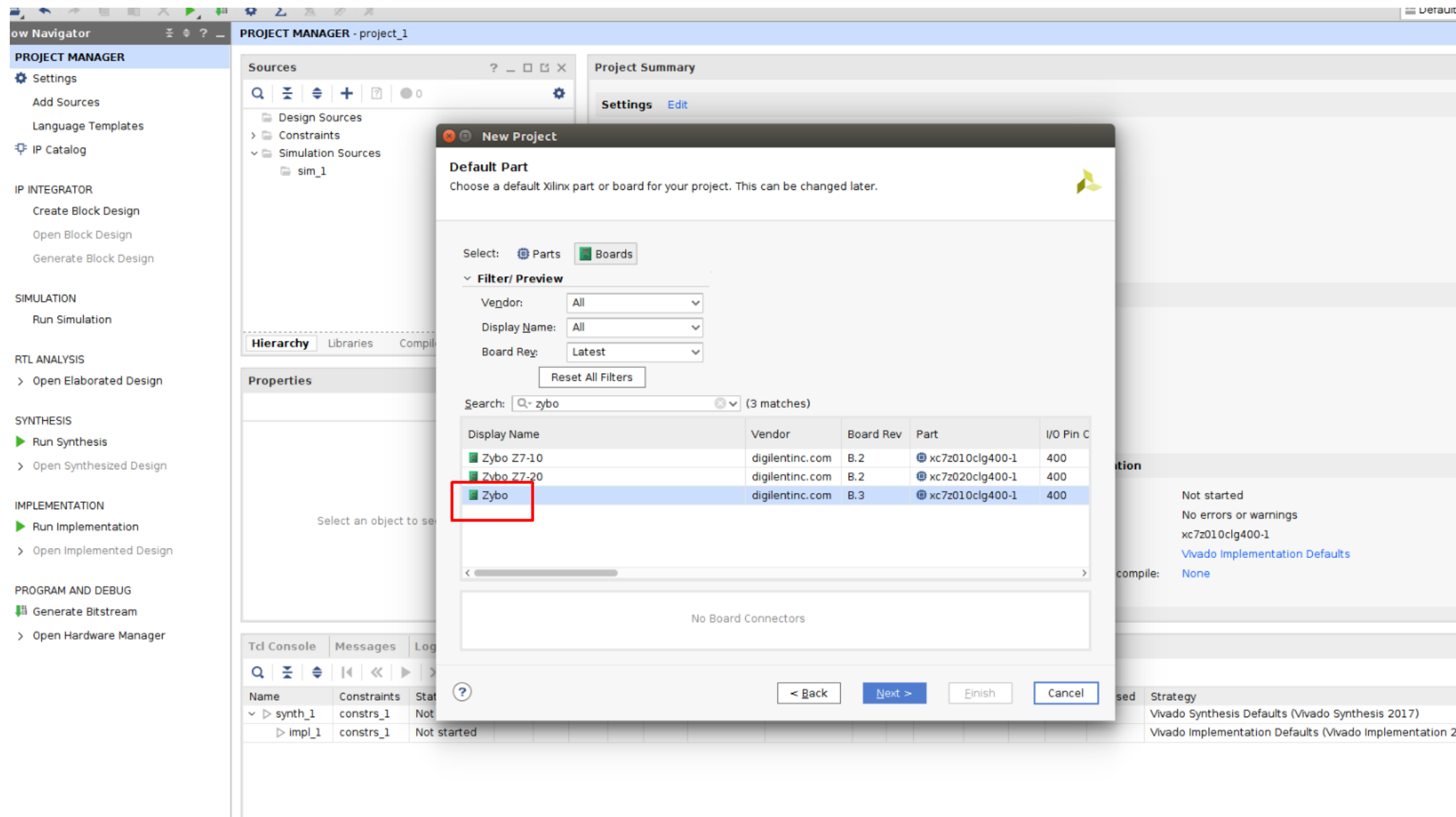
1) Vivado I2C 설계 1



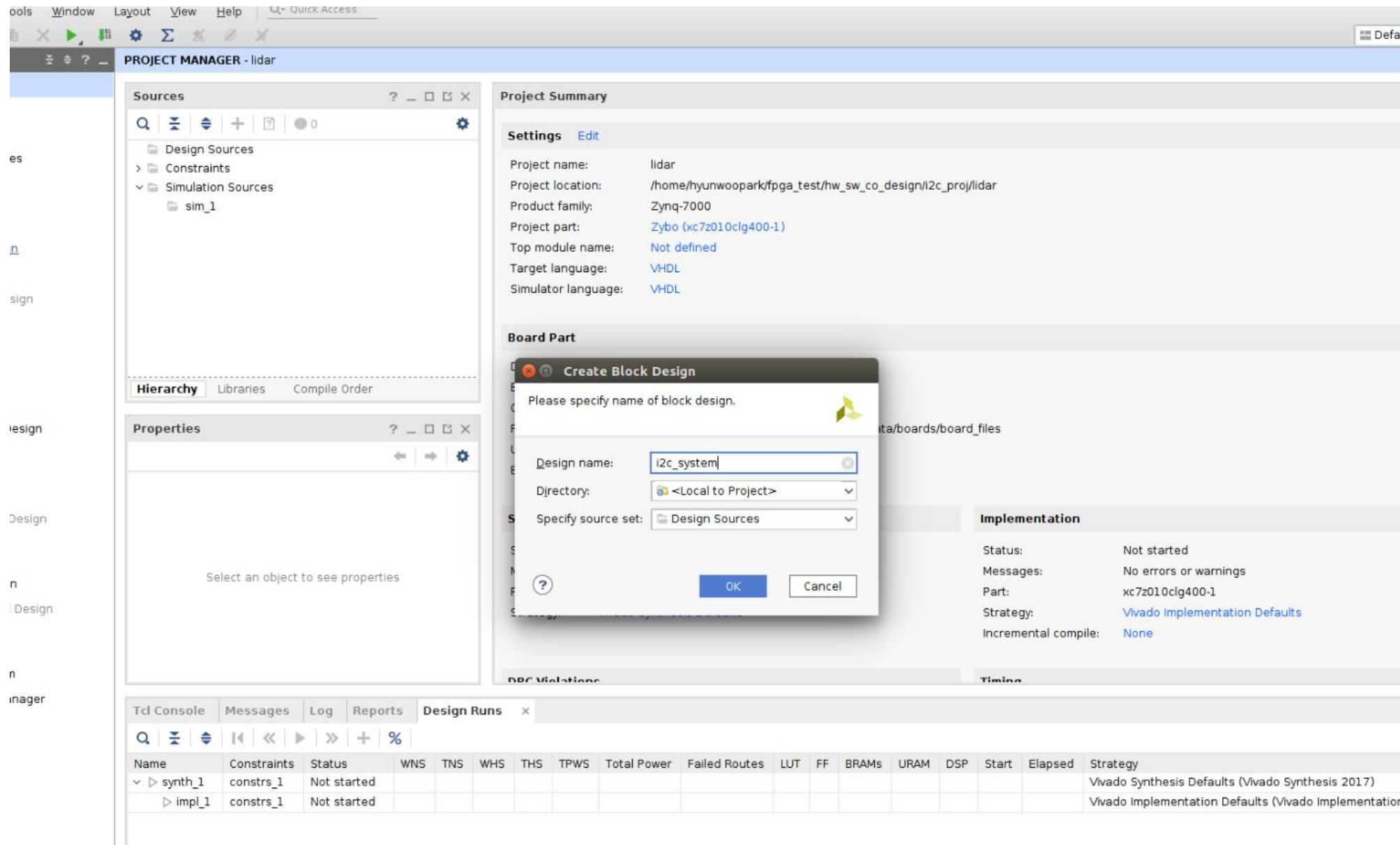
1) Vivado I2C 설계 2



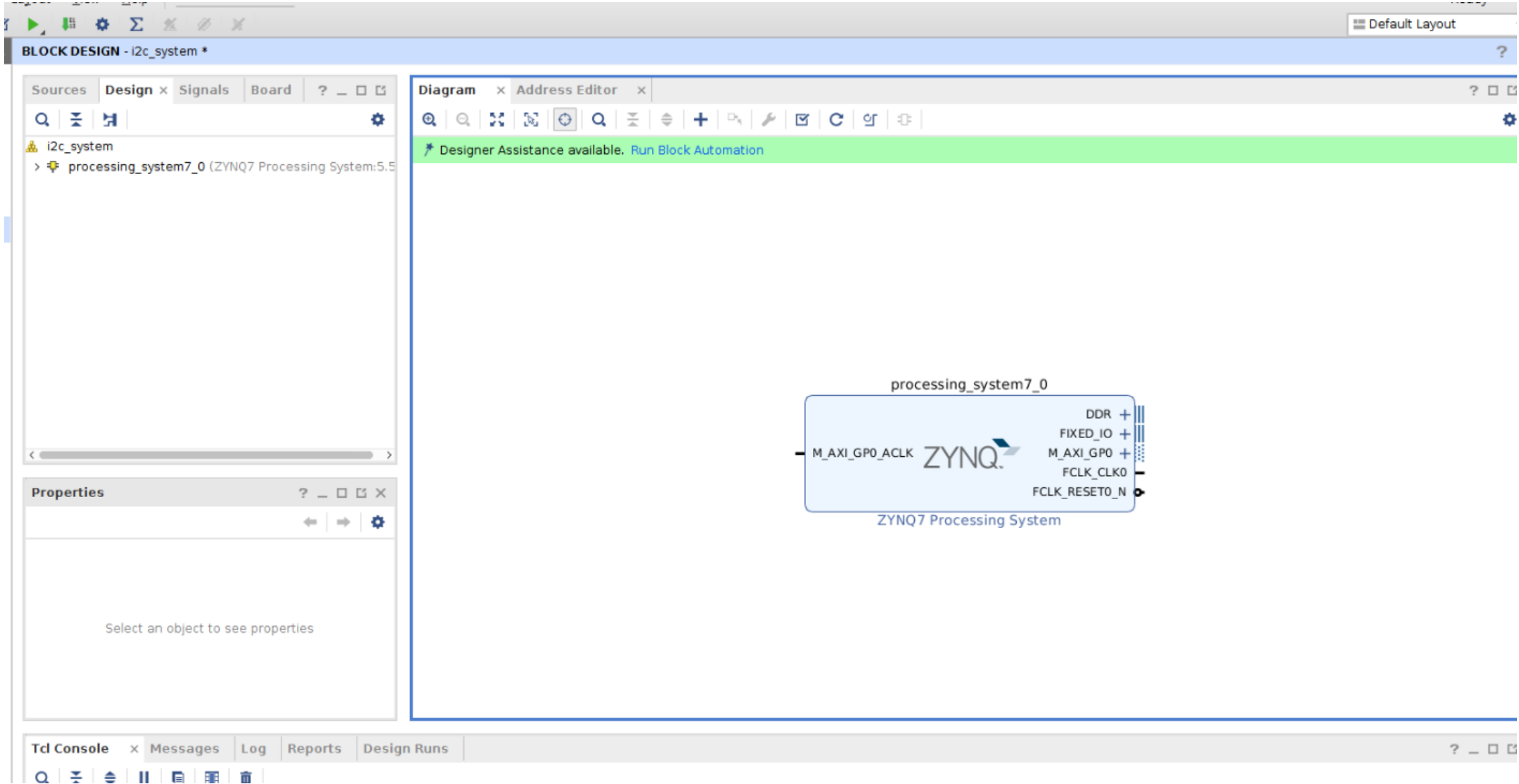
1) Vivado I2C 설계 3



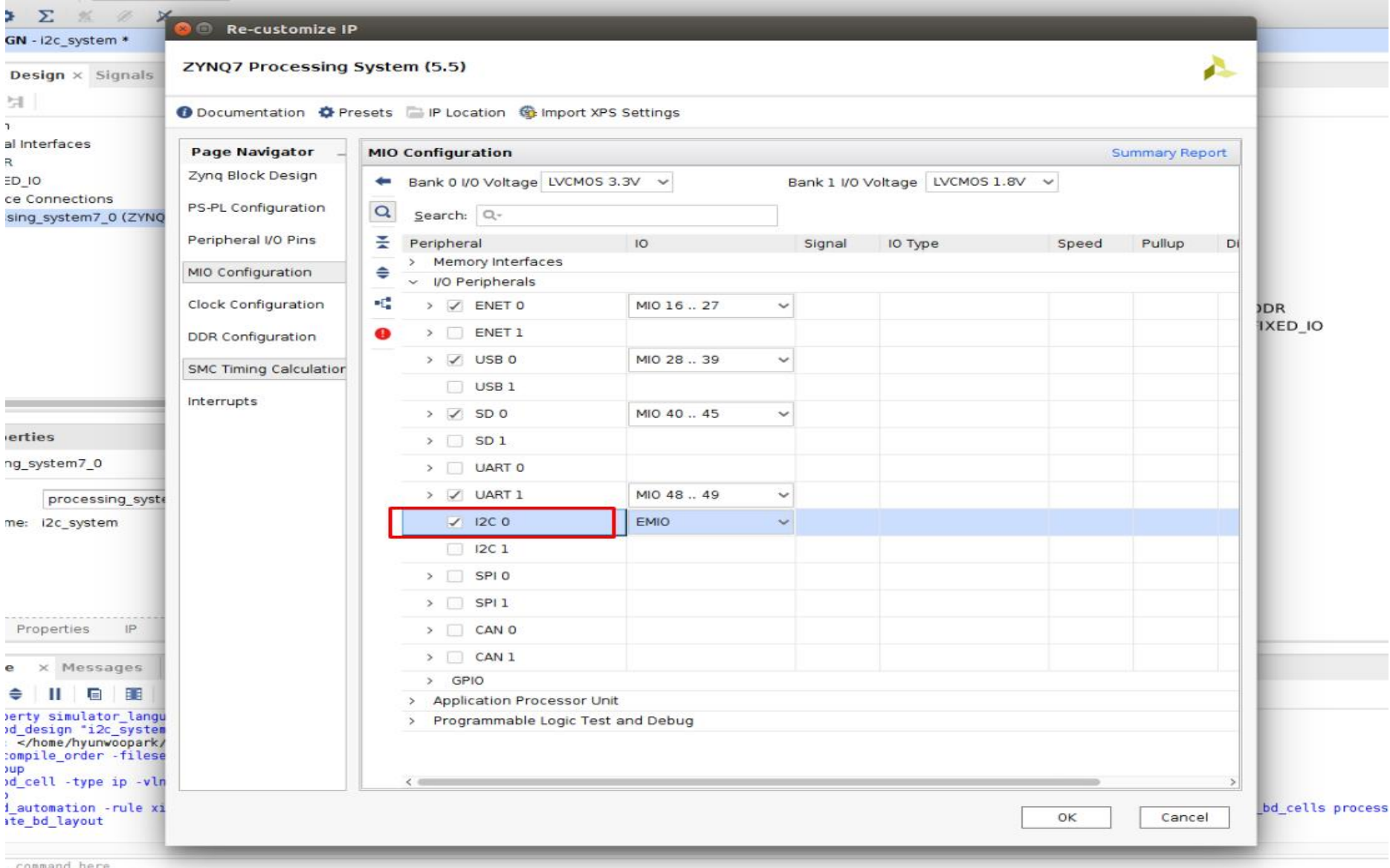
1) Vivado I2C 설계 4



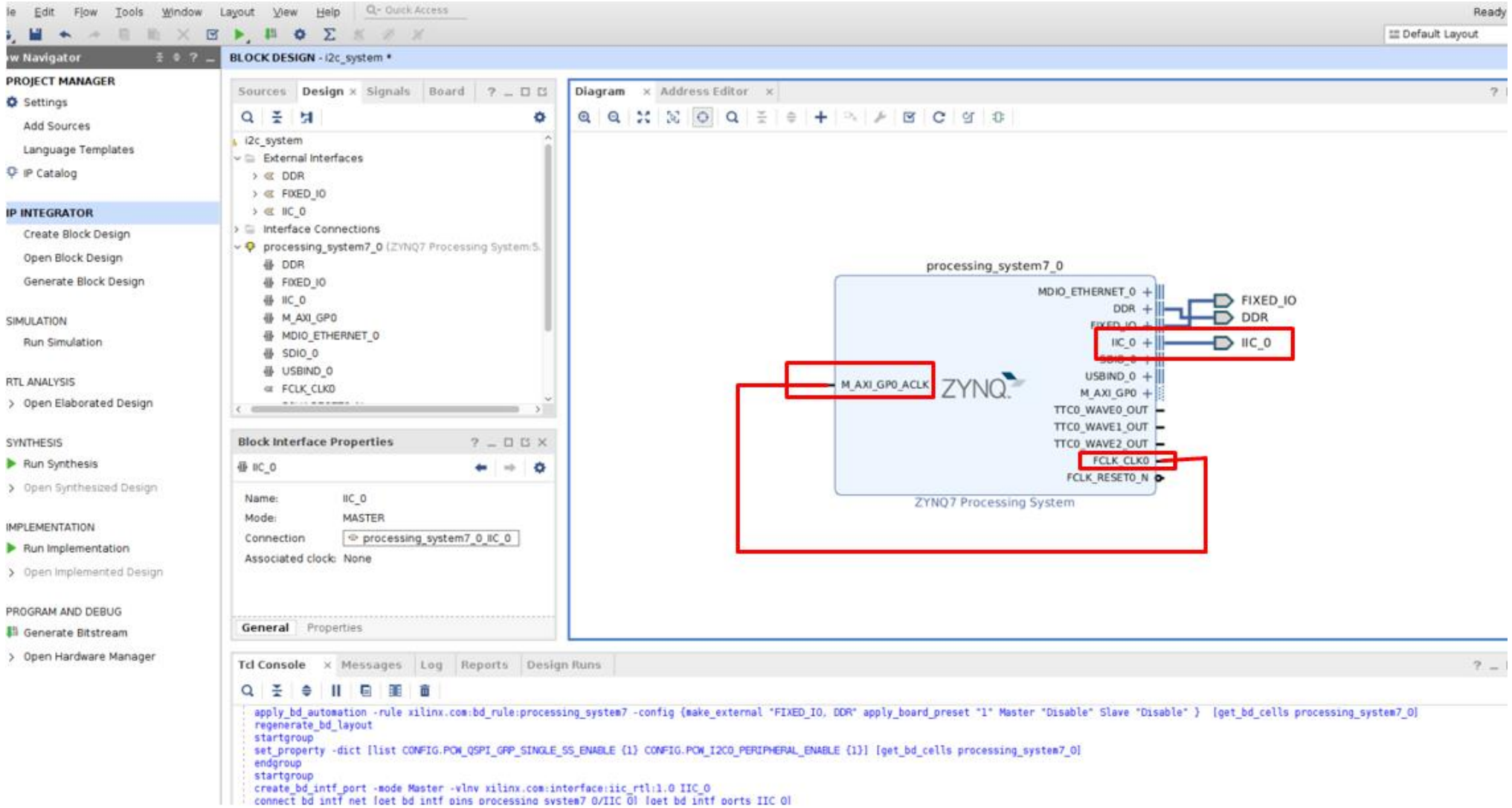
1) Vivado I2C 설계 5



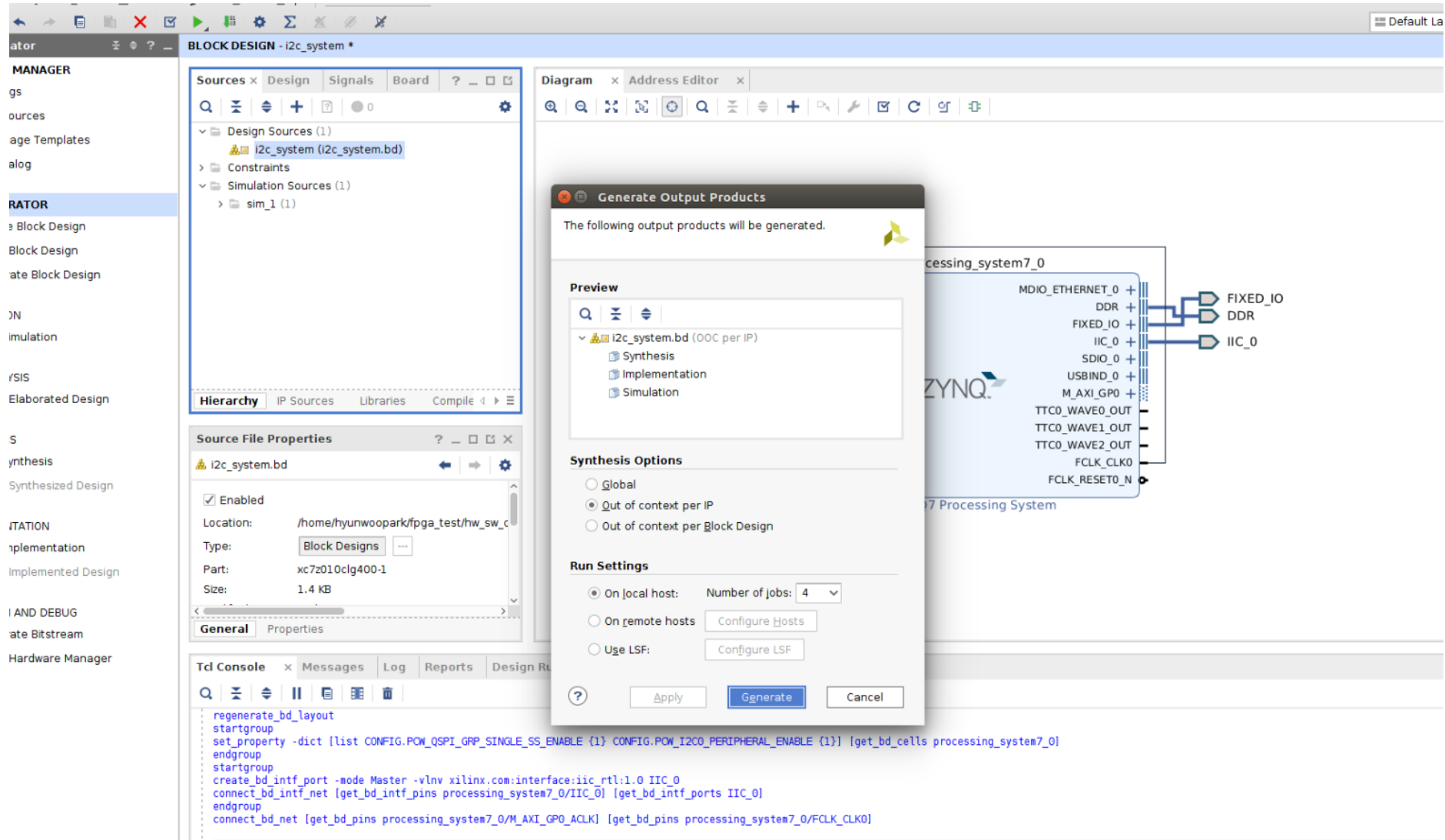
1) Vivado I2C 설계 6



1) Vivado I2C 설계 7



1) Vivado I2C 설계 8



1) Vivado I2C 설계 9

The screenshot displays the Vivado IDE interface during the final stages of an I2C system design. The left sidebar shows the project hierarchy with 'Sources' expanded, listing 'Design Sources (1)' containing 'i2c_system (i2c_system.bd) (1)', 'Constraints', and 'Simulation Sources (1)' containing 'sim_1 (1)'. The 'Source File Properties' window for 'i2c_system.bd' is open, showing it is enabled, located at '/home/hyunwoopark/fpga_test/hw_sw', and is a 'Block Designs' type for part 'xc7z010clg400-1' with a size of 25.7 KB. The 'Diagram' window shows a block diagram of 'processing_system7_0' with various interfaces connected to external components like 'FIXED_IO', 'DDR', and 'IIC_0'. A 'Generate Output Products' dialog box is centered on the screen, displaying an information icon and the message: 'Out-of-context module run was launched for generating output products.' with an 'OK' button. The bottom 'Tcl Console' window shows the command 'generate_target all' and its output, indicating that targets are already up-to-date and no re-generation is needed.

Sources x **Design** | **Signals** | **Board** | ? | - | + | x

Design Sources (1)
 i2c_system (i2c_system.bd) (1)
Constraints
Simulation Sources (1)
 sim_1 (1)

Source File Properties | ? | - | + | x

i2c_system.bd
[?] [←] [→]
[x] Enabled
Location: /home/hyunwoopark/fpga_test/hw_sw
Type: Block Designs
Part: xc7z010clg400-1
Size: 25.7 KB
General Properties

Diagram x **Address Editor** x

processing_system7_0
MDIO_ETHERNET_0 +
DDR +
FIXED_IO +
IIC_0 +
SDIO_0 +
USBIND_0 +
M_AXI_GP0 +
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N

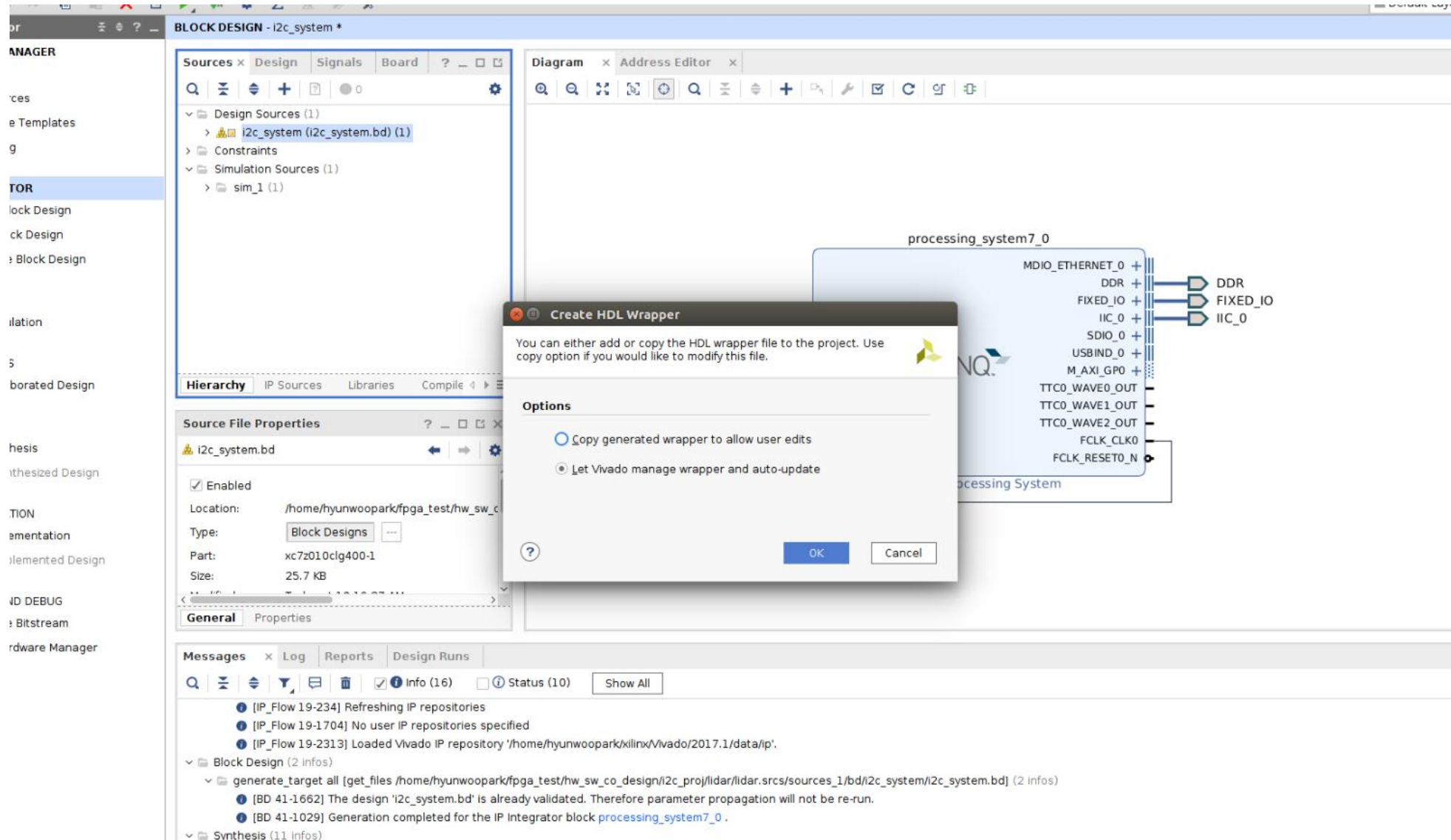
Generate Output Products

Out-of-context module run was launched for generating output products.
OK

Tcl Console x **Messages** | **Log** | **Reports** | **Design Runs**

```
generate_target all [get_files /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/lidar/lidar.srscs/sources_1/bd/i2c_system/i2c_system.bd]  
INFO: [BD 41-1637] Generated targets are already up-to-date for bd-design 'i2c_system' - hence not re-generating.  
catch { config_ip_cache -export [get_ips -all i2c_system_processing_system7_0_0] }  
export_ip_user_files -of_objects [get_files /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/lidar/lidar.srscs/sources_1/bd/i2c_system/i2c_system.bd] -no_script -sync -force -quiet  
create_ip_run [get_files -of_objects [get_filesset sources_1] /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/lidar/lidar.srscs/sources_1/bd/i2c_system/i2c_system.bd]  
launch_runs -jobs 4 i2c_system_processing_system7_0_0_synth_1
```

1) Vivado I2C 설계 10



1) Vivado I2C 설계 11

The screenshot displays the Vivado IDE interface during the synthesis phase of an I2C design. The left sidebar contains a project tree with the following structure:

- Design Sources (1)
 - i2c_system_wrapper(STRUCTURE) (i2c_system_)
- Constraints
 - constrs_1
- Simulation Sources (1)
 - sim_1 (1)

The 'Source File Properties' window for 'i2c_system_wrapper.vhd' is open, showing the following details:

- Enabled: ☒
- Location: /home/hyunwoopark/fpga_test/hw_sw_c
- Type: VHDL
- Library: xil_defaultlib
- Size: 4.5 KB

The main workspace shows a hardware design of a ZYNQ7 Processing System. A 'Synthesis Completed' dialog box is overlaid on the design, indicating that the synthesis was successful. The dialog provides the following options for the next step:

- ☒ Run Implementation
- ☐ Open Synthesized Design
- ☐ View Reports
- ☐ Don't show this dialog again

The background hardware design shows the ZYNQ7 Processing System with various components connected to the system bus, including MDIO_ETHERNET_0, DDR, FIXED_IO, IIC_0, SDIO_0, USBIND_0, M_AXI_GP0, TTC0_WAVE0_OUT, TTC0_WAVE1_OUT, TTC0_WAVE2_OUT, FCLK_CLK0, and FCLK_RESET0_N.

The bottom status bar shows the 'Messages' window with the following information:

- Vivado Commands (3 infos)
 - General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository '/home/hyunwoopark/xilinx/Vivado/2017.1/data/ip'.

1) Vivado I2C 설계 12

Navigator

Add Sources

Language Templates

IP Catalog

INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

ULATION

Run Simulation

ANALYSIS

Open Elaborated Design

ITHESIS

Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

Report DRC

Report Noise

Report Utilization

Report Power

Schematic

IMPLEMENTATION

Run Implementation

Open Implemented Design

Constraints Wizard

Edit Timing Constraints

IMPLEMENTS DESIGN * - xc7z010clg400-1 (active)

Sources

Netlist

Device Constraints

Internal VREF

0.6V

0.675V

0.75V

0.9V

NONE (2)

I/O Bank 34

I/O Bank 35

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

I/O Port Properties

Clock Regions

iic_0_sda_io

Name: iic_0_sda_io

Direction: INOUT

Package pin: H15

Fixed

Site type: IO_L19P_T3_35

Site info: IOB_X0Y62

Cell: iic_0_sda_iobuf

Net: iic_0_sda_iobuf/I/O

General

Properties

Configure

Power

Package

Device

i2c_system_wrapper.vhd

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

A B C D E F G H I J K L M N P Q R T U V W X Y

Tcl Console

Messages

Log

Reports

Design Runs

Timing

Power

DRC

Package Pins

I/O Ports

Name

Direction

Board Part Pin

Board Part Interface

Neg Diff Pair

Package Pin

Fixed

Bank

I/O Std

Vcco

Vref

Drive Strength

Slew Type

Pull Type

Off-Ch

> DDR_53145 (71)

INOUT

✓

502

(Multiple)*

1.500

(Multiple)

(Multiple)*

(Multiple)*

(Multiple)*

NONE

FP_VT

> FIXED_IO_53145 (59)

INOUT

✓

(Multiple)

(Multiple)*

(Multiple)

(Multiple)

(Multiple)*

(Multiple)*

(Multiple)

(Multij

> IIC_0_53145 (2)

INOUT

✓

35

LVCMOS33*

3.300

12

SLOW

NONE

FP_VT

> Scalar ports (2)

iic_0_scl_io

INOUT

✓

35

LVCMOS33*

3.300

12

SLOW

NONE

FP_VT

iic_0_sda_io

INOUT

✓

35

LVCMOS33*

3.300

12

SLOW

NONE

FP_VT

> Scalar ports (0)

1) Vivado I2C 설계 13

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj$ ls
lidar
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj$ mkdir PETALINUX
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj$ ls
lidar PETALINUX
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj$ cd PETALINUX/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX$ ls
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX$
```

먼저, petalinux-create project create 해야함

```
INFO: Create project: i2c_lidar
INFO: New project successfully created in /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX$ ls
i2c_lidar
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX$ cd i2c_lidar/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ ls
config.project hw-description subsystems
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ petalinux-config --get-hw-description=~/fpga_test/
hw_sw_co_design/i2c_proj/lidar/lidar.sdk
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename i2c_system_wrapper.hdf to system.hdf

***** hsi v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/build/linux/hw-description/hw-description.tcl -notrace
INFO: [Common 17-206] Exiting hsi at Tue Jun 5 10:49:46 2018...
INFO: Config linux
[INFO ] config linux
Configuration written to /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

[INFO ] generate DTS to /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 5 seconds
WARNING: ps7_ethernet_0: No reset found
WARNING: ps7_i2c_0: No reset found
INFO: [Common 17-206] Exiting hsi at Tue Jun 5 10:50:04 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Tue Jun 5 10:50:17 2018...
```

1) Vivado I2C 설계 14

Petalinux 개조를 하려면 여기서 bootcode를 건들이면 됨.

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description subsystems
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ cd components/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components$ ls
bootloader
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components$ cd bootloader/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader$ ls
zynq_fsbl
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader$ cd zynq_fsbl/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ ls
fsbl_debug.h  fsbl_hooks.c  image_mover.h  Makefile  nand.c  nor.h  ps7_init.c  qspl.c  rsa.h  zynq_fsbl_bsp
fsbl.h        fsbl_hooks.h  lscript.ld     md5.c     nand.h  pcap.c  ps7_init.h  qspl.h  sd.c
fsbl_handoff.S image_mover.c main.c       md5.h     nor.c   pcap.h  ps7_parameters.xml  rsa.c  sd.h
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$
```

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ vi main.c
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ petalinux-config
-c u-boot
INFO: Checking component...
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
#
# configuration written to .config
#
[INFO ] config linux/u-boot

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$
```


1) Vivado I2C 설계 15

```
/home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/configs/u-boot/config - U-Boot 2015.07 Configurati
> Device Drivers
Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing
<Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [*]
built-in [ ] excluded <M> module < > module capable

1. Device Drivers
    [*] Enable Driver Model
    [*] Enable warnings in driver model
    [*] Support device removal
    [*] Support stdio registration
    [*] Support numbered aliases in device tree
    [ ] Enable CPU drivers using Driver Model
    [ ] Enable demo uclass support
    PCI ---->
    NAND Device Support ---->
    SPI Flash Support ---->
    [ ] Enable Chrome OS EC
    [ ] Enable FSL SEC_MON Driver
    [ ] Enable PCA9551 LED driver
    [ ] Enable Driver Model for Ethernet drivers
    [ ] Network device support ----
    [ ] Enable Chrome OS EC keyboard support
    [ ] Enable Driver Model for serial drivers
    [ ] Enable an early debug UART for debugging
    [ ] Enable sandbox TPM driver
2. [*] Enable Driver Model for I2C drivers
    [*] Enable I2C compatibility layer
    SPI Support ---->
    [ ] Enable Driver Model for GPIO drivers
    [ ] LPC32XX GPIO driver
    [ ] Vybrid GPIO driver
    Power ---->
    [ ] Enable VESA video driver support
    [ ] SSD2828 bridge chip
    [ ] Enable DisplayPort support
    [ ] Enable video support on Tegra124
    [ ] Enable sound support
    [ ] Support for Host-side USB
    MMC Host controller Support ----
    [ ] Enable Driver Model for RTC drivers
    [ ] Freescale Crypto Driver Support
    [ ] Driver support for thermal devices

<Select> < Exit > < Help > < Save > < Load >
```

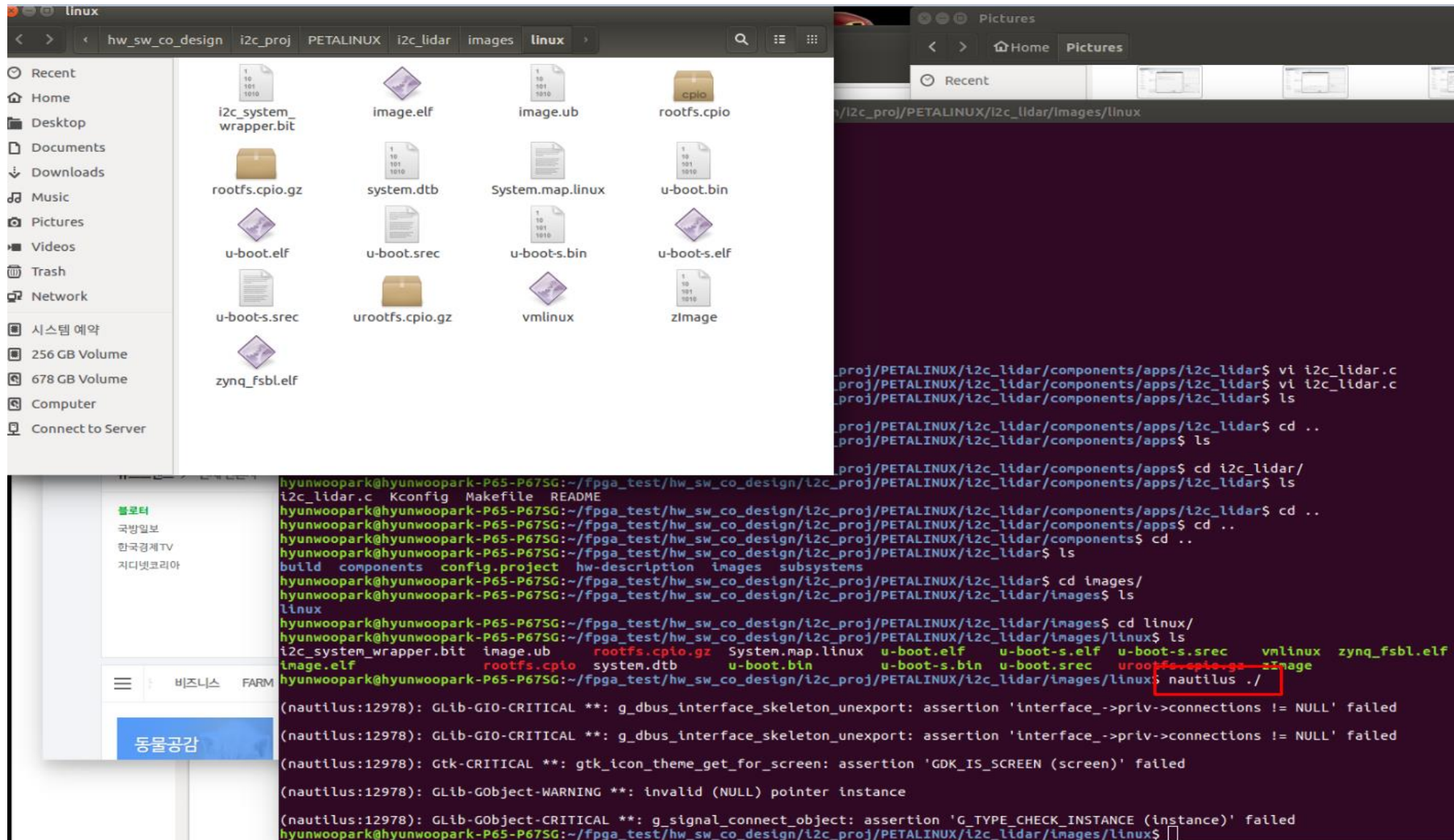
1) Vivado I2C 설계 16

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build system.dtb
[INFO ] build linux/kernel
```

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ petalinux-create -t apps -n i2c_lidar --enable
INFO: Create apps: i2c_lidar
INFO: New apps successfully created in /home/hyunwoopark/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar
INFO: Enabling created component...
INFO: It has been enabled to linux/rootfs
```

```
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar$ cd components/apps/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/apps$ ls
i2c_lidar
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/apps$ cd i2c_lidar/
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar$ ls
i2c_lidar.c Kconfig Makefile README
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar$ vi i2c_lidar.c
```

1) Vivado I2C 설계 17



1) Vivado I2C 설계 18

```
(nandctl.12978): Glib-GObject-CRITICAL **: g_signal_connect_object: assertion 'G_TYPE_CHECK_INSTANCE (instance)' failed
hyunwoopark@hyunwoopark-P65-P67SG:~/fpga_test/hw_sw_co_design/i2c_proj/PETALINUX/i2c_lidar/images/linux$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/i2c_lidar
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] build zynq-fsbl
```

2) LIDAR 센서 제어 C code 1

```
#include <stdio.h>
#include <linux/i2c.h>
#include <linux/i2c-dev.h>
#include <sys/ioctl.h>
#include <fcntl.h>
#include <unistd.h>
#include <errno.h>
#include <string.h>
#include <stdlib.h>
#include <sys/types.h>
#include <sys/stat.h>
```

```
#define I2C_FILE_NAME_0  "/dev/i2c-0"
#define I2C_FILE_NAME_1  "/dev/i2c-1"
#define LIDAR_SLAVE_ADDR 0x62
```

```
#define ACQ_COMMAND      0x00
#define STATUS           0x01
#define SIG_COUNT_VAL    0x02
#define ACQ_CONFIG_REG   0x04
#define THRESHOLD_BYPASS 0x1C
#define READ_FROM        0x89
```

```
#define NO_CORRECTION     0
#define CORRECTION        1
```

```
#define AR_VELOCITY      0
#define AR_PEAK_CORR     1
#define AR_NOISE_PEAK    2
#define AR_SIGNAL_STRENGTH 3
#define AR_FULL_DELAY_HIGH 4
#define AR_FULL_DELAY_LOW 5
```

```
#define OUTPUT_OF_ALL    0
#define DISTANCE_ONLY    1
#define DISTANCE_WITH_VELO 2
#define VELOCITY_ONLY    3
```

```
#define USAGE  "i2c_LiDAR_fn <OUTPUT_OPTIONS>\n\
<I2C_DEVICE_NUMBER>Wn"W\n\
    "<OUTPUT_OPTION>Wn"W\n\
    "0 : output of allWn"W\n\
    "1 : distance onlyWn"W\n\
    "2 : distance with velocityWn"W\n\
    "3 : velocity onlyWn"W
```

```
unsigned get_status();
void i_read(unsigned char, unsigned, unsigned char*);
void i_write(unsigned char reg, unsigned char value);
void measurement(unsigned char, unsigned char, unsigned char*);
void display(unsigned char, unsigned char*);
```

```
int fd = 0;
```

```
int main(int argc, char **argv){
    unsigned char receives[8] = {AR_VELOCITY, 0, 0, AR_PEAK_CORR, AR_NOISE_PEAK,
        AR_SIGNAL_STRENGTH, AR_FULL_DELAY_HIGH, AR_FULL_DELAY_LOW};
    unsigned char i, options;
    char *file_name = NULL;
```

```
    if(argc < 2) printf("%sWn",USAGE);
    else if(argc > 2 && atoi(argv[2])) file_name = I2C_FILE_NAME_1;
    else file_name = I2C_FILE_NAME_0;
```

```
    options = atoi(argv[1]);
```

```
    if((fd = open(file_name, O_RDWR)) < 0){
```

```
        perror("---OPEN DEVICE ERROR ");
        return -1;
```

```
    }
```

```
    if(ioctl(fd, I2C_SLAVE, LIDAR_SLAVE_ADDR) < 0){
```

```
        perror("---SLAVE ADDR CONNECT ERROR");
        return -1;
```

```
    }
```

```
    i_write(SIG_COUNT_VAL, 0x80);
    i_write(ACQ_CONFIG_REG, 0x08);
    i_write(THRESHOLD_BYPASS, 0x00);
```

```
    while(1){
        measurement(CORRECTION, options, receives);
        for(i=0; i<99; i++)
            measurement(NO_CORRECTION, options, receives);
    }
    close(fd);
    return 0;
```

```
}
```

2) LIDAR 센서 제어 C code 2

```
unsigned get_status(){
    unsigned char buf[1] = {STATUS};

    if(write(fd, buf, 1) != 1){
        perror("---WRITE REGISTER ERROR ");
        return 1;
    }

    if(read(fd, buf, 1) != 1){
        perror("---WRITE REGISTER ERROR ");
        return 1;
    }

    return buf[0] & 0x01;
}

void i_read(unsigned char reg, unsigned read_size, unsigned
char *receives){
    unsigned char buf[1] = {reg};
    unsigned busy_flag = 1, busy_counter = 0;

    while(busy_flag) {
        busy_flag = get_status();
        busy_counter ++;
        if(busy_counter > 9999) {
            printf("BUSY COUNT TIME OUTT !Wn");
            return ;
        }
    }
    if(!busy_flag){
        if(write(fd, buf, 1) != 1){
            perror("---WRITE REGISTER ERROR ");
            return ;
        }

        if(read(fd, receives, read_size) != read_size){
            perror("---WRITE REGISTER ERROR ");
            return ;
        }
    }
}
```

```
void i_write(unsigned char reg, unsigned char value){
    unsigned char buf[2] = {reg, value};

    if(write(fd, buf, 2) != 2){
        perror("---WRITE REGISTER ERROR ");
        return ;
    }
    usleep(1000);
}

void measurement(unsigned char is_correction, unsigned char options, unsigned
char *buf){
    unsigned char i;
    if(is_correction) i_write(ACQ_COMMAND, 0x04);
    else i_write(ACQ_COMMAND, 0x03);

    i_read(READ_FROM, 8, buf);

    for(i=1;i<6; i++) buf[i] = buf[i+2];

    display(options, buf);
}

void display(unsigned char options, unsigned char *buf){
    unsigned char i;
    char* strings[5] = {"Velocity", "Peak value in correlation record",
        "Correlation record noise floor", "Received signal strength", "Distance"};
    buf[AR_FULL_DELAY_HIGH] = buf[AR_FULL_DELAY_HIGH] << 8 |
    buf[AR_FULL_DELAY_LOW];

    switch(options){
        case OUTPUT_OF_ALL :
            for(i=0; i<5; i++) printf("%s WtWtWtWt = %dWn", strings[i], buf[i]);
            break;
        case DISTANCE_ONLY :
            printf("%s WtWtWtWt = %dWn", strings[4], buf[AR_FULL_DELAY_HIGH]);
            break;
        case DISTANCE_WITH_VELO :
            printf("%s WtWtWtWt = %dWn", strings[0], buf[AR_VELOCITY]);
            printf("%s WtWtWtWt = %dWn", strings[4], buf[AR_FULL_DELAY_HIGH]);
            break;
        case VELOCITY_ONLY :
            printf("%s WtWtWtWt = %dWn", strings[0], buf[AR_VELOCITY]);
            break;
    }
    printf("Wn");
}
```


3) LIDAR 제어 결과물

