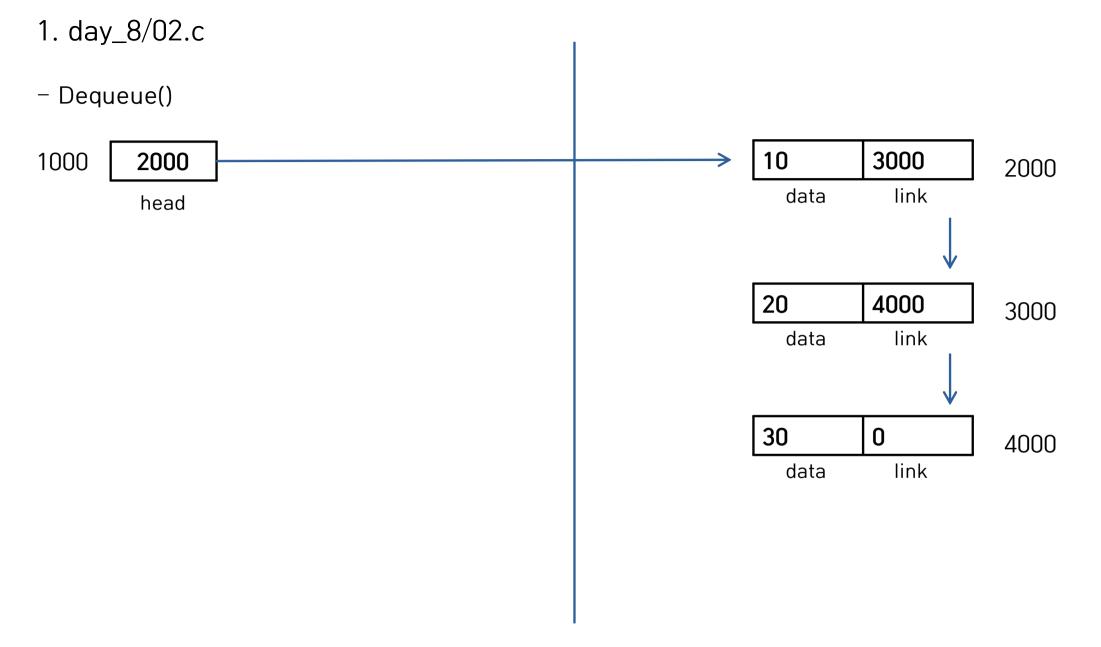
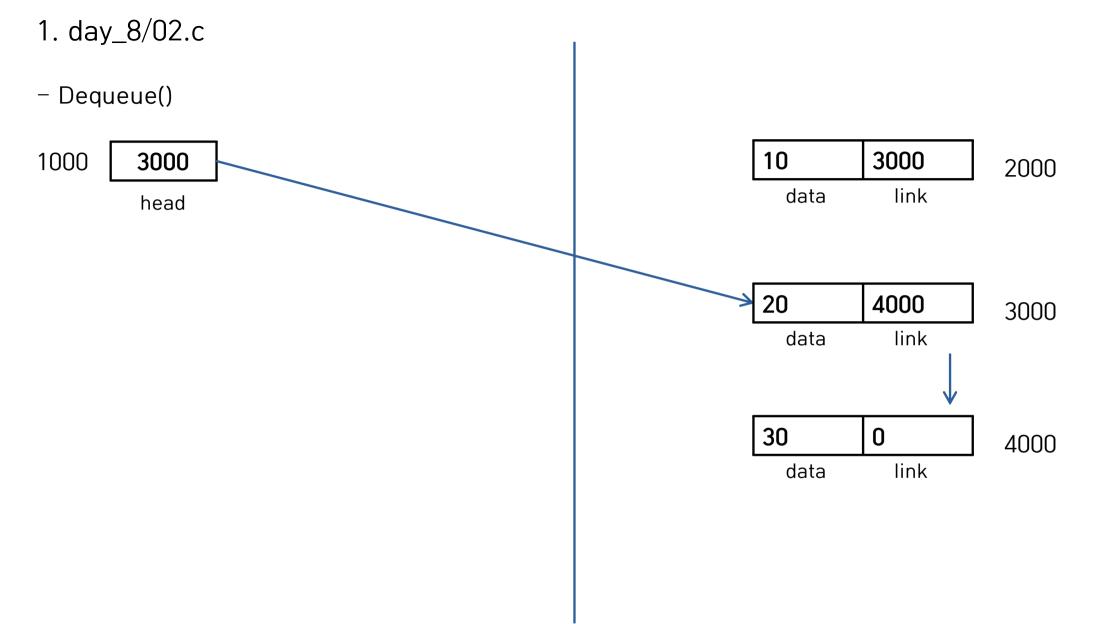
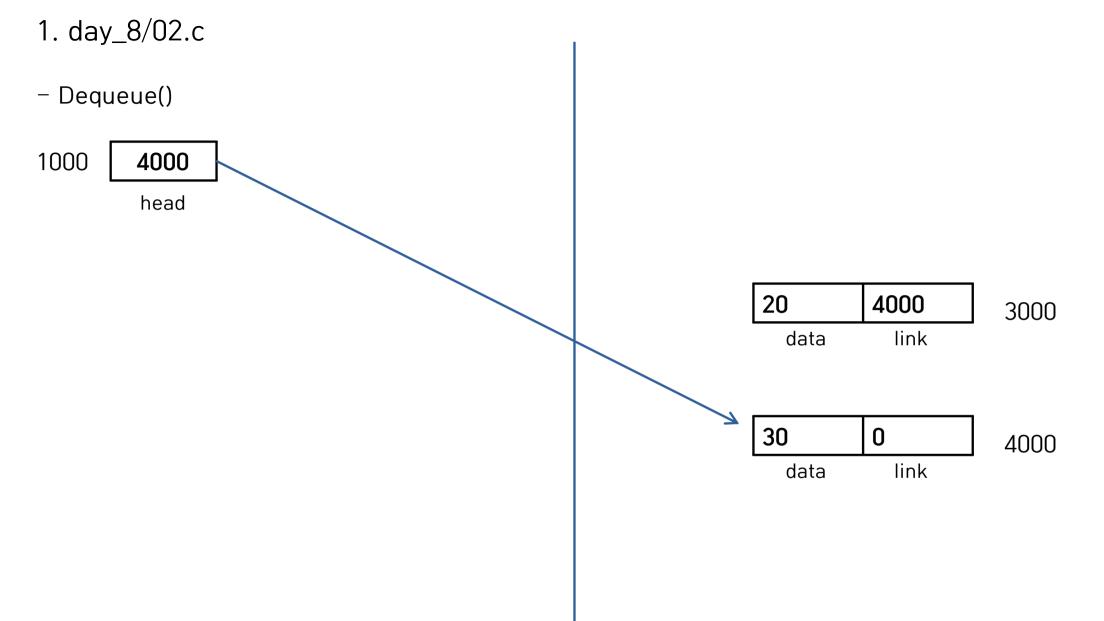
Xilinx Zynq FPGA, TI DSP, MCU 기반의 프로그래밍 및 회로 설계 전문가 과정

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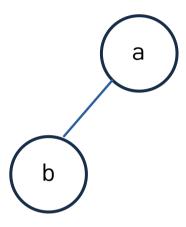




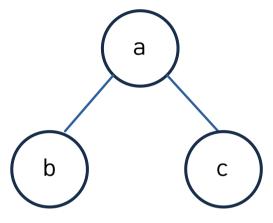
- tree_ins(root, data)



- tree_ins(root, data)



- tree_ins(root, data)



```
tree_ins(root, c)
{

if(root == NULL)

{

root에 메모리 생성
root에 data 입력

}

else
{

(1) 인자값 c가 root의 data값 a보다 작거나 같은 경우
tree_ins(root->pLeft, c)

(2) 인자값 c가 root의 data값 a보다 큰 경우
tree_ins(root->pRight, c)

}
```

