Xilinx Zynq FPGA, TI DSP, MCU 기반

의

프로그래밍 및 회로 설계 전문가 과정

#49

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trimLPO();

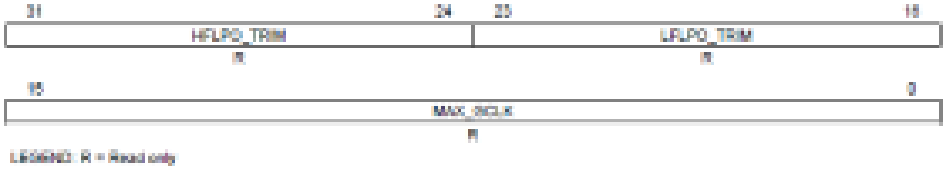
```
void trimLPO(void)
{

/* USER CODE BEGIN (4) */
/* USER CODE END */

    /** @b Initialize Lpo: */
    /** Load TRIM values from OTP if present else load user defined values */
    /*SAFETYMCUSW 139 S MR:13.7 <APPROVED> "Hardware status bit read check" */
    if(LPO_TRIM_VALUE != 0xFFFFU)
    {

        systemREG1->LPOMONCTL  = (uint32)((uint32)1U << 24U)
                               | LPO_TRIM_VALUE;
    }
    else
    {

        systemREG1->LPOMONCTL   =  (uint32)((uint32)1U << 24U)
                                | (uint32)((uint32)16U << 8U)
                                | 16U;
    }

/* USER CODE BEGIN (5) */
/* USER CODE END */

}
```

#define LPO_TRIM_VALUE (((*(volatile uint32 *)0xF00801B4U) & 0xFFFF0000U)>>16U)
최상위 16 비트만 뽑는다.

7.5.2.3 LPO Trim and Max HCLK

The HF LPO trim solution, LF LPO trim solution and maximum GCLK1 frequency can be read from TI OTP location F008 01B4h as shown in Figure 7-5 and described in Table 7-7.

Figure 7-5. TI OTP Bank 0 LPO Trim and Max HCLK Information



LEGEND: R = Read only

Table 7-7. TI OTP Bank 0 LPO Trim and Max HCLK Information Field Descriptions

Bit	Field	Description
31-24	HFLPO_TRIM	HF LPO Trim Solution
23-16	LFLPO_TRIM	LF LPO Trim Solution
15-0	MAX_GCLK	Maximum GCLK1 Speed

HFLPO_TRIM 의 정보가 MAX_GCLK 로 들어간다

2.5.1.30 LPO/Clock Monitor Control Register (LPOMONCTL)

The LPOMONCTL register, shown in Figure 2-37 and described in Table 2-49, controls the Low Frequency (Clock Source 4) and High Frequency (Clock Source 5) Low Power Oscillator's trim values.

Figure 2-37. LPO/Clock Monitor Control Register (LPOMONCTL) (offset = 088h)

31–25	24	23–17	16
Reserved	BIAS ENABLE	Reserved	OSCFRQCONFIGCNT
R-0	R/WP-1	R-0	R/WP-0

15–13	12–8	7–5	4–0
Reserved	HFTRIM	Reserved	LFTRIM
R-0	R/WP-10h	R-0	R/WP-10h

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -n = value after reset

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Reads return 0. Writes have no effect.
24	BIAS ENABLE		Bias enable.
		0	The bias circuit inside the low-power oscillator (LPO) is disabled.
		1	The bias circuit inside the low-power oscillator (LPO) is enabled.
23-17	Reserved	0	Reads return 0. Writes have no effect.
16	OSCFRQCONFIGCNT		Configures the counter based on OSC frequency.
		0	*Read*: OSC freq is ≤ 20MHz. *Write*: A write of 0 has no effect.
		1	*Read*: OSC freq is > 20MHz and ≤ 80MHz. *Write*: A write of 1 has no effect.
15-13	Reserved	0	Reads return 0. Writes have no effect.

```
LPOMONCNTL = (uint32)((uint32)1U << 24U)
                                    | LPO_TRIM_VALUE;
```

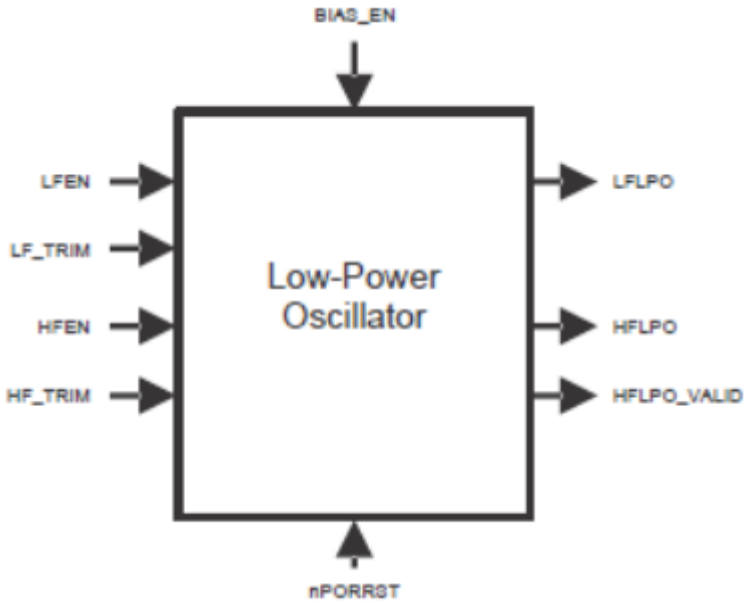
24 번 비트를 1 로 설정하고 HFLPO_TRIM 의 정보가 MAX_GCLK 를 or 연산한다.

24 번 비트는 BIAS ENABLE 로 1 일때 바이어스회로가 저전력 오실레이터로 동작가능하다.

Table 2-49. LPO/Clock Monitor Control Register (LPOMONCTL) Field Descriptions (continued)

Bit	Field	Value	Description
12-8	HFTRIM		High-frequency oscillator trim value. This four-bit value is used to center the HF oscillator's frequency. **Caution: This value should only be changed when the HF oscillator is not the source for a clock domain, otherwise a system failure could result.** The following values are the ratio: f / fo in the F021 process.
		0	29.52
		1h	34.24%
		2h	38.85%
		3h	43.45%
		4h	47.99%
		5h	52.55%
		6h	57.02%
		7h	61.46%
		8h	65.92%
		9h	70.17
		Ah	74.55%
		Bh	78.92%
		Ch	83.17%
		Dh	87.43%
		Eh	91.75%
		Fh	95.89%
		10h	100.00% Default at Reset
		11h	104.09
		12h	108.17
		13h	112.32
		14h	116.41
		15h	120.67
		16h	124.42
		17h	128.38
		18h	132.24
		19h	136.15
		1Ah	140.15
		1Bh	143.94
		1Ch	148.02
		1Dh	151.80x
		1Eh	155.50x
		1Fh	159.35%
7-5	Reserved	0	Reads return 0. Writes have no effect.

LPO_TRIM_VALUE 는 HFLPO_TRIM 의 리셋 벨류가 MAX_GCLK 에 저장된 상태 즉 리셋상태이므로 10h 100% Default at Reset 상태이다.
이는 LPO 회로를 보며 설명한다.



위의 설정은 LPO 회로의 BIAS 를 동작시키고 나머지들을 손실없이 원래값 그대로 동작시킨다는 뜻이 된다.
LF low freq
HF High freq
lf = 80khz
hf = 10mhz

mapClocks();

2.5.2.6 HCLK Control Register (HCLKCNTL)

This register is shown in Figure 2-64 and described in Table 2-77.

Figure 2-64. HCLK Control Register (HCLKCNTL) (offset = 54h)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		HCLKR	
R-0		R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-77. HCLK Control Register (HCLKCNTL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reads return 0. Writes have no effect.
1-0	HCLKR		HCLK divider value. The value of HCLKR bits determine the HCLK frequency as a ratio of GCLK1.
		0	HCLK is equal to GCLK1 divide by 1.
		1h	HCLK is equal to GCLK1 divide by 2.
		2h	HCLK is equal to GCLK1 divide by 3.
		3h	HCLK is equal to GCLK1 divide by 4.

디바이스모듈가 여기에 들어가는 클록을 매칭시켜준다.

HCLKCNTL = 1U

GCLK1 을 갖고와서 2 분주 해서 사용한다.

Figure 2-20. Clock Domain Disable Register (CDDIS) (offset = 3Ch)

31	16
Reserved	
R-0	

15	12	11	10	9	8
Reserved		VCLKA4OFF	Reserved	Reserved	VCLK3OFF
R-0		R/WP-0	R/WP-0	R/WP-0	R/WP-0

7	6	5	4	3	2	1	0
Reserved	RTICLK1OFF	VCLKA2OFF	VCLKA1OFF	VCLK2OFF	VCLKPOFF	HCLKOFF	GCLK1OFF
R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-32. Clock Domain Disable Register (CDDIS) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
11	VCLKA4OFF		VCLKA4 domain off.
		0	The VCLKA4 domain is enabled.
		1	The VCLKA4 domain is disabled.
10-9	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
8	VCLK3OFF		VCLK3 domain off.
		0	The VCLK3 domain is enabled.
		1	The VCLK3 domain is disabled.
7	Reserved	0-1	Reads return 0 or 1 and privilege mode writes allowed.
6	RTICLK1OFF		RTICLK1 domain off.
		0	The RTICLK1 domain is enabled.
		1	The RTICLK1 domain is disabled.
5-4	VCLKA[2-1]OFF		VCLKA[2-1] domain off.
		0	The VCLKA[2-1] domain is enabled.
		1	The VCLKA[2-1] domain is disabled.
3	VCLK2OFF		VCLK2 domain off.
		0	The VCLK2 domain is enabled.
		1	The VCLK2 domain is disabled.
2	VCLKPOFF		VCLK_periph domain off.
		0	The VCLK_periph domain is enabled.
		1	The VCLK_periph domain is disabled.

4 번비트 0 , 5 번비트 1, 8 번비트 0, 9 번비트 0, 10 번비트 0, 11 번비트 0

4 번비트 0 The VCLKA1[2-1] domain is enabled.

vclka1 can 통신에 이용 110MHz 동작주파수

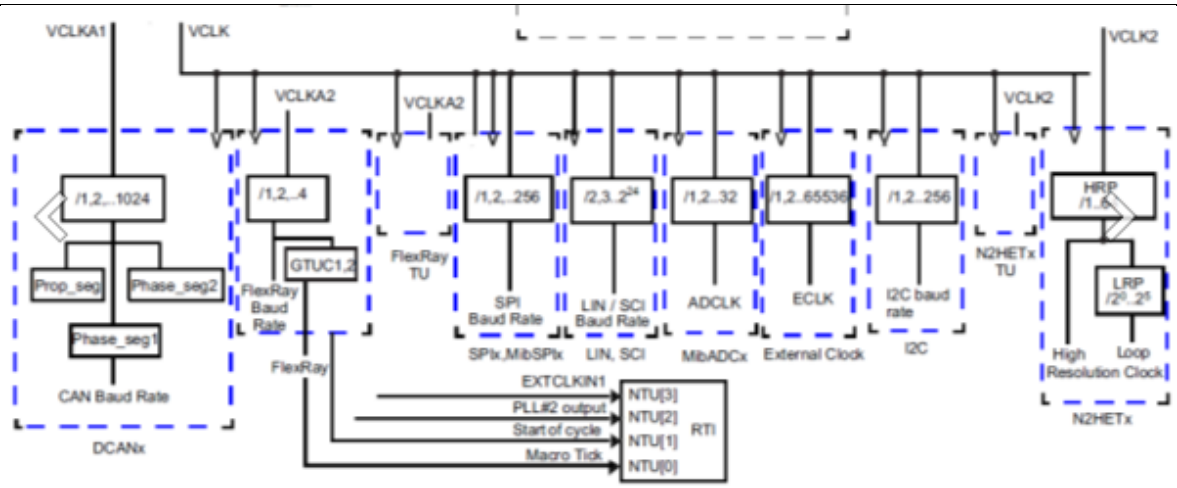


Figure 6-6. Device Clock Domains

5 번비트 1

The VCLKA2[2-1] domain is disabled.

Flex Ray = can 통신 일부 비쌈 그걸 비활성화

8 bit The VCLK3 domain is enabled.

11 bit The VCLKA4 domain is enabled.

VCLK4 는 분주해서 이더넷으로 사용

VCLK3 는 이더넷이랑 EMIF 로 같이들어감

2.5.1.19 Clock Source Valid Status Register (CSVSTAT)

The CSVSTAT register, shown in Figure 2-26 and described in Table 2-38, indicates the status of usable clock sources.

Figure 2-26. Clock Source Valid Status Register (CSVSTAT) (offset = 54h)

31							8
Reserved							
R-0							

7	6	5	4	3	2	1	0
CLKSR7V	CLKSR6V	CLKSR5V	CLKSR4V	CLKSR3V	Reserved	CLKSR1V	CLKSR0V
R-1	R-0	R-0	R-1	R-1	R-0	R-0	R-0

LEGEND: R = Read only; -n = value after reset

Table 2-38. Clock Source Valid Register (CSVSTAT) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved.	0	Reads return 0. Writes have no effect.
7-3	CLKSR[7-3]V		Clock source[7-0] valid.
		0	Clock source[7-0] is not valid.
		1	Clock source[7-0] is valid.
			Note: If the valid bit of the source of a clock domain is not set (that is, the clock source is not fully stable), the respective clock domain is disabled by the Global Clock Module (GCM).
2	Reserved.	0	Reads return 0. Writes have no effect.
1-0	CLKSR[1-0]V		Clock source[1–0] valid.
		0	Clock source[1–0] is not valid.
		1	Clock source[1–0] is valid.
			Note: If the valid bit of the source of a clock domain is not set (that is, the clock source is not fully stable), the respective clock domain is disabled.

NOTE: A list of the available clock sources is shown in the Table 2-29.

데이터시트상 VCAT 했던거 안정화 됐으면 1 안되면 0 이 나온다.

이레지스터의 비트는 하드웨어가 셋팅해준다.

SYS_CSDIS = systemREG1->CSDIS;

2.5.1.10 Clock Source Disable Register (CSDIS)

The CSDIS register, shown in Figure 2-17 and described in Table 2-28, controls and displays the state of the device clock sources.

Figure 2-17. Clock Source Disable Register (CSDIS) (offset = 30h)

31							8
Reserved							
R-0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKSR7OFF	CLKSR6OFF	CLKSR5OFF	CLKSR4OFF	CLKSR3OFF	Reserved	CLKSR1OFF	CLKSR0OFF
R/WP-1	R/WP-1	R/WP-0	R/WP-0	R/WP-1	R-1	R/WP-1	R/WP-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -n = value after reset

Table 2-28. Clock Source Disable Register (CSDIS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reads return 0. Writes have no effect.
7-3	CLKSR[7-3]OFF		Clock source[7-3] off.
		0	Clock source[7-3] is enabled.
		1	Clock source[7-3] is disabled.
			Note: On wakeup, only clock sources 0, 4, and 5 are enabled.
2	Reserved	1	Reads return 1. Writes have no effect.
1-0	CLKSR[1-0]OFF		Clock source[1-0] off.
		0	Clock source[1-0] is enabled.
		1	Clock source[1-0] is disabled.
			Note: On wakeup, only clock sources 0, 4, and 5 are enabled.

Table 2-29. Clock Sources Table

Clock Source #	Clock Source Name
Clock Source 0	Oscillator
Clock Source1	PLL1
Clock Source 2	Not Implemented
Clock Source 3	EXTCLKIN
Clock Source 4	Low Frequency LPO (Low Power Oscillator) clock
Clock Source 5	High frequency LPO (Low Power Oscillator) clock
Clock Source 6	PLL2
Clock Source 7	EXTCLKIN2

활성화된 클럭과 비활성화된 클럭을 명확히 구분한다.

디바이스 클럭소스의 상태를 보여줌 안정된 상태인지 불안정한 상태인지.

밑에 와일문에서 안정한 상태까지 반복한다.

```
while ((SYS_CSVSTAT & ((SYS_CSDIS ^ 0xFFU) & 0xFFU)) != ((SYS_CSDIS ^ 0xFFU) & 0xFFU))
    {
        SYS_CSVSTAT = systemREG1->CSVSTAT;
        SYS_CSDIS = systemREG1->CSDIS;
    } /* Wait */
```

안정화 상태가 되면 와일문을 빠져나온다.

```
systemREG1->GHVSRC = (uint32)((uint32)SYS_PLL1 << 24U)
                   | (uint32)((uint32)SYS_PLL1 << 16U)
                   | (uint32)((uint32)SYS_PLL1 << 0U);
```

GHVSRC 클럭을 어떤식으로 제어할지 봐주는 레지스터

SYS_PLL1 = 0x1U

SYS_PLL1 24 번 16 번 0 번 비트 활성화

2.5.1.16 GCLK1, HCLK, VCLK, and VCLK2 Source Register (GHVSRC)

The GHVSRC register, shown in Figure 2-23 and described in Table 2-35, controls the clock source configuration for the GCLK1, HCLK, VCLK and VCLK2 clock domains.

Figure 2-23. GCLK1, HCLK, VCLK, and VCLK2 Source Register (GHVSRC) (offset = 48h)

31 28	27 24	23 20	19 16
Reserved	GHVWAKE	Reserved	HVLPM
R-0	R/WP-0	R-0	R/WP-0

15 4	3 0
Reserved	GHVSRC
R-0	R/WP-0

LEGEND: R = Read only; R/W = Read/Write; WP = Write in privileged mode only; -*n* = value after reset

Table 2-35. GCLK1, HCLK, VCLK, and VCLK2 Source Register (GHVSRC) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reads return 0. Writes have no effect.
27-24	GHVWAKE		GCLK1, HCLK, VCLK source on wakeup.
		0	Clock source0 is the source for GCLK1, HCLK, VCLK on wakeup.
		1h	Clock source1 is the source for GCLK1, HCLK, VCLK on wakeup.
		2h	Clock source2 is the source for GCLK1, HCLK, VCLK on wakeup.
		3h	Clock source3 is the source for GCLK1, HCLK, VCLK on wakeup.
		4h	Clock source4 is the source for GCLK1, HCLK, VCLK on wakeup.
		5h	Clock source5 is the source for GCLK1, HCLK, VCLK on wakeup.
		6h	Clock source6 is the source for GCLK1, HCLK, VCLK on wakeup.
		7h	Clock source7 is the source for GCLK1, HCLK, VCLK on wakeup.
		8h-Fh	Reserved
23-20	Reserved	0	Reads return 0. Writes have no effect.
19-16	HVLPM		HCLK, VCLK, VCLK2 source on wakeup when GCLK1 is turned off.
		0	Clock source0 is the source for HCLK, VCLK, VCLK2 on wakeup.
		1h	Clock source1 is the source for HCLK, VCLK, VCLK2 on wakeup.
		2h	Clock source2 is the source for HCLK, VCLK, VCLK2 on wakeup.
		3h	Clock source3 is the source for HCLK, VCLK, VCLK2 on wakeup.
		4h	Clock source4 is the source for HCLK, VCLK, VCLK2 on wakeup.
		5h	Clock source5 is the source for HCLK, VCLK, VCLK2 on wakeup.
		6h	Clock source6 is the source for HCLK, VCLK, VCLK2 on wakeup.
		7h	Clock source7 is the source for HCLK, VCLK, VCLK2 on wakeup.
		8h-Fh	Reserved
15-4	Reserved	0	Reads return 0. Writes have no effect.
3-0	GHVSRC		GCLK1, HCLK, VCLK, VCLK2 current source. **Note: The GHVSRC[3-0] bits are updated with the HVLPM[3-0] setting when GCLK1 is turned off, and are updated with the GHVWAKE[3-0] setting on system wakeup.**
		0	Clock source0 is the source for GCLK1, HCLK, VCLK, VCLK2.
		1h	Clock source1 is the source for GCLK1, HCLK, VCLK, VCLK2.
		2h	Clock source2 is the source for GCLK1, HCLK, VCLK, VCLK2.
		3h	Clock source3 is the source for GCLK1, HCLK, VCLK, VCLK2.
		4h	Clock source4 is the source for GCLK1, HCLK, VCLK, VCLK2.
		5h	Clock source5 is the source for GCLK1, HCLK, VCLK, VCLK2.
		6h	Clock source6 is the source for GCLK1, HCLK, VCLK, VCLK2.
		7h	Clock source7 is the source for GCLK1, HCLK, VCLK, VCLK2.
		8h-Fh	Reserved

Clock source1 is the source for GCLK1, HCLK, VCLK on wakeup. 구동이 된 상황 (클럭을 처음에 제어하는 녀석 클럭소스 1 번)

Clock source1 is the source for HCLK, VCLK, VCLK2 on wakeup.

Clock source1 is the source for GCLK1, HCLK, VCLK on wakeup.

모두다 Clock source1 (pll1) 을 기준으로 동작한다.

위에 모두다 동일한 내용이므로 우리는 0 번 비트만 있어도 된다.

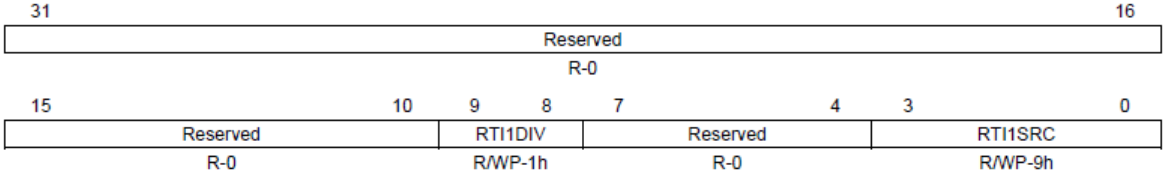
2.5.1.18 RTI Clock Source Register (RCLKSRC)

The RCLKSRC register, shown in Figure 2-25 and described in Table 2-37, controls the RTI (Real Time Interrupt) clock source selection.

NOTE: Important constraint when the RTI clock source is not VCLK

If the RTIx clock source is chosen to be anything other than the default VCLK, then the RTI clock needs to be at least three times slower than the VCLK. This can be achieved by configuring the RTIxCLK divider in this register. This divider is internally bypassed when the RTIx clock source is VCLK.

Figure 2-25. RTI Clock Source Register (RCLKSRC) (offset = 50h)



LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 2-37. RTI Clock Source Register (RCLKSRC) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reads return 0. Writes have no effect.
9-8	RTI1DIV		RTI clock1 Divider.
		0	RTICLK1 divider value is 1.
		1h	RTICLK1 divider value is 2.
		2h	RTICLK1 divider value is 4.
		3h	RTICLK1 divider value is 8.
7-4	Reserved	0	Reads return 0. Writes have no effect.
3-0	RTI1SRC		RTI clock1 source.
		0	Clock source0 is the source for RTICLK1.
		1h	Clock source1 is the source for RTICLK1.
		2h	Clock source2 is the source for RTICLK1.
		3h	Clock source3 is the source for RTICLK1.
		4h	Clock source4 is the source for RTICLK1.
		5h	Clock source5 is the source for RTICLK1.
		6h	Clock source6 is the source for RTICLK1.
		7h	Clock source7 is the source for RTICLK1.
		8h-Fh	VCLK is the source for RTICLK1.

real time interrupt

우리는 인터럽트를 사용 안하기 때문에 솔직히 볼필요 없다.