Video Input Port

This chapter describes the Video Input Port (VIP) module for the device.

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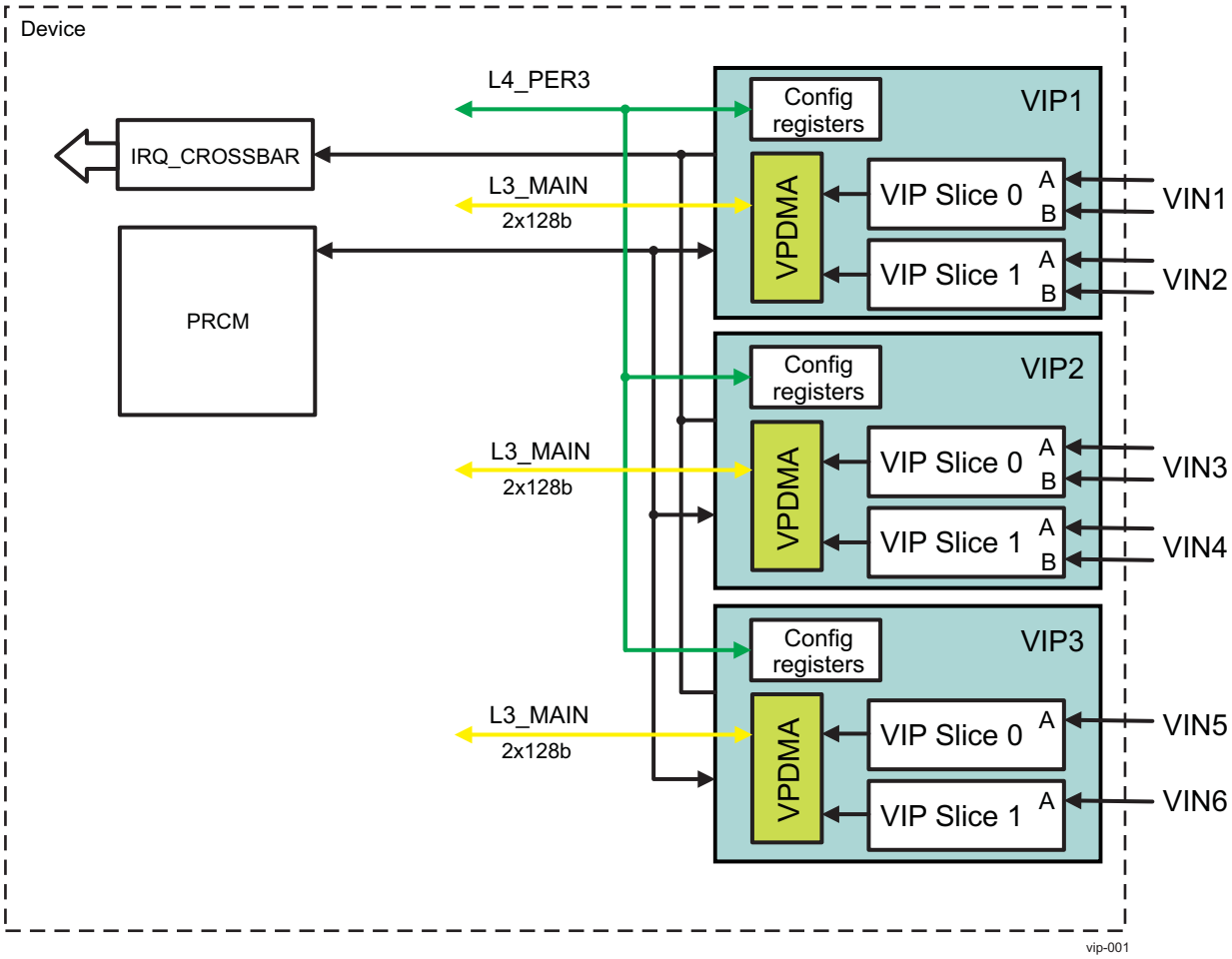
9.1 VIP Overview

The VIP module provides video capture functions for the device. VIP incorporates a multi-channel raw video parser, various video processing blocks, and a flexible Video Port Direct Memory Access (VPDMA) engine to store incoming video in various formats. The device integrates three instantiations of the VIP module giving the ability of capturing up to ten video streams.

Figure 9-1 shows a block diagram with the VIP modules within the device.

Figure 9-1. VIP Overview



A VIP module includes the following main features:

- Two independently configurable external video input capture slices (Slice 0 and Slice 1) each providing up to two video input ports, Port A and Port B:
  - Port A can be configured as a 24/16/8-bit port. Port A of VIP3 slices provides only 16-bit interface.
  - Port B is a fixed 8-bit port. Port B of VIP3 slices is not used.
- Each video Port A can be operated as a port with clock independent input channels (with interleaved or separated Y/C data input). Embedded sync and external sync modes are supported for all input configurations.
- Support for a single external asynchronous pixel clock, up to 165MHz per port.
- Pixel Clock Input Domain Port A supports up to one 24-bit input data bus, including BT.1120 style embedded sync for 16-bit and 24-bit data.
- Embedded Sync data interface mode supports single or multiplexed sources
- Discrete Sync data interface mode supports only single source input
- 24-bit data input plus discrete syncs can be configured to include:

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  - 8-bit YUV422 (Y and U/V time interleaved)
  - 16-bit YUV422 (CbY and CrY time interleaved)
  - 24-bit YUV444
  - 16-bit RGB565
  - 24-bit RGB888
  - 12/16-bit RAW Capture
  - 24-bit RAW capture
- Discrete sync modes include:
  - VSYNC + HSYNC (FID determined by FID signal pin or HSYNC/VSYNC skew)
  - VSYNC + ACTVID + FID
  - VBLANK + ACTVID (ACTVID toggles in VBLANK) + FID
  - VBLANK + ACTVID (no ACTVID toggles in VBLANK) + FID
- Multichannel parser (embedded syncs only):
  - Embedded syncs only
  - Pixel (2x or 4x) or Line multiplexed modes supported
  - Performs demultiplexing and basic error checking
  - Supports maximum of 9 channels in Line Mux (8 normal + 1 split line)
- Ancillary data capture support:
  - For 16-bit or 24-bit input, ancillary data may be extracted from any single channel
  - For 8-bit time interleaved input, ancillary data can be chosen from the Luma channel, the Chroma channel, or both channels
  - Horizontal blanking interval data capture only supported when using discrete syncs (VSYNC + HSYNC or VSYNC + HBLANK)
  - Ancillary data extraction supported on multichannel capture as well as single source streams
- Format conversion and scaling:
  - Programmable color space conversion
  - YUV422 to YUV444 conversion
  - YUV444 to YUV422 conversion
  - YUV422 to YUV420 conversion
  - YUV444 Source: YUV444 to YUV444, YUV444 to RGB888, YUV444 to YUV422, YUV444 to YUV420
  - RGB888 Source: RGB888 to RGB888, RGB888 to YUV444, RGB888 to YUV422, RGB888 to YUV420
  - YUV422 Source: YUV422 to YUV422, YUV422 to YUV420, YUV422 to YUV444, YUV422 to RGB888
  - Supports RAW to RAW (no processing)
  - Scaling and format conversions do not work for multiplexed input
- Supports up to 2047 pixels wide input - when scaling is engaged
- Supports up to 3840 pixels wide input - when only chroma up/down sampling is engaged, without scaling
- Supports up to 4095 pixels wide input - without scaling and chroma up/down sampling
- The maximum supported input resolution is further limited by:
  - Pixel clock and feature-dependent constraints
  - For RGB24-bit format (RAW data), the maximum frame width is limited to 2730 pixels

A VPDMA module includes the following main features:

- VPDMA output buffer size restriction feature, which ensures that writes do not exceed allocated memory buffer size

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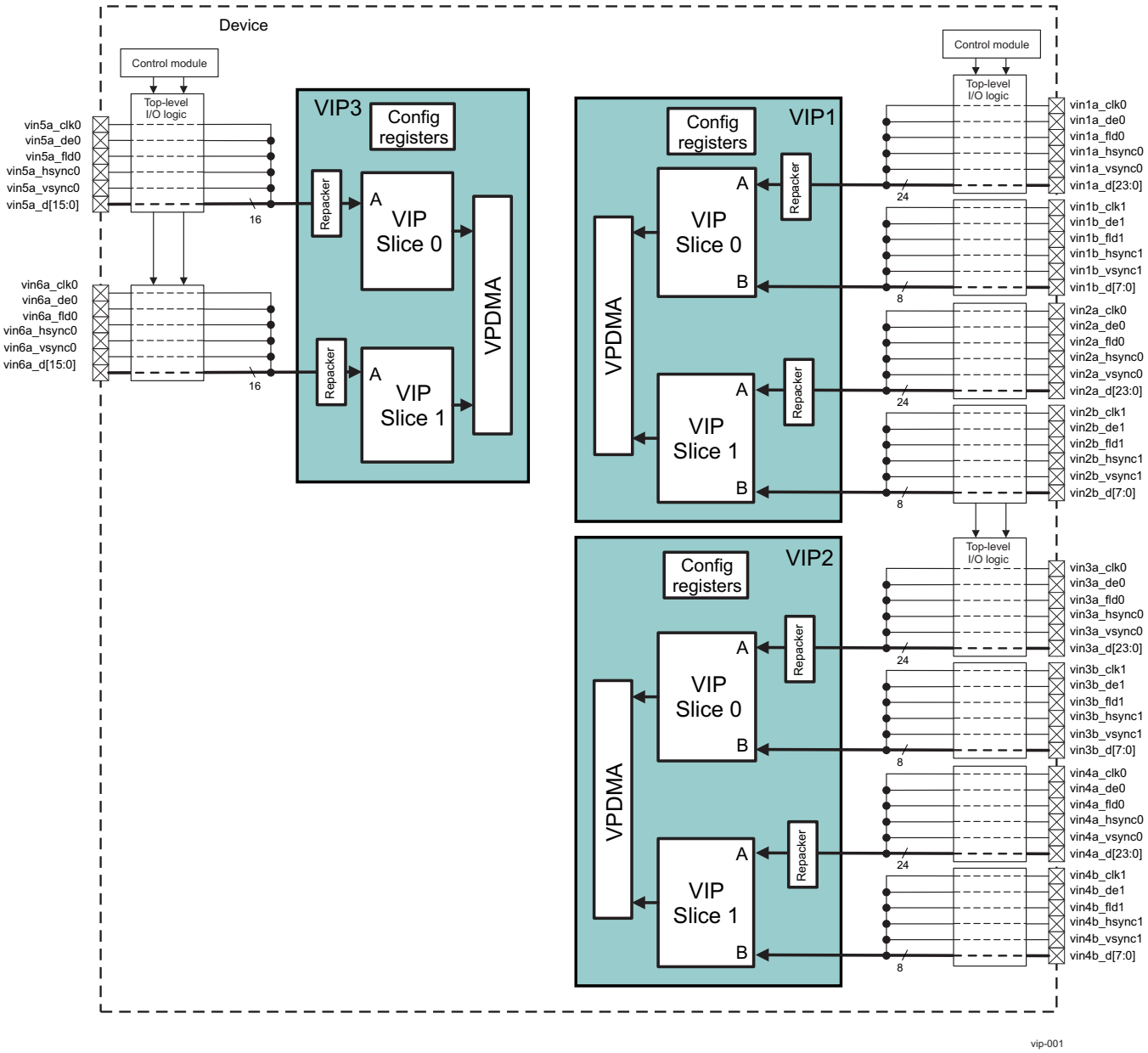
- Support for Tiled (2D) and raster addressing without bandwidth penalty
- Dual clients per channel allows for capture of scaled and nonscaled versions of the data stream (non-multiplexed mode only)
- Start on new frame capability
- Interrupt every X number of frames
- Interrupt every X lines (synced to frame start)
- Dynamic MFLAG generation

9.2 VIP Environment

This section describes the VIP modules from an environment point of view (external connections). It describes the VIP connectivity options and lists all possible interfaces. Figure 9-2 is a block diagram of the VIP environment.

Figure 9-2. VIP Environment



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NOTE: VIP3 does not include port B, and VIP3 Port A can be configured up to 16 bits, for each slice.

Table 9-1. VIP1 Interface Signals

Sub-module Name	Signal Name	Type[1]	Description
Slice 0	vin1a_d[23:0]	I	Pixel data.
Port A	vin1a_clk0	I	Pixel clock.
	vin1a_vsync0	I	Vertical synchronization.
	vin1a_hsync0	I	Horizontal synchronization.
	vin1a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin1a_fld0	I	The FID signal indicates the field identifier for the video input field: • 0 means even. • 1 means odd.
Slice 0	vin1b_d[7:0]	I	Pixel data.
Port B	vin1b_clk1	I	Pixel clock.
	vin1b_vsync1	I	Vertical synchronization.
	vin1b_hsync1	I	Horizontal synchronization.
	vin1b_de1	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin1b_fld1	I	The FID signal indicates the field identifier for the video input field: • 0 means even. • 1 means odd.
Slice 1	vin2a_d[23:0]	I	Pixel data.
Port A	vin2a_clk0	I	Pixel clock.
	vin2a_vsync0	I	Vertical synchronization.
	vin2a_hsync0	I	Horizontal synchronization.
	vin2a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin2a_fld0	I	The FID signal indicates the field identifier for the video input field: • 0 means even. • 1 means odd.
Slice 1	vin2b_d[7:0]	I	Pixel data.
Port B	vin2b_clk1	I	Pixel clock.
	vin2b_vsync1	I	Vertical synchronization.
	vin2b_hsync1	I	Horizontal synchronization.

(1) I = Input, O = Output, I/O = Input/Output

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Table 9-1. VIP1 Interface Signals (continued)

Sub-module Name	Signal Name	Type[1]	Description
	vin2b_de1	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin2b_fld1	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.

Table 9-2. VIP2 Interface Signals

Sub-module Name	Signal Name	Type[1]	Description
Slice 0	vin3a_d[23:0]	I	Pixel data.
Port A	vin3a_clk0	I	Pixel clock.
	vin3a_vsync0	I	Vertical synchronization.
	vin3a_hsync0	I	Horizontal synchronization.
	vin3a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin3a_fld0	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.
Slice 0	vin3b_d[7:0]	I	Pixel data.
Port B	vin3b_clk1	I	Pixel clock.
	vin3b_vsync1	I	Vertical synchronization.
	vin3b_hsync1	I	Horizontal synchronization.
	vin3b_de1	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin3b_fld1	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.
Slice 1	vin4a_d[23:0]	I	Pixel data
Port A	vin4a_clk0	I	Pixel clock
	vin4a_vsync0	I	Vertical synchronization.
	vin4a_hsync0	I	Horizontal synchronization.
	vin4a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.

(1) I = Input, O = Output, I/O = Input/Output

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Table 9-2. VIP2 Interface Signals (continued)

Sub-module Name	Signal Name	Type[1]	Description
	vin4a_fld0	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.
Slice 1	vin4b_d[7:0]	I	Pixel data.
Port B	vin4b_clk1	I	Pixel clock.
	vin4b_vsync1	I	Vertical synchronization.
	vin4b_hsync1	I	Horizontal synchronization.
	vin4b_de1	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin4b_fld1	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.

Table 9-3. VIP3 Interface Signals

Sub-module Name	Signal Name	Type[1]	Description
Slice 0	vin5a_d[15:0]	I	Pixel data.
Port A	vin5a_clk0	I	Pixel clock.
	vin5a_vsync0	I	Vertical synchronization.
	vin5a_hsync0	I	Horizontal synchronization.
	vin5a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin5a_fld0	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.
Slice 1	vin6a_d[15:0]	I	Pixel data.
Port A	vin6a_clk0	I	Pixel clock.
	vin6a_vsync0	I	Vertical synchronization.
	vin6a_hsync0	I	Horizontal synchronization.
	vin6a_de0	I	The DE signal acts as an Input-enable signal to indicate when data must be latched using the input clock. DE is also referred to as ACTVID throughout the VIP chapter. Both of these terms, ACTVID and DE, are the same and used interchangeably.
	vin6a_fld0	I	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.

(1) I = Input, O = Output, I/O = Input/Output

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Table 9-4 and Table 9-5 summarize the mapping of RGB and YUV color components to VIP input data signals, with corresponding settings of VIP_MAIN[1:0] DATA_INTERFACE_MODE register bit-field.

Table 9-4. VIP Port A Input Data Signals to RGB and YUV Color Components Mapping

VIP Modules	VIP Port A Data Signals	24-bit RGB888 Input Mode	16-bit RGB565 Input Mode	24-bit YUV444 Input Mode	16-bit YUV422 Input Mode (1)	8-bit YUV422 Input Mode (2)
		DATA_INTERFACE_MODE = 00b	DATA_INTERFACE_MODE = 00b	DATA_INTERFACE_MODE = 00b	DATA_INTERFACE_MODE = 01b	DATA_INTERFACE_MODE = 10b
VIP1 and VIP2 only	vinXa_d23	Red 7 (MS bit)	Red 4 (MS bit)	Y7 (MS bit)	-	-
X = 1 to 4	vinXa_d22	Red 6	Red 3	Y6	-	-
	vinXa_d21	Red 5	Red 2	Y5	-	-
	vinXa_d20	Red 4	Red 1	Y4	-	-
	vinXa_d19	Red 3	Red 0	Y3	-	-
	vinXa_d18	Red 2	-	Y2	-	-
	vinXa_d17	Red 1	-	Y1	-	-
	vinXa_d16	Red 0	-	Y0	-	-
VIP1 to VIP3	vinXa_d15	Green 7	Green 5	Cb7	Y7 (MS bit)	-
X = 1 to 6	vinXa_d14	Green 6	Green 4	Cb6	Y6	-
	vinXa_d13	Green 5	Green 3	Cb5	Y5	-
	vinXa_d12	Green 4	Green 2	Cb4	Y4	-
	vinXa_d11	Green 3	Green 1	Cb3	Y3	-
	vinXa_d10	Green 2	Green 0	Cb2	Y2	-
	vinXa_d9	Green 1	-	Cb1	Y1	-
	vinXa_d8	Green 0	-	Cb0	Y0	-
	vinXa_d7	Blue 7	Blue 4	Cr7	Cb7/Cr7/...	Cb7/Y7/Cr7/... (MS bit)
	vinXa_d6	Blue 6	Blue 3	Cr6	Cb6/Cr6/...	Cb6/Y6/Cr6/...
	vinXa_d5	Blue 5	Blue 2	Cr5	Cb5/Cr5/...	Cb5/Y5/Cr5/...
	vinXa_d4	Blue 4	Blue 1	Cr4	Cb4/Cr4/...	Cb4/Y4/Cr4/...
	vinXa_d3	Blue 3	Blue 0 (LS bit)	Cr3	Cb3/Cr3/...	Cb3/Y3/Cr3/...
	vinXa_d2	Blue 2	-	Cr2	Cb2/Cr2/...	Cb2/Y2/Cr2/...
	vinXa_d1	Blue 1	-	Cr1	Cb1/Cr1/...	Cb1/Y1/Cr1/...
	vinXa_d0	Blue 0 (LS bit)	-	Cr0 (LS bit)	Cb0/Cr0/... (LS bit)	Cb0/Y0/Cr0/... (LS bit)

(1) Chroma is time division multiplexed (interleaved). For more details, see Section 9.4.5.6.2, *16b Interface Mode*.
(2) Luma and Chroma are time division multiplexed (interleaved). For more details, see Section 9.4.5.6.1, *8b Interface Mode*.

NOTE: 16-bit RGB data can be captured also on the vinXa_d[15:0] input data bus of Port A. In this case, the 16-bit RGB data captured by the VIP_PARSER will be passed to VPDMA, as if it is a 16-bit YUV data. The VIP_MAIN[1:0] DATA_INTERFACE_MODE register bit-field must be configured for a 16-bit input mode. The VPDMA will then directly store this data in memory as a 16-bit data, provided that any 16-bit data type in the VPDMA outbound descriptor is set.

Table 9-5. VIP Port B Input Data Signals to YUV Color Components Mapping

VIP Modules	VIP Port B Data Signals	8-bit YUV422 Input Mode (1)
		DATA_INTERFACE_MODE = 10b
VIP1 and VIP2 only	vinYb_d7	Cb7/Y7/Cr7/... (MS bit)
Y = 1 to 4	vinYb_d6	Cb6/Y6/Cr6/...
	vinYb_d5	Cb5/Y5/Cr5/...

(1) Luma and Chroma are time division multiplexed (interleaved). For more details, see Section 9.4.5.6.1, *8b Interface Mode*.

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Table 9-5. VIP Port B Input Data Signals to YUV Color Components Mapping (continued)

VIP Modules	VIP Port B Data Signals	8-bit YUV422 Input Mode (1)
	vinYb_d4	Cb4/Y4/Cr4/...
	vinYb_d3	Cb3/Y3/Cr3/...
	vinYb_d2	Cb2/Y2/Cr2/...
	vinYb_d1	Cb1/Y1/Cr1/...
	vinYb_d0	Cb0/Y0/Cr0/... (LS bit)

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9.3 VIP Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests. Figure 9-3summarizes the integration of the module in the device.

Figure 9-3. VIP Integration

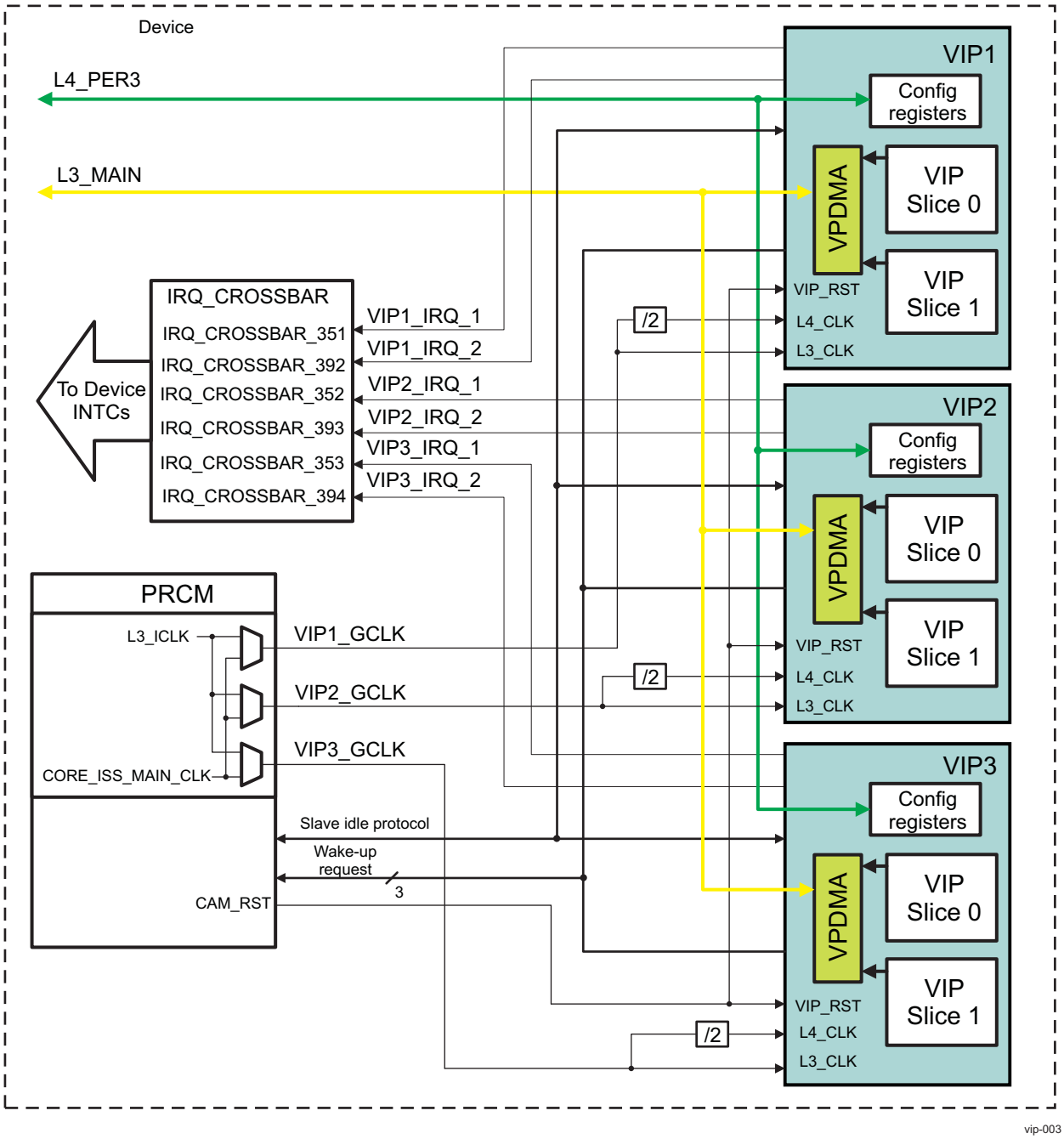

Table 9-6 and Table 9-7 list the integration attributes and clock and resets, respectively.

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Table 9-6. VIP Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
VIP1 VIP2 VIP3	PD_CAM	L4_PER3 for configuration L3_MAIN for data (through VPDMA module)

Table 9-7. VIP Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
VIP1	L3_CLK PROC_CLK	VIP1_GCLK	PRCM	L3_CLK is the clock used to drive and receive data over the bus to L3_MAIN. The VIP subsystem uses this clock to fetch external data and transfer this data to internal processing PROC_CLK is the clock used to drive data processing within the VIP subsystem.
	L4_CLK	VIP1_GCLK/2	PRCM	L4_CLK is the interface clock for Memory Mapped Registers (MMR) configuration bus
VIP2	L3_CLK PROC_CLK	VIP2_GCLK	PRCM	L3_CLK is the clock used to drive and receive data over the bus to L3_MAIN. The VIP subsystem uses this clock to fetch external data and transfer this data to internal processing PROC_CLK is the clock used to drive data processing within the VIP subsystem.
	L4_CLK	VIP2_GCLK/2	PRCM	L4_CLK is the interface clock for Memory Mapped Registers (MMR) configuration bus
VIP3	L3_CLK PROC_CLK	VIP3_GCLK	PRCM	L3_CLK is the clock used to drive and receive data over the bus to L3_MAIN. The VIP subsystem uses this clock to fetch external data and transfer this data to internal processing PROC_CLK is the clock used to drive data processing within the VIP subsystem.
	L4_CLK	VIP3_GCLK/2	PRCM	L4_CLK is the interface clock for Memory Mapped Registers (MMR) configuration bus
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
VIP1	VIP_RST	CAM_RST	PRCM	VIP1 Reset
VIP2	VIP_RST	CAM_RST	PRCM	VIP2 Reset
VIP3	VIP_RST	CAM_RST	PRCM	VIP3 Reset

Table 9-8. VIP Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination IRQ_CROSSBAR Input**	**Default Mapping**	**Description**

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Table 9-8. VIP Hardware Requests (continued)

VIP1	VIP1_IRQ1	IRQ_CROSSBAR_351	N/A	VIP1 interrupt requests. These IRQ source signals are not mapped by default to any device INTC.
	VIP1_IRQ2	IRQ_CROSSBAR_392	N/A	
VIP2	VIP2_IRQ1	IRQ_CROSSBAR_352	N/A	VIP2 interrupt requests. These IRQ source signals are not mapped by default to any device INTC.
	VIP2_IRQ2	IRQ_CROSSBAR_393	N/A	
VIP3	VIP3_IRQ1	IRQ_CROSSBAR_353	N/A	VIP3 interrupt requests. These IRQ source signals are not mapped by default to any device INTC.
	VIP3_IRQ2	IRQ_CROSSBAR_394	N/A	

NOTE: The "**Default Mapping**" column in Table 9-8 *VIP Hardware Requests* shows the default mapping of module IRQ source signals. These module IRQ source signals can also be mapped to other lines of each device Interrupt controller through the IRQ_CROSSBAR module, respectively.
For more information about the IRQ_CROSSBAR module, see Section 18.4.6.4, *IRQ_CROSSBAR Module Functional Description*, in Chapter 18, *Control Module*.
For more information about the device interrupt controllers, see Chapter 17, *Interrupt Controllers*.

9.4 VIP Functional Description

9.4.1 VIP Block Diagram

Figure 9-4 shows the internal structure of a single VIP module in the device.

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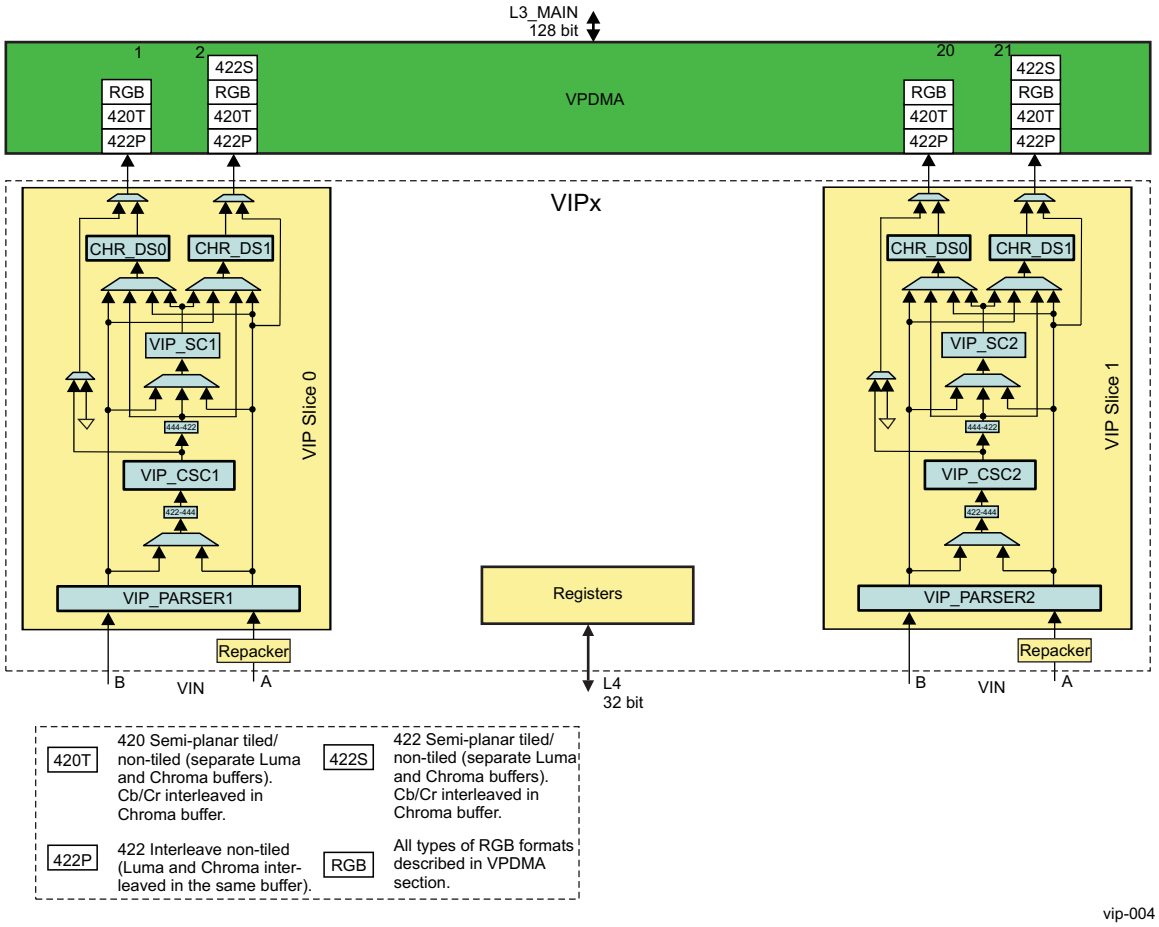
Figure 9-4. VIP Block Diagram



9.4.2 VIP Software Reset

Software reset in the VIP module can be done by setting the VIP_CLKC_RST[16] VIP1_DP_RST for Slice 0, VIP_CLKC_RST[17] VIP2_DP_RST for Slice 1, VIP_CLKC_RST[0] VPDMA_RST for VIP VPDMA to 0x1. By setting VIP_CLKC_RST[31] MAIN_RST reset is performed for all modules within the instance. Software must ensure that the software reset completes before performing operations within the VIP module.

9.4.3 VIP Power and Clocks Management

The VIP modules support the MStandby/Wait and IdleReq/SidleAck protocols as defined in Chapter 3, *Power, Reset, and Clock Management.*

Power Management within the VIP module can be accomplished in several ways:

- L4 MConnect/SConnect can disable the internal L4 clock network
- L3 MConnect/Sconnect can disable the internal L3 clock network

These items are accomplished using the standard slave idle (for L4) and master standby (for L3) protocols. When these modules are instructed to disable clocks for the internal L3 or L4 (MMR) clock domains, the internal clock networks will be shut down. This shut down applies to the clock signals - L3_CLK and L4_CLK.

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9.4.3.1 VIP Clocks

The VIP internal clock domains can only be shut down by writing the appropriate register bit within the Clock Enable register - VIP_CLKC_CLKEN[16] VIP1_DP_EN for slice0, VIP_CLKC_CLKEN[17] VIP2_DP_EN for slice1 and VIP_CLKC_CLKEN[0] VPDMA_EN for the VPDMA engine

9.4.3.2 VIP Idle Mode

The VIP supports no-idle mode, force-idle mode, and smart-idle mode. The mode can be selected byprogramming the appropriate value in the VIP_SYSCONFIG[3:2] IDLEMODE bit field.

Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state.

- Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements.
- No-idle mode: local target never enters idle state.
- Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA related requests) wakeup events

9.4.3.3 VIP StandBy Mode

The VIP supports no-standby mode and force-standby mode. The mode is set in the VIP_SYSCONFIG[5:4] STANDBYMODE bit field.

Configuration of the local initiator state management mode:

- Force-standby mode: local initiator is unconditionally placed in standby state.
- No-standby mode: local initiator is unconditionally placed out of standby state.

9.4.4 VIP Slice

9.4.4.1 VIP Slice Processing Path Overview

Figure 9-5 shows in details the internal processing path and output signals to VPDMA for a single VIP Slice. External video source drives the input side of the VIP Slice. Port A[x:y] can be in YUV422 format (A[15:0] in the diagram) or RGB/YUV444 format (A[23:0] in the diagram), depending on the external video input source and configuration options within the VIP_PARSER. Port B[x:y] can be in YUV422 format (B[15:0] in the diagram). When the VIP_PARSER is configured to capture 24bit RGB/444 data, A[23:0] is used and the data path inside VIP must be configured correctly for it. Multiplexer selections and controls shown in Figure 9-5 are described in register VIP_CLKC_VIP0DPS for Slice 0, and register VIP_CLKC_VIP1DPS for Slice 1. The outputs of each VIP Slice drive the VPDMA module, which sends the resulting data to DDR memory.

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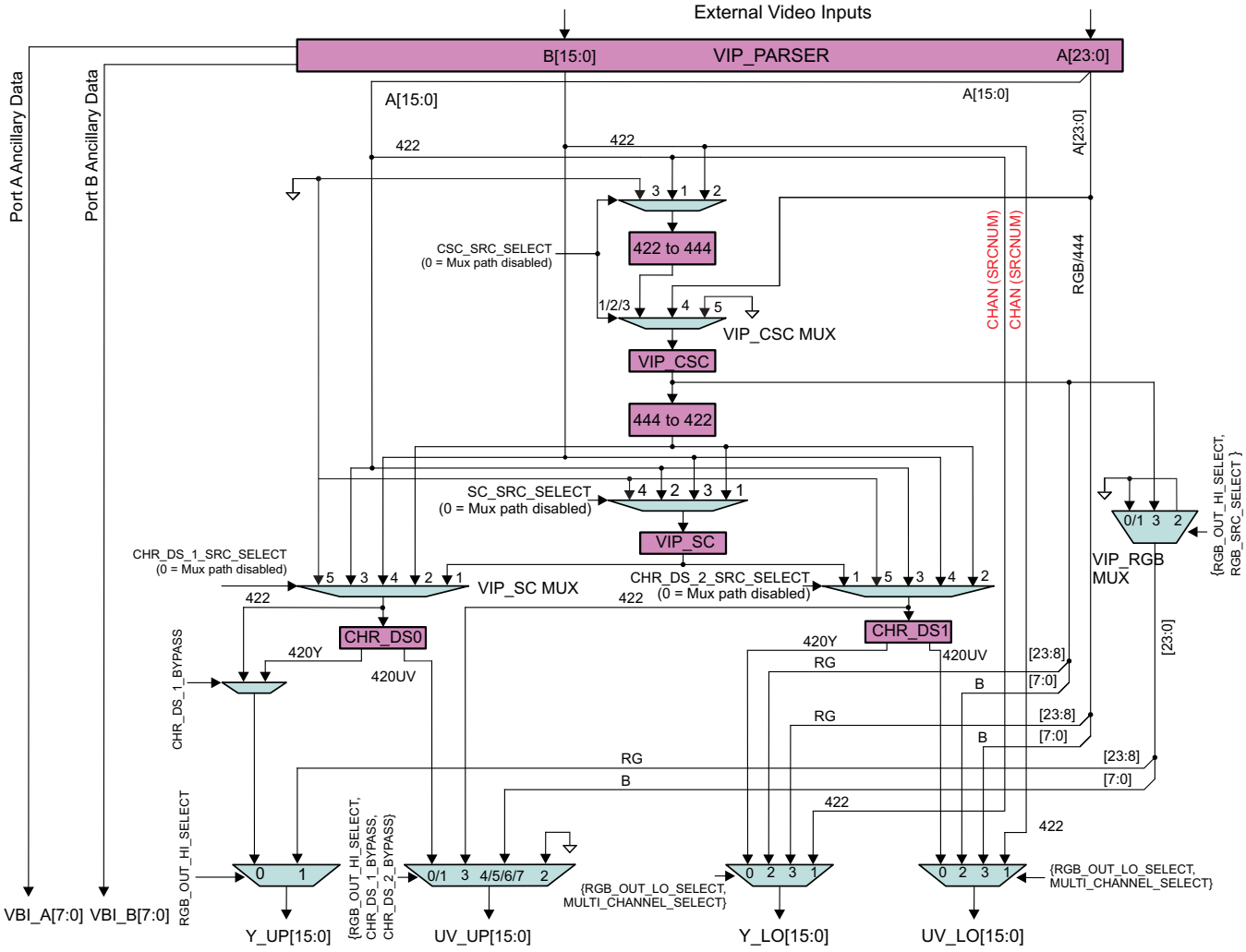
Figure 9-5. VIP Slice Detailed Block Diagram



NOTE: Port A of VIP3 module supports up to 16-bit data, and Port B is not used (this applies to both Slice 0 and Slice 1 of VIP3).

Table 9-9. Register Call Summary Table for Figure 9-5

Multiplexer Control	Register Bit-fields for Slice 0	Register Bit-fields for Slice 1	Description
CSC_SRC_SELECT	VIP_CLKC_VIP0DPS[2:0] VIP1_CSC_SRC_SELECT	VIP_CLKC_VIP1DPS[2:0] VIP2_CSC_SRC_SELECT	VIP CSC Source Selection MUX
SC_SRC_SELECT	VIP_CLKC_VIP0DPS [5:3] VIP1_SC_SRC_SELECT	VIP_CLKC_VIP1DPS [5:3] VIP2_SC_SRC_SELECT	VIP SC_M Source Selection MUX
CHR_DS_1_SRC_SELECT	VIP_CLKC_VIP0DPS[11:9] VIP1_CHR_DS_1_SRC_SELECT	VIP_CLKC_VIP1DPS[11:9] VIP2_CHR_DS_1_SRC_SELECT	VIP Chroma Downsampler 1 Source Selection MUX
CHR_DS_1_BYPASS	VIP_CLKC_VIP0DPS[16] VIP1_CHR_DS_1_BYPASS	VIP_CLKC_VIP1DPS[16] VIP2_CHR_DS_1_BYPASS	VIP Chroma Downsampler 1 Bypass MUX

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Table 9-9. Register Call Summary Table for Figure 9-5 (continued)

Multiplexer Control	Register Bit-fields for Slice 0	Register Bit-fields for Slice 1	Description
CHR_DS_2_SRC_SELECT	VIP_CLKC_VIP0DPS[14:12] VIP1_CHR_DS_2_SRC_SELECT	VIP_CLKC_VIP1DPS[14:12] VIP2_CHR_DS_2_SRC_SELECT	VIP Chroma Downsampler 2 Source Selection MUX
CHR_DS_2_BYPASS	VIP_CLKC_VIP0DPS[17] VIP1_CHR_DS_2_BYPASS	VIP_CLKC_VIP1DPS[17] VIP2_CHR_DS_2_BYPASS	VIP Chroma Downsampler 1 Bypass MUX
RGB_OUT_HI_SELECT	VIP_CLKC_VIP0DPS[8] VIP1_RGB_OUT_HI_SELECT	VIP_CLKC_VIP1DPS[8] VIP2_RGB_OUT_HI_SELECT	VIP HI RGB Output Selection MUX
RGB_OUT_LO_SELECT	VIP_CLKC_VIP0DPS[7] VIP1_RGB_OUT_LO_SELECT	VIP_CLKC_VIP1DPS[7] VIP2_RGB_OUT_LO_SELECT	VIP LO RGB Output Selection MUX
MULTI_CHANNEL_SELECT	VIP_CLKC_VIP0DPS[15] VIP1_MULTI_CHANNEL_SELECT	VIP_CLKC_VIP1DPS[15] VIP2_MULTI_CHANNEL_SELECT	VIP Multi Channel Selection MUX
RGB_SRC_SELECT	VIP_CLKC_VIP0DPS[6] VIP1_RGB_SRC_SELECT	VIP_CLKC_VIP1DPS[6] VIP2_RGB_SRC_SELECT	VIP RGB Output Path Selection MUX

9.4.4.2 VIP Slice Processing Path Multiplexers

9.4.4.2.1 VIP_CSC Multiplexers

The following registers are controling the VIP Color Space Converter (CSC) multiplexers: VIP_CLKC_VIP0DPS[2:0] VIP1_CSC_SRC_SELECT for Slice 0 and VIP_CLKC_VIP1DPS[2:0] VIP2_CSC_SRC_SELECT for Slice 1.

The VIP_CSC block (for each slice within the VIP subsystem) receives data from one the following sources:

- VIP_PARSER Port A Output (422)
- VIP_PARSER Port B Output (422)
- VIP_PARSER Port A Output (RGB)

The default state for this multiplexer is disabled, so there is no VIP_CSC input.

9.4.4.2.2 VIP_SC Multiplexer

The multiplexer for Slice 0 and Slice 1 is controleld by VIP_CLKC_VIP0DPS[5:3] VIP1_SC_SRC_SELECT and VIP_CLKC_VIP1DPS[5:3] VIP2_SC_SRC_SELECT, respectively.

The scaler module (VIP_SC) within the VIP subsystem (for a single slice) receives data from one of the following sources:

- VIP_CSC
- VIP_PARSER Port A Output
- VIP_PARSER Port B Output

The default state for this multiplexer is disabled, so there is no VIP_SC input.

9.4.4.2.3 Output to VPDMA Multiplexers

This section is under development and is included as a placeholder for future updates.

9.4.4.3 VIP Slice Processing Path Examples

The following sections provide VIP Slice data path examples for different types of input data, and describe the corresponding multiplexer configurations.

In the block diagrams of the following sections, Output A refers to _LO[15:0] outputs, an Output B refers to _UP[15:0] outputs.

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9.4.4.3.1 Input: A:RGB, B:YUV422; Output: A:RGB, B:RGB

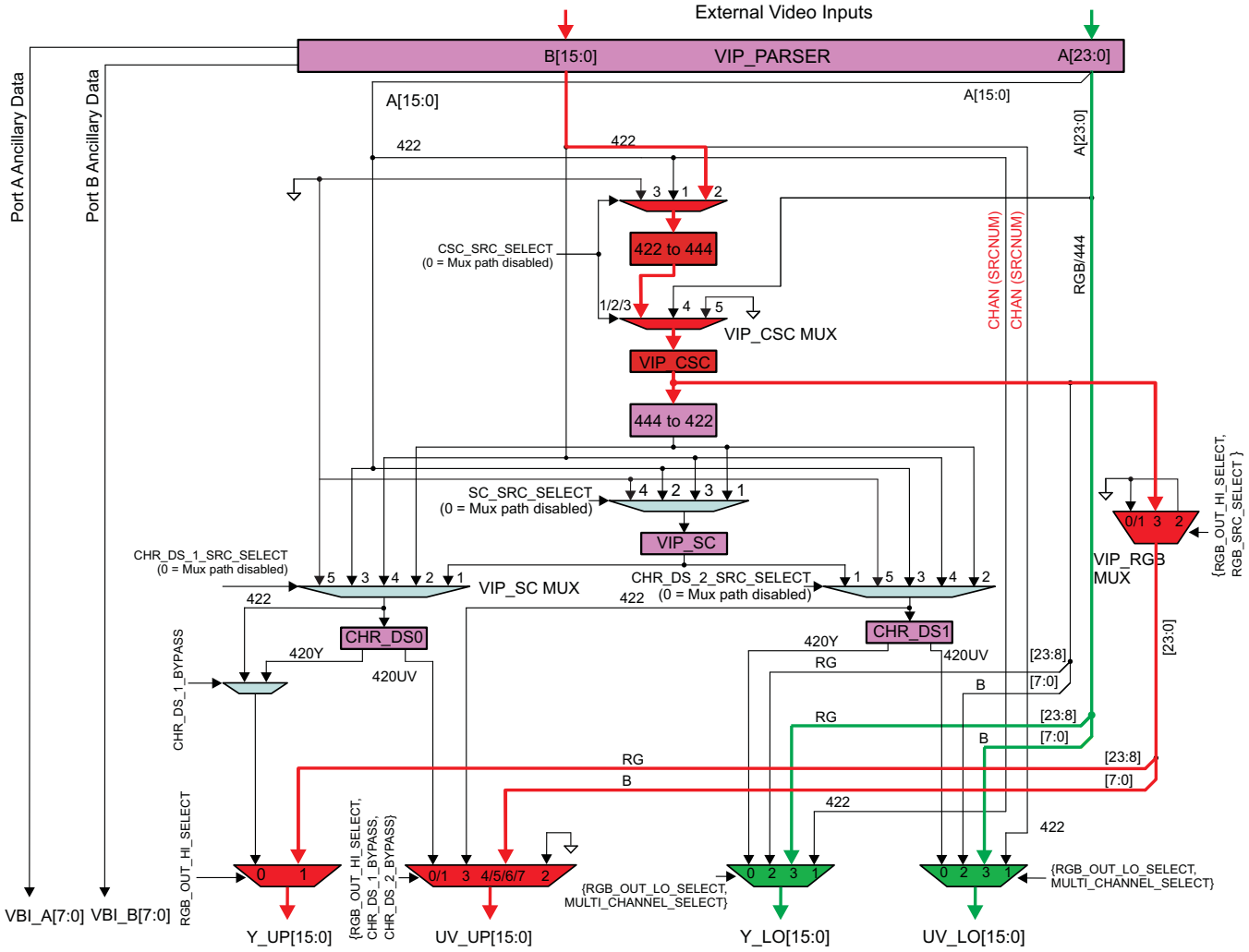
Tested in single channel embedded and discrete mode.

Input: A:RGB, B:YUV422; Output: A:RGB, B:RGB

Multiplexers Settings:

- VIPx_CSC_SRC_SELECT = 2
- VIPx_SC_SRC_SELECT = 0
- VIPx_CHR_DS_1_SRC_SELECT = 0
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 0
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 1
- VIPx_RGB_OUT_LO_SELECT = 1
- VIPx_MULTI_CHANNEL_SELECT = 1

Figure 9-6. Input: A:RGB, B:YUV422; Output: A:RGB, B:RGB



9.4.4.3.2 Input: A:YUV422 8/16, B:YUV422; Output: A:Scaled YUV420, B: RGB

Tested in single channel embedded and discrete mode.

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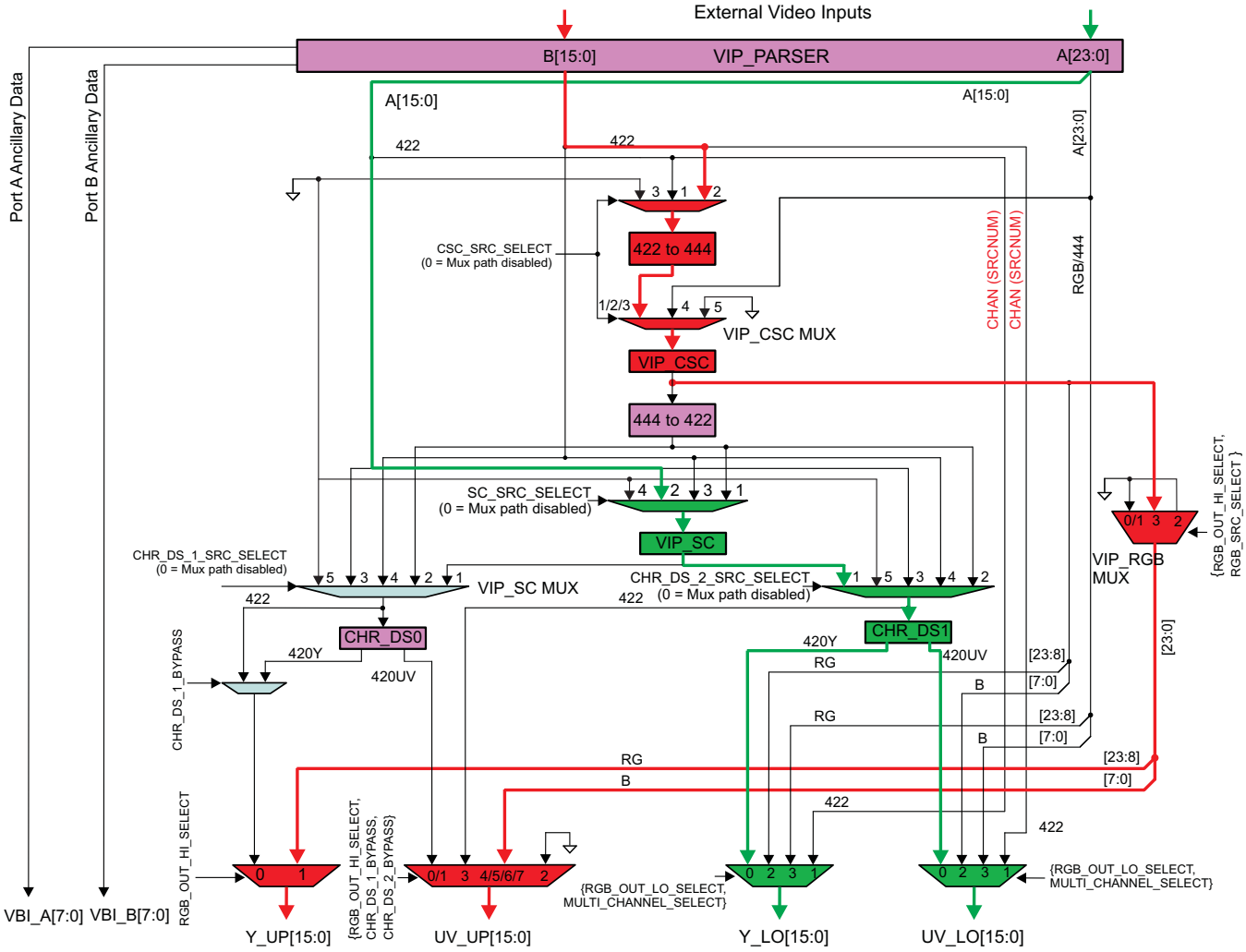
Mux Settings:

- VIPx_CSC_SRC_SELECT = 2
- VIPx_SC_SRC_SELECT = 2
- VIPx_CHR_DS_1_SRC_SELECT = 0
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 1
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

Figure 9-7. Input: A:YUV422 8/16, B:YUV422; Output: A:Scaled YUV420, B: RGB



9.4.4.3.3 *Input: A:RGB, B:YUV422; Output: A:RGB, B:Scaled YUV420*

Tested in single channel embedded and discrete mode and multi-channel mode.

Multiplexers Settings:

- VIPx_CSC_SRC_SELECT = 4
- VIPx_SC_SRC_SELECT = 1

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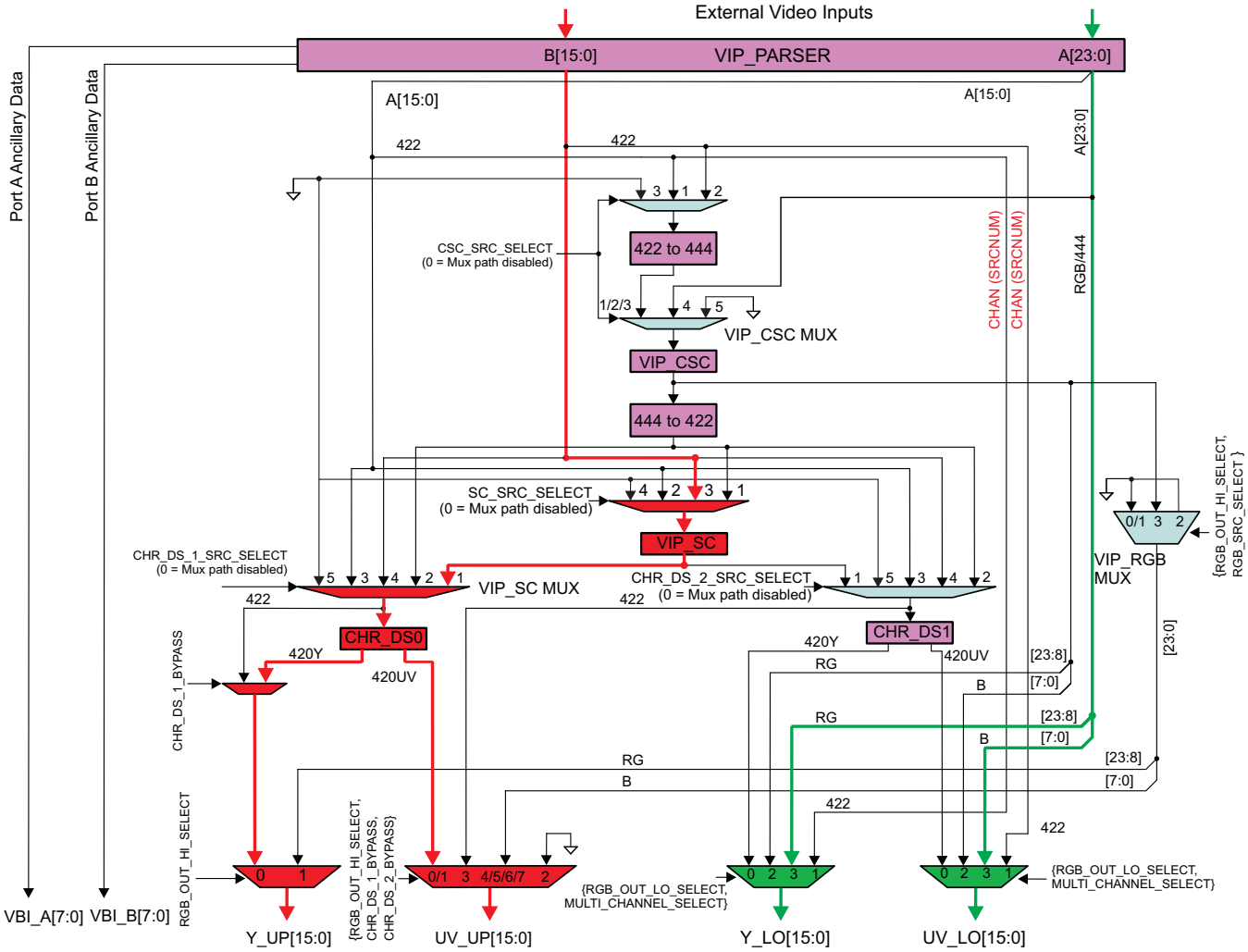
- VIPx_CHR_DS_1_SRC_SELECT = 2
- VIPx_CHR_DS_1_BYPASS = 1
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 1
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 0
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 1

Figure 9-8. Input: A:RGB, B:YUV422; Output: A:RGB, B:Scaled YUV420



9.4.4.3.4 Input: A:YUV444, B:YUV422; Output: A: YUV422, B:YUV422, B: Scaled YUV422

Tested in single channel embedded and discrete mode.

Multiplexer Settings:

- VIPx_CSC_SRC_SELECT = 4
- VIPx_SC_SRC_SELECT = 1
- VIPx_CHR_DS_1_SRC_SELECT = 2
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1

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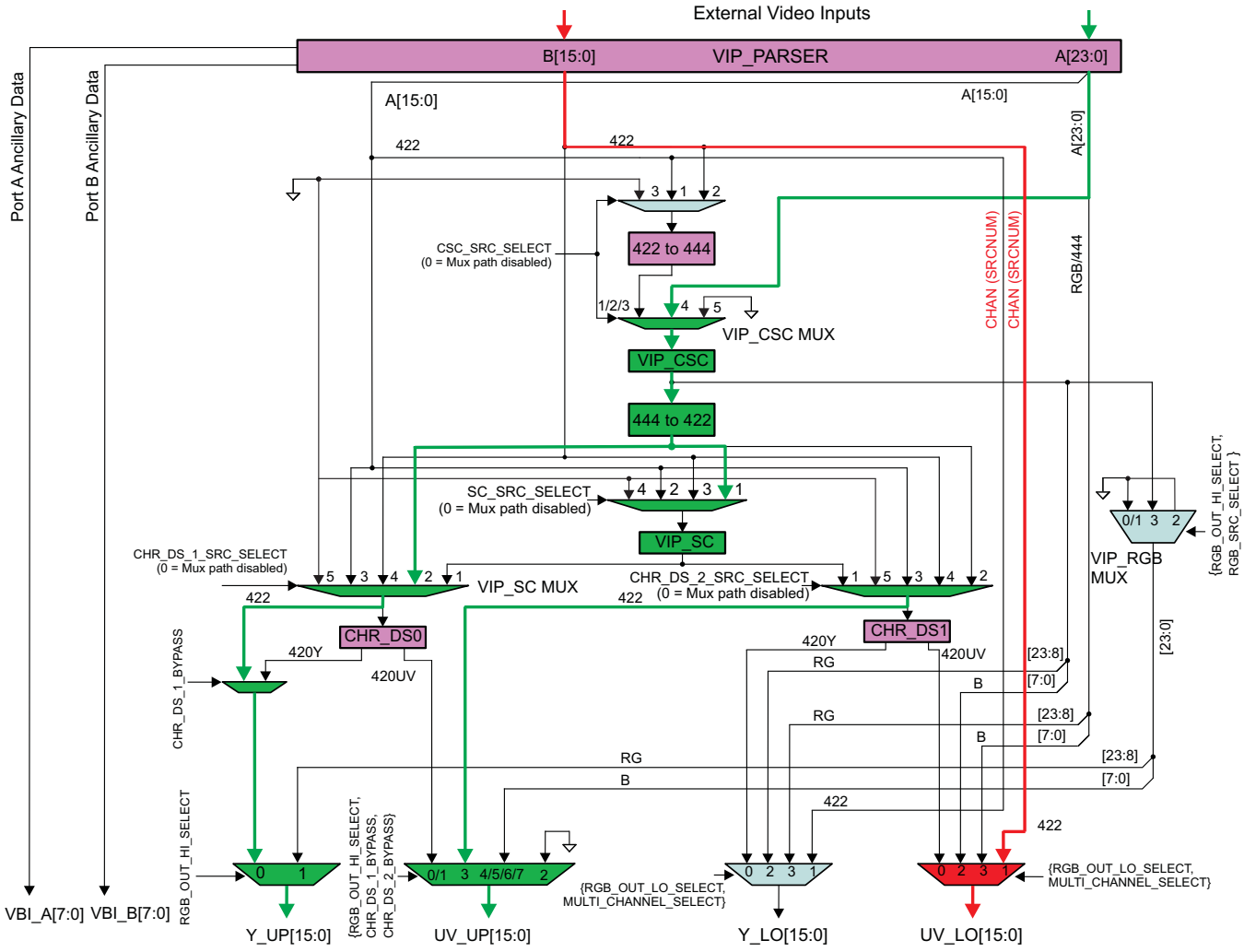
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 0
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

Figure 9-9. Input: A:YUV444, B:YUV422; Output: A: YUV422, B:YUV422, B: Scaled YUV422



9.4.4.3.5 *Input: A:YUV444; Output: A:Scaled YUV420, B:YUV420*

Tested in single channel embedded and discrete mode.

Multiplexer Settings:

- VIPx_CSC_SRC_SELECT = 4
- VIPx_SC_SRC_SELECT = 1
- VIPx_CHR_DS_1_SRC_SELECT = 2
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 0

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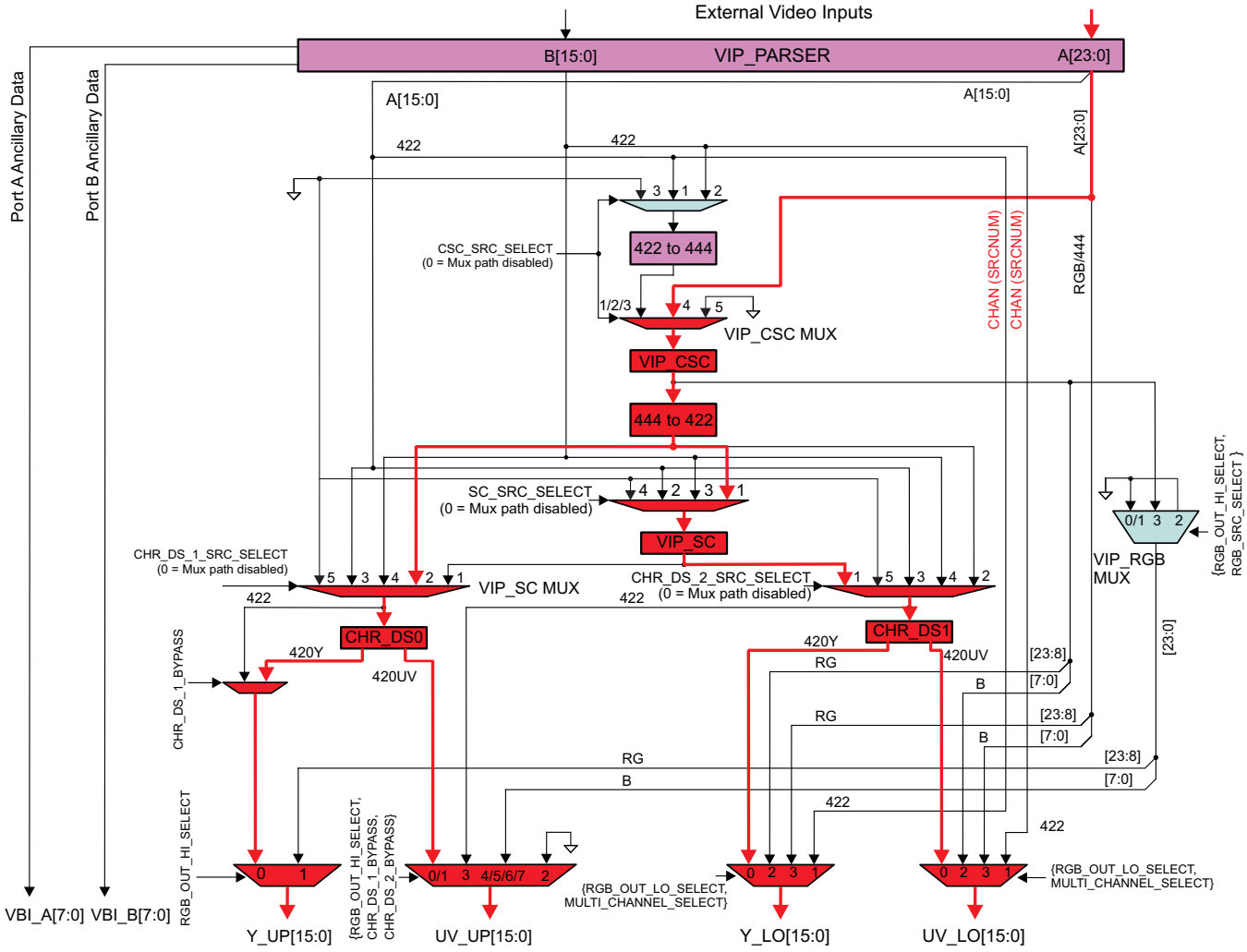
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

Figure 9-10. Input: A:YUV444; Output: A:Scaled YUV420, B:YUV420



9.4.4.3.6 Input: A:YUV444; Output: A: Scaled YUV420, B:YUV444

Tested in single channel embedded and discrete mode.

Multiplexer Settings:

- VIPx_CSC_SRC_SELECT = 4
- VIPx_SC_SRC_SELECT = 1
- VIPx_CHR_DS_1_SRC_SELECT = 0
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 1
- VIPx_RGB_OUT_HI_SELECT = 1
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

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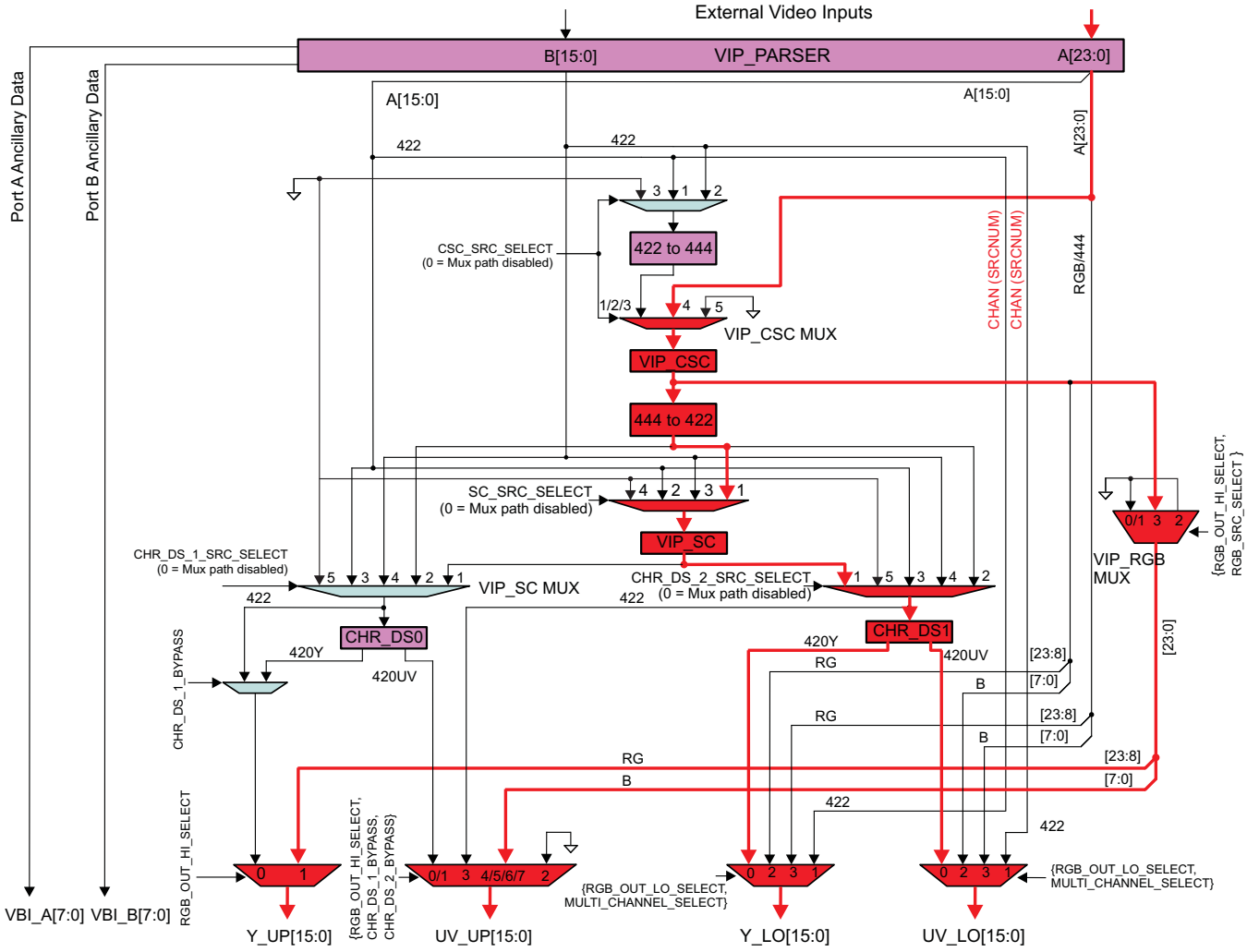
Figure 9-11. Input: A:YUV444; Output: A: Scaled YUV420, B:YUV444



9.4.4.3.7 Input: A: YUV422 8/16; Output A:Scaled YUV420, B:Scaled YUV444

Tested in single channel embedded and discrete mode.

Multiplexer Settings:

- VIPx_CSC_SRC_SELECT = 1
- VIPx_SC_SRC_SELECT = 1
- VIPx_CHR_DS_1_SRC_SELECT = 0
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 1
- VIPx_RGB_OUT_HI_SELECT = 1
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

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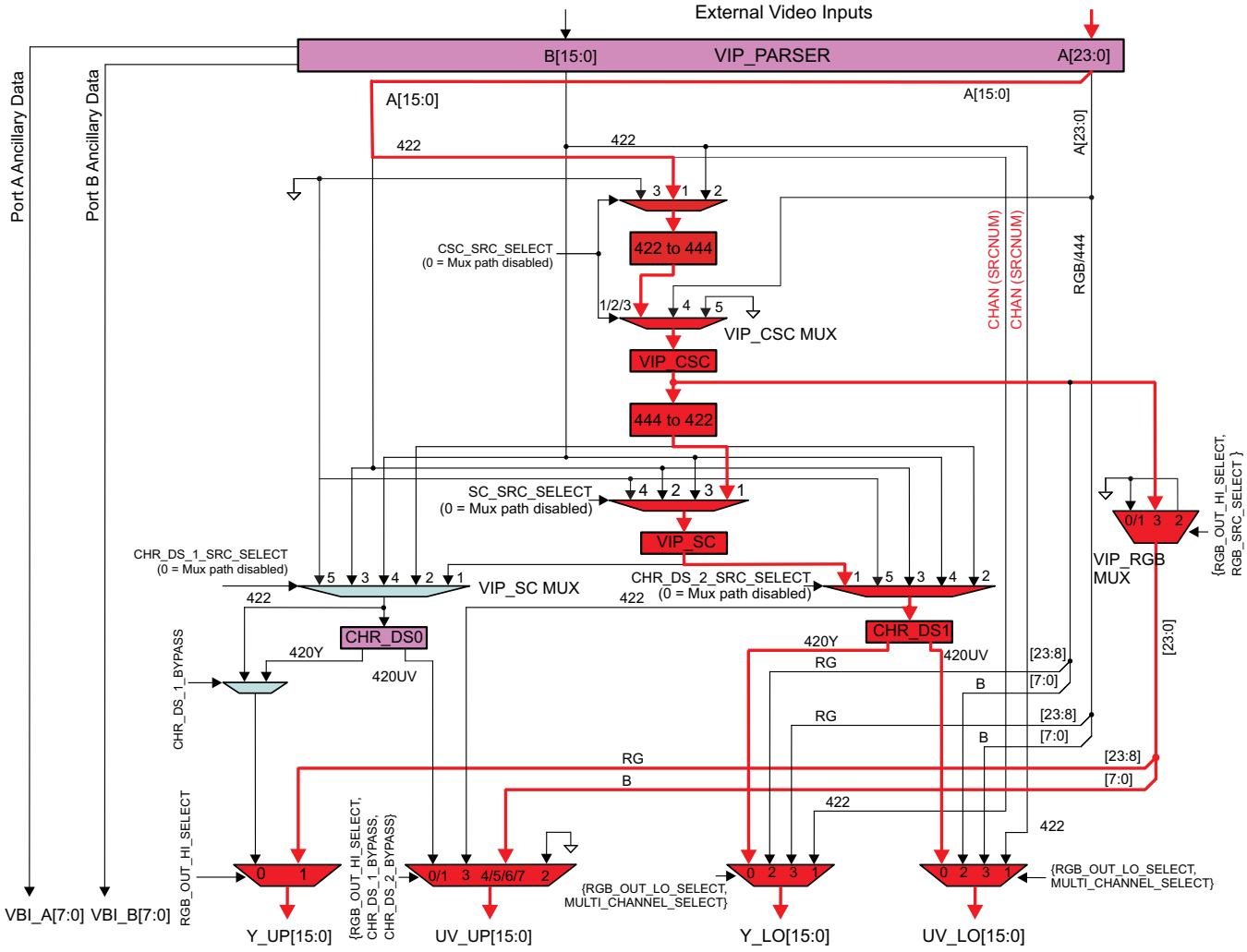
Figure 9-12. Input: A: YUV422 8/16; Output A:Scaled YUV420, B:Scaled YUV444



9.4.4.3.8 Input: A:YUV422 8/16, B:YUV422; Output: A: Scaled YUV420, B:YUV420

Tested in single channel embedded and discrete mode.

Multiplexer settings:

- VIPx_CSC_SRC_SELECT = 0
- VIPx_SC_SRC_SELECT = 2
- VIPx_CHR_DS_1_SRC_SELECT = 4
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 1
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 0
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

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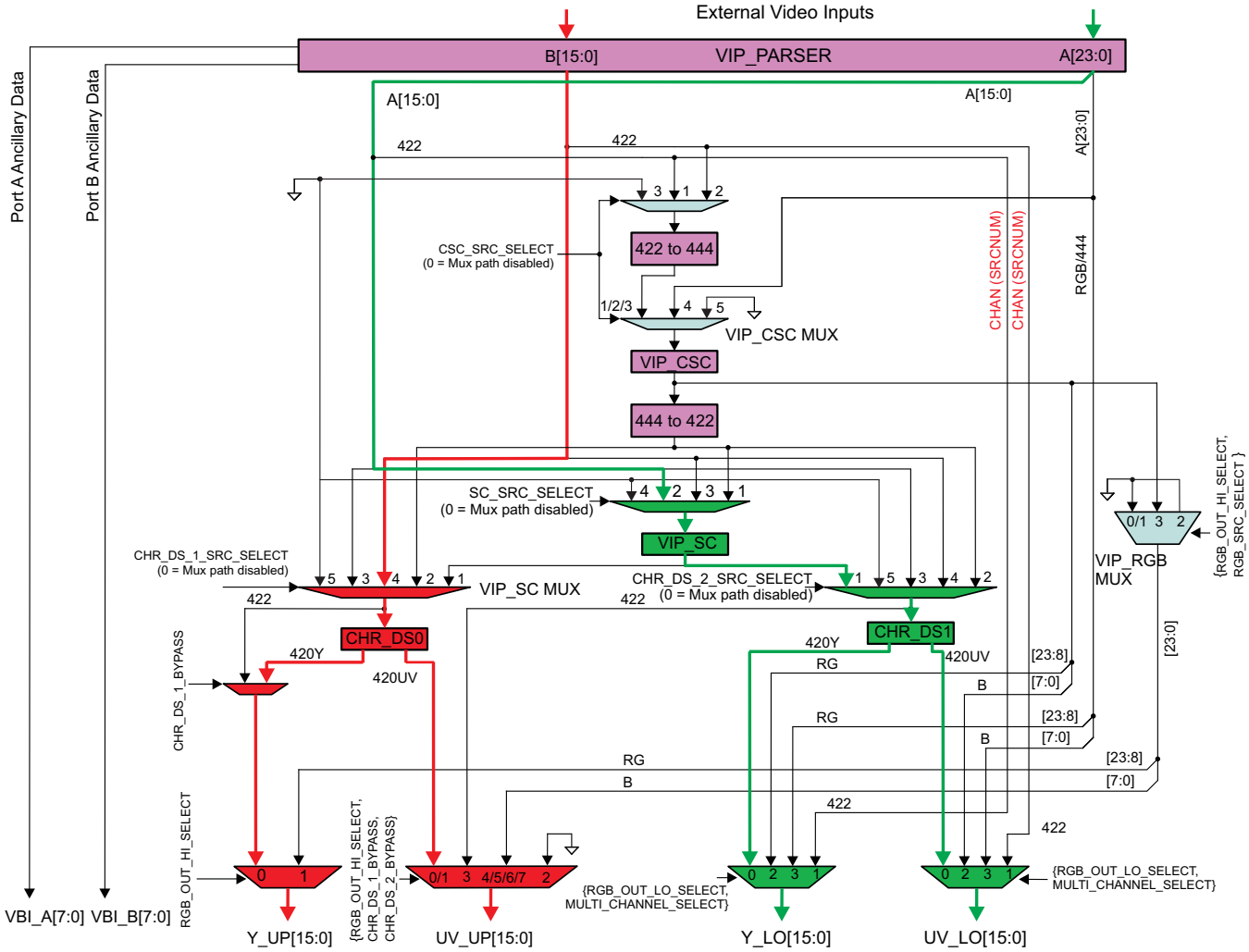
Figure 9-13. Input: A:YUV422 8/16, B:YUV422; Output: A: Scaled YUV420, B:YUV420



9.4.4.3.9 Input : A: YUV422 8/16, B: YUV422; Output: A: YUV420, B: YUV420

Tested in single channel embedded and discrete mode.

Multiplexer settings:

- VIPx_CSC_SRC_SELECT = 0
- VIPx_SC_SRC_SELECT = 0
- VIPx_CHR_DS_1_SRC_SELECT = 4
- VIPx_CHR_DS_1_BYPASS = 0
- VIPx_CHR_DS_2_SRC_SELECT = 3
- VIPx_CHR_DS_2_BYPASS = 0
- VIPx_RGB_SRC_SELECT = 0
- VIPx_RGB_OUT_HI_SELECT = 0
- VIPx_RGB_OUT_LO_SELECT = 0
- VIPx_MULTI_CHANNEL_SELECT = 0

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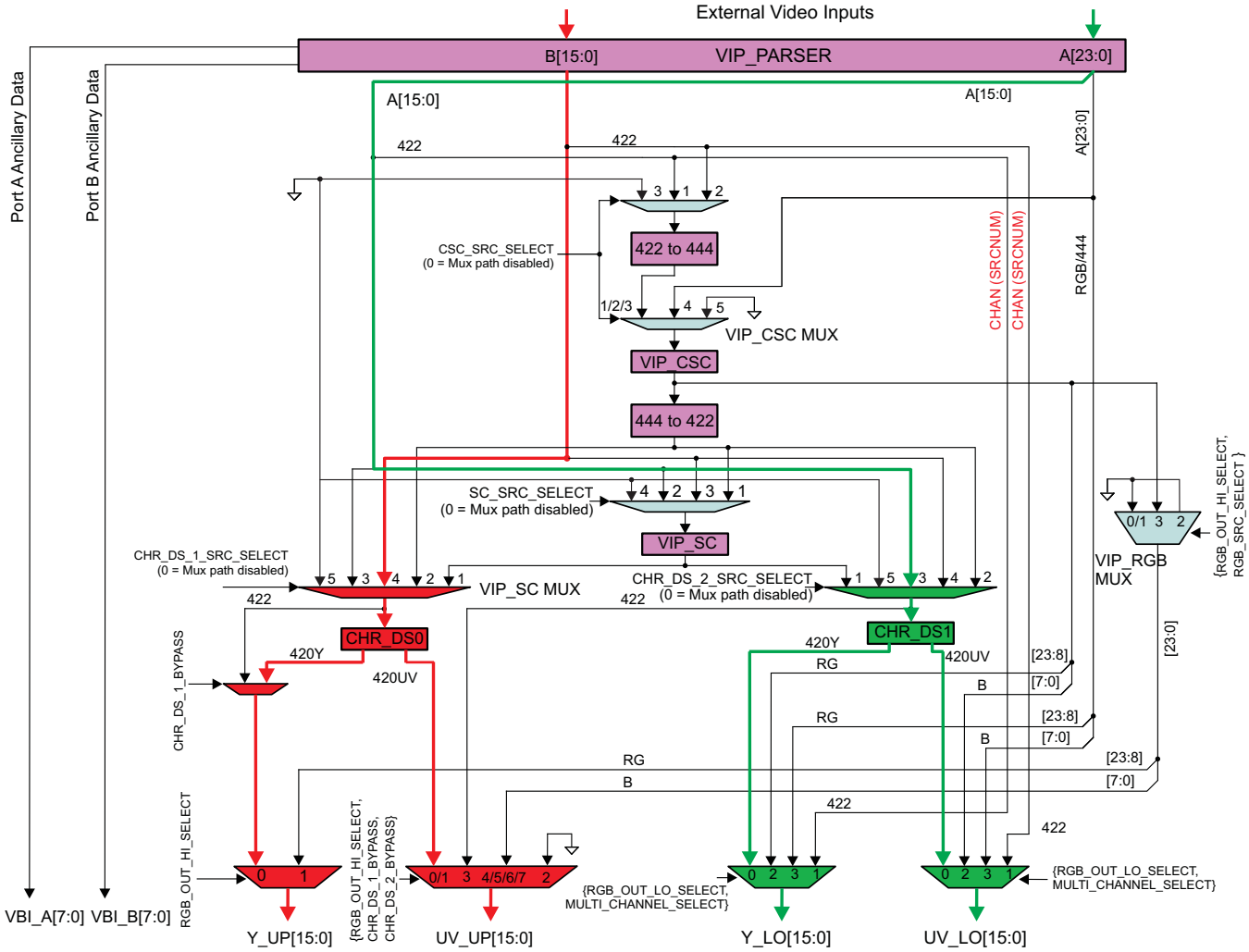
Figure 9-14. Input : A: YUV422 8/16, B: YUV422; Output: A: YUV420, B: YUV420



9.4.5 VIP Parser

The VIP Parser (VIP_PARSER) module is used to capture the external video data into the VIP module.

9.4.5.1 Features

Each VIP module contains two VIP_PARSER modules (one VIP_PARSER per slice).

For a single VIP_PARSER, the video capture functions include:

- Two Pixel Clock Input Domains are supported (Port A and Port B):
  - Each Pixel Clock Input Domain has separate clock and framing signals.
  - Each Pixel Clock Input Domain can support embedded (BT.656/1120 style in /24-bit, or BT.656 in 8-bit) or discrete (BT.601 style) sync.
  - Pixel Clock Input Domain Port B supports one 8-bit input data bus. At SoC level, the same device pins may be shared between Port A and Port B. One 24-bit chip level set of device pins is shared. Port A has access to all 24 bits. Port B only has access to 8 bits.
- Embedded Sync data interface mode supports single or multiplexed sources;
- Discrete Sync data interface mode supports only single source input;
- The two Pixel Clock Input Domains can be individually configured in any combination of Embedded or Discrete Sync;

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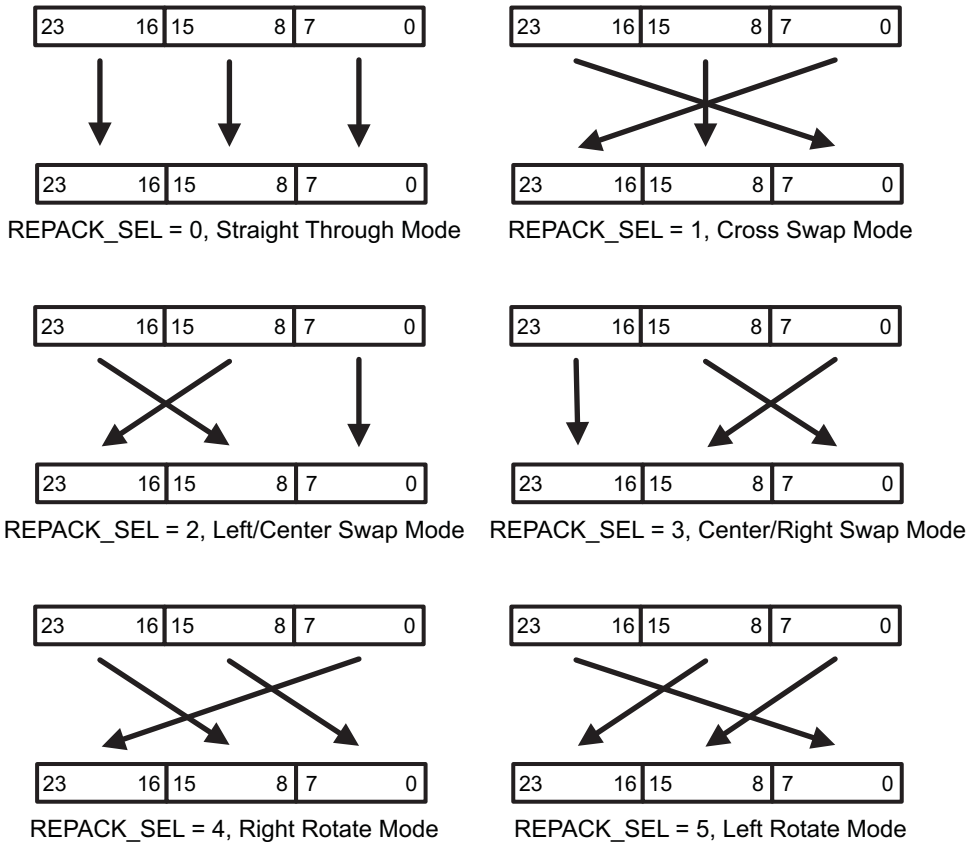
- Vertical Ancillary Data capture is supported for each input source;
- A maximum of 8 + 1 (8 normal line sources + 1 split-line source) multiplexed sources are supported for a single Pixel Clock Input Domain using TI Line Mux Mode;
- Multiplexed data can only appear in embedded sync mode;
- Where possible, blanking pixels that may contain embedded vertical ancillary data will be stored in a dedicated buffer per each video source;
- Optional selection of channel (Luma or Chroma, or both) from which Vertical Ancillary data is extracted for YUV422 source;
- For RGB source, Vertical Ancillary data can be found in one of the R, G, or B channels. The VIP_PARSER can select the channel from which Vertical Ancillary data is extracted;
- Ancillary Data can appear in the Horizontal Blanking as well as the Vertical Blanking. Typically, only Vertical Blanking Ancillary Data is captured. However, Horizontal Blanking Ancillary Data can be captured as well using HSYNC style discrete sync capture mode;
- Video up to WUXGA (1920 × 1200) can be supported using Port A in 16-bit or 24-bit mode.

9.4.5.2 Repacker

The Repacker module rearranges the input bit ordering of the 24-bit data bus on Port A of each VIP slice. This module allows external input data to be presented to the datapath such that various data packing formats can be achieved in memory. As shown in Figure 9-15, a Repacker exists for each 24-bit input port.

The Repacker module is a simple multiplexer that serves to move input bits to different locations on the its output bus to VIP Parser. Figure 9-15 shows the supported bytelane swapping modes corresponding to different VIP_XTRA_PORT_A[30:28] REPACK_SEL settings.

Figure 9-15. Bytelane Swapping Modes



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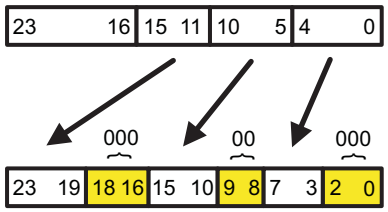
16-bit RAW data entering the VIP subsystem is packed as a contiguous input bus from bits 15 to 0. This 16-bit RAW input must be remapped to the RGB565 format, so that it can be saved to DDR memory properly, because the VPDMA does not support the RAW16 input format natively. Instead, the RAW 16 format is first remapped as RGB565 data and then given to the VPDMA. Figure 9-16 describes the VIP_XTRA_PORT_A[30:28] REPACK_SEL = 6 option to remap a contiguous [15:0] RAW input data bus to a RGB565 compliant output bus. This RAW16 data will use RGB565 data types in the VPDMA Data Descriptors.

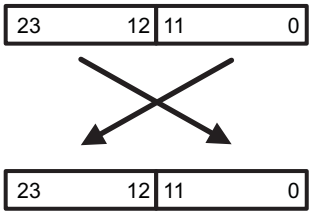
Figure 9-16. RAW16 to RGB565 Mapping



REPACK_SEL = 6, RAW16 Mapping Mode

Figure 9-17 describes the mux configuration where 12 bit components are swapped. This mode may be useful when the input data is 12 bit per component YUV422 and is sent directly to memory.

Figure 9-17. RAW12 Swap



REPACK_SEL = 7, RAW12 Swapping Mode

NOTE: There is no repacker for the 8-bit input port (Port B of each VIP slice).

When using Embedded Sync input, REPACK_SEL should be be set to “000”. The RAW16 and RAW12 mapping modes do not work for embedded sync streams.

9.4.5.3 Analog Video

A digital interface stream is based on analog video. The waveform for a line of NTSC analog video is shown in Figure 9-18.

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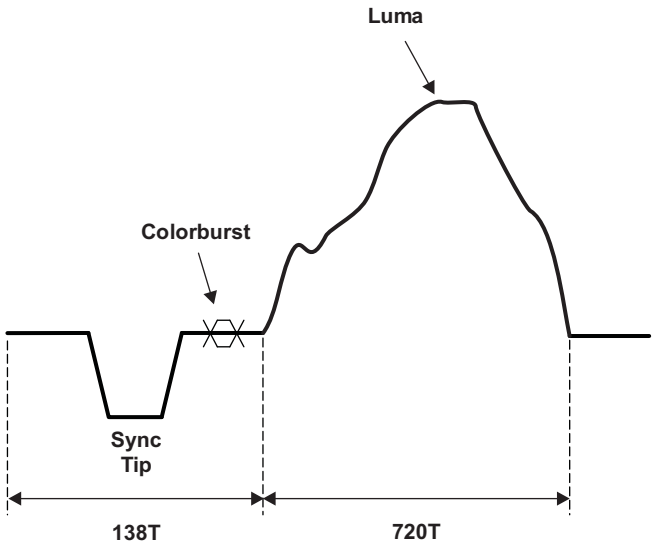
Figure 9-18. NTSC Analog Video Waveform for One Horizontal Line



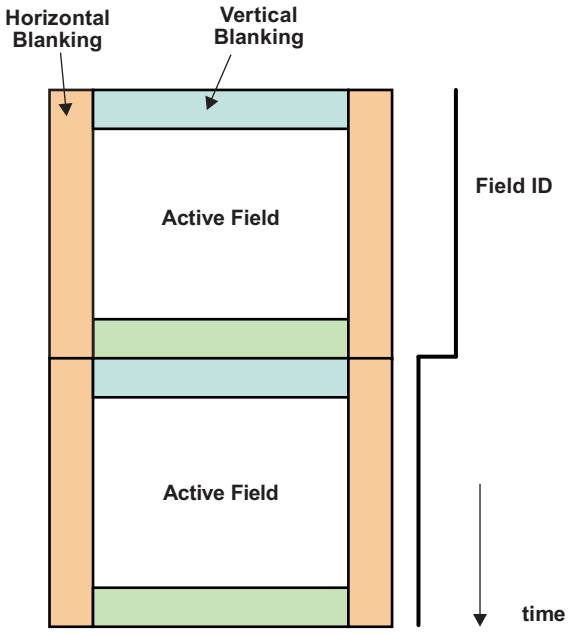
T is a time constant. For NTSC, T=1/13.5 MHz = 74ns.

9.4.5.4 Digitized Video

Digitized video is based on scan lines in found in analog video. BT.601 uses various sync signals to specify when a new field and a new line starts. BT.656 and BT.1120 uses sync words embedded in the data stream to specify start of field and start of line.

An image can be digitized into regions shown in Figure 9-19.

Figure 9-19. Digitized Video



With the capability to encode sync words inside the data stream, there is more flexibility for adding non-video related data, called Ancillary Data. Also, code words embedded in the digital stream can be used as a type of identifier for multiplexing several sources of video into one data stream.

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Figure 9-20 shows End-of-Active-Video (EAV) and Start-of-Active-Video (SAV) code words added to a video transmission. The period between the EAV and SAV is equivalent to Horizontal Blanking. The period between the SAV to the next EAV is active video or vertical blanking.

In the BT.656 or BT.1120 embedded code word scheme, three bits of the EAV/SAV code word are important: F (field), H (horizontal blanking), and V (vertical blanking).

Figure 9-20. Code Word Embedded Video Format

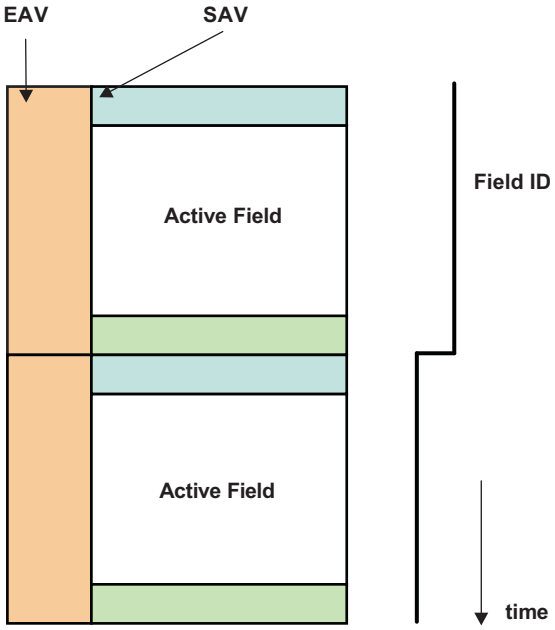
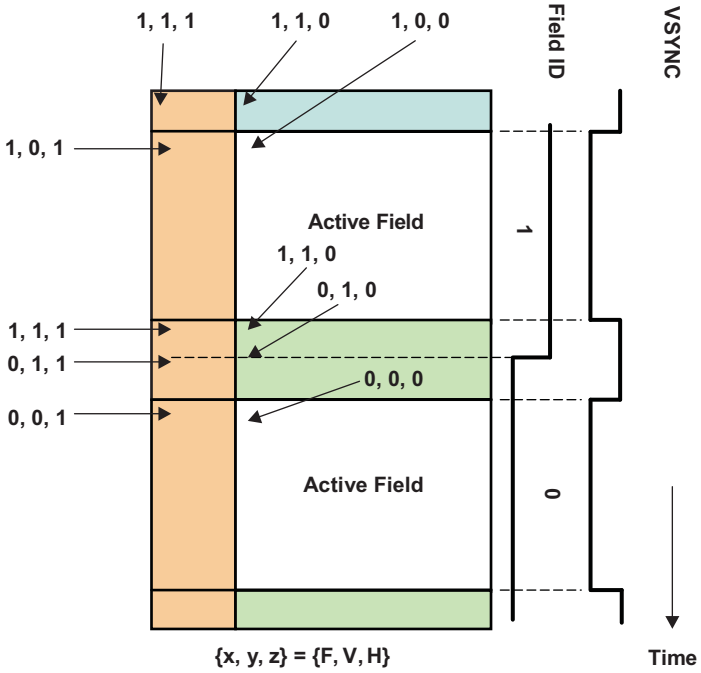


Figure 9-21 shows the values of F, V, and H flags at different locations in the picture. The Field flag represents the state of the Field ID for the picture. For progressive frames, F is always '0.' The V flag specifies vertical blanking areas. The H flag specifies horizontal blanking portions of the picture.

Figure 9-21. Digitized Video with F, V, and H Flags in EAV/SAV



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9.4.5.5 Frame Buffers

The VIP/VPDMA support Frame Buffers in DDR memory for Active Video and Ancillary Data.

4:2:2 data is always saved in packed pixel buffers.

4:2:0 data is saved in Planar Luma buffers and Planar CbCr pair buffers.

A Luma Frame Buffer is a Planar storage area. Each line is the width in pixels (1Byte/pixel) of the output picture size format. The frame buffer contains the number of active video lines in the output picture size format.

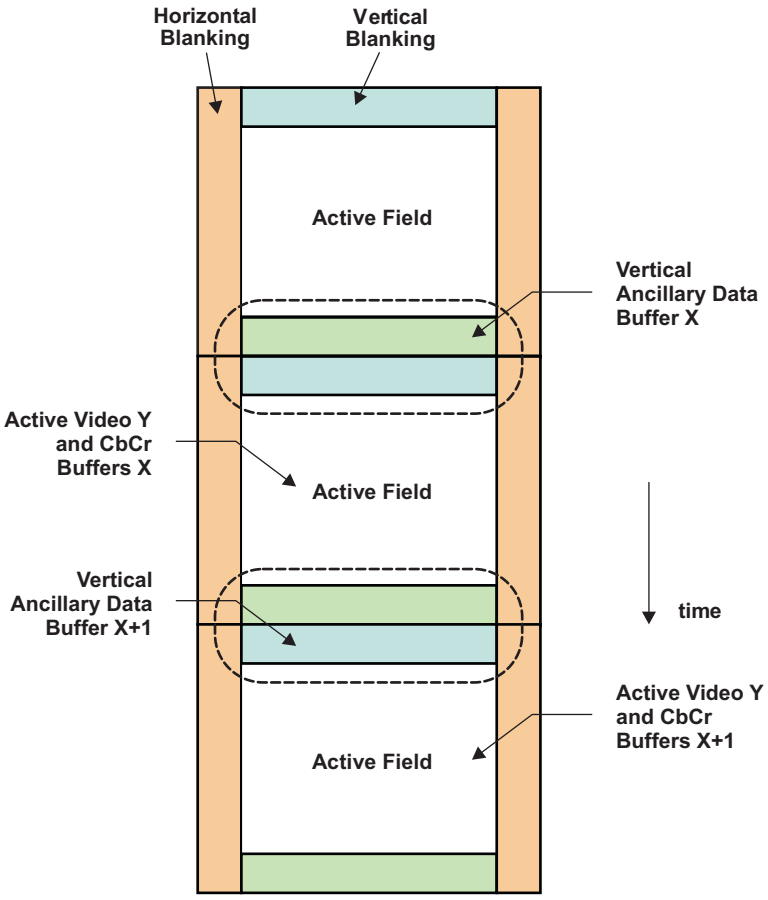
A Chroma Pair Frame Buffer is Planar storage of CbCr pixel pairs, with each pixel being a byte. For 4:2:0 storage, N lines in the output picture active video results in N/2 lines of CbCr pairs being stored.

The Ancillary Data buffer is different than the Active Video Frame Buffers. The Ancillary Data buffer only stores Vertical Blanking Ancillary Data. The number of lines in the Ancillary Data buffer is the same as the number of Vertical Blanking lines. Typically, only one channel is extracted from the Vertical Blanking data, so the width of the Ancillary Data buffer is the same as the width of the Luma Buffer.

In 8-bit input mode, it is possible for both Luma and Chroma sites to be extracted for Vertical Ancillary data. Each color component is strobed on separate input clock cycles. In this case, the line width of the Ancillary data is twice the Luma line width of the picture. Both Luma and Chroma sites cannot be extracted for 16-bit input mode because both Luma and Chroma are sent on the same input clock cycle and the Ancillary port to the VPDMA VPI is only 8 bits wide.

Figure 9-22 shows how the planar data regions are stored in DDR memory. The vertical blanking data is stored in a set of Planar Buffers. Note that the bottom of the Vertical Ancillary Data from the previous field or frame is stored in the same buffer as the top of the Vertical Ancillary Data from the current field or frame.

Figure 9-22. Planar Buffer Storage Description



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The Luma representing Active Video is stored in a set of Planar Buffers. The CbCr Chroma Pairs are stored in a set of Planar Buffers.

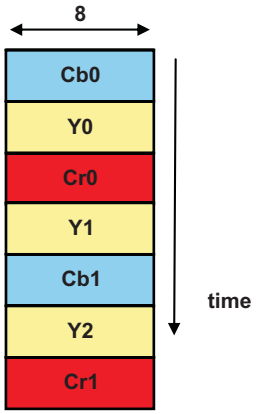
9.4.5.6 Input Data Interface

This section describes how the data (luma and chroma data for YUV422 format capture and R,G, and B data for RGB888 format capture) is muxed for the various interface modes.

9.4.5.6.1 8b Interface Mode

In 8-bit data interface mode, the input pixels are multiplexed according to Figure 9-23. The Chroma Format is 4:2:2. Sites with Cb/Cr pixels are known as Chroma sites. Those sites with Y pixels are known as Luma sites.

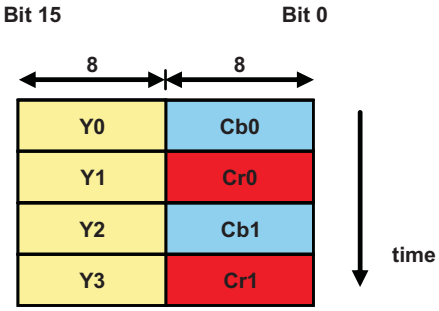
Figure 9-23. 8-bit Interface Discrete Sync Pixel Multiplexing



9.4.5.6.2 16b Interface Mode

In 16-bit interface mode, Luma is on 8 MSB bits of the data bus and Cb/Cr chroma pixels alternate on the other 8 bits of the data bus as shown in Figure 9-24.

Figure 9-24. 16-bit Interface Discrete Sync Pixel Multiplexing



9.4.5.6.3 24b Interface Mode

RGB or YUV444 data is sent in 24b Interface Mode. The three components are packed into the data bus and sent to the VPDMA. The 24-bit Luma VPI client to the VPDMA carries all three components. This data is saved to the DDR in packed mode. That is, the three components are not separated by hardware. The 24-bit data bus is shown in Figure 9-25.

Ancillary data is saved in the Ancillary Data buffer. The VIP_PORT_A[5:4] CTRL_CHAN_SEL and VIP_PORT_B[5:4] CTRL_CHAN_SEL configuration register is used to select whether the ancillary data is from the R/Y, G/U, or B/V channels.

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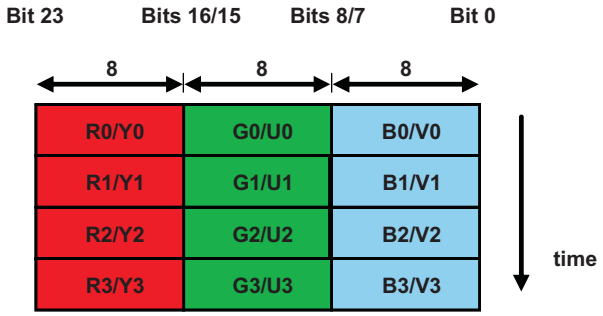
Figure 9-25. 24b Interface RGB Discrete Sync

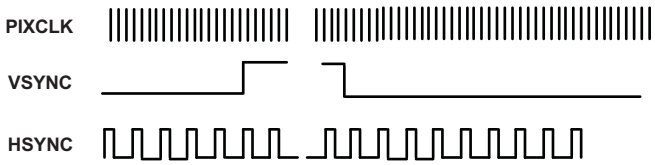


In 24b interface mode YUV4:4:4 data is also supported. The flow for YUV4:4:4 data is the same as RGB data (Figure 9-25). Bits [23:16] of the input data bus are placed on bits [23:16] of the data bus going to VPDMA, bits [15:8] of the input bus are placed on bits [15:8] of the data bus going to VPDMA and finally bits [7:0] of the input data bus, are placed on bits [7:0] on the bus going to VPDMA.

9.4.5.6.4 Signal Relationships

A digital representation of video can be realized by using HSYNC and VSYNC signals to identify frame start and line start. Suppose HSYNC and VSYNC are active high, Figure 9-26 shows the general relationship of these signals.

Figure 9-26. Discrete Sync Signals



Every PIXCLK cycle carries either an active pixel or a blanking pixel. VSYNC pulses between two fields (or frames, in the case of progressive video). HSYNC pulses to signify the beginning of every line. An ACTVID signal can be used as a data valid to specify active video.

Discrete Sync cannot be used with any multi-camera multiplexed stream inputs. In the device, if Port A is configured for 24-bit discrete sync, then Port B must be disabled since there are no more data input pins left over for Port B.

If Port A is not 24 bits, then the 8-bit Port B can be configured and enabled for either discrete or embedded sync.

9.4.5.6.5 General 5 Pin Interfaces

Discrete Sync signal handling varies among different sending devices. The information that must be conveyed includes the pixel data value, field ID, horizontal blanking, and vertical blanking. Many devices can be configured to adjust the timing of the signals relative to each other.

In this section, DATA will be depicted as 8 bits. However, discrete sync does optionally support 16-bit and 24-bit data input. Type 1 is named after a generic five pin interface between the sending and receiving devices.

In Figure 9-27, P0 represents the first pixel in the horizontal blanking interval following the last vertical blanking line of the previous field or frame. HSYNC specifies the horizontal blanking region and VSYNC specifies that the P0 pixel is in the vertical sync area. HSYNC can be a strobe that is active one or more cycles and can deassert before the actual end of horizontal blanking or HSYNC may be active for the full duration of horizontal blanking.

Likewise, VSYNC can be a strobe that is active one or more cycles and can deassert before the actual end of vertical blanking or VSYNC may be active for the full duration of vertical blanking.

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FID can change at this pixel or it may change later. For interlaced source, though, the FID will be inverted for this pixel at the same time point in the next field. So, it does not really matter when FID is captured. Many sending devices allow the location of FID changes to be programmable.

In this diagram and all others in this document, the active polarities of the interface signals can be either high or low. For the sake of uniformity in this document, all polarities are drawn active high. Also, different vendors have different datasheet names for the interface signals.

Figure 9-27. Type 1, First Horizontal Blanking Pixel

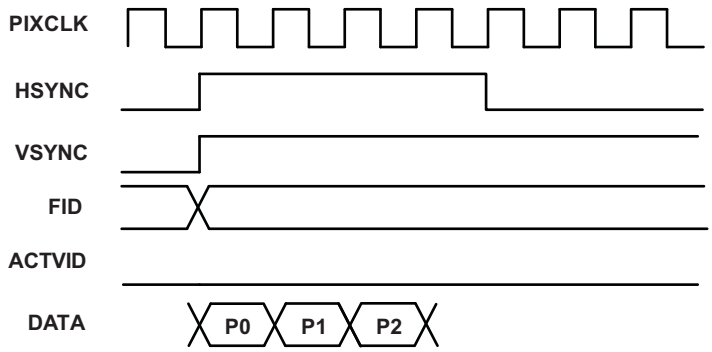
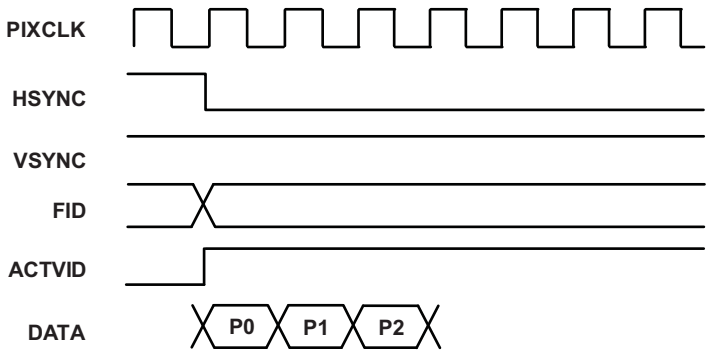


Figure 9-28 shows the P0 pixel being the first Chroma Channel data value in the Vertical Ancillary Data region. HSYNC is definitely de-asserted by now since P0 is no longer in horizontal blanking. ACTVID may or may not be active for Vertical Ancillary Data. Some devices consider these pixels to be Active (as in non-horizontal blanking). Other devices consider only video to be ACTIVE Video.

Figure 9-28. Type 1, First Vertical Ancillary Data Pixel



Following the vertical blanking region, the video portion of the field or frame starts. Figure 9-29 shows the horizontal blanking area in this video portion of the field or frame. P0 is the first pixel in the horizontal blanking. HSYNC is active for one or more pixel clocks. VSYNC is inactive in this video area. FID can change here. ACTVID is low since P0 is horizontal blanking.

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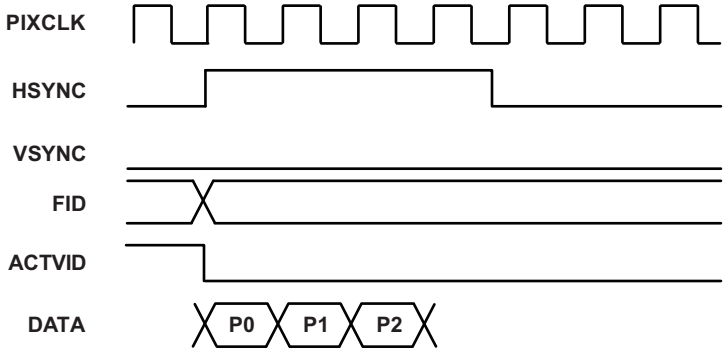
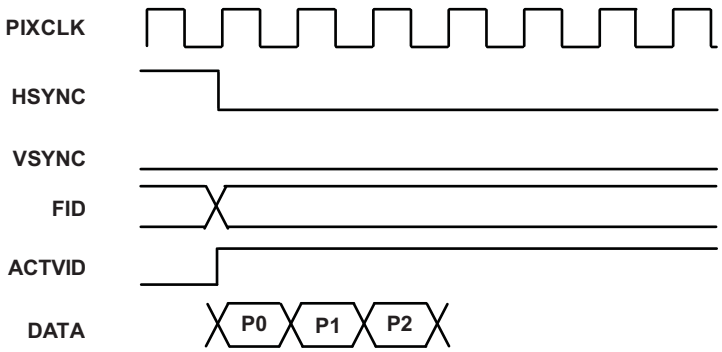
Figure 9-29. Type 1, Horizontal Blanking in Video Region



In Figure 9-30, P0 represents the first Chroma pixel in the Active video line. HSYNC is inactive, since P0 is in the active video region. Likewise, VSYNC is inactive. FID may or may not change here. ACTVID is high to signal capturing of video pixels.

Figure 9-30. Type 1, First Video Pixel



9.4.5.6.6 Signal Subsets—4 Pin VSYNC, ACTVID, and FID

A sending device may use only a subset of the signals described in Section 9.4.5.6.4. The sending device just needs to convey important signals required to capture the field or frame. It can be shown that various selections of four pins can be used to satisfy all Type 1 conditions.

Three pins, VSYNC, ACTVID, and FID, plus a pixel clock can be used to support discrete sync. VSYNC would bump the capture buffer. An inactive to active level of ACTVID specifies a line of data to capture. FID determines the field ID polarity. The scenario in which the sending device wants the receiving end to capture Vertical Ancillary Data using 4-pin signaling is shown in Figure 9-31.

Figure 9-31. 4-Pin Reduced ACTVID Signaling with Vertical Ancillary Data

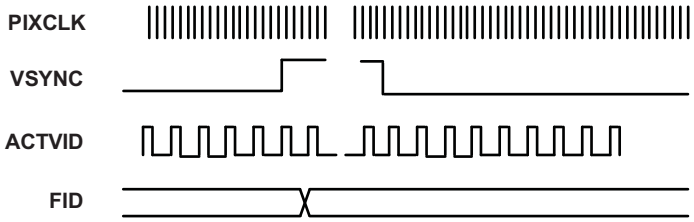


Figure 9-32 describes the case using the 4-pin interface in which the sending device does not send Vertical Ancillary Data.

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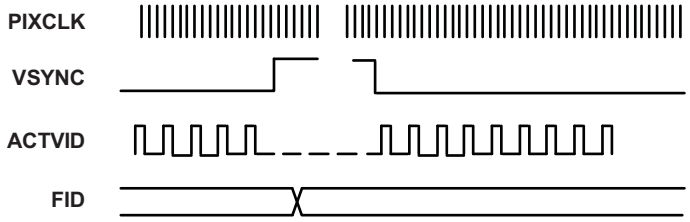
Figure 9-32. 4-Pin Reduced ACTVID Signaling with No Vertical Ancillary Data

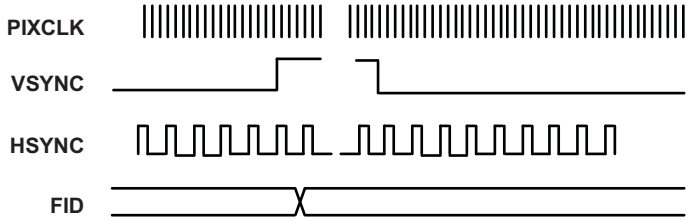


9.4.5.6.7 Signal Subsets—4 Pin VSYNC, HSYNC, and FID

In this style of Discrete Sync, as shown in Figure 9-33, four pins are used including the Pixel Clock. HSYNC signals the beginning of the line. All data in the line is captured, including Horizontal Blanking Data. In fact, this signaling mode is the only one which allows Horizontal Blanking Data to be captured.

Of course, by capturing the horizontal blanking pixels in the frame buffers, there is no way to be certain exactly where the blanking ends and the active video starts. One would have to rely solely on video format specs to find the active video inside the frame buffer.

Figure 9-33. 4-Pin Reduced HSYNC Signaling with Vertical Ancillary Data



9.4.5.6.8 Vertical Sync

Vertical Sync is used to indicate lines that are in the vertical blanking interval. The VSYNC also separates fields or frames. To be spec compliant, VSYNC should be active for a few lines at the bottom of the picture. The exact number of vertical blanking lines at the bottom depends on the specification for the picture format (480i, 480p, 720p, 1080i, 1080p).

Likewise, the number of vertical blanking lines at the top of the picture depends on the video format specification corresponding to the incoming picture.

In the VIP_PARSER, lines associated with an Active VSYNC are stored in the vertical ancillary data buffers using the ANC VPI port to the VPDMA. Lines without an Active VSYNC are stored in the active video Luma and Chroma-pair buffers using the Y and UV VPI ports, respectively, to the VPDMA.

When using HSYNC signaling instead of ACTVID, the VSYNC signal may be derived from an analog source such as an NTSC/PAL decoder. In this case, VSYNC may not transition on the exact cycle as HSYNC. Thus, the VIP_PARSER supports a window region around HSYNC in which VSYNC transitions will be detected. A VSYNC transition occurring within the window is identified the same way as if VSYNC transitioned on the same cycle as HSYNC going active.

The window is defined by a pre-window, which is determined by the VIP_PORT_A[21:16] FID_SKEW_PRECOUNT and VIP_PORT_B[21:16] FID_SKEW_PRECOUNT registers. There is also a post-window that is defined by VIP_PORT_A[29:24] FID_SKEW_POSTCOUNT and VIP_PORT_B[29:24] FID_SKEW_POSTCOUNT for port B. Note that although the configuration registers are named FID_SKEW, they are also used for defining the VSYNC transition window. The window region definition is shown in Figure 9-34.

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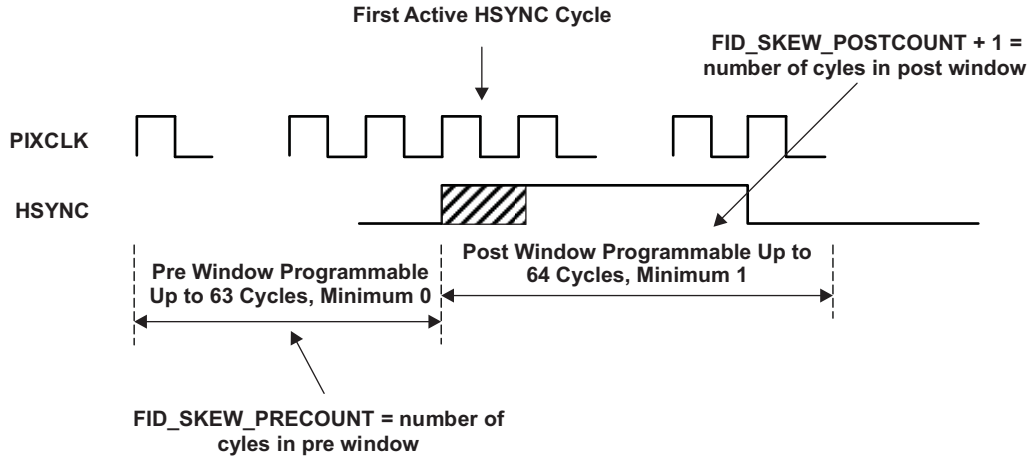
Figure 9-34. VSYNC Pre and Post Window



The results of VSYNC behavior in the transition window are shown in Figure 9-35. A low to high transition in the window is equivalent to VSYNC going low to high on the active HSYNC cycle.

Likewise, a high to low transition in the window is equivalent to VSYNC going high to low on the active HSYNC cycle.

Two transitions of VSYNC within the VSYNC window is not allow and is undefined behavior.

If VSYNC is high throughout the transition window, then the HSYNC line is in vertical blanking.

If VSYNC is low throughout the transition window, then the HSYNC line is in active video.

Note that VSYNC skew generally only applies to input signals that have been sampled from an analog source, as in a NTSC/PAL decoder. If the VSYNC is a VBLANK-type signal or if the sending device is another all-digital IC, then the VSYNC signal does not have a skew since VSYNC will be aligned to HSYNC. In this case, setting FID_SKEW_PRECOUNT = ‘0’ and FID_SKEW_POSTCOUNT = ‘0’ (within PORT_A and PORT_B registers) defines a minimum size window which will capture the value of VSYNC on the same cycle that HSYNC goes active.

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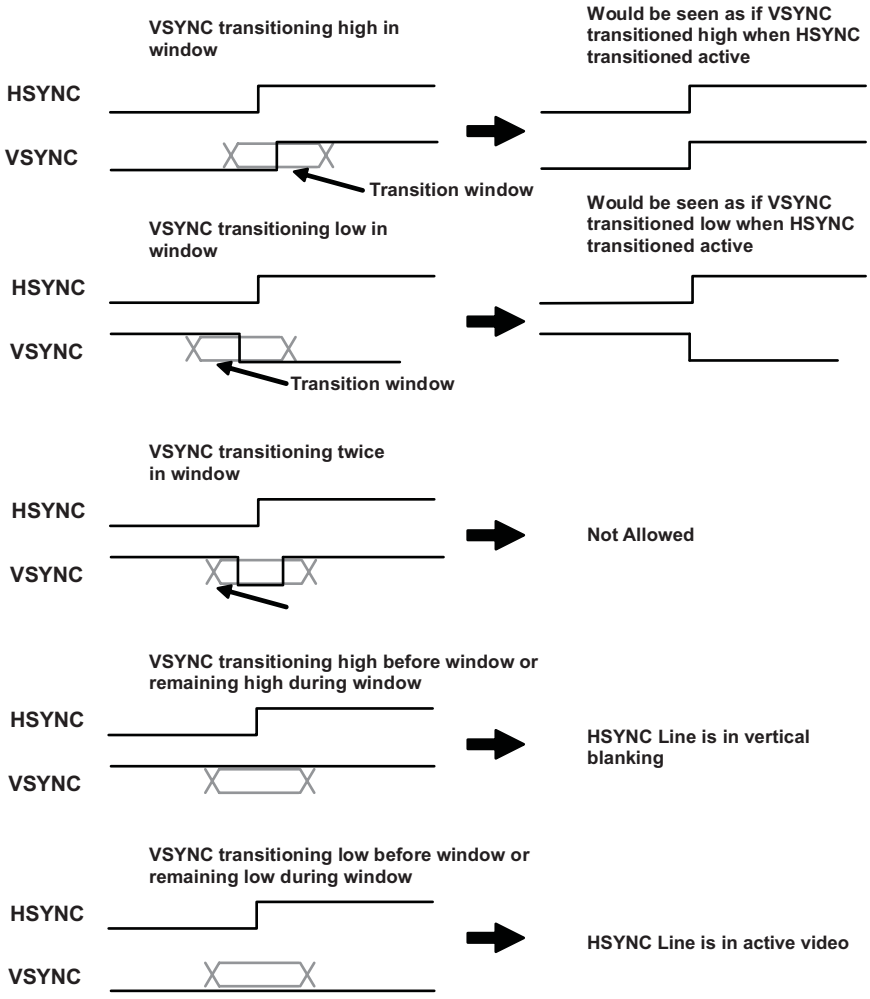
Figure 9-35. VSYNC Equivalence When Using Transition Window



9.4.5.6.9 Field ID Determination Using Dedicated Signal

For Progressive Source, FIELD ID is always '0.'

For Interlaced Source, FIELD ID needs to be extracted consistently.

In some cases, vertical sync is active on the first pixel of a line in the vertical blanking period and it stays active until the last line in the vertical blanking period.

However, the pixel where the FIELD ID signal transitions can be quite variable and depends on the external chip driving the VIP_PARSER. Many parts that generate digitized raw video have a programmable feature to specify when FIELD ID changes. FIELD ID is valid at the same point for every field. That is, if FIELD ID is read at one particular place in a field, the polarity of the signal will be reversed at the same location in the next field. So, FIELD ID can be corrected with a programmable polarity configuration bit FID_POLARITY (within VIP_PORT_A and VIP_PORT_B registers) that is XOR'ed with the captured value.

For discrete sync mode, FIELD ID will be registered on the first active pixel capture cycle of each line in both styles of HSYNC and ACTVID usage as specified in Figure 9-36 and Figure 9-37.

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Figure 9-36. FID Registering When Using HSYNC

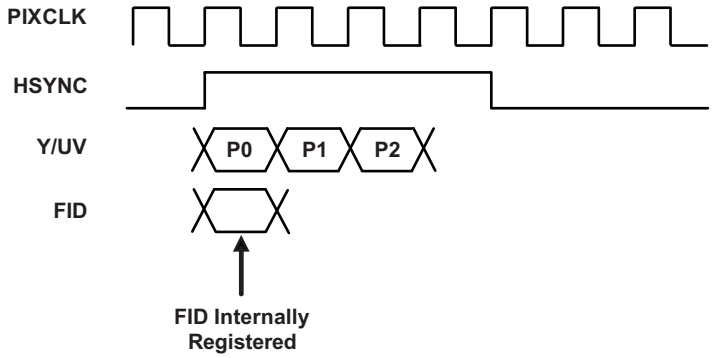
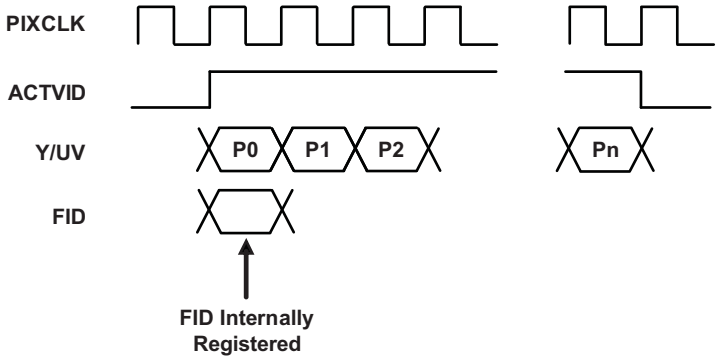


Figure 9-37. FID Registering When Using ACTVID



9.4.5.6.10 Field ID Determination Using VSYNC Skew

In order to save a device pin, there is a case where a skew may be inserted into VSYNC (with respect to HSYNC) when HSYNC is used as a start of line indicator as described in Figure 9-33. In this case, no FIELD ID signal is sent by the source chip. A description of Field ID determination by VSYNC skew is shown in Figure 9-38.

The active polarity of VSYNC falling within n pixel clock cycles of the first active cycle of HSYNC indicates the field id. If VSYNC is active before this time window, then the FIELD_ID = ‘1’ for the next picture. If VSYNC becomes active within this window, then FIELD_ID = ‘0’ for the next picture.

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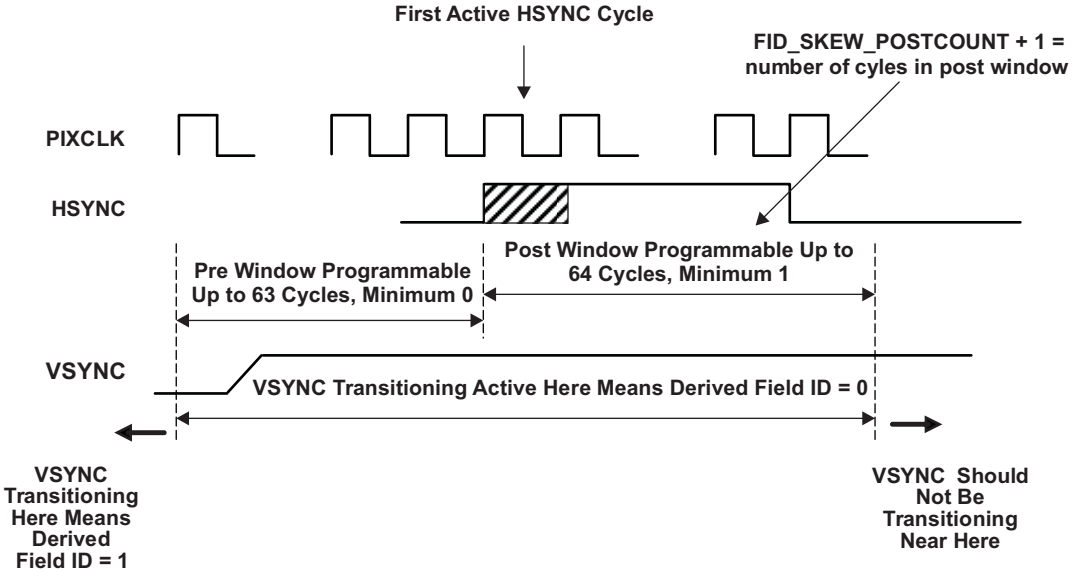
Figure 9-38. Field ID Determination By VSYNC Skew



When using FID determination by VSYNC skew, the value for VSYNC is also determined by transitions in the window as shown in Figure 9-35.

The VIP_PARSER supports a configuration FID_POLARITY bit within VIP_PORT_A and VIP_PORT_B registers. For FID determination by VSYNC Skew, the fid determination functions are described in Table 9-10.

Table 9-10. Polarity Table for FID Determination By VSYNC Skew

FID_POLARITY	Transition in Pre/Post Range	FID Determination
0	No	1
0	Yes	0
1	No	0
1	Yes	1

9.4.5.6.11 Rationale for FID Determination By VSYNC Skew

FID determination by VSYNC skew is a method for field ID determination derived from the analog NTSC and PAL interlaced specifications. Under this method, the sending device will not be providing a FID signal. NTSC has 525 total lines split between two fields. PAL has 625 total lines split between two fields. Each of these interlaced standards support an odd number of lines.

Let's consider just the 525 active line NTSC signal. For the sake of consistency, let's call Line 1 the first line of the 2-field pair and Line 525 the last line of the 2-field pair.

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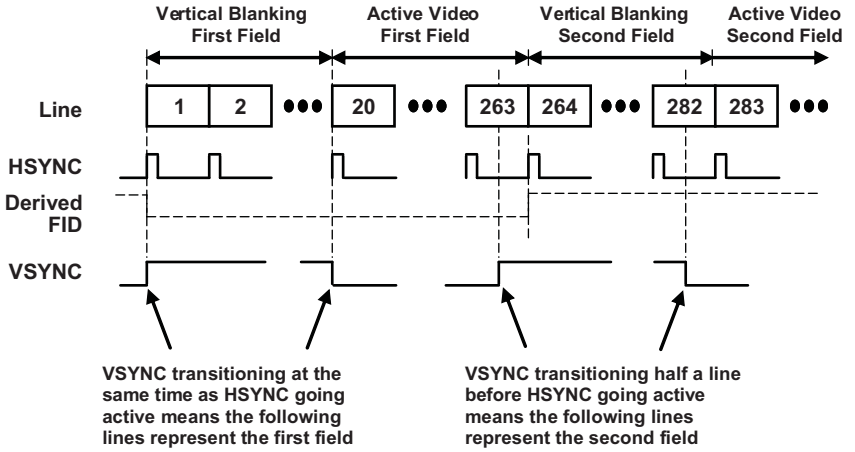
Figure 9-39. Example of 525-line FID Determination By VSYNC Skew



A waveform is shown in Figure 9-39. VSYNC is defined to go active at the same time as HSYNC for the first line of the first field in a two-field picture pair. For this first field, VSYNC will go inactive after Line 20.

For the second field, VSYNC will go active in the middle of Line 263 to signal that Line 264 is the start of a vertical blanking interval. When HSYNC for Line 264 arrives, coinciding with the vertical blanking interval for the beginning of the second field, VSYNC has already been active for half of Line 263. For the second field, VSYNC will go inactive midway through Line 282 to indicate that Line 283 is active video. When HSYNC for Line 283 appears, VSYNC has already been inactive for half a line.

By seeing whether VSYNC transitions at the beginning of a line or whether it transitions at the midway point of a line, one can determine whether the upcoming group of lines represents the first field or the second field. The derived FID is shown in dashed lines.

The analog NTSC specification defines the field ID changing part way into the vertical blanking. That is, the first few lines of vertical blanking belong to the previous field and the next several lines of vertical blanking belong to the upcoming field. The VIP_PARSER saves one channel of the entire vertical blanking interval between two active video fields into a single buffer. The hardware does not discriminate between whether the vertical blanking lines belong to the bottom of the previous field or those belonging to the start of the next field. This usage model is consistent with vertical ancillary data capture for embedded sync mode of operation.

Obviously, FID Determination by VSYNC skew cannot be used when framing does not use the VSYNC signal but rather relies on the ACTVID signal instead.

9.4.5.6.12 ACTVID Framing

Instead of an HSYNC signal, the VIP_PARSER can use ACTVID framing as described in Figure 9-32. Under ACTVID Framing, VSYNC is used to separate vertical blanking lines from active video lines.

FID determination by VSYNC Skew is not allowed for ACTVID framing because there is no HSYNC input signal in this mode. Also, the VSYNC transition window is not employed. VSYNC is captured at the first pixel of each ACTVID grouping of pixels. Lines are separated by ACTVID transitioning inactive.

9.4.5.6.13 Ancillary Data Storage in Descrete Sync Mode

Ancillary data appearing in horizontal blanking is called Horizontal Blanking Ancillary Data. Ancillary Data in vertical blanking is called Vertical Blanking Ancillary Data.

Horizontal Blanking Ancillary Data is not commonly used. For the ACTVID data valid mode described in Figure 9-31, there is no way to capture Horizontal Blanking Ancillary Data. Using the HSYNC mode in Figure 9-33, all blanking pixels are captured. However, the horizontal ancillary data is byte-by-byte distributed between the Luma and Chroma frame buffers. Chroma sited bytes are saved in the Chroma frame buffer and Luma sited bytes are saved in the Luma frtame buffer. Some CPU effort would be needed in order to extract ancillary data from the desired Luma or Chroma channel frame buffers. Also, the video on each line starts after the horizontal blanking period. This situation is shown in Figure 9-40.

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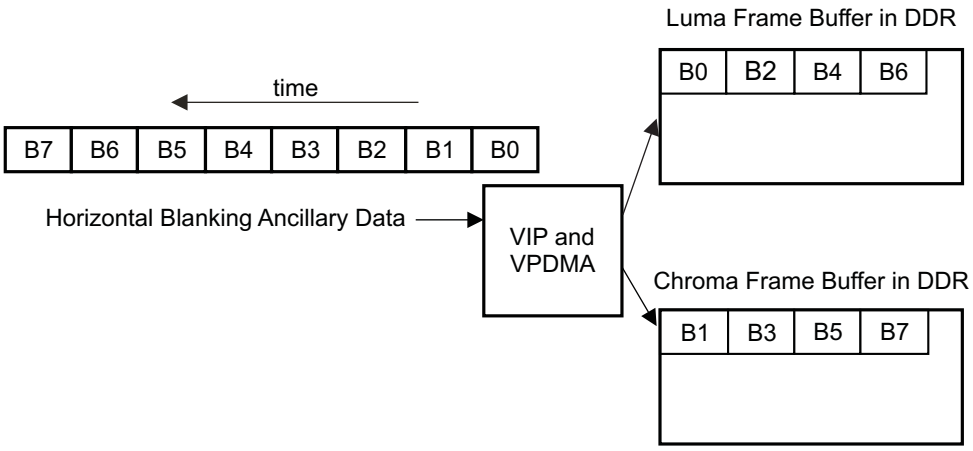
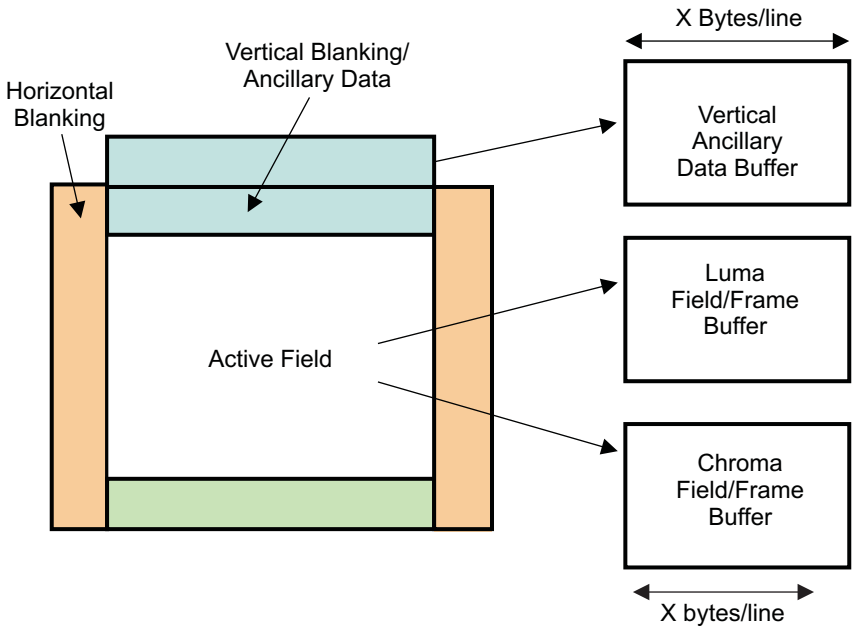
Figure 9-40. Horizontal Ancillary Data Packing When HSYNC Used as Sync Signal



With Interlaced source material, Vertical Blanking Ancillary data will be stored in a separate Vertical Ancillary Data Buffer as shown in Figure 9-41. The Channel from which vertical ancillary data is extracted is a configuration option. For an input image of x active pixels per line, each line of Vertical Blanking Ancillary Data will have x bytes. Unlike the horizontal case, the CPU parsing this Ancillary Data will see a contiguous section of Vertical Ancillary Data that is not intermixed with Video data.

Figure 9-41. Interlaced Field Vertical Blanking Ancillary Data Storage



For Progressive source video, the FIELD ID does not change. So, the Vertical Ancillary Data Buffer will contain all the information beginning from the vertical blanking of the previous frame. This situation is shown in Figure 9-42.

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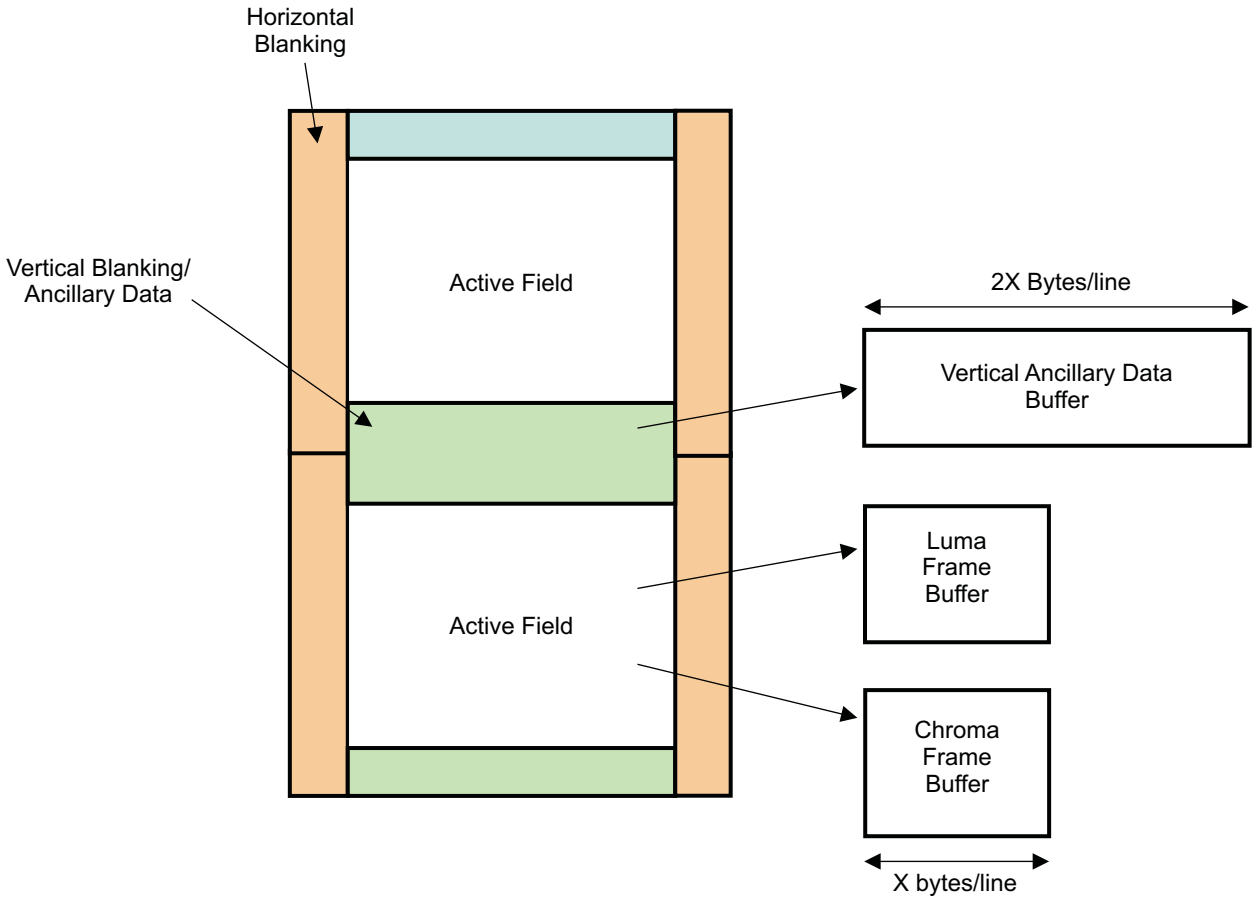
Figure 9-42. Progressive Frame Vertical Blanking Ancillary Data Storage

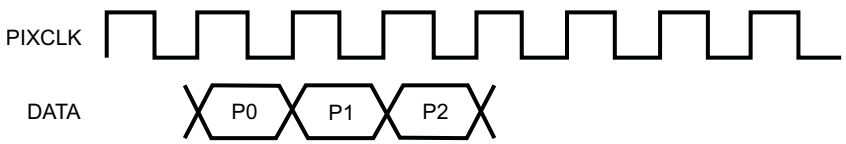


9.4.5.7 BT.656 Style Embedded Sync

9.4.5.7.1 Data Input

Like Discrete Sync Input, Embedded Sync mode takes data from the 24b input bus. Input data can be 8, 16, or 24 bits wide. A sample is retrieved each and every Pixel Clock cycle. There is no valid signal gating data entry. Figure 9-43 shows a valid data sample each Pixel Clock period.

Figure 9-43. Embedded Sync Data Entry



9.4.5.7.2 Sync Words

In embedded sync mode, code words are inserted into the stream at pixel clock rates. For external devices that send out 10 bits (single pixel interface) or 20 bits (parallel Y-Cb/Cr interface) of data, only the 8 (single pixel interface) or 16 (parallel 8bY-8bCb/Cr interface) most significant bits of each pixel are used.

The key code words are Start of Active Video (SAV) and End of Active Video (EAV). Three flags are found in these code words: F (field), V (vertical sync), and H (horizontal sync). These flags signify the position in the frame corresponding to the data immediately following the codeword. The flags determine whether the code is EAV or SAV and where they lie in the picture. The first byte of the code word is 0xFF. The second and third bytes are 0x00. The bit ordering of the fourth byte is detailed in Table 9-11.

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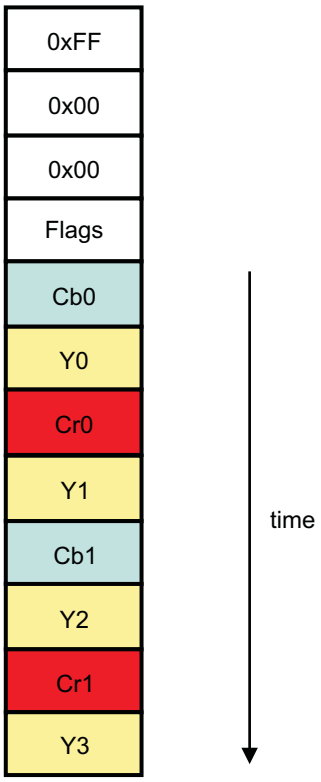
Table 9-11. Fourth Byte of EAV/SAV Code Word

7 (fixed)	6 (F)	5 (V)	4 (H)	3 (P3=V^H)	2 (P2=F^H)	1 (P1=F^V)	0 (P0=F^V^H)	Description
1	0	0	0	0	0	0	0	SAV, Field 0, Active Video
1	0	0	1	1	1	0	1	EAV. Field 0, Horizontal Blanking
1	0	1	0	1	0	1	1	SAV, Field 0, Vertical Blanking
1	0	1	1	0	1	1	0	EAV, Field 0, Horizontal Blanking in Vertical Blanking Region
1	1	0	0	0	1	1	1	SAV, Field 1, Active Video
1	1	0	1	1	0	1	0	EAV, Field 1, Horizontal Blanking
1	1	1	0	1	1	0	0	SAV, Field 1, Vertical Blanking
1	1	1	1	0	0	0	1	EAV, Field 1, Horizontal Blanking in Vertical Blanking Region

An example of the input ordering of the embedded code word, followed by active video, is shown in Figure 9-44. The input data mode is 8 bits for the example.

Figure 9-44. Code Word Format Example Followed by Video Data



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9.4.5.7.3 Error Correction

The FVH flags are sent with four protection bits to support double error detection, single error correction. A non-correctable detected error is simply ignored. An option exists for the protection bits to correct a single bit error in the FVH flags. The correction table is shown in Table 9-12. n/c means that the error condition is detected, but it is non-correctable.

Table 9-12. Error Correction Matrix

	F, V, and H Flags							
P3, P2, P1, P0	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0000	000	000	000	n/c	000	n/c	n/c	111
0001	000	n/c	n/c	111	n/c	111	111	111
0010	000	n/c	n/c	011	n/c	101	n/c	n/c
0011	n/c	n/c	010	n/c	100	n/c	n/c	111
0100	000	n/c	n/c	011	n/c	n/c	110	n/c
0101	n/c	001	n/c	n/c	100	n/c	n/c	111
0110	n/c	011	011	011	100	n/c	n/c	011
0111	100	n/c	n/c	011	100	100	100	n/c
1000	000	n/c	n/c	n/c	n/c	101	110	n/c
1001	n/c	001	010	n/c	n/c	n/c	n/c	111
1010	n/c	101	010	n/c	101	101	n/c	101
1011	010	n/c	010	010	n/c	101	010	n/c
1100	n/c	001	110	n/c	110	n/c	110	110
1101	001	001	n/c	001	n/c	001	110	n/c
1110	n/c	n/c	n/c	011	n/c	101	110	n/c
1111	n/c	001	010	n/c	100	n/c	n/c	n/c

9.4.5.7.4 Embedded Sync Ancillary Data

With Embedded Sync streams, only Vertical Ancillary Data can be extracted. The Vertical Ancillary Data buffer is the same width as the corresponding Luma and Chroma buffers. The channel from which Vertical Ancillary Data is extracted is a configuration option.

Horizontal Ancillary data cannot be extracted using embedded sync mode.

The Vertical Ancillary Data is captured starting from the end of the previous active video. See Figure 9-45 for a more detailed description of embedded sync packing.

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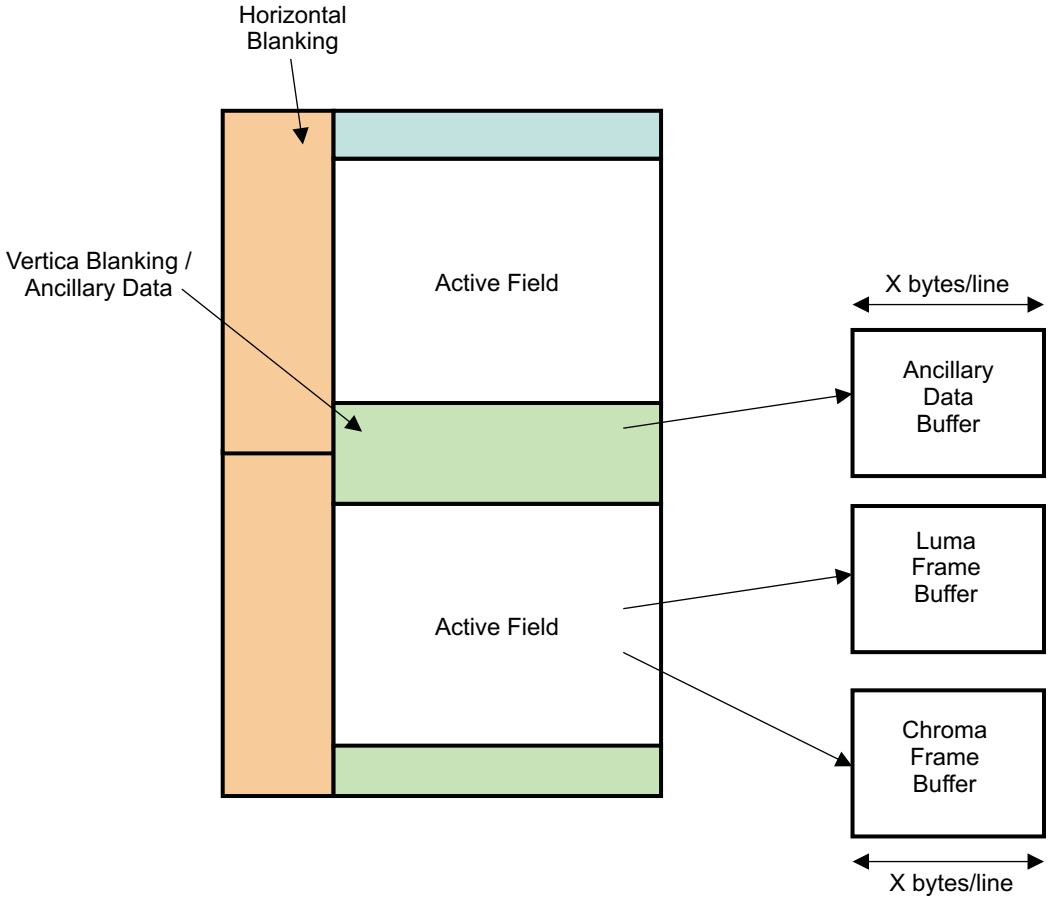
Figure 9-45. Embedded Sync Packing



9.4.5.7.5 Embedded Sync RGB 24-bit Data

YUV streams are separated into a planar Luma buffer, a planar Chroma Pair (CbCr) buffer, and a planar Vertical Ancillary Data buffer. RGB streams, on the other hand, are stored in a packed R-G-B format, as shown in Figure 9-46.

The BT.1120 standard defines a method of carrying RGB streams. After the SAV code, 8 bits of R, 8 bits of G, and 8 bits of B data are clocked in one cycle. A 24 bit data bus is required. The channel in which to search for the embedded sync codes and the FVH control code is determined by a configuration selection. Only vertical ancillary data from one channel (R, G, or B), which happens to be the channel where control codes are found, are captured. Vertical ancillary data in the other two channels are ignored.

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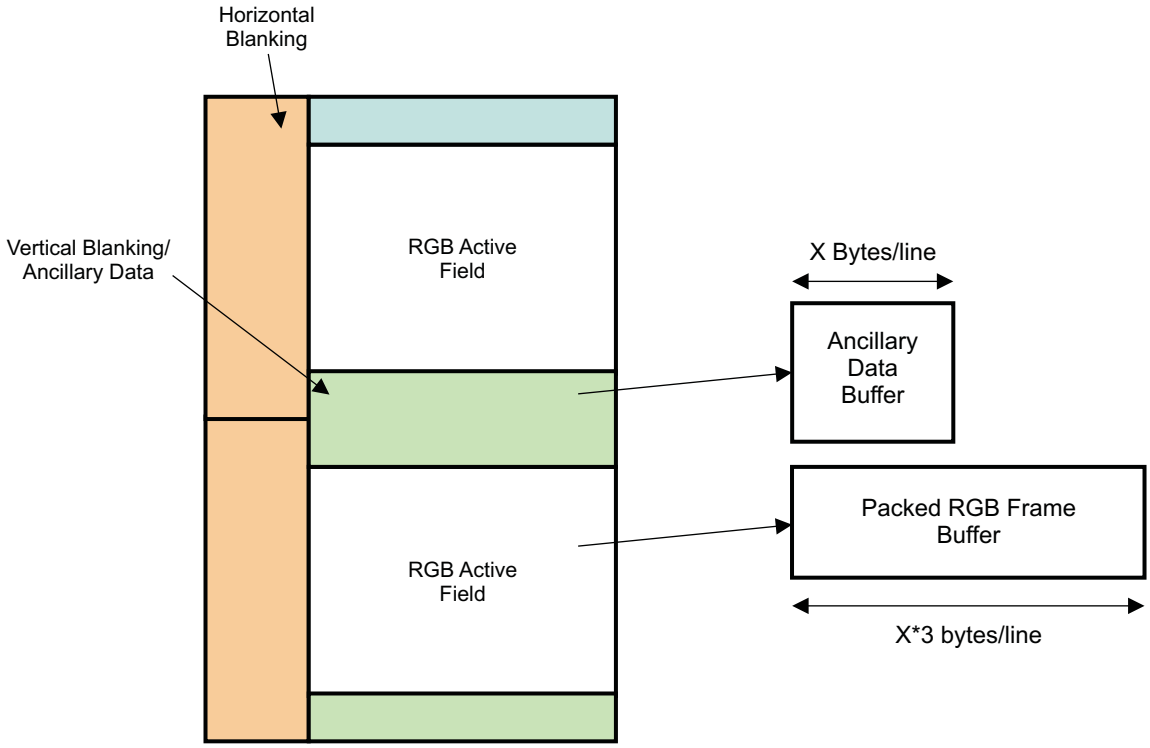
Figure 9-46. RGB Frame Storage



9.4.5.8 Source Multiplexing

9.4.5.8.1 Multiplexing Scenarios

Some applications require multiple camera sources to be used at the same time. For this type of device, one solution would be to support N-number of 8-bit or 16-bit data interfaces for each of N cameras. However, this solution does not efficiently minimize pin count. One set of 8-bit or 16-bit interfaces has the bandwidth to support more than one video source, depending on the resolution of the video. Table 9-13 is explanatory only and shows the number of sources that can be multiplexed in one VIP for 8-bit and 16-bit interface modes. Note that it does not reflect the capabilities of the VIP_PARSER. In addition, the interface pixel clock rates are shown. The VPDMA limits 16 camera sources to be saved to DDR memory per Pixel Clock Input Domain.

Table 9-13. Multiplexing Configurations and Pixel Clock Rates

	Maximum Channels in Single 16-bit Data Interface Mode	Maximum Channels in Dual 8-bit Data Interface Mode - Interleaved Channels per Single 8-bit Port. One 16-bit VIP can be configured to support two such 8-bit ports.	Interface Clock Rate (MHz)
HD Interlaced	2	1	148.5
D1 Interlaced	8	4	108.1
CIF Interlaced	n/a	n/a	n/a
HD Progressive	1	n/a	148.5
D1 Progressive	4	2	108.1
CIF Progressive (1)	32	16	162.2

(1) Blanking pixels are not used in the CIF clock rate calculations. Addition of blanking pixels would require a slightly higher clock rate.

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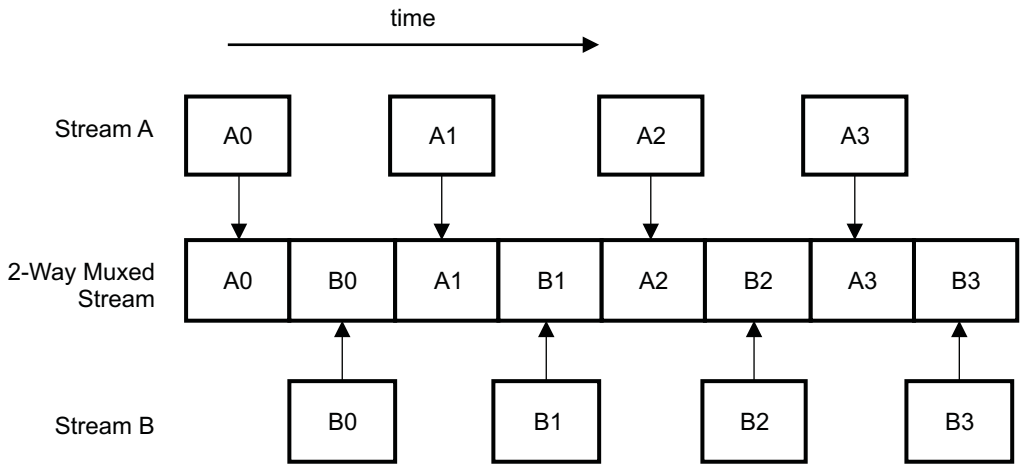
NOTE: These Channel Density values reflect one VIP subsystem.

9.4.5.8.2 2-Way Multiplexing

For 2-Way Multiplexing, two embedded sync streams are interleaved a pixel at a time as shown in Figure 9-47.

Figure 9-47. 2-Way Multiplexing



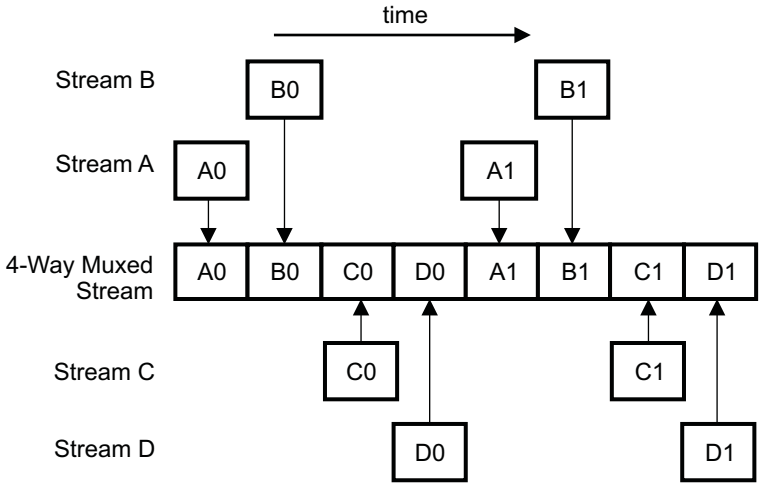
The sync codeword, FF-00-00-XY, is replicated in both source streams. In 2-Way Multiplexing, the sizes of both camera sources must be the same. Likewise, the Vertical Ancillary Data size for both sources must be identical. However, the two streams are not necessarily sending the same pixel site in adjacent clock cycles.

9.4.5.8.3 4-Way Multiplexing

For 4-Way Multiplexing, four embedded sync streams are multiplexed into one as seen in Figure 9-48.

Again, the sync codeword is in all four sources. Like 2-Way Multiplexing, the sizes of the four camera sources are the same and the sizes of the Vertical Ancillary Data regions are the same. The four streams are not necessarily sending the same pixel site in adjacent clock cycles.

Figure 9-48. Example of 4-Way Multiplexing



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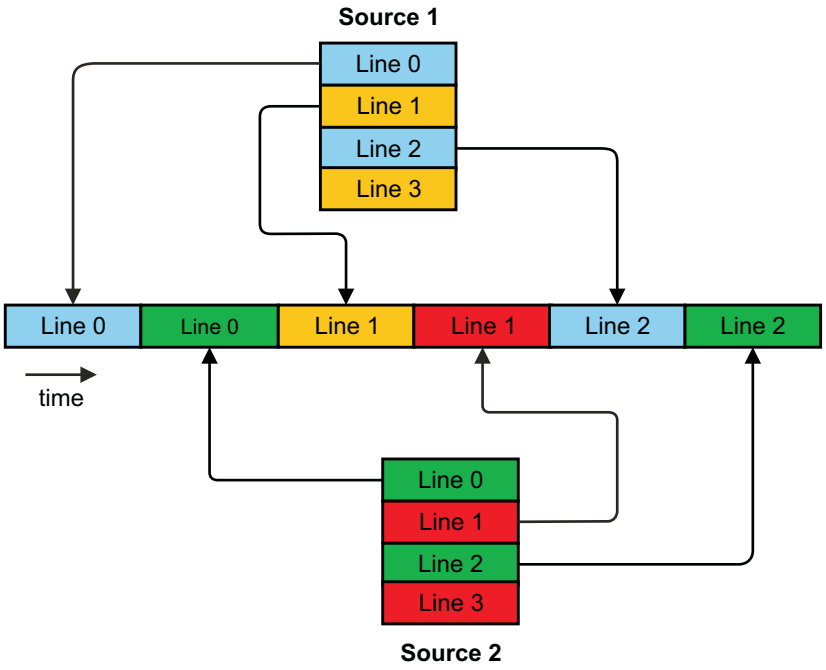
9.4.5.8.4 Line Multiplexing

In Line Multiplexing, n-different sources are sent into the VIP a complete line at a time using a modified version of embedded sync. An example of Line Multiplexing for two sources is shown in Figure 9-49.

Figure 9-49. Example of Line Multiplexing



The width and height of each source in Line Multiplexed data can be different. For instance, one source can be PAL while another one can be NTSC. A line is comprised of YUV422 pixels in repeating patterns of CbYCrY.

9.4.5.8.5 Super Frame Concept in Line Multiplexing

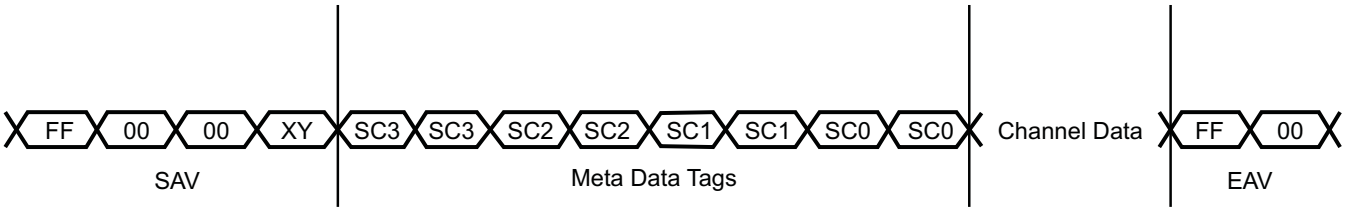
Different camera sources are interleaved on a line-by-line basis. The beginning of each line carries a Metadata tag that provides key information about that line. This Metadata tag is preceded by a SAV codeword in which F=0, V=0, and H=0.

At the end of the line, an EAV code is inserted with an appropriate number of padding pixels following it. This EAV code has F=0, V=0, and H=1. The startcodes used for the Metadata wrapped lines and the dummy lines form the Super Frame. The VIP_PARSER module has logic to parse out the super frame, analyze the Metadata tags, and frame buffer the line contents appropriately.

9.4.5.8.6 8-bit Data Interface in Line Multiplexing

Figure 9-50 is an example of an 8-bit line multiplexing interface. Channel Data is the CbYCrY sequence representing a line. Preceding Channel Data is the four byte Meta Data tags. Note that the Meta Data bytes are replicated in both the Luma and the Chroma sites. The entire structure is bounded by a traditional SAV/EAV code in which the V flag is 0.

Figure 9-50. 8-bit Line Mux Interface



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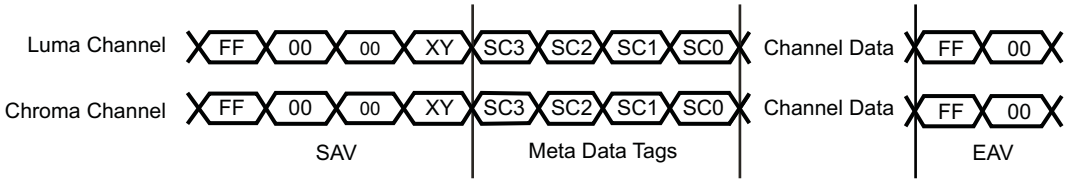
9.4.5.8.7 16-bit Data Interface in Line Multiplexing

Figure 9-51 describes the 16-bit line multiplexing interface. Channel Data is the active line. All the Y pixels are in the Luma Channel. The CbCr pixels are in the Chroma Channel. Each cycle, a 16-bit value representing one Luma sample and one Chroma sample enters the VIP_PARSER. The Meta Data tags are replicated in both channels. Likewise, the SAV/EAV startcodes are found in both channels. The V flags for the SAV/EAV startcodes are always 0.

Figure 9-51. 16-bit Line Mux Interface



9.4.5.8.8 Split Lines in Line Multiplex Mode

Suppose an external device is sending two dissimilar sources in Line Multiplex mode. One narrower source has X pixels per line. The wider source has 2X pixels per line.

The Meta Data has provisions for the external device to split a line. The Beginning of Line (BOL) and End of Line (EOL) flags tag a split line as described in Table 9-14.

Table 9-14. Split Line Table

BOL	EOL	Function
0	0	Undefined
0	1	Line Segment is the second half of a line
1	0	Line Segment is the first half of a line
1	1	Line has not been segmented into two.

9.4.5.8.9 Meta Data

Table 9-15 shows the bitfields in the Meta Data start codes.

Table 9-15. Meta Data Layout

Byte	7	6	5	4	3	2	1	0
SC3	1	BOP	EOP	RSVD	CH_ID[3:0]			
SC3	1	BOP	EOP	RSVD	CH_ID[3:0]			
SC2	0	BOL	EOL	VDET	LINE_ID[10:7]			
SC1	~LINE_ID[6]	LINE_ID[6:0]						
SC0	PAD	F	V	H	P3	P2	P1	P0

BOP tags the line as a startline in a period. A period is defined as the contiguous lines in a vertical blanking period or the contiguous lines in a field or frame. For the vertical blanking period case, the vertical blanking at the bottom of the previous field or frame combined with the vertical blanking at the top of the current field or frame is combined to create one period.

EOP tags the line as an endline in a period. Figure 9-52 shows the definition of the two types of Periods as outlined by BOP and EOP.

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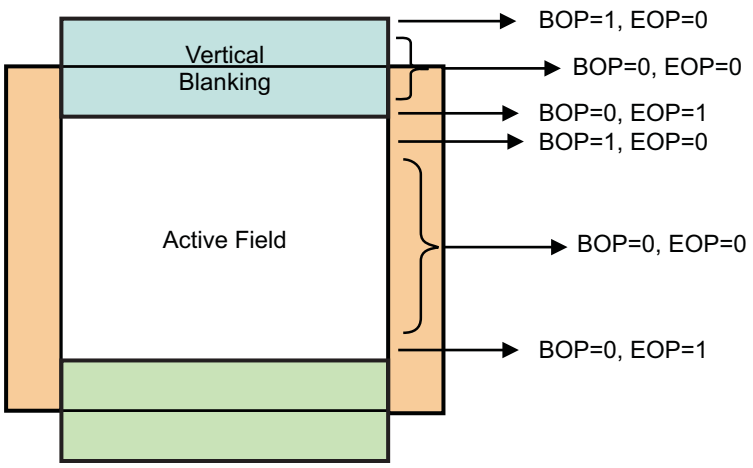
Figure 9-52. BOP/EOP Definition of a Period



For the Split Line at the top of a Period, the BOP bit is set for both halves of the split line. Likewise, for the Split Line at the bottom of a Period, the EOP bit is set for both halves of the split line.

CH_ID is the channel ID, which tags the camera source that generated the incoming line. A maximum of 16 camera sources are support per Pixel Input Clock Domain.

LINE_ID is the line number, starting from 0 and incrementing by one for each subsequent line from the same source.

PAD is a flag which tags the line as an artificially inserted padding line. When PAD is '0', the line should be discarded.

F, V, H, P3, P2, P1, and P0 are the bits representing the normal XY code. F is the Field ID associated with line, V signals when the line is in the vertical blanking, H specifies that the line is in the Horizontal Blanking, and P3:P0 are the protection bits.

Since only active video and vertical ancillary data lines are encapsulated in the Meta Data, the H bit in the SC0 byte should never be '1'.

9.4.5.8.10 TI Line Mux Mode, Split Lines, and Channel ID Remapping

The VIP_PARSER supports a maximum of 8 different Channel IDs per Port. The Channel IDs must be in the range {0:7} (3 bits). In the source multiplex, only one source can be a split line source and have the same Channel ID as one of the non-split line sources.

This scenario involves an external NTSC decoder which supports 8 D1 cameras. The external NTSC decoder will downscale the 8 sources to SIF format. However, one camera source will be sent in the multiplex as both the downscaled version and the original D1 sized version. They will both have the same Channel ID. However, the D1 version will be sent as a split-line. The source multiplex will thus have 9 maximum streams.

The VIP_PARSER (for TI Line Mux Mode only), will left shift the Channel ID by one. Bit 0 is used as an indicator whether the Source is a split-line source or a normal non-split line source. Only one of the nine inputs can be a split line source.

Table 9-16. TI Line Mux Mode Channel ID Remapping

	Channel ID Sent to VPDMA	
Source Input Channel ID	**Non-split Line**	**Split Line**
0x0	0x0	0x1
0x1	0x2	0x3
0x2	0x4	0x5
0x3	0x6	0x7
0x4	0x8	0x9

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Table 9-16. TI Line Mux Mode Channel ID Remapping (continued)

0x5	0xA	0xB
0x6	0xC	0xD
0x7	0xE	0xF

All subsequent references to the Camera Source, such as in a VPDMA return descriptor, will reference the remapped Channel ID.

The VIP_OUTPUT_PORT_A_SRC0_SIZE through VIP_OUTPUT_PORT_A_SRC15_SIZE registers for Port A, and VIP_OUTPUT_PORT_B_SRC0_SIZE through VIP_OUTPUT_PORT_B_SRC15_SIZE registers for Port B and the VIP_OUTPUT_PORT_A_SRC_FID and VIP_OUTPUT_PORT_B_SRC_FID status registers reflect the remapped Channel ID when the port is in TI Line Mux mode.

9.4.5.9 Channel ID Extraction for 2x/4x Multiplexed Source

9.4.5.9.1 Channel ID Extraction Overview

For 2-way and 4-way multiplexed source, the Channel ID is either embedded in the four protection bits inside the EAV/SAV code words or in the horizontal blanking pixel data. A configuration setting determines where the VIP_PARSER would search for the Channel ID.

9.4.5.9.2 Channel ID Embedded in Protection Bits for 2- and 4-Way Multiplexing

The four-bit channel ID is an identifier corresponding with the source number (camera) of the incoming video. As shown in Table 9-17, the Channel ID is placed in the code fourth byte of the EAV/SAV code words normally used for protection bits. With 4 bits, the maximum number of sources that can be defined in this range is 16. However, only Channel IDs in the range {0:7} are supported. Obviously, error correction cannot be performed on the FVH flags since the protection bits are no longer there.

Table 9-17. Channel ID Embedded in EAV/SAV

7 (fixed)	6 (F)	5 (V)	4 (H)	3 (ch_id[3])	2 (ch_id[2])	1 (ch_id[1])	0 (ch_id[0])	Description
1	0	0	0	Ch_id = {0:15}				SAV, Field 0, Active Video
1	0	0	1	Ch_id = {0:15}				EAV, Field 0, Horizontal Blanking
1	0	1	0	Ch_id = {0:15}				SAV, Field 0, Vertical Blanking
1	0	1	1	Ch_id = {0:15}				EAV, Field 0, Horizontal Blanking in Vertical Blanking Region
1	1	0	0	Ch_id = {0:15}				SAV, Field 1, Active Video
1	1	0	1	Ch_id = {0:15}				EAV, Field 1, Horizontal Blanking
1	1	1	0	Ch_id = {0:15}				SAV, Field 1, Vertical Blanking
1	1	1	1	Ch_id = {0:15}				EAV, Field 1, Horizontal Blanking in Vertical Blanking Region

9.4.5.9.3 Channel ID Embedded in Horizontal Blanking Pixel Data for 2- and 4-Way Multiplexing

In Horizontal Blanking and Vertical Blanking, non-ancillary data pixels should be Y=0x10 and Cb=Cr=0x80. When the Channel ID is embedded in the Horizontal Blanking for 2 and 4-way multiplexing, the lower nibbles of all Luma and Chroma pixels are replaced by the 4 bit Channel ID. This scenario is shown in Figure 9-53. The maximum number of values defined by this 4-bit range is 2^4 = 16. However, only Channel IDs in the range {0:7} are supported.

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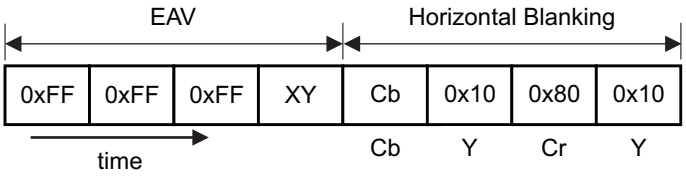
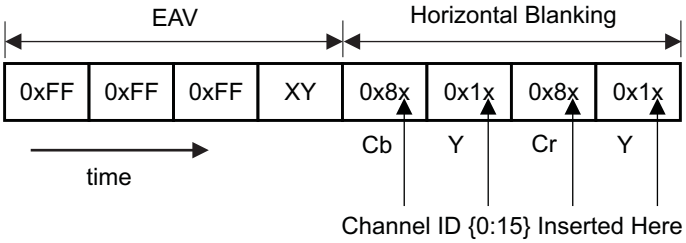
Figure 9-53. Channel ID Inserted Into Horizontal Blanking

Regular Horizontal Blanking Following EAV



Channel ID Inserted Into Horizontal Blanking Following EAV



9.4.5.10 Embedded Sync Mux Modes and Data Bus Widths

Legal combinations of Embedded Sync Mux Modes and Data Bus Widths are described in Table 9-18.

Table 9-18. Valid Embedded Sync Mux Mode and Data Bus Width Combinations

	1x Mux	2x Mux	4x Mux	Line Mux
8 Bit	v	v	v	v
16 Bit	v	n/a	n/a	v
24 Bit	v	n/a	n/a	n/a

9.4.5.11 Ancillary and Active Video Cropping

One Source Number for each Port can be cropped. Cropping is available for both Ancillary Data and Active Video.

For the Vertical Ancillary Data from Port A, cropping is enabled by setting the VIP_ANC_CROP_HORZ_PORT_A[15] ANC_BYPASS_N bit. The Source Number from Port A that gets cropped is defined by the VIP_ANC_CROP_HORZ_PORT_A[31:28] ANC_TARGET_SRCNUM register. VIP_ANC_CROP_HORZ_PORT_A[11:0] ANC_SKIP_NUMPIX, VIP_ANC_CROP_HORZ_PORT_A[27:16] ANC_USE_NUMPIX, VIP_ANC_CROP_VERT_PORT_A[11:0] ANC_SKIP_NUMLINES, and VIP_ANC_CROP_VERT_PORT_A[27:16] ANC_USE_NUMLINES define the region of the selected Source Number that is cropped and sent to DRAM. The Vertical Ancillary Data Cropping region is described in Figure 9-54.

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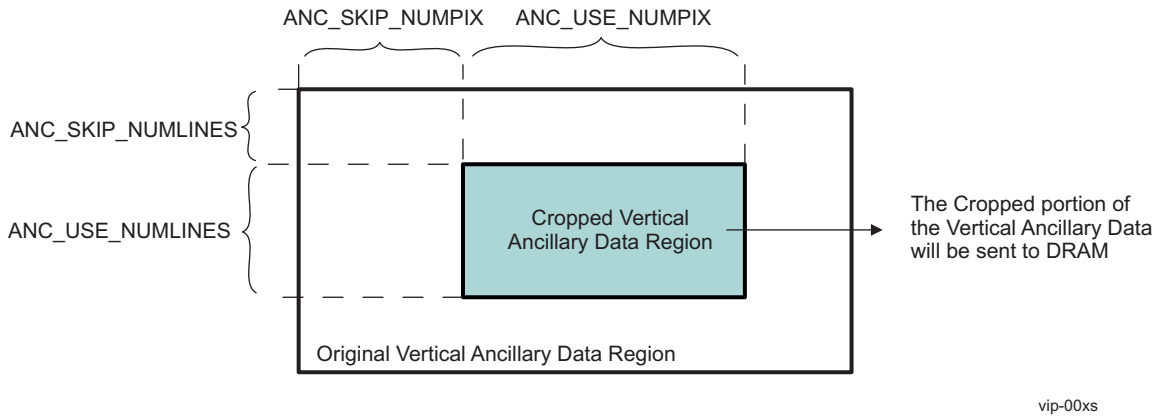
Figure 9-54. Vertical Ancillary Data Cropping

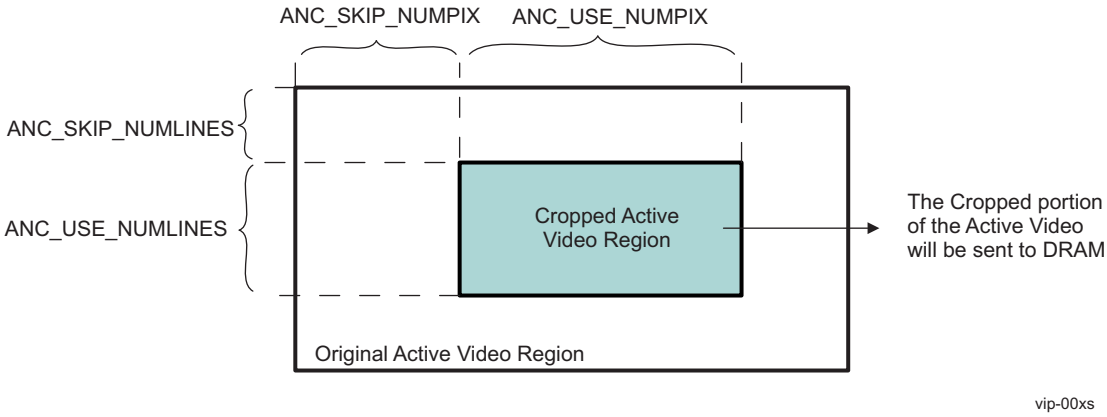


Note that for 8-bit input mode only, a setting exists that allow Vertical Ancillary data from both the Luma and Chroma channels to be captured. Both channels of Vertical Ancillary Data are captured when VIP_XTRA_PORT_A[14:13] ANC_CHAN_SEL_8B is set to “1x”. Thus, the number of data elements per line in this case is twice the equivalent number of Luma pixels per line. In other words, for this particular dual channel capture example, if there are 720 Luma pixels per line, then the total number of Vertical Ancillary Data Pixels in the source picture can be 2x720=1440 pixels.

For Active Video from Por tA, cropping is enabled by setting the VIP_CROP_HORZ_PORT_A[15] ACT_BYPASS_N bit. The Source Number from Port A that gets cropped is defined by the VIP_CROP_HORZ_PORT_A[31:28] ACT_TARGET_SRCNUM register.

VIP_CROP_HORZ_PORT_A[11:0] ACT_SKIP_NUMPIX, VIP_CROP_HORZ_PORT_A[27:16] ACT_USE_NUMPIX, VIP_CROP_VERT_PORT_A[11:0] ACT_SKIP_NUMLINES, and VIP_CROP_VERT_PORT_A[27:16] ACT_USE_NUMLINES define the region of the selected Source Number that is cropped and sent to DRAM. The Vertical Ancillary Data Cropping region is described in Figure 9-55

Figure 9-55. Active Video Cropping



Cropping for Port B works in a similar way to Port A. Since picture data is in 4:2:2 format, ANC_SKIP_NUMPIX(ACT_SKIP_NUMPIX) and ANC_USE_NUMPIX (ACT_USE_NUMPIX) must be evenly divisible by 2. If the output of VIP_PARSER is sent to a 4:2:2 to 4:2:0 converter, then ANC_USE_NUMLINES(ACT_USE_NUMLINES) must also be evenly divisible by 2.

Error cases in cropping occur when the crop window programmed is larger than the incoming video frame. Crop window errors normally result in the return of the crop region where the crop window overlays the incoming video frame. However, there is one problematic error cropping case, as illustrated in Figure 9-56.

The programmed crop window extends below the input picture and the last pixel of the input picture is not a part of the selected crop region. In this case, at the last pixel of the last line in the green crop output, there is no way to determine that this pixel is the last pixel of the cropped output.

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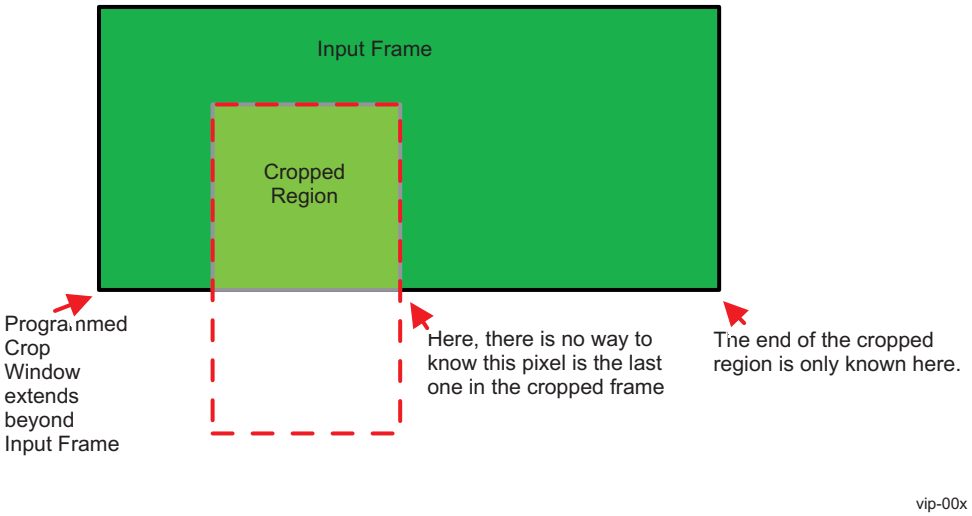
Figure 9-56. Problematic Error Cropping Case



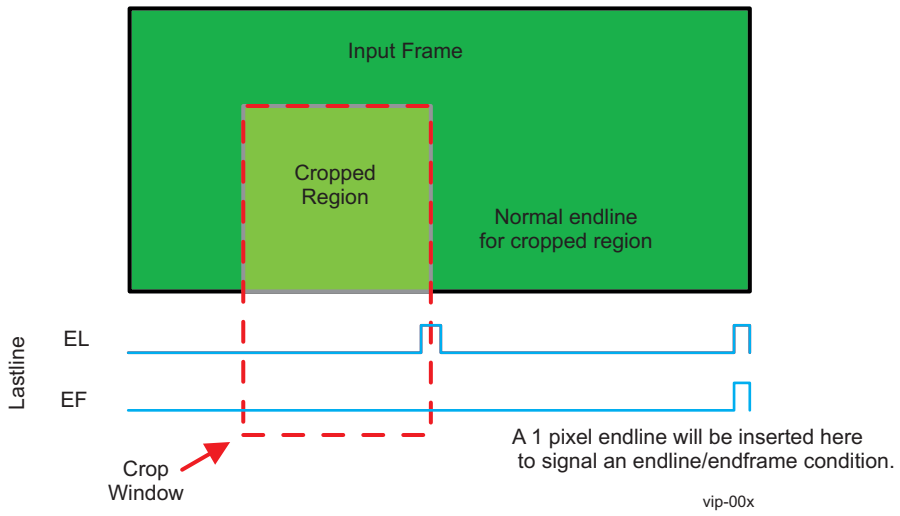
In this case, the crop tool sends outs a single pixel with an endline and endframe when it reaches the last pixel of the input picture. If the green cropped region has n lines, the actual output from the crop tool will have n+1 lines and the width of the last line will be 1 pixel.

Figure 9-57 shows the endline (EL) and endframe (EF) signals corresponding to the last line of the cropped region. At the last line and last pixel of the cropped region, the crop tool will only output an endline. It cannot output an endframe at this point because the crop tool might get another line from the streaming input.

Later, on the same input line, the last pixel of the input frame appears. Here, the crop tool knows that the cropped region has ended. In this case, a single endline/endframe pixel is sent out to signal that the frame has ended.

NOTE: There is no interrupt to notify that application level that a crop error has occurred.

Figure 9-57. Endline/Endframe Behavior for Error Cropping Case



9.4.5.12 Interrupts

The VIP_PARSER module has 19 interrupts out of which one can be mapped to VIP top level.

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When an interrupt occurs and is determined to be from the VIP_PARSER module, the VIP_PARSER level of masks, clears, and status registers must be checked and updated first.

Table 9-19 describes each of the interrupts events supported by the VIP_PARSER, together with associated Interrupt Mask (VIP_FIQ_MASK), Interrupt Clear (VIP_FIQ_CLEAR), and Interrupt Status (VIP_FIQ_STATUS) registers.

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Table 9-19. VIP_PARSER Interrupt Events

Event Flag	Event Mask	Map to	Description
VIP_FIQ_STATUS[21] PORT_A_YUV_PROTOCOL_VIOLATION	VIP_FIQ_MASK[21] PORT_A_YUV_PROTOCOL_VIOLATION_MASK	PrtBDisableComplete	When a port is running and VIP_PORT_B[8] ENABLE bit is turned off, logic exists to ensure that a complete frame is sent out of the Ancillary and Active Video VPI ports. That is, a frame is not stopped in the middle. This interrupt is activated when all active frames have been sent out Port B following a disable.
VIP_FIQ_STATUS[20] PORT_A_ANC_PROTOCOL_VIOLATION	VIP_FIQ_MASK[20] PORT_A_ANC_PROTOCOL_VIOLATION_MASK	PrtADisableComplete	When a port is running and VIP_PORT_A[8] ENABLE bit is turned off, logic exists to ensure that a complete frame is sent out of the Ancillary and Active Video VPI ports. That is, a frame is not stopped in the middle. This interrupt is activated when all active frames have been sent out Port A following a disable.
VIP_FIQ_STATUS[19] PORT_B_YUV_PROTOCOL_VIOLATION	VIP_FIQ_MASK[19] PORT_B_YUV_PROTOCOL_VIOLATION_MASK	PrtBANCProtocolVio	This interrupt is enabled when the protocol checker on the output of the VIP_PARSER encounters a violation on the Ancillary VPI of Port B.
VIP_FIQ_STATUS[18] PORT_B_ANC_PROTOCOL_VIOLATION	VIP_FIQ_MASK[18] PORT_B_ANC_PROTOCOL_VIOLATION_MASK	PrtBYUVProtocolVio	This interrupt is enabled when the protocol checker on the output of the VIP_PARSER encounters a violation on the Active Video VPI of Port B.
VIP_FIQ_STATUS[17] PORT_A_CFG_DISABLE_COMPLETE	VIP_FIQ_MASK[17] PORT_A_CFG_DISABLE_COMPLETE_MASK	PrtAANCProtocolVio	This interrupt is enabled when the protocol checker on the output of the VIP_PARSER encounters a violation on the Ancillary VPI of Port A.
VIP_FIQ_STATUS[16] PORT_B_CFG_DISABLE_COMPLETE_CLR	VIP_FIQ_MASK[16] PORT_B_CFG_DISABLE_COMPLETE_MASK	PrtAYUVProtocolVio	This interrupt is enabled when the protocol checker on the output of the VIP_PARSER encounters a violation on the Active Video VPI of Port A.
VIP_FIQ_STATUS[15] PORT_B_SRC0_SIZE_STATUS	VIP_FIQ_MASK[15] PORT_B_SRC0_SIZE	PrtBSrc0Size	The output size for Srcnum=0 on Port B differs from the XTRA_PORT_B[11:0] SRC0_NUMLINES and [27:16] SRC0_NUMPIX register settings
VIP_FIQ_STATUS[14] PORT_A_SRC0_SIZE_STATUS	VIP_FIQ_MASK[14] PORT_A_SRC0_SIZE	PrtASrc0Size	The output size for Srcnum=0 on Port A differs from the XTRA_PORT_B[11:0] SRC0_NUMLINES and [27:16] SRC0_NUMPIX register settings
VIP_FIQ_STATUS[13] PORT_B_DISCONN_STATUS	VIP_FIQ_MASK[13] PORT_B_DISCONN	PrtBDisconn	Port B Link Disconnect for Srcnum 0
VIP_FIQ_STATUS[12] PORT_B_CONN_STATUS	VIP_FIQ_MASK[12] PORT_B_CONN	PrtBConn	Port B Link Connect for Srcnum 0
VIP_FIQ_STATUS[11] PORT_A_DISCONN_STATUS	VIP_FIQ_MASK[11] PORT_A_DISCONN	PrtADisConn	Port A Link Disconnect for Srcnum 0
VIP_FIQ_STATUS[10] PORT_A_CONN_STATUS	VIP_FIQ_MASK[10] PORT_A_CONN	PrtAConn	Port A Link Connect for Srcnum 0
VIP_FIQ_STATUS[9] OUTPUT_FIFO_PRTB_ANC_STATUS	VIP_FIQ_MASK[9] OUTPUT_FIFO_PRTB_ANC_OF	OpPrtBAnc	Overflow at Ancillary Data VPDMA interface for the Port B
VIP_FIQ_STATUS[7] OUTPUT_FIFO_PRTB_LUMA_STATUS	VIP_FIQ_MASK[7] OUTPUT_FIFO_PRTB_YUV_OF	OpPrtBYUV	Overflow at Luma VPDMA interface for Port B

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Table 9-19. VIP_PARSER Interrupt Events (continued)

Event Flag	Event Mask	Map to	Description
VIP_FIQ_STATUS[6] OUTPUT_FIFO_PRTA_ANC_STATUS	VIP_FIQ_MASK[6] OUTPUT_FIFO_PRTA_ANC_OF	OpPrtAAnc	Overflow at Ancillary Data VPDMA interface for the Port A
VIP_FIQ_STATUS[4] OUTPUT_FIFO_PRTA_LUMA_STATUS	VIP_FIQ_MASK[4] OUTPUT_FIFO_PRTA_YUV_OF	OpPrtAYUV	Overflow at Luma VPDMA interface for Port A
VIP_FIQ_STATUS[3] ASYNC_FIFO_PRTB_STATUS	VIP_FIQ_MASK[3] ASYNC_FIFO_PRTB_OF	InPrtB	Overflow at Input Async FIFO for Port B
VIP_FIQ_STATUS[2] ASYNC_FIFO_PRTA_STATUS	VIP_FIQ_MASK[2] ASYNC_FIFO_PRTA_OF	InPrtA	Overflow at Input Async FIFO for Port A
VIP_FIQ_STATUS[1] PRTB_VDET_STATUS	VIP_FIQ_MASK[1] PRTB_VDET_MASK	PrtBVdet	Video Detect Interrupt for Port B
VIP_FIQ_STATUS[0] PRTA_VDET_STATUS	VIP_FIQ_MASK[0] PRTA_VDET_MASK	PrtAVdet	Video Detect Interrupt for Port A

A ‘1’ in the Status register associated with an Interrupt source shows that the interrupt source is pending. The Status register is read-only. To clear a bit in the Status register, the associated bit in the Clear register must be written with a ‘1.’

A ’1’ in the bit position of the Mask register associated with an Interrupt source ensures that the hardware interrupt will never be passed on to the VIP top level. A ‘0’ in the bit position of the Mask register associated with an Interrupt source will cause the interrupt controller to see a VIP_PARSER interrupt in the event the hardware in the parser triggers it.

A ‘1’ in the bit position of the Clear register associated with an Interrupt source clears the hardware interrupt status register until the next time the hardware triggers it. After a Clear, the CPU should set the bit back to a ‘0.’ Otherwise, the hardware would not be able to set any subsequent interrupts of the same type.

9.4.5.13 VDET Interrupt

For Line Multiplexing Embedded Sync mode only, the Meta Data Header includes a Video Detect (VDET) flag. The device sets this VDET flag whenever NTSC or PAL sync is found. Some other external devices using Line Multiplexing mode may not use VDET. However, when VDET changes, a VDET interrupt is issued (see Table 9-19, *Interrupts*, for more details on the interrupt). Each Pixel Clock Input Domain (Port A and Port B) has a separate VDET interrupt.

The VDET status register is comprised of 32 bits, each bit representing the value of the VDET flag found in the meta data of the Channel ID. Bit 0 is the VDET value from Channel ID 0, Bit 1is is VDET value from Channel ID 1, and so on. There is a separate status register for each Pixel Input Clock Domain (VIP_PORT_A_VDET_VEC and VIP_PORT_B_VDET_VEC registers).

In Line Mux mode, the meta-data field defining the srcnum is 5-bits wide. Only the last three bits of this field and the upper two bits are reserved. This bit should always be set to 1 in TI Line Mux mode.

9.4.5.14 Source Video Size

For each Pixel Input Clock Domain, status registers are available to log the last active video height and width found from 16 camera sources. There is no interrupt activated on the change in the source size in any of the input sources. These readonly registers only inform the application of the width and the height of the last active field or frame associated with each channel ID.

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In 2x/4x pixel multiplexing, the four bit nibble carrying the Srcnum defines a maximum of 16 sources.

9.4.5.15 Clipping

In ITU-656/BT.1120 embedded sync streams, the values 0x00 and 0xFF are reserved for sync detection. These values are illegal in the rest of the stream. Only when the ITU-1364 standard came out to for digitally inserted vertical blanking data structures did the 0x00 and 0xFF codes get re-used in the packet synchronization structure.

The VIP_PARSER supports one configuration bit that, when enabled, changes all 0x00 to 0x01 and 0xFF to 0xFE in the vertical ancillary data. Another configuration bit, when enabled, changes all 0x00 to 0x01 and 0xFF to 0xFE in the active video portion of the input picture.

Generally, clipping is only desired for discrete sync input data captured from a NTSC/PAL decoder type of device which does not follow pixel range rules. For Discrete Sync input, the possibility to clip inputs to legal values exists. Clipping is desired if the picture sent to DRAM will be streamed out of the IC again usin an ITU-656/BT.1120 style output port. If the picture is processed inside the SOC before it is streamed out, then the processing procedure or the output streaming hardware needs to ensure that illegal values are not in the stream.

For Embedded Sync input, illegal values should not exist except for the ITU-1364 data sync sequence 00-FF-FF. Otherwise, the VIP Parser cannot determine good EAV/SAV. In the hardware, clipping is allowed for Embedded Sync streams even though it is not particularly a useful feature.

Note that if the clipping is enabled for ancillary data, the post processing software will never be able to find a data packet sync header, since the 00-FF-FF sequence will be changed to 01-FE-FE.

For 24-bit YUV, clipping is done on each 8 bit channel. If data[23:16]==0xFF, the clipped value will be 0xFE. If data[23:16]==0x00, the clipped value will be 0x01. Likewise, clipping is done for data bit ranges 15:8 and 7:0

From a software point of view, clipping should never be enabled for 24-bit RGB. RGB should use the full 8-bit quantization range for each color component. The hardware, however, will clip RGB in active video, if VIP_MAIN[5] CLIP_ACTIVE='1'. The clipping will be done on each 8-bit channel as described for 24-bit YUV.

9.4.5.16 Current and Last FID Value

The FID values for the current field or frame are reported in the Status Registers. When a new field or frame enters, the current FID values are saved into the previous FID status registers and the new FID value is loaded into the current FID register.

Following a reset, the previous and current FID status registers are set to '1.' The first two fields or frames are ignored. On the third input field or frame after a reset, the previous FID is loaded with the current FID ('1'), and the current FID is loaded with the actual FID. By the fourth field or frame after a reset, both the previous and current FID values should represent the values found in the input stream.

The FID values are reported for each camera source in both Pixel Input Clock Domains.

9.4.5.17 Disable Handling

A feature was defined for the case of single stream (either discrete sync or embedded sync) input handling where VIP_PORT_A[8] ENABLE for Port A and VIP_PORT_B[8] ENABLE for Port B is taken inactive. The single stream case was deemed more important than the multi-stream one since the output of the VIP_PARSER may be used to drive the Scaler module. The Scaler needs to work on a frame boundary (startframe to endframe) or it may lock up without a reset. The goal of the disable handling for the single stream case is to complete a field or frame of output data to the downstream module. Then, upon enabling of the port again, the system should start up properly without a need to reset the individual modules within the VIP instance.

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In this scenario, suppose the VIP_PARSER has been processing a single input stream. Then, ENABLE is brought inactive. The VIP_PARSER will continue to output data downstream until it sends out an endframe pixel and the downstream module accepts the endframe pixel.

9.4.5.18 Picture Size Interrupt

Each VIP port can be set up to trigger an interrupt if the picture size varies from a pre-programmed expected picture size. This interrupt is supported only for the Active Video portion of the input video and not for the Vertical Ancillary portion. Also this interrupt is only support for source number 0 in multi channel capture.

The interrupts are named PrtASrc0Size and PrtBSrc0Size. They are described in Table 9-19, *VIP_PARSER Interrupt Events*

For Port A, the expected active video picture size values are programmed in VIP_XTRA_PORT_A[11:0] SRC0_NUMLINES and VIP_XTRA_PORT_A[27:16] SRC0_NUMPIX. For PortB, the expected active video picture size values are programmed in VIP_XTRA_PORT_B[11:0] SRC0_NUMLINES and VIP_XTRA_PORT_B[27:16] SRC0_NUMPIX.

NOTE: Picture Size Interrupt reflects the Active Video going into the DRAM. If cropping is enabled for Srcnum=0, the Picture Size is the post-cropped size.

9.4.5.19 Discrete Sync Signals

External ICs generally produce discrete sync interface signals seen in Figure 9-58.

VBLNKrepresents the vertical blanking interval. Generally, vertical blanking is at the top of a NTSC/PAL field. In certain standards, the last few lines of a field or frame are in vertical blanking in addition to the beginning few lines in the following field or frame.

VSYNC is the vertical sync indicator. VSYNC is active during a portion of the vertical blanking. For NTSC and PAL, since these standards define an odd number of lines for a field pair, VSYNC can be use in conjunction with HSYNC to determine FID polarity. Generally, VSYNC is defined to transition inactive to active sometime during vertical blanking. This signal then transitions to an inactive state before the end of vertical blanking. Certain standards define the line numbers where VSYNC transitions.

HBLNK is the horizontal blanking interval for each line. The horizontal blanking is the same number of pixels whether the line is in the active video region or in the vertical blanking region of the scan.

ACTVID is the region of a line that is active video. It is the inverse of the HBLNK signal. The number of pixels in the ACTVID region is the same for a line in vertical blanking as a line in active video. ACTVID(1) is a situation where the signal toggles in vertical blanking as well as active video. ACTVID(2) shows the signal toggling only in non-vertical blanking regions. Once ACTVID transitions active, it stays active for every PIXCLK until the end of the line.

HSYNC transitions from inactive to active for the first pixel of each line, which is a horizontal blanking pixel. HSYNC will transition to the inactive state before the end of the line. HSYNC is similar to HBLNK in that they both transition active on the same PIXCLK cycle. However, HBLNK transitions inactive at the end of the horizontal blanking period. HSYNC can transition inactive either before or after the horizontal blanking period.

Group 1 signals define the vertical separation between fields or frames. Group 2 signals define the separation between lines. One of the Group 1 signals can be tied to the VSYNC input. The ACTVID(1) and ACTVID(2) signals from Group 2 are tied to the ACTVID input. One of the other two Group 2 signals, HBLNK or HSYNC, can be tied to the HSYNC input.

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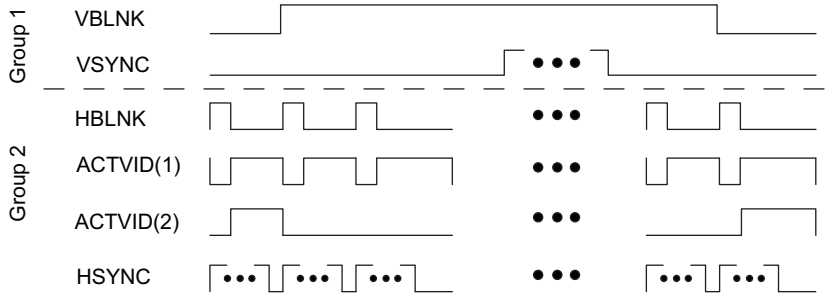
VIP_PORT_A[15] USE_ACTVID_HSYNC_N for Port A and VIP_PORT_B[15] USE_ACTVID_HSYNC_N for Port B defines whether the line separation method uses the signal from the ACTVID or the HSYNC input of the VIP_PARSER module.

VIP_PORT_A[22] DISCRETE_BASIC_MODE for Port A VIP_PORT_B[22] DISCRETE_BASIC_MODE for Port B determines whether discrete sync works as described in Section 9.4.5.6 *Input Data Interface* or whether a “basic mode” input handler is invoked.

By choosing one signal from Group 1 and one signal from Group 2, there should be a way to capture the external data.

Figure 9-58. Generic External Sync Signals



NOTE: 1. VIP_PARSER module defines three discrete sync control signals: ACTVID, HSYNC, and VSYNC.

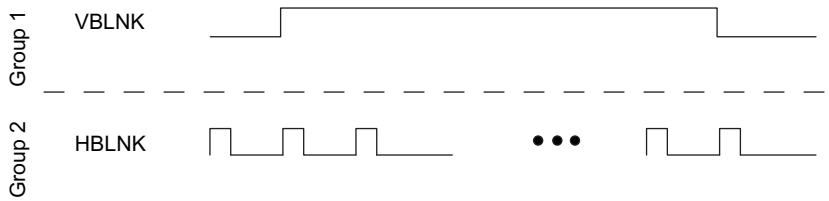
2. In order to capture external data PIXCLK must never stop, for either horizontal or vertical blanking.

9.4.5.19.1 VBLNK and HBLNK

Figure 9-59 shows VBLNK from Group 1 and HBLNK from Group 2 being used. In this case, set USE_ACTVID_HSYNC_N=’0’ and DISCRETE_BASIC_MODE=’0’. Vertical Ancillary lines will be sent to the Vertical Ancillary output at Active Video will be sent out the Active Video output.

If DISCRETE_BASIC_MODE=’1’ is chosen, all lines including vertical blanking ones will be sent to the Active Video buffer. Since a line is delineated by HBLNK and HBLNK toggles in vertical blanking as well as active video, every incoming pixel will be save to the Active Video buffer.

Figure 9-59. vblnk and hblnk



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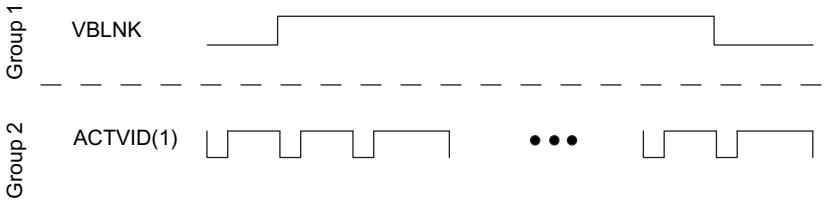
9.4.5.19.2 BLNK and ACTVID (1)

Figure 9-60 shows VBLNK from Group 1 and ACTVID(1) from Group 2 being used. ACTVID is toggling during Vertical Blanking. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='0'. Vertical Ancillary lines will be sent to the Vertical Ancillary output and Active Video will be sent out the Active Video output.

If DISCRETE_BASIC_MODE='1' is chosen, all lines will be sent to the Active Video output.

Figure 9-60. VBLNK and ACTID (1)

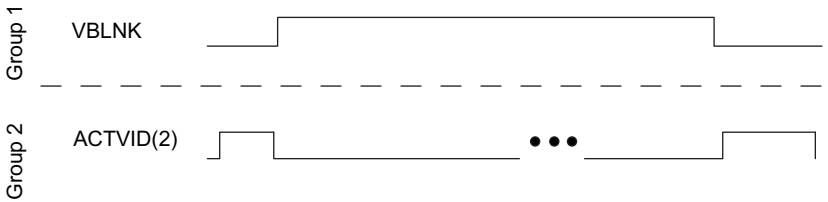


9.4.5.19.3 VBLNK and ACTVID(2)

Figure 9-61 shows VBLNK from Group 1 and ACTVID(2) from Group 2 being used. ACTVID is not toggling during Vertical Blanking. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='1'. Since there are no line sync/clocking signals in the Vertical Blanking period, only Active Video lines will be sent to the Active Video output.

If DISCRETE_BASIC_MODE='0' is set, then the hardware will lock up as there is no way for it to determine a frame boundary.

Figure 9-61. VBLNK and ACTVID(2)



9.4.5.19.4 VBLNK and HSYNC

Figure 9-62 shows VBLNK from Group 1 and HSYNC from Group 2 being used. In this scenario, set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODEN='0'. Vertical Ancillary lines will be sent to the Vertical Ancillary output at Active Video will be sent out the Active Video output.

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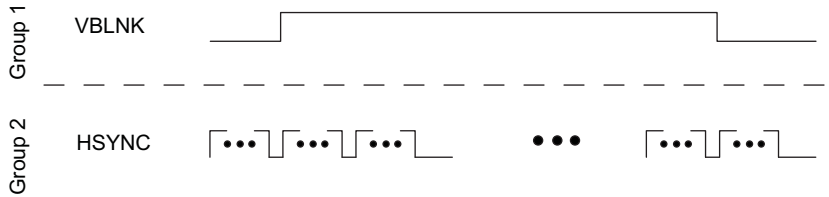
Figure 9-62. VBLNK and HSYNC



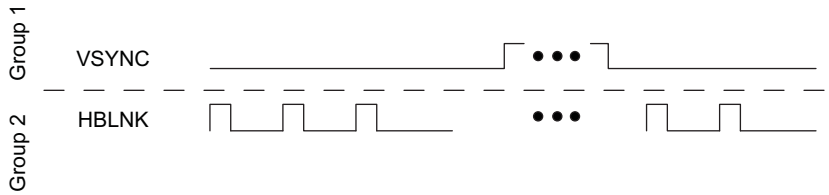
9.4.5.19.5 VSYNC and HBLNK

Figure 9-63 shows VSYNC from Group 1 and HBLINK from Group 2 being used. Set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='1'.

Also, no automatic parsing of vertical ancillary data will be performed so the Ancillary VPI port to the VPDMA should be disabled. All lines, including both vertical ancillary and active video, will appear in the Video DRAM buffer. Lines starting after an inactive to active transition on VSYNC will delineate a start of frame. Every data element strobed on the Pixel clock's active edge will be stored in the Active Video Buffer.

In Figure 9-63, it is likely the HBLINK will toggle when VSYNC is active. In this case, setting USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='0' mean that those lines appearing under the active VSYNC will be sent to the Ancillary Data Buffer. All other captured lines will be sent to the Active Video Buffer.

Figure 9-63. VSYNC and HBLNK



9.4.5.19.6 VSYNC and ACTIVID(1)

Figure 9-64 shows VSYNC from Group 1 and ACTIVID(1) from Group 2 being used. ACTIVID is toggling during the VBLNK interval. ACTIVID does not necessarily toggle during VSYNC. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='1'.

Also, no automatic parsing of vertical ancillary data will be performed so there is no activity on the Ancillary VPI port to the VPDMA. All lines, including both vertical ancillary and active video, will appear in the Video DRAM buffer. Lines starting after an inactive to active transition on VSYNC will delineate a start of frame. Lines are denoted by an inactive to active transition of ACTIVID. Only those pixels gated by an active ACTIVID will be saved.

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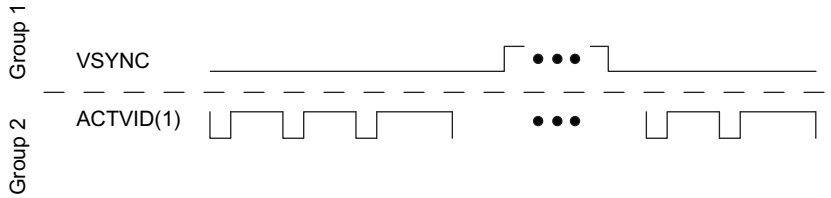
Figure 9-64. VSYNC and ACTIVID(1)

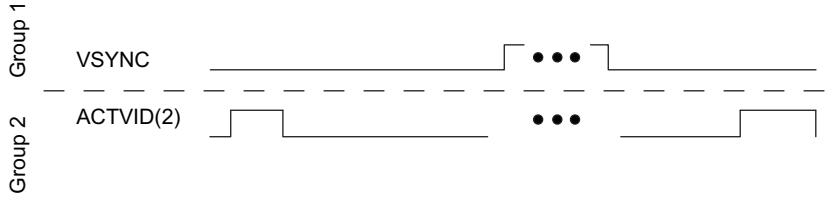


9.4.5.19.7 VSYNC and ACTIVID(2)

Figure 9-65 shows VSYNC from Group 1 and ACTIVID(2) from Group 2 being used. ACTIVID is not toggling during the entire VBLNK interval. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='1'.

Also, no automatic parsing of vertical ancillary data will be performed so the the Ancillary VPI port to the VPDMA should be turned off. All active video lines, since there are no vertical ancillary data lines, will appear in the Video DRAM buffer. Lines starting after an inactive to active transition on VSYNC will delineate a start of frame. Lines are denoted by an inactive to active transition of ACTIVID. Once a line starts, ACTIVID stays active for every pixel clock until the end of the line. Only those pixels gated by an active ACTIVID will be saved.

Figure 9-65. VSYNC and ACTIVID(2)



9.4.5.19.8 VSYNC and HSYNC

Figure 9-66 shows VSYNC from Group 1 and HSYNC from Group 2 being used. Set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='1'.

In the event that the machine is set to DISCRETE_BASIC_MODE='0', lockup will not occur as long as there is an HSYNC active transition during the time that VSYNC is active. This scenario is likely. However, if there is not at least one such transition on HSYNC, then the machine experiences a lock up. It cannot distinguish the end of one frame from the start of the next frame.

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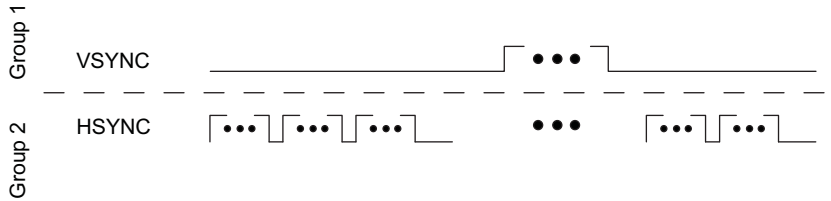
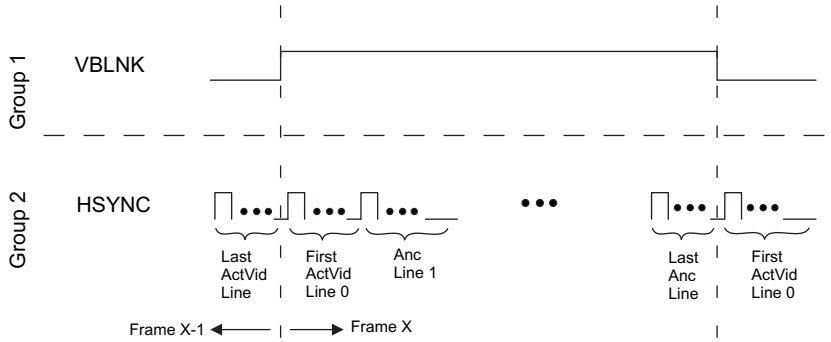
Figure 9-66. VSYNC and HSYNC



9.4.5.19.9 Line and Pixel Capture Examples

When DISCRETE_BASIC_MODE='0', VBLNK is generally used. All the lines where the start of line is under an active VBLNK are sent to the Ancillary Data buffer. All the lines where the start of line is not under an active VBLNK are sent to the Active Video framebuffer. This situation is shown in Figure 9-67.

Figure 9-67. Ancillary and Active Video Line Determination



The start of line is the pixel represented by the inactive to active transition on HSYNC when USE_ACTVID_HSYNC_N = '1'. Figure 9-68 illustrates the delineation of a line when using USE_ACTVID_HSYNC_N = '1.'

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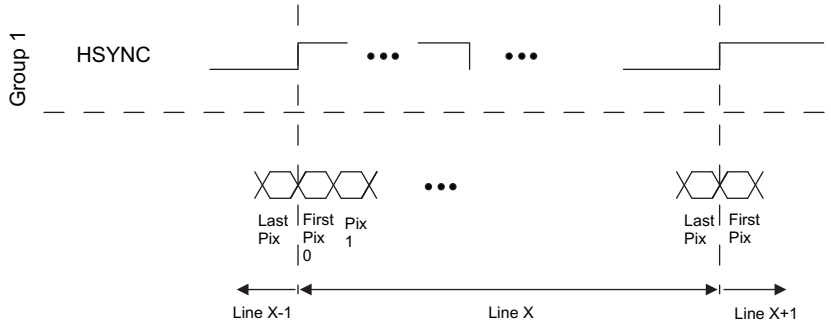
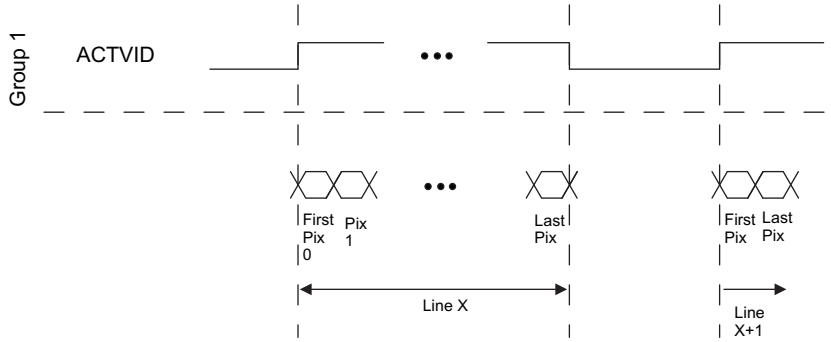
Figure 9-68. HSYNC Pixel Capture



The start of line is the pixel represented by the inactive to active transition on ACTVID when USE_ACTVID_HSYNC_N = '0.' Note that ACTVID stays active for the entire duration of active video portion of the line. This scenario is shown in Figure 9-69

Figure 9-69. ACTVID Pixel Capture



In 8-bit mode, the 4:2:2 YUV input color component order is Cb, Y followed by Cr and Y. For 16-bit and 24-bit input modes, all the components are sent in the same cycle.

9.4.5.20 VIP Overflow Detection and Recovery

It is possible that an overflow can occur in the VIP_PARSER. Overflow detection is determined by reading the VIP_FIQ_STATUS register and checking for bits 8, 7, 5, 4, 3 and 2. If video is being captured, and any of these bits are set, it indicates that not all of the incoming video data was sent to DDR meory. VIP overflow can be caused by one of the following:

1. External pixel clock is faster than processing clock
2. DDR bandwidth is temporarily over-consumed
3. VIP scaler is being used inline with external video input, and is upscaling.

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- VIP scaler in this use case can only be used for downscaling

4. VIP scaler is being used inline with external video input, but has not been configured with scaler coefficients

- VIP scaler will not accept video input if it is not first configured with scaler coefficients. This will cause overflow

5. VIP scaler is being used inline, but has not been enabled

6. External cables are connected or disconnected while the system is running, resulting in corrupted video streams going into the VIP

7. Bad external video cable, which causes corrupted video streams going into the VIP

Items 6 and 7 above are typically seen as noise events, where it is likely that multiple horizontal syncs per line and/or multiple vertical syncs per frame will be observed. These result in high peak throughput requirements, leading to DDR bandwidth being temporarily over-consumed, and thus VIP overflow.

The high level recovery method for VIP overflow on Port A is outlined in the steps below. Port B is similar.

1. Set VIP_XTRA6_PORT_A[31:16] YUV_SRCNUM_STOP_IMMEDIATELY = 0xFFFF_FFFF
2. Set VIP_XTRA6_PORT_A[15:0] ANC_SRCNUM_STOP_IMMEDIATELY = 0xFFFF_FFFF
3. Set VIP_PORT_A[8] ENABLE = 0
4. Set VIP_PORT_A[7] CLR_ASYNC_FIFO_RD and VIP_PORT_A[6] CLR_ASYNC_FIFO_WR to 1
5. Set VIP_PORT_A[23] SW_RESET to 1
6. Reset other VIP modules
   - For each module used downstream of VIP_PARSER, write 1 to the bit location of the VIP_CLKC_RST register which is connected to VIP_PARSER
7. Abort VPDMA channels
   - Write to list attribute to stop list 0
   - Write to list address register location of abort list
   - Write to list attribute register list 0 and size of abort list
8. Set VIP_PORT_A[23] SW_RESET to 0
9. Un-reset other VIP modules
   - For each module used downstream of VIP_PARSER, write 0 to the bit location of the VIP_CLKC_RST register which is connected to VIP_PARSER
10. (Delay)
11. SC coeff downloaded (if VIP_SCALER is being used)
12. (Delay)
13. Set VIP_XTRA6_PORT_A[31:16] YUV_SRCNUM_STOP_IMMEDIATELY = 0x0000_0000
14. Set VIP_XTRA6_PORT_A[15:0] ANC_SRCNUM_STOP_IMMEDIATELY = 0x0000_0000

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15. Set VIP_PORT_A[8] ENABLE = 1
16. Set VIP_PORT_A[7] CLR_ASYNC_FIFO_RD and VIP_PORT_A[6] CLR_ASYNC_FIFO_WR to 0

9.4.6 VIP Color Space Converter (CSC)

The Color Space Converter (CSC) module is used to convert video data from one color space to another with nine programmable integer multipliers.

9.4.6.1 CSC Features

- All parameters are programmable
- Each parameter is configurable in signed 13-bits
- Support for Bypass Mode

9.4.6.2 CSC Functional Description

The conversion between the different color spaces requires addition and multiplication operations on color and intensity components. The mathematical expression of the conversion can be written as:

```
Y   = A0*R + B0*G + C0*B + D0
Cb  = A1*R + B1*G + C1*B + D1
Cr  = A2*R + B2*G + C2*B + D2
```

Color space coeficients are set through the following registers:

- For luma component:
  - VIP_CSC00[12:0] A0
  - VIP_CSC00[28:16] B0
  - VIP_CSC01[28:16] C0
  - VIP_CSC04[27:16] D0
- For Cb component:
  - VIP_CSC01[28:16] A1
  - VIP_CSC02[12:0] B1
  - VIP_CSC02[27:16] C1
  - VIP_CSC05[11:0] D1
- For Cr component :
  - VIP_CSC03[12:0] A2
  - VIP_CSC03[27:16] B2
  - VIP_CSC04[12:0] C2
  - VIP_CSC05[27:16] D2

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Using YUV to RGB conversion as an example: YUV represents one color space and RGB represents another color space. The conversion can be written in the matrix format shown in Figure 9-70.

Figure 9-70. Matrix Format

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} A0 & B0 & C0 \\ A1 & B1 & C1 \\ A2 & B2 & C2 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} D0 \\ D1 \\ D2 \end{bmatrix}$$

Since HDTV and SDTV have different conversion requirements, both conversions of RGB-to-YCbCr and YCbCr-to-RGB are described. The details of derivations of these matrixes will be given in the following subsections.

9.4.6.2.1 HDTV Application

9.4.6.2.1.1 HDTV Application with Video Data Range

The two equations presented in this section are for the HDTV application. The chromaticity parameters are defined by ITU-R709 standard.

The input video data for these equations should be within the range that is defined for video application.

In an 8-bit system:

- Rd, Gd, Bd, and Yd will be in the range [16-235]
- Cb and Cr will be the range [16-240]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, and Yd will be in the range [64-940]
- Cb and Cr will be in the range [64-960]
- D = 4

Conversion from RGB to YCbCr:

Figure 9-71. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.2126 & 0.7152 & 0.0722 \\ -0.1172 & -0.3942 & 0.5114 \\ 0.5114 & -0.4646 & -0.0468 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} D$$

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Conversion from YCbCr to RGB:

Figure 9-72. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.5396 \\ 1 & -0.1831 & -0.4577 \\ 1 & 1.8142 & 0 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -197 \\ 82 \\ -232 \end{bmatrix} D$$

9.4.6.2.1.2 HDTV Application with Graphics Data Range

The two equations presented in this section are for the HDTV application with graphics range data input. The main application is for computer graphics display. The chromaticity parameters are defined by ITU-R709 standard.

The input data ranges for these equations are as follows.

In an 8-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be the range [0-255]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be in the range [0-1023]
- D = 4

Conversion from RGB to YCbCr:

Figure 9-73. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.1826 & 0.6142 & 0.0620 \\ -0.1006 & -0.3385 & 0.4392 \\ 0.4392 & -0.3990 & -0.0402 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

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Figure 9-74. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1.1644 & -0.0003 & 1.7927 \\ 1.1644 & -0.2132 & -0.5329 \\ 1.1642 & 2.1125 & -0.0001 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -248 \\ 77 \\ -289 \end{bmatrix} D$$

9.4.6.2.1.3 Quantized Coefficients for Color Space Converter in HDTV

This section quantizes all the coefficients of color space conversion based on a 10-bit system for HDTV application. These coefficients can be input to the registers of programmable color space converter. Refer to register section for the corresponding register setting.

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Table 9-20. Quantized Coefficients of HDTV Application with Video Data Range

Conversion from RGB to YCbCr					Conversion from YCbCr to RGB			
Coefficient Names	Registers	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	VIP_CSC00[12:0] A0	0.2126	218	0x00DA	A0(13-bit)	1	1024	0x0400
B0(13-bit)	VIP_CSC00[28:16] B0	0.7152	732	0x02DC	B0(13-bit)	0	0	0x0000
C0(13-bit)	VIP_CSC01[28:16] C0	0.0722	74	0x004A	C0(13-bit)	1.5396	1577	0x0629
A1(13-bit)	VIP_CSC01[28:16] A1	-0.1172	-120	0x1F88	A1(13-bit)	1	1024	0x0400
B1(13-bit)	VIP_CSC02[12:0] B1	-0.3942	-404	0x1E6C	B1(13-bit)	-0.1831	-187	0x1F45
C1(13-bit)	VIP_CSC02[27:16] C1	0.5114	524	0x020C	C1(13-bit)	-0.4577	-469	0x1E2B
A2(13-bit)	VIP_CSC03[12:0] A2	0.5114	524	0x020C	A2(13-bit)	1	1024	0x0400
B2(13-bit)	VIP_CSC03[27:16] B2	-0.4646	-476	0x1E24	B2(13-bit)	1.8142	1858	0x0742
C2(13-bit)	VIP_CSC04[12:0] C2	-0.0468	-48	0x1FD0	C2(13-bit)	0	0	0x0000
D0(12-bit)	VIP_CSC04[27:16] D0	0	0	0x000	D0(12-bit)	-197	-788	0xCEC
D1(12-bit)	VIP_CSC05[11:0] D1	128	512	0x200	D1(12-bit)	82	328	0x148
D2(12-bit)	VIP_CSC05[27:16] D2	128	512	0x200	D2(12-bit)	-232	-928	0xC60

Table 9-21. Quantized Coefficients of HDTV Application with Graphics Data Range

Conversion from RGB to YCbCr					Conversion from YCbCr to RGB			
Coefficient Names	Registers	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	VIP_CSC00[12:0] A0	0.1826	187	0x00BB	A0(13-bit)	1.1644	1192	0x04A8
B0(13-bit)	VIP_CSC00[28:16] B0	0.6142	629	0x0275	B0(13-bit)	-0.0003	0	0x0000
C0(13-bit)	VIP_CSC01[28:16] C0	0.062	63	0x003F	C0(13-bit)	1.7927	1836	0x072C
A1(13-bit)	VIP_CSC01[28:16] A1	-0.1006	-103	0x1F99	A1(13-bit)	1.1644	1192	0x04A8
B1(13-bit)	VIP_CSC02[12:0] B1	-0.3385	-347	0x1EA5	B1(13-bit)	-0.2132	-218	0x1F26
C1(13-bit)	VIP_CSC02[27:16] C1	0.4392	450	0x01C2	C1(13-bit)	-0.5329	-546	0x1DDE
A2(13-bit)	VIP_CSC03[12:0] A2	0.4392	450	0x01C2	A2(13-bit)	1.1642	1192	0x04A8
B2(13-bit)	VIP_CSC03[27:16] B2	-0.399	-409	0x1E67	B2(13-bit)	2.1125	2163	0x0873
C2(13-bit)	VIP_CSC04[12:0] C2	-0.0402	-41	0x1FD7	C2(13-bit)	-0.0001	0	0x0000
D0(12-bit)	VIP_CSC04[27:16] D0	16	64	0x040	D0(12-bit)	-248	-992	0xC20
D1(12-bit)	VIP_CSC05[11:0] D1	128	512	0x200	D1(12-bit)	77	308	0x134
D2(12-bit)	VIP_CSC05[27:16] D2	128	512	0x200	D2(12-bit)	-289	-1156	0xB7C

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9.4.6.2.2 SDTV Application

9.4.6.2.2.1 SDTV Application with Video Data Range

The two equations presented in this section are for the SDTV application. The chromaticity parameters are defined by ITU-R601 standard.

The input video data for these equations should be within the range that is defined for video application.

In an 8-bit system:

- Rd, Gd, Bd, and Yd will be in the range [16-235]
- Cb and Cr will be the range [16-240]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, and Yd will be in the range [64-940]
- Cb and Cr will be in the range [64-960]
- D = 4

Conversion from RGB to YCbCr:

Figure 9-75. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.172 & -0.339 & 0.511 \\ 0.511 & -0.428 & -0.083 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 9-76. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1 & -0.0003 & 1.3717 \\ 1 & -0.3365 & -0.6984 \\ 1 & 1.7336 & -0.0016 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -176 \\ 132 \\ -222 \end{bmatrix} D$$

9.4.6.2.2.2 SDTV Application with Graphics Data Range

The two equations presented in this section are for the SDTV application with graphics range data input. The main application is for computer graphics display. The chromaticity parameters are defined by ITU-R601 standard.

The input data ranges for these equations are as following.

In an 8-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be the range [0-255]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be in the range [0-1023]
- D = 4

Conversion from RGB to YCbCr:

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Figure 9-77. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.257 & 0.504 & 0.098 \\ -0.148 & -0.291 & 0.439 \\ 0.439 & -0.368 & -0.071 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 9-78. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1.1641 & -0.0018 & 1.5958 \\ 1.1641 & -0.3914 & -0.8135 \\ 1.1641 & 2.0178 & -0.0012 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -223 \\ 136 \\ -277 \end{bmatrix} D$$

9.4.6.2.2.3 Quantized Coefficients for Color Space Converter in SDTV

This section quantizes all the coefficients of color space conversion based on a 10-bit system for SDTV application. These coefficients can be input to the registers of programmable color space converter. Refer to register section for the corresponding register setting.

Table 9-22. Quantized Coefficients of SDTV Application with Video Data Range

Conversion from RGB to YCbCr					Conversion from YCbCr to RGB			
Coefficient Names	Registers	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	VIP_CSC00[12:0] A0	0.299	306	0x0132	A0(13-bit)	1	1024	0x0400
B0(13-bit)	VIP_CSC00[28:16] B0	0.587	601	0x0259	B0(13-bit)	-0.0003	0	0x0000
C0(13-bit)	VIP_CSC01[28:16] C0	0.114	117	0x0075	C0(13-bit)	1.3717	1405	0x057D
A1(13-bit)	VIP_CSC01[28:16] A1	-0.172	-176	0x1F50	A1(13-bit)	1	1024	0x0400
B1(13-bit)	VIP_CSC02[12:0] B1	-0.339	-347	0x1EA5	B1(13-bit)	-0.3365	-345	0x1EA7
C1(13-bit)	VIP_CSC02[27:16] C1	0.511	523	0x020B	C1(13-bit)	-0.6984	-715	0x1D35
A2(13-bit)	VIP_CSC03[12:0] A2	0.511	523	0x020B	A2(13-bit)	1	1024	0x0400
B2(13-bit)	VIP_CSC03[27:16] B2	-0.428	-438	0x1E4A	B2(13-bit)	1.7336	1775	0x06EF
C2(13-bit)	VIP_CSC04[12:0] C2	-0.083	-85	0x1FAB	C2(13-bit)	-0.0016	-2	0x1FFE
D0(12-bit)	VIP_CSC04[27:16] D0	0	0	0x000	D0(12-bit)	-176	-704	0xD40
D1(12-bit)	VIP_CSC05[11:0] D1	128	512	0x200	D1(12-bit)	132	528	0x210
D2(12-bit)	VIP_CSC05[27:16] D2	128	512	0x200	D2(12-bit)	-222	-888	0xC88

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Table 9-23. Quantized Coefficients of SDTV Application with Graphics Data Range

Conversion from RGB to YCbCr					Conversion from YCbCr to RGB			
Coefficient Names	Registers	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	VIP_CSC00[12:0] A0	0.257	263	0x0107	A0(13-bit)	1.1641	1192	0x04A8
B0(13-bit)	VIP_CSC00[28:16] B0	0.504	516	0x0204	B0(13-bit)	-0.0018	-2	0x1FFE
C0(13-bit)	VIP_CSC01[28:16] C0	0.098	100	0x0064	C0(13-bit)	1.5958	1634	0x0662
A1(13-bit)	VIP_CSC01[28:16] A1	-0.148	-152	0x1F68	A1(13-bit)	1.1641	1192	0x04A8
B1(13-bit)	VIP_CSC02[12:0] B1	-0.291	-298	0x1ED6	B1(13-bit)	-0.3914	-401	0x1E6F
C1(13-bit)	VIP_CSC02[27:16] C1	0.439	450	0x01C2	C1(13-bit)	-0.8135	-833	0x1CBF
A2(13-bit)	VIP_CSC03[12:0] A2	0.439	450	0x01C2	A2(13-bit)	1.1641	1192	0x04A8
B2(13-bit)	VIP_CSC03[27:16] B2	-0.368	-377	0x1E87	B2(13-bit)	2.0178	2066	0x0812
C2(13-bit)	VIP_CSC04[12:0] C2	-0.071	-73	0x1FB7	C2(13-bit)	-0.0012	-1	0x1FFF
D0(12-bit)	VIP_CSC04[27:16] D0	16	64	0x040	D0(12-bit)	-223	-892	0xC84
D1(12-bit)	VIP_CSC05[11:0] D1	128	512	0x200	D1(12-bit)	136	544	0x220
D2(12-bit)	VIP_CSC05[27:16] D2	128	512	0x200	D2(12-bit)	-277	-1108	0xBAC

9.4.6.3 CSC Bypass Mode

CSC module can be bypassed by setting VIP_CSC05[28] BYPASS bit-field to 1.

9.4.7 VIP Scaler (SC)

This section describes the highly optimized video resizers, SC (scalers), in the VIP modules.

9.4.7.1 SC Features

- Independent vertical and horizontal up and down scaling
- Running average vertical down scaling for memory optimization
- Decimation and polyphase filtering for horizontal scaling
- Non-linear scaling for stretched/compressed left and right sides
- Input image trimmer for pan/scan support
- Pre-scaling peaking filter for enhanced sharpness
- Scale field as frame
- Interlacing of scaled output
- Full 1080p input and output support
- YCbCr422 input and output
- Maximum horizontal scaling ratio only limited by output line buffer (2047 pixels)
- Scaling filter Coefficient memory download via VPI (Video Port Interface) Control interface

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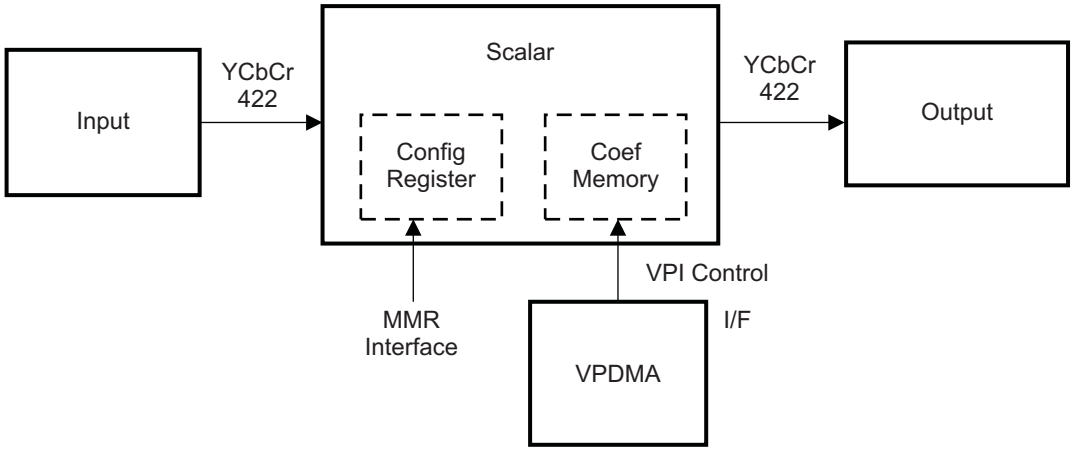
9.4.7.2 SC Functional Description

Scaler takes in a 10-bit YCbCr 422 video frame from an upstream module, performs vertical/horizontal scaling and outputs a YCbCr422 scaled image to a next downstream module. All configurations are done via the MMR interface except for the scaler coefficient memory configuration that is done via the common VPI control interface bus by VPDMA. Figure 9-79 shows the high-level block diagram of the scaler module.

Figure 9-79. High Level Block Diagram

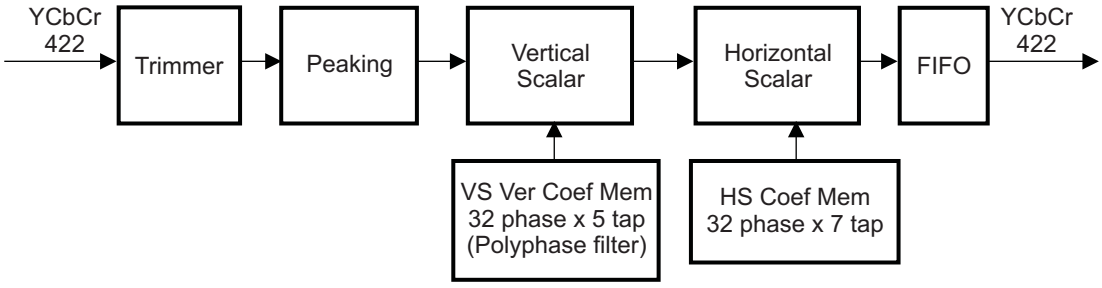


The SC is used in the video path and in all other video write-back data paths in the VIP module.

Scaling is performed in following three steps:

1. Trimming and Pre-peaking filtering
2. Vertical Scaling (Polyphase/Running Average Filter)
3. Horizontal polyphase scaling

Figure 9-80. SC Block Diagram



9.4.7.2.1 Trimmer

The trimmer can be programmed to re-define a new source image within the input video frame sent from an upstream module before it is sent to the scaling sub-modules. This feature enables small area zoom out, source pan/scan, or removal of unwanted area in the video (such as black box / curtains / noisy line-21 video) without modifying the VPDMA parameters.

Horizontal and vertical offset is set through VIP_CFG_SC25[26:16] CFG_OFF_W and VIP_CFG_SC25[10:0] CFG_OFF_H registers.

Width and height are set through VIP_CFG_SC24[26:16] CFG_ORG_W and VIP_CFG_SC24[10:0] CFG_ORG_H registers.

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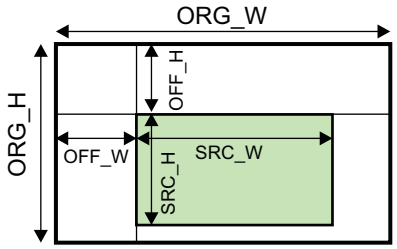
Figure 9-81. Input Image Trimming



NOTE: Width and height of the source image are global parameters and are set with VIP_CFG_SC5[22:12] CFG_SRC_W and VIP_CFG_SC5[10:0] CFG_SRC_H registers.

It is required that the input image frame (CFG_SRC_W x CFG_SRC_H) to be at least 32 × 32 (after trimming, if the trimming is enabled) to properly fill the input filter stage pipelines.

9.4.7.2.2 Peaking

The peaking block increases the amplitude of high frequency luminance information in horizontal direction to increase the sharpness of a video image before it is scaled. As shown in Figure 9-82, the high-frequency luminance is increased using an 11-tap High-Pass filter with adjustable gain. The non-linear coring function removes low-level noise and the modified luminance is then added to the original luminance signal. The implementation details are shown in Figure 9-82.

Figure 9-82. Filter Implementation and Parameter Description

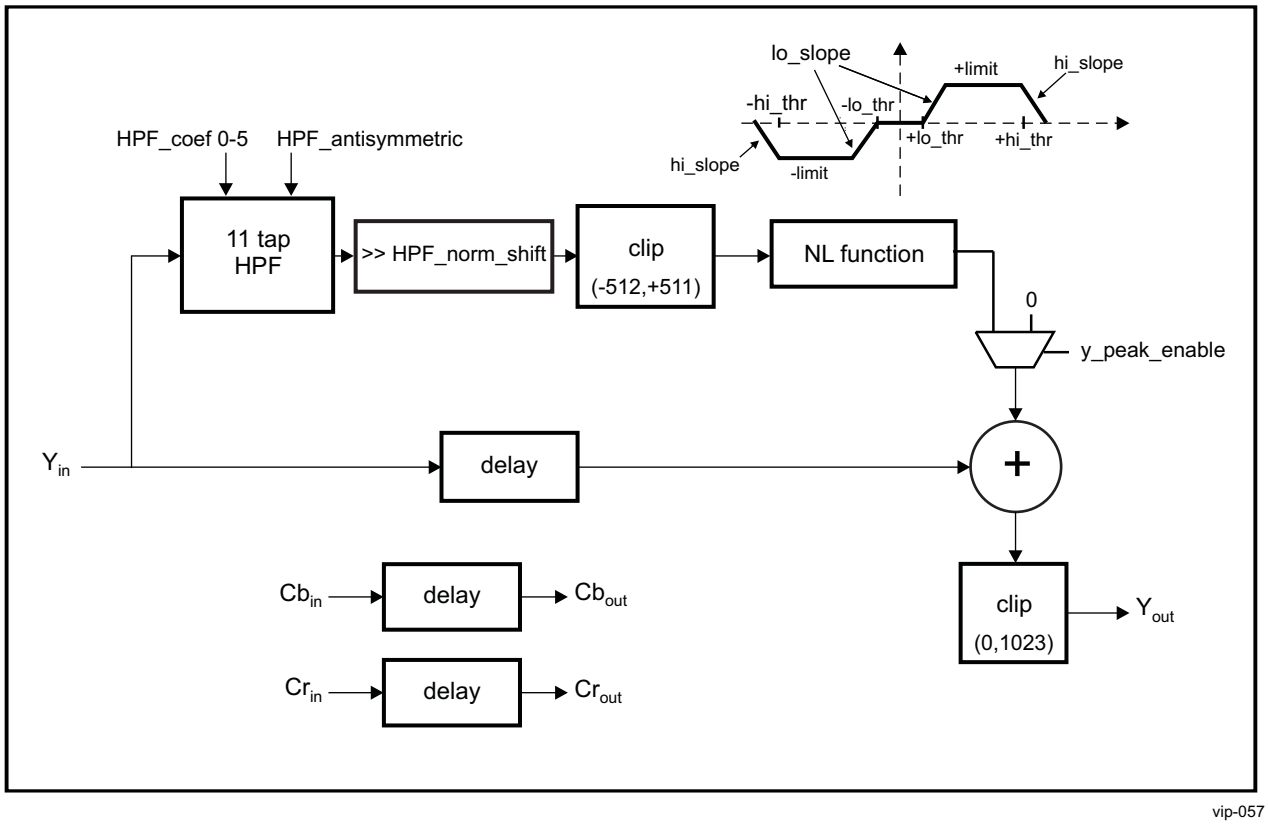


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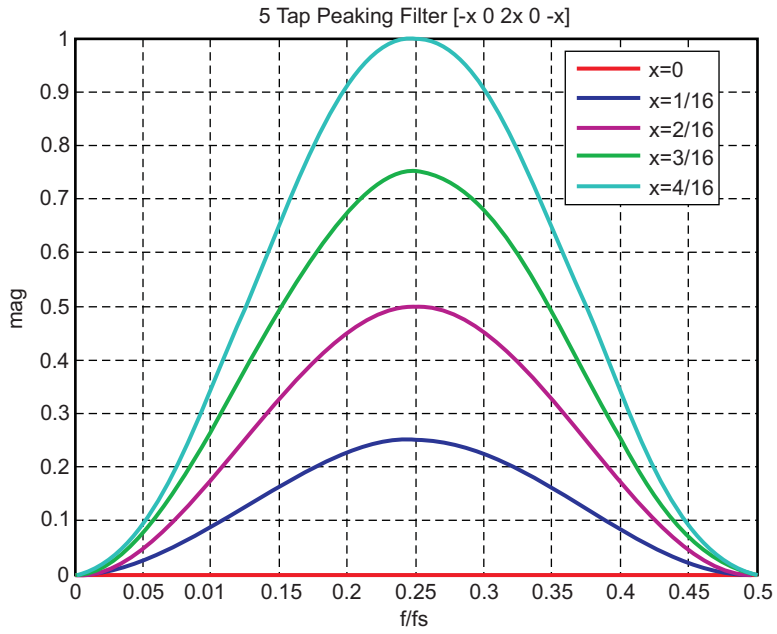
Table 9-24. Parameter Description

Parameter	Description	Bits	Default
VIP_CFG_SC19[7:0] CFG_HPF_COEF0 to VIP_CFG_SC20[15:8] CFG_HPF_COEF5	FIR coefficients	8	[0 0 0-4 0 8]
VIP_CFG_SC20[18:16] CFG_HPF_NORM_SHIFT	Right shift	3	4
VIP_CFG_SC21[8:0] CFG_NL_LO_THR	Coring threshold	9	16
VIP_CFG_SC22[8:0] CFG_NL_HI_THR	High threshold	9	400
VIP_CFG_SC21[23:16] CFG_NL_LO_SLOPE	Lo slope= - CFG_NL_LO_SLOPE/16	8	16
VIP_CFG_SC22[18:16] CFG_NL_HI_SLOPE_SHIFT	Hi slope = $2^{(CFG_NL_HI_SLOPE_SHIFT-3)}$	3	4
VIP_CFG_SC20[28:20] CFG_NL_LIMIT	Clipping limit	9	200
VIP_CFG_SC0[14] CFG_Y_PK_EN	Control	1	0

Parameters for the Peaking filters are defined in VIP_CFG_SC19 through VIP_CFG_SC22 registers. The frequency responses of the peaking-filter with different sets of coefficients are shown in Figure 9-83. If the source of the input video is NTSC or PAL format, the peaking filter can be configured to reject the color subcarrier frequency.

Figure 9-83. Peaking Filter at fs/4



9.4.7.2.3 Vertical Scaler

The vertical scaler has a polyphase (32-phase × 5-tap) filter and a running average filter as shown in Figure 9-84. While the polyphase filter can be used for any up-scaling and preferably downscaling to 3/16 scale factor, the running average filter is used only for downscaling to a ½ or less size. Selection between these two scalers is based on the user setting of VIP_CFG_SC0[4] CFG_USE_RAV parameter (CFG_USE_RAV= '0' for poliphase filter, and CFG_USE_RAV= '1' for running average filter), according to the user preference of the tradeoff between sharpness preserving and introduced artifacts.

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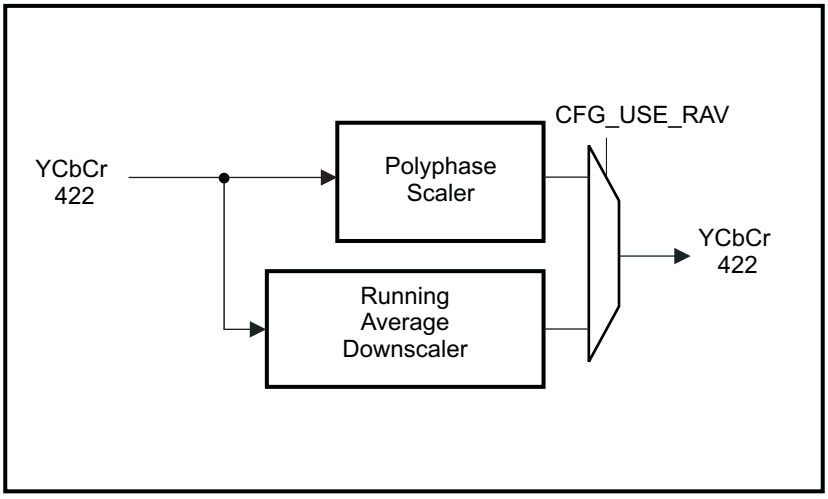
Figure 9-84. Vertical Scaler Block Diagram



9.4.7.2.3.1 Running Average Filter

When a poly-phase filter is used, usually it has to have many taps in order to achieve acceptable quality for very small downscaling ratio, which requires the use of many line buffers. In VIP, there is a weighted Running Average filter for downscaling when the scaling factor is small (for example, when the scaling ratio is less than 0.5). This highly optimized design requires only one line buffer for luma and one for chroma, which still achieving acceptable quality. The output of the running average filter is based on weighted average of pixels in the current and previous rows in vertical direction. Initializations of accumulators affect the weights.

9.4.7.2.3.2 Vertical Scaler Configuration Parameters

Table 9-25. Vertical Scaler Configuration Parameters

Parameter	Typical Value	Controls	Description
VIP_CFG_SC0[10] CFG_INTERLACE_I		Frame or Field	0 = progressive, 1 = interlace
VIP_CFG_SC0[0] CFG_INTERLACE_O			0 = progressive 1 = interlace
VIP_CFG_SC0[3] CFG_INVT_FID			Invert field ID input
VIP_CFG_SC0[4] CFG_USE_RAV		Scaler Mode	0 = use polyphase scaler 1 = use running average scaler
VIP_CFG_SC1[26:0] CFG_ROW_ACC_INC		Bilinear & Polyphase Scalers	For progressive in/progressive out: round(2^{16}*(srcH-1)/(tarH - 1)) For progressive_in/interlace_out: round(2^{16}*2*(srcH-1)/(2*tarH - 1)) For interlace_in/progressive_out: round(2^{16}*(2*srcH-1)/(2*(tarH - 1))) For interlace_in/interlace_out: round(2^{16}*(2*srcH - 1)/(2*tarH - 1)) For interlace in/out, srcH/tarH are number of field lines as specified in VIP_CFG_SC4/VIP_CFG_SC5 descriptions.
VIP_CFG_SC2[27:0] CFG_ROW_ACC_OFFSET	0		Initial row accumulator value for progressive frame and top field
VIP_CFG_SC3[27:0] CFG_ROW_ACC_OFFSET_B	0		Initial row accumulator value for bottom field
VIP_CFG_SC13[27:24] CFG_DELTA_CHROMA_THR	4	Bilinear Scaler	Range for chroma soft switch based on pixel differences (max limit = 8)

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Table 9-25. Vertical Scaler Configuration Parameters (continued)

Parameter	Typical Value	Controls	Description
VIP_CFG_SC13[21:12] CFG_CHROMA_INTP_THR	64		Threshold used in chroma soft switch based on pixel differences
VIP_CFG_SC13[9:0] CFG_SC_FACTOR_RAV		Running Average Scaler	Scale factor = round(1024 × tarH/srcH)
VIP_CFG_SC6[9:0] CFG_ROW_ACC_INIT_RAV			Initial row accumulator value for progressive frame and top field
VIP_CFG_SC6[19:10] CFG_ROW_ACC_INIT_RAV_B			Initial row accumulator value for bottom field

NOTE: Bi-linear scaler is not present in this device

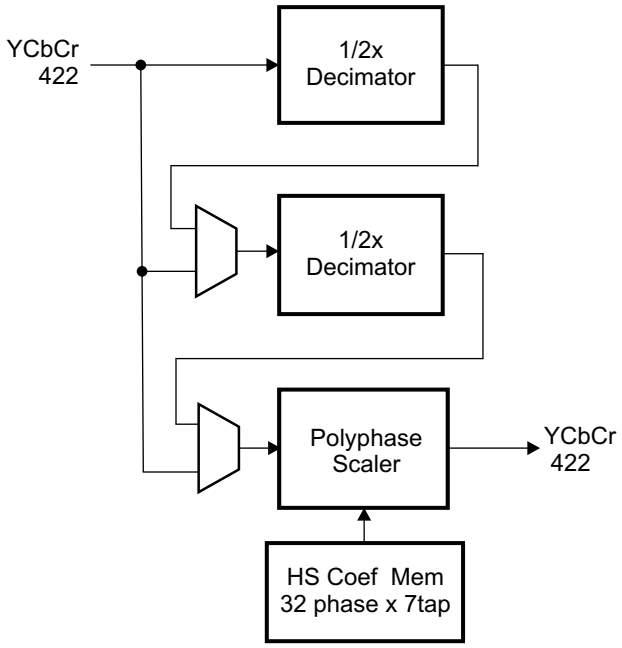
9.4.7.2.4 Horizontal Scaler

The Horizontal scaler is implemented using a 32-phase × 7-tap polyphase filter preceded by two sets of 1/2x decimators. The general configuration of the Horizontal scaler is performed as follows:

- For up scaling, the input video is interpolated using the polyphase scaler.
- For downscaling, it is recommended that input video is decimated by 2 until the modified scale factor falls between 1/2 and 1. Then, a polyphase filter is configured with coefficients selected based on the mod_scale_factor calculated as shown below from one of nine different sets of coefficients: (8,9,10,11,12,13,14,15,16)/16.

```
if  (scale_factor>=1/2)  {
   mux=0;  mod_scale_factor=scale factor;
} else if  (scale_factor>=1/4) {
   mux=1; mod_scale_factor=2*scale_factor;
} else {
   mux=2; mod_scale_factor=4*scale_factor;
}
```

Figure 9-85. Horizontal Scaler Block Diagram



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In auto mode (CFG_AUTO_HS == 1), scaler will operate as per above recommendation. In addition to this, for (CFG_AUTO_HS==1), polyphase filtering will be bypassed when (scale_factor == 1) or (scale_factor == ½) or (scale_factor == ¼). If CFG_AUTO_HS==0) is used, user must provide proper values for dcm_2x, dcm_4x, proper values for all inputs to polyphase filter in the registers as well as appropriate coefficient sets. There is no constraint on polyphase filtering in terms of scaling ratio. However, there are constraints on input and output image width for scaler. Frame dimensions are limited from 64x64 to 2047x2047.

9.4.7.2.4.1 Half Decimation Filter

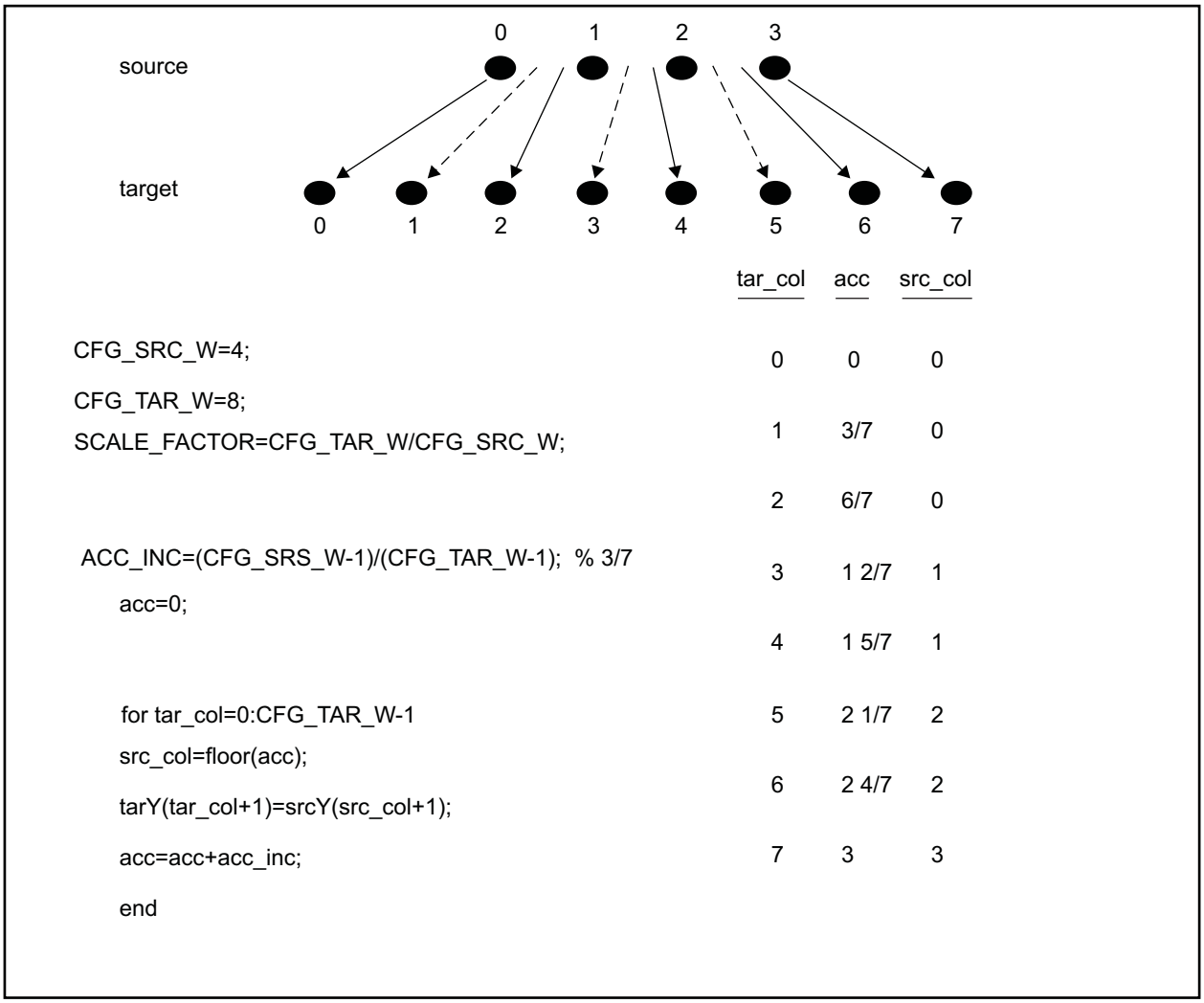
The half-decimation filter is an 11-tap filter with following coefficients: (14, 0, -29, 0, 79, 128, 79, 0, -29, 0, 14). For processing left and right edge pixels, the first and last data are repeated to pre-fill and extend the filter data pipeline respectively. These coefficients are hard-coded into scaler design and user cannot modify these.

9.4.7.2.4.2 Polyphase Filter

The horizontal scaling is done by stepping across the target row and interpolating target pixels based on source pixels. Accumulator points to the source pixel that corresponds to the target pixel.

Figure 9-86 shows an up-scaling example.

Figure 9-86. Polyphase Filtering Example



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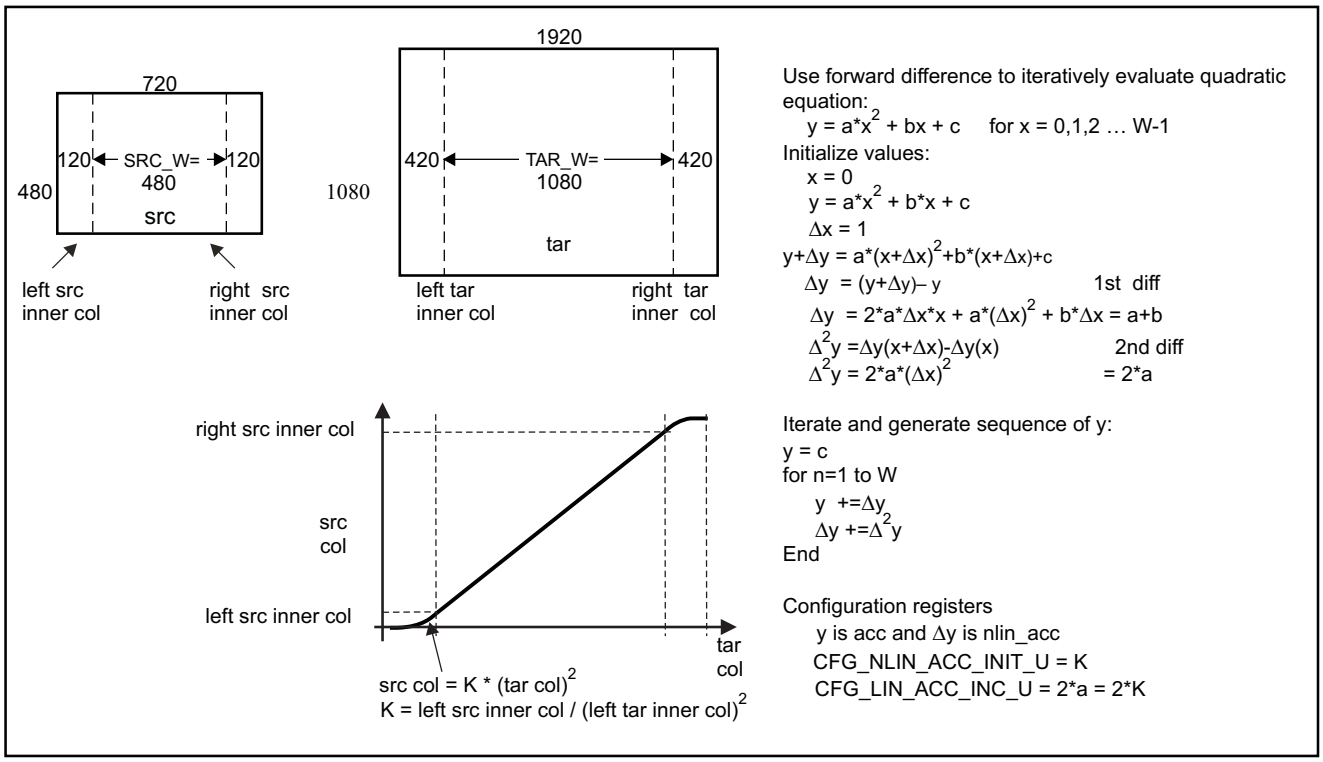
9.4.7.2.4.3 Nonlinear Horizontal Scaling

The horizontal scaler supports non-linear scaling to maintain the same aspect ratio for inner picture while stretching picture edges to fill the required resolution when capturing a 4 × 3 picture and fetching it as a 16 × 9 to memory. Non-linear scaling parameters are set with VIP_CFG_SC4[30:28] CFG_NLIN_ACC_INIT_U and VIP_CFG_SC4[26:24] CFG_LIN_ACC_INC_U registers. When setting up a non-linear scaling application, the inner picture is defined as the center square portion of the image with width and height equal to the height of the source image. Remaining side regions are then scaled non-linearly. Figure 9-87 shows a non-linear scaling case.

Figure 9-87. Non-linear Scaling Example



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9.4.7.2.4.4 Horizontal Scaler Configuration Registers

Table 9-26. Register Group 1

Parameter	Controls	Description			
VIP_CFG_SC4[10:0] CFG_TAR_H	Image Dimension	Source Width			
VIP_CFG_SC4[22:12] CFG_TAR_W		Target Width			
VIP_CFG_SC0[1] CFG_LINEAR	Scaler Mode	If (linear == 1) SRC_Wi = SRC_W and TAR_Wi = TAR_W Else SRC_W= SRC_H and TAR_W = TAR_H			
VIP_CFG_SC0[2] CFG_SC_BYPASS		0 = enable scaler, 1 = bypass scaler			
VIP_CFG_SC0[6] CFG_AUTO_HS		CFG_AUTO_HS	CFG_DCM_2X	CFG_DCM_4X	Definition
		0	0	0	Polyphase scaling
VIP_CFG_SC0[7] CFG_DCM_2X		0	0	1	Horizontal decimation by 4 and polyphase scaling
		0	1	0	Horizontal decimation by 2 and polyphase scaling
VIP_CFG_SC0[8] CFG_DCM_4X		1	-	-	Automatic (selection of decimation filter is automatic)

Table 9-27. Register Group 2

Scale Factor	Decimation Usage	Control Register Bit
< 1/4	Decimation by 4	VIP_CFG_SC0[8] CFG_DCM_4X (set to 1 to enable decimation; disabled by default)
== 1/4	Decimation by 4	
1/4 < and < 1/2	Decimation by 2	VIP_CFG_SC0[7] CFG_DCM_2X (set to 1 to enable decimation; disabled by default)
== 1/2	Decimation by 2	
1/2 < and < 1	Bypassed	VIP_CFG_SC0[7] CFG_DCM_2X and CFG_DCM_4X (set to 0 to disable decimation; default value)
1	Bypassed	
> 1	Bypassed	

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Table 9-28. Register Group 3

Parameter	Controls	Description
VIP_CFG_SC9[26:24] CFG_LIN_ACC_INC	Polyphase Scaler	if upscaling then CFG_LIN_ACC_INC = round(2^{24}*(srcWi-1)/(tarWi-1)) elseif downscaling CFG_LIN_ACC_INC= round(2^{24}*(srcWi/n-1)/(tarWi-1)) where n=2 or 4
VIP_CFG_SC8[10:0] CFG_NLIN_LEFT		if linear==1 CFG_NLIN_LEFT = 0 else CFG_NLIN_LEFT = (tarW - tarWi)/2
VIP_CFG_SC8[22:12] CFG_NLIN_RIGHT		if linear==1 CFG_NLIN_RIGHT = tarW-1 else CFG_NLIN_RIGHT = Ltar + tarWi – 1
VIP_CFG_SC5[26:24] CFG_NLIN_ACC_INC_U		if tarW/srcW >= 1 then d = 0 if Ltar!=0 K = round[2^{24}*Lsrc/(Ltar*Ltar)] where Lsrc = (srcW-srcWi)/2 else K = 0 else d = (tarW-1)/2 if Ltar!=0 K = round[2^{24} * Lsrc / (Ltar*(Ltar-2d))] where Lsrc= (srcW-srcWi)/(2n) and n=1,2 or 4 else K = 0 CFG_LIN_ACC_INC = 2*K (negative for downscaling)
VIP_CFG_SC4[30:28] CFG_NLIN_ACC_INIT_U		CFG_LIN_ACC_INC = K*(1-2*d)

NOTE: Source width and height variables for the polyphase filter are internally set with trimmer and decimation filter adjusted values.

9.4.7.2.5 Basic Configurations

Table 9-29 shows how the scaler should be configured based on the scale factor and the input/output mode.

Table 9-29. Scaler Configuration

Interlace		Mode[1]	VIP_CFG_SC5[10:0] CFG_SRC_H mod_srcH	VIP_CFG_SC4[10:0] CFG_TAR_H mod_tarH	Scale Factor
In	Out				
0	0	p->p	CFG_SRC_H	CFG_TAR_H	CFG_TAR_H/CFG_SRC_H
0	1	p->i	CFG_SRC_H	CFG_TAR_H/2	CFG_TAR_H/CFG_SRC_H
1	0	i->p	CFG_SRC_H/2	CFG_TAR_H	CFG_TAR_H/(CFG_SRC_H/2)
1	1	i->i	CFG_SRC_H/2	CFG_TAR_H/2	(CFG_TAR_H/2)/(CFG_SRC_H/2)

(1) p = progressive; i = interlaced

Table 9-30 shows how the vertical scaler should be configured based on the scale factor and the input/output mode.

Table 9-30. Vertical Scaler Configuration

Interlace		Mode[1]	VIP_CFG_SC9[26:24] CFG_ROW_ACC_INC/216	VIP_CFG_SC6[9:0] CFG_ROW_ACC_INIT_RAV/216	VIP_CFG_SC6[19:10] CFG_ROW_ACC_INIT_RAV_B/216
In	Out			Top	Bot
0	0	p->p	(CFG_SRC_H-1)/(CFG_TAR_H-1)	0	0
0	1	p->i	2*(CFG_SRC_H-1)/(CFG_TAR_H-1)	0	(CFG_SRC_H-1)/(CFG_TAR_H-1)
1	0	i->p	1/2*(CFG_SRC_H-1)/(CFG_TAR_H-1)	0	-0.5

(1) p = progressive; i = interlaced

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Table 9-30. Vertical Scaler Configuration (continued)

1	1	i->i	(CFG_SRC_H-1)/(CFG_TAR_H-1)	0	[(CFG_SRC_H-1)/(CFG_TAR_H-1)-1]/2

9.4.7.2.6 Coefficient Memory

9.4.7.2.6.1 Overview

The scaler requires initialization of eight coefficient SRAMS prior to processing a video frame. These coefficients are stored in the external DDR memories and downloaded by the VPDMA. The VPDMA writes the coefficient data through the VPI Control Interface bus.

The eight coefficient SRAMs are:

- HS horizontal polyphase scaler, Luma and Chroma (7tap)
- VS vertical polyphase scaler, Luma and Chroma (5tap or 3tap)

9.4.7.2.6.2 Physical Coefficient SRAM Layout

Each of the six legacy coefficient SRAMs is 32 phases × 91 bits. A single coefficient value is 13 bits. Therefore, one word of the SRAM contains 7 coefficient values as shown in Figure 9-88, and 224 coefficient values are stored in each SRAM.

Figure 9-88. SRAM Layout for 7tap Coefficient

Phase 0	C6	C5	C4	C3	C2	C1	C0
Phase 31	C223	C222	C221	C220	C219	C218	C217

The two vertical polyphase SRAMs are 32 phases × 65 bits. A single coefficient is 13 bits. Therefore, one word of SRAM contains 5 coefficient values as shown in Figure 9-89.

Figure 9-89. SRAM Layout for 5tap Coefficient

Phase 0	C4	C3	C2	C1	C0
Phase 31	C221	C220	C219	C218	C217

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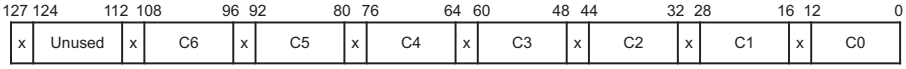
9.4.7.2.6.3 Scaler Coefficients Packing on 128-bit VPI Control I/F

A coefficient value is 13 bits wide and takes a single half word. Thus, one VPI Control write carries one phase's worth of coefficients. The last half-word in a quad-word is not used for 7tap coefficients.

Figure 9-90. VPI Control I/F Coef Data Format (7tap)



The Vertical Polyphase scaler coefficients have only five or three values per phase, so the last three (or five) entries are unused. The Vertical Polyphase coefficient packing is shown in Figure 9-91 and Figure 9-92.

Figure 9-91. VPI Control I/F Coef Data Format (5tap)

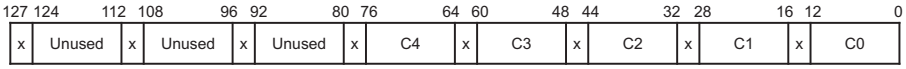
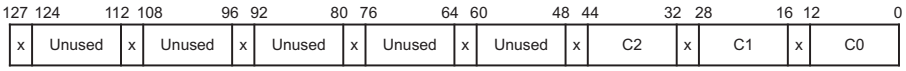


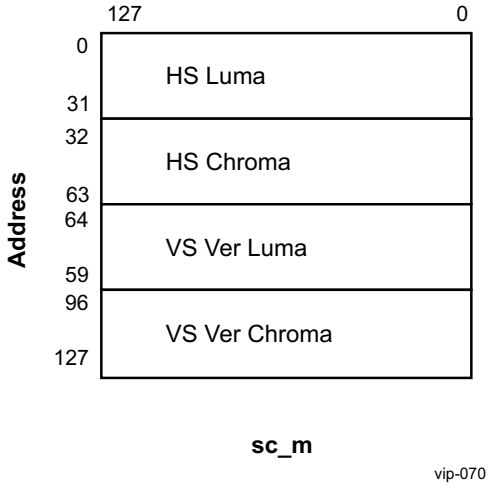
Figure 9-92. VPI Control I/F Coef Data Format (3tap)



9.4.7.2.6.4 VPI Control I/F Memory Map for Scaler Coefficients

The memory map of the VPI Control I/F for the Scaler coefficients is shown in Figure 9-93. All coefficients can be filled up by a single VPI Control write command. The update address feature of VPI Control I/F enables individual access to a certain location of memories.

Figure 9-93. VPI Control I/F Memory Map (Write)



The module supports the VPI Control Read to read back the contents in the coefficient memories for debug purpose. Figure 9-94 shows the memory map of the VPI Control Read. As the VPI Control Read has only 32 bit data bus, it requires the word addressing while the write does the quad-word addressing.

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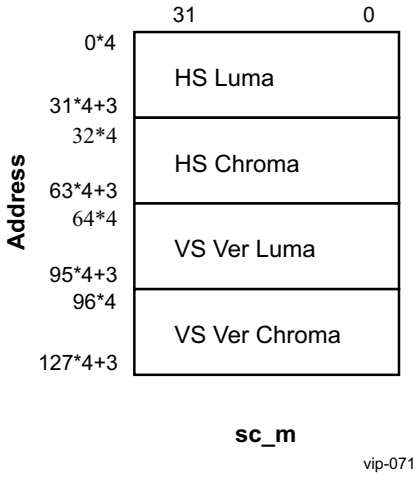
Figure 9-94. VPI Control I/F Memory Map (Read)



9.4.7.2.6.5 VPI Control Interface

VPDMA is used to configure the coefficient memories of scaler through VPI control interface. Since the coefficient memories are not shadowed (unlike the memory mapped registers), VPI control write access needs to be done only during the gap between video frame processing times. If a write request is made while the Scaler is active, the access will be held off by the hardware until the last data of the currently processed frame is sent out. Care must be given to the order of the DMA descriptors so that blocking of VPI control bus does not occur.

9.4.7.2.6.6 Coefficient Table Selection Guide

The scaler filter coefficient tables are pre-generated using a MATLAB® program for various scaling factor ranges. Table 9-31 provides a general selection guide table for coefficient data files.

The mentioned .dat files are available in Section 9.4.7.4.

Table 9-31. Coefficient Data Files

Scaler	Scale Factor	Coeff table
HS Polyphase Filter	All upscaling	Section 9.4.7.4.1.1, *ppfcoef_scael_eq_1_32_phases_flip.dat*
	½ or ¼ down scaling	Section 9.4.7.4.1.1, ppfcoef_scale_eq_1_32_phases_flip.dat
	> 15/16	Section 9.4.7.4.1.9, *ppfcoef_scale_eq_15div16_32_phases_flip.dat*
	> 14/16	Section 9.4.7.4.1.8, *ppfcoef_scale_eq_14div16_32_phases_flip.dat*
	> 13/16	Section 9.4.7.4.1.7, *ppfcoef_scale_eq_13div16_32_phases_flip.dat*
	> 12/16	Section 9.4.7.4.1.6, *ppfcoef_scale_eq_12div16_32_phases_flip.dat*
	> 11/16	Section 9.4.7.4.1.5, *ppfcoef_scale_eq_11div16_32_phases_flip.dat*
	> 10/16	Section 9.4.7.4.1.4, *ppfcoef_scale_eq_10div16_32_phases_flip.dat*
	> 9/16	Section 9.4.7.4.1.3, *ppfcoef_scale_eq_9div16_32_phases_flip.dat*
	> 8/16	Section 9.4.7.4.1.2, *ppfcoef_scale_eq_8div16_32_phases_flip.dat*(1)

(1) HS Scaler has two sets of ½ decimator to perform downscaling ratios below ½ and ¼.

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Table 9-31. Coefficient Data Files (continued)

Scaler	Scale Factor	Coeff table
VS Polyphase Filter	Upscaling	Section 9.4.7.4.2.1, *ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat*
	> 15/16	Section 9.4.7.4.2.6.8, *ppfcoef_scale_eq_15div16_32_phases_ver_5tap_flip.dat*
	> 14/16	Section 9.4.7.4.2.6.7, *ppfcoef_scale_eq_14div16_32_phases_ver_5tap_flip.dat*
	> 13/16	Section 9.4.7.4.2.6.6, *ppfcoef_scale_eq_13div16_32_phases_ver_5tap_flip.dat*
	> 12/16	Section 9.4.7.4.2.6.5, *ppfcoef_scale_eq_12div16_32_phases_ver_5tap_flip.dat*
	> 11/16	Section 9.4.7.4.2.6.4, *ppfcoef_scale_eq_11div16_32_phases_ver_5tap_flip.dat*
	> 10/16	Section 9.4.7.4.2.6.3, *ppfcoef_scale_eq_10div16_32_phases_ver_5tap_flip.dat*
	> 9/16	Section 9.4.7.4.2.6.2, *ppfcoef_scale_eq_9div16_32_phases_ver_5tap_flip.dat*
	> 8/16	Section 9.4.7.4.2.6.1, *ppfcoef_scale_eq_8div16_32_phases_ver_5tap_flip.dat*
	else	For down-scaling <8/16, RAV filter is recommended. In this case, coeffcients for vertical scaling need to be loaded.

9.4.7.3 SC Code

9.4.7.3.1 Generate Coefficient Memory Image

The following Perl script is used to generate a coefficient memory image for a given set of scaling factors.

```
#!/usr/local/bin/perl

#$dir="coef/";                    # directory which contains the coef files
#$cfg_file="sc_config1.cfg";      # configuration file name
#$spl_file="sc_config_supl.cfg";  # supplemental configuration file name
$cfg_file=$ARGV[0];               # configuration file name
$spl_file=$ARGV[1];               # supplemental configuration file name
$dir=$ARGV[2];                    # directory which contains the coef files

$coef_width=13;  # coef bit width
$coef_ntap=7;    # coef tap
$coef_nphase=32; # coef phase
$coef_norm=11;   # coef norm

#-----------------------------------------------------------
# read config file to get srcH/tarH/interlace_i/interlace_o
#-----------------------------------------------------------
open(INFILE, "<$cfg_file") or die "### ERROR: Cannot open $cfg_file";
while(<INFILE>){
  if (m/([-0-9]+) +\/\/ +srcW/) {
    $srcW = $1;
  } elsif (m/([-0-9]+) +\/\/ +srcH/) {
    $srcH = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarW/) {
    $tarW = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarH/) {
    $tarH = $1;
  } elsif (m/([-0-9]+) +\/\/ +interlace_in/) {
    $interlace_i = $1;
  } elsif (m/([-0-9]+) +\/\/ +interlace_out/) {
    $interlace_o = $1;
  }
```


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```
}
close(INFILE);

#-------------------------------------------------------------
# read supplemental config file to get srcWi/tarWi from
#-------------------------------------------------------------
open(INFILE,"<$spl_file") or die "### ERROR: Cannot open $spl_file";
while(<INFILE>){
  if (m/([-0-9]+) +\/\/ +srcWi/) {
    $srcWi = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarWi/) {
    $tarWi = $1;
  } elsif (m/([-0-9]+) +\/\/ +profile/) {
    $profile = $1; # 0:HIGH,1:MEDIUM,2:LOW
  }
}
close(INFILE);
#-------------------------------------------------------------
# determine coef file based on the width/height
#-------------------------------------------------------------
#VS
#$vsc_file0 = "mod_ppfcoef_scale_eq_1_32_phases_flip.dat";
$vsc_file0  = "ppfcoef_scale_eq_1_32_phases_flip_PPF3_peak5_gain_eq_1_25.dat";
#VS VER
$mod_tarH = ($interlace_i == 0 && $interlace_o == 1)   $tarH<<1 : $tarH; if ($profile==2) {
  # LOW profile
  if ($mod_tarH >= $srcH) {
    $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_3tap_flip.dat";
} else {
    if ($mod_tarH >=($srcH>>1)) {
      $n = int(16.0*$mod_tarH/$srcH);
      $vsc_ver_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_ver_3tap_flip.dat",$n);
    } else {
      $n = 0;
      $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_3tap_flip.dat";
    }
  }
} else {
  if ($mod_tarH >= $srcH) {
    $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat";
  } else {
      $n = int(16.0*$mod_tarH/$srcH);
      $vsc_ver_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_ver_5tap_flip.dat",$n);
  }
}

# HS
if ($tarWi >= $srcWi) {
  $hsc_file0 = "ppfcoef_scale_eq_1_32_phases_flip.dat";
} elsif ( ($tarWi == ($srcWi>>1)) || ($tarWi == ($srcWi>>2)) ) {
  $hsc_file0 = "ppfcoef_scale_eq_1_32_phases_flip.dat";
} else {
if ($tarWi > ($srcWi>>1)) {
    $n = int(16.0*$tarWi/$srcWi);
  } elsif ($tarWi > ($srcWi>>2)) {
    $n = int(16.0*$tarWi/($srcWi>>1));
  } elsif ($tarWi >=($srcWi>>3)) {
    $n = int(16.0*$tarWi/($srcWi>>2));
  } else {
    $n = 0;
  }
  $hsc_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_flip.dat",$n);
}
#-------------------------------------------------------------
# write out the coef hex file
#-------------------------------------------------------------
```


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```
&write_coef($hsc_file0);
&write_coef($hsc_file0);
&write_coef($vsc_ver_file0);
&write_coef($vsc_ver_file0);
&write_coef($vsc_file0);
&write_coef($vsc_file0);
sub write_coef {

  my ($filename) = @_;

  open(INFILE, "<$dir/$filename") or die "### ERROR: Cannot open $dir/$filename";

  $line=<INFILE>;
@val=split(' ',$line);
  $ntap=$val[0];
  $nphase=$val[1];
  $norm=$val[2];
for ($p=0;$p<$nphase;$p++) {
    $line=<INFILE>;@val=split(' ',$line);
    for($i=0;$i<$ntap;$i++) {
      if ($val[$i]<0) {
        $val[$i]+=(1<<$coef_width);
      }
    }
    undef(@coef);
    unshift(@coef, sprintf("%04x",$val[0]));
    unshift(@coef, sprintf("%04x",$val[1]));
    unshift(@coef, sprintf("%04x",$val[2]));
    unshift(@coef, sprintf("%04x",$val[3]));
    unshift(@coef, sprintf("%04x",$val[4]));
    unshift(@coef, sprintf("%04x",$val[5]));
    unshift(@coef, sprintf("%04x",$val[6]));
    unshift(@coef, sprintf("%04x",0));
    $coef=join("",@coef);
    print "$coef\n";
  }

  close(INFILE);
}
```

9.4.7.3.2 Scaler Configuration Calculation

The following C-code shows how configuration parameters are calculated:

```
// ======================================
// Required Input Parameter
// ======================================
//   srcW, srcH, tarW, tarH, srcWi, tarWi
//   input/output scan modes
//   Note:  srcH and tarH refer to number of lines in the frame even for interlace in/out
//          scaling.  Based on scaling scan mode input/output scan mode option,
//          heights are adjusted during internal calculations see mod_srcH and mod_tarH.


pixel_scale_factor=4;  // 10 bit pixel
hor_pixel_offset =0.0

  // ================================================================================================
  // Peaking Filter Configuration
  // ================================================================================================
  // ----------------------------------------------------------------
  // HPF Coef
  // ----------------------------------------------------------------
    y_peak_enable     =   0;

    peak_select=0; // 0=peak at fs/4  1=NTSC  2=PAL
```


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```
        switch(peak_select) {
        case 0: {// peak at fs/4 and gain = 1
                 HPF_coef0         =   0;
                 HPF_coef1         =   0;
                 HPF_coef2         =   0;
                 HPF_coef3         =  -4;
                 HPF_coef4         =   0;
                 HPF_coef5         =   8; // mid tap
                 HPF_norm_shift    =   4;
             break;
    }
        case 1: {// NTSC: peak at 0.133*fs and gain=1
                 HPF_coef0         =  -2;
                 HPF_coef1         =  -8;
                 HPF_coef2         =  -8;
                 HPF_coef3         =  -2;
                 HPF_coef4         =  12;
                 HPF_coef5         =  16; // mid tap
                 HPF_norm_shift    =   6;
                 break;
        }
        case 2: {// PAL: peak at 0.163*fs and gain=1
                 HPF_coef0         =   2;
                 HPF_coef1         =  -4;
                 HPF_coef2         = -11;
                 HPF_coef3         =  -7;
                 HPF_coef4         =   9;
                 HPF_coef5         =  22; // mid tap
                 HPF_norm_shift    =   6;
                 break;
        }
        }

      // ---------------------------------------------------------------
      // NonLinear Coring Function typical values
      // ---------------------------------------------------------------
        NL_coring_thr     =  16;
        NL_limit          = 200;
        NL_lo_slope       =  16;
        NL_hi_thr         = 400;
        NL_hi_slope_shift =   4;



      // ============================================================================================
      // Edge Detection Configuration
      // ============================================================================================
        // edge detection
        confidence_default = 0; // 0  =use 5 tap polyphase filter for SC with ev_enable =0

        min_Gy_thr         =  64; // 64
        min_Gy_thr_range   =   3; // 3 power of 2
        gradient_thr       = 200; // 200
    gradient_thr_range =   6; // 6 power of 2

        ev_thr = int(4.0*3.111+0.5); // edge vector soft switch threshold (3.2)


      // ============================================================================================
      // vertical scaler configuration
      // ============================================================================================
      // ---------------------------------------------------------------
      // vertical scaler typical parameters
      // ---------------------------------------------------------------
        invert_field_ID           =  0; // invert field ID input
        delta_ev_thr              =  1; // edge vector soft switch range
```


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```
    ver_pixel_offset          =  0.0;
    uv_intp_thr               =  pixel_scale_factor*16;
    delta_y_thr               =  4; // luma soft switch range
    delta_uv_thr              =  4; // chroma soft switch range
  //
  //
  // ------------------------------------------------------------------
  // Vertical Scaler Mode Determination
  // ------------------------------------------------------------------
  //
  //  interlace
  //   in   out   mode mod_srcH mod_tarH         scale
  // ----- ------ ---- -------- --------   -----------------
  //   0      0   p->p   srcH     tarH           tarH/srcH
  //   0      1   p->i   srcH     tarH>>1        tarH/srcH
  //   1      0   i->p   srcH>>1  tarH           tarH/(srcH/2)
  //   1      1   i->i   srcH>>1  tarH>>1    (tarH/2)/(srcH/2)

  if (interlace_in)  mod_srcH=srcH>>1; // interlace
  else               mod_srcH=srcH;    // progressive
  if (interlace_out) mod_tarH=tarH>>1; // interlace
  else               mod_tarH=tarH;    // progressive

  // determine vertical scaler
  if ((interlace_in==0)&&(interlace_out==1)) {
    if (tarH>((1+srcH)>>1)) use_rav = 0;   // 1=use RAV scaler 0=use polyphase scaler
    else                    use_rav = 1;
  } else {
    if (mod_tarH>((1+mod_srcH)>>1)) use_rav = 0; // 1=use RAV scaler  0=use polyphase scaler
    else                            use_rav = 1;
}



  // ------------------------------------------------------------------
  // RAV or Polyphase parameters
  // ------------------------------------------------------------------
  if (use_rav) {  // downscale
    // ------------
    // --- RAV ----
    // ------------
    if (use_internal_defaults) enable_edge_detection =   0;

    if ((interlace_in==0)&&(interlace_out==1)) scale = double(tarH)/double(srcH);
    else                                      scale = double(mod_tarH)/double(mod_srcH);
    sc_factor_rav = int(1024.0*scale+0.5);
// Peter's method
    delta     = (1.0/scale-1.0)/2.0;
    int_part  = floor(delta);
    frac_part = delta-int_part;

    row_acc_init_rav   = int(1024*(scale+(1.0-
scale)/2.0)+0.5);                                    // top field
    row_acc_init_b_rav = int(1024*(scale+(1.0-2.0*frac_part)*(1.0-
(1.0+2.0*int_part)*scale)/2.0)+0.5); // bottom field

    row_acc_inc        = 0; // polyphase scaler
    row_acc_offset     = 0; // polyphase scaler
    row_acc_offset_b   = 0; // polyphase scaler

  } else { // upscale using polyphase scaler
    // ------------
    // --- PPF ----
    // ------------
    if (use_internal_defaults) enable_edge_detection =   1;
```


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```
    sc_factor_rav      = 0;
    delta_rav          = 0;
    row_acc_init_rav   = 0;
    row_acc_init_b_rav = 0;

    // upscaler
    // interlace                              row acc init value
        //  in   out mode      row acc inc      top          bottom
    // ---- ---- ---- -------------------- ---  ---------------------
    //   0    0  p->p     (srcH-1)/(tarH-1)  0             0
    //   0    1  p->i   2*(srcH-1)/(tarH-1)  0    (srcH-1)/(tarH-1)
    //   1    0  i->p 1/2*(srcH-1)/(tarH-1)  0           -0.5
    //   1    1  i->i     (srcH-1)/(tarH-1)  0   [(srcH-1)/(tarH-1)-1]/2

    row_acc_offset   = int(65536.0*ver_pixel_offset +0.5);  // progressive or top field
    if (interlace_in) {
if (interlace_out) {
         row_acc_inc      =  int(65536.0*double(srcH-1)/double(tarH-1)+0.5);
        row_acc_offset_b =  (int(65536.0/2.0*(double(srcH-1)/(double(tarH-1))-
                              1.0)+0.5))+row_acc_offset;
       } else { // progressive out
          row_acc_inc      = int(65536.0*double(srcH-1)/(2.0*double(tarH-1))+0.5);
            if ((-0.5+row_acc_offset)<0.0) round_factor=-0.5;
            else                           round_factor= 0.5;
            row_acc_offset_b = int(65536.0*(-0.5)+round_factor)+row_acc_offset;
       }
    } else {   // progressive in
       if (interlace_out) {
        row_acc_inc      = int(65536.0*2.0*double(srcH-1)/double(tarH-1)+0.5);
        row_acc_offset_b =  int(65536.0*double(srcH-1)/double(tarH-1)+0.5)+row_acc_offset;
       } else { // progressive out
          row_acc_inc      =  int(65536.0*double(srcH-1)/double(tarH-1)+0.5);
           row_acc_offset_b = row_acc_offset;
       }
    }
  }
// ===============================================================================================
  // Horizontal Scaler configuration
  // ===============================================================================================
  // ---------------------------------------------------------------
  // horizontal scaler mode determination
  // ---------------------------------------------------------------
  auto_hs                = 1;
  dcm_2x                 = 0;
  dcm_4x                 = 0;
  hp_bypass              = 0;
  if (srcWi==srcW) linear = 1;
  else             linear = 0;

  // hor scaler parameters
  if (tarW>srcW) {              // upscale
    mod_srcW  = srcW;
    mod_srcWi = srcWi;
} else if (tarW<=(srcW>>2)) {  // downscale by <=1/4
    mod_srcW  = srcW>>2;
    mod_srcWi = srcWi>>2;
  } else if (tarW<=(srcW>>1)) {  // downscale by <=1/2
    mod_srcW  = srcW>>1;
    mod_srcWi = srcWi>>1;
  } else {                      // downscale by <=1
    mod_srcW  = srcW;
    mod_srcWi = srcWi;
  }

  // Not used any more:
  // hs_factor       = int(16.0*double(tarWi)/double(mod_srcWi)+0.5);  // hor scale factor (6.4)
```


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```
  // ---------------------------------------------------------------
  // Horizontal PolyPhase Settings  --
  // ---------------------------------------------------------------
  lin_acc_inc     = int(16777216.0*double(mod_srcWi-1)/double(tarWi-1)+0.5);
  col_acc_offset  = int(16777216.0*hor_pixel_offset +0.5);
  nlin_left       = (tarW-tarWi)>>1;
  nlin_right      = nlin_left+tarWi-1;
  if (linear) {
    nlin_acc_inc    = 0;
    nlin_acc_init   = 0;
  } else {
     // ---------------------------------
     // Non-linear scaling configuration
     // ---------------------------------
    nlin_left_src   = (mod_srcW-mod_srcWi)>>1;

        if (tarWi>=srcWi) {    // upscale
      d             =  0.0;
      round_factor  =  0.5;
        } else {                 // downscale
      d             = (double(tarW)-1.0)/2.0;
      round_factor  = -0.5;
    }

      K             = 16777216.0*double(nlin_left_src)/(double(nlin_left)*double(nlin_left-
2.0*d));
    nlin_acc_inc  = int(2.0*K+round_factor);
    nlin_acc_init = int(K*(1.0-2.0*d)+0.5);
  }
nlin_left_tar  = nlin_left;
  nlin_right_tar = nlin_right;

  // ================================================================================================
  // Bypass Determination
  // ================================================================================================
  // bypass
  if ((srcW==tarW)&&(srcWi==tarWi)&&(mod_srcH==mod_tarH)) sc_bypass = 1;
  else                                                    sc_bypass = 0;
  //

}
```

9.4.7.3.3 Typical Configuration Values

The following is the list of all scaler register fields that are set to constant values, representing typical settings:

VIP_CFG_SC0[3] CFG_INVT_FID = 0 (Field ID will be used without inversion)

VIP_CFG_SC0[5] CFG_ENABLE_EV = 1 (Field ID will be used without inversion)

VIP_CFG_SC0[6] CFG_AUTO_HS = 1 (The hardware will automatically decide, if current operation is up or down scaling. In down-scaling, it will also decide, if 2X or 4X decimation filter is needed)

VIP_CFG_SC0[7] CFG_DCM_2X = 0 (The 2X decimation filter is disabled)

VIP_CFG_SC0[8] CFG_DCM_4X = 0 (The 4X decimation filter is disabled)

VIP_CFG_SC0[11] CFG_ENABLE_SIN2_VER_INTP = 1 (Modified bilinear interpolation is used)

VIP_CFG_SC0[14] CFG_Y_PK_EN = 0 (Luma peaking is disabled)

VIP_CFG_SC0[15] CFG_TRIM= 1 (Trimming is enabled)

VIP_CFG_SC12[24:0] CFG_COL_ACC_OFFSET = 0 (No horizontal offset is involved)

VIP_CFG_SC13[21:12] CFG_CHROMA_INTP_THR = 64 (If the difference is less than this threshold, the interpolation of chroma should be done along edge direction. Otherwise, the interpolation of chroma should be done vertically)

VIP_CFG_SC13[27:24] CFG_DELTA_CHROMA_THR = 4 (max limit=8)

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VIP_CFG_SC18[24:16] CFG_CONF_DEFAULT = 0x100 (Defines confidence factor when edge detection is disabled (VIP_CFG_SC0[5] CFG_ENABLE_EV bit = 0))
VIP_CFG_SC19 = 0xFC000000
VIP_CFG_SC20 = 0x0C840800
VIP_CFG_SC21 = 0x00100010
VIP_CFG_SC22 = 0x00040190

9.4.7.4 SC Coefficient Data Files

9.4.7.4.1 HS Polyphase Filter Coefficients

9.4.7.4.1.1 ppfcoef_scale_eq_1_32_phases_flip.dat

```
 7  32 11
31 -112  210 1790  210 -112   31
28  -98  159 1787  264 -126   34
25  -84  111 1779  320 -140   37
22  -71   65 1767  379 -154   40
19  -58   23 1750  439 -168   43
16  -45  -17 1728  502 -181   45
14  -33  -53 1701  565 -193   47
11  -22  -86 1670  631 -205   49
 9  -11 -116 1635  696 -216   51
 7   -1 -142 1594  763 -225   52
 5    8 -166 1551  830 -233   53
 3   16 -186 1504  898 -240   53
 2   23 -204 1455  965 -245   52
 1   30 -218 1401 1031 -248   51
 0   35 -230 1345 1097 -249   50
-1   40 -238 1286 1162 -248   47
44 -244 1224 1224 -244   44    0
47 -248 1162 1286 -238   40   -1
50 -249 1097 1345 -230   35    0
51 -248 1031 1401 -218   30    1
52 -245  965 1455 -204   23    2
53 -240  898 1504 -186   16    3
53 -233  830 1551 -166    8    5
52 -225  763 1594 -142   -1    7
51 -216  696 1635 -116  -11    9
49 -205  631 1670  -86  -22   11
47 -193  565 1701  -53  -33   14
45 -181  502 1728  -17  -45   16
43 -168  439 1750   23  -58   19
40 -154  379 1767   65  -71   22
37 -140  320 1779  111  -84   25
34 -126  264 1787  159  -98   28
```

9.4.7.4.1.2 ppfcoef_scale_eq_8div16_32_phases_flip.dat

```
 7  32 11
  -28   61  542  898  542   61  -28
  -27   52  523  899  560   70  -29
  -26   44  505  898  578   79  -30
  -25   37  487  895  595   89  -30
  -24   30  468  892  613  100  -31
  -22   23  450  887  630  111  -31
  -21   17  432  883  647  122  -32
  -20   11  414  877  664  134  -32
  -19    6  396  871  680  146  -32
  -18    1  378  864  695  159  -31
  -16   -4  360  856  711  172  -31
  -15   -8  343  847  726  185  -30
  -14  -12  325  838  740  200  -29
```


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```
  -13  -15  308  828  754  214  -28
  -12  -18  292  816  768  229  -27
  -10  -21  275  805  780  244  -25
  -23  258  789  789  258  -23    0
  -25  244  780  805  275  -21  -10
  -27  229  768  816  292  -18  -12
  -28  214  754  828  308  -15  -13
  -29  200  740  838  325  -12  -14
  -30  185  726  847  343   -8  -15
  -31  172  711  856  360   -4  -16
  -31  159  695  864  378    1  -18
  -32  146  680  871  396    6  -19
  -32  134  664  877  414   11  -20
  -32  122  647  883  432   17  -21
  -31  111  630  887  450   23  -22
  -31  100  613  892  468   30  -24
  -30   89  595  895  487   37  -25
  -30   79  578  898  505   44  -26
  -29   70  560  899  523   52  -27
```

9.4.7.4.1.3 ppfcoef_scale_eq_9div16_32_phases_flip.dat

```
7  32 11
  -33    8  547 1004  547    8  -33
  -31    0  525 1003  570   16  -35
  -29   -7  503 1001  592   25  -37
  -27  -13  481  998  614   34  -39
  -26  -19  459  995  636   44  -41
  -24  -25  437  990  658   55  -43
  -22  -29  414  983  679   67  -44
  -20  -34  393  976  700   79  -46
  -18  -38  371  968  721   91  -47
  -17  -41  350  959  742  104  -49
  -15  -44  330  948  761  118  -50
  -13  -46  309  936  780  133  -51
  -12  -48  289  924  799  148  -52
  -11  -50  270  911  817  163  -52
   -9  -51  250  897  833  180  -52
   -8  -52  232  882  850  196  -52
  -52  213  863  863  213  -52    0
  -52  196  850  882  232  -52   -8
  -52  180  833  897  250  -51   -9
  -52  163  817  911  270  -50  -11
  -52  148  799  924  289  -48  -12
  -51  133  780  936  309  -46  -13
  -50  118  761  948  330  -44  -15
  -49  104  742  959  350  -41  -17
  -47   91  721  968  371  -38  -18
  -46   79  700  976  393  -34  -20
  -44   67  679  983  414  -29  -22
  -43   55  658  990  437  -25  -24
  -41   44  636  995  459  -19  -26
  -39   34  614  998  481  -13  -27
  -37   25  592 1001  503   -7  -29
  -35   16  570 1003  525    0  -31
```

9.4.7.4.1.4 ppfcoef_scale_eq_10div16_32_phases_flip.dat

```
7  32 11
  -30  -46  542 1116  542  -46  -30
  -28  -52  515 1115  570  -39  -33
  -25  -57  488 1113  597  -32  -36
  -23  -62  462 1109  624  -24  -38
  -20  -65  435 1104  650  -15  -41
  -18  -69  409 1097  678   -5  -44
  -16  -71  383 1089  704    6  -47
```


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```
-14  -74  358 1081  730   17  -50
-12  -75  333 1070  756   29  -53
-11  -76  309 1058  782   42  -56
 -9  -77  285 1045  806   56  -58
 -8  -77  262 1030  831   71  -61
 -6  -77  239 1015  855   86  -64
 -5  -76  218  997  877  103  -66
 -4  -75  196  980  899  120  -68
 -3  -74  176  961  920  138  -70
-72  156  940  940  156  -72    0
-70  138  920  961  176  -74   -3
-68  120  899  980  196  -75   -4
-66  103  877  997  218  -76   -5
-64   86  855 1015  239  -77   -6
-61   71  831 1030  262  -77   -8
-58   56  806 1045  285  -77   -9
-56   42  782 1058  309  -76  -11
-53   29  756 1070  333  -75  -12
-50   17  730 1081  358  -74  -14
-47    6  704 1089  383  -71  -16
-44   -5  678 1097  409  -69  -18
-41  -15  650 1104  435  -65  -20
-38  -24  624 1109  462  -62  -23
-36  -32  597 1113  488  -57  -25
-33  -39  570 1115  515  -52  -28
```

9.4.7.4.1.5 ppfcoef_scale_eq_11div16_32_phases_flip.dat

```
7  32 11
-19  -94  522 1230  522  -94  -19
-17  -98  490 1230  555  -90  -22
-14 -100  458 1227  587  -85  -25
-12 -102  427 1223  620  -79  -29
-10 -103  397 1217  652  -73  -32
 -8 -104  367 1209  685  -65  -36
 -6 -104  337 1199  717  -56  -39
 -4 -103  309 1187  749  -47  -43
 -3 -102  281 1174  781  -36  -47
 -1 -100  253 1159  812  -24  -51
  0  -98  227 1142  843  -11  -55
  1  -96  201 1124  874    3  -59
  1  -93  177 1105  903   18  -63
  2  -90  153 1084  932   34  -67
  2  -87  131 1062  961   51  -72
  3  -83  109 1038  987   69  -75
-79   89 1014 1014   89  -79    0
-75   69  987 1038  109  -83    3
-72   51  961 1062  131  -87    2
-67   34  932 1084  153  -90    2
-63   18  903 1105  177  -93    1
-59    3  874 1124  201  -96    1
-55  -11  843 1142  227  -98    0
-51  -24  812 1159  253 -100   -1
-47  -36  781 1174  281 -102   -3
-43  -47  749 1187  309 -103   -4
-39  -56  717 1199  337 -104   -6
-36  -65  685 1209  367 -104   -8
-32  -73  652 1217  397 -103  -10
-29  -79  620 1223  427 -102  -12
-25  -85  587 1227  458 -100  -14
-22  -90  555 1230  490  -98  -17
```

9.4.7.4.1.6 ppfcoef_scale_eq_12div16_32_phases_flip.dat

```
7  32 11
   -3 -132  486 1346  486 -132   -3
```


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```
  -1 -132  449 1345  524 -131   -6
   1 -131  413 1342  562 -130   -9
   3 -130  378 1336  600 -127  -12
   4 -128  343 1328  639 -123  -15
   5 -125  309 1319  677 -119  -18
   6 -122  277 1306  716 -113  -22
   7 -118  245 1292  754 -106  -26
   8 -114  214 1276  793  -98  -31
   8 -109  185 1257  831  -89  -35
   9 -105  156 1237  869  -78  -40
   9 -100  130 1214  906  -66  -45
   9  -94  104 1190  942  -53  -50
   9  -89   79 1165  978  -38  -56
   8  -83   56 1138 1012  -22  -61
   8  -78   35 1108 1046   -4  -67
 -72   15 1081 1081   15  -72    0
 -67   -4 1046 1108   35  -78    8
 -61  -22 1012 1138   56  -83    8
 -56  -38  978 1165   79  -89    9
 -50  -53  942 1190  104  -94    9
 -45  -66  906 1214  130 -100    9
 -40  -78  869 1237  156 -105    9
 -35  -89  831 1257  185 -109    8
 -31  -98  793 1276  214 -114    8
 -26 -106  754 1292  245 -118    7
 -22 -113  716 1306  277 -122    6
 -18 -119  677 1319  309 -125    5
 -15 -123  639 1328  343 -128    4
 -12 -127  600 1336  378 -130    3
  -9 -130  562 1342  413 -131    1
  -6 -131  524 1345  449 -132   -1
```

9.4.7.4.1.7 ppfcoef_scale_eq_13div16_32_phases_flip.dat

```
7  32 11
  14 -154  435 1458  435 -154   14
  15 -150  393 1458  477 -157   12
  16 -146  353 1454  521 -160   10
  16 -141  314 1447  565 -161    8
  17 -135  276 1436  609 -161    6
  17 -129  239 1425  654 -161    3
  17 -123  204 1410  699 -159    0
  16 -116  170 1393  745 -156   -4
  16 -109  137 1373  790 -151   -8
  16 -102  107 1350  835 -146  -12
  15  -94   77 1325  879 -138  -16
  14  -87   50 1298  924 -130  -21
  13  -80   24 1269  968 -119  -27
  12  -72    0 1238 1010 -107  -33
  11  -65  -22 1204 1053  -94  -39
  10  -58  -43 1169 1093  -78  -45
 -52  -62 1138 1138  -62  -52    0
 -45  -78 1093 1169  -43  -58   10
 -39  -94 1053 1204  -22  -65   11
 -33 -107 1010 1238    0  -72   12
 -27 -119  968 1269   24  -80   13
 -21 -130  924 1298   50  -87   14
 -16 -138  879 1325   77  -94   15
 -12 -146  835 1350  107 -102   16
  -8 -151  790 1373  137 -109   16
  -4 -156  745 1393  170 -116   16
   0 -159  699 1410  204 -123   17
   3 -161  654 1425  239 -129   17
   6 -161  609 1436  276 -135   17
   8 -161  565 1447  314 -141   16
  10 -160  521 1454  353 -146   16
```


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```
   12 -157  477 1458  393 -150   15
```

9.4.7.4.1.8 ppfcoef_scale_eq_14div16_32_phases_flip.dat

```
 7  32 11
   27 -158  370 1570  370 -158   27
   27 -150  324 1568  417 -165   27
   26 -142  281 1563  465 -172   27
   25 -133  238 1555  515 -178   26
   24 -124  198 1543  565 -183   25
   23 -115  159 1527  616 -186   24
   22 -106  122 1510  667 -189   22
   21  -97   87 1489  719 -191   20
   19  -87   54 1464  772 -191   17
   18  -78   23 1437  824 -190   14
   16  -69   -6 1407  876 -187   11
   15  -60  -32 1373  927 -182    7
   13  -52  -57 1339  979 -176    2
   12  -44  -79 1300 1030 -168   -3
   11  -36  -99 1261 1079 -159   -9
    9  -28 -117 1218 1128 -147  -15
  -21 -134 1179 1179 -134  -21    0
  -15 -147 1128 1218 -117  -28    9
   -9 -159 1079 1261  -99  -36   11
   -3 -168 1030 1300  -79  -44   12
    2 -176  979 1339  -57  -52   13
    7 -182  927 1373  -32  -60   15
   11 -187  876 1407   -6  -69   16
   14 -190  824 1437   23  -78   18
   17 -191  772 1464   54  -87   19
   20 -191  719 1489   87  -97   21
   22 -189  667 1510  122 -106   22
   24 -186  616 1527  159 -115   23
   25 -183  565 1543  198 -124   24
   26 -178  515 1555  238 -133   25
   27 -172  465 1563  281 -142   26
   27 -165  417 1568  324 -150   27
```

9.4.7.4.1.9 ppfcoef_scale_eq_15div16_32_phases_flip.dat

```
 7  32 11
   33 -143  294 1680  294 -143   33
   31 -132  246 1678  345 -155   35
   30 -121  199 1671  398 -165   36
   27 -109  154 1661  452 -175   38
   25  -97  112 1647  508 -185   38
   23  -86   72 1629  564 -193   39
   21  -75   35 1607  622 -201   39
   19  -64    0 1580  681 -207   39
   17  -53  -32 1551  740 -213   38
   15  -43  -61 1518  799 -217   37
   13  -33  -88 1481  859 -219   35
   11  -24 -113 1442  919 -220   33
    9  -15 -134 1399  978 -219   30
    8   -7 -153 1354 1036 -217   27
    6    0 -170 1307 1094 -212   23
    5    7 -184 1257 1150 -205   18
   13 -196 1207 1207 -196   13    0
   18 -205 1150 1257 -184    7    5
   23 -212 1094 1307 -170    0    6
   27 -217 1036 1354 -153   -7    8
   30 -219  978 1399 -134  -15    9
   33 -220  919 1442 -113  -24   11
   35 -219  859 1481  -88  -33   13
   37 -217  799 1518  -61  -43   15
   38 -213  740 1551  -32  -53   17
```


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```
 39 -207  681 1580    0  -64   19
 39 -201  622 1607   35  -75   21
 39 -193  564 1629   72  -86   23
 38 -185  508 1647  112  -97   25
 38 -175  452 1661  154 -109   27
 36 -165  398 1671  199 -121   30
 35 -155  345 1678  246 -132   31
```

9.4.7.4.2 VS Polyphase Filter Coefficients

9.4.7.4.2.1 ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat

```
5  32 11
  -47  177 1788  177  -47
  -40  133 1785  225  -55
  -33   91 1778  276  -64
  -27   53 1765  330  -73
  -21   18 1747  386  -82
  -15  -13 1722  445  -91
  -11  -41 1693  507 -100
   -7  -66 1660  570 -109
   -3  -88 1622  635 -118
    0 -107 1579  703 -127
    2 -122 1532  771 -135
    4 -135 1482  839 -142
    5 -145 1428  909 -149
    6 -153 1371  978 -154
    7 -158 1310 1047 -158
    7 -161 1247 1116 -161
 -162 1186 1186 -162    0
 -161 1116 1247 -161    7
 -158 1047 1310 -158    7
 -154  978 1371 -153    6
 -149  909 1428 -145    5
 -142  839 1482 -135    4
 -135  771 1532 -122    2
 -127  703 1579 -107    0
 -118  635 1622  -88   -3
 -109  570 1660  -66   -7
 -100  507 1693  -41  -11
  -91  445 1722  -13  -15
  -82  386 1747   18  -21
  -73  330 1765   53  -27
  -64  276 1778   91  -33
  -55  225 1785  133  -40
```

9.4.7.4.2.2 ppfcoef_scale_eq_3_32_phases_flip.dat

```
5,   32,   11,
  130,  515,  758,  515,  130,
  121,  503,  757,  528,  139,
  113,  490,  756,  541,  148,
  105,  477,  755,  553,  158,
   97,  464,  753,  566,  168,
   90,  451,  751,  578,  178,
   83,  437,  749,  590,  189,
   76,  424,  746,  602,  200,
   69,  411,  743,  614,  211,
   63,  398,  739,  626,  222,
   57,  386,  734,  637,  234,
   52,  373,  729,  648,  246,
   46,  360,  725,  659,  258,
   41,  347,  719,  670,  271,
   37,  335,  713,  680,  283,
   32,  322,  707,  690,  297,
  314,  710,  710,  314,    0,
```


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```
  297,  690,  707,  322,   32,
  283,  680,  713,  335,   37,
  271,  670,  719,  347,   41,
  258,  659,  725,  360,   46,
  246,  648,  729,  373,   52,
  234,  637,  734,  386,   57,
  222,  626,  739,  398,   63,
  211,  614,  743,  411,   69,
  200,  602,  746,  424,   76,
  189,  590,  749,  437,   83,
  178,  578,  751,  451,   90,
  168,  566,  753,  464,   97,
  158,  553,  755,  477,  105,
  148,  541,  756,  490,  113,
  139,  528,  757,  503,  121};
```

9.4.7.4.2.3 ppfcoef_scale_eq_4_32_phases_flip.dat

```
5,   32,   11,
  116,  515,  786,  515,  116,
  107,  502,  785,  530,  124,
   99,  488,  784,  544,  133,
   92,  473,  783,  557,  143,
   85,  459,  781,  571,  152,
   78,  445,  778,  585,  162,
   71,  431,  775,  598,  173,
   65,  417,  772,  611,  183,
   59,  403,  767,  624,  195,
   53,  389,  763,  637,  206,
   48,  375,  758,  649,  218,
   43,  362,  752,  661,  230,
   38,  348,  747,  673,  242,
   34,  334,  740,  685,  255,
   30,  321,  733,  696,  268,
   26,  308,  726,  707,  281,
  298,  726,  726,  298,    0,
  281,  707,  726,  308,   26,
  268,  696,  733,  321,   30,
  255,  685,  740,  334,   34,
  242,  673,  747,  348,   38,
  230,  661,  752,  362,   43,
  218,  649,  758,  375,   48,
  206,  637,  763,  389,   53,
  195,  624,  767,  403,   59,
  183,  611,  772,  417,   65,
  173,  598,  775,  431,   71,
  162,  585,  778,  445,   78,
  152,  571,  781,  459,   85,
  143,  557,  783,  473,   92,
  133,  544,  784,  488,   99,
  124,  530,  785,  502,  107};
```

9.4.7.4.2.4 ppfcoef_scale_eq_5_32_phases_flip.dat

```
5,   32,   11,
   98,  515,  822,  515,   98,
   90,  500,  821,  531,  106,
   83,  484,  820,  547,  114,
   75,  469,  819,  562,  123,
   69,  453,  816,  577,  133,
   63,  438,  813,  592,  142,
   57,  422,  809,  607,  153,
   51,  407,  805,  622,  163,
   46,  391,  801,  636,  174,
   41,  376,  795,  650,  186,
   37,  361,  789,  664,  197,
```


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```
 32,  347,  782,  678,  209,
 28,  332,  775,  691,  222,
 25,  317,  767,  704,  235,
 22,  303,  759,  716,  248,
 18,  289,  750,  729,  262,
278,  746,  746,  278,    0,
262,  729,  750,  289,   18,
248,  716,  759,  303,   22,
235,  704,  767,  317,   25,
222,  691,  775,  332,   28,
209,  678,  782,  347,   32,
197,  664,  789,  361,   37,
186,  650,  795,  376,   41,
174,  636,  801,  391,   46,
163,  622,  805,  407,   51,
153,  607,  809,  422,   57,
142,  592,  813,  438,   63,
133,  577,  816,  453,   69,
123,  562,  819,  469,   75,
114,  547,  820,  484,   83,
106,  531,  821,  500,   90};
```

9.4.7.4.2.5 ppfcoef_scale_eq_6_32_phases_flip.dat

```
5,   32,   11,
   77,  513,  868,  513,   77,
   70,  496,  867,  531,   84,
   63,  479,  866,  548,   92,
   57,  461,  864,  566,  100,
   51,  444,  861,  583,  109,
   46,  427,  857,  600,  118,
   41,  409,  853,  617,  128,
   36,  393,  847,  633,  139,
   32,  376,  841,  650,  149,
   28,  359,  835,  666,  160,
   24,  343,  827,  682,  172,
   21,  327,  819,  697,  184,
   18,  311,  810,  712,  197,
   15,  296,  800,  727,  210,
   13,  281,  790,  741,  223,
   11,  266,  779,  755,  237,
  253,  771,  771,  253,    0,
  237,  755,  779,  266,   11,
  223,  741,  790,  281,   13,
  210,  727,  800,  296,   15,
  197,  712,  810,  311,   18,
  184,  697,  819,  327,   21,
  172,  682,  827,  343,   24,
  160,  666,  835,  359,   28,
  149,  650,  841,  376,   32,
  139,  633,  847,  393,   36,
  128,  617,  853,  409,   41,
  118,  600,  857,  427,   46,
  109,  583,  861,  444,   51,
  100,  566,  864,  461,   57,
   92,  548,  866,  479,   63,
   84,  531,  867,  496,   70};
```

9.4.7.4.2.6 ppfcoef_scale_eq_7_32_phases_flip.dat

```
5,   32,   11,
   53,  510,  922,  510,   53,
   47,  490,  922,  529,   60,
   41,  470,  921,  549,   67,
   36,  451,  918,  569,   74,
   32,  431,  915,  588,   82,
```


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```
  27,  412,  910,  608,   91,
  23,  393,  905,  627,  100,
  20,  374,  898,  646,  110,
  17,  356,  890,  665,  120,
  14,  337,  882,  684,  131,
  11,  320,  873,  702,  142,
   9,  302,  863,  720,  154,
   7,  285,  852,  737,  167,
   6,  269,  840,  753,  180,
   4,  253,  827,  770,  194,
   3,  237,  815,  785,  208,
 223,  801,  801,  223,    0,
 208,  785,  815,  237,    3,
 194,  770,  827,  253,    4,
 180,  753,  840,  269,    6,
 167,  737,  852,  285,    7,
 154,  720,  863,  302,    9,
 142,  702,  873,  320,   11,
 131,  684,  882,  337,   14,
 120,  665,  890,  356,   17,
 110,  646,  898,  374,   20,
 100,  627,  905,  393,   23,
  91,  608,  910,  412,   27,
  82,  588,  915,  431,   32,
  74,  569,  918,  451,   36,
  67,  549,  921,  470,   41,
  60,  529,  922,  490,   47};
```

9.4.7.4.2.6.1 ppfcoef_scale_eq_8div16_32_phases_ver_5tap_flip.dat

```
5  32 11
   28  502  988  502   28
   24  479  987  524   34
   19  457  985  547   40
   15  435  982  570   46
   12  413  978  592   53
    9  392  972  614   61
    6  371  965  637   69
    4  350  957  659   78
    2  330  948  680   88
    0  310  938  702   98
   -1  291  926  723  109
   -2  272  914  744  120
   -3  254  900  764  133
   -3  237  886  783  145
   -4  220  871  802  159
   -4  204  855  820  173
  188  836  836  188    0
  173  820  855  204   -4
  159  802  871  220   -4
  145  783  886  237   -3
  133  764  900  254   -3
  120  744  914  272   -2
  109  723  926  291   -1
   98  702  938  310    0
   88  680  948  330    2
   78  659  957  350    4
   69  637  965  371    6
   61  614  972  392    9
   53  592  978  413   12
   46  570  982  435   15
   40  547  985  457   19
   34  524  987  479   24
```


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9.4.7.4.2.6.2 ppfcoef_scale_eq_9div16_32_phases_ver_5tap_flip.dat

```
5  32 11
    3  489 1064  489    3
    0  464 1062  515    7
   -3  439 1060  540   12
   -5  414 1056  566   17
   -7  390 1050  592   23
   -9  366 1044  618   29
  -10  343 1035  644   36
  -11  320 1025  670   44
  -12  298 1014  695   53
  -12  277 1001  720   62
  -12  256  987  745   72
  -12  236  972  769   83
  -12  217  956  792   95
  -11  199  938  815  107
  -10  181  920  837  120
  -10  165  900  859  134
  148  876  876  148    0
  134  859  900  165  -10
  120  837  920  181  -10
  107  815  938  199  -11
   95  792  956  217  -12
   83  769  972  236  -12
   72  745  987  256  -12
   62  720 1001  277  -12
   53  695 1014  298  -12
   44  670 1025  320  -11
   36  644 1035  343  -10
   29  618 1044  366   -9
   23  592 1050  390   -7
   17  566 1056  414   -5
   12  540 1060  439   -3
    7  515 1062  464    0
```

9.4.7.4.2.6.3 ppfcoef_scale_eq_10div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -20  470 1148  470  -20
  -22  442 1147  499  -18
  -23  413 1144  529  -15
  -24  386 1139  558  -11
  -24  359 1132  588   -7
  -24  333 1124  618   -3
  -24  308 1113  648    3
  -23  283 1101  678    9
  -23  260 1088  707   16
  -22  237 1072  737   24
  -21  215 1056  765   33
  -19  194 1037  793   43
  -18  174 1017  822   53
  -16  156  995  848   65
  -15  138  973  875   77
  -13  121  949  900   91
  105  919  919  105    0
   91  900  949  121  -13
   77  875  973  138  -15
   65  848  995  156  -16
   53  822 1017  174  -18
   43  793 1037  194  -19
   33  765 1056  215  -21
   24  737 1072  237  -22
   16  707 1088  260  -23
    9  678 1101  283  -23
    3  648 1113  308  -24
   -3  618 1124  333  -24
```


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```
 -7  588 1132  359  -24
-11  558 1139  386  -24
-15  529 1144  413  -23
-18  499 1147  442  -22
```

9.4.7.4.2.6.4 ppfcoef_scale_eq_11div16_32_phases_ver_5tap_flip.dat

```
5  32 11
-40  444 1240  444  -40
-40  412 1240  476  -40
-40  381 1236  510  -39
-39  350 1231  544  -38
-37  321 1223  577  -36
-36  293 1212  612  -33
-34  265 1200  646  -29
-32  239 1185  681  -25
-30  214 1169  715  -20
-28  190 1150  750  -14
-26  167 1130  783   -6
-23  146 1107  816    2
-21  126 1083  849   11
-19  107 1057  882   21
-17   90 1030  913   32
-15   73 1002  943   45
 58  966  966   58    0
 45  943 1002   73  -15
 32  913 1030   90  -17
 21  882 1057  107  -19
 11  849 1083  126  -21
  2  816 1107  146  -23
 -6  783 1130  167  -26
-14  750 1150  190  -28
-20  715 1169  214  -30
-25  681 1185  239  -32
-29  646 1200  265  -34
-33  612 1212  293  -36
-36  577 1223  321  -37
-38  544 1231  350  -39
-39  510 1236  381  -40
-40  476 1240  412  -40
```

9.4.7.4.2.6.5 ppfcoef_scale_eq_12div16_32_phases_ver_5tap_flip.dat

```
5  32 11
-56  409 1342  409  -56
-54  373 1342  445  -58
-51  339 1337  482  -59
-49  306 1330  521  -60
-46  274 1321  559  -60
-43  244 1308  598  -59
-40  215 1293  638  -58
-36  187 1275  678  -56
-33  161 1255  718  -53
-30  137 1233  757  -49
-27  114 1208  797  -44
-24   93 1182  836  -39
-21   73 1152  875  -31
-18   55 1122  912  -23
-16   38 1090  950  -14
-14   23 1056  986   -3
  9 1015 1015    9    0
 -3  986 1056   23  -14
-14  950 1090   38  -16
-23  912 1122   55  -18
-31  875 1152   73  -21
-39  836 1182   93  -24
```


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```
  -44  797 1208  114  -27
  -49  757 1233  137  -30
  -53  718 1255  161  -33
  -56  678 1275  187  -36
  -58  638 1293  215  -40
  -59  598 1308  244  -43
  -60  559 1321  274  -46
  -60  521 1330  306  -49
  -59  482 1337  339  -51
  -58  445 1342  373  -54
```

9.4.7.4.2.6.6 ppfcoef_scale_eq_13div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -65  364 1450  364  -65
  -61  326 1448  404  -69
  -57  289 1443  445  -72
  -53  253 1435  488  -75
  -48  220 1423  531  -78
  -44  188 1408  576  -80
  -40  158 1390  621  -81
  -36  130 1370  666  -82
  -32  103 1346  713  -82
  -28   79 1320  758  -81
  -24   56 1290  805  -79
  -21   36 1259  850  -76
  -18   17 1224  896  -71
  -15    0 1188  940  -65
  -12  -15 1149  984  -58
  -10  -28 1109 1027  -50
  -40 1064 1064  -40    0
  -50 1027 1109  -28  -10
  -58  984 1149  -15  -12
  -65  940 1188    0  -15
  -71  896 1224   17  -18
  -76  850 1259   36  -21
  -79  805 1290   56  -24
  -81  758 1320   79  -28
  -82  713 1346  103  -32
  -82  666 1370  130  -36
  -81  621 1390  158  -40
  -80  576 1408  188  -44
  -78  531 1423  220  -48
  -75  488 1435  253  -53
  -72  445 1443  289  -57
  -69  404 1448  326  -61
```

9.4.7.4.2.6.7 ppfcoef_scale_eq_14div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -67  310 1562  310  -67
  -61  269 1559  353  -72
  -55  230 1553  398  -78
  -50  193 1543  445  -83
  -44  158 1529  493  -88
  -39  125 1512  543  -93
  -34   94 1491  594  -97
  -30   66 1468  645 -101
  -25   41 1439  697 -104
  -22   17 1408  751 -106
  -18   -4 1373  804 -107
  -15  -23 1336  857 -107
  -12  -40 1296  910 -106
   -9  -55 1253  962 -103
   -7  -67 1208 1013  -99
   -5  -78 1161 1064  -94
```


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```
  -86 1110 1110  -86    0
  -94 1064 1161  -78   -5
  -99 1013 1208  -67   -7
 -103  962 1253  -55   -9
 -106  910 1296  -40  -12
 -107  857 1336  -23  -15
 -107  804 1373   -4  -18
 -106  751 1408   17  -22
 -104  697 1439   41  -25
 -101  645 1468   66  -30
  -97  594 1491   94  -34
  -93  543 1512  125  -39
  -88  493 1529  158  -44
  -83  445 1543  193  -50
  -78  398 1553  230  -55
  -72  353 1559  269  -61
```

9.4.7.4.2.6.8 ppfcoef_scale_eq_15div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -61  248 1674  248  -61
  -54  204 1673  293  -68
  -47  163 1665  342  -75
  -41  125 1654  392  -82
  -35   90 1638  445  -90
  -29   57 1618  499  -97
  -24   27 1593  556 -104
  -20    0 1565  613 -110
  -16  -24 1532  672 -116
  -12  -46 1495  732 -121
   -9  -65 1455  793 -126
   -6  -81 1411  854 -130
   -4  -95 1364  915 -132
   -2 -107 1315  975 -133
    0 -116 1262 1035 -133
    1 -123 1208 1094 -132
 -128 1152 1152 -128    0
 -132 1094 1208 -123    1
 -133 1035 1262 -116    0
 -133  975 1315 -107   -2
 -132  915 1364  -95   -4
 -130  854 1411  -81   -6
 -126  793 1455  -65   -9
 -121  732 1495  -46  -12
 -116  672 1532  -24  -16
 -110  613 1565    0  -20
 -104  556 1593   27  -24
  -97  499 1618   57  -29
  -90  445 1638   90  -35
  -82  392 1654  125  -41
  -75  342 1665  163  -47
  -68  293 1673  204  -54
```

9.4.7.4.3 VS (Bilinear Filter Coefficients)

9.4.7.4.3.1 ppfcoef_scale_eq_1_32_phases_flip_PPF3_peak5_gain_eq_1_25.dat

This is not applicable for this device

```
7  32 11
  -11 -106  190 1902  190 -106  -11
   -9 -105  153 1897  230 -105  -13
   -8 -105  121 1887  274 -105  -16
   -6 -104   91 1869  320 -104  -18
   -5 -102   65 1843  370 -102  -21
   -4 -101   42 1812  424 -101  -24
```


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```
 -3  -99   20 1776  480  -99  -27
 -2  -96    3 1730  539  -96  -30
 -1  -93  -12 1679  602  -93  -34
 -1  -90  -26 1627  665  -90  -37
  0  -87  -37 1568  732  -87  -41
  0  -84  -46 1506  801  -84  -45
  0  -80  -54 1439  871  -80  -48
  0  -76  -60 1371  941  -76  -52
  1  -72  -65 1299 1013  -72  -56
  1  -68  -69 1227 1085  -68  -60
-64  -64 1152 1152  -64  -64    0
-60  -68 1085 1227  -69  -68    1
-56  -72 1013 1299  -65  -72    1
-52  -76  941 1371  -60  -76    0
-48  -80  871 1439  -54  -80    0
-45  -84  801 1506  -46  -84    0
-41  -87  732 1568  -37  -87    0
-37  -90  665 1627  -26  -90   -1
-34  -93  602 1679  -12  -93   -1
-30  -96  539 1730    3  -96   -2
-27  -99  480 1776   20  -99   -3
-24 -101  424 1812   42 -101   -4
-21 -102  370 1843   65 -102   -5
-18 -104  320 1869   91 -104   -6
-16 -105  274 1887  121 -105   -8
-13 -105  230 1897  153 -105   -9
```

9.4.8 VIP Video Port Direct Memory Access (VPDMA)

9.4.8.1 VPDMA Introduction

The VPDMA primary function is to move data between external memory and internal processing modules that source or sink data. VPDMA is capable buffering this data and then delivering the data as demanded to the modules as programmed. The modules that source or sink data are referred to as clients. A channel is setup inside the VPDMA to connect a specific memory buffer to a specific client. The VPDMA centralizes the DMA control functions and buffering required to allow all the clients to minimize the effect of long latency times. The VPDMA also supports a descriptor based mode where lists of descriptors can be setup to configure all the channels as they become available.

Additionally, in a third-party configuration, the VPDMA is capable of performing DMA transfers as requested by the pulsing of an event strobe. The VPDMA is capable of generation of an address which may reach any location in the range for which it is configured. It is capable of moving this data either to or from a Shared Buffer and ultimately to or from a Client Buffer. For the two type of Client Buffers that are used to drive data into a subsystem (Streaming Buffer and Random Access Buffer) data is either pushed into the buffer or pulled out of the buffer dependent upon the direction of the data transfer. For third-party DMA operations the data is transferred into a Client buffer, and then transferred out of the Client Buffer to the transfer destination. These transfers are triggered by an Event pulse to each of the Client Buffers which are Routing Buffer types.

9.4.8.2 VPDMA Basic Definitions

9.4.8.2.1 Client

The modules that source or sink data are referred to as clients. The clients of the VPDMA are the physical between the processing modules (VIP) and external memory. A channel is the mechanism inside the VPDMA that connects a specific memory buffer or transfer to a specific client.

The start event can also be selected by a channel attribute or to be controlled by an internal frame signal controlled by the List Manager.

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9.4.8.2.2 Channel

The VPDMA requires a channel to be setup for each group of transfers. All the channels are described through a Data Transfer Descriptor that has a common format. The client that the channel is mapped to interprets the information in the descriptor to perform the requested data transfer.

Each of the channels has a type of data that it can support based upon the client that it services. The VPDMA supports three types of channels:

- **YUV Channel** - Clients taking data YUV data
- **RGB Channel** - Clients taking RGB data
- **Miscellaneous Channel** - The Miscellaneous channel type is for any data type that is not a normal video type. The Miscellaneous channel type makes no assumptions on data type and just passes the data to the client and supports a single buffer for the client.

9.4.8.2.3 List

A list is a group of descriptors that makes up a set of DMA transfers that need to be completed. The VPDMA supports one kind of list only:

- The **Regular List** is a single list that the VPDMA will execute each descriptor once and initiate an interrupt when the list has completed. A regular list can contain any kind of descriptor without limitation and be of any size.

The VPDMA Controller works on lists of descriptors. In this mode the processor writes the lists of descriptors in the order it wants them executed. It then writes the location of the list to the VIP_LIST_ADDR register, followed by writing the size (bit LIST_SIZE) and type (bit LIST_TYPE) of the list, and list number (bit LIST_NUM) to the VIP_LIST_ATTR register. The List Manager module then schedules a DMA transfer to pull in the portion of the list that it can store in internal VPDMA memory. The List Manager will sequentially process the active list of descriptors until either the descriptor requires the use of a client that is currently active, or if it is waiting for the next portion of the list to be transferred from a DMA request. If there is no active list to process the list manager will go into an IDLE mode waiting for any client that is blocking a list or a list DMA transfer to complete.

All the DMA transfers are controlled by List Manager module inside VPDMA. List Manager needs to be loaded with FIRMWARE, before any DMA transfer from memory, after the VPDMA reset. The first MMR write to VIP_LIST_ADDR register after VPDMA reset should be the address of the memory buffer(128-bit aligned, that is, last four bits of the buffer address should be zero) where the firmware is stored. List Manager then schedules a DMA transaction to fetch the firmware and sets the VIP_LIST_ATTR[19] RDY bit after the firmware loading is complete.

9.4.8.2.4 Data Formats Supported

Following list summarizes the data formats supported in the VPDMA. For more inforamtion see Section 9.4.8.9, *VPDMA Data Formats*.

- RGB Data Types:
  - RGB16-565
  - ARGB-1555
  - ARGB-4444
  - RGBA-5551
  - RGBA-4444
  - ARGB24-6666
  - RGB24-888
  - ARGB32-8888
  - RGBA24-6666
  - RGBA32-8888
  - BGR16-565
  - ABGR-1555

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  - ABGR-4444
  - BGRA-5551
  - BGRA-4444
  - ABGR24-6666
  - BGR24-888
  - ABGR32-8888
  - BGRA24-6666
  - BGRA32-8888
- YUV Data Types:
  - Y 4:4:4
  - Y 4:2:2
  - Y 4:2:0
  - C 4:4:4
  - C 4:2:2
  - C 4:2:0
  - CY 4:2:2
  - YCbC 4:4:4
  - YC 4:2:2

NOTE: VPDMA supports swapping formats (RGB/BGR and Cb/Cr)

9.4.8.3 VPDMA Client Buffering and Functionality

Table 9-32 lists for each client:

- The channels used, amount of buffering allocated for it, and the shared buffer used for its memory
- The line sizes it handles for tiled and non-tiled memory spaces, as well as any additional features it supports

Table 9-32. VPDMA Client Buffering and Functionality

Client	Channel(s)	Tiled Memory Max Line Size	Non-Tiled Memory Max Line Size	Additional Features
vip1_lo_y	vip1_mult_porta_src0 vip1_mult_porta_src1 vip1_mult_porta_src2 vip1_mult_porta_src3 vip1_mult_porta_src4 vip1_mult_porta_src5 vip1_mult_porta_src6 vip1_mult_porta_src7 vip1_mult_porta_src8 vip1_mult_porta_src9 vip1_mult_porta_src10 vip1_mult_porta_src11 vip1_mult_porta_src12 vip1_mult_porta_src13 vip1_mult_porta_src14 vip1_mult_porta_src15 vip1_portb_luma vip1_portb_rgb	1920 (color seperate) 960 (interleaved)	4096	TILED

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Table 9-32. VPDMA Client Buffering and Functionality (continued)

vip1_lo_uv	vip1_mult_portb_src0 vip1_mult_portb_src1 vip1_mult_portb_src2 vip1_mult_portb_src3 vip1_mult_portb_src4 vip1_mult_portb_src5 vip1_mult_portb_src6 vip1_mult_portb_src7 vip1_mult_portb_src8 vip1_mult_portb_src9 vip1_mult_portb_src10 vip1_mult_portb_src11 vip1_mult_portb_src12 vip1_mult_portb_src13 vip1_mult_portb_src14 vip1_mult_portb_src15 vip1_portb_chroma	1920 (color seperate) 960 (interleaved)	4096	TILED
vip1_up_y	vip1_porta_luma vip1_porta_rgb	1920 (color seperate) 960 (interleaved)	4096	TILED
vip1_up_uv	vip1_porta_chroma	1920 (color seperate) 960 (interleaved)	4096	TILED
vip2_lo_y	vip2_mult_porta_src0 vip2_mult_porta_src1 vip2_mult_porta_src2 vip2_mult_porta_src3 vip2_mult_porta_src4 vip2_mult_porta_src5 vip2_mult_porta_src6 vip2_mult_porta_src7 vip2_mult_porta_src8 vip2_mult_porta_src9 vip2_mult_porta_src10 vip2_mult_porta_src11 vip2_mult_porta_src12 vip2_mult_porta_src13 vip2_mult_porta_src14 vip2_mult_porta_src15 vip2_portb_luma vip2_portb_rgb	1920 (color seperate) 960 (interleaved)	4096	TILED
vip2_lo_uv	vip2_mult_portb_src0 vip2_mult_portb_src1 vip2_mult_portb_src2 vip2_mult_portb_src3 vip2_mult_portb_src4 vip2_mult_portb_src5 vip2_mult_portb_src6 vip2_mult_portb_src7 vip2_mult_portb_src8 vip2_mult_portb_src9 vip2_mult_portb_src10 vip2_mult_portb_src11 vip2_mult_portb_src12 vip2_mult_portb_src13 vip2_mult_portb_src14 vip2_mult_portb_src15 vip2_portb_chroma	1920 (color seperate) 960 (interleaved)	4096	TILED
vip2_up_y	vip2_porta_luma vip2_porta_rgb	1920 (color seperate) 960 (interleaved)	4096	TILED
vip2_up_uv	vip2_porta_chroma	1920 (color seperate) 960 (interleaved)	4096	TILED
vpi_ctl		Tiled Data Not Supported	4096	

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Table 9-32. VPDMA Client Buffering and Functionality (continued)

vip1_anc_a	vip1_mult_anca_src0 vip1_mult_anca_src1 vip1_mult_anca_src2 vip1_mult_anca_src3 vip1_mult_anca_src4 vip1_mult_anca_src5 vip1_mult_anca_src6 vip1_mult_anca_src7 vip1_mult_anca_src8 vip1_mult_anca_src9 vip1_mult_anca_src10 vip1_mult_anca_src11 vip1_mult_anca_src12 vip1_mult_anca_src13 vip1_mult_anca_src14 vip1_mult_anca_src15	Tiled Data Not Supported	4096	
vip1_anc_b	vip1_mult_ancb_src0 vip1_mult_ancb_src1 vip1_mult_ancb_src2 vip1_mult_ancb_src3 vip1_mult_ancb_src4 vip1_mult_ancb_src5 vip1_mult_ancb_src6 vip1_mult_ancb_src7 vip1_mult_ancb_src8 vip1_mult_ancb_src9 vip1_mult_ancb_src10 vip1_mult_ancb_src11 vip1_mult_ancb_src12 vip1_mult_ancb_src13 vip1_mult_ancb_src14 vip1_mult_ancb_src15	Tiled Data Not Supported	4096	
vip2_anc_a	vip2_mult_anca_src0 vip2_mult_anca_src1 vip2_mult_anca_src2 vip2_mult_anca_src3 vip2_mult_anca_src4 vip2_mult_anca_src5 vip2_mult_anca_src6 vip2_mult_anca_src7 vip2_mult_anca_src8 vip2_mult_anca_src9 vip2_mult_anca_src10 vip2_mult_anca_src11 vip2_mult_anca_src12 vip2_mult_anca_src13 vip2_mult_anca_src14 vip2_mult_anca_src15	Tiled Data Not Supported	4096	

9.4.8.4 VPDMA Channels Assignment

Table 9-33 lists all of the channels in VPDMA and its base attributes. The Data Type column states what type of data YUV, RGB or OTHER the channel handles and in parentheses are the legal data type values that can be entered into a data transfer decriptor. The Client field states the name of the Client and in parentheses it states the reference number in Figure 9-4, *VIP Block Diagram*.

Table 9-33. VPDMA Channels Assignment

Channel	Description	Channel Number	Data Type	Client
vip1_mult_porta_src0	Video Input 1 Port A Channel 0	38	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src1	Video Input 1 Port A Channel 1	39	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src2	Video Input 1 Port A Channel 2	40	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src3	Video Input 1 Port A Channel 3	41	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src4	Video Input 1 Port A Channel 4	42	YUV (0x7)	vip1_lo_y (2)

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Table 9-33. VPDMA Channels Assignment (continued)

Channel	Description	Channel Number	Data Type	Client
vip1_mult_porta_src5	Video Input 1 Port A Channel 5	43	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src6	Video Input 1 Port A Channel 6	44	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src7	Video Input 1 Port A Channel 7	45	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src8	Video Input 1 Port A Channel 8	46	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src9	Video Input 1 Port A Channel 9	47	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src10	Video Input 1 Port A Channel 10	48	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src11	Video Input 1 Port A Channel 11	49	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src12	Video Input 1 Port A Channel 12	50	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src13	Video Input 1 Port A Channel 13	51	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src14	Video Input 1 Port A Channel 14	52	YUV (0x7)	vip1_lo_y (2)
vip1_mult_porta_src15	Video Input 1 Port A Channel 15	53	YUV (0x7)	vip1_lo_y (2)
vip1_mult_portb_src0	Video Input 1 Port B Channel 0	54	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src1	Video Input 1 Port B Channel 1	55	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src2	Video Input 1 Port B Channel 2	56	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src3	Video Input 1 Port B Channel 3	57	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src4	Video Input 1 Port B Channel 4	58	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src5	Video Input 1 Port B Channel 5	59	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src6	Video Input 1 Port B Channel 6	60	YUV (0x7)	vip1_lo_uv(1)
vip1_mult_portb_src7	Video Input 1 Port B Channel 7	61	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src8	Video Input 1 Port B Channel 8	62	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src9	Video Input 1 Port B Channel 9	63	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src10	Video Input 1 Port B Channel 10	64	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src11	Video Input 1 Port B Channel 11	65	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src12	Video Input 1 Port B Channel 12	66	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src13	Video Input 1 Port B Channel 13	67	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src14	Video Input 1 Port B Channel 14	68	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_portb_src15	Video Input 1 Port B Channel 15	69	YUV (0x7)	vip1_lo_uv (1)
vip1_mult_anca_src0	Video Input 1 Port A Ancillary Data Channel 0	70	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src1	Video Input 1 Port A Ancillary Data Channel 1	71	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src2	Video Input 1 Port A Ancillary Data Channel 2	72	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src3	Video Input 1 Port A Ancillary Data Channel 3	73	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src4	Video Input 1 Port A Ancillary Data Channel 4	74	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src5	Video Input 1 Port A Ancillary Data Channel 5	75	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src6	Video Input 1 Port A Ancillary Data Channel 6	76	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src7	Video Input 1 Port A Ancillary Data Channel 7	77	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src8	Video Input 1 Port A Ancillary Data Channel 8	78	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src9	Video Input 1 Port A Ancillary Data Channel 9	79	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src10	Video Input 1 Port A Ancillary Data Channel 10	80	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src11	Video Input 1 Port A Ancillary Data Channel 11	81	OTHER (8)	vip1_anc_a(2)

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Table 9-33. VPDMA Channels Assignment (continued)

Channel	Description	Channel Number	Data Type	Client
vip1_mult_anca_src12	Video Input 1 Port A Ancillary Data Channel 12	82	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src13	Video Input 1 Port A Ancillary Data Channel 13	83	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src14	Video Input 1 Port A Ancillary Data Channel 14	84	OTHER (8)	vip1_anc_a(2)
vip1_mult_anca_src15	Video Input 1 Port A Ancillary Data Channel 15	85	OTHER (8)	vip1_anc_a(2)
vip1_mult_ancb_src0	Video Input 1 Port B Ancillary Data Channel 0	86	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src1	Video Input 1 Port B Ancillary Data Channel 1	87	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src2	Video Input 1 Port B Ancillary Data Channel 2	88	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src3	Video Input 1 Port B Ancillary Data Channel 3	89	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src4	Video Input 1 Port B Ancillary Data Channel 4	90	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src5	Video Input 1 Port B Ancillary Data Channel 5	91	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src6	Video Input 1 Port B Ancillary Data Channel 6	92	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src7	Video Input 1 Port B Ancillary Data Channel 7	93	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src8	Video Input 1 Port B Ancillary Data Channel 8	94	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src9	Video Input 1 Port B Ancillary Data Channel 9	95	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src10	Video Input 1 Port B Ancillary Data Channel 10	96	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src11	Video Input 1 Port B Ancillary Data Channel 11	97	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src12	Video Input 1 Port B Ancillary Data Channel 12	98	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src13	Video Input 1 Port B Ancillary Data Channel 13	99	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src14	Video Input 1 Port B Ancillary Data Channel 14	100	OTHER (8)	vip1_anc_b(2)
vip1_mult_ancb_src15	Video Input 1 Port B Ancillary Data Channel 15	101	OTHER (8)	vip1_anc_b(2)
vip1_porta_luma	Video Input 1 Port A 420 Data Luma	102	YUV (0x1, 0x2, 0x7)	vip1_up_y (1)
vip1_porta_chroma	Video Input 1 Port A 420 Data Chroma	103	YUV (0x5, 0x6, 0x7)	vip1_up_uv(1)
vip1_portb_luma	Video Input 1 Port B 420 Data Luma	104	YUV (0x1, 0x2, 0x7)	vip1_lo_y (2)
vip1_portb_chroma	Video Input 1 Port B 420 Data Chroma	105	YUV (0x5, 0x6, 0x7)	vip1_lo_uv (2)
vip1_porta_rgb	Video Input 1 Port A RGB Data	106	RGB (0x0 - 0x8)	vip1_up_y (1)
vip1_portb_rgb	Video Input 1 Port B RGB Data	107	RGB (0x0 - 0x8)	vip1_lo_y (2)
vip2_mult_porta_src0	Video Input 2 Port A Channel 0	108	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src1	Video Input 2 Port A Channel 1	109	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src2	Video Input 2 Port A Channel 2	110	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src3	Video Input 2 Port A Channel 3	111	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src4	Video Input 2 Port A Channel 4	112	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src5	Video Input 2 Port A Channel 5	113	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src6	Video Input 2 Port A Channel 6	114	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src7	Video Input 2 Port A Channel 7	115	YUV (0x7)	vip2_lo_y (21)

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Table 9-33. VPDMA Channels Assignment (continued)

Channel	Description	Channel Number	Data Type	Client
vip2_mult_porta_src8	Video Input 2 Port A Channel 8	116	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src9	Video Input 2 Port A Channel 9	117	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src10	Video Input 2 Port A Channel 10	118	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src11	Video Input 2 Port A Channel 11	119	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src12	Video Input 2 Port A Channel 12	120	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src13	Video Input 2 Port A Channel 13	121	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src14	Video Input 2 Port A Channel 14	122	YUV (0x7)	vip2_lo_y (21)
vip2_mult_porta_src15	Video Input 2 Port A Channel 15	123	YUV (0x7)	vip2_lo_y (21)
vip2_mult_portb_src0	Video Input 2 Port B Channel 0	124	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src1	Video Input 2 Port B Channel 1	125	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src2	Video Input 2 Port B Channel 2	126	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src3	Video Input 2 Port B Channel 3	127	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src4	Video Input 2 Port B Channel 4	128	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src5	Video Input 2 Port B Channel 5	129	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src6	Video Input 2 Port B Channel 6	130	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src7	Video Input 2 Port B Channel 7	131	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src8	Video Input 2 Port B Channel 8	132	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src9	Video Input 2 Port B Channel 9	133	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src10	Video Input 2 Port B Channel 10	134	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src11	Video Input 2 Port B Channel 11	135	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src12	Video Input 2 Port B Channel 12	136	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src13	Video Input 2 Port B Channel 13	137	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src14	Video Input 2 Port B Channel 14	138	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_portb_src15	Video Input 2 Port B Channel 15	139	YUV (0x7)	vip2_lo_uv (20)
vip2_mult_anca_src0	Video Input 2 Port A Ancillary Data Channel 0	140	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src1	Video Input 2 Port A Ancillary Data Channel 1	141	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src2	Video Input 2 Port A Ancillary Data Channel 2	142	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src3	Video Input 2 Port A Ancillary Data Channel 3	143	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src4	Video Input 2 Port A Ancillary Data Channel 4	144	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src5	Video Input 2 Port A Ancillary Data Channel 5	145	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src6	Video Input 2 Port A Ancillary Data Channel 6	146	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src7	Video Input 2 Port A Ancillary Data Channel 7	147	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src8	Video Input 2 Port A Ancillary Data Channel 8	148	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src9	Video Input 2 Port A Ancillary Data Channel 9	149	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src10	Video Input 2 Port A Ancillary Data Channel 10	150	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src11	Video Input 2 Port A Ancillary Data Channel 11	151	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src12	Video Input 2 Port A Ancillary Data Channel 12	152	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src13	Video Input 2 Port A Ancillary Data Channel 13	153	OTHER (8)	vip2_anc_a(21)

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Table 9-33. VPDMA Channels Assignment (continued)

Channel	Description	Channel Number	Data Type	Client
vip2_mult_anca_src14	Video Input 2 Port A Ancillary Data Channel 14	154	OTHER (8)	vip2_anc_a(21)
vip2_mult_anca_src15	Video Input 2 Port A Ancillary Data Channel 15	155	OTHER (8)	vip2_anc_a(21)
vip2_mult_ancb_src0	Video Input 2 Port B Ancillary Data Channel 0	156	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src1	Video Input 2 Port B Ancillary Data Channel 1	157	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src2	Video Input 2 Port B Ancillary Data Channel 2	158	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src3	Video Input 2 Port B Ancillary Data Channel 3	159	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src4	Video Input 2 Port B Ancillary Data Channel 4	160	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src5	Video Input 2 Port B Ancillary Data Channel 5	161	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src6	Video Input 2 Port B Ancillary Data Channel 6	162	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src7	Video Input 2 Port B Ancillary Data Channel 7	163	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src8	Video Input 2 Port B Ancillary Data Channel 8	164	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src9	Video Input 2 Port B Ancillary Data Channel 9	165	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src10	Video Input 2 Port B Ancillary Data Channel 10	166	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src11	Video Input 2 Port B Ancillary Data Channel 11	167	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src12	Video Input 2 Port B Ancillary Data Channel 12	168	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src13	Video Input 2 Port B Ancillary Data Channel 13	169	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src14	Video Input 2 Port B Ancillary Data Channel 14	170	OTHER (8)	vip2_anc_b(21)
vip2_mult_ancb_src15	Video Input 2 Port B Ancillary Data Channel 15	171	OTHER (8)	vip2_anc_b(21)
vip2_porta_luma	Video Input 2 Port A 420 Data Luma	172	YUV (0x1, 0x2, 0x7)	vip2_up_y (20)
vip2_porta_chroma	Video Input 2 Port A 420 Data Chroma	173	YUV (0x5, 0x6, 0x7)	vip2_up_uv(20)
vip2_portb_luma	Video Input 2 Port B 420 Data Luma	174	YUV (0x1, 0x2, 0x7)	vip2_lo_y (21)
vip2_portb_chroma	Video Input 2 Port B 420 Data Chroma	175	YUV (0x5, 0x6, 0x7)	vip2_lo_uv (21)
vip2_porta_rgb	Video Input 2 Port A RGB Data	176	RGB (0x0 - 0x8)	vip2_up_y(20)
vip2_portb_rgb	Video Input 2 Port B RGB Data	177	RGB (0x0 - 0x8)	vip2_lo_y (21)

9.4.8.5 VPDMA MFLAG Mechanism

The device L3_MAIN interconnect accepts MFLAG signals from certain initiators that can influence the internal L3_MAIN arbitration mechanisms. As a result, a higher priority is given to the data traffic initiated by these initiators. The VIP VPDMA can directly drive such MFLAG signals dynamically. The MFLAG generation for VIP VPDMA is enabled by default, and there is no register control over it.

The VPDMA arbitrates between multiple DMA sources within the VIP based on FIFO levels of DMA channels connected to VPDMA. Priority escalation mechanism implemented within VIP subsystem is based on overflow threshold and FIFO margin.

The following is a summary of priority and MFLAG levels provided by the VIP:

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- High priority (MFLAG = 3) when FIFO margin is below 25%
- Medium priority (MFLAG = 1) when FIFO margin is between 25% and 50%
- Low priority (MFLAG = 0) when FIFO margin is above 50%

Additionally, the VIP subsystem also generates MReqPriority based upon a programmed descriptor configuration. The MReqPriority configuration influences the arbitration mechanism in the Memory Subsystem only and has no influence on the arbitration that takes place within L3_MAIN interconnect. For more information see Section 9.4.8.7.1.4, *Data Packet Descriptor Word 3*.

9.4.8.6 VPDMA Interrupts

The VPDMA has 4 interrupt group(s). Each group has an interrupt for all the client interrupts, an interrupt for every 32 channels, a interrupt for each list complete, an interrupt for each list notify and an interrupt for for all of the descriptor interrupts. Each of these groups can be individually masked so that only the interrupts specified will trigger the higher level interrupt.

Each interrupt source can be individually masked independently for each seperate interrupt group. A status register bit exists for each interrupt source for for each interrupt group, that is set whenever the interrupt event occurs even when if the interrupt is masked. The status register bit will remain set until cleared by software by writing a one to the status bit.

Table 9-34 shows all interrupt events from VPDMA that go to VIP top level. The interrupt events are mapped to two interrupt lines, INT0 and INT1, that go to VIP top level.

Table 9-34. VPDMA Interrupt Events

Interrupt	Event Flag Registers	Event Mask Registers	Description
vpdma_int_channel_group0	VIP_INT0_CHANNEL0_INT_STAT VIP_INT1_CHANNEL0_INT_STAT	VIP_INT0_CHANNEL0_INT_MASK VIP_INT1_CHANNEL0_INT_MASK	An unmasked channel interrupt for interrupt group 0 in channel register 0 or 1 has fired.
vpdma_int_channel_group1	VIP_INT0_CHANNEL1_INT_STAT VIP_INT1_CHANNEL1_INT_STAT	VIP_INT0_CHANNEL1_INT_MASK VIP_INT1_CHANNEL1_INT_MASK	An unmasked channel interrupt for interrupt group 1 in channel register 0 or 1 has fired.
vpdma_int_channel_group2	VIP_INT0_CHANNEL2_INT_STAT VIP_INT1_CHANNEL2_INT_STAT	VIP_INT0_CHANNEL2_INT_MASK VIP_INT1_CHANNEL2_INT_MASK	An unmasked channel interrupt for interrupt group 2 in channel register 0 or 1 has fired.
vpdma_int_channel_group3	VIP_INT0_CHANNEL3_INT_STAT VIP_INT1_CHANNEL3_INT_STAT	VIP_INT0_CHANNEL3_INT_MASK VIP_INT1_CHANNEL3_INT_MASK	An unmasked channel interrupt for interrupt group 3 in channel register 0 or 1 has fired.
vpdma_int_channel_group4	VIP_INT0_CHANNEL4_INT_STAT VIP_INT1_CHANNEL4_INT_STAT	VIP_INT0_CHANNEL4_INT_MASK VIP_INT1_CHANNEL4_INT_MASK	An unmasked channel interrupt for interrupt group 4 in channel register 0 or 1 has fired.
vpdma_int_channel_group5	VIP_INT0_CHANNEL5_INT_STAT VIP_INT1_CHANNEL5_INT_STAT	VIP_INT0_CHANNEL5_INT_MASK VIP_INT1_CHANNEL5_INT_MASK	An unmasked channel interrupt for interrupt group 5 in channel register 0 or 1 has fired.
vpdma_int_list0_complete			List 0 has completed
vpdma_int_list0_notify			The data transfer in list 0 with the Notify Field set in the descriptor has completed
vpdma_int_list1_complete			List 1 has completed

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Table 9-34. VPDMA Interrupt Events (continued)

Interrupt	Event Flag Registers	Event Mask Registers	Description
vpdma_int_list1_notify			The data transfer in list 1 with the Notify Field set in the descriptor has completed
vpdma_int_list2_complete			List 2 has completed
vpdma_int_list2_notify			The data transfer in list 2 with the Notify Field set in the descriptor has completed
vpdma_int_list3_complete			List 3 has completed
vpdma_int_list3_notify			The data transfer in list 3 with the Notify Field set in the descriptor has completed
vpdma_int_list4_complete	VIP_INT0_LIST0_INT_STAT VIP_INT1_LIST0_INT_STAT	VIP_INT0_LIST0_INT_MASK VIP_INT1_LIST0_INT_MASK	List 4 has completed
vpdma_int_list4_notify			The data transfer in list 4 with the Notify Field set in the descriptor has completed
vpdma_int_list5_complete			List 5 has completed
vpdma_int_list5_notify			The data transfer in list 5 with the Notify Field set in the descriptor has completed
vpdma_int_list6_complete			List 6 has completed
vpdma_int_list6_notify			The data transfer in list 6 with the Notify Field set in the descriptor has completed
vpdma_int_list7_complete			List 7 has completed
vpdma_int_list7_notify			The data transfer in list 7 with the Notify Field set in the descriptor has completed
vpdma_int_client	VIP_INT0_CLIENT0_INT_STAT VIP_INT0_CLIENT1_INT_STAT VIP_INT1_CLIENT0_INT_STAT VIP_INT1_CLIENT1_INT_STAT	VIP_INT0_CLIENT0_INT_MASK VIP_INT0_CLIENT1_INT_MASK VIP_INT1_CLIENT0_INT_MASK VIP_INT1_CLIENT1_INT_MASK	Client Interrupt
vpdma_int_descriptor	VIP_INT0_LIST0_INT_STAT VIP_INT1_LIST0_INT_STAT	VIP_INT0_LIST0_INT_STAT VIP_INT1_LIST0_INT_STAT	Descriptor Interrupt

In Table 9-34 above, the “channel_group”, “client” and “descriptor” interrupts are actually a set of additional interrupts. When software receives an interrupt from a “channel_group,” “client,” or “descriptor” it must read the appropriate register within the VPDMA (refer to Table 9-35 to determine what the actual interrupt was).

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Table 9-35. VIP Interrupt Sources

Interrupt	Interrupt Group	Description
channel_vip1_mult_anca_src0	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src1	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src10	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src11	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src12	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src13	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src14	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src15	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src2	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src3	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src4	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src5	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_anca_src6	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src7	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src8	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src9	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_ancb_src0	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src1	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src10	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src11	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src12	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src13	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src14	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src15	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_ancb_src2	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src3	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src4	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src5	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src6	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src7	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src8	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src9	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_porta_src0	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src1	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src10	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src11	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_porta_src12	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src13	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src14	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src15	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src2	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src3	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src4	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src5	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src6	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src7	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src8	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src9	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_portb_src0	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src1	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src10	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src11	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src12	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src13	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src14	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src15	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src2	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src3	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src4	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src5	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_portb_src6	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src7	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src8	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src9	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_porta_chroma	channel_group3	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_porta_luma	channel_group3	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_porta_rgb	channel_group3	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point.
channel_vip1_portb_chroma	channel_group3	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_portb_luma	channel_group3	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_portb_rgb	channel_group3	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip2_mult_anca_src0	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src1	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_anca_src10	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src11	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src12	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src13	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src14	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src15	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src2	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src3	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src4	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src5	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src6	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src7	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_anca_src8	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src9	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_ancb_src0	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src1	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src10	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src11	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src12	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src13	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src14	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src15	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src2	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src3	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_ancb_src4	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src5	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src6	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src7	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src8	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src9	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_porta_src0	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src1	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src10	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src11	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src12	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src13	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_porta_src14	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src15	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src2	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src3	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src4	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src5	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src6	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src7	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src8	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src9	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_portb_src0	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src1	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_portb_src10	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src11	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src12	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src13	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src14	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src15	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src2	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src3	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src4	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src5	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src6	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src7	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_portb_src8	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src9	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_porta_chroma	channel_group5	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_porta_luma	channel_group5	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_porta_rgb	channel_group5	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point.
channel_vip2_portb_chroma	channel_group5	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_portb_luma	channel_group5	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_portb_rgb	channel_group5	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
client_vip1_anc_a	client	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_anc_b	client	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_lo_uv	client	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_lo_y	client	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
client_vip1_up_uv	client	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_up_y	client	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_anc_a	client	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_anc_b	client	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_lo_uv	client	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_lo_y	client	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_up_uv	client	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_up_y	client	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vpi_ctl	client	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
control_descriptor_int0	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0.
control_descriptor_int1	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1.
control_descriptor_int10	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10.
control_descriptor_int11	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11.
control_descriptor_int12	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12.
control_descriptor_int13	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13.
control_descriptor_int14	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14.
control_descriptor_int15	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15.

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Table 9-35. VIP Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
control_descriptor_int2	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2.
control_descriptor_int3	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3.
control_descriptor_int4	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4.
control_descriptor_int5	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5.
control_descriptor_int6	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6.
control_descriptor_int7	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7.
control_descriptor_int8	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8.
control_descriptor_int9	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9.
list0_complete	list0_complete	List 0 has completed
list0_notify	list0_notify	The data transfer in list 0 with the Notify Field set in the descriptor has completed
list1_complete	list1_complete	List 1 has completed
list1_notify	list1_notify	The data transfer in list 1 with the Notify Field set in the descriptor has completed
list2_complete	list2_complete	List 2 has completed
list2_notify	list2_notify	The data transfer in list 2 with the Notify Field set in the descriptor has completed
list3_complete	list3_complete	List 3 has completed
list3_notify	list3_notify	The data transfer in list 3 with the Notify Field set in the descriptor has completed
list4_complete	list4_complete	List 4 has completed
list4_notify	list4_notify	The data transfer in list 4 with the Notify Field set in the descriptor has completed
list5_complete	list5_complete	List 5 has completed
list5_notify	list5_notify	The data transfer in list 5 with the Notify Field set in the descriptor has completed
list6_complete	list6_complete	List 6 has completed
list6_notify	list6_notify	The data transfer in list 6 with the Notify Field set in the descriptor has completed
list7_complete	list7_complete	List 7 has completed
list7_notify	list7_notify	The data transfer in list 7 with the Notify Field set in the descriptor has completed

9.4.8.7 VPDMA Descriptors

The VPDMA needs to be programmed through descriptors (a pre-defined structure of eight or four 32-bit words depending on type of descriptors) other than VPDMA Memory Mapped Registers (MMR). Descriptors are of three types:

(i) **Data Transfer Descriptors** - A memory structure used to describe a desired memory transaction to or from a client.

(ii) **Control Descriptors** - A memory structure used to perform a control operation inside the DMA controller

(iii) **Configuration Descriptors** - A memory structure used to described a setup that should be applied to an processing modules like MMR write, scalar coefficient write etc.

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9.4.8.7.1 Data Transfer Descriptors

In order to set up data transfers from the VPDMA, a data transfer descriptor is added into a list. The fields used for an Inbound and Outbound descriptor vary slightly. An outbound transfer can have two different outbound transfers. The two transfers are the main data transfer and a write of an Inbound Descriptor. The created inbound descriptor is formatted so it can be read back in directly to the next channel specified in the original descriptor.

Figure 9-95. Inbound Data Transfer Descriptor Format

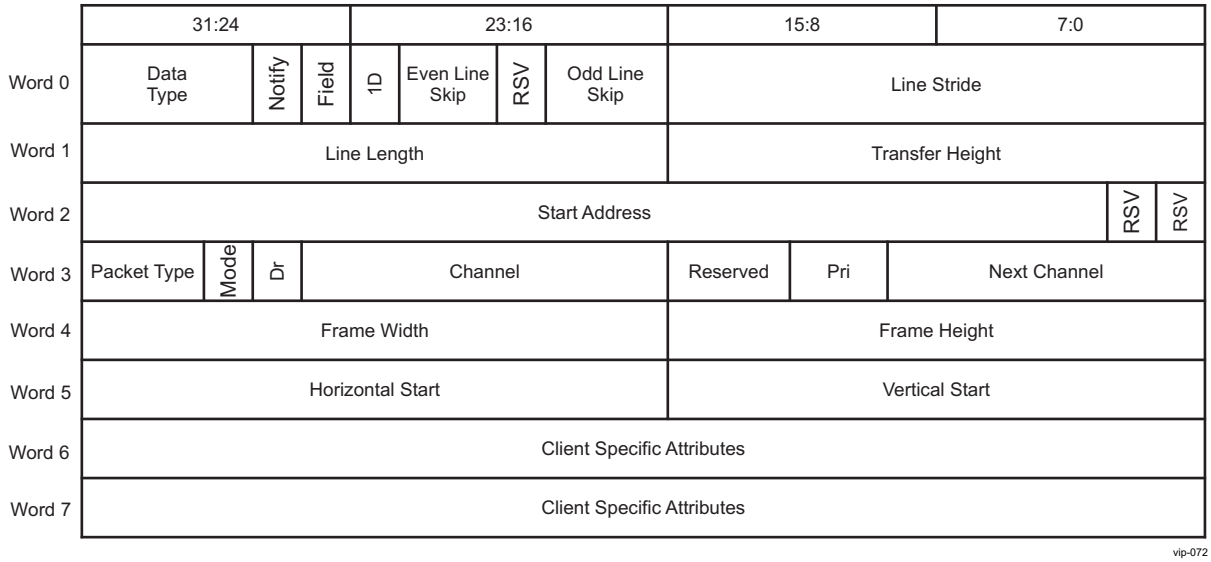
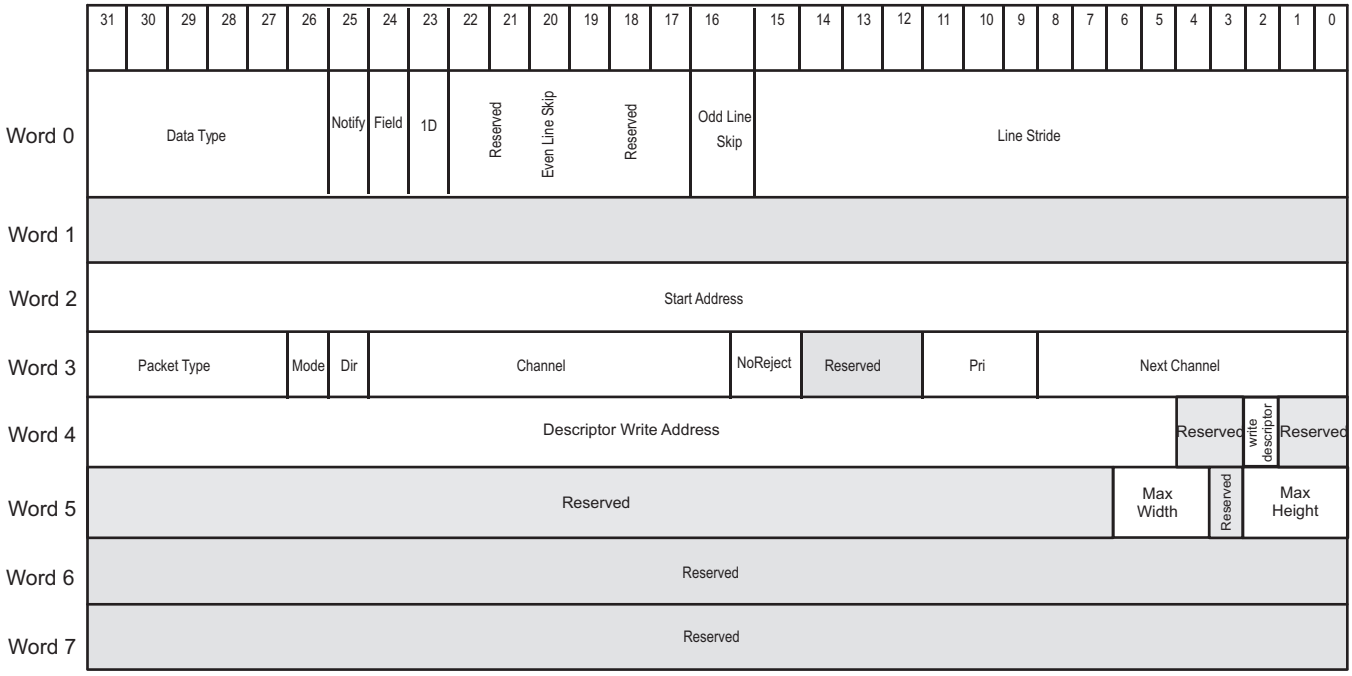


Figure 9-96. Outbound Data Transfer Descriptor Format



The general data transfer Descriptor formats can be seen in the above figures. The descriptor consists of 8 × 32bit words. A Data Transfer Descriptor will be removed from the list when the resource specified by the Channel field is free. If the Channel is not free when the list reaches a data transfer descriptor then the list will stall until the current transfer on the channel has completed.

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9.4.8.7.1.1 Data Packet Descriptor Word 0 (Data)

Table 9-36. Data Packet Descriptor Word 0 Field Descriptions

Bit	Field	Value	Description
31:26	Data Type		**Miscellaneous Channel**
			Sets the pixel size in bits plus 1
			RGB Channel
		0	RGB16-565
		1h	ARGB-1555
		2h	ARGB-4444
		3h	RGBA-5551
		4h	RGBA-4444
		5h	ARGB24-6666
		6h	RGB24-888
		7h	ARGB32-8888
		8h	RGBA24-6666
		9h	RGBA32-8888
		10h	BGR16-565
		11h	ABGR-1555
		12h	ABGR-4444
		13h	BGRA-5551
		14h	BGRA-4444
		15h	ABGR24-6666
		16h	BGR24-888
		17h	ABGR32-8888
		18h	BGRA24-6666
		19h	BGRA32-8888
			YUV Channel
		0	Y 4:4:4
		1	Y 4:2:2
		2	Y 4:2:0
		4	C 4:4:4
		5	C 4:2:2
		6	C 4:2:0
		7	CY 4:2:2
		8	YCbC 4:4:4
		14h	Cb 4:4:4
		15h	Cb 4:2:2
		16h	Cb 4:2:0
		17h	CbY 4:2:2
		27h	YC 4:2:2
		37h	YCb 4:2:2
25	Notify	0-1	Send List Notification Interrupt upon last transfer of this channel
24	Field	0-1	Field Value
23	1D	0	The transfer is one dimensional. The transfer and frame sizes are combined to make a single 32 bit transfer size. For writes this value is passed to the generated descriptor. This feature is not supported by all clients. Only clients that support the feature will recognize this bit. **Note:** 1D mode is not supported by VIP modules

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Table 9-36. Data Packet Descriptor Word 0 Field Descriptions (continued)

Bit	Field	Value	Description
22:20	Even Line Skip		Field Value
		0	+1 line
		1h	+2 lines
		2h-7h	Reserved
19	Reserved		Reserved for future use
18:16	Odd Line Skip		Field Value
		0	+1 line
		1h	+2 lines
		2h-7h	Reserved
15:0	Line Stride	0-FFFFh	Address stride between lines in bytes

9.4.8.7.1.1.1 Data Type

Bits 31-26 indicate the type of data that is to be transferred. This value is used to compute the number of bytes per pixel so that transactions may be made for the appropriate amount of data. The types of data are dependent on the type of channel. The VPDMA descriptor data types RGB or YUV are defined associated with the VPDMA channel assignment. This helps the engine to distinguish between the overlapping values of the descriptor data types for RGB and YUV data.

- For the Miscellaneous channel, the Data Type selects the size in bits of the data. The range is from 0 to 63 to represent the sizes from 1 to 64 bits.
- For a YUV channel, the Data Type determines, if the data channel is interleaved or color space separate. If color spaced separate, it is still assumed that the two chroma pixels are interleaved.

CAUTION

VPDMA defines the component ordering for its RGB data types in the opposite direction of what commonly used image identifiers expect. To avoid color component swapping in the display and/or in the video/image data written out to the memory, the proper Data Type settings for both RGB and YUV data types must be made. The following paragraphs provide more details on how to set Data Type correctly, in order to match the data stored or expected in the memory.

Setting RGB Data Types

The commonly used RGB format identifiers require the color components to be stored in a little-endian style, where the left most component is the LSB component.

- For an ARGB data type, the A component is the LSB location, as shown in Table 9-37 and Table 9-38;
- For a BGRA data type, the B component would be in the LSB location;

Table 9-37. Common ARGB in Memory (Byte Order)

Addr (LSB)	Addr + 1	Addr + 2	Addr + 3 (MSB)
A	R	G	B

Table 9-38. Common ARGB in 32-bit Memory/CPU Register

Bit 31	Bit 23	Bit 15	Bit 7
B	G	R	A

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VPDMA specifies its component ordering in the big-endian style, which requires the data to be stored in the reversed order. Example with ARGB data type is shown in Table 9-39 and Table 9-40. The VPDMA ordering for ARGB data type matches the common BGRA data format.

Table 9-39. VPDMA ARGB in Memory (Byte Order)

Addr (LSB)	Addr + 1	Addr + 2	Addr + 3 (MSB)
B	G	R	A

Table 9-40. VPDMA ARGB in 32-bit Memory/CPU Register

Bit 31	Bit 23	Bit 15	Bit 7
A	R	G	B

In order color components to be mapped correctly and to avoid swapping, the reversal must be taken into consideration when configuring the Data Type in the VPDMA transfer descriptor.

Table 9-41 shows the proper settings required for RGB data types for both storage schemes.

Table 9-41. VPDMA Descriptor RGB Data Type Mapping

Source/Destination Image		VPDMA Data Type Mapping Value	
RGB Component order	Common Image Format Names	**Column A** Source data stored in the VPDMA defined order	**Column B** Source data stored in the opposite of VPDMA defined order
RGB	RGB16-565	0x0	0x10
	ARGB-1555	0x1	0x13
	ARGB-4444	0x2	0x14
	RGBA-5551	0x3	0x11
	RGBA-4444	0x4	0x12
	ARGB24-6666	0x5	0x18
	RGB24-888	0x6	0x16
	ARGB32-8888	0x7	0x19
	RGBA24-6666	0x8	0x15
	RGBA32-8888	0x9	0x17
BGR	BGR16-565	0x10	0x0
	ABGR-1555	0x11	0x3
	ABGR-4444	0x12	0x4
	BGRA-5551	0x13	0x1
	BGRA-4444	0x14	0x2
	ABGR24-6666	0x15	0x8
	BGR24-888	0x16	0x6
	ABGR32-8888	0x17	0x7
	BGRA24-6666	0x18	0x5
	BGRA32-8888	0x19	0x9

In Table 9-41, if the application uses the same data type definition as the VPDMA (that is, RGB24 refers to the B in the LSB), the data types in Column A should be used. But, if the application expects the common data type component order for RGB data type names, the VPDMA data types in Column B should be used.

For example:

- To display an ARGB32-8888 source image data with A in the LSB, the data type in the descriptor should be set to 0x19. But, to display an ARGB32-888 source image data with B in the LSB, the data type in the descriptor should be set to 0x7.
- To capture and write out a RGB24-888 image in the memory with R in the LSB, the data type in the

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descriptor should be set to 0x16 (this case assumes the VIP VIN d[23:0] data input is mapped to RGB bus with B component in the LSB).

Setting YUV Data Types

There is no component order reversal for YUV data types. The VPDMA uses generic data type names to specify the memory storage format and the application simply needs to follow the VPDMA defined ordering.

Table 9-42 shows how common YUV data types map to the VPDMA YUV data types in order to clarify the YUV data type configuration.

Table 9-42. VPDMA Descriptor YUV Data Type Mapping

Source YUV Image Types			VPDMA Data Type Mapping (Value)		
Chroma Sub-sample	Common YUV Image Format Type Names	Memory Packed Order [MSB - LSB]	Luma/Chroma Interleaved Channel	Luma-only Channel	Chroma-only Channel
444	YUV	V U Y	YC 4:4:4 (0x8)		
	UVY	Y V U	Cb 4:4:4 (0x14)		
422	NV16 (YUV422SP_UV)	V U		Y 4:2:2 (0x1)	C 4:2:2 (0x5)
	NV16 (YUV422SP_VU)	U V		Y 4:2:2 (0x1)	Cb 4:2:2 (0x15)
	YUV2/YUYV/V422 (YUV422I_YUYV)	V Y U Y	YC 4:2:2 (0x7)		
	YUV422I_YVYU	U Y V Y	CbY 4:2:2 (0x17)		
	Y422/UYVY (YUV422I_UYVY)	Y V Y U	YC 4:2:2 (0x27)		
	YUV422I_VYUY	Y U Y V	YCb 4:2:2 (0x37)		
420	NV12 (YUV420SP_UV)	V U		Y 4:2:0 (0x2) YC 4:2:2 (0x7) (see (1))	C 4:2:0 (0x6) YC 4:2:2 (0x7) (see (1))
	NV21 (YUV420SP_VU)	U V		Y 4:2:0 (0x2) YC 4:2:2 (0x7) (see (1))	Cb 4:2:0 (0x16) YC 4:2:2 (0x7) (see (1))

(1) If 422 source data is used, unused component data fetched (either Luma or Chroma) will be discarded.

For further details on the data formats, refer to Section 9.4.8.9, *VPDMA Data Formats*.

9.4.8.7.1.1.2 Notify

The Notify bit is used in conjunction with the Notify interrupts and when the channel has completed the DMA transfer the Notify Interrupt for the list that contains the descriptor will fire. The last Notify bit set for a specific list will be used so only a single Notify should be set in a list.

9.4.8.7.1.1.3 Field

The Field bit is the field value of the data that will be passed down to the clients. If the data is interlaced, then this value should be cleared to 0.

9.4.8.7.1.1.4 Even Line Skip

The Even Line skip is used with Line Stride to generate the next line address on an even line. All frames start on line 0. This value allows for the DMA controller to skip lines for interlaced data in a progressive frame buffer.

9.4.8.7.1.1.5 Odd Line Skip

The Odd Line skip is used with Line Stride to generate the next line address on an odd line. All frames start on line 0, so this will apply starting with the second line. This value allows for the DMA controller to skip lines for interlaced data in a progressive frame buffer.

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9.4.8.7.1.1.6 Line Stride

Bits 15:0 are the stride between lines in bytes at the external address. This value is added or subtracted based upon an adjustment using the current skip value. Operation of the external address pointer shall load the Source Address upon start of the transfer, then at the end of each line increment or decrement by the value computed using the Line Stride and Skip value for the line. The line stride must be aligned to an L3 data bus width. The lower bits of the stride will always be treated as zero to force the alignment.

9.4.8.7.1.2 Data Packet Descriptor Word 1

Table 9-43. Data Packet Descriptor Word 1 Field Description

Bits	Name	Description
31:16	Line Length	Line Length in Pixels
15:0	Transfer Height	Number of rows in transfer.

9.4.8.7.1.2.1 Line Length

Bits 31-16 are the line length in pixels of the current channel. This is ignored for the outbound transfer as the client will provide the line length with the end of line signal on the client interface. The maximum supported line length is currently 4096.

9.4.8.7.1.2.2 Transfer Height

Bits 15-0 are the number of lines to be transferred in the current channel. This is ignored for outbound transfers as the client will provide the line length with the end of frame signal on the client interface. The maximum supported transfer size is currently 2048.

9.4.8.7.1.3 Data Packet Descriptor Word 2

Table 9-44. Data Packet Descriptor Word 2 Field Descriptions

Bit	Field	Value	Description
31:0	Start Address		32-bit data source address [31:0]
			If Mode is TILED, then TILER specific ADDRESS Map is used:
			Bits 31-29:
		0	0-degree view
		1h	180-degree view + mirroring
		2h	0-degree view + mirroring
		3h	180-degree view
		4h	270-degree view + mirroring
		5h	270-degree view
		6h	90-degree view
		7h	90-degree view + mirroring
			Bits 28-27:
		0	8-bit container
		1h	16-bit container
		2h	32-bit container
		3h	Page Mode
			If Mode is NORMAL, then bits 31-26 are the upper bits of the address.

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9.4.8.7.1.3.1 Start Address

This is the byte aligned address for the first data transfer. The address on the OCP bus will always be word aligned.

9.4.8.7.1.4 Data Packet Descriptor Word 3

Table 9-45. Data Packet Descriptor Word 3 Field Descriptions

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = 0xa
26	Mode	0= Normal, 1=TILED
25	Direction	Inbound = 0, Outbound = 1
24:16	Channel	Channel for which this descriptor describes
15	Reserved	Reserved for future use
11:9	Priority	Only Bit 9 and Bit 11 are used to set the priority. Bit 10 is ignored. Highest = 0, Lowest = 3 By default, hardware assigns priority = 3. This priority level is used in the arbitration between the masters (for DDR access). See Section 9.4.8.7.1.4.5, *Priority*, for more details.
8:0	Next Channel	Next Channel to execute on a line or the channel to use in the generated write descriptor.

9.4.8.7.1.4.1 Packet Type

Bits 31:27 are a unique code which indicates that this Descriptor is a VPDMA descriptor.

9.4.8.7.1.4.2 Mode

Bit 26 is used to indicate if the transfer is to regular memory space or to Tiled memory space. The VPDMA will use this to determine if it does standard raster based addressing or if it assumes that the data is stored in TILER format. If data is stored in TILER format then the buffer is turned into 2 or 4 line buffers depending on the container type. For shared clients that use the memory, such as the ancillary data and the VIP port, only one can be active, if the mode field is set. Only clients that support Tiling will properly pack the data for tiling on the output interface. This must only be set for channels going to clients that support the TILING feature in the client configuration.

9.4.8.7.1.4.3 Direction

Bit 25 is used to indicate the direction of transfer. This bit indicates that the data flow is from an external source to an internal buffer (inbound) or data transfers form an internal buffer to an external location (outbound).

9.4.8.7.1.4.4 Channel

Bits 24:16 are the Channels which is supported by the descriptor. This is the identification of the specific Channel which is controlled by the contents of the descriptor. The channel assignments can be found in the channel table.

9.4.8.7.1.4.5 Priority

Bits 11:9 are set to indicate priority of the transfer, these are directly mapped to the OCP reqinfo bits.

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9.4.8.7.1.4.6 Next Channel

Bits 8:0 give the next channel to use to create a composite frame. The next channel must be to a free channel. The last channel of a row should point back to the initial channel which must be a channel tied directly to a client. The Descriptor for the Next Channel must be of the same type as the current descriptor.

9.4.8.7.1.5 Data Packet Descriptor Word 4

9.4.8.7.1.5.1 Inbound data

Table 9-46. Data Packet Descriptor Word 4 Inbound Data Field Descriptions

Bits	Name	Description
31:16	Frame Width	Width of the client frame.
15:0	Frame Height	Height of the client frame

9.4.8.7.1.5.1.1 Frame Width

Bits 31:16 indicate the width in pixels of the frame. This is the width of the entire frame and not just the width of the data represented by the current channel unless this channel fills the entire frame. This allows for the VPDMA to present a larger frame of data to the client while only fetching the required data. The currently supported maximum width is 4096.

9.4.8.7.1.5.1.2 Frame Height

Bits 15:0 indicate the height in pixels of the entire frame. This is the height of the entire frame and not just the height of the data represented by the current channel unless this channel fills the entire frame. This allows for the VPDMA to present a larger frame of data to the client while only fetching the required data. The currently supported maximum height is 2048.

9.4.8.7.1.5.2 Outbound data

Table 9-47. Data Packet Descriptor Word 4 Outbound Data Field Descriptions

Bits	Name	Description
31:5	Descriptor Write Address	The 32 byte aligned location to write an inbound descriptor
2	Write Descriptor	If set to 1, a descriptor will be generated when the client completes a frame.
1	Drop Data	If set to 1, the data will not be written out. Also, if this is set, the write descriptor bit must be set. This allows for descriptors to only be written out so that software can determine the size of the required buffer before data is written out.
0	Use Descriptor Register	If set to 1, the CURRENT_DESCRIPTOR register will be used for the write address location. If set to 0, the Descriptor Write Address field in this word will be used for the Descriptor Write Address.

9.4.8.7.1.5.2.1 Descriptor Write Address

Bits 31:5 set the 32 byte address to write the generated descriptor. This address is only used if the Write Descriptor bit is set to 1 and the Use Descriptor Register bit is set to 0. If this case is met when the channel is complete a descriptor that meets the inbound descriptor format will be written to the location specified by this field. This allows for software to have a specific channel write its descriptor to a specific address no matter what order the channel completes compared to other outbound channels.

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9.4.8.7.1.5.2.2 Write Descriptor

Bit 2 determines if a descriptor should be written out when the client is completed. If this bit is set the descriptor will be written. The format of the descriptor will be of an Inbound Data Transfer descriptor with the LINE LENGTH and TRANSFER HEIGHT fields determined by the counters in the clients. This means that the direction bit will be the opposite of the inbound descriptor. The FRAME WIDTH and FRAME HEIGHT values will match the LINE LENGTH and TRANSFER HEIGHT fields. The CHANNEL and NEXT CHANNEL fields will match the NEXT CHANNEL field of the original descriptor. The FIELD bit will match the source field captured by the client. The NOTIFY bit will always be 0. All other fields will match the original outbound descriptor. If the Outbound descriptor MODE is set to TILED data then the descriptor address used will be in TILED data space and software must ensure that the address is in page mode for the address of the descriptor.

9.4.8.7.1.5.2.3 Drop Data

Bit 1 determines if the data should be written out or not. In some cases software might only want to write the descriptor out to determine the size of the buffer that will be required to store incoming data. By setting this bit,no data will be written out. If this bit is set then the Write Descriptor bit MUST be set. Bit 0 determines where the descriptor should be written.

9.4.8.7.1.6 Data Packet Descriptor Word 5

9.4.8.7.1.6.1 Outbound data

Width and Height are set in the following register bit-fields:

- For Max_Size1: VIP_MAX_SIZE1[31:16] MAX_WIDTH and VIP_MAX_SIZE1[15:0] MAX_HEIGHT registers
- For Max_Size2: VIP_MAX_SIZE2[31:16] MAX_WIDTH and VIP_MAX_SIZE2[15:0] MAX_HEIGHT registers
- For Max_Size3: VIP_MAX_SIZE3[31:16] MAX_WIDTH and VIP_MAX_SIZE3[15:0] MAX_HEIGHT registers

Table 9-48. Data Packet Descriptor Word 5 Outbound Data Field Descriptions

Bits	Name	Description
6:4	Max Width	The maximum allowable pixels per line. 0: Unlimited Line Size
		1: Use Max_Size1 Max Width field
		2: Use Max_Size2 Max Width field
		3: Use Max_Size3 Max Width field
		4: 352 pixels
		5: 768 pixels
		6: 1280 pixels
		7: 1920 pixels
		Others: Reserved
2:0	Max Height	The maximum allowable lines per frame. 0: Unlimited Frame Size
		1: Use Max_Size1 Max Height field
		2: Use Max_Size2 Max Height field
		3: Use Max_Size3 Max Height field
		4: 288 lines
		5: 576 lines
		6: 720 lines
		7: 1080 lines
		Others: Reserved

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9.4.8.7.1.6.1.1 Max Width

Bits 6:4 are encoded to set the maximum transferred line size. If the field is not set to unlimited if the client sending data into the VPDMA exceeds the maximum allowed pixels the data will continue to be received from the client but will not be sent to external memory until an end of line is received from the client sending data. The outbound descriptor if created will still have the transmitted size of the last line of the frame which will match the max width. If the frame does not exceed the max width then the actual transmitted size will be placed in the descriptor. Tiled clients such as the noise filter should always set this to 0. If Max Width is 0 and the line size is larger then 4096 pixels then the address counters will overflow and the data at the start of the line will be overwritten.

9.4.8.7.1.6.1.2 Max Height

Bits 2:0 are encoded to set the maximum transferred frame size. If the field is not set to unlimited if the client sending data into the VPDMA exceeds the maximum allowed lines the data will continue to be received from the client but will not be sent to external memory until an end of frame is received from the client sending data. The outbound descriptor if created will still have the transmitted number of lines received which would match the max height. If the frame does not exceed the max height then the actual transmitted size will be placed in the descriptor. Tiled clients such as the noise filter should always set this to 0.

9.4.8.7.2 Configuration Descriptor

The Configuration Descriptor is used in a List to setup a client configuration. The configuration descriptor consists of a header and a payload portion. The payload can either be part of the list that the descriptor is contained in or it can be at a separate location. The VPDMA will pass the payload of the configuration descriptor down to the client over the VPI Control port interface or through the MMR configuration port depending on the destination field. A Configuration Descriptor to any single destination except Destination 0 must be on a single list. Configuration Descriptors to different destinations may be on different lists..

The Configuration Descriptor Header is 4 × 32 bit words. A configuration descriptor is not consumed until the destination specified has received the entire configuration payload. Therefore the list is expected to stall while the configuration takes place. This ensures that all descriptors after a configuration descriptor in the list will occur after the desired configuration.

9.4.8.7.2.1 Configuration Descriptor Header Word0

Table 9-49. Configuration Descriptor Header Word0 Field Descriptions

Bits	Name	Description
31:0	Address Offset of the Destination	This is the address offset location in the destination that the block of data in the payload should be written. This field is only used if the descriptor Class is a block type. Otherwise this field is reserved.

9.4.8.7.2.2 Configuration Descriptor Header Word1

Table 9-50. Configuration Descriptor Header Word1 Field Descriptions

Bits	Name	Description
15:0	Number of Data Words	Length of First Data Packet for Class 1(block).

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9.4.8.7.2.2.1 Number of Data Words

Bits 15:0 indicate the length of the first data block if the class is 1 as specified in Configuration Descriptor Header Word3. If the class is not 1 then this field should be set to 0.

9.4.8.7.2.3 Configuration Descriptor Header Word2

Table 9-51. Configuration Descriptor Header Word2 Field Descriptions

Bits	Name	Description
31:0	Payload Location	Pointer to the data payload

9.4.8.7.2.3.1 Payload Location

Bits 31:0 contain the pointer to the data payload if the command packet is an indirect type. This value along with the Payload Length will be combined to issue a DMA transaction that must complete before the List Manager can finish processing this descriptor. The list will be made inactive pending this DMA completion. This address should be on a 16 byte boundary so the lower 4 bits should always be 0.

9.4.8.7.2.4 Configuration Descriptor Header Word3

Table 9-52. Configuration Descriptor Header Word3 Field Descriptions

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = 0xb
26	Direct	Direct Command = 1 Indirect Command = 0
25:24	Class	0 = Address, Data Set 1 = Block 2,3 Reserved for Future Use
23:16	Destination	Destination of the configuration payload
15:0	Payload Length	Length of Payload in Words.

9.4.8.7.2.4.1 Packet Type

Bits 31:27, this field indicates the type of descriptor and should be set 0xB for configuration descriptor.

9.4.8.7.2.4.2 Direct

Bit 26, this field indicates that the descriptor is a direct command or indirect command. A direct command means that the payload is contiguous with the descriptor and will be pulled in by the list manager descriptor control as it processes the list. A direct payload must end on or before a 256 byte boundary in the list. An indirect command is when the Address is located in Word2 is a pointer to the data payload. A DMA transaction will be scheduled to bring the payload into the List Manager to allow for the payload to be sent to the destination.

9.4.8.7.2.4.3 Class

Bits 25:24, this field indicates the type of payload is associated with command descriptor, and thus how to handle the payload.

A 0 indicates that the payload consists of blocks of data with each block having an address and length. The first word after a sub-block contains the next address and length in bytes. This allows for writing to multiple configuration regions in a client. The Configuration Descriptor word1 is the first address and length pair. All addresses used must be larger then the previous address for all destinations except for the MMR destination. If a sub block length is not evenly divisible into 16 then zeroes should be padded in the payload so that the Next Client Address and Length field start on a 16 byte boundary.

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9.4.8.7.2.4.3.1 Address Data Block Format

Table 9-53. Address Data Block Format Field Descriptions

Bits	Name	Description
31-0		Next Client Address
31-0		Configuration for Next Client Address
31-0		Configuration for Next Client Address + 4
31-0		Configuration for Next Client Address + 8
31-0		Configuration for Next Client Address + 12
31-0		Configuration for Next Client Address + 16
31-0		Next Client Address 2
15-0		Sub Block Length

A 1 indicates the payload is simply block data. The data is contiguous and starts at the offset of the destination as specified in word1.

9.4.8.7.2.4.4 Destination

The Destination field is used to determine where the configuration payload should be sent. The values for the destination field can be seen in the table below.

Table 9-54. Destination Field Description

Destination Value	Actual Destination	Description
0	mmr_client	Write to MMR registers to setup other modules
7	VIP Slice 0	VIP Slice 0 Scaler Coefficient Tables
8	VIP Slice 1	VIP Slice 1 Scaler Coefficient Tables

9.4.8.7.2.4.5 Descriptor Length

Bits 15:0, this field indicates the size of the payload in words for the command. This is 128 bit words. The maximum number of words is 1023 words in a single payload

9.4.8.7.3 Control Descriptor

9.4.8.7.3.1 Generic Control Descriptor Format

A control descriptor is the mechanism that is used in a list to give commands to the List Manager. These descriptors are not considered consumed until the List Manager has done the instruction required by the descriptor. All control descriptors have a common Header located at Word 3 but the remaining words are based on the specific control descriptor.

9.4.8.7.3.2 Control Descriptor Header Description

Table 9-55. Control Descriptor Header Description

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = 0xc
26:25	Reserved	Reserved
24:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	The type of control descriptor that should be run by the List Manager

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9.4.8.7.3.2.1 Packet Type

This field indicates a VPDMA control descriptor.

9.4.8.7.3.2.2 Source

The source is combined with the control field to determine what the control descriptor should use as the source for its synchronization event.

9.4.8.7.3.2.3 Control

The Control field defines the specific function of the descriptor. Table 9-56 lists the different control descriptors.

9.4.8.7.3.3 Control Descriptor Types

Table 9-56. Control Descriptor Types Summary

Control Descriptor	Control Field Value	Description
Sync on Client	0	Wait for the client attached to the channel specified to reach a certain event before proceeding.
Sync on List	1h	Wait for another list(s) to reach its Sync on List Descriptor
Sync on External Event	2h	Wait for a Register write to the LIST_STAT_SYNC bit specified or for an external event.
Sync on Channel	4h	Wait for the channel specified to complete
Change Client Interrupt	5h	Change the interrupt event for a client interrupt but do not wait for the event to occur.
Send Interrupt	6h	Generate an interrupt event on one of the Control Descriptor Interrupts
Reload List	7h	Reload the list from the location and size specified.
Abort Channel	8h	Abort the transfer in the channel specified.

9.4.8.7.3.3.1 Sync on Client

A Sync on Client Control descriptor uses the source field to select a channel to modify the attached clients interrupt generation event. For a client that supports multiple channels then only an event on the portion of the client that supports that client will cause the interrupt to be generation. After configuring the interrupt generation event the list will then stall until that event has occurred.

Table 9-57. Sync on Client Field Descriptions (Word - 1)

Bits	Name	Description
31:16	PIXEL_COUNT	Specify the pixel position on a line specified by LINE_COUNT where a pixel based event would occur.
15:0	LINE_COUNT	Specify the line where a line based event would trigger

Table 9-58. Sync on Client Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:24	Reserved	Reserved

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Table 9-58. Sync on Client Field Descriptions (Word - 3) (continued)

Bits	Name	Description
23:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	Control type = 0

9.4.8.7.3.3.2 Sync on List

The Sync on List Control descriptor is a mechanism to ensure that multiple lists have all reached a common point. The Sync on List descriptor uses the Source field as a mask for each list that should be synchronized which must include the list where the control descriptor resides. Once all lists specified in the source field have reached their Sync on List descriptor all lists will resume with the lowest list number resuming first. All Sync on List Control descriptors in each of the lists must have the same source field so that all lists will synchronize upon reaching that point.

If it is desired to synchronize list 0 and list 1 then the source field would be 0x3. If it is desired to synchronize list 1, list 3, and list 4 then the source field would be 0x1a. Word 0, Word 1 and Word 2 are reserved.

Table 9-59. Sync on List Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:24	Reserved	Reserved
23:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	Control type = 1h

9.4.8.7.3.3.3 Sync on External Event

A Sync on External Event descriptor ensures an external event has occurred before proceeding. The external event can be a write to a bit of the LIST_STAT_SYNC register or other external events that are determined at VPDMA elaboration to have occurred. This descriptor can be used to allow for external software to control progression of the list. The descriptor can also be used to select external signals that are brought into the VPDMA. The current implementation just synchronize on the LIST_STAT_SYNC bit for the list number that called the descriptor.

Table 9-60. Sync on External Event Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:4	Reserved	Reserved
3:0	Control	Control type = 2h

9.4.8.7.3.3.4 Sync on Channel

A Sync on Channel descriptor stalls the list until the channel specified is free. If the channel is already free then the descriptor will not cause the list to stall. Word 0, Word 1 and Word 2 are reserved.

Table 9-61. Sync on Channel Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:24	Reserved	Reserved

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Table 9-61. Sync on Channel Field Descriptions (Word - 3) (continued)

Bits	Name	Description
23:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	Control type = 4h

9.4.8.7.3.3.5 Sync on LM Timer

A Sync on LM Timer descriptor sets a value from the current timer position to wait. The LM timer is a free running counter at the LM processing clock. The Timer Value in the descriptor is added to the value of the timer at the time the descriptor is received and the list will stall for this many cycles before it becomes active again.

9.4.8.7.3.3.6 Change Client Interrupt

A Change Channel Interrupt Source descriptor uses the source field to select a channel to modify the attached clients interrupt generation event. The list will not stall on this descriptor. The format of the fields is identical to the Sync on Client Descriptor. Word 0 is reserved.

Table 9-62. Change Client Interrupt Field Descriptions (Word - 1)

Bits	Name	Description
31:16	PIXEL_COUNT	Specify the pixel position on a line specified by LINE_COUNT where a pixel based event would occur.
15:0	LINE_COUNT	Specify the line where a line based event would trigger.

Table 9-63. Change Client Interrupt Field Descriptions (Word - 2)

Bits	Name	Description
31:4	Reserved	Reserved
3:0	Event	Specify the event which should trigger the client interrupt.

Table 9-64. Change Client Interrupt Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:24	Reserved	Reserved
23:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	Control type = 5h

9.4.8.7.3.3.7 Send Interrupt

A Send Interrupt descriptor will cause the VPDMA to generate an interrupt on the list manager controlled interrupts as specified by the Source Field. The list will not stall on this descriptor. For example, if source is 0 then control_descriptor_int0 will fire. If source is 12, then control_descriptor_int12 will fire. For more information ot VPDMA interrupt events, see Section 9.4.8.6, *VPDMA Interrupts*.

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Table 9-65. Send Interrupt Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:24	Reserved	Reserved
23:16	Source	Specifies the source used for the control event.
15:4	Reserved	Reserved for future use
3:0	Control	Control type = 6h

9.4.8.7.3.3.8 Reload List

A Reload List descriptor causes ending descriptors after this descriptor in the original list to be dropped and a new list at the location and of the size specified in the descriptor. This descriptor can be used to allow for linked lists in the VPDMA as the list will continue from this point and fetch the list specified and it does not have to be continuous with the current list.

Table 9-66. Reload List Field Descriptions (Word - 0)

Bits	Name	Description
31:0	LIST_ADDRESS	31 most-significant Bits of the memory address where the descriptors to be loaded are stored. Address must be 16 byte aligned.

Table 9-67. Reload List Field Descriptions (Word - 1)

Bits	Name	Description
31:16	Reserved	Reserved
15:0	LIST_SIZE	Size of the list to load

Table 9-68. Reload List Field Descriptions (Word - 3)

Bits	Name	Description
31:27	Packet Type	Host Packet Descriptor Type = Ch
26:4	Reserved	Reserved
3:0	Control	Control type = 7h

9.4.8.7.3.3.9 Abort Channel

An Abort Channel descriptor is used to clear a channel. This clears the channel from issuing any more requests. Any outstanding requests for that channel will complete as originally scheduled. All data inside the client will be flushed. For Tiled Clients such as the noise filter it is required to issue two consecutive abort channel descriptors to ensure the channel is aborted for both the current tile and next tile. Word 0, Word 1 and Word 2 are reserved.

Table 9-69. Abort Channel Field Descriptions (Word - 3)

Bit	Name	Description
31:27	Packet Type	Host Packet Descriptor type = 0xC
26:24	Reserved	Reserved
23:16	Source	VPDMA Channel Number whose transfers are to be aborted
15:4	Reserved	Reserved
3:0	Control	Control type = 9h

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9.4.8.8 VPDMA Configuration

The following section describes the different ways of configuring VPDMA for data transfers.

9.4.8.8.1 Regular List

A regular list executes each descriptor in order until the end of the list is reached. When the end of the list is reached an interrupt is sent and the list can be reused by software. A regular list can contain any descriptor types. Software creates the list at some location in external memory. After completing writing the list software then writes the location of the list to the VIP_LIST_ADDR[31:0] VIP_LIST_ADDR register and then writes the VIP_LIST_ATTR register. If the NUMBER in the VIP_LIST_ATTR[26:24] LIST_NUM is not an active list then the List will be loaded and begin to execute the next time the List Manager gets to IDLE after processing previous loaded lists. If the NUMBER in the VIP_LIST_ATTR[26:24] LIST_NUM is busy then the VIP_LIST_ADDR and VIP_LIST_ATTR registers will be locked until the active list specified by NUMBER completes.

The different ports inside VPDMA requires different list setup, as explained in the following sections.

9.4.8.8.2 Video Input Ports

The Video Input Ports can be used in multiple ways. Depending on how the input ports are configured will determine how the lists to manage them need to be setup. The ways in which the ports can work are multiplexed data stream, single YUV color separate stream, dual YUV interleaved or single RGB stream. Each port also has an ancillary data port that can run either multiplexed or single data stream and shares the buffering with the main data stream. For all cases the descriptor must be loaded into the client before the vertical sync is received on the VIP port or the entire frame will be dropped. As with all write clients the VIP channels can be shadowed so the next frame/field descriptor can be loaded while the previous frame is running without stalling the list.

9.4.8.8.2.1 Multiplexed Data Streams

In the case of a multiplexed data stream input the channels that should be used are VIP(X)_MULT_PORT(Y)_SRC(Z). Where X is the specific VIP slice of the instance that wants to be used and port Y is the port A or port B that is receiving the data. Finally Z is the channel number. For Split line mux mode the LSB of the channel will determine, if the line is a split line or a complete line. This is required so that the data streams do not get mixed when a channel ends without completing a line. In this mode the data will always be sent out as 422 Interleaved data to the destination specified in the descriptor.

9.4.8.8.2.2 Single YUV Color Separate

If the port is configured to be used as sending out color separated YUV data then the channels that must be used are VIPX_PORTY_LUMA and VIPX_PORTY_CHROMA for the luma and chroma components respectively. The data type can be either 420 or 422 color separate in this case.

9.4.8.8.2.3 Dual YUV Interleaved

If the port is configured to be used to send out 422 interleaved data from a non-multiplexed source then the channels that must be used are VIPX_PORTY_LUMA or VIPX_PORTY_CHROMA depending on if the data stream is connected to the luma or chroma port. The data type must be 422 interleaved in this case.

9.4.8.9 VPDMA Data Formats

Each of the channels has a type of data that it can support based upon the client that it services. Also for each channel, the data type will assume that data is packed in memory a certain way and will be prevented to the client in the same manner to the client no matter what the format of the data in memory.

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9.4.8.9.1 YUV Data Formats

The YUV formatted channels expect video data that is in YUV color space. The YUV data can be type is for YUV data and it can support both interleaved data where Luma and Chroma are in the same data buffer or it can support co-planar data where the Luma and Chroma are in separate data buffers. The YUV channel also can be given a position to give a different start position for the client instead of the default upper left hand corner of the frame. The storage format for YUV data depends on the data type field. The data type must be set to a data type that the channel can support. All the clients that data are provided too will either accept Luma Only, Chroma Only or Luma and Chroma in a parallel data bus.

9.4.8.9.1.1 Y 4:4:4 (Data Type 0)

The Y 4:4:4 data type is used for a co-planar 4:4:4 data. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container. This data block should have the width and height set to the desired frame size expected by the receiving client.

Figure 9-97. Y 4:4:4 (Data Type 0)

9.4.8.9.1.2 Y 4:2:2 (Data Type 1)

The Y 4:2:2 data type is used for a co-planar 4:2:2 data. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container. This data block should have the width and the height of the desired frame sent by the VPDMA to the receive client.

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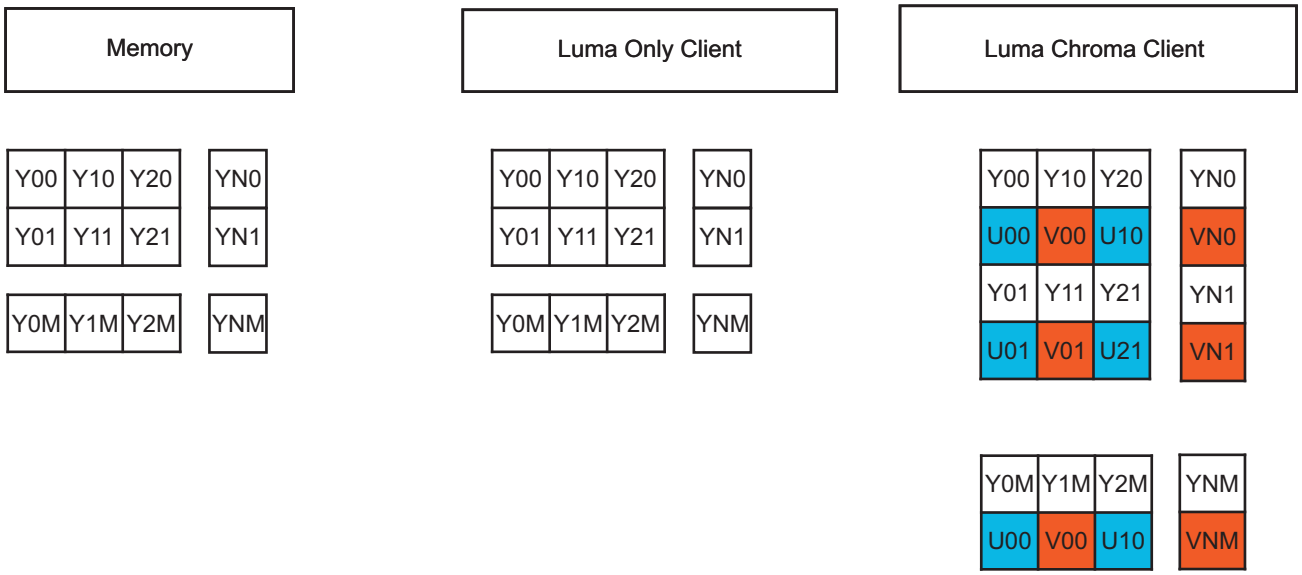
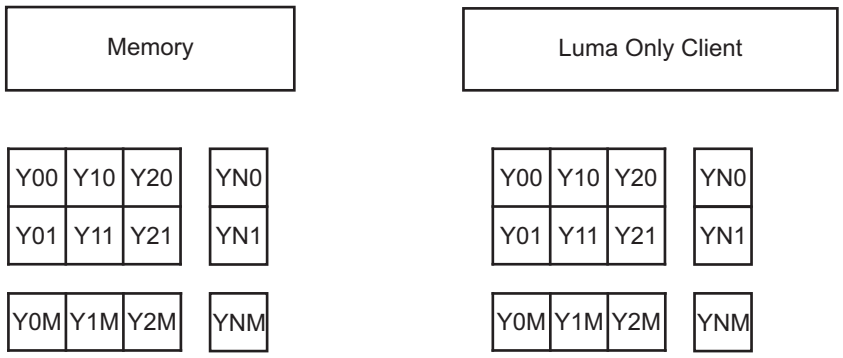
Figure 9-98. Y 4:2:2 (Data Type 1)



9.4.8.9.1.3 Y 4:2:0 (Data Type 2)

The Y 4:2:0 data type is used for a co-planar 4:2:0 data type. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container. This data block should have the width and the height of the expected frame for the client.

Figure 9-99. Y 4:2:0 (Data Type 2)



9.4.8.9.1.4 C 4:4:4 (Data Type 4)

The C 4:4:4 data type is used for a co-planar 4:4:4 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container. This data block should have the width and height of the expected client frame.

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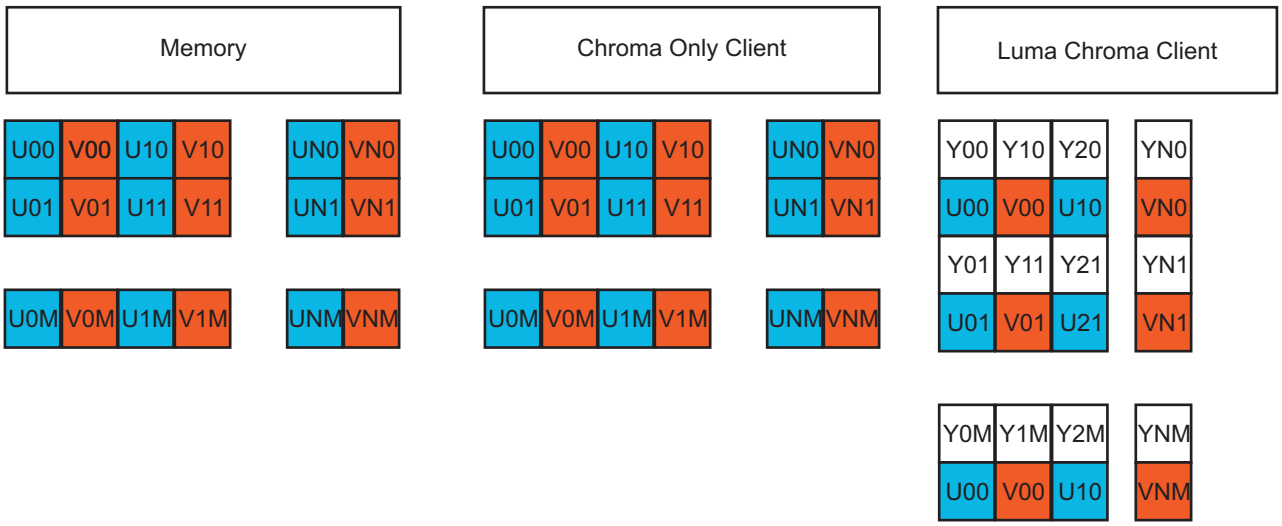
Figure 9-100. C 4:4:4 (Data Type 4)

9.4.8.9.1.5 C 4:2:2 (Data Type 5)

The C 4:2:2 data type is used for co-planar 4:2:2 data.It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container. This data block should have the width and the height of the expected client frame.

Figure 9-101. C 4:2:2 (Data Type 5)



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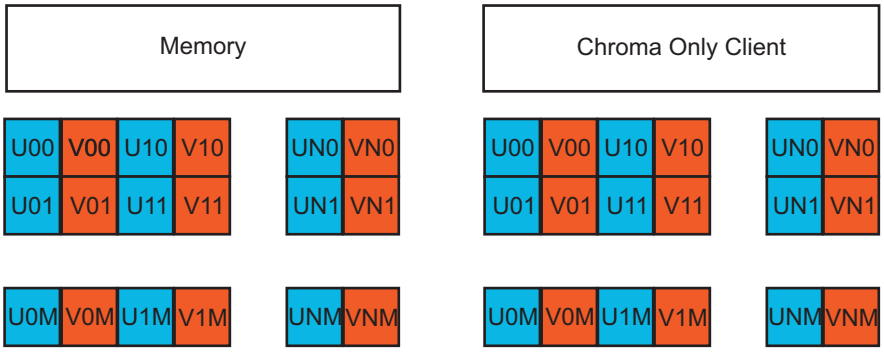
9.4.8.9.1.6 C 4:2:0 (Data Type 6)

The C 4:2:0 data type is used for a co-planar 4:2:0 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in a 16 bit container. This data block should have the width and half the height of the expected clients frame.

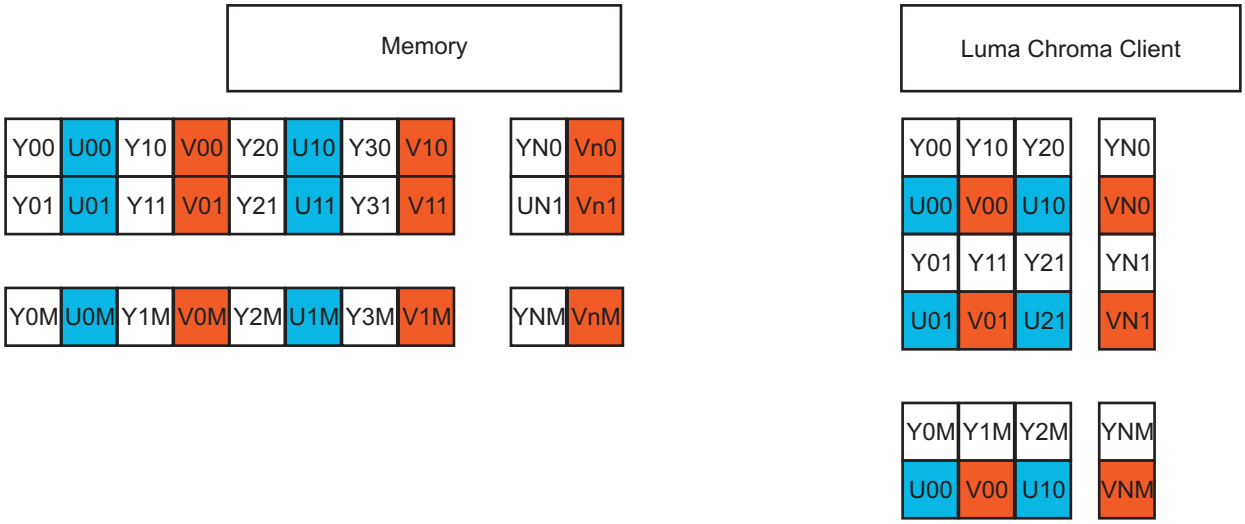
Figure 9-102. C 4:2:0 (Data Type 6)



9.4.8.9.1.7 YC 4:2:2 (Data Type 7)

The YC 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Y0 in the lowest byte followed by Cb followed by Y1 finally Cr in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container. The data block width and height should be set the same as the expected client.

Figure 9-103. YC 4:2:2 (Data Type 7)



9.4.8.9.1.8 YC 4:4:4 (Data Type 8)

The YC 4:4:4 data type is used for interleaved 4:4:4 data. It is expected to be packed with Y0 in the lowest byte followed by Cb followed by Cr. The transfer counts each YCbCr triplet in a 24 bit word as a pixel. A 2D transfer of the data is NOT supported in the VPDMA. The data block width and height should be set to the number of pixels and lines that are expected by the client.

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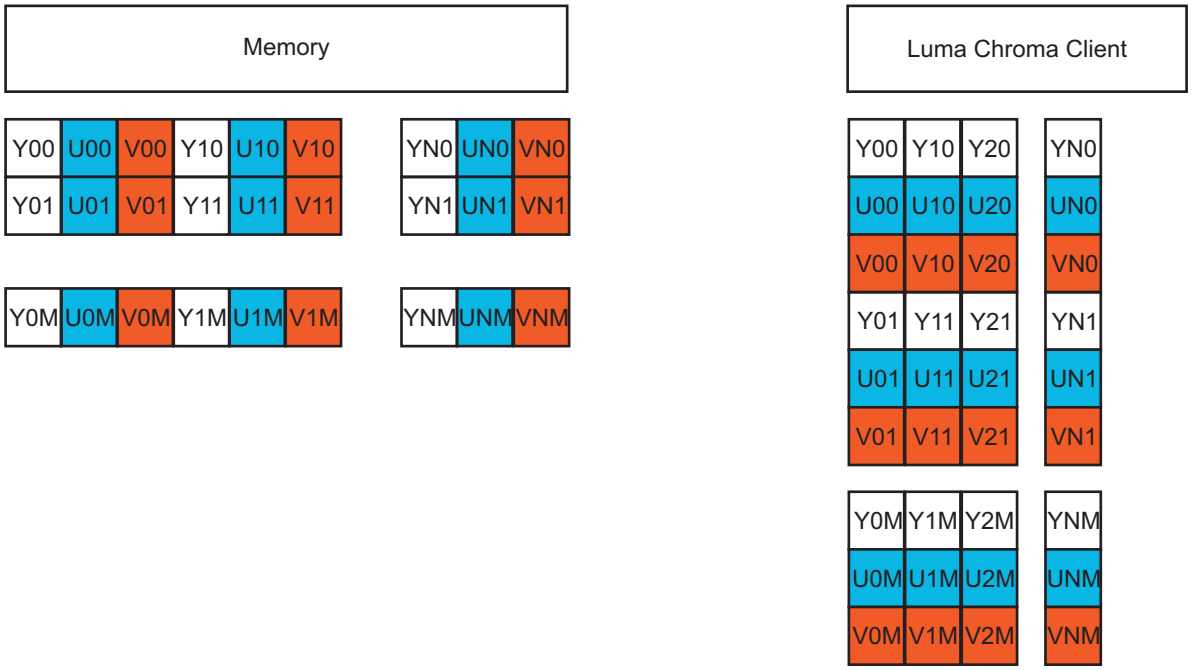
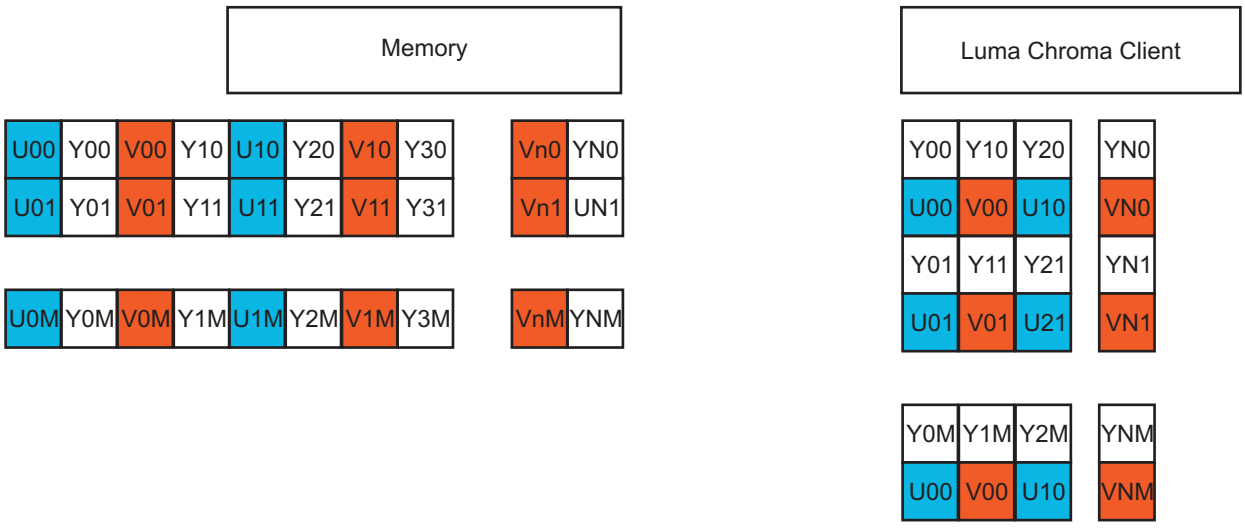
Figure 9-104. YC 4:4:4 (Data Type 8)



9.4.8.9.1.9 CY 4:2:2 (Data Type 23)

The CY 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Cb in the lowest byte followed by Y0 followed by Cr finally Y1 in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container. The data block width and height should be set the same as the expected client.

Figure 9-105. CY 4:2:2 (Data Type 23h)



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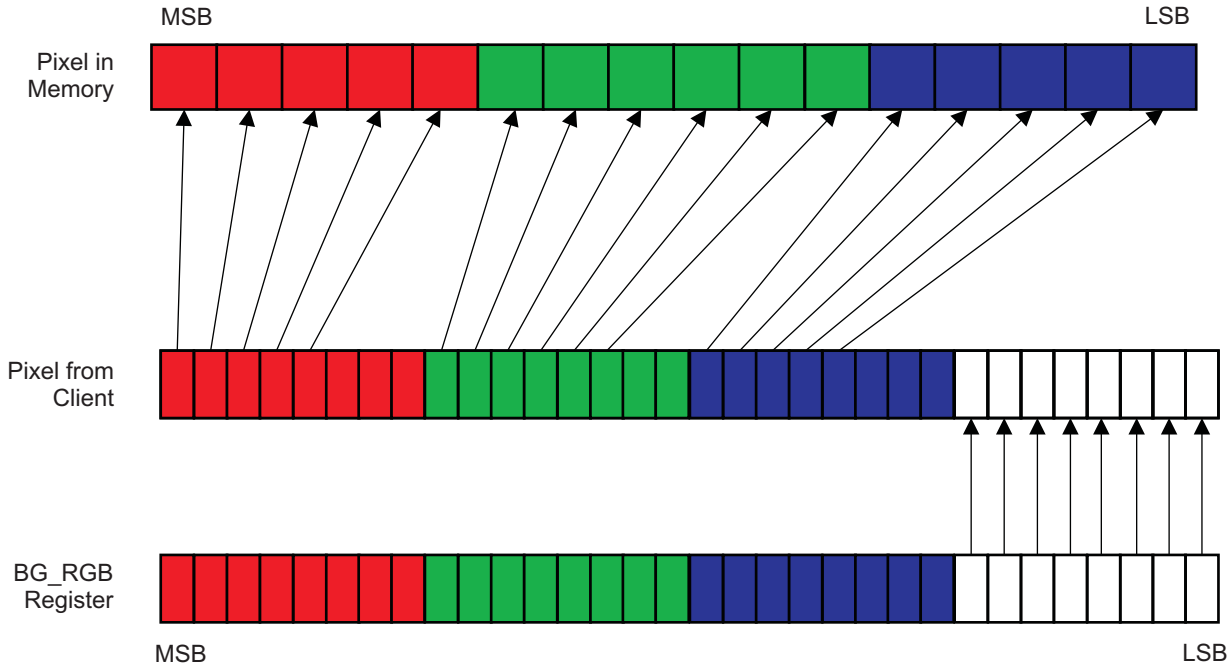
9.4.8.9.2 RGB Data Formats

The RGB channel type is used to provide data for a client that expects to transmit RGB data. In all modes the client is always RGBA 8888 data. The lower bits, if not provided by the data stream, are a replication of the lower bit of the data. For outbound data the input is assumed to be RGB 888 and the Alpha value is taken from the Background Color register to make a full ARGB 8888. The lower bits are dropped from this data, if a data type specifies less then the full 8 bits per color. The client has individual data buses for each component so they have no order dependency in the data bus.

9.4.8.9.2.1 RGB16-565 (Data Type 0)

In RGB16-565 mode, each pixel is a single RGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lower 5 bits for blue data, the middle 6 bits for green data and the upper 5 bits for red data.

Figure 9-106. RGB16-565 (Data Type 0)



9.4.8.9.2.2 ARGB-1555 (Data Type 1)

In ARGB-1555 mode, each pixel is a single ARGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lower 5 bits for blue data, the next 5 bits for green data the next 5 bits for red data and the upper most bit for the blend value to use 0 or 0xFF.

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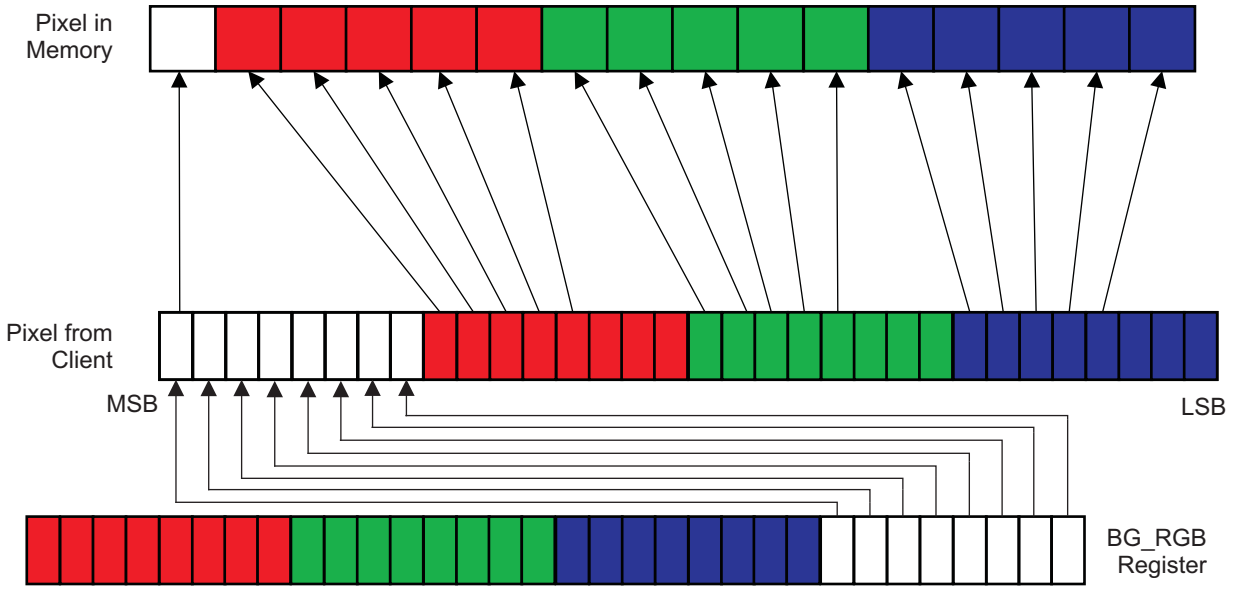
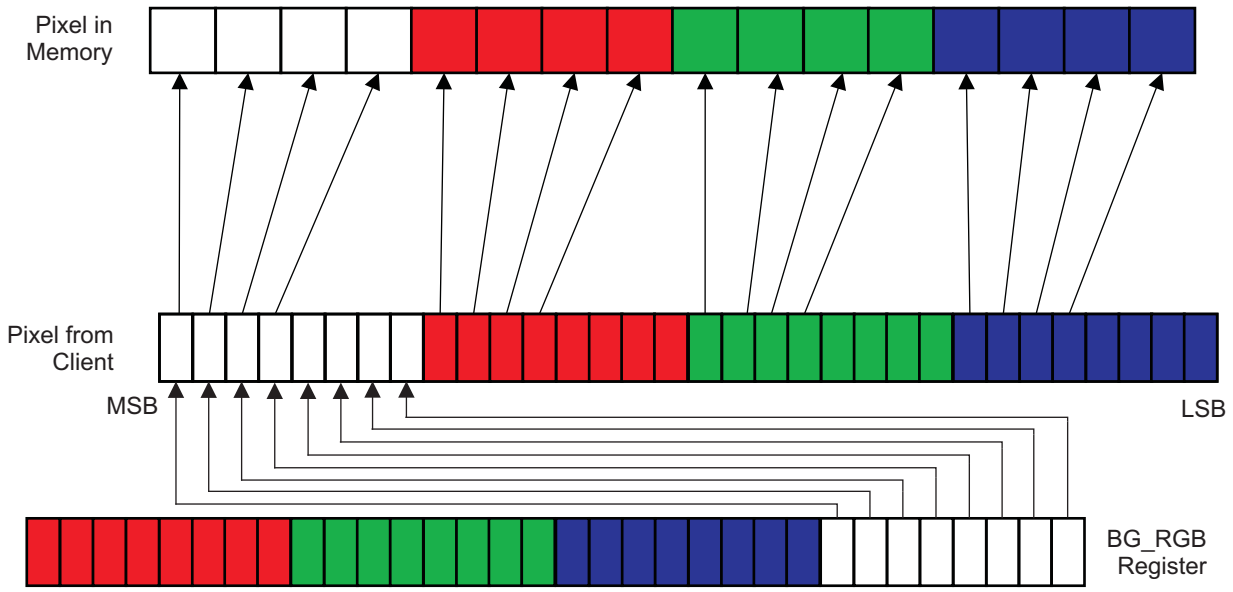
Figure 9-107. ARGB-1555 (Data Type 1)



9.4.8.9.2.3 ARGB-4444 (Data Type 2)

In ARGB16-4444 mode, each pixel is a single RGBA pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest 4 bits for blue data, the next 4 bits for green data the next 4 bits for red data and the upper most 4 bits for the blend value.

Figure 9-108. ARGB-4444 (Data Type 2)



9.4.8.9.2.4 RGBA-5551 (Data Type 3)

In RGBA-5551 mode, each pixel is a single ARGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest most bit for the blend value to use 0 or 0xff the next 5 bits for blue data, the next 5 bits for green data the next 5 bits for red data.

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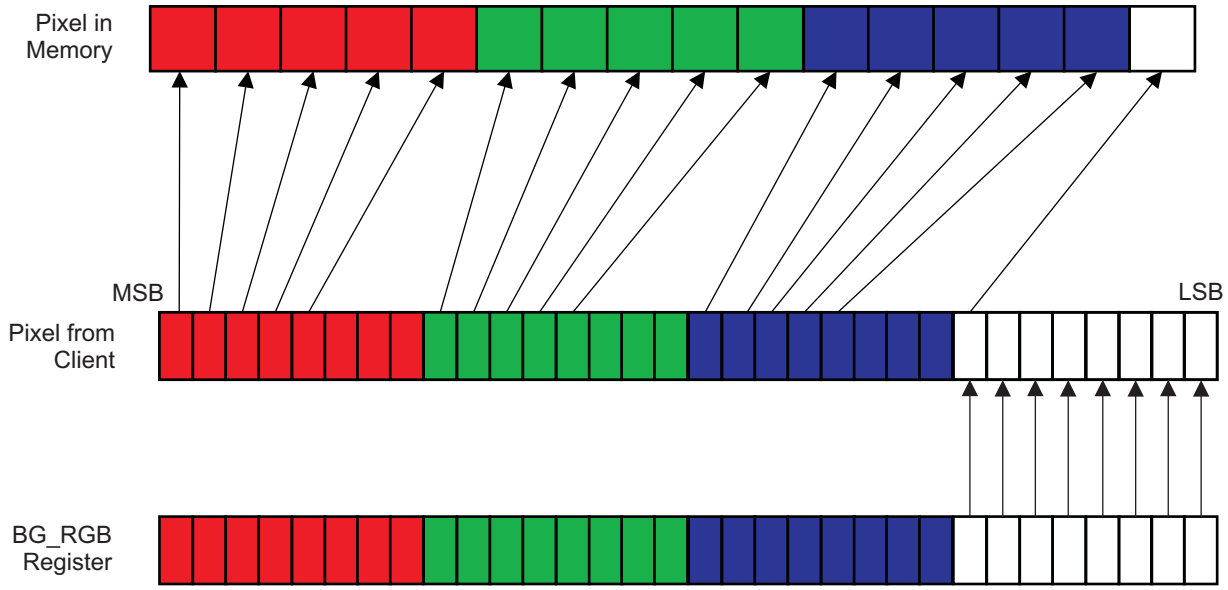
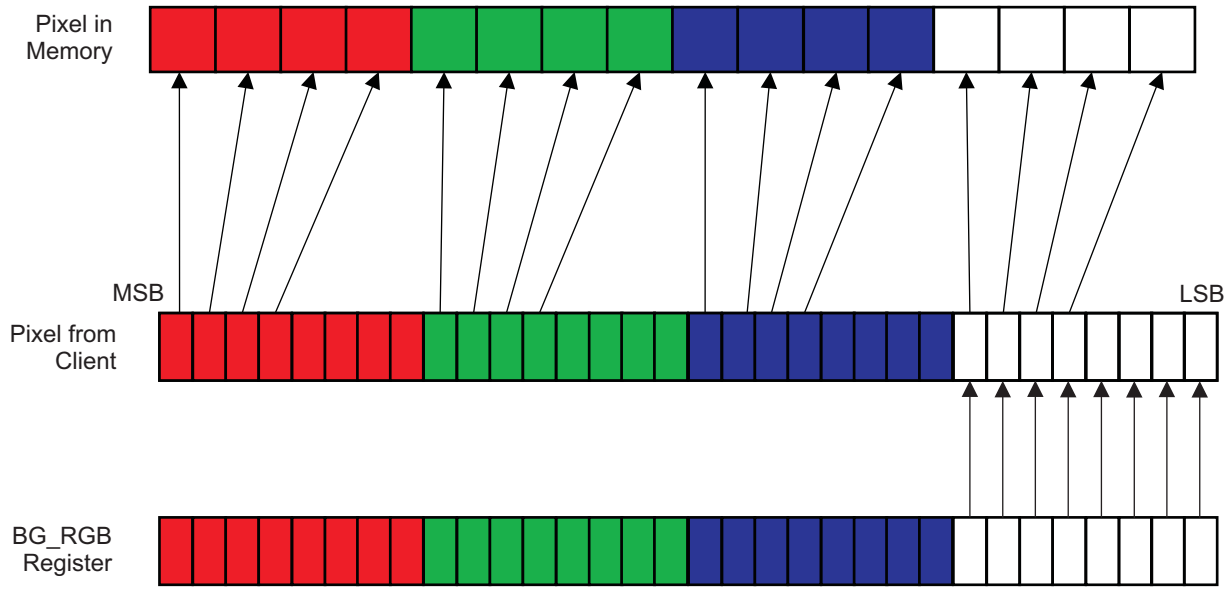
Figure 9-109. RGBA-5551 (Data Type 3)



9.4.8.9.2.5 RGBA-4444 (Data Type 4)

In RGBA-4444 mode, each pixel is a single RGBA pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest 4 bits for the blend value, the next 4 bits for blue data, the next 4 bits for green data and the upper most 4 bits for red data.

Figure 9-110. RGBA-4444 (Data Type 4)



9.4.8.9.2.6 ARGB24-6666 (Data Type 5)

In ARGB24-6666 mode, each pixel is a single ARGB pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 6 bits for the blend value, the next 6 bits for blue data, the next 6 bits for green data and the upper most 6 bits for red data.

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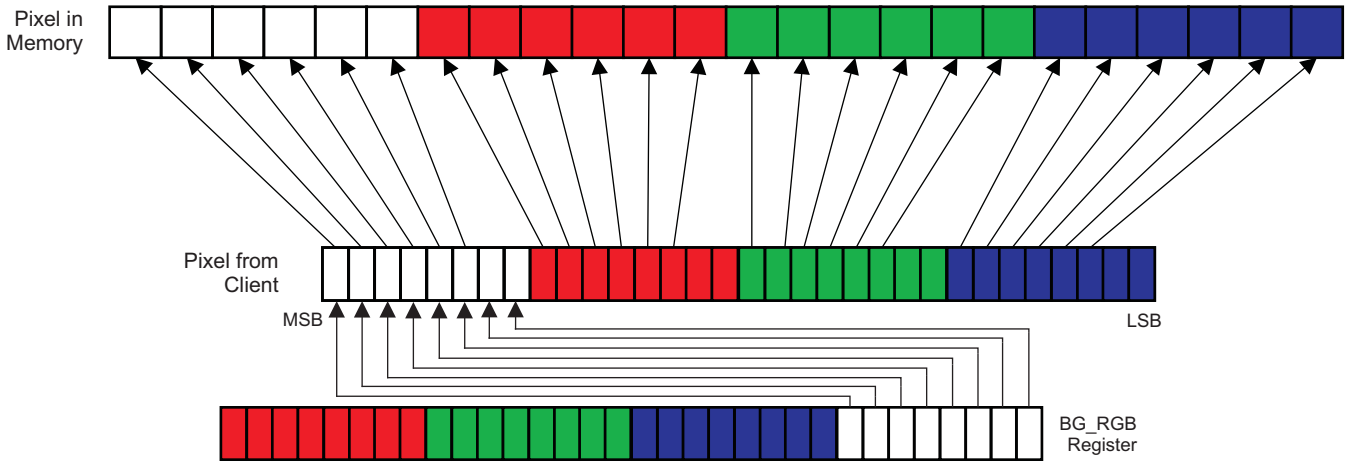
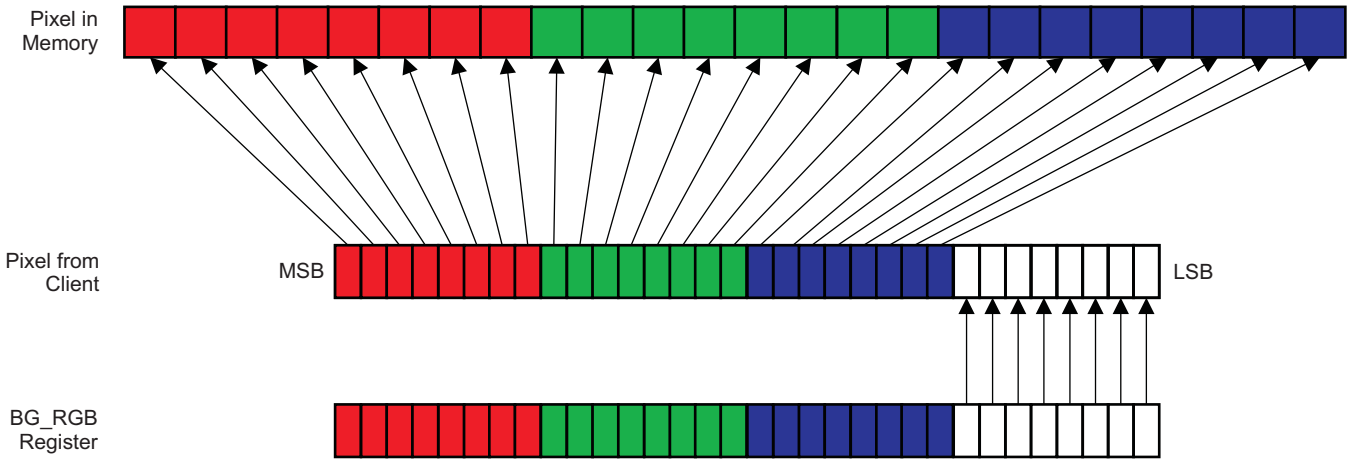
Figure 9-111. ARGB24-6666 (Data Type 5)



9.4.8.9.2.7 RGB24-888 (Data Type 6)

In RGB24-888 mode, each pixel is a single RGB pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 8 bits for blue data, the next 8 bits for green data and the upper most 8 bits for red data it uses the BG_RGB Blend value for the Blend value.

Figure 9-112. RGB24-888 (Data Type 6)



9.4.8.9.2.8 ARGB32-8888 (Data Type 7)

In ARGB32-8888 mode, each pixel is a single ARGB pixel with 32 bits of data for each pixel. The 32 bitsof data uses the lowest 8 bits for blue data, the next 8 bits for green data and the next 8 bits for red data it uses the upper most bits for the blend value.

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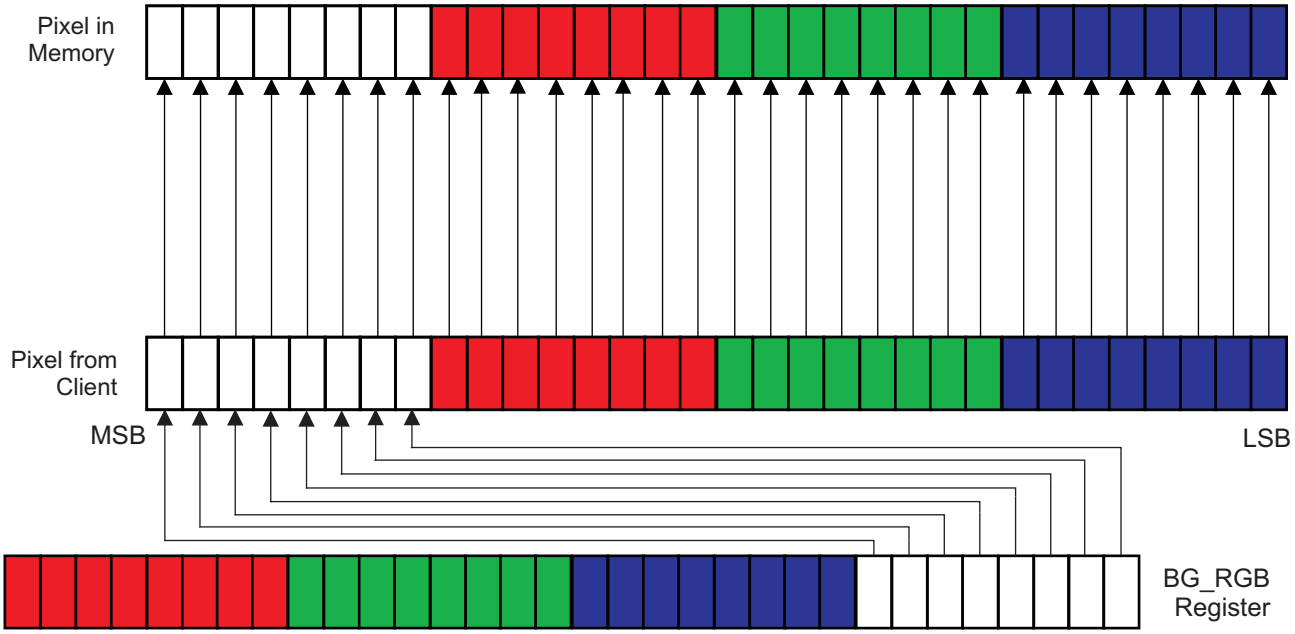
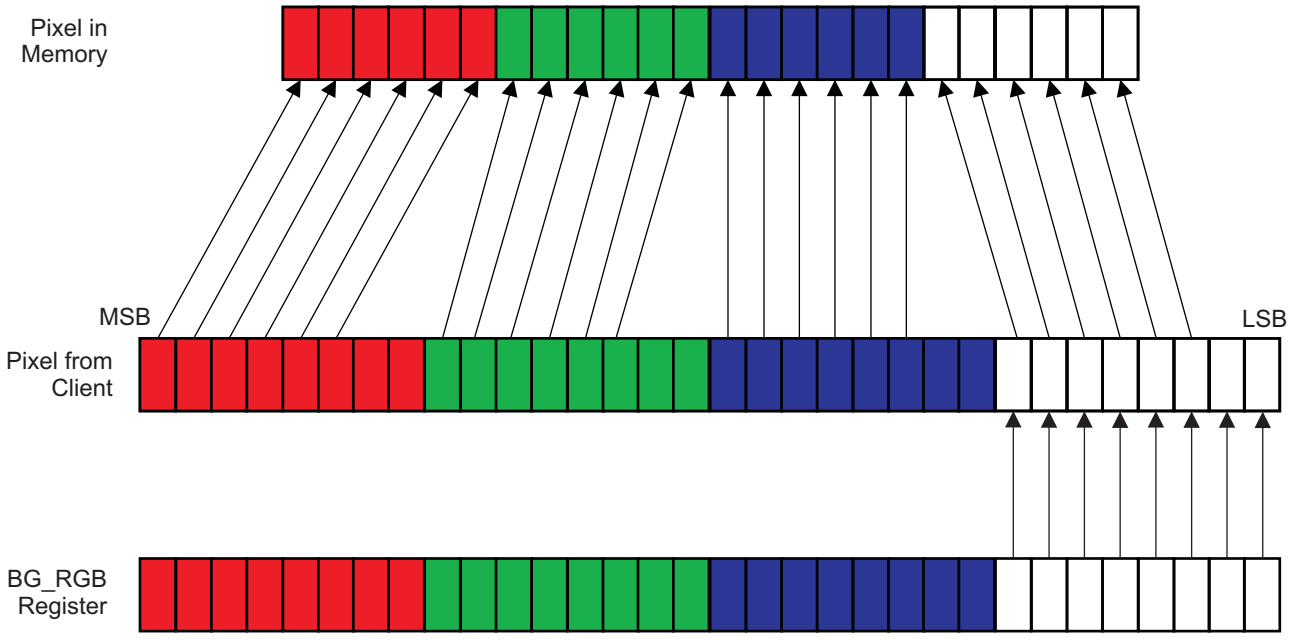
Figure 9-113. ARGB32-8888 (Data Type 7)



9.4.8.9.2.9 RGBA24-6666 (Data Type 8)

In RGBA24-6666 mode, each pixel is a single RGBA pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 6 bits for the blend value, the next 6 bits for blue data, the next 6 bits for green data and the upper 6 bits for red data.

Figure 9-114. RGBA24-6666 (Data Type 8)



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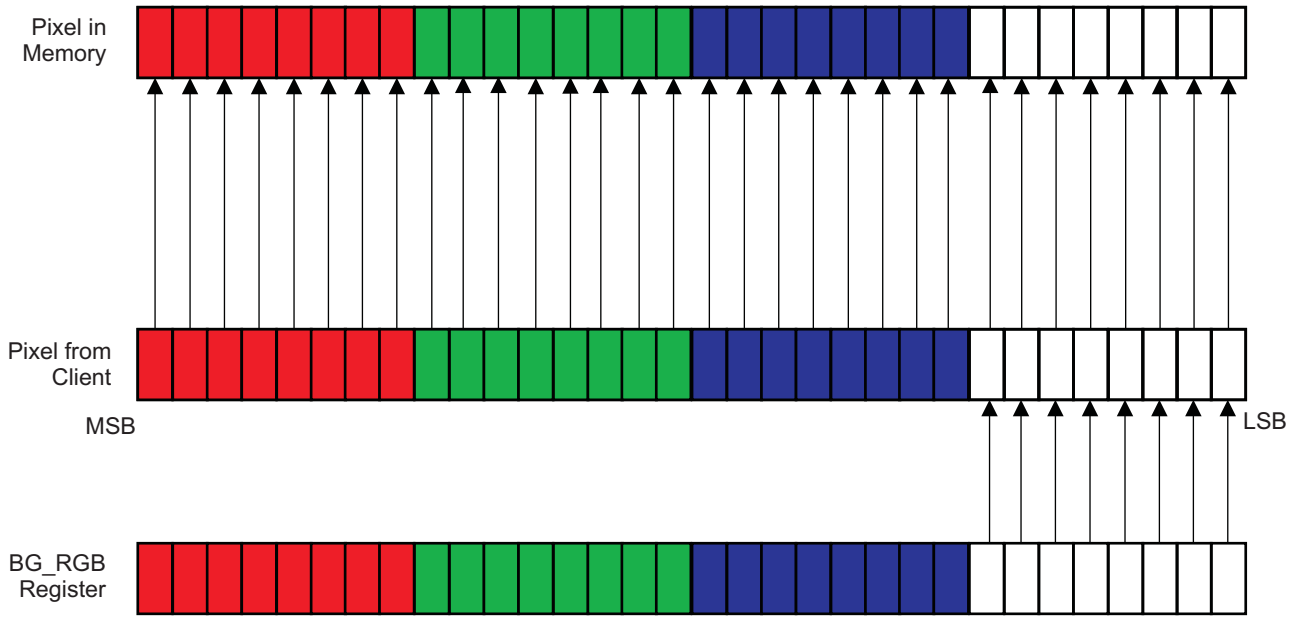
9.4.8.9.2.10 RGBA32-8888 (Data Type 9)

In RGBA32-8888 mode, each pixel is a single ARGB pixel with 32 bits of data for each pixel. The 32 bits of data uses the lowest 8 bits for the blend value the next 8 bits for blue data, the next 8 bits for green data and the upper most 8 bits for red data.

Figure 9-115. RGBA32-8888 (Data Type 9)



9.4.8.9.3 Miscellaneous Data Type

The Miscellaneous channel type is for any data type that is not a normal video type. The Miscellaneous channel type makes no assumptions on data type and just passes the data to the client and supports a single buffer for the client. The size of the miscellaneous data type is always determined by the Data Type field of the descriptor which specifies the number of bits in the descriptor.

A memory structure used to describe a desired memory transaction to or from a client. The descriptor at a minimum gives an address location for the memory portion of the transfer, the channel to use for this transaction and the size of the transaction. The data descriptor can also contain attributes to be passed down to the client or be linked to another data descriptor to form a larger frame from many smaller frames.

9.5 VIP Register Manual

9.5.1 VIP Instance Summary

Table 9-70. VIP Instance Summary

Module Name	Module Base Address	Size
VIP1_top_level	0x4897 0000	276 Bytes
VIP1_Slice0_parser	0x4897 5500	216 Bytes
VIP1_Slice0_csc	0x4897 5700	24 Bytes
VIP1_Slice0_sc	0x4897 5800	128 Bytes
VIP1_Slice1_parser	0x4897 5A00	216 Bytes
VIP1_Slice1_csc	0x4897 5C00	24 Bytes
VIP1_Slice1_sc	0x4897 5D00	128 Bytes
VIP1_VPDMA	0x4897 D000	1016 Bytes

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Table 9-70. VIP Instance Summary (continued)

Module Name	Module Base Address	Size
VIP2_top_level	0x4899 0000	276 Bytes
VIP2_Slice0_parser	0x4899 5500	216 Bytes
VIP2_Slice0_csc	0x4899 5700	24 Bytes
VIP2_Slice0_sc	0x4899 5800	128 Bytes
VIP2_Slice1_parser	0x4899 5A00	216 Bytes
VIP2_Slice1_csc	0x4899 5C00	24 Bytes
VIP2_Slice1_sc	0x4899 5D00	128 Bytes
VIP2_VPDMA	0x4899 D000	1016 Bytes
VIP3_top_level	0x489B 0000	276 Bytes
VIP3_Slice0_parser	0x489B 5500	216 Bytes
VIP3_Slice0_csc	0x489B 5700	24 Bytes
VIP3_Slice0_sc	0x489B 5800	128 Bytes
VIP3_Slice1_parser	0x489B 5A00	216 Bytes
VIP3_Slice1_csc	0x489B 5C00	24 Bytes
VIP3_Slice1_sc	0x489B 5D00	128 Bytes
VIP3_VPDMA	0x489B D000	1016 Bytes

9.5.2 VIP Top Level Registers

9.5.2.1 VIP Top Level Register Summary

Table 9-71. VIP Top Level Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_top_level Base Address	VIP2_top_level Base Address	VIP3_top_level Base Address
VIP_CLKC_PID	RW	32	0x0000 0000	0x4897 0000	0x4899 0000	0x489B 0000
VIP_SYSCONFIG	RW	32	0x0000 0010	0x4897 0010	0x4899 0010	0x489B 0010
VIP_INTC_INTR0_STATUS_RAW0	RW	32	0x0000 0020	0x4897 0020	0x4899 0020	0x489B 0020
VIP_INTC_INTR0_STATUS_RAW1	RW	32	0x0000 0024	0x4897 0024	0x4899 0024	0x489B 0024
VIP_INTC_INTR0_STATUS_ENA0	RW	32	0x0000 0028	0x4897 0028	0x4899 0028	0x489B 0028
VIP_INTC_INTR0_STATUS_ENA1	RW	32	0x0000 002C	0x4897 002C	0x4899 002C	0x489B 002C
VIP_INTC_INTR0_ENA_SET0	RW	32	0x0000 0030	0x4897 0030	0x4899 0030	0x489B 0030
VIP_INTC_INTR0_ENA_SET1	RW	32	0x0000 0034	0x4897 0034	0x4899 0034	0x489B 0034
VIP_INTC_INTR0_ENA_CLR0	RW	32	0x0000 0038	0x4897 0038	0x4899 0038	0x489B 0038
VIP_INTC_INTR0_ENA_CLR1	RW	32	0x0000 003C	0x4897 003C	0x4899 003C	0x489B 003C
VIP_INTC_INTR1_STATUS_RAW0	RW	32	0x0000 0040	0x4897 0040	0x4899 0040	0x489B 0040
VIP_INTC_INTR1_STATUS_RAW1	RW	32	0x0000 0044	0x4897 0044	0x4899 0044	0x489B 0044
VIP_INTC_INTR1_STATUS_ENA0	RW	32	0x0000 0048	0x4897 0048	0x4899 0048	0x489B 0048
VIP_INTC_INTR1_STATUS_ENA1	RW	32	0x0000 004C	0x4897 004C	0x4899 004C	0x489B 004C
VIP_INTC_INTR1_ENA_SET0	RW	32	0x0000 0050	0x4897 0050	0x4899 0050	0x489B 0050
VIP_INTC_INTR1_ENA_SET1	RW	32	0x0000 0054	0x4897 0054	0x4899 0054	0x489B 0054
VIP_INTC_INTR1_ENA_CLR0	RW	32	0x0000 0058	0x4897 0058	0x4899 0058	0x489B 0058
VIP_INTC_INTR1_ENA_CLR1	RW	32	0x0000 005C	0x4897 005C	0x4899 005C	0x489B 005C
VIP_INTC_EOI	RW	32	0x0000 00A0	0x4897 00A0	0x4899 00A0	0x489B 00A0
VIP_CLKC_CLKEN	RW	32	0x0000 0100	0x4897 0100	0x4899 0100	0x489B 0100
VIP_CLKC_RST	RW	32	0x0000 0104	0x4897 0104	0x4899 0104	0x489B 0104
VIP_CLKC_DPS	RW	32	0x0000 0108	0x4897 0108	0x4899 0108	0x489B 0108
VIP_CLKC_VIP0DPS	RW	32	0x0000 010C	0x4897 010C	0x4899 010C	0x489B 010C
VIP_CLKC_VIP1DPS	RW	32	0x0000 0110	0x4897 0110	0x4899 0110	0x489B 0110

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9.5.2.2 VIP Top Level Register Description

Table 9-72. VIP_CLKC_PID

Address Offset	0x0000 0000		
Physical Address	0x4897 0000 0x4899 0000 0x489B 0000	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	This register follows the format described in PDR3.5		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCHEME		RESERVED		FUNC												RTL					MAJOR			CUSTOM				MINOR			

Bits	Field Name	Description	Type	Reset
31:30	SCHEME	The scheme of the register used. This indicates the PDR3.5 Method	R	0x0
29:28	RESERVED		R	0x0
27:16	FUNC	The function of the module being used	R	0x0
15:11	RTL	RTL Release Version The PDR release number of this IP	R	0x0
10:8	MAJOR	ajor Release Number	R	0x0
7:6	CUSTOM	Custom IP	R	0x0
5:0	MINOR	inor Release Number	R	0x0

Table 9-73. Register Call Summary for Register VIP_CLKC_PID

VIP Register Manual
- VIP Top Level Register Summary: [0]

Table 9-74. VIP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4897 0010 0x4899 0010 0x489B 0010	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	VIP_SYSCONFIG		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only 0x2: Same behavior as bit-field value of 0x1. 0x3: Reserved	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state 0x0 : Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only 0x1 : No-idle mode: local target never enters idle state. Backup mode, for debug only 0x2 : Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events 0x3 : Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate IP module 'swakeup' output(s) is (are) implemented	RW	0x2
1:0	RESERVED		R	0x0

Table 9-75. Register Call Summary for Register VIP_SYSCONFIG

VIP Functional Description
- VIP Idle Mode: [0]
- VIP StandBy Mode: [1]

VIP Register Manual
- VIP Top Level Register Summary: [2]
- VIP Top Level Register Description: [5]

Table 9-76. VIP_INTC_INTR0_STATUS_RAW0

Address Offset	0x0000 0020		
Physical Address	0x4897 0020 0x4899 0020 0x489B 0020	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Status Raw/Set Register 0. This register contains the raw interrupt status as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	RESERVED			VPDMA_INT0_DESCRIPTOR_RAW	VPDMA_INT0_LIST7_NOTIFY_RAW	VPDMA_INT0_LIST7_COMPLETE_RAW	VPDMA_INT0_LIST6_NOTIFY_RAW	VPDMA_INT0_LIST6_COMPLETE_RAW	VPDMA_INT0_LIST5_NOTIFY_RAW	VPDMA_INT0_LIST5_COMPLETE_RAW	VPDMA_INT0_LIST4_NOTIFY_RAW	VPDMA_INT0_LIST4_COMPLETE_RAW	VPDMA_INT0_LIST3_NOTIFY_RAW	VPDMA_INT0_LIST3_COMPLETE_RAW	VPDMA_INT0_LIST2_NOTIFY_RAW	VPDMA_INT0_LIST2_COMPLETE_RAW	VPDMA_INT0_LIST1_NOTIFY_RAW	VPDMA_INT0_LIST1_COMPLETE_RAW	VPDMA_INT0_LIST0_NOTIFY_RAW	VPDMA_INT0_LIST0_COMPLETE_RAW

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_RAW	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_RAW	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT0_DESCRIPTOR_RAW	VPDMA INT0 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
15	VPDMA_INT0_LIST7_NOTIFY_RAW	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
14	VPDMA_INT0_LIST7_COMPLETE_RAW	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
13	VPDMA_INT0_LIST6_NOTIFY_RAW	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
12	VPDMA_INT0_LIST6_COMPLETE_RAW	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
11	VPDMA_INT0_LIST5_NOTIFY_RAW	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
10	VPDMA_INT0_LIST5_COMPLETE_RAW	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
9	VPDMA_INT0_LIST4_NOTIFY_RAW	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
8	VPDMA_INT0_LIST4_COMPLETE_RAW	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
7	VPDMA_INT0_LIST3_NOTIFY_RAW	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_LIST3_COMPLETE_RAW	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_LIST2_NOTIFY_RAW	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	VPDMA_INT0_LIST2_COMPLETE_RAW	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_LIST1_NOTIFY_RAW	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_LIST1_COMPLETE_RAW	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_LIST0_NOTIFY_RAW	VPDMA INT0 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_LIST0_COMPLETE_RAW	VPDMA INT0 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-77. Register Call Summary for Register VIP_INTC_INTR0_STATUS_RAW0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-78. VIP_INTC_INTR0_STATUS_RAW1

Address Offset	0x0000 0024		
Physical Address	0x4897 0024 0x4899 0024 0x489B 0024	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Status Raw/Set Register 1. This register contains the raw interrupt status as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW	VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	RESERVED														VPDMA_INT0_CLIENT_RAW	RESERVED	VPDMA_INT0_CHANNEL_GROUP5_RAW	VPDMA_INT0_CHANNEL_GROUP4_RAW	VPDMA_INT0_CHANNEL_GROUP3_RAW	VPDMA_INT0_CHANNEL_GROUP2_RAW	VPDMA_INT0_CHANNEL_GROUP1_RAW	VPDMA_INT0_CHANNEL_GROUP0_RAW

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT0_CLIENT_RAW	VPDMA INT0 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	RESERVED		R	0x0
5	VPDMA_INT0_CHANNEL_GROUP5_RAW	VPDMA INT0 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_CHANNEL_GROUP4_RAW	VPDMA INT0 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_CHANNEL_GROUP3_RAW	VPDMA INT0 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_CHANNEL_GROUP2_RAW	VPDMA INT0 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_CHANNEL_GROUP1_RAW	VPDMA INT0 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_CHANNEL_GROUP0_RAW	VPDMA INT0 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-79. Register Call Summary for Register VIP_INTC_INTR0_STATUS_RAW1

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-80. VIP_INTC_INTR0_STATUS_ENA0

Address Offset	0x0000 0028		
Physical Address	0x4897 0028 0x4899 0028 0x489B 0028	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Status Enabled/Clear Register 0. This register contains the enabled interrupt status as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	RESERVED			VPDMA_INT0_DESCRIPTOR_ENA	VPDMA_INT0_LIST7_NOTIFY_ENA	VPDMA_INT0_LIST7_COMPLETE_ENA	VPDMA_INT0_LIST6_NOTIFY_ENA	VPDMA_INT0_LIST6_COMPLETE_ENA	VPDMA_INT0_LIST5_NOTIFY_ENA	VPDMA_INT0_LIST5_COMPLETE_ENA	VPDMA_INT0_LIST4_NOTIFY_ENA	VPDMA_INT0_LIST4_COMPLETE_ENA	VPDMA_INT0_LIST3_NOTIFY_ENA	VPDMA_INT0_LIST3_COMPLETE_ENA	VPDMA_INT0_LIST2_NOTIFY_ENA	VPDMA_INT0_LIST2_COMPLETE_ENA	VPDMA_INT0_LIST1_NOTIFY_ENA	VPDMA_INT0_LIST1_COMPLETE_ENA	VPDMA_INT0_LIST0_NOTIFY_ENA	VPDMA_INT0_LIST0_COMPLETE_ENA

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT0_DESCRIPTOR_ENA	VPDMA INT0 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
15	VPDMA_INT0_LIST7_NOTIFY_ENA	VPDMA INT0 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT0_LIST7_COMPLETE_ENA	VPDMA INT0 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT0_LIST6_NOTIFY_ENA	VPDMA INT0 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT0_LIST6_COMPLETE_ENA	VPDMA INT0 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT0_LIST5_NOTIFY_ENA	VPDMA INT0 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT0_LIST5_COMPLETE_ENA	VPDMA INT0 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT0_LIST4_NOTIFY_ENA	VPDMA INT0 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
8	VPDMA_INT0_LIST4_COMPLETE_ENA	VPDMA INT0 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
7	VPDMA_INT0_LIST3_NOTIFY_ENA	VPDMA INT0 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_LIST3_COMPLETE_ENA	VPDMA INT0 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_LIST2_NOTIFY_ENA	VPDMA INT0 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	VPDMA_INT0_LIST2_COMPLETE_ENA	VPDMA INT0 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_LIST1_NOTIFY_ENA	VPDMA INT0 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_LIST1_COMPLETE_ENA	VPDMA INT0 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_LIST0_NOTIFY_ENA	VPDMA INT0 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_LIST0_COMPLETE_ENA	VPDMA INT0 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-81. Register Call Summary for Register VIP_INTC_INTR0_STATUS_ENA0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-82. VIP_INTC_INTR0_STATUS_ENA1

Address Offset	0x0000 002C		
Physical Address	0x4897 002C 0x4899 002C 0x489B 002C	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Status Enabled/Clear Register 1. This register contains the enabled interrupt status as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA	VIP2_CHR_DS_1_UV_ERR_INT_ENA	VIP1_CHR_DS_2_UV_ERR_INT_ENA	VIP1_CHR_DS_1_UV_ERR_INT_ENA	RESERVED														VPDMA_INT0_CLIENT_ENA	RESERVED	VPDMA_INT0_CHANNEL_GROUP5_ENA	VPDMA_INT0_CHANNEL_GROUP4_ENA	VPDMA_INT0_CHANNEL_GROUP3_ENA	VPDMA_INT0_CHANNEL_GROUP2_ENA	VPDMA_INT0_CHANNEL_GROUP1_ENA	VPDMA_INT0_CHANNEL_GROUP0_ENA

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT0_CLIENT_ENA	VPDMA INT0 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	RESERVED		R	0x0
5	VPDMA_INT0_CHANNEL_GROUP5_ENA	VPDMA INT0 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_CHANNEL_GROUP4_ENA	VPDMA INT0 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_CHANNEL_GROUP3_ENA	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_CHANNEL_GROUP2_ENA	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_CHANNEL_GROUP1_ENA	VPDMA INT0 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_CHANNEL_GROUP0_ENA	VPDMA INT0 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-83. Register Call Summary for Register VIP_INTC_INTR0_STATUS_ENA1

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-84. VIP_INTC_INTR0_ENA_SET0

Address Offset	0x0000 0030		
Physical Address	0x4897 0030 0x4899 0030 0x489B 0030	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Enable/Set Register 0. This register contains the interrupt enable status/set as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	RESERVED			VPDMA_INT0_DESCRIPTOR_ENA_SET	VPDMA_INT0_LIST7_NOTIFY_ENA_SET	VPDMA_INT0_LIST7_COMPLETE_ENA_SET	VPDMA_INT0_LIST6_NOTIFY_ENA_SET	VPDMA_INT0_LIST6_COMPLETE_ENA_SET	VPDMA_INT0_LIST5_NOTIFY_ENA_SET	VPDMA_INT0_LIST5_COMPLETE_ENA_SET	VPDMA_INT0_LIST4_NOTIFY_ENA_SET	VPDMA_INT0_LIST4_COMPLETE_ENA_SET	VPDMA_INT0_LIST3_NOTIFY_ENA_SET	VPDMA_INT0_LIST3_COMPLETE_ENA_SET	VPDMA_INT0_LIST2_NOTIFY_ENA_SET	VPDMA_INT0_LIST2_COMPLETE_ENA_SET	VPDMA_INT0_LIST1_NOTIFY_ENA_SET	VPDMA_INT0_LIST1_COMPLETE_ENA_SET	VPDMA_INT0_LIST0_NOTIFY_ENA_SET	VPDMA_INT0_LIST0_COMPLETE_ENA_SET

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA_SET	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA_SET	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT0_DESCRIPTOR_ENA_SET	VPDMA INT0 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
15	VPDMA_INT0_LIST7_NOTIFY_ENA_SET	VPDMA INT0 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT0_LIST7_COMPLETE_ENA_SET	VPDMA INT0 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT0_LIST6_NOTIFY_ENA_SET	VPDMA INT0 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT0_LIST6_COMPLETE_ENA_SET	VPDMA INT0 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT0_LIST5_NOTIFY_ENA_SET	VPDMA INT0 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT0_LIST5_COMPLETE_ENA_SET	VPDMA INT0 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT0_LIST4_NOTIFY_ENA_SET	VPDMA INT0 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
8	VPDMA_INT0_LIST4_COMPLETE_ENA_SET	VPDMA INT0 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
7	VPDMA_INT0_LIST3_NOTIFY_ENA_SET	VPDMA INT0 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_LIST3_COMPLETE_ENA_SET	VPDMA INT0 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_LIST2_NOTIFY_ENA_SET	VPDMA INT0 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_LIST2_COMPLETE_ENA_SET	VPDMA INT0 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_LIST1_NOTIFY_ENA_SET	VPDMA INT0 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	VPDMA_INT0_LIST1_COMPLETE_ENA_SET	VPDMA INT0 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_LIST0_NOTIFY_ENA_SET	VPDMA INT0 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_LIST0_COMPLETE_ENA_SET	VPDMA INT0 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-85. Register Call Summary for Register VIP_INTC_INTR0_ENA_SET0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-86. VIP_INTC_INTR0_ENA_SET1

Address Offset	0x0000 0034		
Physical Address	0x4897 0034 0x4899 0034 0x489B 0034	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Enable/Set Register 1. This register contains the interrupt enable status/set as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	RESERVED														VPDMA_INT0_CLIENT_ENA_SET	VPDMA_INT0_CHANNEL_GROUP6_ENA_SET	VPDMA_INT0_CHANNEL_GROUP5_ENA_SET	VPDMA_INT0_CHANNEL_GROUP4_ENA_SET	VPDMA_INT0_CHANNEL_GROUP3_ENA_SET	VPDMA_INT0_CHANNEL_GROUP2_ENA_SET	VPDMA_INT0_CHANNEL_GROUP1_ENA_SET	VPDMA_INT0_CHANNEL_GROUP0_ENA_SET

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT0_CLIENT_ENA_SET	VPDMA INT0 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_CHANNEL_GROUP6_ENA_SET	VPDMA INT0 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_CHANNEL_GROUP5_ENA_SET	VPDMA INT0 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_CHANNEL_GROUP4_ENA_SET	VPDMA INT0 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_CHANNEL_GROUP3_ENA_SET	VPDMA INT0 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_CHANNEL_GROUP2_ENA_SET	VPDMA INT0 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_CHANNEL_GROUP1_ENA_SET	VPDMA INT0 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_CHANNEL_GROUP0_ENA_SET	VPDMA INT0 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-87. Register Call Summary for Register VIP_INTC_INTR0_ENA_SET1

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-88. VIP_INTC_INTR0_ENA_CLR0

Address Offset	0x0000 0038		
Physical Address	0x4897 0038 0x4899 0038 0x489B 0038	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Enable/Clear Register 0. This register contains the interrupt enable status/clear as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	RESERVED			VPDMA_INT0_DESCRIPTOR_ENA_CLR	VPDMA_INT0_LIST7_NOTIFY_ENA_CLR	VPDMA_INT0_LIST7_COMPLETE_ENA_CLR	VPDMA_INT0_LIST6_NOTIFY_ENA_CLR	VPDMA_INT0_LIST6_COMPLETE_ENA_CLR	VPDMA_INT0_LIST5_NOTIFY_ENA_CLR	VPDMA_INT0_LIST5_COMPLETE_ENA_CLR	VPDMA_INT0_LIST4_NOTIFY_ENA_CLR	VPDMA_INT0_LIST4_COMPLETE_ENA_CLR	VPDMA_INT0_LIST3_NOTIFY_ENA_CLR	VPDMA_INT0_LIST3_COMPLETE_ENA_CLR	VPDMA_INT0_LIST2_NOTIFY_ENA_CLR	VPDMA_INT0_LIST2_COMPLETE_ENA_CLR	VPDMA_INT0_LIST1_NOTIFY_ENA_CLR	VPDMA_INT0_LIST1_COMPLETE_ENA_CLR	VPDMA_INT0_LIST0_NOTIFY_ENA_CLR	VPDMA_INT0_LIST0_COMPLETE_ENA_CLR

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA_CLR	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA_CLR	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT0_DESCRIPTOR_ENA_CLR	VPDMA INT0 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
15	VPDMA_INT0_LIST7_NOTIFY_ENA_CLR	VPDMA INT0 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT0_LIST7_COMPLETE_ENA_CLR	VPDMA INT0 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT0_LIST6_NOTIFY_ENA_CLR	VPDMA INT0 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT0_LIST6_COMPLETE_ENA_CLR	VPDMA INT0 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT0_LIST5_NOTIFY_ENA_CLR	VPDMA INT0 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT0_LIST5_COMPLETE_ENA_CLR	VPDMA INT0 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT0_LIST4_NOTIFY_ENA_CLR	VPDMA INT0 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
8	VPDMA_INT0_LIST4_COMPLETE_ENA_CLR	VPDMA INT0 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
7	VPDMA_INT0_LIST3_NOTIFY_ENA_CLR	VPDMA INT0 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_LIST3_COMPLETE_ENA_CLR	VPDMA INT0 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_LIST2_NOTIFY_ENA_CLR	VPDMA INT0 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_LIST2_COMPLETE_ENA_CLR	VPDMA INT0 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_LIST1_NOTIFY_ENA_CLR	VPDMA INT0 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_LIST1_COMPLETE_ENA_CLR	VPDMA INT0 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT0_LIST0_NOTIFY_ENA_CLR	VPDMA INT0 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_LIST0_COMPLETE_ENA_CLR	VPDMA INT0 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-89. Register Call Summary for Register VIP_INTC_INTR0_ENA_CLR0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-90. VIP_INTC_INTR0_ENA_CLR1

Address Offset	0x0000 003C		
Physical Address	0x4897 003C 0x4899 003C 0x489B 003C	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC INTR0 Interrupt Enable/Clear Register 1. This register contains the interrupt enable status/clear as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	RESERVED														VPDMA_INT0_CLIENT_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP0_ENA_CLR

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT0_CLIENT_ENA_CLR	VPDMA INT0 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT0_CHANNEL_GROUP6_ENA_CLR	VPDMA INT0 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT0_CHANNEL_GROUP5_ENA_CLR	VPDMA INT0 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT0_CHANNEL_GROUP4_ENA_CLR	VPDMA INT0 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT0_CHANNEL_GROUP3_ENA_CLR	VPDMA INT0 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT0_CHANNEL_GROUP2_ENA_CLR	VPDMA INT0 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
1	VPDMA_INT0_CHANNEL_GROUP1_ENA_CLR	VPDMA INT0 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT0_CHANNEL_GROUP0_ENA_CLR	VPDMA INT0 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-91. Register Call Summary for Register VIP_INTC_INTR0_ENA_CLR1

VIP Register Manual
- VIP Top Level Register Summary: [0]

Table 9-92. VIP_INTC_INTR1_STATUS_RAW0

Address Offset	0x0000 0040		
Physical Address	0x4897 0040 0x4899 0040 0x489B 0040	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Status Raw/Set Register 0. This register contains the raw interrupt status as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	RESERVED			VPDMA_INT1_DESCRIPTOR_RAW	VPDMA_INT1_LIST7_NOTIFY_RAW	VPDMA_INT1_LIST7_COMPLETE_RAW	VPDMA_INT1_LIST6_NOTIFY_RAW	VPDMA_INT1_LIST6_COMPLETE_RAW	VPDMA_INT1_LIST5_NOTIFY_RAW	VPDMA_INT1_LIST5_COMPLETE_RAW	VPDMA_INT1_LIST4_NOTIFY_RAW	VPDMA_INT1_LIST4_COMPLETE_RAW	VPDMA_INT1_LIST3_NOTIFY_RAW	VPDMA_INT1_LIST3_COMPLETE_RAW	VPDMA_INT1_LIST2_NOTIFY_RAW	VPDMA_INT1_LIST2_COMPLETE_RAW	VPDMA_INT1_LIST1_NOTIFY_RAW	VPDMA_INT1_LIST1_COMPLETE_RAW	VPDMA_INT1_LIST0_NOTIFY_RAW	VPDMA_INT1_LIST0_COMPLETE_RAW

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_RAW	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_RAW	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT1_DESCRIPTOR_RAW	VPDMA INT1 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
15	VPDMA_INT1_LIST7_NOTIFY_RAW	VPDMA INT1 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
14	VPDMA_INT1_LIST7_COMPLETE_RAW	VPDMA INT1 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
13	VPDMA_INT1_LIST6_NOTIFY_RAW	VPDMA INT1 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
12	VPDMA_INT1_LIST6_COMPLETE_RAW	VPDMA INT1 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
11	VPDMA_INT1_LIST5_NOTIFY_RAW	VPDMA INT1 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
10	VPDMA_INT1_LIST5_COMPLETE_RAW	VPDMA INT1 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
9	VPDMA_INT1_LIST4_NOTIFY_RAW	VPDMA INT1 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
8	VPDMA_INT1_LIST4_COMPLETE_RAW	VPDMA INT1 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
7	VPDMA_INT1_LIST3_NOTIFY_RAW	VPDMA INT1 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_LIST3_COMPLETE_RAW	VPDMA INT1 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
5	VPDMA_INT1_LIST2_NOTIFY_RAW	VPDMA INT1 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_LIST2_COMPLETE_RAW	VPDMA INT1 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_LIST1_NOTIFY_RAW	VPDMA INT1 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_LIST1_COMPLETE_RAW	VPDMA INT1 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_LIST0_NOTIFY_RAW	VPDMA INT1 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_LIST0_COMPLETE_RAW	VPDMA INT1 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-93. Register Call Summary for Register VIP_INTC_INTR1_STATUS_RAW0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-94. VIP_INTC_INTR1_STATUS_RAW1

Address Offset	0x0000 0044		
Physical Address	0x4897 0044 0x4899 0044 0x489B 0044	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Status Raw/Set Register 1. This register contains the raw interrupt status as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW	VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	RESERVED														VPDMA_INT1_CLIENT_RAW	RESERVED	VPDMA_INT1_CHANNEL_GROUP5_RAW	VPDMA_INT1_CHANNEL_GROUP4_RAW	VPDMA_INT1_CHANNEL_GROUP3_RAW	VPDMA_INT1_CHANNEL_GROUP2_RAW	VPDMA_INT1_CHANNEL_GROUP1_RAW	VPDMA_INT1_CHANNEL_GROUP0_RAW

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT1_CLIENT_RAW	VPDMA INT1 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	RESERVED		R	0x0
5	VPDMA_INT1_CHANNEL_GROUP5_RAW	VPDMA INT1 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_CHANNEL_GROUP4_RAW	VPDMA INT1 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_CHANNEL_GROUP3_RAW	VPDMA INT1 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_CHANNEL_GROUP2_RAW	VPDMA INT1 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_CHANNEL_GROUP1_RAW	VPDMA INT1 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_CHANNEL_GROUP0_RAW	VPDMA INT1 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-95. Register Call Summary for Register VIP_INTC_INTR1_STATUS_RAW1

VIP Register Manual

- VIP Top Level Register Summary: [0]

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Table 9-96. VIP_INTC_INTR1_STATUS_ENA0

Address Offset	0x0000 0048		
Physical Address	0x4897 0048 0x4899 0048 0x489B 0048	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Status Enabled/Clear Register 0. This register contains the enabled interrupt status as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	RESERVED			VPDMA_INT1_DESCRIPTOR_ENA	VPDMA_INT1_LIST7_NOTIFY_ENA	VPDMA_INT1_LIST7_COMPLETE_ENA	VPDMA_INT1_LIST6_NOTIFY_ENA	VPDMA_INT1_LIST6_COMPLETE_ENA	VPDMA_INT1_LIST5_NOTIFY_ENA	VPDMA_INT1_LIST5_COMPLETE_ENA	VPDMA_INT1_LIST4_NOTIFY_ENA	VPDMA_INT1_LIST4_COMPLETE_ENA	VPDMA_INT1_LIST3_NOTIFY_ENA	VPDMA_INT1_LIST3_COMPLETE_ENA	VPDMA_INT1_LIST2_NOTIFY_ENA	VPDMA_INT1_LIST2_COMPLETE_ENA	VPDMA_INT1_LIST1_NOTIFY_ENA	VPDMA_INT1_LIST1_COMPLETE_ENA	VPDMA_INT1_LIST0_NOTIFY_ENA	VPDMA_INT1_LIST0_COMPLETE_ENA

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT1_DESCRIPTOR_ENA	VPDMA INT1 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
15	VPDMA_INT1_LIST7_NOTIFY_ENA	VPDMA INT1 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT1_LIST7_COMPLETE_ENA	VPDMA INT1 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT1_LIST6_NOTIFY_ENA	VPDMA INT1 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT1_LIST6_COMPLETE_ENA	VPDMA INT1 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT1_LIST5_NOTIFY_ENA	VPDMA INT1 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT1_LIST5_COMPLETE_ENA	VPDMA INT1 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT1_LIST4_NOTIFY_ENA	VPDMA INT1 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
8	VPDMA_INT1_LIST4_COMPLETE_ENA	VPDMA INT1 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
7	VPDMA_INT1_LIST3_NOTIFY_ENA	VPDMA INT1 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_LIST3_COMPLETE_ENA	VPDMA INT1 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT1_LIST2_NOTIFY_ENA	VPDMA INT1 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_LIST2_COMPLETE_ENA	VPDMA INT1 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_LIST1_NOTIFY_ENA	VPDMA INT1 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_LIST1_COMPLETE_ENA	VPDMA INT1 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_LIST0_NOTIFY_ENA	VPDMA INT1 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_LIST0_COMPLETE_ENA	VPDMA INT1 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-97. Register Call Summary for Register VIP_INTC_INTR1_STATUS_ENA0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-98. VIP_INTC_INTR1_STATUS_ENA1

Address Offset	0x0000 004C		
Physical Address	0x4897 004C 0x4899 004C 0x489B 004C	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Status Enabled/Clear Register 1. This register contains the enabled interrupt status as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA	VIP2_CHR_DS_1_UV_ERR_INT_ENA	VIP1_CHR_DS_2_UV_ERR_INT_ENA	VIP1_CHR_DS_1_UV_ERR_INT_ENA	RESERVED														VPDMA_INT1_CLIENT_ENA	RESERVED	VPDMA_INT1_CHANNEL_GROUP5_ENA	VPDMA_INT1_CHANNEL_GROUP4_ENA	VPDMA_INT1_CHANNEL_GROUP3_ENA	VPDMA_INT1_CHANNEL_GROUP2_ENA	VPDMA_INT1_CHANNEL_GROUP1_ENA	VPDMA_INT1_CHANNEL_GROUP0_ENA

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT1_CLIENT_ENA	VPDMA INT1 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
6	RESERVED		R	0x0
5	VPDMA_INT1_CHANNEL_GROUP5_ENA	VPDMA INT1 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_CHANNEL_GROUP4_ENA	VPDMA INT1 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_CHANNEL_GROUP3_ENA	VPDMA INT1 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_CHANNEL_GROUP2_ENA	VPDMA INT1 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_CHANNEL_GROUP1_ENA	VPDMA INT1 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_CHANNEL_GROUP0_ENA	VPDMA INT1 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect	RW	0x0

Table 9-99. Register Call Summary for Register VIP_INTC_INTR1_STATUS_ENA1

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-100. VIP_INTC_INTR1_ENA_SET0

Address Offset	0x0000 0050		
Physical Address	0x4897 0050 0x4899 0050 0x489B 0050	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Enable/Set Register 0. This register contains the interrupt enable status/set as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	RESERVED			VPDMA_INT1_DESCRIPTOR_ENA_SET	VPDMA_INT1_LIST7_NOTIFY_ENA_SET	VPDMA_INT1_LIST7_COMPLETE_ENA_SET	VPDMA_INT1_LIST6_NOTIFY_ENA_SET	VPDMA_INT1_LIST6_COMPLETE_ENA_SET	VPDMA_INT1_LIST5_NOTIFY_ENA_SET	VPDMA_INT1_LIST5_COMPLETE_ENA_SET	VPDMA_INT1_LIST4_NOTIFY_ENA_SET	VPDMA_INT1_LIST4_COMPLETE_ENA_SET	VPDMA_INT1_LIST3_NOTIFY_ENA_SET	VPDMA_INT1_LIST3_COMPLETE_ENA_SET	VPDMA_INT1_LIST2_NOTIFY_ENA_SET	VPDMA_INT1_LIST2_COMPLETE_ENA_SET	VPDMA_INT1_LIST1_NOTIFY_ENA_SET	VPDMA_INT1_LIST1_COMPLETE_ENA_SET	VPDMA_INT1_LIST0_NOTIFY_ENA_SET	VPDMA_INT1_LIST0_COMPLETE_ENA_SET

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA_SET	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA_SET	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT1_DESCRIPTOR_ENA_SET	VPDMA INT1 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
15	VPDMA_INT1_LIST7_NOTIFY_ENA_SET	VPDMA INT1 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT1_LIST7_COMPLETE_ENA_SET	VPDMA INT1 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT1_LIST6_NOTIFY_ENA_SET	VPDMA INT1 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT1_LIST6_COMPLETE_ENA_SET	VPDMA INT1 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT1_LIST5_NOTIFY_ENA_SET	VPDMA INT1 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT1_LIST5_COMPLETE_ENA_SET	VPDMA INT1 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT1_LIST4_NOTIFY_ENA_SET	VPDMA INT1 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
8	VPDMA_INT1_LIST4_COMPLETE_ENA_SET	VPDMA INT1 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
7	VPDMA_INT1_LIST3_NOTIFY_ENA_SET	VPDMA INT1 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_LIST3_COMPLETE_ENA_SET	VPDMA INT1 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT1_LIST2_NOTIFY_ENA_SET	VPDMA INT1 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_LIST2_COMPLETE_ENA_SET	VPDMA INT1 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_LIST1_NOTIFY_ENA_SET	VPDMA INT1 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_LIST1_COMPLETE_ENA_SET	VPDMA INT1 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_LIST0_NOTIFY_ENA_SET	VPDMA INT1 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_LIST0_COMPLETE_ENA_SET	VPDMA INT1 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-101. Register Call Summary for Register VIP_INTC_INTR1_ENA_SET0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-102. VIP_INTC_INTR1_ENA_SET1

Address Offset	0x0000 0054		
Physical Address	0x4897 0054 0x4899 0054 0x489B 0054	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Enable/Set Register 1. This register contains the interrupt enable status/set as defined in HL0.8		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	RESERVED														VPDMA_INT1_CLIENT_ENA_SET	VPDMA_INT1_CHANNEL_GROUP6_ENA_SET	VPDMA_INT1_CHANNEL_GROUP5_ENA_SET	VPDMA_INT1_CHANNEL_GROUP4_ENA_SET	VPDMA_INT1_CHANNEL_GROUP3_ENA_SET	VPDMA_INT1_CHANNEL_GROUP2_ENA_SET	VPDMA_INT1_CHANNEL_GROUP1_ENA_SET	VPDMA_INT1_CHANNEL_GROUP0_ENA_SET

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT1_CLIENT_ENA_SET	VPDMA INT1 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_CHANNEL_GROUP6_ENA_SET	VPDMA INT1 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT1_CHANNEL_GROUP5_ENA_SET	VPDMA INT1 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_CHANNEL_GROUP4_ENA_SET	VPDMA INT1 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_CHANNEL_GROUP3_ENA_SET	VPDMA INT1 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_CHANNEL_GROUP2_ENA_SET	VPDMA INT1 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
1	VPDMA_INT1_CHANNEL_GROUP1_ENA_SET	VPDMA INT1 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_CHANNEL_GROUP0_ENA_SET	VPDMA INT1 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-103. Register Call Summary for Register VIP_INTC_INTR1_ENA_SET1

VIP Register Manual
- VIP Top Level Register Summary: [0]

Table 9-104. VIP_INTC_INTR1_ENA_CLR0

Address Offset	0x0000 0058		
Physical Address	0x4897 0058 0x4899 0058 0x489B 0058	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Enable/Clear Register 0. This register contains the interrupt enable status/clear as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	RESERVED			VPDMA_INT1_DESCRIPTOR_ENA_CLR	VPDMA_INT1_LIST7_NOTIFY_ENA_CLR	VPDMA_INT1_LIST7_COMPLETE_ENA_CLR	VPDMA_INT1_LIST6_NOTIFY_ENA_CLR	VPDMA_INT1_LIST6_COMPLETE_ENA_CLR	VPDMA_INT1_LIST5_NOTIFY_ENA_CLR	VPDMA_INT1_LIST5_COMPLETE_ENA_CLR	VPDMA_INT1_LIST4_NOTIFY_ENA_CLR	VPDMA_INT1_LIST4_COMPLETE_ENA_CLR	VPDMA_INT1_LIST3_NOTIFY_ENA_CLR	VPDMA_INT1_LIST3_COMPLETE_ENA_CLR	VPDMA_INT1_LIST2_NOTIFY_ENA_CLR	VPDMA_INT1_LIST2_COMPLETE_ENA_CLR	VPDMA_INT1_LIST1_NOTIFY_ENA_CLR	VPDMA_INT1_LIST1_COMPLETE_ENA_CLR	VPDMA_INT1_LIST0_NOTIFY_ENA_CLR	VPDMA_INT1_LIST0_COMPLETE_ENA_CLR

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	VIP2_PARSER_INT_ENA_CLR	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
20	VIP1_PARSER_INT_ENA_CLR	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
19:17	RESERVED		R	0x0
16	VPDMA_INT1_DESCRIPTOR_ENA_CLR	VPDMA INT1 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	VPDMA_INT1_LIST7_NOTIFY_ENA_CLR	VPDMA INT1 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
14	VPDMA_INT1_LIST7_COMPLETE_ENA_CLR	VPDMA INT1 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
13	VPDMA_INT1_LIST6_NOTIFY_ENA_CLR	VPDMA INT1 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
12	VPDMA_INT1_LIST6_COMPLETE_ENA_CLR	VPDMA INT1 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
11	VPDMA_INT1_LIST5_NOTIFY_ENA_CLR	VPDMA INT1 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
10	VPDMA_INT1_LIST5_COMPLETE_ENA_CLR	VPDMA INT1 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
9	VPDMA_INT1_LIST4_NOTIFY_ENA_CLR	VPDMA INT1 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
8	VPDMA_INT1_LIST4_COMPLETE_ENA_CLR	VPDMA INT1 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
7	VPDMA_INT1_LIST3_NOTIFY_ENA_CLR	VPDMA INT1 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_LIST3_COMPLETE_ENA_CLR	VPDMA INT1 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
5	VPDMA_INT1_LIST2_NOTIFY_ENA_CLR	VPDMA INT1 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_LIST2_COMPLETE_ENA_CLR	VPDMA INT1 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_LIST1_NOTIFY_ENA_CLR	VPDMA INT1 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_LIST1_COMPLETE_ENA_CLR	VPDMA INT1 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_LIST0_NOTIFY_ENA_CLR	VPDMA INT1 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_LIST0_COMPLETE_ENA_CLR	VPDMA INT1 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

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Table 9-105. Register Call Summary for Register VIP_INTC_INTR1_ENA_CLR0

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-106. VIP_INTC_INTR1_ENA_CLR1

Address Offset	0x0000 005C		
Physical Address	0x4897 005C 0x4899 005C 0x489B 005C	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC intr1 Interrupt Enable/Clear Register 1. This register contains the interrupt enable status/clear as defined in HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	RESERVED														VPDMA_INT1_CLIENT_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP0_ENA_CLR

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x0
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
21:8	RESERVED		R	0x0
7	VPDMA_INT1_CLIENT_ENA_CLR	VPDMA INT1 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
6	VPDMA_INT1_CHANNEL_GROUP6_ENA_CLR	VPDMA INT1 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

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Bits	Field Name	Description	Type	Reset
5	VPDMA_INT1_CHANNEL_GROUP5_ENA_CLR	VPDMA INT1 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
4	VPDMA_INT1_CHANNEL_GROUP4_ENA_CLR	VPDMA INT1 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
3	VPDMA_INT1_CHANNEL_GROUP3_ENA_CLR	VPDMA INT1 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
2	VPDMA_INT1_CHANNEL_GROUP2_ENA_CLR	VPDMA INT1 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
1	VPDMA_INT1_CHANNEL_GROUP1_ENA_CLR	VPDMA INT1 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0
0	VPDMA_INT1_CHANNEL_GROUP0_ENA_CLR	VPDMA INT1 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect	RW	0x0

Table 9-107. Register Call Summary for Register VIP_INTC_INTR1_ENA_CLR1

VIP Register Manual
- VIP Top Level Register Summary: [0]

Table 9-108. VIP_INTC_EOI

Address Offset	0x0000 00A0		
Physical Address	0x4897 00A0 0x4899 00A0 0x489B 00A0	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	INTC EOI Register. This register contains the EOI vector register contents as defined by HL0.8		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOI_VECTOR																															

Bits	Field Name	Description	Type	Reset
31:0	EOI_VECTOR	Number associated with the ipgenericirq for intr output. There are 4 interrupt outputs Write 0x0 : Write to intr0 IP Generic Write 0x1 : Write to intr1 IP Generic Write 0x2 : Write to intr2 IP Generic Write 0x3 : Write to intr3 IP Generic Any other write value is ignored.	RW	0x0

Table 9-109. Register Call Summary for Register VIP_INTC_EOI

VIP Register Manual
- VIP Top Level Register Summary: [0]

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Table 9-110. VIP_CLKC_CLKEN

Address Offset	0x0000 0100		
Physical Address	0x4897 0100 0x4899 0100 0x489B 0100	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	CLKC Module Clock Enable Register. This register contains clock enables for the processing paths in the VIP module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														VIP2_DP_EN	VIP1_DP_EN	RESERVED															VPDMA_EN

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0
17	VIP2_DP_EN	VIP Slice1 Data Path Clock Enable, 1 = Clock Enabled, 0 = Clock Disabled	RW	0x0
16	VIP1_DP_EN	VIP Slice0 Data Path Clock Enable, 1 = Clock Enabled, 0 = Clock Disabled	RW	0x0
15:1	RESERVED		R	0x0
0	VPDMA_EN	VPDMA Clock Enable, 1 = Clock Enabled, 0 = Clock Disabled	RW	0x0

Table 9-111. Register Call Summary for Register VIP_CLKC_CLKEN

VIP Functional Description
- VIP Clocks: [0] [1] [2]

VIP Register Manual
- VIP Top Level Register Summary: [3]

Table 9-112. VIP_CLKC_RST

Address Offset	0x0000 0104		
Physical Address	0x4897 0104 0x4899 0104 0x489B 0104	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	CLKC Module Reset Register. This register contains resets for the processing paths in the VIP module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAIN_RST	RESERVED		S1_CHR_DS_1_RST	S0_CHR_DS_1_RST	S1_CHR_DS_0_RST	S0_CHR_DS_0_RST	RESERVED	S1_SC_RST	S0_SC_RST	S1_CSC_RST	S0_CSC_RST	S1_PARSER_RST	S0_PARSER_RST	VIP2_DP_RST	VIP1_DP_RST	RESERVED															VPDMA_RST

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Bits	Field Name	Description	Type	Reset
31	MAIN_RST	Reset for all modules in VIP Main Data Path	RW	0x0
30:29	RESERVED	Reserved	R	0x0
28	S1_CHR_DS_1_RST	VIP Slice1 CHRDS1 reset	RW	0x0
27	S0_CHR_DS_1_RST	VIP Slice0 CHRDS1 reset	RW	0x0
26	S1_CHR_DS_0_RST	VIP Slice1 CHRDS0 reset	RW	0x0
25	S0_CHR_DS_0_RST	VIP Slice0 CHRDS0 reset	RW	0x0
24	RESERVED	Reserved	RW	0x0
23	S1_SC_RST	VIP Slice1 SC reset	RW	0x0
22	S0_SC_RST	VIP Slice0 SC reset	RW	0x0
21	S1_CSC_RST	VIP Slice1 CSC reset	RW	0x0
20	S0_CSC_RST	VIP Slice0 CSC reset	RW	0x0
19	S1_PARSER_RST	VIP Slice1 parser reset	RW	0x0
18	S0_PARSER_RST	VIP Slice0 parser reset	RW	0x0
17	VIP2_DP_RST	VIP Slice1 Data Path Reset	RW	0x0
16	VIP1_DP_RST	VIP Slice0 Data Path Reset	RW	0x0
15:1	RESERVED	Reserved	R	0x0000
0	VPDMA_RST	VPDMA Reset	RW	0x0

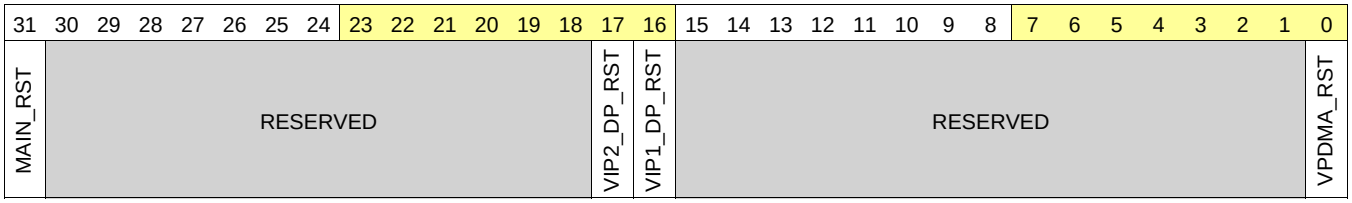
Table 9-113. Register Call Summary for Register VIP_CLKC_RST

VIP Functional Description
- VIP Software Reset: [0] [1] [2] [3]
- VIP Overflow Detection and Recovery: [4] [5]

VIP Register Manual
- VIP Top Level Register Summary: [6]

Table 9-114. VIP_CLKC_DPS

Address Offset	0x0000 0108		
Physical Address	0x4897 0108 0x4899 0108 0x489B 0108	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	CLKC Main Data Path Select Register. This register selects the various data paths within main portion (non-VIP) of the subsystem		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	MAIN_RST	Reset for all modules in DSS Main Data Path	RW	0x0
30:18	RESERVED		R	0x0
17	VIP2_DP_RST	Video Input Port 2 Data Path Reset	RW	0x0
16	VIP1_DP_RST	Video Input Port 1 Data Path Reset	RW	0x0
15:1	RESERVED		R	0x0
0	VPDMA_RST	VPDMA Reset	RW	0x0

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Table 9-115. Register Call Summary for Register VIP_CLKC_DPS

VIP Register Manual

- VIP Top Level Register Summary: [0]

Table 9-116. VIP_CLKC_VIP0DPS

Address Offset	0x0000 010C		
Physical Address	0x4897 010C 0x4899 010C 0x489B 010C	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	CLKC Video Input Port 1 Data Path Select Register. This register selects the various data paths within the Video Input Port portion of the subsystem		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIP1_DATAPATH_SELECT				VIP1_TESTPORT_A_SELECT	VIP1_TESTPORT_B_SELECT	RESERVED								VIP1_CHR_DS_2_BYPASS	VIP1_CHR_DS_1_BYPASS	VIP1_MULTI_CHANNEL_SELECT				VIP1_CHR_DS_2_SRC_SELECT				VIP1_CHR_DS_1_SRC_SELECT				VIP1_RGB_OUT_HI_SELECT				VIP1_RGB_OUT_LO_SELECT	VIP1_RGB_SRC_SELECT	VIP1_SC_SRC_SELECT			VIP1_CSC_SRC_SELECT		

Bits	Field Name	Description	Type	Reset
31:28	VIP1_DATAPATH_SELECT	VIP1 Datapath Register Field Enable 0000 : All fields written 0001 : Only vip1_csc_src_select written 0010 : Only vip1_sc_src_select written 0011 : Only vip1_rgb_src_select written 0100 : Only vip1_rgb_out_lo_select written 0101 : Only vip1_rgb_out_hi_select written 0110 : Only vip1_chr_ds_1_src_select written 0111 : Only vip1_chr_ds_2_src_select written 1000 : Only vip1_multi_channel_select written 1001 : Only vip1_chr_ds_1_bypass written 1010 : Only vip1_chr_ds_2_bypass written 1011 : Reserved 1100 : Reserved 1101 : Reserved 1110 : Reserved 1111 : Reserved	RW	0x0
27	VIP1_TESTPORT_A_SELECT	0 : Normal mode 1: Test Mode	RW	0x0
26	VIP1_TESTPORT_B_SELECT	0 : Normal mode 1: Test Mode	RW	0x0
25:18	RESERVED		R	0x0
17	VIP1_CHR_DS_2_BYPASS	Video Input Port 1 Chroma Downsampler 2 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420	RW	0x0
16	VIP1_CHR_DS_1_BYPASS	Video Input Port 1 Chroma Downsampler 1 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	VIP1_MULTI_CHANNEL_SELECT	Video Input Port 1 Multi Channel Select 0 : VIP_PARSER A and B channels operate in single channel mode 1 : VIP_PARSER A and B channels directly drive VPDMA (multi-channel case) Multi-Channel means that the A and B sources are from multiple channels and used in a multiplexed stream mode. The VIP Parser extracts the channel ID from each source and outputs this information to VPDMA, and thus to memory. When operating in a multiplexed stream mode, this bit must be set to 1 to enable the channel information to be passed to memory. If this is not set, the channel number (or source number) will be 0 for all streams. If vip1_rgb_out_select = 1, then VIP_PARSER A port is connected to VPDMA	RW	0x0
14:12	VIP1_CHR_DS_2_SRC_SELECT	Video Input Port 1 Chroma Downsampler 2 Source Select 0 : Path Disabled (no input to CHR_DS) 1 : Source from Scaler (SC_M) 2 : Source from Color Space Converter (CSC) 3 : Source from VIP_PARSER A port 4 : Source from VIP_PARSER B port 5 : Source from Transcode (422) 6 : Reserved 7 : Reserved	RW	0x0
11:9	VIP1_CHR_DS_1_SRC_SELECT	Video Input Port 1 Chroma Downsampler 1 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved	RW	0x0
8	VIP1_RGB_OUT_HI_SELECT	Video Input Port 1 HI RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB	RW	0x0
7	VIP1_RGB_OUT_LO_SELECT	Video Input Port 1 LO RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB	RW	0x0
6	VIP1_RGB_SRC_SELECT	Video Input Port 1 RGB Output Path Select 0 : Source from Compositor RGB input 1 : Source from CSC	RW	0x0
5:3	VIP1_SC_SRC_SELECT	Video Input Port 1 SC_M Source Select 000 : Path Disabled 001 : Source from Color Space Converter (CSC) 010 : Source from VIP_PARSER A port 011 : Source from VIP_PARSER B port 100 : Source from Transcode (422) 101 : Reserved 110 : Reserved 111 : Reserved	RW	0x0
2:0	VIP1_CSC_SRC_SELECT	Video Input Port 1 CSC Source Select 000 : Path Disabled 001 : Source from VIP_PARSER A (422) port 010 : Source from VIP_PARSER B port 011 : Source from Transcode (422) 100 : Source from VIP_PARSER A (RGB) port 101 : Source from Compositor (RGB) 110 : Reserved 111 : Reserved	RW	0x0

Table 9-117. Register Call Summary for Register VIP_CLKC_VIP0DPS

VIP Functional Description
- VIP Slice Processing Path Overview: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- VIP Slice Processing Path Multiplexers: [11] [12]

VIP Register Manual
- VIP Top Level Register Summary: [13]

Table 9-118. VIP_CLKC_VIP1DPS

Address Offset	0x0000 0110		
Physical Address	0x4897 0110 0x4899 0110 0x489B 0110	**Instance**	VIP1_top_level VIP2_top_level VIP3_top_level
Description	CLKC Video Input Port 2 Data Path Select Register. This register selects the various data paths within the Video Input Port portion of the subsystem		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIP2_DATAPATH_SELECT				VIP2_TESTPORT_A_SELECT	VIP2_TESTPORT_B_SELECT	RESERVED								VIP2_CHR_DS_2_BYPASS	VIP2_CHR_DS_1_BYPASS	VIP2_MULTI_CHANNEL_SELECT	VIP2_CHR_DS_2_SRC_SELECT			VIP2_CHR_DS_1_SRC_SELECT			VIP2_RGB_OUT_HI_SELECT	VIP2_RGB_OUT_LO_SELECT	VIP2_RGB_SRC_SELECT	VIP2_SC_SRC_SELECT				VIP2_CSC_SRC_SELECT		

Bits	Field Name	Description	Type	Reset
31:28	VIP2_DATAPATH_SELECT	VIP2 Datapath Register Field Enable 0000 : All fields written 0001 : Only vip2_csc_src_select written 0010 : Only vip2_sc_src_select written 0011 : Only vip2_rgb_src_select written 0100 : Only vip2_rgb_out_lo_select written 0101 : Only vip2_rgb_out_hi_select written 0110 : Only vip2_chr_ds_1_src_select written 0111 : Only vip2_chr_ds_2_src_select written 1000 : Only vip2_multi_channel_select written 1001 : Only vip2_chr_ds_1_bypass written 1010 : Only vip2_chr_ds_2_bypass written 1011 : Reserved 1100 : Reserved 1101 : Reserved 1110 : Reserved 1111 : Reserved	RW	0x0
27	VIP2_TESTPORT_A_SELECT	0 : Normal mode 1: Test Mode	RW	0x0
26	VIP2_TESTPORT_B_SELECT	0 : Normal mode 1: Test Mode	RW	0x0
25:18	RESERVED		R	0x0
17	VIP2_CHR_DS_2_BYPASS	Video Input Port 2 Chroma Downsampler 2 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420	RW	0x0
16	VIP2_CHR_DS_1_BYPASS	Video Input Port 2 Chroma Downsampler 1 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420	RW	0x0
15	VIP2_MULTI_CHANNEL_SELECT	Video Input Port 2 Multi Channel Select 0 : VIP_PARSER A and B channels operate in single channel mode 1 : VIP_PARSER A and B channels directly drive VPDMA (multi-channel case) Multi-Channel means that the A and B sources are from multiple channels and used in a multiplexed stream mode. The VIP Parser extracts the channel ID from each source and outputs this information to VPDMA, and thus to memory. When operating in a multiplexed stream mode, this bit must be set to 1 to enable the channel information to be passed to memory. If this is not set, the channel number (or source number) will be 0 for all streams. If vip2_rgb_out_select = 1, then VIP_PARSER A port is connected to VPDMA	RW	0x0
14:12	VIP2_CHR_DS_2_SRC_SELECT	Video Input Port 2 Chroma Downsampler 2 Source Select 0 : Path Disabled (no input to CHR_DS) 1 : Source from Scaler (SC_M) 2 : Source from Color Space Converter (CSC) 3 : Source from VIP_PARSER A port 4 : Source from VIP_PARSER B port 5 : Source from Transcode (422) 6 : Reserved 7 : Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
11:9	VIP2_CHR_DS_1_SRC_SELECT	Video Input Port 2 Chroma Downsampler 1 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved	RW	0x0
8	VIP2_RGB_OUT_HI_SELECT	Video Input Port 2 HI RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB	RW	0x0
7	VIP2_RGB_OUT_LO_SELECT	Video Input Port 2 LO RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB	RW	0x0
6	VIP2_RGB_SRC_SELECT	Video Input Port 2 RGB Output Path Select 0 : Source from Compositor RGB input 1 : Source from CSC	RW	0x0
5:3	VIP2_SC_SRC_SELECT	Video Input Port 2 SC_M Source Select 000 : Path Disabled 001 : Source from Color Space Converter (CSC) 010 : Source from VIP_PARSER A port 011 : Source from VIP_PARSER B port 100 : Source from Transcode (422) 101 : Reserved 110 : Reserved 111 : Reserved	RW	0x0
2:0	VIP2_CSC_SRC_SELECT	Video Input Port 2 CSC Source Select 000 : Path Disabled 001 : Source from VIP_PARSER A (422) port 010 : Source from VIP_PARSER B port 011 : Source from Transcode (422) 100 : Source from VIP_PARSER A (RGB) port 101 : Source from Compositor (RGB) 110 : Reserved 111 : Reserved	RW	0x0

Table 9-119. Register Call Summary for Register VIP_CLKC_VIP1DPS

VIP Functional Description
- VIP Slice Processing Path Overview: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- VIP Slice Processing Path Multiplexers: [11] [12]

VIP Register Manual
- VIP Top Level Register Summary: [13]

9.5.3 VIP Parser Registers

9.5.3.1 VIP Parser Register Summary

Table 9-120. VIP Parser Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_Slice0_parser Base Address	VIP1_Slice1_parser Base Address	VIP2_Slice0_parser Base Address
VIP_MAIN	RW	32	0x0000 0000	0x4897 5500	0x4897 5A00	0x4899 5500
VIP_PORT_A	RW	32	0x0000 0004	0x4897 5504	0x4897 5A04	0x4899 5504
VIP_XTRA_PORT_A	RW	32	0x0000 0008	0x4897 5508	0x4897 5A08	0x4899 5508
VIP_PORT_B	RW	32	0x0000 000C	0x4897 550C	0x4897 5A0C	0x4899 550C
VIP_XTRA_PORT_B	RW	32	0x0000 0010	0x4897 5510	0x4897 5A10	0x4899 5510
VIP_FIQ_MASK	RW	32	0x0000 0014	0x4897 5514	0x4897 5A14	0x4899 5514
VIP_FIQ_CLEAR	RW	32	0x0000 0018	0x4897 5518	0x4897 5A18	0x4899 5518
VIP_FIQ_STATUS	R	32	0x0000 001C	0x4897 551C	0x4897 5A1C	0x4899 551C
VIP_OUTPUT_PORT_A_SRC_FID	R	32	0x0000 0020	0x4897 5520	0x4897 5A20	0x4899 5520
VIP_OUTPUT_PORT_A_ENC_FID	R	32	0x0000 0024	0x4897 5524	0x4897 5A24	0x4899 5524
VIP_OUTPUT_PORT_B_SRC_FID	R	32	0x0000 0028	0x4897 5528	0x4897 5A28	0x4899 5528
VIP_OUTPUT_PORT_B_ENC_FID	R	32	0x0000 002C	0x4897 552C	0x4897 5A2C	0x4899 552C
VIP_OUTPUT_PORT_A_SRC0_SIZE	R	32	0x0000 0030	0x4897 5530	0x4897 5A30	0x4899 5530
VIP_OUTPUT_PORT_A_SRC1_SIZE	R	32	0x0000 0034	0x4897 5534	0x4897 5A34	0x4899 5534
VIP_OUTPUT_PORT_A_SRC2_SIZE	R	32	0x0000 0038	0x4897 5538	0x4897 5A38	0x4899 5538
VIP_OUTPUT_PORT_A_SRC3_SIZE	R	32	0x0000 003C	0x4897 553C	0x4897 5A3C	0x4899 553C
VIP_OUTPUT_PORT_A_SRC4_SIZE	R	32	0x0000 0040	0x4897 5540	0x4897 5A40	0x4899 5540

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Table 9-120. VIP Parser Registers Mapping Summary 1 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_Slice0_parser Base Address	VIP1_Slice1_parser Base Address	VIP2_Slice0_parser Base Address
VIP_OUTPUT_PORT_A_SRC5_SIZE	R	32	0x0000 0044	0x4897 5544	0x4897 5A44	0x4899 5544
VIP_OUTPUT_PORT_A_SRC6_SIZE	R	32	0x0000 0048	0x4897 5548	0x4897 5A48	0x4899 5548
VIP_OUTPUT_PORT_A_SRC7_SIZE	R	32	0x0000 004C	0x4897 554C	0x4897 5A4C	0x4899 554C
VIP_OUTPUT_PORT_A_SRC8_SIZE	R	32	0x0000 0050	0x4897 5550	0x4897 5A50	0x4899 5550
VIP_OUTPUT_PORT_A_SRC9_SIZE	R	32	0x0000 0054	0x4897 5554	0x4897 5A54	0x4899 5554
VIP_OUTPUT_PORT_A_SRC10_SIZE	R	32	0x0000 0058	0x4897 5558	0x4897 5A58	0x4899 5558
VIP_OUTPUT_PORT_A_SRC11_SIZE	R	32	0x0000 005C	0x4897 555C	0x4897 5A5C	0x4899 555C
VIP_OUTPUT_PORT_A_SRC12_SIZE	R	32	0x0000 0060	0x4897 5560	0x4897 5A60	0x4899 5560
VIP_OUTPUT_PORT_A_SRC13_SIZE	R	32	0x0000 0064	0x4897 5564	0x4897 5A64	0x4899 5564
VIP_OUTPUT_PORT_A_SRC14_SIZE	R	32	0x0000 0068	0x4897 5568	0x4897 5A68	0x4899 5568
VIP_OUTPUT_PORT_A_SRC15_SIZE	R	32	0x0000 006C	0x4897 556C	0x4897 5A6C	0x4899 556C
VIP_OUTPUT_PORT_B_SRC0_SIZE	R	32	0x0000 0070	0x4897 5570	0x4897 5A70	0x4899 5570
VIP_OUTPUT_PORT_B_SRC1_SIZE	R	32	0x0000 0074	0x4897 5574	0x4897 5A74	0x4899 5574
VIP_OUTPUT_PORT_B_SRC2_SIZE	R	32	0x0000 0078	0x4897 5578	0x4897 5A78	0x4899 5578
VIP_OUTPUT_PORT_B_SRC3_SIZE	R	32	0x0000 007C	0x4897 557C	0x4897 5A7C	0x4899 557C
VIP_OUTPUT_PORT_B_SRC4_SIZE	R	32	0x0000 0080	0x4897 5580	0x4897 5A80	0x4899 5580
VIP_OUTPUT_PORT_B_SRC5_SIZE	R	32	0x0000 0084	0x4897 5584	0x4897 5A84	0x4899 5584
VIP_OUTPUT_PORT_B_SRC6_SIZE	R	32	0x0000 0088	0x4897 5588	0x4897 5A88	0x4899 5588
VIP_OUTPUT_PORT_B_SRC7_SIZE	R	32	0x0000 008C	0x4897 558C	0x4897 5A8C	0x4899 558C
VIP_OUTPUT_PORT_B_SRC8_SIZE	R	32	0x0000 0090	0x4897 5590	0x4897 5A90	0x4899 5590
VIP_OUTPUT_PORT_B_SRC9_SIZE	R	32	0x0000 0094	0x4897 5594	0x4897 5A94	0x4899 5594
VIP_OUTPUT_PORT_B_SRC10_SIZE	R	32	0x0000 0098	0x4897 5598	0x4897 5A98	0x4899 5598
VIP_OUTPUT_PORT_B_SRC11_SIZE	R	32	0x0000 009C	0x4897 559C	0x4897 5A9C	0x4899 559C
VIP_OUTPUT_PORT_B_SRC12_SIZE	R	32	0x0000 00A0	0x4897 55A0	0x4897 5AA0	0x4899 55A0
VIP_OUTPUT_PORT_B_SRC13_SIZE	R	32	0x0000 00A4	0x4897 55A4	0x4897 5AA4	0x4899 55A4
VIP_OUTPUT_PORT_B_SRC14_SIZE	R	32	0x0000 00A8	0x4897 55A8	0x4897 5AA8	0x4899 55A8
VIP_OUTPUT_PORT_B_SRC15_SIZE	R	32	0x0000 00AC	0x4897 55AC	0x4897 5AAC	0x4899 55AC
VIP_PORT_A_VDET_VEC	R	32	0x0000 00B0	0x4897 55B0	0x4897 5AB0	0x4899 55B0
VIP_PORT_B_VDET_VEC	R	32	0x0000 00B4	0x4897 55B4	0x4897 5AB4	0x4899 55B4
VIP_ANC_CROP_HORZ_PORT_A	RW	32	0x0000 00B8	0x4897 55B8	0x4897 5AB8	0x4899 55B8
VIP_ANC_CROP_VERT_PORT_A	RW	32	0x0000 00BC	0x4897 55BC	0x4897 5ABC	0x4899 55BC
VIP_CROP_HORZ_PORT_A	RW	32	0x0000 00C0	0x4897 55C0	0x4897 5AC0	0x4899 55C0
VIP_CROP_VERT_PORT_A	RW	32	0x0000 00C4	0x4897 55C4	0x4897 5AC4	0x4899 55C4
VIP_ANC_VIP_CROP_HORZ_PORT_B	RW	32	0x0000 00C8	0x4897 55C8	0x4897 5AC8	0x4899 55C8
VIP_ANC_VIP_CROP_VERT_PORT_B	RW	32	0x0000 00CC	0x4897 55CC	0x4897 5ACC	0x4899 55CC
VIP_CROP_HORZ_PORT_B	RW	32	0x0000 00D0	0x4897 55D0	0x4897 5AD0	0x4899 55D0
VIP_CROP_VERT_PORT_B	RW	32	0x0000 00D4	0x4897 55D4	0x4897 5AD4	0x4899 55D4
VIP_XTRA6_PORT_A	RW	32	0x0000 00D8	0x4897 55D8	0x4897 5AD8	0x4899 55D8
VIP_XTRA7_PORT_B	RW	32	0x0000 00DC	0x4897 55DC	0x4897 5ADC	0x4899 55DC
VIP_XTRA8_PORT_A	RW	32	0x0000 00E0	0x4897 55E0	0x4897 5AE0	0x4899 55E0
VIP_XTRA9_PORT_B	RW	32	0x0000 00E4	0x4897 55E4	0x4897 5AE4	0x4899 55E4

Table 9-121. VIP Parser Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	VIP2_Slice1_parser Base Address	VIP3_Slice0_parser Base Address	VIP3_Slice1_parser Base Address
VIP_MAIN	RW	32	0x0000 0000	0x4899 5A00	0x489B 5500	0x489B 5A00
VIP_PORT_A	RW	32	0x0000 0004	0x4899 5A04	0x489B 5504	0x489B 5A04
VIP_XTRA_PORT_A	RW	32	0x0000 0008	0x4899 5A08	0x489B 5508	0x489B 5A08
VIP_PORT_B	RW	32	0x0000 000C	0x4899 5A0C	0x489B 550C	0x489B 5A0C

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Table 9-121. VIP Parser Registers Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP2_Slice1_parser Base Address	VIP3_Slice0_parser Base Address	VIP3_Slice1_parser Base Address
VIP_XTRA_PORT_B	RW	32	0x0000 0010	0x4899 5A10	0x489B 5510	0x489B 5A10
VIP_FIQ_MASK	RW	32	0x0000 0014	0x4899 5A14	0x489B 5514	0x489B 5A14
VIP_FIQ_CLEAR	RW	32	0x0000 0018	0x4899 5A18	0x489B 5518	0x489B 5A18
VIP_FIQ_STATUS	R	32	0x0000 001C	0x4899 5A1C	0x489B 551C	0x489B 5A1C
VIP_OUTPUT_PORT_A_SRC_FID	R	32	0x0000 0020	0x4899 5A20	0x489B 5520	0x489B 5A20
VIP_OUTPUT_PORT_A_ENC_FID	R	32	0x0000 0024	0x4899 5A24	0x489B 5524	0x489B 5A24
VIP_OUTPUT_PORT_B_SRC_FID	R	32	0x0000 0028	0x4899 5A28	0x489B 5528	0x489B 5A28
VIP_OUTPUT_PORT_B_ENC_FID	R	32	0x0000 002C	0x4899 5A2C	0x489B 552C	0x489B 5A2C
VIP_OUTPUT_PORT_A_SRC0_SIZE	R	32	0x0000 0030	0x4899 5A30	0x489B 5530	0x489B 5A30
VIP_OUTPUT_PORT_A_SRC1_SIZE	R	32	0x0000 0034	0x4899 5A34	0x489B 5534	0x489B 5A34
VIP_OUTPUT_PORT_A_SRC2_SIZE	R	32	0x0000 0038	0x4899 5A38	0x489B 5538	0x489B 5A38
VIP_OUTPUT_PORT_A_SRC3_SIZE	R	32	0x0000 003C	0x4899 5A3C	0x489B 553C	0x489B 5A3C
VIP_OUTPUT_PORT_A_SRC4_SIZE	R	32	0x0000 0040	0x4899 5A40	0x489B 5540	0x489B 5A40
VIP_OUTPUT_PORT_A_SRC5_SIZE	R	32	0x0000 0044	0x4899 5A44	0x489B 5544	0x489B 5A44
VIP_OUTPUT_PORT_A_SRC6_SIZE	R	32	0x0000 0048	0x4899 5A48	0x489B 5548	0x489B 5A48
VIP_OUTPUT_PORT_A_SRC7_SIZE	R	32	0x0000 004C	0x4899 5A4C	0x489B 554C	0x489B 5A4C
VIP_OUTPUT_PORT_A_SRC8_SIZE	R	32	0x0000 0050	0x4899 5A50	0x489B 5550	0x489B 5A50
VIP_OUTPUT_PORT_A_SRC9_SIZE	R	32	0x0000 0054	0x4899 5A54	0x489B 5554	0x489B 5A54
VIP_OUTPUT_PORT_A_SRC10_SIZE	R	32	0x0000 0058	0x4899 5A58	0x489B 5558	0x489B 5A58
VIP_OUTPUT_PORT_A_SRC11_SIZE	R	32	0x0000 005C	0x4899 5A5C	0x489B 555C	0x489B 5A5C
VIP_OUTPUT_PORT_A_SRC12_SIZE	R	32	0x0000 0060	0x4899 5A60	0x489B 5560	0x489B 5A60
VIP_OUTPUT_PORT_A_SRC13_SIZE	R	32	0x0000 0064	0x4899 5A64	0x489B 5564	0x489B 5A64
VIP_OUTPUT_PORT_A_SRC14_SIZE	R	32	0x0000 0068	0x4899 5A68	0x489B 5568	0x489B 5A68
VIP_OUTPUT_PORT_A_SRC15_SIZE	R	32	0x0000 006C	0x4899 5A6C	0x489B 556C	0x489B 5A6C
VIP_OUTPUT_PORT_B_SRC0_SIZE	R	32	0x0000 0070	0x4899 5A70	0x489B 5570	0x489B 5A70
VIP_OUTPUT_PORT_B_SRC1_SIZE	R	32	0x0000 0074	0x4899 5A74	0x489B 5574	0x489B 5A74
VIP_OUTPUT_PORT_B_SRC2_SIZE	R	32	0x0000 0078	0x4899 5A78	0x489B 5578	0x489B 5A78
VIP_OUTPUT_PORT_B_SRC3_SIZE	R	32	0x0000 007C	0x4899 5A7C	0x489B 557C	0x489B 5A7C
VIP_OUTPUT_PORT_B_SRC4_SIZE	R	32	0x0000 0080	0x4899 5A80	0x489B 5580	0x489B 5A80
VIP_OUTPUT_PORT_B_SRC5_SIZE	R	32	0x0000 0084	0x4899 5A84	0x489B 5584	0x489B 5A84
VIP_OUTPUT_PORT_B_SRC6_SIZE	R	32	0x0000 0088	0x4899 5A88	0x489B 5588	0x489B 5A88
VIP_OUTPUT_PORT_B_SRC7_SIZE	R	32	0x0000 008C	0x4899 5A8C	0x489B 558C	0x489B 5A8C
VIP_OUTPUT_PORT_B_SRC8_SIZE	R	32	0x0000 0090	0x4899 5A90	0x489B 5590	0x489B 5A90
VIP_OUTPUT_PORT_B_SRC9_SIZE	R	32	0x0000 0094	0x4899 5A94	0x489B 5594	0x489B 5A94
VIP_OUTPUT_PORT_B_SRC10_SIZE	R	32	0x0000 0098	0x4899 5A98	0x489B 5598	0x489B 5A98
VIP_OUTPUT_PORT_B_SRC11_SIZE	R	32	0x0000 009C	0x4899 5A9C	0x489B 559C	0x489B 5A9C
VIP_OUTPUT_PORT_B_SRC12_SIZE	R	32	0x0000 00A0	0x4899 5AA0	0x489B 55A0	0x489B 5AA0
VIP_OUTPUT_PORT_B_SRC13_SIZE	R	32	0x0000 00A4	0x4899 5AA4	0x489B 55A4	0x489B 5AA4
VIP_OUTPUT_PORT_B_SRC14_SIZE	R	32	0x0000 00A8	0x4899 5AA8	0x489B 55A8	0x489B 5AA8
VIP_OUTPUT_PORT_B_SRC15_SIZE	R	32	0x0000 00AC	0x4899 5AAC	0x489B 55AC	0x489B 5AAC
VIP_PORT_A_VDET_VEC	R	32	0x0000 00B0	0x4899 5AB0	0x489B 55B0	0x489B 5AB0
VIP_PORT_B_VDET_VEC	R	32	0x0000 00B4	0x4899 5AB4	0x489B 55B4	0x489B 5AB4
VIP_ANC_CROP_HORZ_PORT_A	RW	32	0x0000 00B8	0x4899 5AB8	0x489B 55B8	0x489B 5AB8
VIP_ANC_CROP_VERT_PORT_A	RW	32	0x0000 00BC	0x4899 5ABC	0x489B 55BC	0x489B 5ABC
VIP_CROP_HORZ_PORT_A	RW	32	0x0000 00C0	0x4899 5AC0	0x489B 55C0	0x489B 5AC0
VIP_CROP_VERT_PORT_A	RW	32	0x0000 00C4	0x4899 5AC4	0x489B 55C4	0x489B 5AC4
VIP_ANC_VIP_CROP_HORZ_PORT_B	RW	32	0x0000 00C8	0x4899 5AC8	0x489B 55C8	0x489B 5AC8
VIP_ANC_VIP_CROP_VERT_PORT_B	RW	32	0x0000 00CC	0x4899 5ACC	0x489B 55CC	0x489B 5ACC
VIP_CROP_HORZ_PORT_B	RW	32	0x0000 00D0	0x4899 5AD0	0x489B 55D0	0x489B 5AD0
VIP_CROP_VERT_PORT_B	RW	32	0x0000 00D4	0x4899 5AD4	0x489B 55D4	0x489B 5AD4

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Table 9-121. VIP Parser Registers Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP2_Slice1_parser Base Address	VIP3_Slice0_parser Base Address	VIP3_Slice1_parser Base Address
VIP_XTRA6_PORT_A	RW	32	0x0000 00D8	0x4899 5AD8	0x489B 55D8	0x489B 5AD8
VIP_XTRA7_PORT_B	RW	32	0x0000 00DC	0x4899 5ADC	0x489B 55DC	0x489B 5ADC
VIP_XTRA8_PORT_A	RW	32	0x0000 00E0	0x4899 5AE0	0x489B 55E0	0x489B 5AE0
VIP_XTRA9_PORT_B	RW	32	0x0000 00E4	0x4899 5AE4	0x489B 55E4	0x489B 5AE4

9.5.3.2 VIP Parser Register Description

Table 9-122. VIP_MAIN

Address Offset	0x0000 0000		
Physical Address	0x4897 5500 0x4897 5A00 0x4899 5500 0x4899 5A00 0x489B 5500 0x489B 5A00	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	ain Configuration for VIP Parser		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLIP_ACTIVE		CLIP_BLNK		RESERVED		DATA_INTERFACE_MODE	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0
5	CLIP_ACTIVE	Discrete Sync Only 0 = Do not clip active pixels 1 = Clip Active Pixels as follows: 0xFF -andgt; 0xFE.. 0x00 -andgt; 0x01	RW	0x0
4	CLIP_BLNK	Discrete Sync Only 0 = Do not clip Blanking Data 1 = Clip Blanking Data as follows: 0xFF -andgt; 0xFE.. 0x00 -andgt; 0x01	RW	0x0
3:2	RESERVED		R	0x0
1:0	DATA_INTERFACE_MODE	00 = 24b data interface. Uses Port A settings 01 = 16b data interface. Uses Port A settings. 10 = Dual independent 8b data interfaces. Uses independent Port A and Port B settings. 11 = Undefined	RW	0x0

Table 9-123. Register Call Summary for Register VIP_MAIN

VIP Environment
- VIP Environment: [0] [1]

VIP Functional Description
- VIP Slice Processing Path Overview:
- Input Data Interface:
- Clipping: [9]

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Table 9-123. Register Call Summary for Register VIP_MAIN (continued)

VIP Register Manual

- VIP Parser Register Summary: [10] [13]

Table 9-124. VIP_PORT_A

Address Offset	0x0000 0004		
Physical Address	0x4897 5504 0x4897 5A04 0x4899 5504 0x4899 5A04 0x489B 5504 0x489B 5A04	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Configuration for Input Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANALYZER_FVH_ERR_CORRECTION_ENABLE	ANALYZER_2X4X_SRCNUM_POS	FID_SKEW_POSTCOUNT						SW_RESET	DISCRETE_BASIC_MODE	FID_SKEW_PRECOUNT						USE_ACTVID_HSYNC_N	FID_DETECT_MODE	ACTVID_POLARITY	VSYNC_POLARITY	HSYNC_POLARITY	PIXCLK_EDGE_POLARITY	FID_POLARITY	ENABLE	CLR_ASYNC_FIFO_RD	CLR_ASYNC_FIFO_WR	CTRL_CHAN_SEL	SYNC_TYPE				

Bits	Field Name	Description	Type	Reset
31	ANALYZER_FVH_ERR_CORRECTION_ENABLE	Embedded Sync Only 0 = Ignore the protection bits in the XV (fvh) codeword header. This setting is typically desired. 1 = Use the protection bits in an attempt to do error correction for the fvh control bits.	RW	0x0
30	ANALYZER_2X4X_SRCNUM_POS	Embedded Sync Only 0 = For 2x/4x mux mode, srcnum is in the least significant nibble of the XV/fvh codeword (srcnum replaces the protection bits) 1 = For 2x/4x mux mode, srcnum is in the least significant nibble of a horizontal blanking pixel value	RW	0x0
29:24	FID_SKEW_POSTCOUNT	Discrete Sync Only post count value when using vsync skew in FID determination	RW	0x0
23	SW_RESET	0 = Normal 1 = Reset Port A logic. Must be set to ?0? again by the software for the module to function.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	DISCRETE_BASIC_MODE	This register is valid for Discrete Sync mode only. 0 = Normal Discrete Mode. Hsync Style Capture operates as follows: - Captures line starting from HSYNC inactive to active condition. - VSYNC determined by sync window. - FID can be determined by VSYNC skew or captured from pin at first pixel in first line. ACTVID style capture works as follows: - Captures line during contiguous ACTVID envelope. - VSYNC is captured at the first pixel in each line. - FID is captured on first pixel of ACTVID window. 1 = Basic Discrete Mode. When using hsync with Hsync Style Capture operates as follows: - The last line of active video ends on the pixel clock cycle where VSYNC transitions from inactive to active. - FID pin value is captured on this cycle and is used for the next field. - FID detection by VSYNC skew is not allowed. ACTVID style capture works as follows: - VSYNC is expected to transition from inactive to active between ACTVID window. - This VSYNC transition allows the next line in an ACTVID envelope to be sent to a new VPDMA buffer. - FID value is determined by the FID pin value on the cycle where VSYNC transitions from inactive to active. In basic discrete mode, there is no Vertical Ancillary Data. Therefore, VPDMA descriptors should not use Ancillary Data channels.	RW	0x0
21:16	FID_SKEW_PRECOUNT	Discrete Sync Only pre count value when using vsync skew in FID determination	RW	0x0
15	USE_ACTVID_HSYNC_N	Discrete Sync Only 0 = Use HSYNC style line capture 1 = Use ACTVID style line capture	RW	0x0
14	FID_DETECT_MODE	Discrete Sync Only 0 = Take FID from pin 1 = FID is determined by VSYNC skew	RW	0x0
13	ACTVID_POLARITY	Discrete Sync Only 0 = ACTVID is active low 1 = ACTVID is active high	RW	0x0
12	VSYNC_POLARITY	Discrete Sync Only 0 = VSYNC is active low 1 = VSYNC is active high	RW	0x0
11	HSYNC_POLARITY	Discrete Sync Only 0 = HSYNC is active low 1 = HSYNC is active high	RW	0x0
10	PIXCLK_EDGE_POLARITY	0 = Rising Edge is active PIXCLK edge 1 = Falling Edge is active PIXCLK edge	RW	0x0
9	FID_POLARITY	0 = Keep FID as found 1 = Invert Determined Value of FID	RW	0x0
8	ENABLE	0 = Disable Port 1 = Enable Port	RW	0x0
7	CLR_ASYNC_FIFO_RD	0 = Normal 1 = Clear Async FIFO Read Logic	RW	0x0
6	CLR_ASYNC_FIFO_WR	0 = Normal 1 = Clear Async FIFO Write Logic	RW	0x0
5:4	CTRL_CHAN_SEL	Embedded Sync Only In 8b mode.. there is only one channel on data[7:0]. In 16b mode.. there are two channels. The Luma Channel is on data[15:8]. The Chroma Channel is on data[7:0]. In 24b mode.. there are three channels. The R channel is on data[23:16].. the G channel is on [15:8]. and the B channel is on data[7:0]. 00 = Use data[7:0] to extract control codes. 01 = Use data[15:8] to extract control codes. 10 = Use data[23:16] to extract control codes. 11 = Undefined In 16b and 24b modes.. this register is also used to select the channel from which Ancillary Data is extracted. The Ancillary Data channel must be the same as the control code channel. For 8b mode.. the anc_chan_sel_8b register is used to select the Luma or Chroma channel from which Ancillary Data is taken.	RW	0x0
3:0	SYNC_TYPE	0000 = embedded sync single 4:2:2 YUV stream 0001 = embedded sync 2x multiplexed 4:2:2 YUV stream 0010 = embedded sync 4x multiplexed 4:2:2 YUV stream 0011 = embedded sync line multiplexed 4:2:2 YUV stream 0100 = discrete sync single 4:2:2 YUV stream 0101 = embedded sync single RGB stream or single 444 YUV stream 0110 = reserved 0111 = reserved 1000 = reserved 1001 = reserved 1010 = discrete sync single 24b RGB stream	RW	0x0

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Table 9-125. Register Call Summary for Register VIP_PORT_A

VIP Functional Description

- Input Data Interface: [0] [1] [2] [3] [4]
- Interrupts: [5]
- Disable Handling: [6]
- Discrete Sync Signals: [7] [8]
- VIP Overflow Detection and Recovery: [9] [10] [11] [12] [13] [14] [15] [16]

VIP Register Manual

- VIP Parser Register Summary: [17] [20]

Table 9-126. VIP_XTRA_PORT_A

Address Offset	0x0000 0008		
Physical Address	0x4897 5508 0x4897 5A08 0x4899 5508 0x4899 5A08 0x489B 5508 0x489B 5A08	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	ore Configuration for Input Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			REPACK_SEL				SRC0_NUMPIX									RESERVED		ANC_CHAN_SEL_8B		RESERVED			SRC0_NUMLINES									

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30:28	REPACK_SEL	000 = Straight Through 001 = Cross Swap 010 = Left Center Swap 011 = Center Right Swap 100 = Right Rotate 101 = Left Rotate 110 = RAW16 to RGB565 Mapping 111 = RAW12 Swap	RW	0x0
27:16	SRC0_NUMPIX	Number of expected pixels on Source Number 0. The Port_a_src0_size interrupt will trigger if a line is encountered that differs from this pixelcount.	RW	0x0
15	RESERVED		R	0x0
14:13	ANC_CHAN_SEL_8B	In 8b mode, Vertically Ancillary Data typically resides in the Luma sites. This bit allows vertical ancillary data to be extracted from the chroma sites instead . 00 = Extract 8b Mode Vertical Ancillary Data from Luma Sites 01 = Extract 8b Mode Vertical Ancillary Data from Chroma Sites 10, 11 = Extract every single sample of vertical ancillary data. The output line is twice as wide as the other modes. For 16b and 24b inputs, ctrl_chan_sel is used to select which channel is used as a source for vertical ancillary data.	RW	0x0
12	RESERVED		R	0x0
11:0	SRC0_NUMLINES	Number of expected lines on Source Number 0. The Port_a_src0_size interrupt will trigger if a field/frame is encountered that differs from this linecount.	RW	0x0

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Table 9-127. Register Call Summary for Register VIP_XTRA_PORT_A

VIP Functional Description

- Repacker: [0] [1]
- Ancillary and Active Video Cropping: [2]
- Picture Size Interrupt: [3] [4]

VIP Register Manual

- VIP Parser Register Summary: [5] [8]

Table 9-128. VIP_PORT_B

Address Offset	0x0000 000C		
Physical Address	0x4897 550C	**Instance**	VIP1_Slice0_parser
	0x4897 5A0C		VIP1_Slice1_parser
	0x4899 550C		VIP2_Slice0_parser
	0x4899 5A0C		VIP2_Slice1_parser
	0x489B 550C		VIP3_Slice0_parser
	0x489B 5A0C		VIP3_Slice1_parser
Description	Configuration for Input Port B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANALYZER_FVH_ERR_CORRECTION_ENABLE	ANALYZER_2X4X_SRCNUM_POS	FID_SKEW_POSTCOUNT						SW_RESET	DISCRETE_BASIC_MODE	FID_SKEW_PRECOUNT						USE_ACTVID_HSYNC_N	FID_DETECT_MODE	ACTVID_POLARITY	VSYNC_POLARITY	HSYNC_POLARITY	PIXCLK_EDGE_POLARITY	FID_POLARITY	ENABLE	CLR_ASYNC_FIFO_RD	CLR_ASYNC_FIFO_WR	CTRL_CHAN_SEL	SYNC_TYPE				

Bits	Field Name	Description	Type	Reset
31	ANALYZER_FVH_ERR_CORRECTION_ENABLE	Embedded Sync Only 0 = Ignore the protection bits in the XV (fvh) codeword header. This setting is typically desired. 1 = Use the protection bits in an attempt to do error correction for the fvh control bits.	RW	0x0
30	ANALYZER_2X4X_SRCNUM_POS	Embedded Sync Only 0 = For 2x/4x mux mode, srcnum is in the least significant nibble of the XV/fvh codeword (srcnum replaces the protection bits) 1 = For 2x/4x mux mode, srcnum is in the least significant nibble of a horizontal blanking pixel value	RW	0x0
29:24	FID_SKEW_POSTCOUNT	Discrete Sync Only post count value when using vsync skew in FID determination	RW	0x0
23	SW_RESET	0 = Normal 1 = Reset Port B logic. Must be set to ?0? again by the software for the module to function.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	DISCRETE_BASIC_MODE	This register is valid for Discrete Sync mode only. 0 = Normal Discrete Mode. Hsync Style Capture operates as follows: - Captures line starting from HSYNC inactive to active condition. - VSYNC determined by sync window. - FID can be determined by VSYNC skew or captured from pin at first pixel in first line. ACTVID style capture works as follows: - Captures line during contiguous ACTVID envelope. - VSYNC is captured at the first pixel in each line. - FID is captured on first pixel of ACTVID window. 1 = Basic Discrete Mode. When using hsync with Hsync Style Capture operates as follows: - The last line of active video ends on the pixel clock cycle where VSYNC transitions from inactive to active. - FID pin value is captured on this cycle and is used for the next field. - FID detection by VSYNC skew is not allowed. ACTVID style capture works as follows: - VSYNC is expected to transition from inactive to active between ACTVID window. - This VSYNC transition allows the next line in an ACTVID envelope to be sent to a new VPDMA buffer. - FID value is determined by the FID pin value on the cycle where VSYNC transitions from inactive to active. In basic discrete mode, there is no Vertical Ancillary Data. Therefore, VPDMA descriptors should not use Ancillary Data channels.	RW	0x0
21:16	FID_SKEW_PRECOUNT	Discrete Sync Only pre count value when using vsync skew in FID determination	RW	0x0
15	USE_ACTVID_HSYNC_N	Discrete Sync Only 0 = Use HSYNC style line capture 1 = Use ACTVID style line capture	RW	0x0
14	FID_DETECT_MODE	Discrete Sync Only 0 = Take FID from pin 1 = FID is determined by VSYNC skew	RW	0x0
13	ACTVID_POLARITY	Discrete Sync Only 0 = ACTVID is active low 1 = ACTVID is active high	RW	0x0
12	VSYNC_POLARITY	Discrete Sync Only 0 = VSYNC is active low 1 = VSYNC is active high	RW	0x0
11	HSYNC_POLARITY	Discrete Sync Only 0 = HSYNC is active low 1 = HSYNC is active high	RW	0x0
10	PIXCLK_EDGE_POLARITY	0 = Rising Edge is active PIXCLK edge 1 = Falling Edge is active PIXCLK edge	RW	0x0
9	FID_POLARITY	0 = Keep FID as found 1 = Invert Determined Value of FID	RW	0x0
8	ENABLE	0 = Disable 1 = Enable	RW	0x0
7	CLR_ASYNC_FIFO_RD	0 = Normal 1 = Clear Async FIFO Read Logic	RW	0x0
6	CLR_ASYNC_FIFO_WR	0 = Normal 1 = Clear Async FIFO Write Logic	RW	0x0
5:4	CTRL_CHAN_SEL	PORT B supports on 8b mode. Always write 0 to this field. The anc_chan_sel_8b register is used to select the Luma or Chroma channel from which Ancillary Data is taken.	RW	0x0
3:0	SYNC_TYPE	0000 = embedded sync single YUV stream 0001 = embedded sync 2x multiplexed YUV stream 0010 = embedded sync 4x multiplexed YUV stream 0011 = embedded sync line multiplexed YUV stream 0100 = discrete sync single YUV stream 0101 = embedded sync single RGB stream 0110 = reserved 0111 = reserved 1000 = reserved 1001 = reserved 1010 = discrete sync single 24b RGB stream	RW	0x0

Table 9-129. Register Call Summary for Register VIP_PORT_B

VIP Functional Description

- Input Data Interface: [0] [1] [2] [3] [4]
- Interrupts: [5]
- Disable Handling: [6]
- Discrete Sync Signals: [7] [8]

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Table 9-129. Register Call Summary for Register VIP_PORT_B (continued)

VIP Register Manual • VIP Parser Register Summary: [9] [12]

Table 9-130. VIP_XTRA_PORT_B

Address Offset	0x0000 0010		
Physical Address	0x4897 5510 0x4897 5A10 0x4899 5510 0x4899 5A10 0x489B 5510 0x489B 5A10	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	ore Configuration for Input Port B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SRC0_NUMPIX												RESERVED	ANC_CHAN_SEL_8B		RESERVED	SRC0_NUMLINES												

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	SRC0_NUMPIX	Number of expected pixels on Source Number 0. The Port_b_src0_size interrupt will trigger if a line is encountered that differs from this pixelcount.	RW	0x0
15	RESERVED		R	0x0
14:13	ANC_CHAN_SEL_8B	In 8b mode, Vertically Ancillary Data typically resides in the Luma sites. This bit allows vertical ancillary data to be extracted from the chroma sites instead . 00 = Extract 8b Mode Vertical Ancillary Data from Luma Sites 01 = Extract 8b Mode Vertical Ancillary Data from Chroma Sites 10, 11 = Extract every single sample of vertical ancillary data. The output line is twice as wide as the other modes. For 16b and 24b inputs, ctrl_chan_sel is used to select which channel is used as a source for vertical ancillary data.	RW	0x0
12	RESERVED		R	0x0
11:0	SRC0_NUMLINES	Number of expected lines on Source Number 0. The Port_b_src0_size interrupt will trigger if a field/frame is encountered that differs from this linecount.	RW	0x0

Table 9-131. Register Call Summary for Register VIP_XTRA_PORT_B

VIP Functional Description • Picture Size Interrupt: [0] [1]
VIP Register Manual • VIP Parser Register Summary: [2] [5]

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Table 9-132. VIP_FIQ_MASK

Address Offset	0x0000 0014		
Physical Address	0x4897 5514 0x4897 5A14 0x4899 5514 0x4899 5A14 0x489B 5514 0x489B 5A14	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	ask Bits for ARM FIQs		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PORT_B_CFG_DISABLE_COMPLETE_MASK	PORT_A_CFG_DISABLE_COMPLETE_MASK	PORT_B_ANC_PROTOCOL_VIOLATION_MASK	PORT_B_YUV_PROTOCOL_VIOLATION_MASK	PORT_A_ANC_PROTOCOL_VIOLATION_MASK	PORT_A_YUV_PROTOCOL_VIOLATION_MASK	PORT_B_SRC0_SIZE	PORT_A_SRC0_SIZE	PORT_B_DISCONN	PORT_B_CONN	PORT_A_DISCONN	PORT_A_CONN	OUTPUT_FIFO_PRTB_ANC_OF	RESERVED	OUTPUT_FIFO_PRTB_YUV_OF	OUTPUT_FIFO_PRTA_ANC_OF	RESERVED	OUTPUT_FIFO_PRTA_YUV_OF	ASYNC_FIFO_PRTB_OF	ASYNC_FIFO_PRTA_OF	PRTB_VDET_MASK	PRTA_VDET_MASK

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	PORT_B_CFG_DISABLE_COMPLETE_MASK	Port B Cfg Disable Complete Mask	RW	0x0
20	PORT_A_CFG_DISABLE_COMPLETE_MASK	Port A Cfg Disable Complete Mask	RW	0x0
19	PORT_B_ANC_PROTOCOL_VIOLATION_MASK	Port B ANC VPI Protocol Violation Mask	RW	0x0
18	PORT_B_YUV_PROTOCOL_VIOLATION_MASK	Port B YUV VPI Protocol Violation Mask	RW	0x0
17	PORT_A_ANC_PROTOCOL_VIOLATION_MASK	Port A ANC VPI Protocol Violation Mask	RW	0x0
16	PORT_A_YUV_PROTOCOL_VIOLATION_MASK	Port A YUV VPI Protocol Violation Mask	RW	0x0
15	PORT_B_SRC0_SIZE	Video size detected on Port B does not match size programmed in xtra_port_b register	RW	0x0
14	PORT_A_SRC0_SIZE	Video size detected on Port A does not match size programmed in xtra_port_a register	RW	0x0
13	PORT_B_DISCONN	Port B Link Disconnect Srcnum 0 Mask	RW	0x0
12	PORT_B_CONN	Port B Link Connect Srcnum 0 Mask	RW	0x0
11	PORT_A_DISCONN	Port A Link Disconnect Scrnum 0 Mask	RW	0x0
10	PORT_A_CONN	Port A Link Connect Srcnum 0 Mask	RW	0x0
9	OUTPUT_FIFO_PRTB_ANC_OF	Output FIFO Port B Ancillary Overflow Mask	RW	0x0
8	RESERVED		R	0x0
7	OUTPUT_FIFO_PRTB_YUV_OF	Output FIFO Port B Luma Overflow Mask	RW	0x0
6	OUTPUT_FIFO_PRTA_ANC_OF	Output FIFO Port A Ancillary Overflow Mask	RW	0x0
5	RESERVED		R	0x0
4	OUTPUT_FIFO_PRTA_YUV_OF	Output FIFO Port A Luma Overflow Mask	RW	0x0
3	ASYNC_FIFO_PRTB_OF	Port B Async FIFO Overflow FIQ Mask	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	ASYNC_FIFO_PRTA_OF	Port A Async FIFO Overflow FIQ Mask	RW	0x0
1	PRTB_VDET_MASK	Port B Video Detect FIQ Mask	RW	0x0
0	PRTA_VDET_MASK	Port A Video Detect FIQ Mask	RW	0x0

Table 9-133. Register Call Summary for Register VIP_FIQ_MASK

VIP Functional Description
- Interrupts: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [18] [19] [20] [21] [22]

VIP Register Manual
- VIP Parser Register Summary: [23] [26]

Table 9-134. VIP_FIQ_CLEAR

Address Offset	0x0000 0018		
Physical Address	0x4897 5518 0x4897 5A18 0x4899 5518 0x4899 5A18 0x489B 5518 0x489B 5A18	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Clears bits in the FIQ Status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PORT_A_YUV_PROTOCOL_VIOLATION_CLR	PORT_A_ANC_PROTOCOL_VIOLATION_CLR	PORT_B_YUV_PROTOCOL_VIOLATION_CLR	PORT_B_ANC_PROTOCOL_VIOLATION_CLR	PORT_A_CFG_DISABLE_COMPLETE_CLR	PORT_B_CFG_DISABLE_COMPLETE_CLR	PORT_B_SRC0_SIZE_CLR	PORT_A_SRC0_SIZE_CLR	PORT_B_DISCONN_CLR	PORT_B_CONN_CLR	PORT_A_DISCONN_CLR	PORT_A_CONN_CLR	OUTPUT_FIFO_PRTB_ANC_CLR	RESERVED	OUTPUT_FIFO_PRTB_YUV_CLR	OUTPUT_FIFO_PRTA_ANC_CLR	RESERVED	OUTPUT_FIFO_PRTA_YUV_CLR	ASYNC_FIFO_PRTB_CLR	ASYNC_FIFO_PRTA_CLR	PRTB_VDET_CLR	PRTA_VDET_CLR

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	PORT_A_YUV_PROTOCOL_VIOLATION_CLR	Write 1 followed by 0 to Clear Port B Cfg Disable Complete FIQ	RW	0x0
20	PORT_A_ANC_PROTOCOL_VIOLATION_CLR	Write 1 followed by 0 to Clear Port A Cfg Disable Complete FIQ	RW	0x0
19	PORT_B_YUV_PROTOCOL_VIOLATION_CLR	Write 1 followed by 0 to Clear Port B ANC VPI Protocol Violation FIQ	RW	0x0
18	PORT_B_ANC_PROTOCOL_VIOLATION_CLR	Write 1 followed by 0 to Clear Port B YUV VPI Protocol Violation FIQ	RW	0x0
17	PORT_A_CFG_DISABLE_COMPLETE_CLR	Write 1 followed by 0 to Clear Port A ANC VPI Protocol Violation FIQ	RW	0x0
16	PORT_B_CFG_DISABLE_COMPLETE_CLR	Write 1 followed by 0 to Clear Port A YUV VPI Protocol Violation FIQ	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	PORT_B_SRC0_SIZE_CLR	Write 1 followed by 0 to Clear Port B Src0 Size FIQ	RW	0x0
14	PORT_A_SRC0_SIZE_CLR	Write 1 followed by 0 to Clear Port A Src0 Size FIQ	RW	0x0
13	PORT_B_DISCONN_CLR	Write 1 followed by 0 to Clear Port B Link Disconnect FIQ	RW	0x0
12	PORT_B_CONN_CLR	Write 1 followed by 0 to Clear Port B Link Connect FIQ	RW	0x0
11	PORT_A_DISCONN_CLR	Write 1 followed by 0 to Clear Port A Link Disconnect FIQ	RW	0x0
10	PORT_A_CONN_CLR	Write 1 followed by 0 to Clear Port A Link Connect FIQ	RW	0x0
9	OUTPUT_FIFO_PRTB_ANC_CLR	Write 1 followed by 0 to Clear Output FIFO Port B Ancillary Overflow FIQ	RW	0x0
8	RESERVED		R	0x0
7	OUTPUT_FIFO_PRTB_YUV_CLR	Write 1 followed by 0 to Clear Output FIFO Port B Luma Overflow FIQ	RW	0x0
6	OUTPUT_FIFO_PRTA_ANC_CLR	Write 1 followed by 0 to Clear Output FIFO Port A Ancillary Overflow FIQ	RW	0x0
5	RESERVED		R	0x0
4	OUTPUT_FIFO_PRTA_YUV_CLR	Write 1 followed by 0 to Clear Output FIFO Port A Luma Overflow FIQ	RW	0x0
3	ASYNC_FIFO_PRTB_CLR	Write 1 followed by 0 to Clear Async FIFO Port B Overflow FIQ	RW	0x0
2	ASYNC_FIFO_PRTA_CLR	Write 1 followed by 0 to Clear Async FIFO Port A Overflow FIQ	RW	0x0
1	PRTB_VDET_CLR	Write 1 followed by 0 to Clear Video Detect FIQ for Port B	RW	0x0
0	PRTA_VDET_CLR	Write 1 followed by 0 to Clear Video Detect FIQ for Port A	RW	0x0

Table 9-135. Register Call Summary for Register VIP_FIQ_CLEAR

VIP Functional Description
- Interrupts: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

Table 9-136. VIP_FIQ_STATUS

Address Offset	0x0000 001C		
Physical Address	0x4897 551C 0x4897 5A1C 0x4899 551C 0x4899 5A1C 0x489B 551C 0x489B 5A1C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	FIQ Status values		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PORT_B_CFG_DISABLE_COMPLETE_CLR	PORT_A_CFG_DISABLE_COMPLETE	PORT_B_ANC_PROTOCOL_VIOLATION	PORT_B_YUV_PROTOCOL_VIOLATION	PORT_A_ANC_PROTOCOL_VIOLATION	PORT_A_YUV_PROTOCOL_VIOLATION	PORT_B_SRC0_SIZE_STATUS	PORT_A_SRC0_SIZE_STATUS	PORT_B_DISCONN_STATUS	PORT_B_CONN_STATUS	PORT_A_DISCONN_STATUS	PORT_A_CONN_STATUS	OUTPUT_FIFO_PRTB_ANC_STATUS	OUTPUT_FIFO_PRTB_CHROMA_STATUS	OUTPUT_FIFO_PRTB_LUMA_STATUS	OUTPUT_FIFO_PRTA_ANC_STATUS	OUTPUT_FIFO_PRTA_CHROMA_STATUS	OUTPUT_FIFO_PRTA_LUMA_STATUS	ASYNC_FIFO_PRTB_STATUS	ASYNC_FIFO_PRTA_STATUS	PRTB_VDET_STATUS	PRTA_VDET_STATUS

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21	PORT_B_CFG_DISABLE_COMPLETE_CLR	Port B Cfg Disable Complete FIQ	R	0x0
20	PORT_A_CFG_DISABLE_COMPLETE	Port A Cfg Disable Complete FIQ	R	0x0
19	PORT_B_ANC_PROTOCOL_VIOLATION	Port B ANC VPI Protocol Violation FIQ	R	0x0
18	PORT_B_YUV_PROTOCOL_VIOLATION	Port B YUV VPI Protocol Violation FIQ	R	0x0
17	PORT_A_ANC_PROTOCOL_VIOLATION	Port A ANC VPI Protocol Violation FIQ	R	0x0
16	PORT_A_YUV_PROTOCOL_VIOLATION	Port A YUV VPI Protocol Violation FIQ	R	0x0
15	PORT_B_SRC0_SIZE_STATUS	Port B Source 0 Size FIQ	R	0x0
14	PORT_A_SRC0_SIZE_STATUS	Port A Source 0 Size FIQ	R	0x0
13	PORT_B_DISCONN_STATUS	Port B Disconnect FIQ	R	0x0
12	PORT_B_CONN_STATUS	Port B Connect FIQ	R	0x0
11	PORT_A_DISCONN_STATUS	Port A Disconnect FIQ	R	0x0
10	PORT_A_CONN_STATUS	Port A Connect FIQ	R	0x0
9	OUTPUT_FIFO_PRTB_ANC_STATUS	Output FIFO Port B Ancillary Overflow Status	R	0x0
8	OUTPUT_FIFO_PRTB_CHROMA_STATUS	Output FIFO Port B Chroma Overflow Status	R	0x0
7	OUTPUT_FIFO_PRTB_LUMA_STATUS	Output FIFO Port B Luma Overflow Status	R	0x0
6	OUTPUT_FIFO_PRTA_ANC_STATUS	Output FIFO Port A Ancillary Overflow Status	R	0x0
5	OUTPUT_FIFO_PRTA_CHROMA_STATUS	Output FIFO Port A Chroma Overflow Status	R	0x0
4	OUTPUT_FIFO_PRTA_LUMA_STATUS	Output FIFO Port A Luma Overflow Status	R	0x0
3	ASYNC_FIFO_PRTB_STATUS	Async FIFO Port B Overflow Status	R	0x0
2	ASYNC_FIFO_PRTA_STATUS	Async FIFO Port A Overflow Status	R	0x0
1	PRTB_VDET_STATUS	VDET Status for Port B	R	0x0
0	PRTA_VDET_STATUS	VDET Status for Port A	R	0x0

Table 9-137. Register Call Summary for Register VIP_FIQ_STATUS

VIP Functional Description
- Interrupts: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [18] [19] [20] [21] [22]
- VIP Overflow Detection and Recovery: [23]

VIP Register Manual
- VIP Parser Register Summary: [24] [27]

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Table 9-138. VIP_OUTPUT_PORT_A_SRC_FID

Address Offset	0x0000 0020		
Physical Address	0x4897 5520 0x4897 5A20 0x4899 5520 0x4899 5A20 0x489B 5520 0x489B 5A20	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Current and Previous Output Port A Source FID values		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTA_SRC15_CURR_SOURCE_FID	PRTA_SRC15_PREV_SOURCE_FID	PRTA_SRC14_CURR_SOURCE_FID	PRTA_SRC14_PREV_SOURCE_FID	PRTA_SRC13_CURR_SOURCE_FID	PRTA_SRC13_PREV_SOURCE_FID	PRTA_SRC12_CURR_SOURCE_FID	PRTA_SRC12_PREV_SOURCE_FID	PRTA_SRC11_CURR_SOURCE_FID	PRTA_SRC11_PREV_SOURCE_FID	PRTA_SRC10_CURR_SOURCE_FID	PRTA_SRC10_PREV_SOURCE_FID	PRTA_SRC9_CURR_SOURCE_FID	PRTA_SRC9_PREV_SOURCE_FID	PRTA_SRC8_CURR_SOURCE_FID	PRTA_SRC8_PREV_SOURCE_FID	PRTA_SRC7_CURR_SOURCE_FID	PRTA_SRC7_PREV_SOURCE_FID	PRTA_SRC6_CURR_SOURCE_FID	PRTA_SRC6_PREV_SOURCE_FID	PRTA_SRC5_CURR_SOURCE_FID	PRTA_SRC5_PREV_SOURCE_FID	PRTA_SRC4_CURR_SOURCE_FID	PRTA_SRC4_PREV_SOURCE_FID	PRTA_SRC3_CURR_SOURCE_FID	PRTA_SRC3_PREV_SOURCE_FID	PRTA_SRC2_CURR_SOURCE_FID	PRTA_SRC2_PREV_SOURCE_FID	PRTA_SRC1_CURR_SOURCE_FID	PRTA_SRC1_PREV_SOURCE_FID	PRTA_SRC0_CURR_SOURCE_FID	PRTA_SRC0_PREV_SOURCE_FID

Bits	Field Name	Description	Type	Reset
31	PRTA_SRC15_CURR_SOURCE_FID	For Source ID 15 from Port A. Source Field ID for Current Field	R	0x0
30	PRTA_SRC15_PREV_SOURCE_FID	For Source ID 15 from Port A. Source Field ID for Previous Field	R	0x0
29	PRTA_SRC14_CURR_SOURCE_FID	For Source ID 14 from Port A. Source Field ID for Current Field	R	0x0
28	PRTA_SRC14_PREV_SOURCE_FID	For Source ID 14 from Port A. Source Field ID for Previous Field	R	0x0
27	PRTA_SRC13_CURR_SOURCE_FID	For Source ID 13 from Port A. Source Field ID for Current Field	R	0x0
26	PRTA_SRC13_PREV_SOURCE_FID	For Source ID 13 from Port A. Source Field ID for Previous Field	R	0x0
25	PRTA_SRC12_CURR_SOURCE_FID	For Source ID 12 from Port A. Source Field ID for Current Field	R	0x0
24	PRTA_SRC12_PREV_SOURCE_FID	For Source ID 12 from Port A. Source Field ID for Previous Field	R	0x0
23	PRTA_SRC11_CURR_SOURCE_FID	For Source ID 11 from Port A. Source Field ID for Current Field	R	0x0
22	PRTA_SRC11_PREV_SOURCE_FID	For Source ID 11 from Port A. Source Field ID for Previous Field	R	0x0
21	PRTA_SRC10_CURR_SOURCE_FID	For Source ID 10 from Port A. Source Field ID for Current Field	R	0x0
20	PRTA_SRC10_PREV_SOURCE_FID	For Source ID 10 from Port A. Source Field ID for Previous Field	R	0x0
19	PRTA_SRC9_CURR_SOURCE_FID	For Source ID 9 from Port A. Source Field ID for Current Field	R	0x0
18	PRTA_SRC9_PREV_SOURCE_FID	For Source ID 9 from Port A. Source Field ID for Previous Field	R	0x0
17	PRTA_SRC8_CURR_SOURCE_FID	For Source ID 8 from Port A. Source Field ID for Current Field	R	0x0

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Bits	Field Name	Description	Type	Reset
16	PRTA_SRC8_PREV_SOURCE_FID	For Source ID 8 from Port A. Source Field ID for Previous Field	R	0x0
15	PRTA_SRC7_CURR_SOURCE_FID	For Source ID 7 from Port A. Source Field ID for Current Field	R	0x0
14	PRTA_SRC7_PREV_SOURCE_FID	For Source ID 7 from Port A. Source Field ID for Previous Field	R	0x0
13	PRTA_SRC6_CURR_SOURCE_FID	For Source ID 6 from Port A. Source Field ID for Current Field	R	0x0
12	PRTA_SRC6_PREV_SOURCE_FID	For Source ID 6 from Port A. Source Field ID for Previous Field	R	0x0
11	PRTA_SRC5_CURR_SOURCE_FID	For Source ID 5 from Port A. Source Field ID for Current Field	R	0x0
10	PRTA_SRC5_PREV_SOURCE_FID	For Source ID 5 from Port A. Source Field ID for Previous Field	R	0x0
9	PRTA_SRC4_CURR_SOURCE_FID	For Source ID 4 from Port A. Source Field ID for Current Field	R	0x0
8	PRTA_SRC4_PREV_SOURCE_FID	For Source ID 4 from Port A. Source Field ID for Previous Field	R	0x0
7	PRTA_SRC3_CURR_SOURCE_FID	For Source ID 3 from Port A. Source Field ID for Current Field	R	0x0
6	PRTA_SRC3_PREV_SOURCE_FID	For Source ID 3 from Port A. Source Field ID for Previous Field	R	0x0
5	PRTA_SRC2_CURR_SOURCE_FID	For Source ID 2 from Port A. Source Field ID for Current Field	R	0x0
4	PRTA_SRC2_PREV_SOURCE_FID	For Source ID 2 from Port A. Source Field ID for Previous Field	R	0x0
3	PRTA_SRC1_CURR_SOURCE_FID	For Source ID 1 from Port A. Source Field ID for Current Field	R	0x0
2	PRTA_SRC1_PREV_SOURCE_FID	For Source ID 1 from Port A. Source Field ID for Previous Field	R	0x0
1	PRTA_SRC0_CURR_SOURCE_FID	For Source ID 0 from Port A. Source Field ID for Current Field	R	0x0
0	PRTA_SRC0_PREV_SOURCE_FID	For Source ID 0 from Port A. Source Field ID for Previous Field	R	0x0

Table 9-139. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC_FID

VIP Functional Description • Source Multiplexing: [0]
VIP Register Manual • VIP Parser Register Summary: [1] [4]

Table 9-140. VIP_OUTPUT_PORT_A_ENC_FID

Address Offset	0x0000 0024		
Physical Address	0x4897 5524 0x4897 5A24 0x4899 5524 0x4899 5A24 0x489B 5524 0x489B 5A24	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Current and Previous Output Port A Encoder FID values		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTA_SRC15_CURR_ENC_FID	PRTA_SRC15_PREV_ENC_FID	PRTA_SRC14_CURR_ENC_FID	PRTA_SRC14_PREV_ENC_FID	PRTA_SRC13_CURR_ENC_FID	PRTA_SRC13_PREV_ENC_FID	PRTA_SRC12_CURR_ENC_FID	PRTA_SRC12_PREV_ENC_FID	PRTA_SRC11_CURR_ENC_FID	PRTA_SRC11_PREV_ENC_FID	PRTA_SRC10_CURR_ENC_FID	PRTA_SRC10_PREV_ENC_FID	PRTA_SRC9_CURR_ENC_FID	PRTA_SRC9_PREV_ENC_FID	PRTA_SRC8_CURR_ENC_FID	PRTA_SRC8_PREV_ENC_FID	PRTA_SRC7_CURR_ENC_FID	PRTA_SRC7_PREV_ENC_FID	PRTA_SRC6_CURR_ENC_FID	PRTA_SRC6_PREV_ENC_FID	PRTA_SRC5_CURR_ENC_FID	PRTA_SRC5_PREV_ENC_FID	PRTA_SRC4_CURR_ENC_FID	PRTA_SRC4_PREV_ENC_FID	PRTA_SRC3_CURR_ENC_FID	PRTA_SRC3_PREV_ENC_FID	PRTA_SRC2_CURR_ENC_FID	PRTA_SRC2_PREV_ENC_FID	PRTA_SRC1_CURR_ENC_FID	PRTA_SRC1_PREV_ENC_FID	PRTA_SRC0_CURR_ENC_FID	PRTA_SRC0_PREV_ENC_FID

Bits	Field Name	Description	Type	Reset
31	PRTA_SRC15_CURR_ENC_FID	For Source ID 15 from Port A. Encoder Field ID for Current Field	R	0x0
30	PRTA_SRC15_PREV_ENC_FID	For Source ID 15 from Port A. Encoder Field ID for Previous Field	R	0x0
29	PRTA_SRC14_CURR_ENC_FID	For Source ID 14 from Port A. Encoder Field ID for Current Field	R	0x0
28	PRTA_SRC14_PREV_ENC_FID	For Source ID 14 from Port A. Encoder Field ID for Previous Field	R	0x0
27	PRTA_SRC13_CURR_ENC_FID	For Source ID 13 from Port A. Encoder Field ID for Current Field	R	0x0
26	PRTA_SRC13_PREV_ENC_FID	For Source ID 13 from Port A. Encoder Field ID for Previous Field	R	0x0
25	PRTA_SRC12_CURR_ENC_FID	For Source ID 12 from Port A. Encoder Field ID for Current Field	R	0x0
24	PRTA_SRC12_PREV_ENC_FID	For Source ID 12 from Port A. Encoder Field ID for Previous Field	R	0x0
23	PRTA_SRC11_CURR_ENC_FID	For Source ID 11 from Port A. Encoder Field ID for Current Field	R	0x0
22	PRTA_SRC11_PREV_ENC_FID	For Source ID 11 from Port A. Encoder Field ID for Previous Field	R	0x0
21	PRTA_SRC10_CURR_ENC_FID	For Source ID 10 from Port A. Encoder Field ID for Current Field	R	0x0
20	PRTA_SRC10_PREV_ENC_FID	For Source ID 10 from Port A. Encoder Field ID for Previous Field	R	0x0
19	PRTA_SRC9_CURR_ENC_FID	For Source ID 9 from Port A. Encoder Field ID for Current Field	R	0x0
18	PRTA_SRC9_PREV_ENC_FID	For Source ID 9 from Port A. Encoder Field ID for Previous Field	R	0x0
17	PRTA_SRC8_CURR_ENC_FID	For Source ID 8 from Port A. Encoder Field ID for Current Field	R	0x0
16	PRTA_SRC8_PREV_ENC_FID	For Source ID 8 from Port A. Encoder Field ID for Previous Field	R	0x0
15	PRTA_SRC7_CURR_ENC_FID	For Source ID 7 from Port A. Encoder Field ID for Current Field	R	0x0
14	PRTA_SRC7_PREV_ENC_FID	For Source ID 7 from Port A. Encoder Field ID for Previous Field	R	0x0
13	PRTA_SRC6_CURR_ENC_FID	For Source ID 6 from Port A. Encoder Field ID for Current Field	R	0x0
12	PRTA_SRC6_PREV_ENC_FID	For Source ID 6 from Port A. Encoder Field ID for Previous Field	R	0x0
11	PRTA_SRC5_CURR_ENC_FID	For Source ID 5 from Port A. Encoder Field ID for Current Field	R	0x0
10	PRTA_SRC5_PREV_ENC_FID	For Source ID 5 from Port A. Encoder Field ID for Previous Field	R	0x0

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Bits	Field Name	Description	Type	Reset
9	PRTA_SRC4_CURR_ENC_FID	For Source ID 4 from Port A. Encoder Field ID for Current Field	R	0x0
8	PRTA_SRC4_PREV_ENC_FID	For Source ID 4 from Port A. Encoder Field ID for Previous Field	R	0x0
7	PRTA_SRC3_CURR_ENC_FID	For Source ID 3 from Port A. Encoder Field ID for Current Field	R	0x0
6	PRTA_SRC3_PREV_ENC_FID	For Source ID 3 from Port A. Encoder Field ID for Previous Field	R	0x0
5	PRTA_SRC2_CURR_ENC_FID	For Source ID 2 from Port A. Encoder Field ID for Current Field	R	0x0
4	PRTA_SRC2_PREV_ENC_FID	For Source ID 2 from Port A. Encoder Field ID for Previous Field	R	0x0
3	PRTA_SRC1_CURR_ENC_FID	For Source ID 1 from Port A. Encoder Field ID for Current Field	R	0x0
2	PRTA_SRC1_PREV_ENC_FID	For Source ID 1 from Port A. Encoder Field ID for Previous Field	R	0x0
1	PRTA_SRC0_CURR_ENC_FID	For Source ID 0 from Port A. Encoder Field ID for Current Field	R	0x0
0	PRTA_SRC0_PREV_ENC_FID	For Source ID 0 from Port A. Encoder Field ID for Previous Field	R	0x0

Table 9-141. Register Call Summary for Register VIP_OUTPUT_PORT_A_ENC_FID

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

Table 9-142. VIP_OUTPUT_PORT_B_SRC_FID

Address Offset	0x0000 0028		
Physical Address	0x4897 5528 0x4897 5A28 0x4899 5528 0x4899 5A28 0x489B 5528 0x489B 5A28	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Current and Previous Output Port B Source FID values		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTB_SRC15_CURR_SOURCE_FID	PRTB_SRC15_PREV_SOURCE_FID	PRTB_SRC14_CURR_SOURCE_FID	PRTB_SRC14_PREV_SOURCE_FID	PRTB_SRC13_CURR_SOURCE_FID	PRTB_SRC13_PREV_SOURCE_FID	PRTB_SRC12_CURR_SOURCE_FID	PRTB_SRC12_PREV_SOURCE_FID	PRTB_SRC11_CURR_SOURCE_FID	PRTB_SRC11_PREV_SOURCE_FID	PRTB_SRC10_CURR_SOURCE_FID	PRTB_SRC10_PREV_SOURCE_FID	PRTB_SRC9_CURR_SOURCE_FID	PRTB_SRC9_PREV_SOURCE_FID	PRTB_SRC8_CURR_SOURCE_FID	PRTB_SRC8_PREV_SOURCE_FID	PRTB_SRC7_CURR_SOURCE_FID	PRTB_SRC7_PREV_SOURCE_FID	PRTB_SRC6_CURR_SOURCE_FID	PRTB_SRC6_PREV_SOURCE_FID	PRTB_SRC5_CURR_SOURCE_FID	PRTB_SRC5_PREV_SOURCE_FID	PRTB_SRC4_CURR_SOURCE_FID	PRTB_SRC4_PREV_SOURCE_FID	PRTB_SRC3_CURR_SOURCE_FID	PRTB_SRC3_PREV_SOURCE_FID	PRTB_SRC2_CURR_SOURCE_FID	PRTB_SRC2_PREV_SOURCE_FID	PRTB_SRC1_CURR_SOURCE_FID	PRTB_SRC1_PREV_SOURCE_FID	PRTB_SRC0_CURR_SOURCE_FID	PRTB_SRC0_PREV_SOURCE_FID

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Bits	Field Name	Description	Type	Reset
31	PRTB_SRC15_CURR_SOURCE_FID	For Source ID 15 from Port B. Source Field ID for Current Field	R	0x0
30	PRTB_SRC15_PREV_SOURCE_FID	For Source ID 15 from Port B. Source Field ID for Previous Field	R	0x0
29	PRTB_SRC14_CURR_SOURCE_FID	For Source ID 14 from Port B. Source Field ID for Current Field	R	0x0
28	PRTB_SRC14_PREV_SOURCE_FID	For Source ID 14 from Port B. Source Field ID for Previous Field	R	0x0
27	PRTB_SRC13_CURR_SOURCE_FID	For Source ID 13 from Port B. Source Field ID for Current Field	R	0x0
26	PRTB_SRC13_PREV_SOURCE_FID	For Source ID 13 from Port B. Source Field ID for Previous Field	R	0x0
25	PRTB_SRC12_CURR_SOURCE_FID	For Source ID 12 from Port B. Source Field ID for Current Field	R	0x0
24	PRTB_SRC12_PREV_SOURCE_FID	For Source ID 12 from Port B. Source Field ID for Previous Field	R	0x0
23	PRTB_SRC11_CURR_SOURCE_FID	For Source ID 11 from Port B. Source Field ID for Current Field	R	0x0
22	PRTB_SRC11_PREV_SOURCE_FID	For Source ID 11. from Port B Source Field ID for Previous Field	R	0x0
21	PRTB_SRC10_CURR_SOURCE_FID	For Source ID 10 from Port B. Source Field ID for Current Field	R	0x0
20	PRTB_SRC10_PREV_SOURCE_FID	For Source ID 10 from Port B. Source Field ID for Previous Field	R	0x0
19	PRTB_SRC9_CURR_SOURCE_FID	For Source ID 9 from Port B. Source Field ID for Current Field	R	0x0
18	PRTB_SRC9_PREV_SOURCE_FID	For Source ID 9 from Port B. Source Field ID for Previous Field	R	0x0
17	PRTB_SRC8_CURR_SOURCE_FID	For Source ID 8 from Port B. Source Field ID for Current Field	R	0x0
16	PRTB_SRC8_PREV_SOURCE_FID	For Source ID 8 from Port B. Source Field ID for Previous Field	R	0x0
15	PRTB_SRC7_CURR_SOURCE_FID	For Source ID 7 from Port B. Source Field ID for Current Field	R	0x0
14	PRTB_SRC7_PREV_SOURCE_FID	For Source ID 7 from Port B. Source Field ID for Previous Field	R	0x0
13	PRTB_SRC6_CURR_SOURCE_FID	For Source ID 6 from Port B. Source Field ID for Current Field	R	0x0
12	PRTB_SRC6_PREV_SOURCE_FID	For Source ID 6 from Port B. Source Field ID for Previous Field	R	0x0
11	PRTB_SRC5_CURR_SOURCE_FID	For Source ID 5 from Port B. Source Field ID for Current Field	R	0x0
10	PRTB_SRC5_PREV_SOURCE_FID	For Source ID 5 from Port B. Source Field ID for Previous Field	R	0x0
9	PRTB_SRC4_CURR_SOURCE_FID	For Source ID 4 from Port B. Source Field ID for Current Field	R	0x0
8	PRTB_SRC4_PREV_SOURCE_FID	For Source ID 4 from Port B. Source Field ID for Previous Field	R	0x0
7	PRTB_SRC3_CURR_SOURCE_FID	For Source ID 3 from Port B. Source Field ID for Current Field	R	0x0
6	PRTB_SRC3_PREV_SOURCE_FID	For Source ID 3 from Port B. Source Field ID for Previous Field	R	0x0
5	PRTB_SRC2_CURR_SOURCE_FID	For Source ID 2 from Port B. Source Field ID for Current Field	R	0x0
4	PRTB_SRC2_PREV_SOURCE_FID	For Source ID 2 from Port B. Source Field ID for Previous Field	R	0x0
3	PRTB_SRC1_CURR_SOURCE_FID	For Source ID 1 from Port B. Source Field ID for Current Field	R	0x0

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Bits	Field Name	Description	Type	Reset
2	PRTB_SRC1_PREV_SOURCE_FID	For Source ID 1 from Port B. Source Field ID for Previous Field	R	0x0
1	PRTB_SRC0_CURR_SOURCE_FID	For Source ID 0 from Port B. Source Field ID for Current Field	R	0x0
0	PRTB_SRC0_PREV_SOURCE_FID	For Source ID 0 from Port B. Source Field ID for Previous Field	R	0x0

Table 9-143. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC_FID

VIP Functional Description
- Source Multiplexing: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

Table 9-144. VIP_OUTPUT_PORT_B_ENC_FID

Address Offset	0x0000 002C		
Physical Address	0x4897 552C 0x4897 5A2C 0x4899 552C 0x4899 5A2C 0x489B 552C 0x489B 5A2C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Current and Previous Output Port B Encoder FID values		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTB_SRC15_CURR_ENC_FID	PRTB_SRC15_PREV_ENC_FID	PRTB_SRC14_CURR_ENC_FID	PRTB_SRC14_PREV_ENC_FID	PRTB_SRC13_CURR_ENC_FID	PRTB_SRC13_PREV_ENC_FID	PRTB_SRC12_CURR_ENC_FID	PRTB_SRC12_PREV_ENC_FID	PRTB_SRC11_CURR_ENC_FID	PRTB_SRC11_PREV_ENC_FID	PRTB_SRC10_CURR_ENC_FID	PRTB_SRC10_PREV_ENC_FID	PRTB_SRC9_CURR_ENC_FID	PRTB_SRC9_PREV_ENC_FID	PRTB_SRC8_CURR_ENC_FID	PRTB_SRC8_PREV_ENC_FID	PRTB_SRC7_CURR_ENC_FID	PRTB_SRC7_PREV_ENC_FID	PRTB_SRC6_CURR_ENC_FID	PRTB_SRC6_PREV_ENC_FID	PRTB_SRC5_CURR_ENC_FID	PRTB_SRC5_PREV_ENC_FID	PRTB_SRC4_CURR_ENC_FID	PRTB_SRC4_PREV_ENC_FID	PRTB_SRC3_CURR_ENC_FID	PRTB_SRC3_PREV_ENC_FID	PRTB_SRC2_CURR_ENC_FID	PRTB_SRC2_PREV_ENC_FID	PRTB_SRC1_CURR_ENC_FID	PRTB_SRC1_PREV_ENC_FID	PRTB_SRC0_CURR_ENC_FID	PRTB_SRC0_PREV_ENC_FID

Bits	Field Name	Description	Type	Reset
31	PRTB_SRC15_CURR_ENC_FID	For Source ID 15 from Port B. Encoder Field ID for Current Field	R	0x0
30	PRTB_SRC15_PREV_ENC_FID	For Source ID 15 from Port B. Encoder Field ID for Previous Field	R	0x0
29	PRTB_SRC14_CURR_ENC_FID	For Source ID 14 from Port B. Encoder Field ID for Current Field	R	0x0
28	PRTB_SRC14_PREV_ENC_FID	For Source ID 14 from Port B. Encoder Field ID for Previous Field	R	0x0
27	PRTB_SRC13_CURR_ENC_FID	For Source ID 13 from Port B. Encoder Field ID for Current Field	R	0x0
26	PRTB_SRC13_PREV_ENC_FID	For Source ID 13 from Port B. Encoder Field ID for Previous Field	R	0x0
25	PRTB_SRC12_CURR_ENC_FID	For Source ID 12 from Port B. Encoder Field ID for Current Field	R	0x0
24	PRTB_SRC12_PREV_ENC_FID	For Source ID 12 from Port B. Encoder Field ID for Previous Field	R	0x0

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Bits	Field Name	Description	Type	Reset
23	PRTB_SRC11_CURR_ENC_FID	For Source ID 11 from Port B. Encoder Field ID for Current Field	R	0x0
22	PRTB_SRC11_PREV_ENC_FID	For Source ID 11 from Port B. Encoder Field ID for Previous Field	R	0x0
21	PRTB_SRC10_CURR_ENC_FID	For Source ID 10 from Port B. Encoder Field ID for Current Field	R	0x0
20	PRTB_SRC10_PREV_ENC_FID	For Source ID 10 from Port B. Encoder Field ID for Previous Field	R	0x0
19	PRTB_SRC9_CURR_ENC_FID	For Source ID 9 from Port B. Encoder Field ID for Current Field	R	0x0
18	PRTB_SRC9_PREV_ENC_FID	For Source ID 9 from Port B. Encoder Field ID for Previous Field	R	0x0
17	PRTB_SRC8_CURR_ENC_FID	For Source ID 8 from Port B. Encoder Field ID for Current Field	R	0x0
16	PRTB_SRC8_PREV_ENC_FID	For Source ID 8 from Port B. Encoder Field ID for Previous Field	R	0x0
15	PRTB_SRC7_CURR_ENC_FID	For Source ID 7 from Port B. Encoder Field ID for Current Field	R	0x0
14	PRTB_SRC7_PREV_ENC_FID	For Source ID 7 from Port B. Encoder Field ID for Previous Field	R	0x0
13	PRTB_SRC6_CURR_ENC_FID	For Source ID 6 from Port B. Encoder Field ID for Current Field	R	0x0
12	PRTB_SRC6_PREV_ENC_FID	For Source ID 6 from Port B. Encoder Field ID for Previous Field	R	0x0
11	PRTB_SRC5_CURR_ENC_FID	For Source ID 5 from Port B. Encoder Field ID for Current Field	R	0x0
10	PRTB_SRC5_PREV_ENC_FID	For Source ID 5 from Port B. Encoder Field ID for Previous Field	R	0x0
9	PRTB_SRC4_CURR_ENC_FID	For Source ID 4 from Port B. Encoder Field ID for Current Field	R	0x0
8	PRTB_SRC4_PREV_ENC_FID	For Source ID 4 from Port B. Encoder Field ID for Previous Field	R	0x0
7	PRTB_SRC3_CURR_ENC_FID	For Source ID 3 from Port B. Encoder Field ID for Current Field	R	0x0
6	PRTB_SRC3_PREV_ENC_FID	For Source ID 3 from Port B. Encoder Field ID for Previous Field	R	0x0
5	PRTB_SRC2_CURR_ENC_FID	For Source ID 2 from Port B. Encoder Field ID for Current Field	R	0x0
4	PRTB_SRC2_PREV_ENC_FID	For Source ID 2 from Port B. Encoder Field ID for Previous Field	R	0x0
3	PRTB_SRC1_CURR_ENC_FID	For Source ID 1 from Port B. Encoder Field ID for Current Field	R	0x0
2	PRTB_SRC1_PREV_ENC_FID	For Source ID 1 from Port B. Encoder Field ID for Previous Field	R	0x0
1	PRTB_SRC0_CURR_ENC_FID	For Source ID 0 from Port B. Encoder Field ID for Current Field	R	0x0
0	PRTB_SRC0_PREV_ENC_FID	For Source ID 0 from Port B. Encoder Field ID for Previous Field	R	0x0

Table 9-145. Register Call Summary for Register VIP_OUTPUT_PORT_B_ENC_FID

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

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Table 9-146. VIP_OUTPUT_PORT_A_SRC0_SIZE

Address Offset	0x0000 0030		
Physical Address	0x4897 5530 0x4897 5A30 0x4899 5530 0x4899 5A30 0x489B 5530 0x489B 5A30	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC0_WIDTH								RESERVED								PRTA_SRC0_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC0_WIDTH	On Port A. Width of Source ID 0	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC0_HEIGHT	On Port A. Height of Source ID 0	R	0x0

Table 9-147. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC0_SIZE

VIP Functional Description
- Source Multiplexing: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

Table 9-148. VIP_OUTPUT_PORT_A_SRC1_SIZE

Address Offset	0x0000 0034		
Physical Address	0x4897 5534 0x4897 5A34 0x4899 5534 0x4899 5A34 0x489B 5534 0x489B 5A34	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC1_WIDTH								RESERVED								PRTA_SRC1_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC1_WIDTH	On Port A. Width of Source ID 1	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC1_HEIGHT	On Port A. Height of Source ID 1	R	0x0

Table 9-149. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC1_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-150. VIP_OUTPUT_PORT_A_SRC2_SIZE

Address Offset	0x0000 0038		
Physical Address	0x4897 5538 0x4897 5A38 0x4899 5538 0x4899 5A38 0x489B 5538 0x489B 5A38	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC2_WIDTH								RESERVED								PRTA_SRC2_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC2_WIDTH	On Port A. Width of Source ID 2	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC2_HEIGHT	On Port A. Height of Source ID 2	R	0x0

Table 9-151. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC2_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-152. VIP_OUTPUT_PORT_A_SRC3_SIZE

Address Offset	0x0000 003C		
Physical Address	0x4897 553C 0x4897 5A3C 0x4899 553C 0x4899 5A3C 0x489B 553C 0x489B 5A3C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC3_WIDTH								RESERVED								PRTA_SRC3_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC3_WIDTH	On Port A. Width of Source ID 3	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC3_HEIGHT	On Port A. Height of Source ID 3	R	0x0

Table 9-153. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC3_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-154. VIP_OUTPUT_PORT_A_SRC4_SIZE

Address Offset	0x0000 0040		
Physical Address	0x4897 5540 0x4897 5A40 0x4899 5540 0x4899 5A40 0x489B 5540 0x489B 5A40	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 4		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC4_WIDTH								RESERVED								PRTA_SRC4_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC4_WIDTH	On Port A. Width of Source ID 4	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC4_HEIGHT	On Port A. Height of Source ID 4	R	0x0

Table 9-155. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC4_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-156. VIP_OUTPUT_PORT_A_SRC5_SIZE

Address Offset	0x0000 0044		
Physical Address	0x4897 5544 0x4897 5A44 0x4899 5544 0x4899 5A44 0x489B 5544 0x489B 5A44	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 5		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC5_WIDTH								RESERVED								PRTA_SRC5_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC5_WIDTH	On Port A. Width of Source ID 5	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC5_HEIGHT	On Port A. Height of Source ID 5	R	0x0

Table 9-157. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC5_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-158. VIP_OUTPUT_PORT_A_SRC6_SIZE

Address Offset	0x0000 0048		
Physical Address	0x4897 5548 0x4897 5A48 0x4899 5548 0x4899 5A48 0x489B 5548 0x489B 5A48	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 6		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC6_WIDTH								RESERVED								PRTA_SRC6_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC6_WIDTH	On Port A. Width of Source ID 6	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC6_HEIGHT	On Port A. Height of Source ID 6	R	0x0

Table 9-159. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC6_SIZE

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

Table 9-160. VIP_OUTPUT_PORT_A_SRC7_SIZE

Address Offset	0x0000 004C		
Physical Address	0x4897 554C 0x4897 5A4C 0x4899 554C 0x4899 5A4C 0x489B 554C 0x489B 5A4C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 7		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC7_WIDTH								RESERVED								PRTA_SRC7_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC7_WIDTH	On Port A. Width of Source ID 7	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC7_HEIGHT	On Port A. Height of Source ID 7	R	0x0

Table 9-161. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC7_SIZE

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

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Table 9-162. VIP_OUTPUT_PORT_A_SRC8_SIZE

Address Offset	0x0000 0050		
Physical Address	0x4897 5550 0x4897 5A50 0x4899 5550 0x4899 5A50 0x489B 5550 0x489B 5A50	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 8		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC8_WIDTH								RESERVED								PRTA_SRC8_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC8_WIDTH	On Port A. Width of Source ID 8	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC8_HEIGHT	On Port A. Height of Source ID 8	R	0x0

Table 9-163. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC8_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-164. VIP_OUTPUT_PORT_A_SRC9_SIZE

Address Offset	0x0000 0054		
Physical Address	0x4897 5554 0x4897 5A54 0x4899 5554 0x4899 5A54 0x489B 5554 0x489B 5A54	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 9		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC9_WIDTH								RESERVED								PRTA_SRC9_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC9_WIDTH	On Port A. Width of Source ID 9	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC9_HEIGHT	On Port A. Height of Source ID 9	R	0x0

Table 9-165. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC9_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-166. VIP_OUTPUT_PORT_A_SRC10_SIZE

Address Offset	0x0000 0058		
Physical Address	0x4897 5558 0x4897 5A58 0x4899 5558 0x4899 5A58 0x489B 5558 0x489B 5A58	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 10		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC10_WIDTH								RESERVED								PRTA_SRC10_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC10_WIDTH	On Port A. Width of Source ID 10	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC10_HEIGHT	On Port A. Height of Source ID 10	R	0x0

Table 9-167. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC10_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-168. VIP_OUTPUT_PORT_A_SRC11_SIZE

Address Offset	0x0000 005C		
Physical Address	0x4897 555C 0x4897 5A5C 0x4899 555C 0x4899 5A5C 0x489B 555C 0x489B 5A5C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 11		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC11_WIDTH								RESERVED								PRTA_SRC11_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC11_WIDTH	On Port A. Width of Source ID 11	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC11_HEIGHT	On Port A. Height of Source ID 11	R	0x0

Table 9-169. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC11_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-170. VIP_OUTPUT_PORT_A_SRC12_SIZE

Address Offset	0x0000 0060		
Physical Address	0x4897 5560 0x4897 5A60 0x4899 5560 0x4899 5A60 0x489B 5560 0x489B 5A60	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 12		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC12_WIDTH								RESERVED								PRTA_SRC12_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC12_WIDTH	On Port A. Width of Source ID 12	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC12_HEIGHT	On Port A. Height of Source ID 12	R	0x0

Table 9-171. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC12_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-172. VIP_OUTPUT_PORT_A_SRC13_SIZE

Address Offset	0x0000 0064		
Physical Address	0x4897 5564 0x4897 5A64 0x4899 5564 0x4899 5A64 0x489B 5564 0x489B 5A64	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 13		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC13_WIDTH								RESERVED								PRTA_SRC13_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC13_WIDTH	On Port A. Width of Source ID 13	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC13_HEIGHT	On Port A. Height of Source ID 13	R	0x0

Table 9-173. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC13_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-174. VIP_OUTPUT_PORT_A_SRC14_SIZE

Address Offset	0x0000 0068		
Physical Address	0x4897 5568 0x4897 5A68 0x4899 5568 0x4899 5A68 0x489B 5568 0x489B 5A68	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 14		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC14_WIDTH								RESERVED								PRTA_SRC14_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC14_WIDTH	On Port A. Width of Source ID 14	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC14_HEIGHT	On Port A. Height of Source ID 14	R	0x0

Table 9-175. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC14_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-176. VIP_OUTPUT_PORT_A_SRC15_SIZE

Address Offset	0x0000 006C		
Physical Address	0x4897 556C 0x4897 5A6C 0x4899 556C 0x4899 5A6C 0x489B 556C 0x489B 5A6C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 15		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTA_SRC15_WIDTH								RESERVED								PRTA_SRC15_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTA_SRC15_WIDTH	On Port A. Width of Source ID 15	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTA_SRC15_HEIGHT	On Port A. Height of Source ID 15	R	0x0

Table 9-177. Register Call Summary for Register VIP_OUTPUT_PORT_A_SRC15_SIZE

VIP Functional Description
- Source Multiplexing: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

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Table 9-178. VIP_OUTPUT_PORT_B_SRC0_SIZE

Address Offset	0x0000 0070		
Physical Address	0x4897 5570 0x4897 5A70 0x4899 5570 0x4899 5A70 0x489B 5570 0x489B 5A70	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC0_WIDTH								RESERVED								PRTB_SRC0_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC0_WIDTH	On Port B. Width of Source ID 0	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC0_HEIGHT	On Port B. Height of Source ID 0	R	0x0

Table 9-179. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC0_SIZE

VIP Functional Description
- Source Multiplexing: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

Table 9-180. VIP_OUTPUT_PORT_B_SRC1_SIZE

Address Offset	0x0000 0074		
Physical Address	0x4897 5574 0x4897 5A74 0x4899 5574 0x4899 5A74 0x489B 5574 0x489B 5A74	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC1_WIDTH								RESERVED								PRTB_SRC1_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC1_WIDTH	On Port B. Width of Source ID 1	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC1_HEIGHT	On Port B. Height of Source ID 1	R	0x0

Table 9-181. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC1_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-182. VIP_OUTPUT_PORT_B_SRC2_SIZE

Address Offset	0x0000 0078		
Physical Address	0x4897 5578 0x4897 5A78 0x4899 5578 0x4899 5A78 0x489B 5578 0x489B 5A78	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC2_WIDTH								RESERVED								PRTB_SRC2_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC2_WIDTH	On Port B. Width of Source ID 2	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC2_HEIGHT	On Port B. Height of Source ID 2	R	0x0

Table 9-183. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC2_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-184. VIP_OUTPUT_PORT_B_SRC3_SIZE

Address Offset	0x0000 007C		
Physical Address	0x4897 557C 0x4897 5A7C 0x4899 557C 0x4899 5A7C 0x489B 557C 0x489B 5A7C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC3_WIDTH								RESERVED								PRTB_SRC3_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC3_WIDTH	On Port B. Width of Source ID 3	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC3_HEIGHT	On Port B. Height of Source ID 3	R	0x0

Table 9-185. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC3_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-186. VIP_OUTPUT_PORT_B_SRC4_SIZE

Address Offset	0x0000 0080		
Physical Address	0x4897 5580 0x4897 5A80 0x4899 5580 0x4899 5A80 0x489B 5580 0x489B 5A80	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 4		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC4_WIDTH								RESERVED								PRTB_SRC4_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC4_WIDTH	On Port B. Width of Source ID 4	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC4_HEIGHT	On Port B. Height of Source ID 4	R	0x0

Table 9-187. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC4_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-188. VIP_OUTPUT_PORT_B_SRC5_SIZE

Address Offset	0x0000 0084		
Physical Address	0x4897 5584 0x4897 5A84 0x4899 5584 0x4899 5A84 0x489B 5584 0x489B 5A84	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 5		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC5_WIDTH								RESERVED								PRTB_SRC5_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC5_WIDTH	On Port B. Width of Source ID 5	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC5_HEIGHT	On Port B. Height of Source ID 5	R	0x0

Table 9-189. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC5_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-190. VIP_OUTPUT_PORT_B_SRC6_SIZE

Address Offset	0x0000 0088		
Physical Address	0x4897 5588 0x4897 5A88 0x4899 5588 0x4899 5A88 0x489B 5588 0x489B 5A88	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 6		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC6_WIDTH								RESERVED								PRTB_SRC6_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC6_WIDTH	On Port B. Width of Source ID 6	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC6_HEIGHT	On Port B. Height of Source ID 6	R	0x0

Table 9-191. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC6_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-192. VIP_OUTPUT_PORT_B_SRC7_SIZE

Address Offset	0x0000 008C		
Physical Address	0x4897 558C 0x4897 5A8C 0x4899 558C 0x4899 5A8C 0x489B 558C 0x489B 5A8C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 7		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC7_WIDTH								RESERVED								PRTB_SRC7_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC7_WIDTH	On Port B. Width of Source ID 7	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC7_HEIGHT	On Port B. Height of Source ID 7	R	0x0

Table 9-193. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC7_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-194. VIP_OUTPUT_PORT_B_SRC8_SIZE

Address Offset	0x0000 0090		
Physical Address	0x4897 5590 0x4897 5A90 0x4899 5590 0x4899 5A90 0x489B 5590 0x489B 5A90	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 8		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC8_WIDTH								RESERVED								PRTB_SRC8_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC8_WIDTH	On Port B. Width of Source ID 8	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC8_HEIGHT	On Port B. Height of Source ID 8	R	0x0

Table 9-195. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC8_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-196. VIP_OUTPUT_PORT_B_SRC9_SIZE

Address Offset	0x0000 0094		
Physical Address	0x4897 5594 0x4897 5A94 0x4899 5594 0x4899 5A94 0x489B 5594 0x489B 5A94	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 9		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC9_WIDTH								RESERVED								PRTB_SRC9_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC9_WIDTH	On Port B. Width of Source ID 9	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC9_HEIGHT	On Port B. Height of Source ID 9	R	0x0

Table 9-197. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC9_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-198. VIP_OUTPUT_PORT_B_SRC10_SIZE

Address Offset	0x0000 0098		
Physical Address	0x4897 5598 0x4897 5A98 0x4899 5598 0x4899 5A98 0x489B 5598 0x489B 5A98	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 10		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC10_WIDTH								RESERVED								PRTB_SRC10_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC10_WIDTH	On Port B. Width of Source ID 10	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC10_HEIGHT	On Port B. Height of Source ID 10	R	0x0

Table 9-199. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC10_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-200. VIP_OUTPUT_PORT_B_SRC11_SIZE

Address Offset	0x0000 009C		
Physical Address	0x4897 559C 0x4897 5A9C 0x4899 559C 0x4899 5A9C 0x489B 559C 0x489B 5A9C	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 11		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC11_WIDTH								RESERVED								PRTB_SRC11_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC11_WIDTH	On Port B. Width of Source ID 11	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC11_HEIGHT	On Port B. Height of Source ID 11	R	0x0

Table 9-201. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC11_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-202. VIP_OUTPUT_PORT_B_SRC12_SIZE

Address Offset	0x0000 00A0		
Physical Address	0x4897 55A0 0x4897 5AA0 0x4899 55A0 0x4899 5AA0 0x489B 55A0 0x489B 5AA0	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 12		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC12_WIDTH								RESERVED								PRTB_SRC12_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC12_WIDTH	On Port B. Width of Source ID 12	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC12_HEIGHT	On Port B. Height of Source ID 12	R	0x0

Table 9-203. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC12_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-204. VIP_OUTPUT_PORT_B_SRC13_SIZE

Address Offset	0x0000 00A4		
Physical Address	0x4897 55A4 0x4897 5AA4 0x4899 55A4 0x4899 5AA4 0x489B 55A4 0x489B 5AA4	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 13		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC13_WIDTH								RESERVED								PRTB_SRC13_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC13_WIDTH	On Port B. Width of Source ID 13	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC13_HEIGHT	On Port B. Height of Source ID 13	R	0x0

Table 9-205. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC13_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

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Table 9-206. VIP_OUTPUT_PORT_B_SRC14_SIZE

Address Offset	0x0000 00A8		
Physical Address	0x4897 55A8 0x4897 5AA8 0x4899 55A8 0x4899 5AA8 0x489B 55A8 0x489B 5AA8	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 14		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC14_WIDTH								RESERVED								PRTB_SRC14_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC14_WIDTH	On Port B. Width of Source ID 14	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC14_HEIGHT	On Port B. Height of Source ID 14	R	0x0

Table 9-207. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC14_SIZE

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-208. VIP_OUTPUT_PORT_B_SRC15_SIZE

Address Offset	0x0000 00AC		
Physical Address	0x4897 55AC 0x4897 5AAC 0x4899 55AC 0x4899 5AAC 0x489B 55AC 0x489B 5AAC	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Width and Height for Source 15		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRTB_SRC15_WIDTH								RESERVED								PRTB_SRC15_HEIGHT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	PRTB_SRC15_WIDTH	On Port B. Width of Source ID 15	R	0x0
15:11	RESERVED		R	0x0
10:0	PRTB_SRC15_HEIGHT	On Port B. Height of Source ID 15	R	0x0

Table 9-209. Register Call Summary for Register VIP_OUTPUT_PORT_B_SRC15_SIZE

VIP Functional Description
- Source Multiplexing: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

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Table 9-210. VIP_PORT_A_VDET_VEC

Address Offset	0x0000 00B0		
Physical Address	0x4897 55B0 0x4897 5AB0 0x4899 55B0 0x4899 5AB0 0x489B 55B0 0x489B 5AB0	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Each bit represents the VDET bit setting for Line Mux Mode		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTA_VDET_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	PRTA_VDET_VEC	For Embedded Sync Only In Line Mux Mode. each bit represents the vdet value on Port A for the corresponding source id. This vector is meaningless for 1x/2x/4x mux modes.	R	0x0

Table 9-211. Register Call Summary for Register VIP_PORT_A_VDET_VEC

VIP Functional Description
- VDET Interrupt: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

Table 9-212. VIP_PORT_B_VDET_VEC

Address Offset	0x0000 00B4		
Physical Address	0x4897 55B4 0x4897 5AB4 0x4899 55B4 0x4899 5AB4 0x489B 55B4 0x489B 5AB4	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Each bit represents the VDET bit setting for Line Mux Mode		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTB_VDET_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	PRTB_VDET_VEC	For Embedded Sync Only In Line Mux Mode. each bit represents the vdet value on Port B for the corresponding source id. This vector is meaningless for 1x/2x/4x mux modes.	R	0x0

Table 9-213. Register Call Summary for Register VIP_PORT_B_VDET_VEC

VIP Functional Description
- VDET Interrupt: [0]

VIP Register Manual
- VIP Parser Register Summary: [1] [4]

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Table 9-214. VIP_ANC_CROP_HORZ_PORT_A

Address Offset	0x0000 00B8		
Physical Address	0x4897 55B8 0x4897 5AB8 0x4899 55B8 0x4899 5AB8 0x489B 55B8 0x489B 5AB8	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Ancillary Cropping Configuration for Input Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_TARGET_SRCNUM				ANC_USE_NUMPIX												ANC_BYPASS_N	RESERVED			ANC_SKIP_NUMPIX												

Bits	Field Name	Description	Type	Reset
31:28	ANC_TARGET_SRCNUM	The cropping module can work on only one srcnum. specified in this field. for each dss_vip_parser output port (Ancillary data).	RW	0x0
27:16	ANC_USE_NUMPIX	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.	RW	0x0
15	ANC_BYPASS_N	0 = Bypass cropping module 1 = Cropping module enabled	RW	0x0
14:12	RESERVED		R	0x0
11:0	ANC_SKIP_NUMPIX	The number of pixels to crop from the beginning of each line.	RW	0x0

Table 9-215. Register Call Summary for Register VIP_ANC_CROP_HORZ_PORT_A

VIP Functional Description

- Ancillary and Active Video Cropping: [0] [1] [2] [3]

VIP Register Manual

- VIP Parser Register Summary: [4] [7]

Table 9-216. VIP_ANC_CROP_VERT_PORT_A

Address Offset	0x0000 00BC		
Physical Address	0x4897 55BC 0x4897 5ABC 0x4899 55BC 0x4899 5ABC 0x489B 55BC 0x489B 5ABC	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Ancillary Cropping Configuration for Input Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ANC_USE_NUMLINES												RESERVED				ANC_SKIP_NUMLINES												

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	ANC_USE_NUMLINES	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's ancillary data region.	RW	0x0
15:12	RESERVED		R	0x0
11:0	ANC_SKIP_NUMLINES	The number of lines to crop from the top of the vertical ancillary data region.	RW	0x0

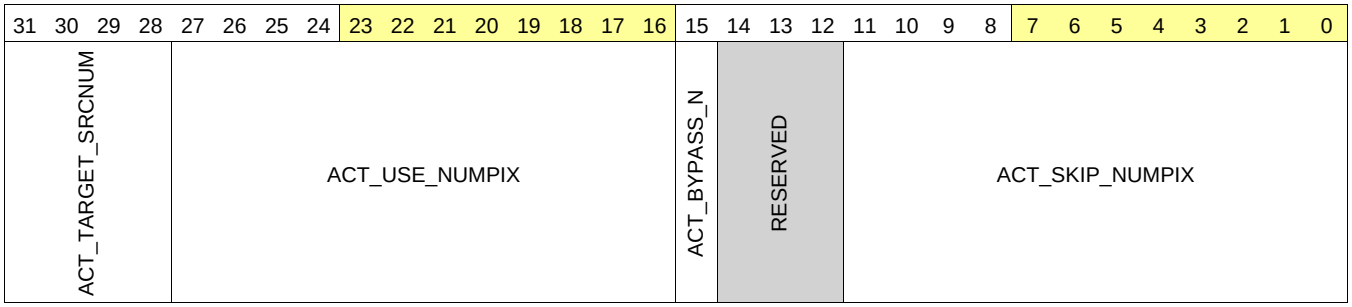
Table 9-217. Register Call Summary for Register VIP_ANC_CROP_VERT_PORT_A

VIP Functional Description
- Ancillary and Active Video Cropping: [0] [1]

VIP Register Manual
- VIP Parser Register Summary: [2] [5]

Table 9-218. VIP_CROP_HORZ_PORT_A

Address Offset	0x0000 00C0		
Physical Address	0x4897 55C0 0x4897 5AC0 0x4899 55C0 0x4899 5AC0 0x489B 55C0 0x489B 5AC0	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Active Video Cropping Configuration for Input Port A		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	ACT_TARGET_SRCNUM	The cropping module can work on only one srcnum. specified in this field. for each dss_vip_parser output port (Active video).	RW	0x0
27:16	ACT_USE_NUMPIX	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.	RW	0x0
15	ACT_BYPASS_N	0 = Bypass cropping module 1 = Cropping module enabled	RW	0x0
14:12	RESERVED		R	0x0
11:0	ACT_SKIP_NUMPIX	The number of pixels to crop from the beginning of each line.	RW	0x0

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Table 9-219. Register Call Summary for Register VIP_CROP_HORZ_PORT_A

VIP Functional Description
• Ancillary and Active Video Cropping: [0] [1] [2] [3]
VIP Register Manual
• VIP Parser Register Summary: [4] [7]

Table 9-220. VIP_CROP_VERT_PORT_A

Address Offset	0x0000 00C4		
Physical Address	0x4897 55C4	**Instance**	VIP1_Slice0_parser
	0x4897 5AC4		VIP1_Slice1_parser
	0x4899 55C4		VIP2_Slice0_parser
	0x4899 5AC4		VIP2_Slice1_parser
	0x489B 55C4		VIP3_Slice0_parser
	0x489B 5AC4		VIP3_Slice1_parser
Description	Active Video Cropping Configuration for Input Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ACT_USE_NUMLINES												RESERVED				ACT_SKIP_NUMLINES											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	ACT_USE_NUMLINES	When cropping.. the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's active video region.	RW	0x0
15:12	RESERVED		R	0x0
11:0	ACT_SKIP_NUMLINES	The number of lines to crop from the top of the vertical active video region.	RW	0x0

Table 9-221. Register Call Summary for Register VIP_CROP_VERT_PORT_A

VIP Functional Description
• Ancillary and Active Video Cropping: [0] [1]
VIP Register Manual
• VIP Parser Register Summary: [2] [5]

Table 9-222. VIP_ANC_VIP_CROP_HORZ_PORT_B

Address Offset	0x0000 00C8		
Physical Address	0x4897 55C8	**Instance**	VIP1_Slice0_parser
	0x4897 5AC8		VIP1_Slice1_parser
	0x4899 55C8		VIP2_Slice0_parser
	0x4899 5AC8		VIP2_Slice1_parser
	0x489B 55C8		VIP3_Slice0_parser
	0x489B 5AC8		VIP3_Slice1_parser
Description	Ancillary Cropping Configuration for Input Port B		
Type	RW		

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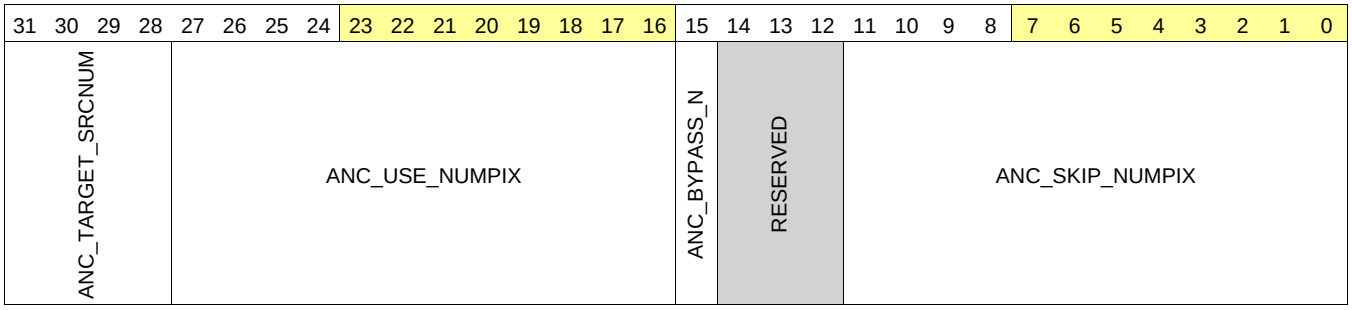


Bits	Field Name	Description	Type	Reset
31:28	ANC_TARGET_SRCNUM	The cropping module can work on only one srcnum. specified in this field. for each dss_vip_parser output port (Ancillary data).	RW	0x0
27:16	ANC_USE_NUMPIX	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.	RW	0x0
15	ANC_BYPASS_N	0 = Bypass cropping module 1 = Cropping module enabled	RW	0x0
14:12	RESERVED		R	0x0
11:0	ANC_SKIP_NUMPIX	The number of pixels to crop from the beginning of each line.	RW	0x0

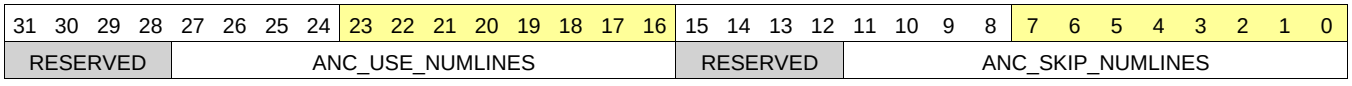
Table 9-223. Register Call Summary for Register VIP_ANC_VIP_CROP_HORZ_PORT_B

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

Table 9-224. VIP_ANC_VIP_CROP_VERT_PORT_B

Address Offset	0x0000 00CC		
Physical Address	0x4897 55CC 0x4897 5ACC 0x4899 55CC 0x4899 5ACC 0x489B 55CC 0x489B 5ACC	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Ancillary Cropping Configuration for Input Port B		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	ANC_USE_NUMLINES	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnums active video region.	RW	0x0
15:12	RESERVED		R	0x0
11:0	ANC_SKIP_NUMLINES	The number of lines to crop from the top of the vertical ancillary data region.	RW	0x0

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Table 9-225. Register Call Summary for Register VIP_ANC_VIP_CROP_VERT_PORT_B

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-226. VIP_CROP_HORZ_PORT_B

Address Offset	0x0000 00D0		
Physical Address	0x4897 55D0 0x4897 5AD0 0x4899 55D0 0x4899 5AD0 0x489B 55D0 0x489B 5AD0	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Active Video Cropping Configuration for Input Port B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACT_TARGET_SRCNUM				ACT_USE_NUMPIX												ACT_BYPASS_N	RESERVED			ACT_SKIP_NUMPIX											

Bits	Field Name	Description	Type	Reset
31:28	ACT_TARGET_SRCNUM	The cropping module can work on only one srcnum. specified in this field. for each dss_vip_parser output port (Active video).	RW	0x0
27:16	ACT_USE_NUMPIX	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.	RW	0x0
15	ACT_BYPASS_N	0 = Bypass cropping module 1 = Cropping module enabled	RW	0x0
14:12	RESERVED		R	0x0
11:0	ACT_SKIP_NUMPIX	The number of pixels to crop from the beginning of each line.	RW	0x0

Table 9-227. Register Call Summary for Register VIP_CROP_HORZ_PORT_B

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-228. VIP_CROP_VERT_PORT_B

Address Offset	0x0000 00D4		
Physical Address	0x4897 55D4 0x4897 5AD4 0x4899 55D4 0x4899 5AD4 0x489B 55D4 0x489B 5AD4	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Active Video Cropping Configuration for Input Port B		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ACT_USE_NUMLINES								RESERVED								ACT_SKIP_NUMLINES							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	ACT_USE_NUMLINES	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's active video region.	RW	0x0
15:12	RESERVED		R	0x0
11:0	ACT_SKIP_NUMLINES	The number of lines to crop from the top of the vertical active video region.	RW	0x0

Table 9-229. Register Call Summary for Register VIP_CROP_VERT_PORT_B

VIP Register Manual

- VIP Parser Register Summary: [0] [3]

Table 9-230. VIP_XTRA6_PORT_A

Address Offset	0x0000 00D8		
Physical Address	0x4897 55D8 0x4897 5AD8 0x4899 55D8 0x4899 5AD8 0x489B 55D8 0x489B 5AD8	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Cfg Disable Active Srcnum Vector Input for Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YUV_SRCNUM_STOP_IMMEDIATELY																ANC_SRCNUM_STOP_IMMEDIATELY															

Bits	Field Name	Description	Type	Reset
31:16	YUV_SRCNUM_STOP_IMMEDIATELY	For the Active Video Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A ?0? in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A ?1? in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to ?0?, the port will never disable.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15:0	ANC_SRCNUM_STOP_IMMEDIATELY	For the Ancillary Data Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A ?0? in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A ?1? in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to ?0?, the port will never disable.	RW	0x0

Table 9-231. Register Call Summary for Register VIP_XTRA6_PORT_A

VIP Functional Description
- VIP Overflow Detection and Recovery: [0] [1] [2] [3]

VIP Register Manual
- VIP Parser Register Summary: [4] [7]

Table 9-232. VIP_XTRA7_PORT_B

Address Offset	0x0000 00DC		
Physical Address	0x4897 55DC 0x4897 5ADC 0x4899 55DC 0x4899 5ADC 0x489B 55DC 0x489B 5ADC	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Cfg Disable Active Srcnum Vector Input for Port B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YUV_SRCNUM_STOP_IMMEDIATELY																ANC_SRCNUM_STOP_IMMEDIATELY															

Bits	Field Name	Description	Type	Reset
31:16	YUV_SRCNUM_STOP_IMMEDIATELY	For the Active Video Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A ?0? in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A ?1? in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to ?0?, the port will never disable.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15:0	ANC_SRCNUM_STOP_IMMEDIATELY	For the Ancillary Data Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A ?0? in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A ?1? in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to ?0?, the port will never disable.	RW	0x0

Table 9-233. Register Call Summary for Register VIP_XTRA7_PORT_B

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-234. VIP_XTRA8_PORT_A

Address Offset	0x0000 00E0		
Physical Address	0x4897 55E0 0x4897 5AE0 0x4899 55E0 0x4899 5AE0 0x489B 55E0 0x489B 5AE0	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Reserved Register for Port A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	ust be 0x0 at all times.	RW	0x0

Table 9-235. Register Call Summary for Register VIP_XTRA8_PORT_A

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

Table 9-236. VIP_XTRA9_PORT_B

Address Offset	0x0000 00E4		
Physical Address	0x4897 55E4 0x4897 5AE4 0x4899 55E4 0x4899 5AE4 0x489B 55E4 0x489B 5AE4	**Instance**	VIP1_Slice0_parser VIP1_Slice1_parser VIP2_Slice0_parser VIP2_Slice1_parser VIP3_Slice0_parser VIP3_Slice1_parser
Description	Reserved Register for Port B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

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Bits	Field Name	Description	Type	Reset
31:0	RESERVED	ust be 0x0 at all times.	RW	0x0

Table 9-237. Register Call Summary for Register VIP_XTRA9_PORT_B

VIP Register Manual
- VIP Parser Register Summary: [0] [3]

9.5.4 VIP CSC Registers

9.5.4.1 VIP CSC Register Summary

Table 9-238. VIP CSC Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_Slice0_csc Base Address	VIP1_Slice1_csc Base Address
VIP_CSC00	RW	32	0x0000 0000	0x4897 5700	0x4897 5C00
VIP_CSC01	RW	32	0x0000 0004	0x4897 5704	0x4897 5C04
VIP_CSC02	RW	32	0x0000 0008	0x4897 5708	0x4897 5C08
VIP_CSC03	RW	32	0x0000 000C	0x4897 570C	0x4897 5C0C
VIP_CSC04	RW	32	0x0000 0010	0x4897 5710	0x4897 5C10
VIP_CSC05	RW	32	0x0000 0014	0x4897 5714	0x4897 5C14

Table 9-239. VIP CSC Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	VIP2_Slice0_csc Base Address	VIP2_Slice1_csc Base Address
VIP_CSC00	RW	32	0x0000 0000	0x4899 5700	0x4899 5C00
VIP_CSC01	RW	32	0x0000 0004	0x4899 5704	0x4899 5C04
VIP_CSC02	RW	32	0x0000 0008	0x4899 5708	0x4899 5C08
VIP_CSC03	RW	32	0x0000 000C	0x4899 570C	0x4899 5C0C
VIP_CSC04	RW	32	0x0000 0010	0x4899 5710	0x4899 5C10
VIP_CSC05	RW	32	0x0000 0014	0x4899 5714	0x4899 5C14

Table 9-240. VIP CSC Registers Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	VIP3_Slice0_csc Base Address	VIP3_Slice1_csc Base Address
VIP_CSC00	RW	32	0x0000 0000	0x489B 5700	0x489B 5C00
VIP_CSC01	RW	32	0x0000 0004	0x489B 5704	0x489B 5C04
VIP_CSC02	RW	32	0x0000 0008	0x489B 5708	0x489B 5C08
VIP_CSC03	RW	32	0x0000 000C	0x489B 570C	0x489B 5C0C
VIP_CSC04	RW	32	0x0000 0010	0x489B 5710	0x489B 5C10
VIP_CSC05	RW	32	0x0000 0014	0x489B 5714	0x489B 5C14

9.5.4.2 VIP CSC Register Description

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Table 9-241. VIP_CSC00

Address Offset	0x0000 0000		
Physical Address	0x4897 5700 0x4897 5C00 0x4899 5700 0x4899 5C00 0x489B 5700 0x489B 5C00	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								B0								RESERVED								A0							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		RW	0x0
28:16	B0	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0
15:13	RESERVED		RW	0x0
12:0	A0	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. Rules for converting a real number coefficient to a 12-bit hex number for this register: - If the real number is positive, then simply multiply it by 1024, and convert the integer part to hex format. For example, 0.673 X 1024 = 689.152, then 0x2B1 should fill in to this register - If the real number is negative, then multiply it by 1024, and convert it to 2's compliment format in 12-bit. For example, if a coefficient is -1.893, by *1024 to this number, it becomes -1938. The 2'S compliment format of -1938 is 0x186E (in 13-bit width). Then 0x186E should be the number assigned to this register.	RW	0x0

Table 9-242. Register Call Summary for Register VIP_CSC00

VIP Functional Description

- CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]

VIP Register Manual

- VIP CSC Register Summary: [10] [12] [13]

Table 9-243. VIP_CSC01

Address Offset	0x0000 0004		
Physical Address	0x4897 5704 0x4897 5C04 0x4899 5704 0x4899 5C04 0x489B 5704 0x489B 5C04	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								A1								RESERVED								C0							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		RW	0x0
28:16	A1	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0
15:13	RESERVED		RW	0x0
12:0	C0	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0

Table 9-244. Register Call Summary for Register VIP_CSC01

VIP Functional Description
- CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]

VIP Register Manual
- VIP CSC Register Summary: [10] [12] [13]

Table 9-245. VIP_CSC02

Address Offset	0x0000 0008		
Physical Address	0x4897 5708 0x4897 5C08 0x4899 5708 0x4899 5C08 0x489B 5708 0x489B 5C08	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C1								RESERVED								B1							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		RW	0x0
28:16	C1	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0
15:13	RESERVED		RW	0x0
12:0	B1	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0

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Table 9-246. Register Call Summary for Register VIP_CSC02

VIP Functional Description
• CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
VIP Register Manual
• VIP CSC Register Summary: [10] [12] [13]

Table 9-247. VIP_CSC03

Address Offset	0x0000 000C		
Physical Address	0x4897 570C 0x4897 5C0C 0x4899 570C 0x4899 5C0C 0x489B 570C 0x489B 5C0C	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								B2								RESERVED								A2							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		RW	0x0
28:16	B2	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0
15:13	RESERVED		RW	0x0
12:0	A2	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0

Table 9-248. Register Call Summary for Register VIP_CSC03

VIP Functional Description
• CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
VIP Register Manual
• VIP CSC Register Summary: [10] [12] [13]

Table 9-249. VIP_CSC04

Address Offset	0x0000 0010		
Physical Address	0x4897 5710 0x4897 5C10 0x4899 5710 0x4899 5C10 0x489B 5710 0x489B 5C10	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								D0								RESERVED								C2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		RW	0x0
27:16	D0	Coefficients of color space converter. This coefficient is an integer number in the range of 2048. It is in 12-bit wide 2's compliment format. The MSB is sign bit. For example, if this coefficient is 749, then 0x2ED (hex format) should be assigned to this register. Another example, if this coefficient is -1021, then 0xC03 should be assigned to this register.	RW	0x0
15:13	RESERVED		RW	0x0
12:0	C2	Coefficients of color space converter. This coefficient is a real number in the range of 4. The MSB is sign bit. (Same format conversion as A0)	RW	0x0

Table 9-250. Register Call Summary for Register VIP_CSC04

VIP Functional Description

- CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]

VIP Register Manual

- VIP CSC Register Summary: [10] [12] [13]

Table 9-251. VIP_CSC05

Address Offset	0x0000 0014		
Physical Address	0x4897 5714 0x4897 5C14 0x4899 5714 0x4899 5C14 0x489B 5714 0x489B 5C14	**Instance**	VIP1_Slice0_csc VIP1_Slice1_csc VIP2_Slice0_csc VIP2_Slice1_csc VIP3_Slice0_csc VIP3_Slice1_csc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			BYPASS	D2												RESERVED				D1											

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		RW	0x0
28	BYPASS	Full CSC bypass mode	RW	0x0
27:16	D2	Coefficients of color space converter. This coefficient is an integer number in the range of 2048. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0)	RW	0x0
15:12	RESERVED		RW	0x0
11:0	D1	Coefficients of color space converter. This coefficient is an integer number in the range of 2048. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0)	RW	0x0

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Table 9-252. Register Call Summary for Register VIP_CSC05

VIP Functional Description • CSC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] • CSC Bypass Mode: [10]
VIP Register Manual • VIP CSC Register Summary: [11] [13] [14]

9.5.5 VIP SC registers

9.5.5.1 VIP SC Register Summary

Table 9-253. VIP SC Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_Slice0_sc Base Address	VIP1_Slice1_sc Base Address
VIP_CFG_SC0	RW	32	0x0000 0000	0x4897 5800	0x4897 5D00
VIP_CFG_SC1	RW	32	0x0000 0004	0x4897 5804	0x4897 5D04
VIP_CFG_SC2	RW	32	0x0000 0008	0x4897 5808	0x4897 5D08
VIP_CFG_SC3	RW	32	0x0000 000C	0x4897 580C	0x4897 5D0C
VIP_CFG_SC4	RW	32	0x0000 0010	0x4897 5810	0x4897 5D10
VIP_CFG_SC5	RW	32	0x0000 0014	0x4897 5814	0x4897 5D14
VIP_CFG_SC6	RW	32	0x0000 0018	0x4897 5818	0x4897 5D18
RESERVED	R	32	0x0000 001C	0x4897 581C	0x4897 5D1C
VIP_CFG_SC8	RW	32	0x0000 0020	0x4897 5820	0x4897 5D20
VIP_CFG_SC9	RW	32	0x0000 0024	0x4897 5824	0x4897 5D24
VIP_CFG_SC10	RW	32	0x0000 0028	0x4897 5828	0x4897 5D28
VIP_CFG_SC11	RW	32	0x0000 002C	0x4897 582C	0x4897 5D2C
VIP_CFG_SC12	RW	32	0x0000 0030	0x4897 5830	0x4897 5D30
VIP_CFG_SC13	RW	32	0x0000 0034	0x4897 5834	0x4897 5D34
RESERVED	R	32	0x0000 0038	0x4897 5838	0x4897 5D38
RESERVED	R	32	0x0000 003C	0x4897 583C	0x4897 5D3C
RESERVED	R	32	0x0000 0040	0x4897 5840	0x4897 5D40
RESERVED	R	32	0x0000 0044	0x4897 5844	0x4897 5D44
VIP_CFG_SC18	RW	32	0x0000 0048	0x4897 5848	0x4897 5D48
VIP_CFG_SC19	RW	32	0x0000 004C	0x4897 584C	0x4897 5D4C
VIP_CFG_SC20	RW	32	0x0000 0050	0x4897 5850	0x4897 5D50
VIP_CFG_SC21	RW	32	0x0000 0054	0x4897 5854	0x4897 5D54
VIP_CFG_SC22	RW	32	0x0000 0058	0x4897 5858	0x4897 5D58
RESERVED	R	32	0x0000 005C	0x4897 585C	0x4897 5D5C
VIP_CFG_SC24	RW	32	0x0000 0060	0x4897 5860	0x4897 5D60
VIP_CFG_SC25	RW	32	0x0000 0064	0x4897 5864	0x4897 5D64
RESERVED	R	32	0x0000 0068	0x4897 5868	0x4897 5D68
RESERVED	R	32	0x0000 006C	0x4897 586C	0x4897 5D6C
RESERVED	R	32	0x0000 0070	0x4897 5870	0x4897 5D70
RESERVED	R	32	0x0000 0074	0x4897 5874	0x4897 5D74
RESERVED	R	32	0x0000 0078	0x4897 5878	0x4897 5D78
RESERVED	R	32	0x0000 007C	0x4897 587C	0x4897 5D7C

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Table 9-254. VIP SC Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	VIP2_Slice0_sc Base Address	VIP2_Slice1_sc Base Address
VIP_CFG_SC0	RW	32	0x0000 0000	0x4899 5800	0x4899 5D00
VIP_CFG_SC1	RW	32	0x0000 0004	0x4899 5804	0x4899 5D04
VIP_CFG_SC2	RW	32	0x0000 0008	0x4899 5808	0x4899 5D08
VIP_CFG_SC3	RW	32	0x0000 000C	0x4899 580C	0x4899 5D0C
VIP_CFG_SC4	RW	32	0x0000 0010	0x4899 5810	0x4899 5D10
VIP_CFG_SC5	RW	32	0x0000 0014	0x4899 5814	0x4899 5D14
VIP_CFG_SC6	RW	32	0x0000 0018	0x4899 5818	0x4899 5D18
RESERVED	R	32	0x0000 001C	0x4899 581C	0x4899 5D1C
VIP_CFG_SC8	RW	32	0x0000 0020	0x4899 5820	0x4899 5D20
VIP_CFG_SC9	RW	32	0x0000 0024	0x4899 5824	0x4899 5D24
VIP_CFG_SC10	RW	32	0x0000 0028	0x4899 5828	0x4899 5D28
VIP_CFG_SC11	RW	32	0x0000 002C	0x4899 582C	0x4899 5D2C
VIP_CFG_SC12	RW	32	0x0000 0030	0x4899 5830	0x4899 5D30
VIP_CFG_SC13	RW	32	0x0000 0034	0x4899 5834	0x4899 5D34
RESERVED	R	32	0x0000 0038	0x4899 5838	0x4899 5D38
RESERVED	R	32	0x0000 003C	0x4899 583C	0x4899 5D3C
RESERVED	R	32	0x0000 0040	0x4899 5840	0x4899 5D40
RESERVED	R	32	0x0000 0044	0x4899 5844	0x4899 5D44
VIP_CFG_SC18	RW	32	0x0000 0048	0x4899 5848	0x4899 5D48
VIP_CFG_SC19	RW	32	0x0000 004C	0x4899 584C	0x4899 5D4C
VIP_CFG_SC20	RW	32	0x0000 0050	0x4899 5850	0x4899 5D50
VIP_CFG_SC21	RW	32	0x0000 0054	0x4899 5854	0x4899 5D54
VIP_CFG_SC22	RW	32	0x0000 0058	0x4899 5858	0x4899 5D58
RESERVED	R	32	0x0000 005C	0x4899 585C	0x4899 5D5C
VIP_CFG_SC24	RW	32	0x0000 0060	0x4899 5860	0x4899 5D60
VIP_CFG_SC25	RW	32	0x0000 0064	0x4899 5864	0x4899 5D64
RESERVED	R	32	0x0000 0068	0x4899 5868	0x4899 5D68
RESERVED	R	32	0x0000 006C	0x4899 586C	0x4899 5D6C
RESERVED	R	32	0x0000 0070	0x4899 5870	0x4899 5D70
RESERVED	R	32	0x0000 0074	0x4899 5874	0x4899 5D74
RESERVED	R	32	0x0000 0078	0x4899 5878	0x4899 5D78
RESERVED	R	32	0x0000 007C	0x4899 587C	0x4899 5D7C

Table 9-255. VIP SC Registers Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	VIP3_Slice0_sc Base Address	VIP3_Slice1_sc Base Address
VIP_CFG_SC0	RW	32	0x0000 0000	0x489B 5800	0x489B 5D00
VIP_CFG_SC1	RW	32	0x0000 0004	0x489B 5804	0x489B 5D04
VIP_CFG_SC2	RW	32	0x0000 0008	0x489B 5808	0x489B 5D08
VIP_CFG_SC3	RW	32	0x0000 000C	0x489B 580C	0x489B 5D0C
VIP_CFG_SC4	RW	32	0x0000 0010	0x489B 5810	0x489B 5D10
VIP_CFG_SC5	RW	32	0x0000 0014	0x489B 5814	0x489B 5D14
VIP_CFG_SC6	RW	32	0x0000 0018	0x489B 5818	0x489B 5D18
RESERVED	R	32	0x0000 001C	0x489B 581C	0x489B 5D1C
VIP_CFG_SC8	RW	32	0x0000 0020	0x489B 5820	0x489B 5D20
VIP_CFG_SC9	RW	32	0x0000 0024	0x489B 5824	0x489B 5D24

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Table 9-255. VIP SC Registers Mapping Summary 3 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP3_Slice0_sc Base Address	VIP3_Slice1_sc Base Address
VIP_CFG_SC10	RW	32	0x0000 0028	0x489B 5828	0x489B 5D28
VIP_CFG_SC11	RW	32	0x0000 002C	0x489B 582C	0x489B 5D2C
VIP_CFG_SC12	RW	32	0x0000 0030	0x489B 5830	0x489B 5D30
VIP_CFG_SC13	RW	32	0x0000 0034	0x489B 5834	0x489B 5D34
RESERVED	R	32	0x0000 0038	0x489B 5838	0x489B 5D38
RESERVED	R	32	0x0000 003C	0x489B 583C	0x489B 5D3C
RESERVED	R	32	0x0000 0040	0x489B 5840	0x489B 5D40
RESERVED	R	32	0x0000 0044	0x489B 5844	0x489B 5D44
VIP_CFG_SC18	RW	32	0x0000 0048	0x489B 5848	0x489B 5D48
VIP_CFG_SC19	RW	32	0x0000 004C	0x489B 584C	0x489B 5D4C
VIP_CFG_SC20	RW	32	0x0000 0050	0x489B 5850	0x489B 5D50
VIP_CFG_SC21	RW	32	0x0000 0054	0x489B 5854	0x489B 5D54
VIP_CFG_SC22	RW	32	0x0000 0058	0x489B 5858	0x489B 5D58
RESERVED	R	32	0x0000 005C	0x489B 585C	0x489B 5D5C
VIP_CFG_SC24	RW	32	0x0000 0060	0x489B 5860	0x489B 5D60
VIP_CFG_SC25	RW	32	0x0000 0064	0x489B 5864	0x489B 5D64
RESERVED	R	32	0x0000 0068	0x489B 5868	0x489B 5D68
RESERVED	R	32	0x0000 006C	0x489B 586C	0x489B 5D6C
RESERVED	R	32	0x0000 0070	0x489B 5870	0x489B 5D70
RESERVED	R	32	0x0000 0074	0x489B 5874	0x489B 5D74
RESERVED	R	32	0x0000 0078	0x489B 5878	0x489B 5D78
RESERVED	R	32	0x0000 007C	0x489B 587C	0x489B 5D7C

9.5.5.2 VIP SC Register Description

Table 9-256. VIP_CFG_SC0

Address Offset	0x0000 0000		
Physical Address	0x4897 5800 0x4897 5D00 0x4899 5800 0x4899 5D00 0x489B 5800 0x489B 5D00	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															CFG_FID_SELFGEN	CFG_TRIM	CFG_Y_PK_EN	RESERVED			CFG_INTERLACE_I	CFG_HP_BYPASS	CFG_DCM_4X	CFG_DCM_2X	CFG_AUTO_HS	CFG_ENABLE_EV	CFG_USE_RAV	CFG_INVT_FID	CFG_SC_BYPASS	CFG_LINEAR	CFG_INTERLACE_O

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0
16	CFG_FID_SELFGEN	FID self generate enable. When input is progressive and this bit is set, the SC generates self-toggling (top/bottom) output FID when performing interlacing.	RW	0x0
15	CFG_TRIM	Trimming enable. When 1, the input image whose size is specified by orgW and orgH registers is trimmed to the size with srcW and srcH from the offset specified by offW and offH. 0: disable trimming 1: enable trimming	RW	0x0
14	CFG_Y_PK_EN	This parameter is used by peaking block. 0: disable luma peaking 1: enable luma peaking	RW	0x0
13:11	RESERVED		R	0x0
10	CFG_INTERLACE_I	This parameter is used by both horizontal and vertical scaling 0: the input video format is progressive 1: the input video format is interlace	RW	0x0
9	CFG_HP_BYPASS	This parameter is used by horizontal scaling. If cfg_auto_hs is 0, horizontal polyphase filter is always enabled. In this case, this register is DON?T CARE. If cfg_auto_hs is 1, 0 : The polyphase scaler is always used regardless of the scaling ratio. 1 : The polyphase scaler is bypassed only when (tar_w == src_w) or (tar_w == src_w/2) or (tar_w == src_w/4)	RW	0x0
8	CFG_DCM_4X	This parameter is used by horizontal scaling. 0: the 4X decimation filter is disabled 1: the 4X decimation filter is enabled Note: (1) Either 2X or 4X can be enabled, but they cannot be enabled simultaneously. (2) This register is only set to 1 when it makes sense to do so. Typically, it is used when (horizontal scale ratio 0.25). (3) This register is DON?T CARE when cfg_auto_hs = 1.	RW	0x0
7	CFG_DCM_2X	This parameter is used by horizontal scaling. 0: the 2X decimation filter is disabled 1: the 2X decimation filter is enabled Note: (1) Either 2X or 4X can be enabled, but they cannot be enabled simultaneously. (2) This register is only set to 1 when it makes sense to do so. Typically, it is used when (0.25 horizontal scale ratio 0.5). (3) This register is DON?T CARE when cfg_auto_hs = 1.	RW	0x0
6	CFG_AUTO_HS	This parameter is used by horizontal scaling. 0: the cfg_dcm_2x and cfg_dcm_4x bits will enable appropriate decimation filters 1: HW will decide whether up-scaling or down-scaling is required based on horizontal scaling ratio (SR). SR 0.5 : horizontal polyphase filter is enabled, all decimation filters are disabled SR = 0.5 : dcm_2x is enabled, horizontal polyphase filter is enabled or disabled based on cfg_hp_bypass 0.5 SR 0.25 : dcm_2x and horizontal polyphase filter both are enabled SR = 0.25 : dcm_4x is enabled, horizontal polyphase filter is enabled or disabled based on cfg_hp_bypass 0.25 SR 0.125 : dcm_4x and horizontal polyphase filter are both enabled SR = 0.125 : Functionally supported, but not recommended in auto mode for image quality concerns	RW	0x0
5	CFG_ENABLE_EV	This parameter is used by the edge-detection block. 0: The output of edge-detection block will be force to ?0? 1: The calculation results of edge-detection block will be output normally	RW	0x0
4	CFG_USE_RAV	This parameter is used by vertical scaling. 0: Poly-phase filter will be used for the vertical scaling 1: Running average filter will be used for the vertical scaling (down scaling only)	RW	0x0
3	CFG_INVT_FID	This parameter is used by vertical scaling. 0: Progressive input 1: Interlaced input Must be set to 1 when CFG_INTERFACE_I = 1.	RW	0x0
2	CFG_SC_BYPASS	This parameter is a general purpose. 0: Scaling module will engaged 1: Scaling module will be bypassed	RW	0x0
1	CFG_LINEAR	This parameter is used by horizontal scaling. 0: Anamorphic scaling 1: Linear scaling	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	CFG_INTERLACE_O	This parameter is used by vertical scaling. 0: The output format of SC is progressive 1: The output format of SC is interlace	RW	0x0

Table 9-257. Register Call Summary for Register VIP_CFG_SC0

VIP Functional Description
- SC Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- SC Code: [14] [15] [16] [17] [18] [19] [20] [21] [22]

VIP Register Manual
- VIP SC Register Summary: [23] [25] [26]

Table 9-258. VIP_CFG_SC1

Address Offset	0x0000 0004		
Physical Address	0x4897 5804 0x4897 5D04 0x4899 5804 0x4899 5D04 0x489B 5804 0x489B 5D04	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_ROW_ACC_INC																							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:0	CFG_ROW_ACC_INC	This parameter is used by vertical scaling. It defines the increment of the row accumulator in vertical poly-phase filter. It can be calculated by following formula: row_acc_inc = round(2^16 *(src_h)/(tar_h)) In case of interlaced input, srcH is input field height In case of interlaced output, tarH is output field height.	RW	0x0

Table 9-259. Register Call Summary for Register VIP_CFG_SC1

VIP Functional Description
- SC Functional Description: [0]
- SC Code:

VIP Register Manual
- VIP SC Register Summary: [7] [9] [10]

Table 9-260. VIP_CFG_SC2

Address Offset	0x0000 0008		
Physical Address	0x4897 5808 0x4897 5D08 0x4899 5808 0x4899 5D08 0x489B 5808 0x489B 5D08	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_ROW_ACC_OFFSET																									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:0	CFG_ROW_ACC_OFFSET	This parameter is used by vertical scaling. It defines the vertical offset during vertical scaling. In progressive mode: this offset will be applied to a frame. In interlace mode: this offset will be applied to the top field.	RW	0x0

Table 9-261. Register Call Summary for Register VIP_CFG_SC2

VIP Functional Description
- SC Functional Description: [0]
- SC Code:

VIP Register Manual
- VIP SC Register Summary: [2] [4] [5]

Table 9-262. VIP_CFG_SC3

Address Offset	0x0000 000C		
Physical Address	0x4897 580C 0x4897 5D0C 0x4899 580C 0x4899 5D0C 0x489B 580C 0x489B 5D0C	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_ROW_ACC_OFFSET_B																									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:0	CFG_ROW_ACC_OFFSET_B	This parameter is used by vertical scaling. It defines the vertical offset during vertical scaling. In progressive mode: this parameter will not be used. In interlace mode: this offset will be applied to the bottom field.	RW	0x0

Table 9-263. Register Call Summary for Register VIP_CFG_SC3

VIP Functional Description
- SC Functional Description: [0]

VIP Register Manual
- VIP SC Register Summary: [1] [3] [4]

Table 9-264. VIP_CFG_SC4

Address Offset	0x0000 0010		
Physical Address	0x4897 5810 0x4897 5D10 0x4899 5810 0x4899 5D10 0x489B 5810 0x489B 5D10	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			

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Table 9-264. VIP_CFG_SC4 (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CFG_NLIN_ACC_INIT_U			RESERVED	CFG_LIN_ACC_INC_U			RESERVED	CFG_TAR_W							RESERVED	CFG_TAR_H														

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30:28	CFG_NLIN_ACC_INIT_U	This parameter is used by horizontal scaling. The 3 MSBbits of 'nlin_acc_init' that is defined in CFG_SC10	RW	0x0
27	RESERVED		R	0x0
26:24	CFG_LIN_ACC_INC_U	This parameter is used by horizontal scaling. The 3 MSBbits of 'lin_acc_inc' that is defined in CFG_SC9	RW	0x0
23	RESERVED		R	0x0
22:12	CFG_TAR_W	This parameter is a general purpose. Scaled target picture width. unit is pixel. This parameter defines the final output picture size	RW	0x0
11	RESERVED		R	0x0
10:0	CFG_TAR_H	This parameter is a general purpose. Scaled target picture height.. unit is line... This parameter defines the final output picture size. For the interlace output.. it should be the number of lines per field.	RW	0x0

Table 9-265. Register Call Summary for Register VIP_CFG_SC4

VIP Functional Description

- SC Functional Description: [0] [1] [2] [3] [4] [5] [6]

VIP Register Manual

- VIP SC Register Summary: [7] [9] [10]

Table 9-266. VIP_CFG_SC5

Address Offset	0x0000 0014		
Physical Address	0x4897 5814 0x4897 5D14 0x4899 5814 0x4899 5D14 0x489B 5814 0x489B 5D14	Instance	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CFG_NLIN_ACC_INC_U			RESERVED	CFG_SRC_W											RESERVED	CFG_SRC_H											

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:24	CFG_NLIN_ACC_INC_U	This parameter is used by horizontal scaling. The 3 MSBbits of ?nlin_acc_inc? that is defined in CFG_SC11	RW	0x0
23	RESERVED		R	0x0
22:12	CFG_SRC_W	This parameter is a general purpose. This parameter defines the width of the source image	RW	0x0
11	RESERVED		R	0x0
10:0	CFG_SRC_H	This parameter is a general purpose. This parameter defines the height of the source image. For the interlace input.. it should be the number of lines per field.	RW	0x0

Table 9-267. Register Call Summary for Register VIP_CFG_SC5

VIP Functional Description
- SC Functional Description: [0] [1] [2] [3] [4]

VIP Register Manual
- VIP SC Register Summary: [5] [7] [8]

Table 9-268. VIP_CFG_SC6

Address Offset	0x0000 0018		
Physical Address	0x4897 5818 0x4897 5D18 0x4899 5818 0x4899 5D18 0x489B 5818 0x489B 5D18	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CFG_ROW_ACC_INIT_RAV_B												CFG_ROW_ACC_INIT_RAV							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x0
19:10	CFG_ROW_ACC_INIT_RAV_B	This parameter is used by vertical scaling. it is used only when the input is interlace format. In vertical down scaling.. the running average filter is applied. This parameter sets the initialization value of the row accumulator in running average filter (for bottom field of interlace format)	RW	0x0
9:0	CFG_ROW_ACC_INIT_RAV	This parameter is used by vertical scaling. In vertical down scaling.. the running average filter is applied. This parameter sets the initialization value of the row accumulator in running average filter (for progressive format or top field of interlace format)	RW	0x0

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Table 9-269. Register Call Summary for Register VIP_CFG_SC6

VIP Functional Description
• SC Functional Description: [0] [1] [2] [3]
VIP Register Manual
• VIP SC Register Summary: [4] [6] [7]

Table 9-270. VIP_CFG_SC8

Address Offset	0x0000 0020		
Physical Address	0x4897 5820 0x4897 5D20 0x4899 5820 0x4899 5D20 0x489B 5820 0x489B 5D20	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_NLIN_RIGHT												RESERVED	CFG_NLIN_LEFT										

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x0
22:12	CFG_NLIN_RIGHT	This parameter is used by horizontal scaling. In anamorphic mode. this parameter defines the width of the strip on right-hand side. In other words. it defines the location of the last pixel where the linear scaling is ended. The unit is the 'pixel location' in an active video line. This parameter will not be used in linear scaling	RW	0x0
11	RESERVED		R	0x0
10:0	CFG_NLIN_LEFT	This parameter is used by horizontal scaling. In anamorphic mode. this parameter defines the width of the strip on left-hand side. In other words. it defines the location of the last pixel in the left-sidenonlinear strip. The unit is the 'pixel location' in an active video line. This parameter will not be used in linear scaling	RW	0x0

Table 9-271. Register Call Summary for Register VIP_CFG_SC8

VIP Functional Description
• SC Functional Description: [0] [1]
VIP Register Manual
• VIP SC Register Summary: [2] [4] [5]

Table 9-272. VIP_CFG_SC9

Address Offset	0x0000 0024		
Physical Address	0x4897 5824 0x4897 5D24 0x4899 5824 0x4899 5D24 0x489B 5824 0x489B 5D24	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			

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Table 9-272. VIP_CFG_SC9 (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_LIN_ACC_INC																															

Bits	Field Name	Description	Type	Reset
31:0	CFG_LIN_ACC_INC	This parameter is used by horizontal scaling. It defines the increment of the linear accumulator. if SR 0.5 then lin_acc_inc = round(2^24*(srcWi -1) /(tarWi -1)) else if 0.25 SR ? 0.5 lin_acc_inc = round(2^24*(srcWi/2 -1) /(tarWi - 1)) else if SR ? 0.25 lin_acc_inc = round(2^24*(srcWi/4 -1) /(tarWi - 1)) where srcWi and tarWi are the inner source width and the inner target width respectively.	RW	0x0

Table 9-273. Register Call Summary for Register VIP_CFG_SC9

VIP Functional Description

- SC Functional Description: [0] [1]

VIP Register Manual

- VIP SC Register Summary: [2] [4] [5]

Table 9-274. VIP_CFG_SC10

Address Offset	0x0000 0028		
Physical Address	0x4897 5828 0x4897 5D28 0x4899 5828 0x4899 5D28 0x489B 5828 0x489B 5D28	Instance	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_NLIN_ACC_INIT																															

Bits	Field Name	Description	Type	Reset
31:0	CFG_NLIN_ACC_INIT	This parameter is used by horizontal scaling. It is used by nonlinear scaling only. It defines the initialization value of the nonlinear accumulator. nlin_acc_init = K*(1-2*d) Here the definitions of K and d are the same as in CFG_SC11	RW	0x0

Table 9-275. Register Call Summary for Register VIP_CFG_SC10

VIP Register Manual

- VIP SC Register Summary: [0] [2] [3]

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Table 9-276. VIP_CFG_SC11

Address Offset	0x0000 002C		
Physical Address	0x4897 582C 0x4897 5D2C 0x4899 582C 0x4899 5D2C 0x489B 582C 0x489B 5D2C	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_NLIN_ACC_INC																															

Bits	Field Name	Description	Type	Reset
31:0	CFG_NLIN_ACC_INC	This parameter is used by horizontal scaling. It is used by nonlinear scaling only. It defines the increment of the nonlinear accumulator. if upscaling then d = 0 if Ltar !=0 then K =round[2^24*Lsrc/(Ltar*Ltar)] where Lsrc= (srcW-srcWi)/2 else K = 0 elseif downscaling d = (tarW-1)/2 if Ltar!=0 then K = round[2^24 * Lsrc / (Ltar*(Ltar-2d))] where Lsrc= (srcW-srcWi)/(2n) and n=1..2 or 4 else K = 0 nlin_acc_inc = 2*K (negative for downscaling)	RW	0x0

Table 9-277. Register Call Summary for Register VIP_CFG_SC11

VIP Register Manual

- VIP SC Register Summary: [0] [2] [3]

Table 9-278. VIP_CFG_SC12

Address Offset	0x0000 0030		
Physical Address	0x4897 5830 0x4897 5D30 0x4899 5830 0x4899 5D30 0x489B 5830 0x489B 5D30	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_COL_ACC_OFFSET																									

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24:0	CFG_COL_ACC_OFFSET	This parameter is used in horizontal scaling. It defines the luma accumulator's offset. Normally this parameter can be set as 0 if no horizontal offset is involved. In some applications.. such as Pan and Scan.. a corresponding offset value should be set. The format is 1.24.	RW	0x0

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Table 9-279. Register Call Summary for Register VIP_CFG_SC12

VIP Functional Description
• SC Code: [0]
VIP Register Manual
• VIP SC Register Summary: [1] [3] [4]

Table 9-280. VIP_CFG_SC13

Address Offset	0x0000 0034		
Physical Address	0x4897 5834 0x4897 5D34 0x4899 5834 0x4899 5D34 0x489B 5834 0x489B 5D34	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CFG_SC_FACTOR_RAV									

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0
9:0	CFG_SC_FACTOR_RAV	This parameter is used by vertical scaling. Vertical scaling factor: It is defined as following: 1024*tarH/srcH. It is used for downscaling by the running average filter	RW	0x0

Table 9-281. Register Call Summary for Register VIP_CFG_SC13

VIP Functional Description
• SC Functional Description: [0] [1] [2]
• SC Code: [3] [4]
VIP Register Manual
• VIP SC Register Summary: [5] [7] [8]

Table 9-282. VIP_CFG_SC18

Address Offset	0x0000 0048		
Physical Address	0x4897 5848 0x4897 5D48 0x4899 5848 0x4899 5D48 0x489B 5848 0x489B 5D48	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CFG_HS_FACTOR									

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0
9:0	CFG_HS_FACTOR	This parameter is used by horizontal scaling. Horizontal-scaling-factor = tarWi/srcWi. Numerical format: 6.4 (6 bit integer and 4 bit fraction)	RW	0x0

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Table 9-283. Register Call Summary for Register VIP_CFG_SC18

VIP Functional Description • SC Code: [0]
VIP Register Manual • VIP SC Register Summary: [1] [3] [4]

Table 9-284. VIP_CFG_SC19

Address Offset	0x0000 004C		
Physical Address	0x4897 584C 0x4897 5D4C 0x4899 584C 0x4899 5D4C 0x489B 584C 0x489B 5D4C	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_HPF_COEF3								CFG_HPF_COEF2								CFG_HPF_COEF1								CFG_HPF_COEF0							

Bits	Field Name	Description	Type	Reset
31:24	CFG_HPF_COEF3	This parameter is used by the peaking block. Defines the coefficient 3 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0
23:16	CFG_HPF_COEF2	This parameter is used by the peaking block. Defines the coefficient 2 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0
15:8	CFG_HPF_COEF1	This parameter is used by the peaking block. Defines the coefficient 1 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0
7:0	CFG_HPF_COEF0	This parameter is used by the peaking block. Defines the coefficient 0 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0

Table 9-285. Register Call Summary for Register VIP_CFG_SC19

VIP Functional Description • SC Functional Description: [0] [1] • SC Code: [2]
VIP Register Manual • VIP SC Register Summary: [3] [5] [6]

Table 9-286. VIP_CFG_SC20

Address Offset	0x0000 0050		
Physical Address	0x4897 5850 0x4897 5D50 0x4899 5850 0x4899 5D50 0x489B 5850 0x489B 5D50	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_NL_LIMIT				RESERVED	CFG_HPF_NORM_SHIFT			CFG_HPF_COEF5								CFG_HPF_COEF4								

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:20	CFG_NL_LIMIT	This parameter is used by the peaking block. The maximum of clipping.	RW	0x0
19	RESERVED		R	0x0
18:16	CFG_HPF_NORM_SHIFT	This parameter is used by the peaking block. Defines the decimal point of the hpf coefficient.	RW	0x0
15:8	CFG_HPF_COEF5	This parameter is used by the peaking block. Defines the coefficient 5 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0
7:0	CFG_HPF_COEF4	This parameter is used by the peaking block. Defines the coefficient 4 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.	RW	0x0

Table 9-287. Register Call Summary for Register VIP_CFG_SC20

VIP Functional Description
- SC Functional Description: [0] [1] [2]
- SC Code: [3]

VIP Register Manual
- VIP SC Register Summary: [4] [6] [7]

Table 9-288. VIP_CFG_SC21

Address Offset	0x0000 0054		
Physical Address	0x4897 5854 0x4897 5D54 0x4899 5854 0x4899 5D54 0x489B 5854 0x489B 5D54	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_NL_LO_SLOPE								RESERVED								CFG_NL_LO_THR							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x0
23:16	CFG_NL_LO_SLOPE	This parameter is used by the peaking block. Slope of the nonlinear peaking function. The format is fixed point 4.4.	RW	0x0
15:9	RESERVED		R	0x0
8:0	CFG_NL_LO_THR	This parameter is used by the peaking block. Threshold for the nonlinear peaking function. Must be 0	RW	0x0

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Table 9-289. Register Call Summary for Register VIP_CFG_SC21

VIP Functional Description • SC Functional Description: [0] [1] • SC Code: [2]
VIP Register Manual • VIP SC Register Summary: [3] [5] [6]

Table 9-290. VIP_CFG_SC22

Address Offset	0x0000 0058		
Physical Address	0x4897 5858 0x4897 5D58 0x4899 5858 0x4899 5D58 0x489B 5858 0x489B 5D58	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CFG_NL_HI_SLOPE_SHIFT			RESERVED								CFG_NL_HI_THR							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0
18:16	CFG_NL_HI_SLOPE_SHIFT	This parameter is used by the peaking block. Slope of the nonlinear peaking function. The gain is 2^(nl_hi_slope_shift-3).	RW	0x0
15:9	RESERVED		R	0x0
8:0	CFG_NL_HI_THR	This parameter is used by the peaking block. Threshold for the nonlinear peaking function. Must be nl_hi_thr.	RW	0x0

Table 9-291. Register Call Summary for Register VIP_CFG_SC22

VIP Functional Description • SC Functional Description: [0] [1] [2] • SC Code: [3]
VIP Register Manual • VIP SC Register Summary: [4] [6] [7]

Table 9-292. VIP_CFG_SC24

Address Offset	0x0000 0060		
Physical Address	0x4897 5860 0x4897 5D60 0x4899 5860 0x4899 5D60 0x489B 5860 0x489B 5D60	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc

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Table 9-292. VIP_CFG_SC24 (continued)

Description	
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_ORG_W								RESERVED								CFG_ORG_H							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	CFG_ORG_W	This parameter is used by the trimmer. Horizontal offset from the left of the original input image.	RW	0x0
15:11	RESERVED		R	0x0
10:0	CFG_ORG_H	This parameter is used by the trimmer. Vertical offset from the top of the original input image.	RW	0x0

Table 9-293. Register Call Summary for Register VIP_CFG_SC24

VIP Functional Description
- SC Functional Description: [0] [1]

VIP Register Manual
- VIP SC Register Summary: [2] [4] [5]

Table 9-294. VIP_CFG_SC25

Address Offset	0x0000 0064		
Physical Address	0x4897 5864 0x4897 5D64 0x4899 5864 0x4899 5D64 0x489B 5864 0x489B 5D64	**Instance**	VIP1_Slice0_sc VIP1_Slice1_sc VIP2_Slice0_sc VIP2_Slice1_sc VIP3_Slice0_sc VIP3_Slice1_sc
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CFG_OFF_W								RESERVED								CFG_OFF_H							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:16	CFG_OFF_W	This parameter is used by the trimmer. Horizontal offset from the left of the original input image.	RW	0x0
15:11	RESERVED		R	0x0
10:0	CFG_OFF_H	This parameter is used by the trimmer. Vertical offset from the top of the original input image.	RW	0x0

Table 9-295. Register Call Summary for Register VIP_CFG_SC25

VIP Functional Description
- SC Functional Description: [0] [1]

VIP Register Manual
- VIP SC Register Summary: [2] [4] [5]

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9.5.6 VIP VPDMA Registers

NOTE: The functionality of the following sets of registers is not supported by VIP VPDMA in this family of devices:

- All VIP_INT2_* registers
- All VIP_INT3_* registers

The following channels are not used by VIP VPDMA in this family of devices. All register bit-fields corresponding to these channels should be kept at their reset value.

- HQ_*
- GRPX_*
- SCALER_OUT
- SCALER_LUMA
- SCALER_CHROMA
- NF_*
- TRANSCODE1_*
- TRANSCODE2_*
- AUX_IN
- PIP_FRAME
- POST_COMP_WR
- VBI_SD_VENC

The following clients are not used by VIP VPDMA in this family of devices. All register bit-fields corresponding to these clients should be kept at their reset value.

- DEI_HQ_*
- TRANS1_LUMA
- TRANS1_CHROMA
- TRANS2_LUMA
- TRANS2_CHROMA
- HDMI_WRBK
- VBI_SDVENC
- NF_420_UV_OUT
- NF_420_Y_OUT
- NF_420_UV_IN
- NF_420_Y_IN
- NF_422_IN
- GRPX1_ST
- GRPX2_ST
- GRPX3_ST
- GRPX1_DATA
- GRPX2_DATA
- GRPX3_DATA
- PIP_WRBK
- SC_IN_*
- SC_OUT
- COMP_WRBK

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9.5.6.1 VIP VPDMA Register Summary

Table 9-296. VIP VPDMA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_VPDMA Base Address	VIP2_VPDMA Base Address	VIP3_VPDMA Base Address
VIP_PID	R	32	0x0000 0000	0x4897 D000	0x4899 D000	0x489B D000
VIP_LIST_ADDR	RW	32	0x0000 0004	0x4897 D004	0x4899 D004	0x489B D004
VIP_LIST_ATTR	RW	32	0x0000 0008	0x4897 D008	0x4899 D008	0x489B D008
VIP_LIST_STAT_SYNC	RW	32	0x0000 000C	0x4897 D00C	0x4899 D00C	0x489B D00C
VIP_BG_RGB	RW	32	0x0000 0018	0x4897 D018	0x4899 D018	0x489B D018
VIP_BG_YUV	RW	32	0x0000 001C	0x4897 D01C	0x4899 D01C	0x489B D01C
VIP_VPDMA_SETUP	RW	32	0x0000 0030	0x4897 D030	0x4899 D030	0x489B D030
VIP_MAX_SIZE1	RW	32	0x0000 0034	0x4897 D034	0x4899 D034	0x489B D034
VIP_MAX_SIZE2	RW	32	0x0000 0038	0x4897 D038	0x4899 D038	0x489B D038
VIP_MAX_SIZE3	RW	32	0x0000 003C	0x4897 D03C	0x4899 D03C	0x489B D03C
VIP_INT0_CHANNEL0_INT_STAT	RW	32	0x0000 0040	0x4897 D040	0x4899 D040	0x489B D040
VIP_INT0_CHANNEL0_INT_MASK	RW	32	0x0000 0044	0x4897 D044	0x4899 D044	0x489B D044
VIP_INT0_CHANNEL1_INT_STAT	RW	32	0x0000 0048	0x4897 D048	0x4899 D048	0x489B D048
VIP_INT0_CHANNEL1_INT_MASK	RW	32	0x0000 004C	0x4897 D04C	0x4899 D04C	0x489B D04C
VIP_INT0_CHANNEL2_INT_STAT	RW	32	0x0000 0050	0x4897 D050	0x4899 D050	0x489B D050
VIP_INT0_CHANNEL2_INT_MASK	RW	32	0x0000 0054	0x4897 D054	0x4899 D054	0x489B D054
VIP_INT0_CHANNEL3_INT_STAT	RW	32	0x0000 0058	0x4897 D058	0x4899 D058	0x489B D058
VIP_INT0_CHANNEL3_INT_MASK	RW	32	0x0000 005C	0x4897 D05C	0x4899 D05C	0x489B D05C
VIP_INT0_CHANNEL4_INT_STAT	RW	32	0x0000 0060	0x4897 D060	0x4899 D060	0x489B D060
VIP_INT0_CHANNEL4_INT_MASK	RW	32	0x0000 0064	0x4897 D064	0x4899 D064	0x489B D064
VIP_INT0_CHANNEL5_INT_STAT	RW	32	0x0000 0068	0x4897 D068	0x4899 D068	0x489B D068
VIP_INT0_CHANNEL5_INT_MASK	RW	32	0x0000 006C	0x4897 D06C	0x4899 D06C	0x489B D06C
VIP_INT0_CLIENT0_INT_STAT	RW	32	0x0000 0078	0x4897 D078	0x4899 D078	0x489B D078
VIP_INT0_CLIENT0_INT_MASK	RW	32	0x0000 007C	0x4897 D07C	0x4899 D07C	0x489B D07C
VIP_INT0_CLIENT1_INT_STAT	RW	32	0x0000 0080	0x4897 D080	0x4899 D080	0x489B D080
VIP_INT0_CLIENT1_INT_MASK	RW	32	0x0000 0084	0x4897 D084	0x4899 D084	0x489B D084
VIP_INT0_LIST0_INT_STAT	RW	32	0x0000 0088	0x4897 D088	0x4899 D088	0x489B D088
VIP_INT0_LIST0_INT_MASK	RW	32	0x0000 008C	0x4897 D08C	0x4899 D08C	0x489B D08C
VIP_INT1_CHANNEL0_INT_STAT	RW	32	0x0000 0090	0x4897 D090	0x4899 D090	0x489B D090
VIP_INT1_CHANNEL0_INT_MASK	RW	32	0x0000 0094	0x4897 D094	0x4899 D094	0x489B D094
VIP_INT1_CHANNEL1_INT_STAT	RW	32	0x0000 0098	0x4897 D098	0x4899 D098	0x489B D098
VIP_INT1_CHANNEL1_INT_MASK	RW	32	0x0000 009C	0x4897 D09C	0x4899 D09C	0x489B D09C
VIP_INT1_CHANNEL2_INT_STAT	RW	32	0x0000 00A0	0x4897 D0A0	0x4899 D0A0	0x489B D0A0
VIP_INT1_CHANNEL2_INT_MASK	RW	32	0x0000 00A4	0x4897 D0A4	0x4899 D0A4	0x489B D0A4
VIP_INT1_CHANNEL3_INT_STAT	RW	32	0x0000 00A8	0x4897 D0A8	0x4899 D0A8	0x489B D0A8
VIP_INT1_CHANNEL3_INT_MASK	RW	32	0x0000 00AC	0x4897 D0AC	0x4899 D0AC	0x489B D0AC
VIP_INT1_CHANNEL4_INT_STAT	RW	32	0x0000 00B0	0x4897 D0B0	0x4899 D0B0	0x489B D0B0
VIP_INT1_CHANNEL4_INT_MASK	RW	32	0x0000 00B4	0x4897 D0B4	0x4899 D0B4	0x489B D0B4
VIP_INT1_CHANNEL5_INT_STAT	RW	32	0x0000 00B8	0x4897 D0B8	0x4899 D0B8	0x489B D0B8
VIP_INT1_CHANNEL5_INT_MASK	RW	32	0x0000 00BC	0x4897 D0BC	0x4899 D0BC	0x489B D0BC
VIP_INT1_CLIENT0_INT_STAT	RW	32	0x0000 00C8	0x4897 D0C8	0x4899 D0C8	0x489B D0C8
VIP_INT1_CLIENT0_INT_MASK	RW	32	0x0000 00CC	0x4897 D0CC	0x4899 D0CC	0x489B D0CC
VIP_INT1_CLIENT1_INT_STAT	RW	32	0x0000 00D0	0x4897 D0D0	0x4899 D0D0	0x489B D0D0
VIP_INT1_CLIENT1_INT_MASK	RW	32	0x0000 00D4	0x4897 D0D4	0x4899 D0D4	0x489B D0D4
VIP_INT1_LIST0_INT_STAT	RW	32	0x0000 00D8	0x4897 D0D8	0x4899 D0D8	0x489B D0D8
VIP_INT1_LIST0_INT_MASK	RW	32	0x0000 00DC	0x4897 D0DC	0x4899 D0DC	0x489B D0DC
VIP_INT2_CHANNEL0_INT_STAT	RW	32	0x0000 00E0	0x4897 D0E0	0x4899 D0E0	0x489B D0E0
VIP_INT2_CHANNEL0_INT_MASK	RW	32	0x0000 00E4	0x4897 D0E4	0x4899 D0E4	0x489B D0E4

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Table 9-296. VIP VPDMA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_VPDMA Base Address	VIP2_VPDMA Base Address	VIP3_VPDMA Base Address
VIP_INT2_CHANNEL1_INT_STAT	RW	32	0x0000 00E8	0x4897 D0E8	0x4899 D0E8	0x489B D0E8
VIP_INT2_CHANNEL1_INT_MASK	RW	32	0x0000 00EC	0x4897 D0EC	0x4899 D0EC	0x489B D0EC
VIP_INT2_CHANNEL2_INT_STAT	RW	32	0x0000 00F0	0x4897 D0F0	0x4899 D0F0	0x489B D0F0
VIP_INT2_CHANNEL2_INT_MASK	RW	32	0x0000 00F4	0x4897 D0F4	0x4899 D0F4	0x489B D0F4
VIP_INT2_CHANNEL3_INT_STAT	RW	32	0x0000 00F8	0x4897 D0F8	0x4899 D0F8	0x489B D0F8
VIP_INT2_CHANNEL3_INT_MASK	RW	32	0x0000 00FC	0x4897 D0FC	0x4899 D0FC	0x489B D0FC
VIP_INT2_CHANNEL4_INT_STAT	RW	32	0x0000 0100	0x4897 D100	0x4899 D100	0x489B D100
VIP_INT2_CHANNEL4_INT_MASK	RW	32	0x0000 0104	0x4897 D104	0x4899 D104	0x489B D104
VIP_INT2_CHANNEL5_INT_STAT	RW	32	0x0000 0108	0x4897 D108	0x4899 D108	0x489B D108
VIP_INT2_CHANNEL5_INT_MASK	RW	32	0x0000 010C	0x4897 D10C	0x4899 D10C	0x489B D10C
VIP_INT2_CLIENT0_INT_STAT	RW	32	0x0000 0118	0x4897 D118	0x4899 D118	0x489B D118
VIP_INT2_CLIENT0_INT_MASK	RW	32	0x0000 011C	0x4897 D11C	0x4899 D11C	0x489B D11C
VIP_INT2_LIST0_INT_STAT	RW	32	0x0000 0128	0x4897 D128	0x4899 D128	0x489B D128
VIP_INT2_LIST0_INT_MASK	RW	32	0x0000 012C	0x4897 D12C	0x4899 D12C	0x489B D12C
VIP_INT3_CHANNEL0_INT_STAT	RW	32	0x0000 0130	0x4897 D130	0x4899 D130	0x489B D130
VIP_INT3_CHANNEL0_INT_MASK	RW	32	0x0000 0134	0x4897 D134	0x4899 D134	0x489B D134
VIP_INT3_CHANNEL1_INT_STAT	RW	32	0x0000 0138	0x4897 D138	0x4899 D138	0x489B D138
VIP_INT3_CHANNEL1_INT_MASK	RW	32	0x0000 013C	0x4897 D13C	0x4899 D13C	0x489B D13C
VIP_INT3_CHANNEL2_INT_STAT	RW	32	0x0000 0140	0x4897 D140	0x4899 D140	0x489B D140
VIP_INT3_CHANNEL2_INT_MASK	RW	32	0x0000 0144	0x4897 D144	0x4899 D144	0x489B D144
VIP_INT3_CHANNEL3_INT_STAT	RW	32	0x0000 0148	0x4897 D148	0x4899 D148	0x489B D148
VIP_INT3_CHANNEL3_INT_MASK	RW	32	0x0000 014C	0x4897 D14C	0x4899 D14C	0x489B D14C
VIP_INT3_CHANNEL4_INT_STAT	RW	32	0x0000 0150	0x4897 D150	0x4899 D150	0x489B D150
VIP_INT3_CHANNEL4_INT_MASK	RW	32	0x0000 0154	0x4897 D154	0x4899 D154	0x489B D154
VIP_INT3_CHANNEL5_INT_STAT	RW	32	0x0000 0158	0x4897 D158	0x4899 D158	0x489B D158
VIP_INT3_CHANNEL5_INT_MASK	RW	32	0x0000 015C	0x4897 D15C	0x4899 D15C	0x489B D15C
VIP_INT3_CLIENT0_INT_STAT	RW	32	0x0000 0168	0x4897 D168	0x4899 D168	0x489B D168
VIP_INT3_CLIENT0_INT_MASK	RW	32	0x0000 016C	0x4897 D16C	0x4899 D16C	0x489B D16C
VIP_INT3_LIST0_INT_STAT	RW	32	0x0000 0178	0x4897 D178	0x4899 D178	0x489B D178
VIP_INT3_LIST0_INT_MASK	RW	32	0x0000 017C	0x4897 D17C	0x4899 D17C	0x489B D17C
VIP_PERF_MON0	RW	32	0x0000 0200	0x4897 D200	0x4899 D200	0x489B D200
VIP_PERF_MON1	RW	32	0x0000 0204	0x4897 D204	0x4899 D204	0x489B D204
VIP_PERF_MON2	RW	32	0x0000 0208	0x4897 D208	0x4899 D208	0x489B D208
VIP_PERF_MON3	RW	32	0x0000 020C	0x4897 D20C	0x4899 D20C	0x489B D20C
VIP_PERF_MON4	RW	32	0x0000 0210	0x4897 D210	0x4899 D210	0x489B D210
VIP_PERF_MON5	RW	32	0x0000 0214	0x4897 D214	0x4899 D214	0x489B D214
VIP_PERF_MON6	RW	32	0x0000 0218	0x4897 D218	0x4899 D218	0x489B D218
VIP_PERF_MON7	RW	32	0x0000 021C	0x4897 D21C	0x4899 D21C	0x489B D21C
VIP_PERF_MON8	RW	32	0x0000 0220	0x4897 D220	0x4899 D220	0x489B D220
VIP_PERF_MON9	RW	32	0x0000 0224	0x4897 D224	0x4899 D224	0x489B D224
VIP_PERF_MON10	RW	32	0x0000 0228	0x4897 D228	0x4899 D228	0x489B D228
VIP_PERF_MON11	RW	32	0x0000 022C	0x4897 D22C	0x4899 D22C	0x489B D22C
VIP_PERF_MON12	RW	32	0x0000 0230	0x4897 D230	0x4899 D230	0x489B D230
VIP_PERF_MON13	RW	32	0x0000 0234	0x4897 D234	0x4899 D234	0x489B D234
VIP_PERF_MON14	RW	32	0x0000 0238	0x4897 D238	0x4899 D238	0x489B D238
VIP_PERF_MON15	RW	32	0x0000 023C	0x4897 D23C	0x4899 D23C	0x489B D23C
VIP_PERF_MON16	RW	32	0x0000 0240	0x4897 D240	0x4899 D240	0x489B D240
VIP_PERF_MON17	RW	32	0x0000 0244	0x4897 D244	0x4899 D244	0x489B D244
VIP_PERF_MON18	RW	32	0x0000 0248	0x4897 D248	0x4899 D248	0x489B D248
VIP_PERF_MON19	RW	32	0x0000 024C	0x4897 D24C	0x4899 D24C	0x489B D24C

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Table 9-296. VIP VPDMA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_VPDMA Base Address	VIP2_VPDMA Base Address	VIP3_VPDMA Base Address
VIP_PERF_MON20	RW	32	0x0000 0250	0x4897 D250	0x4899 D250	0x489B D250
VIP_PERF_MON21	RW	32	0x0000 0254	0x4897 D254	0x4899 D254	0x489B D254
VIP_PERF_MON22	RW	32	0x0000 0258	0x4897 D258	0x4899 D258	0x489B D258
VIP_PERF_MON23	RW	32	0x0000 025C	0x4897 D25C	0x4899 D25C	0x489B D25C
VIP_PERF_MON24	RW	32	0x0000 0260	0x4897 D260	0x4899 D260	0x489B D260
VIP_PERF_MON25	RW	32	0x0000 0264	0x4897 D264	0x4899 D264	0x489B D264
VIP_PERF_MON26	RW	32	0x0000 0268	0x4897 D268	0x4899 D268	0x489B D268
VIP_PERF_MON27	RW	32	0x0000 026C	0x4897 D26C	0x4899 D26C	0x489B D26C
VIP_PERF_MON28	RW	32	0x0000 0270	0x4897 D270	0x4899 D270	0x489B D270
VIP_PERF_MON29	RW	32	0x0000 0274	0x4897 D274	0x4899 D274	0x489B D274
VIP_PERF_MON30	RW	32	0x0000 0278	0x4897 D278	0x4899 D278	0x489B D278
VIP_PERF_MON31	RW	32	0x0000 027C	0x4897 D27C	0x4899 D27C	0x489B D27C
VIP_PERF_MON32	RW	32	0x0000 0280	0x4897 D280	0x4899 D280	0x489B D280
VIP_PERF_MON33	RW	32	0x0000 0284	0x4897 D284	0x4899 D284	0x489B D284
VIP_PERF_MON34	RW	32	0x0000 0288	0x4897 D288	0x4899 D288	0x489B D288
VIP_PERF_MON35	RW	32	0x0000 028C	0x4897 D28C	0x4899 D28C	0x489B D28C
VIP_PERF_MON36	RW	32	0x0000 0290	0x4897 D290	0x4899 D290	0x489B D290
VIP_PERF_MON37	RW	32	0x0000 0294	0x4897 D294	0x4899 D294	0x489B D294
VIP_PERF_MON38	RW	32	0x0000 0298	0x4897 D298	0x4899 D298	0x489B D298
VIP_PERF_MON39	RW	32	0x0000 029C	0x4897 D29C	0x4899 D29C	0x489B D29C
VIP_PERF_MON40	RW	32	0x0000 02A0	0x4897 D2A0	0x4899 D2A0	0x489B D2A0
VIP_PERF_MON41	RW	32	0x0000 02A4	0x4897 D2A4	0x4899 D2A4	0x489B D2A4
VIP_PERF_MON42	RW	32	0x0000 02A8	0x4897 D2A8	0x4899 D2A8	0x489B D2A8
VIP_PERF_MON43	RW	32	0x0000 02AC	0x4897 D2AC	0x4899 D2AC	0x489B D2AC
VIP_PERF_MON44	RW	32	0x0000 02B0	0x4897 D2B0	0x4899 D2B0	0x489B D2B0
VIP_PERF_MON45	RW	32	0x0000 02B4	0x4897 D2B4	0x4899 D2B4	0x489B D2B4
VIP_PERF_MON46	RW	32	0x0000 02B8	0x4897 D2B8	0x4899 D2B8	0x489B D2B8
VIP_PERF_MON47	RW	32	0x0000 02BC	0x4897 D2BC	0x4899 D2BC	0x489B D2BC
VIP_PERF_MON48	RW	32	0x0000 02C0	0x4897 D2C0	0x4899 D2C0	0x489B D2C0
VIP_PERF_MON49	RW	32	0x0000 02C4	0x4897 D2C4	0x4899 D2C4	0x489B D2C4
VIP_PERF_MON50	RW	32	0x0000 02C8	0x4897 D2C8	0x4899 D2C8	0x489B D2C8
VIP_PERF_MON51	RW	32	0x0000 02CC	0x4897 D2CC	0x4899 D2CC	0x489B D2CC
VIP_PERF_MON52	RW	32	0x0000 02D0	0x4897 D2D0	0x4899 D2D0	0x489B D2D0
VIP_PERF_MON53	RW	32	0x0000 02D4	0x4897 D2D4	0x4899 D2D4	0x489B D2D4
VIP_PERF_MON54	RW	32	0x0000 02D8	0x4897 D2D8	0x4899 D2D8	0x489B D2D8
VIP_PERF_MON55	RW	32	0x0000 02DC	0x4897 D2DC	0x4899 D2DC	0x489B D2DC
VIP_PERF_MON56	RW	32	0x0000 02E0	0x4897 D2E0	0x4899 D2E0	0x489B D2E0
VIP_PERF_MON57	RW	32	0x0000 02E4	0x4897 D2E4	0x4899 D2E4	0x489B D2E4
VIP_PERF_MON58	RW	32	0x0000 02E8	0x4897 D2E8	0x4899 D2E8	0x489B D2E8
VIP_PERF_MON59	RW	32	0x0000 02EC	0x4897 D2EC	0x4899 D2EC	0x489B D2EC
VIP_PERF_MON60	RW	32	0x0000 02F0	0x4897 D2F0	0x4899 D2F0	0x489B D2F0
VIP_PERF_MON61	RW	32	0x0000 02F4	0x4897 D2F4	0x4899 D2F4	0x489B D2F4
VIP0_LO_Y_CSTAT	RW	32	0x0000 0388	0x4897 D388	0x4899 D388	0x489B D388
VIP0_LO_UV_CSTAT	RW	32	0x0000 038C	0x4897 D38C	0x4899 D38C	0x489B D38C
VIP0_UP_Y_CSTAT	RW	32	0x0000 0390	0x4897 D390	0x4899 D390	0x489B D390
VIP0_UP_UV_CSTAT	RW	32	0x0000 0394	0x4897 D394	0x4899 D394	0x489B D394
VIP1_LO_Y_CSTAT	RW	32	0x0000 0398	0x4897 D398	0x4899 D398	0x489B D398
VIP1_LO_UV_CSTAT	RW	32	0x0000 039C	0x4897 D39C	0x4899 D39C	0x489B D39C
VIP1_UP_Y_CSTAT	RW	32	0x0000 03A0	0x4897 D3A0	0x4899 D3A0	0x489B D3A0
VIP1_UP_UV_CSTAT	RW	32	0x0000 03A4	0x4897 D3A4	0x4899 D3A4	0x489B D3A4

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Table 9-296. VIP VPDMA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_VPDMA Base Address	VIP2_VPDMA Base Address	VIP3_VPDMA Base Address
VPI_CTL_CSTAT	RW	32	0x0000 03D0	0x4897 D3D0	0x4899 D3D0	0x489B D3D0
VIP0_ANC_A_CSTAT	RW	32	0x0000 03E8	0x4897 D3E8	0x4899 D3E8	0x489B D3E8
VIP0_ANC_B_CSTAT	RW	32	0x0000 03EC	0x4897 D3EC	0x4899 D3EC	0x489B D3EC
VIP1_ANC_A_CSTAT	RW	32	0x0000 03F0	0x4897 D3F0	0x4899 D3F0	0x489B D3F0
VIP1_ANC_B_CSTAT	RW	32	0x0000 03F4	0x4897 D3F4	0x4899 D3F4	0x489B D3F4

9.5.6.2 VIP VPDMA Register Description

Table 9-297. VIP_PID

Address Offset	0x0000 0000		
Physical Address	0x4897 D000 0x4899 D000 0x489B D000	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	PID VIP VPDMA register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID																															

Bits	Field Name	Description	Type	Reset
31:0	PID	PID of VPDMA module	R	0x0

Table 9-298. Register Call Summary for Register VIP_PID

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-299. VIP_LIST_ADDR

Address Offset	0x0000 0004		
Physical Address	0x4897 D004 0x4899 D004 0x489B D004	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The location of a new list to begin processing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
31:0	VIP_LIST_ADDR	Location of a new list of descriptors. This register must be written with the VPDMA Configuration Location after reset.	RW	0x0

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Table 9-300. Register Call Summary for Register VIP_LIST_ADDR

VIP Functional Description
- VPDMA Introduction:
- VPDMA Basic Definitions: [1] [2]
- VPDMA Configuration: [3] [4] [5]

VIP Register Manual
- VIP VPDMA Register Summary: [6]
- VIP VPDMA Register Description: [9] [10] [11] [12]

Table 9-301. VIP_LIST_ATTR

Address Offset	0x0000 0008		
Physical Address	0x4897 D008 0x4899 D008 0x489B D008	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The attributes of a new list. This register should always be written after VIP_LIST_ADDR.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LIST_NUM			RESERVED			STOP	RDY	LIST_TYPE			LIST_SIZE																

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0
26:24	LIST_NUM	The list number that should be assigned to the list located at VIP_LIST_ADDR. If the list is still active this will block all future list writes until the list is available.	RW	0x0
23:21	RESERVED		R	0x0
20	STOP	This bit is written with the LIST_NUMBER field to stop a self-modifying list. When this bit is written a one the list specified by the LIST_NUMBER is sent a stop signal and will finish the current frame of transfers and then free the list resources.	RW	0x0
19	RDY	This bit is low when a new list cannot be written to the VIP_LIST_ADDR register. The reasons this bit would be low are at initial startup if the LIST_MANAGER State Machine image has not completed loading. It also would be low if the last write to the VIP_LIST_ATTR attempted to start a list that is currently active. When this bit is low any writes to the list address register will cause access to not be accepted until this bit has set by the previous list having completed.	R	0x0
18:16	LIST_TYPE	The type of list that has been generated.\\n0: Normal List\\n1: Self-Modifying List\\n2: List Doorbell\\nOthers Reserved for future use	RW	0x0
15:0	LIST_SIZE	Number of 128 bit word in the new list of descriptors. Writes to this register will activate the list in the list stack of the list manager and begin transfer of the list into VPDMA. This size can not be 0.	RW	0x0

Table 9-302. Register Call Summary for Register VIP_LIST_ATTR

VIP Functional Description
- VPDMA Introduction:
- VPDMA Basic Definitions: [2] [3]
- VPDMA Configuration: [4] [5] [6] [7]

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Table 9-302. Register Call Summary for Register VIP_LIST_ATTR (continued)

VIP Register Manual

- VIP VPDMA Register Summary: [8]
- VIP VPDMA Register Description: [11]

Table 9-303. VIP_LIST_STAT_SYNC

Address Offset	0x0000 000C		
Physical Address	0x4897 D00C 0x4899 D00C 0x489B D00C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register is used for processor to List Manager syncronization and status registers for the list.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LIST7_BUSY	LIST6_BUSY	LIST5_BUSY	LIST4_BUSY	LIST3_BUSY	LIST2_BUSY	LIST1_BUSY	LIST0_BUSY	RESERVED								SYNC_LISTS7	SYNC_LISTS6	SYNC_LISTS5	SYNC_LISTS4	SYNC_LISTS3	SYNC_LISTS2	SYNC_LISTS1	SYNC_LISTS0

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x0
23	LIST7_BUSY	The list 7 is currently running. Any attempt to load a new list to list 7 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
22	LIST6_BUSY	The list 6 is currently running. Any attempt to load a new list to list 6 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
21	LIST5_BUSY	The list 5 is currently running. Any attempt to load a new list to list 5 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
20	LIST4_BUSY	The list 4 is currently running. Any attempt to load a new list to list 4 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
19	LIST3_BUSY	The list 3 is currently running. Any attempt to load a new list to list 3 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
18	LIST2_BUSY	The list 2 is currently running. Any attempt to load a new list to list 2 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
17	LIST1_BUSY	The list 1 is currently running. Any attempt to load a new list to list 1 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
16	LIST0_BUSY	The list 0 is currently running. Any attempt to load a new list to list 0 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.	R	0x0
15:8	RESERVED	Reserved	R	0x0
7	SYNC_LISTS7	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 7 waiting on it.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	SYNC_LISTS6	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 6 waiting on it.	RW	0x0
5	SYNC_LISTS5	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 5 waiting on it.	RW	0x0
4	SYNC_LISTS4	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 4 waiting on it.	RW	0x0
3	SYNC_LISTS3	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 3 waiting on it.	RW	0x0
2	SYNC_LISTS2	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 2 waiting on it.	RW	0x0
1	SYNC_LISTS1	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 1 waiting on it.	RW	0x0
0	SYNC_LISTS0	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 0 waiting on it.	RW	0x0

Table 9-304. Register Call Summary for Register VIP_LIST_STAT_SYNC

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-305. VIP_BG_RGB

Address Offset	0x0000 0018		
Physical Address	0x4897 D018 0x4899 D018 0x489B D018	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The registers used to set the background color for RGB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED								GREEN								BLUE								BLEND							

Bits	Field Name	Description	Type	Reset
31:24	RED	The red value to give on an RGB data port for a blank pixel when using virtual video buffering	RW	0x0
23:16	GREEN	The green value to give on an RGB data port for a blank pixel when using virtual video buffering	RW	0x0
15:8	BLUE	The blue value to give on an RGB data port for a blank pixel when using virtual video buffering	RW	0x0
7:0	BLEND	The blend value to give on an RGB data port for a blank pixel when using virtual video buffering	RW	0x0

Table 9-306. Register Call Summary for Register VIP_BG_RGB

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-307. VIP_BG_YUV

Address Offset	0x0000 001C		
Physical Address	0x4897 D01C 0x4899 D01C 0x489B D01C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The registers used to set the background color for YUV		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								Y								CR								CB							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x0
23:16	Y	The Y value to give on a YUV data port for a blank pixel when using virtual video buffering	RW	0x0
15:8	CR	The Cr value to give on a YUV data port for a blank pixel when using virtual video buffering	RW	0x0
7:0	CB	The Cb value to give on a YUV data port for a blank pixel when using virtual video buffering	RW	0x0

Table 9-308. Register Call Summary for Register VIP_BG_YUV

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-309. VIP_VPDMA_SETUP

Address Offset	0x0000 0030		
Physical Address	0x4897 D030 0x4899 D030 0x489B D030	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	Configures global parameters that are shared by all clients.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SEC_BASE_CH

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0
0	SEC_BASE_CH	Use Secondary Channels for Mosaic mode	RW	0x0

Table 9-310. Register Call Summary for Register VIP_VPDMA_SETUP

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-311. VIP_MAX_SIZE1

Address Offset	0x0000 0034		
Physical Address	0x4897 D034 0x4899 D034 0x489B D034	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	Configures maximum width and maximum height global parameters that are shared by all clients to allow for configurable max width and max height when setting is 1 in write descriptor.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_WIDTH																MAX_HEIGHT															

Bits	Field Name	Description	Type	Reset
31:16	MAX_WIDTH	The maximum width to use for setting of max_width 1 in a write descriptor. The value is the number of pixels + 1 so if 1024 pixels are required then set the value to 1023.	RW	0x0
15:0	MAX_HEIGHT	The maximum height to use for setting of max_height 1 in a write descriptor. The value is the number of lines + 1 so if 1024 lines are required then set the value to 1023.	RW	0x0

Table 9-312. Register Call Summary for Register VIP_MAX_SIZE1

VIP Functional Description
- VPDMA Descriptors: [0] [1]

VIP Register Manual
- VIP VPDMA Register Summary: [2]

Table 9-313. VIP_MAX_SIZE2

Address Offset	0x0000 0038		
Physical Address	0x4897 D038 0x4899 D038 0x489B D038	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	Configures maximum width and maximum height global parameters that are shared by all clients to allow for configurable max width and max height when setting is 2 in write descriptor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_WIDTH																MAX_HEIGHT															

Bits	Field Name	Description	Type	Reset
31:16	MAX_WIDTH	The maximum width to use for setting of max_width 2 in a write descriptor. The value is the number of pixels + 1 so if 1024 pixels are required then set the value to 1023.	RW	0x0
15:0	MAX_HEIGHT	The maximum height to use for setting of max_height 2 in a write descriptor. The value is the number of lines + 1 so if 1024 lines are required then set the value to 1023.	RW	0x0

Table 9-314. Register Call Summary for Register VIP_MAX_SIZE2

VIP Functional Description
- VPDMA Descriptors: [0] [1]

VIP Register Manual
- VIP VPDMA Register Summary: [2]

Table 9-315. VIP_MAX_SIZE3

Address Offset	0x0000 003C		
Physical Address	0x4897 D03C 0x4899 D03C 0x489B D03C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	Configures maximum width and maximum height global parameters that are shared by all clients to allow for configurable max width and max height when setting is 3 in write descriptor.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_WIDTH																MAX_HEIGHT															

Bits	Field Name	Description	Type	Reset
31:16	MAX_WIDTH	The maximum width to use for setting of max_width 3 in a write descriptor. The value is the number of pixels + 1 so if 1024 pixels are required then set the value to 1023.	RW	0x0
15:0	MAX_HEIGHT	The maximum height to use for setting of max_height 3 in a write descriptor. The value is the number of lines + 1 so if 1024 lines are required then set the value to 1023.	RW	0x0

Table 9-316. Register Call Summary for Register VIP_MAX_SIZE3

VIP Functional Description
- VPDMA Descriptors: [0] [1]

VIP Register Manual
- VIP VPDMA Register Summary: [2]

Table 9-317. VIP_INT0_CHANNEL0_INT_STAT

Address Offset	0x0000 0040		
Physical Address	0x4897 D040 0x4899 D040 0x489B D040	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_GRPX3	INT_STAT_GRPX2	INT_STAT_GRPX1	INT_STAT_SCALER_OUT	RESERVED								INT_STAT_SCALER_CHROMA	INT_STAT_SCALER_LUMA	INT_STAT_HQ_SCALER	RESERVED	INT_STAT_HQ_MV_OUT	RESERVED		INT_STAT_HQ_MV	RESERVED				INT_STAT_HQ_VID3_CHROMA	INT_STAT_HQ_VID3_LUMA	INT_STAT_HQ_VID2_CHROMA	INT_STAT_HQ_VID2_LUMA	INT_STAT_HQ_VID1_CHROMA	INT_STAT_HQ_VID1_LUMA		

Bits	Field Name	Description	Type	Reset
31	INT_STAT_GRPX3	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_GRPX2	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
29	INT_STAT_GRPX1	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_SCALER_OUT	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value	RW	0x0
27:20	RESERVED	Reserved	R	0x00
19	INT_STAT_SCALER_CHROMA	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_SCALER_LUMA	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_HQ_SCALER	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_STAT_HQ_MV_OUT	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_STAT_HQ_MV	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_STAT_HQ_VID3_CHROMA	The last write DMA transaction has completed for channel hq_vid3_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	INT_STAT_HQ_VID3_LUMA	The last write DMA transaction has completed for channel hq_vid3_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_HQ_VID2_CHROMA	The last write DMA transaction has completed for channel hq_vid2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_HQ_VID2_LUMA	The last write DMA transaction has completed for channel hq_vid2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_HQ_VID1_CHROMA	The last write DMA transaction has completed for channel hq_vid1_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_HQ_VID1_LUMA	The last write DMA transaction has completed for channel hq_vid1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-318. Register Call Summary for Register VIP_INT0_CHANNEL0_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-319. VIP_INT0_CHANNEL0_INT_MASK

Address Offset	0x0000 0044		
Physical Address	0x4897 D044 0x4899 D044 0x489B D044	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_GRPX3	INT_MASK_GRPX2	INT_MASK_GRPX1	INT_MASK_SCALER_OUT	RESERVED								INT_MASK_SCALER_CHROMA	INT_MASK_SCALER_LUMA	INT_MASK_HQ_SCALER	RESERVED	INT_MASK_HQ_MV_OUT	RESERVED		INT_MASK_HQ_MV	RESERVED				INT_MASK_HQ_VID3_CHROMA	INT_MASK_HQ_VID3_LUMA	INT_MASK_HQ_VID2_CHROMA	INT_MASK_HQ_VID2_LUMA	INT_MASK_HQ_VID1_CHROMA	INT_MASK_HQ_VID1_LUMA		

Bits	Field Name	Description	Type	Reset
31	INT_MASK_GRPX3	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_GRPX2	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_GRPX1	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_SCALER_OUT	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27:20	RESERVED	Reserved	R	0x00
19	INT_MASK_SCALER_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_SCALER_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_HQ_SCALER	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_MASK_HQ_MV_OUT	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_MASK_HQ_MV	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_MASK_HQ_VID3_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_HQ_VID3_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_HQ_VID2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_HQ_VID2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
1	INT_MASK_HQ_VID1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_HQ_VID1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-320. Register Call Summary for Register VIP_INT0_CHANNEL0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-321. VIP_INT0_CHANNEL1_INT_STAT

Address Offset	0x0000 0048		
Physical Address	0x4897 D048 0x4899 D048 0x489B D048	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2	INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10	INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2	INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	RESERVED						

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP1_MULT_PORTB_SRC9	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP1_MULT_PORTB_SRC8	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
29	INT_STAT_VIP1_MULT_PORTB_SRC7	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP1_MULT_PORTB_SRC6	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP1_MULT_PORTB_SRC5	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP1_MULT_PORTB_SRC4	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP1_MULT_PORTB_SRC3	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP1_MULT_PORTB_SRC2	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP1_MULT_PORTB_SRC1	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP1_MULT_PORTB_SRC0	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP1_MULT_PORTA_SRC15	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
20	INT_STAT_VIP1_MULT_PORTA_SRC14	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP1_MULT_PORTA_SRC13	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP1_MULT_PORTA_SRC12	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP1_MULT_PORTA_SRC11	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP1_MULT_PORTA_SRC10	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP1_MULT_PORTA_SRC9	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP1_MULT_PORTA_SRC8	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP1_MULT_PORTA_SRC7	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP1_MULT_PORTA_SRC6	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	INT_STAT_VIP1_MULT_PORTA_SRC5	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_MULT_PORTA_SRC4	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_MULT_PORTA_SRC3	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP1_MULT_PORTA_SRC2	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_MULT_PORTA_SRC1	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP1_MULT_PORTA_SRC0	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5:0	RESERVED	Reserved	R	0x00

Table 9-322. Register Call Summary for Register VIP_INT0_CHANNEL1_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-323. VIP_INT0_CHANNEL1_INT_MASK

Address Offset	0x0000 004C		
Physical Address	0x4897 D04C 0x4899 D04C 0x489B D04C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2	INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10	INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2	INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	RESERVED						

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP1_MULT_PORTB_SRC9	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP1_MULT_PORTB_SRC8	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP1_MULT_PORTB_SRC7	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP1_MULT_PORTB_SRC6	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP1_MULT_PORTB_SRC5	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP1_MULT_PORTB_SRC4	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP1_MULT_PORTB_SRC3	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP1_MULT_PORTB_SRC2	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP1_MULT_PORTB_SRC1	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP1_MULT_PORTB_SRC0	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP1_MULT_PORTA_SRC15	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP1_MULT_PORTA_SRC14	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP1_MULT_PORTA_SRC13	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP1_MULT_PORTA_SRC12	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP1_MULT_PORTA_SRC11	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
16	INT_MASK_VIP1_MULT_PORTA_SRC10	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP1_MULT_PORTA_SRC9	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP1_MULT_PORTA_SRC8	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP1_MULT_PORTA_SRC7	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP1_MULT_PORTA_SRC6	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP1_MULT_PORTA_SRC5	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_MULT_PORTA_SRC4	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_MULT_PORTA_SRC3	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_MULT_PORTA_SRC2	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_MULT_PORTA_SRC1	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_MULT_PORTA_SRC0	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5:0	RESERVED	Reserved	R	0x00

Table 9-324. Register Call Summary for Register VIP_INT0_CHANNEL1_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-325. VIP_INT0_CHANNEL2_INT_STAT

Address Offset	0x0000 0050		
Physical Address	0x4897 D050 0x4899 D050 0x489B D050	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2	INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10	INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2	INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP1_MULT_ANCB_SRC9	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP1_MULT_ANCB_SRC8	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP1_MULT_ANCB_SRC7	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP1_MULT_ANCB_SRC6	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP1_MULT_ANCB_SRC5	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP1_MULT_ANCB_SRC4	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP1_MULT_ANCB_SRC3	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
24	INT_STAT_VIP1_MULT_ANCB_SRC2	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP1_MULT_ANCB_SRC1	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP1_MULT_ANCB_SRC0	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP1_MULT_ANCA_SRC15	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP1_MULT_ANCA_SRC14	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP1_MULT_ANCA_SRC13	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP1_MULT_ANCA_SRC12	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP1_MULT_ANCA_SRC11	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP1_MULT_ANCA_SRC10	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	INT_STAT_VIP1_MULT_ANCA_SRC9	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP1_MULT_ANCA_SRC8	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP1_MULT_ANCA_SRC7	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP1_MULT_ANCA_SRC6	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP1_MULT_ANCA_SRC5	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_MULT_ANCA_SRC4	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_MULT_ANCA_SRC3	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP1_MULT_ANCA_SRC2	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_MULT_ANCA_SRC1	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	INT_STAT_VIP1_MULT_ANCA_SRC0	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP1_MULT_PORTB_SRC15	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP1_MULT_PORTB_SRC14	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP1_MULT_PORTB_SRC13	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP1_MULT_PORTB_SRC12	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP1_MULT_PORTB_SRC11	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP1_MULT_PORTB_SRC10	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-326. Register Call Summary for Register VIP_INT0_CHANNEL2_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-327. VIP_INT0_CHANNEL2_INT_MASK

Address Offset	0x0000 0054		
Physical Address	0x4897 D054 0x4899 D054 0x489B D054	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		

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Table 9-327. VIP_INT0_CHANNEL2_INT_MASK (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2	INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10	INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2	INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP1_MULT_ANCB_SRC9	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP1_MULT_ANCB_SRC8	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP1_MULT_ANCB_SRC7	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP1_MULT_ANCB_SRC6	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP1_MULT_ANCB_SRC5	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP1_MULT_ANCB_SRC4	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP1_MULT_ANCB_SRC3	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP1_MULT_ANCB_SRC2	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP1_MULT_ANCB_SRC1	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP1_MULT_ANCB_SRC0	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
21	INT_MASK_VIP1_MULT_ANCA_SRC15	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP1_MULT_ANCA_SRC14	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP1_MULT_ANCA_SRC13	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP1_MULT_ANCA_SRC12	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP1_MULT_ANCA_SRC11	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP1_MULT_ANCA_SRC10	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP1_MULT_ANCA_SRC9	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP1_MULT_ANCA_SRC8	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP1_MULT_ANCA_SRC7	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP1_MULT_ANCA_SRC6	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP1_MULT_ANCA_SRC5	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_MULT_ANCA_SRC4	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_MULT_ANCA_SRC3	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_MULT_ANCA_SRC2	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_MULT_ANCA_SRC1	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_MULT_ANCA_SRC0	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
5	INT_MASK_VIP1_MULT_PORTB_SRC15	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP1_MULT_PORTB_SRC14	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP1_MULT_PORTB_SRC13	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP1_MULT_PORTB_SRC12	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP1_MULT_PORTB_SRC11	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP1_MULT_PORTB_SRC10	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-328. Register Call Summary for Register VIP_INT0_CHANNEL2_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-329. VIP_INT0_CHANNEL3_INT_STAT

Address Offset	0x0000 0058		
Physical Address	0x4897 D058 0x4899 D058 0x489B D058	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12	INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4	INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA	INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10

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Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP2_MULT_PORTB_SRC3	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP2_MULT_PORTB_SRC2	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP2_MULT_PORTB_SRC1	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP2_MULT_PORTB_SRC0	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP2_MULT_PORTA_SRC15	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP2_MULT_PORTA_SRC14	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP2_MULT_PORTA_SRC13	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP2_MULT_PORTA_SRC12	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP2_MULT_PORTA_SRC11	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	INT_STAT_VIP2_MULT_PORTA_SRC10	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP2_MULT_PORTA_SRC9	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP2_MULT_PORTA_SRC8	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP2_MULT_PORTA_SRC7	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP2_MULT_PORTA_SRC6	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_MULT_PORTA_SRC5	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_MULT_PORTA_SRC4	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP2_MULT_PORTA_SRC3	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_MULT_PORTA_SRC2	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
13	INT_STAT_VIP2_MULT_PORTA_SRC1	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP2_MULT_PORTA_SRC0	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP1_PORTB_RGB	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_PORTA_RGB	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_PORTB_CHROMA	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP1_PORTB_LUMA	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_PORTA_CHROMA	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP1_PORTA_LUMA	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP1_MULT_ANCB_SRC15	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	INT_STAT_VIP1_MULT_ANCB_SRC14	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP1_MULT_ANCB_SRC13	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP1_MULT_ANCB_SRC12	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP1_MULT_ANCB_SRC11	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP1_MULT_ANCB_SRC10	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-330. Register Call Summary for Register VIP_INT0_CHANNEL3_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-331. VIP_INT0_CHANNEL3_INT_MASK

Address Offset	0x0000 005C		
Physical Address	0x4897 D05C 0x4899 D05C 0x489B D05C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12	INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4	INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA	INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP2_MULT_PORTB_SRC3	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP2_MULT_PORTB_SRC2	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP2_MULT_PORTB_SRC1	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP2_MULT_PORTB_SRC0	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP2_MULT_PORTA_SRC15	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP2_MULT_PORTA_SRC14	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP2_MULT_PORTA_SRC13	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP2_MULT_PORTA_SRC12	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP2_MULT_PORTA_SRC11	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP2_MULT_PORTA_SRC10	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP2_MULT_PORTA_SRC9	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP2_MULT_PORTA_SRC8	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP2_MULT_PORTA_SRC7	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP2_MULT_PORTA_SRC6	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_MULT_PORTA_SRC5	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
16	INT_MASK_VIP2_MULT_PORTA_SRC4	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_MULT_PORTA_SRC3	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_MULT_PORTA_SRC2	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_MULT_PORTA_SRC1	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_MULT_PORTA_SRC0	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP1_PORTB_RGB	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_PORTA_RGB	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_PORTB_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_PORTB_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_PORTA_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_PORTA_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP1_MULT_ANCB_SRC15	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP1_MULT_ANCB_SRC14	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP1_MULT_ANCB_SRC13	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP1_MULT_ANCB_SRC12	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP1_MULT_ANCB_SRC11	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP1_MULT_ANCB_SRC10	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Table 9-332. Register Call Summary for Register VIP_INT0_CHANNEL3_INT_MASK

VIP Functional Description

- VPDMA Interrupts: [0]

VIP Register Manual

- VIP VPDMA Register Summary: [1]

Table 9-333. VIP_INT0_CHANNEL4_INT_STAT

Address Offset	0x0000 0060		
Physical Address	0x4897 D060 0x4899 D060 0x489B D060	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12	INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4	INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12	INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP2_MULT_ANCB_SRC3	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP2_MULT_ANCB_SRC2	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP2_MULT_ANCB_SRC1	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP2_MULT_ANCB_SRC0	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
27	INT_STAT_VIP2_MULT_ANCA_SRC15	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP2_MULT_ANCA_SRC14	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP2_MULT_ANCA_SRC13	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP2_MULT_ANCA_SRC12	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP2_MULT_ANCA_SRC11	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP2_MULT_ANCA_SRC10	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP2_MULT_ANCA_SRC9	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP2_MULT_ANCA_SRC8	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP2_MULT_ANCA_SRC7	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	INT_STAT_VIP2_MULT_ANCA_SRC6	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_MULT_ANCA_SRC5	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_MULT_ANCA_SRC4	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP2_MULT_ANCA_SRC3	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_MULT_ANCA_SRC2	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP2_MULT_ANCA_SRC1	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP2_MULT_ANCA_SRC0	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP2_MULT_PORTB_SRC15	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP2_MULT_PORTB_SRC14	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
9	INT_STAT_VIP2_MULT_PORTB_SRC13	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP2_MULT_PORTB_SRC12	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP2_MULT_PORTB_SRC11	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP2_MULT_PORTB_SRC10	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP2_MULT_PORTB_SRC9	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP2_MULT_PORTB_SRC8	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP2_MULT_PORTB_SRC7	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP2_MULT_PORTB_SRC6	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP2_MULT_PORTB_SRC5	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	INT_STAT_VIP2_MULT_PORTB_SRC4	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-334. Register Call Summary for Register VIP_INT0_CHANNEL4_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-335. VIP_INT0_CHANNEL4_INT_MASK

Address Offset	0x0000 0064		
Physical Address	0x4897 D064 0x4899 D064 0x489B D064	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12	INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4	INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12	INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP2_MULT_ANCB_SRC3	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP2_MULT_ANCB_SRC2	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP2_MULT_ANCB_SRC1	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP2_MULT_ANCB_SRC0	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
27	INT_MASK_VIP2_MULT_ANCA_SRC15	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP2_MULT_ANCA_SRC14	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP2_MULT_ANCA_SRC13	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP2_MULT_ANCA_SRC12	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP2_MULT_ANCA_SRC11	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP2_MULT_ANCA_SRC10	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP2_MULT_ANCA_SRC9	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP2_MULT_ANCA_SRC8	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP2_MULT_ANCA_SRC7	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP2_MULT_ANCA_SRC6	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_MULT_ANCA_SRC5	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_MULT_ANCA_SRC4	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_MULT_ANCA_SRC3	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_MULT_ANCA_SRC2	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_MULT_ANCA_SRC1	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_MULT_ANCA_SRC0	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	INT_MASK_VIP2_MULT_PORTB_SRC15	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP2_MULT_PORTB_SRC14	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP2_MULT_PORTB_SRC13	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP2_MULT_PORTB_SRC12	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP2_MULT_PORTB_SRC11	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP2_MULT_PORTB_SRC10	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP2_MULT_PORTB_SRC9	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP2_MULT_PORTB_SRC8	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP2_MULT_PORTB_SRC7	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP2_MULT_PORTB_SRC6	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP2_MULT_PORTB_SRC5	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP2_MULT_PORTB_SRC4	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-336. Register Call Summary for Register VIP_INT0_CHANNEL4_INT_MASK

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-337. VIP_INT0_CHANNEL5_INT_STAT

Address Offset	0x0000 0068		
Physical Address	0x4897 D068 0x4899 D068 0x489B D068	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC	RESERVED	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_OTHER	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB	INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12	INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_STAT_TRANSCODE2_CHROMA	The last write DMA transaction has completed for channel transcode2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_TRANSCODE2_LUMA	The last write DMA transaction has completed for channel transcode2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_TRANSCODE1_CHROMA	The last write DMA transaction has completed for channel transcode1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_TRANSCODE1_LUMA	The last write DMA transaction has completed for channel transcode1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_AUX_IN	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_PIP_FRAME	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
25	INT_STAT_POST_COMP_WR	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VBI_SD_VENC	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	RESERVED	Reserved	R	0x0
22	INT_STAT_NF_LAST_CHROMA	The last write DMA transaction has completed for channel nf_last_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_NF_LAST_LUMA	The last write DMA transaction has completed for channel nf_last_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_NF_WRITE_CHROMA	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_NF_WRITE_LUMA	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_OTHER	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_PORTB_RGB	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_PORTA_RGB	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	INT_STAT_VIP2_PORTB_CHROMA	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_PORTB_LUMA	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP2_PORTA_CHROMA	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP2_PORTA_LUMA	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP2_MULT_ANCB_SRC15	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP2_MULT_ANCB_SRC14	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP2_MULT_ANCB_SRC13	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP2_MULT_ANCB_SRC12	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP2_MULT_ANCB_SRC11	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	INT_STAT_VIP2_MULT_ANCB_SRC10	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP2_MULT_ANCB_SRC9	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP2_MULT_ANCB_SRC8	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP2_MULT_ANCB_SRC7	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP2_MULT_ANCB_SRC6	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP2_MULT_ANCB_SRC5	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP2_MULT_ANCB_SRC4	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-338. Register Call Summary for Register VIP_INT0_CHANNEL5_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-339. VIP_INT0_CHANNEL5_INT_MASK

Address Offset	0x0000 006C		
Physical Address	0x4897 D06C 0x4899 D06C 0x489B D06C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		

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Table 9-339. VIP_INT0_CHANNEL5_INT_MASK (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC	RESERVED	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_OTHER	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB	INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12	INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_MASK_TRANSCODE2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_TRANSCODE2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_TRANSCODE1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_TRANSCODE1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_AUX_IN	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_PIP_FRAME	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_POST_COMP_WR	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VBI_SD_VENC	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	RESERVED	Reserved	R	0x0
22	INT_MASK_NF_LAST_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_NF_LAST_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_NF_WRITE_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_NF_WRITE_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	INT_MASK_OTHER	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_PORTB_RGB	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_PORTA_RGB	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_PORTB_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_PORTB_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_PORTA_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_PORTA_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP2_MULT_ANCB_SRC15	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP2_MULT_ANCB_SRC14	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP2_MULT_ANCB_SRC13	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP2_MULT_ANCB_SRC12	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP2_MULT_ANCB_SRC11	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP2_MULT_ANCB_SRC10	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP2_MULT_ANCB_SRC9	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP2_MULT_ANCB_SRC8	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP2_MULT_ANCB_SRC7	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP2_MULT_ANCB_SRC6	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
1	INT_MASK_VIP2_MULT_ANCB_SRC5	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP2_MULT_ANCB_SRC4	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-340. Register Call Summary for Register VIP_INT0_CHANNEL5_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-341. VIP_INT0_CLIENT0_INT_STAT

Address Offset	0x0000 0078		
Physical Address	0x4897 D078 0x4899 D078 0x489B D078	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_GRPX1_DATA	INT_STAT_COMP_WRBK	INT_STAT_SC_OUT	RESERVED								INT_STAT_SC_IN_LUMA	INT_STAT_SC_IN_CHROMA	INT_STAT_PIP_WRBK	INT_STAT_DEI_SC_OUT	RESERVED	INT_STAT_DEI_HQ_MV_OUT	RESERVED		INT_STAT_DEI_HQ_MV_IN	RESERVED					INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA

Bits	Field Name	Description	Type	Reset
31	INT_STAT_GRPX1_DATA	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_COMP_WRBK	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
29	INT_STAT_SC_OUT	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28:21	RESERVED	Reserved	R	0x00
20	INT_STAT_SC_IN_LUMA	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_SC_IN_CHROMA	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_PIP_WRBK	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_DEI_SC_OUT	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_STAT_DEI_HQ_MV_OUT	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_STAT_DEI_HQ_MV_IN	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_STAT_DEI_HQ_3_CHROMA	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	INT_STAT_DEI_HQ_3_LUMA	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_DEI_HQ_2_CHROMA	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_DEI_HQ_2_LUMA	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_DEI_HQ_1_LUMA	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_DEI_HQ_1_CHROMA	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-342. Register Call Summary for Register VIP_INT0_CLIENT0_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-343. VIP_INT0_CLIENT0_INT_MASK

Address Offset	0x0000 007C		
Physical Address	0x4897 D07C 0x4899 D07C 0x489B D07C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_GRPX1_DATA	INT_MASK_COMP_WRBK	INT_MASK_SC_OUT	RESERVED								INT_MASK_SC_IN_LUMA	INT_MASK_SC_IN_CHROMA	INT_MASK_PIP_WRBK	INT_MASK_DEI_SC_OUT	RESERVED	INT_MASK_DEI_HQ_MV_OUT	RESERVED		INT_MASK_DEI_HQ_MV_IN	RESERVED							INT_MASK_DEI_HQ_3_CHROMA	INT_MASK_DEI_HQ_3_LUMA	INT_MASK_DEI_HQ_2_CHROMA	INT_MASK_DEI_HQ_2_LUMA	INT_MASK_DEI_HQ_1_LUMA	INT_MASK_DEI_HQ_1_CHROMA

Bits	Field Name	Description	Type	Reset
31	INT_MASK_GRPX1_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_COMP_WRBK	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_SC_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28:21	RESERVED	Reserved	R	0x00
20	INT_MASK_SC_IN_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_SC_IN_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_PIP_WRBK	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_DEI_SC_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_MASK_DEI_HQ_MV_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_MASK_DEI_HQ_MV_IN	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_MASK_DEI_HQ_3_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_DEI_HQ_3_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_DEI_HQ_2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_DEI_HQ_2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_DEI_HQ_1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	INT_MASK_DEI_HQ_1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-344. Register Call Summary for Register VIP_INT0_CLIENT0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-345. VIP_INT0_CLIENT1_INT_STAT

Address Offset	0x0000 0080		
Physical Address	0x4897 D080 0x4899 D080 0x489B D080	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA	INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	RESERVED	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT	INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y	INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	RESERVED	Reserved	R	0
29	INT_STAT_VIP2_ANC_B	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
28	INT_STAT_VIP2_ANC_A	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
27	INT_STAT_VIP1_ANC_B	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
26	INT_STAT_VIP1_ANC_A	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
25	INT_STAT_TRANS2_LUMA	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
24	INT_STAT_TRANS2_CHROMA	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
23	INT_STAT_TRANS1_LUMA	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
22	INT_STAT_TRANS1_CHROMA	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
21	INT_STAT_HDMI_WRBK_OUT	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
20	INT_STAT_VPI_CTL	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
19	INT_STAT_VBI_SDVENC	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
18	RESERVED	Reserved	R	0
17	INT_STAT_NF_420_UV_OUT	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
16	INT_STAT_NF_420_Y_OUT	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
15	INT_STAT_NF_420_UV_IN	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
14	INT_STAT_NF_420_Y_IN	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
13	INT_STAT_NF_422_IN	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
12	INT_STAT_GRPX3_ST	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
11	INT_STAT_GRPX2_ST	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
10	INT_STAT_GRPX1_ST	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
9	INT_STAT_VIP2_UP_UV	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
8	INT_STAT_VIP2_UP_Y	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
7	INT_STAT_VIP2_LO_UV	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
6	INT_STAT_VIP2_LO_Y	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
5	INT_STAT_VIP1_UP_UV	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
4	INT_STAT_VIP1_UP_Y	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
3	INT_STAT_VIP1_LO_UV	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
2	INT_STAT_VIP1_LO_Y	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
1	INT_STAT_GRPX3_DATA	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
0	INT_STAT_GRPX2_DATA	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

Table 9-346. Register Call Summary for Register VIP_INT0_CLIENT1_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-347. VIP_INT0_CLIENT1_INT_MASK

Address Offset	0x0000 0084		
Physical Address	0x4897 D084 0x4899 D084 0x489B D084	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA	INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	RESERVED	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT	INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y	INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	RESERVED	Reserved	R	0
29	INT_MASK_VIP2_ANC_B	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
28	INT_MASK_VIP2_ANC_A	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
27	INT_MASK_VIP1_ANC_B	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
26	INT_MASK_VIP1_ANC_A	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
25	INT_MASK_TRANS2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
24	INT_MASK_TRANS2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
23	INT_MASK_TRANS1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
22	INT_MASK_TRANS1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
21	INT_MASK_HDMI_WRBK_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
20	INT_MASK_VPI_CTL	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
19	INT_MASK_VBI_SDVENC	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
18	RESERVED	Reserved	R	0
17	INT_MASK_NF_420_UV_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
16	INT_MASK_NF_420_Y_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
15	INT_MASK_NF_420_UV_IN	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
14	INT_MASK_NF_420_Y_IN	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
13	INT_MASK_NF_422_IN	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
12	INT_MASK_GRPX3_ST	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
11	INT_MASK_GRPX2_ST	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
10	INT_MASK_GRPX1_ST	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0

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Bits	Field Name	Description	Type	Reset
9	INT_MASK_VIP2_UP_UV	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
8	INT_MASK_VIP2_UP_Y	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
7	INT_MASK_VIP2_LO_UV	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
6	INT_MASK_VIP2_LO_Y	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
5	INT_MASK_VIP1_UP_UV	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
4	INT_MASK_VIP1_UP_Y	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
3	INT_MASK_VIP1_LO_UV	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
2	INT_MASK_VIP1_LO_Y	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
1	INT_MASK_GRPX3_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
0	INT_MASK_GRPX2_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0

Table 9-348. Register Call Summary for Register VIP_INT0_CLIENT1_INT_MASK

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-349. VIP_INT0_LIST0_INT_STAT

Address Offset	0x0000 0088		
Physical Address	0x4897 D088 0x4899 D088 0x489B D088	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8	INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0	INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE	INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE

Bits	Field Name	Description	Type	Reset
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_LIST7_NOTIFY	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_LIST7_COMPLETE	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_LIST6_NOTIFY	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_LIST6_COMPLETE	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_LIST5_NOTIFY	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_LIST5_COMPLETE	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
9	INT_STAT_LIST4_NOTIFY	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_LIST4_COMPLETE	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_LIST3_NOTIFY	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_LIST3_COMPLETE	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_LIST2_NOTIFY	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_LIST2_COMPLETE	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_LIST1_NOTIFY	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_LIST1_COMPLETE	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_LIST0_NOTIFY	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_LIST0_COMPLETE	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-350. Register Call Summary for Register VIP_INT0_LIST0_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0] [1] [2]
VIP Register Manual • VIP VPDMA Register Summary: [3]

Table 9-351. VIP_INT0_LIST0_INT_MASK

Address Offset	0x0000 008C		
Physical Address	0x4897 D08C 0x4899 D08C 0x489B D08C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA

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Table 9-351. VIP_INT0_LIST0_INT_MASK (continued)

Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int0.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8	INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0	INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE	INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE

Bits	Field Name	Description	Type	Reset
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_LIST7_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_LIST7_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_LIST6_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_LIST6_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_LIST5_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_LIST5_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_LIST4_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_LIST4_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_LIST3_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_LIST3_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_LIST2_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_LIST2_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_LIST1_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_LIST1_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_LIST0_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_LIST0_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Table 9-352. Register Call Summary for Register VIP_INT0_LIST0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-353. VIP_INT1_CHANNEL0_INT_STAT

Address Offset	0x0000 0090		
Physical Address	0x4897 D090 0x4899 D090 0x489B D090	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_GRPX3	INT_STAT_GRPX2	INT_STAT_GRPX1	INT_STAT_SCALER_OUT	RESERVED								INT_STAT_SCALER_CHROMA	INT_STAT_SCALER_LUMA	INT_STAT_HQ_SCALER	RESERVED	INT_STAT_HQ_MV_OUT	RESERVED		INT_STAT_HQ_MV	RESERVED				INT_STAT_HQ_VID3_CHROMA	INT_STAT_HQ_VID3_LUMA	INT_STAT_HQ_VID2_CHROMA	INT_STAT_HQ_VID2_LUMA	INT_STAT_HQ_VID1_CHROMA	INT_STAT_HQ_VID1_LUMA	

Bits	Field Name	Description	Type	Reset
31	INT_STAT_GRPX3	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_GRPX2	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_GRPX1	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_SCALER_OUT	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27:20	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
19	INT_STAT_SCALER_CHROMA	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_SCALER_LUMA	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_HQ_SCALER	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_STAT_HQ_MV_OUT	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_STAT_HQ_MV	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_STAT_HQ_VID3_CHROMA	The last write DMA transaction has completed for channel hq_vid3_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_HQ_VID3_LUMA	The last write DMA transaction has completed for channel hq_vid3_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_HQ_VID2_CHROMA	The last write DMA transaction has completed for channel hq_vid2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	INT_STAT_HQ_VID2_LUMA	The last write DMA transaction has completed for channel hq_vid2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_HQ_VID1_CHROMA	The last write DMA transaction has completed for channel hq_vid1_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_HQ_VID1_LUMA	The last write DMA transaction has completed for channel hq_vid1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

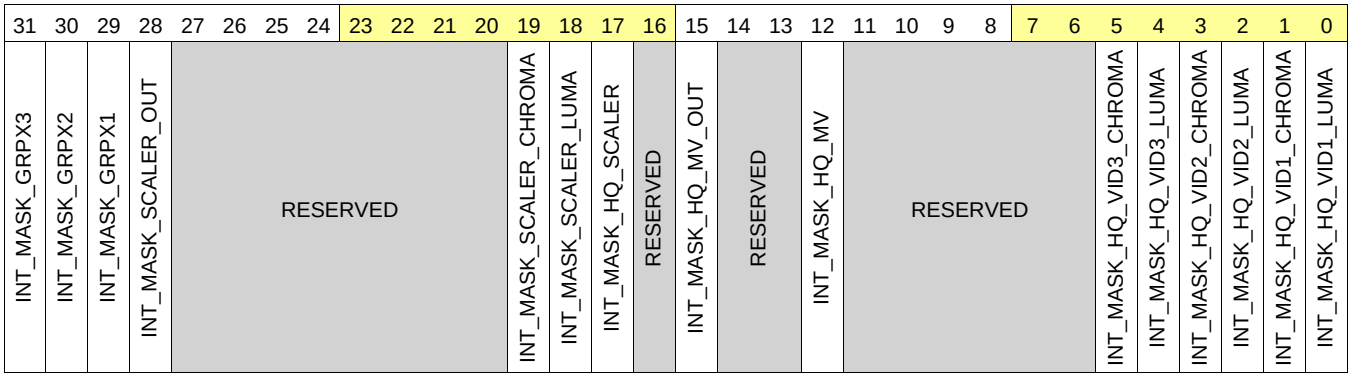
Table 9-354. Register Call Summary for Register VIP_INT1_CHANNEL0_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-355. VIP_INT1_CHANNEL0_INT_MASK

Address Offset	0x0000 0094		
Physical Address	0x4897 D094 0x4899 D094 0x489B D094	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	INT_MASK_GRPX3	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_GRPX2	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
29	INT_MASK_GRPX1	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_SCALER_OUT	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27:20	RESERVED	Reserved	R	0x00
19	INT_MASK_SCALER_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_SCALER_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_HQ_SCALER	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_MASK_HQ_MV_OUT	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_MASK_HQ_MV	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_MASK_HQ_VID3_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_HQ_VID3_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_HQ_VID2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_HQ_VID2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_HQ_VID1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_HQ_VID1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-356. Register Call Summary for Register VIP_INT1_CHANNEL0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-357. VIP_INT1_CHANNEL1_INT_STAT

Address Offset	0x0000 0098		
Physical Address	0x4897 D098 0x4899 D098 0x489B D098	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA

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Table 9-357. VIP_INT1_CHANNEL1_INT_STAT (continued)

Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2	INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10	INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2	INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	RESERVED						

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP1_MULT_PORTB_SRC9	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP1_MULT_PORTB_SRC8	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP1_MULT_PORTB_SRC7	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP1_MULT_PORTB_SRC6	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP1_MULT_PORTB_SRC5	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
26	INT_STAT_VIP1_MULT_PORTB_SRC4	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP1_MULT_PORTB_SRC3	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP1_MULT_PORTB_SRC2	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP1_MULT_PORTB_SRC1	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP1_MULT_PORTB_SRC0	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP1_MULT_PORTA_SRC15	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP1_MULT_PORTA_SRC14	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP1_MULT_PORTA_SRC13	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP1_MULT_PORTA_SRC12	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
17	INT_STAT_VIP1_MULT_PORTA_SRC11	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP1_MULT_PORTA_SRC10	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP1_MULT_PORTA_SRC9	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP1_MULT_PORTA_SRC8	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP1_MULT_PORTA_SRC7	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP1_MULT_PORTA_SRC6	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP1_MULT_PORTA_SRC5	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_MULT_PORTA_SRC4	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_MULT_PORTA_SRC3	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
8	INT_STAT_VIP1_MULT_PORTA_SRC2	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_MULT_PORTA_SRC1	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP1_MULT_PORTA_SRC0	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5:0	RESERVED	Reserved	R	0x00

Table 9-358. Register Call Summary for Register VIP_INT1_CHANNEL1_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-359. VIP_INT1_CHANNEL1_INT_MASK

Address Offset	0x0000 009C		
Physical Address	0x4897 D09C 0x4899 D09C 0x489B D09C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2	INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10	INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2	INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	RESERVED					

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Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP1_MULT_PORTB_SRC9	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP1_MULT_PORTB_SRC8	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP1_MULT_PORTB_SRC7	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP1_MULT_PORTB_SRC6	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP1_MULT_PORTB_SRC5	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP1_MULT_PORTB_SRC4	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP1_MULT_PORTB_SRC3	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP1_MULT_PORTB_SRC2	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP1_MULT_PORTB_SRC1	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP1_MULT_PORTB_SRC0	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP1_MULT_PORTA_SRC15	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP1_MULT_PORTA_SRC14	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP1_MULT_PORTA_SRC13	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP1_MULT_PORTA_SRC12	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP1_MULT_PORTA_SRC11	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP1_MULT_PORTA_SRC10	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP1_MULT_PORTA_SRC9	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP1_MULT_PORTA_SRC8	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP1_MULT_PORTA_SRC7	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP1_MULT_PORTA_SRC6	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	INT_MASK_VIP1_MULT_PORTA_SRC5	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_MULT_PORTA_SRC4	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_MULT_PORTA_SRC3	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_MULT_PORTA_SRC2	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_MULT_PORTA_SRC1	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_MULT_PORTA_SRC0	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5:0	RESERVED	Reserved	R	0x00

Table 9-360. Register Call Summary for Register VIP_INT1_CHANNEL1_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-361. VIP_INT1_CHANNEL2_INT_STAT

Address Offset	0x0000 00A0		
Physical Address	0x4897 D0A0 0x4899 D0A0 0x489B D0A0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2	INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10	INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2	INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10

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Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP1_MULT_ANCB_SRC9	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP1_MULT_ANCB_SRC8	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP1_MULT_ANCB_SRC7	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP1_MULT_ANCB_SRC6	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP1_MULT_ANCB_SRC5	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP1_MULT_ANCB_SRC4	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP1_MULT_ANCB_SRC3	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP1_MULT_ANCB_SRC2	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP1_MULT_ANCB_SRC1	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
22	INT_STAT_VIP1_MULT_ANCB_SRC0	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP1_MULT_ANCA_SRC15	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP1_MULT_ANCA_SRC14	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP1_MULT_ANCA_SRC13	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP1_MULT_ANCA_SRC12	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP1_MULT_ANCA_SRC11	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP1_MULT_ANCA_SRC10	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP1_MULT_ANCA_SRC9	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP1_MULT_ANCA_SRC8	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
13	INT_STAT_VIP1_MULT_ANCA_SRC7	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP1_MULT_ANCA_SRC6	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP1_MULT_ANCA_SRC5	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_MULT_ANCA_SRC4	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_MULT_ANCA_SRC3	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP1_MULT_ANCA_SRC2	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_MULT_ANCA_SRC1	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP1_MULT_ANCA_SRC0	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP1_MULT_PORTB_SRC15	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	INT_STAT_VIP1_MULT_PORTB_SRC14	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP1_MULT_PORTB_SRC13	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP1_MULT_PORTB_SRC12	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP1_MULT_PORTB_SRC11	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP1_MULT_PORTB_SRC10	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-362. Register Call Summary for Register VIP_INT1_CHANNEL2_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-363. VIP_INT1_CHANNEL2_INT_MASK

Address Offset	0x0000 00A4		
Physical Address	0x4897 D0A4 0x4899 D0A4 0x489B D0A4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2	INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10	INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2	INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP1_MULT_ANCB_SRC9	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP1_MULT_ANCB_SRC8	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP1_MULT_ANCB_SRC7	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP1_MULT_ANCB_SRC6	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP1_MULT_ANCB_SRC5	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP1_MULT_ANCB_SRC4	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP1_MULT_ANCB_SRC3	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP1_MULT_ANCB_SRC2	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP1_MULT_ANCB_SRC1	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP1_MULT_ANCB_SRC0	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP1_MULT_ANCA_SRC15	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
20	INT_MASK_VIP1_MULT_ANCA_SRC14	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP1_MULT_ANCA_SRC13	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP1_MULT_ANCA_SRC12	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP1_MULT_ANCA_SRC11	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP1_MULT_ANCA_SRC10	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP1_MULT_ANCA_SRC9	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP1_MULT_ANCA_SRC8	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP1_MULT_ANCA_SRC7	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP1_MULT_ANCA_SRC6	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP1_MULT_ANCA_SRC5	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_MULT_ANCA_SRC4	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_MULT_ANCA_SRC3	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_MULT_ANCA_SRC2	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_MULT_ANCA_SRC1	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_MULT_ANCA_SRC0	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP1_MULT_PORTB_SRC15	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	INT_MASK_VIP1_MULT_PORTB_SRC14	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP1_MULT_PORTB_SRC13	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP1_MULT_PORTB_SRC12	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP1_MULT_PORTB_SRC11	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP1_MULT_PORTB_SRC10	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-364. Register Call Summary for Register VIP_INT1_CHANNEL2_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-365. VIP_INT1_CHANNEL3_INT_STAT

Address Offset	0x0000 00A8		
Physical Address	0x4897 D0A8 0x4899 D0A8 0x489B D0A8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12	INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4	INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA	INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP2_MULT_PORTB_SRC3	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
30	INT_STAT_VIP2_MULT_PORTB_SRC2	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP2_MULT_PORTB_SRC1	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP2_MULT_PORTB_SRC0	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP2_MULT_PORTA_SRC15	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP2_MULT_PORTA_SRC14	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP2_MULT_PORTA_SRC13	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VIP2_MULT_PORTA_SRC12	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP2_MULT_PORTA_SRC11	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP2_MULT_PORTA_SRC10	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
21	INT_STAT_VIP2_MULT_PORTA_SRC9	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP2_MULT_PORTA_SRC8	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP2_MULT_PORTA_SRC7	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP2_MULT_PORTA_SRC6	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_MULT_PORTA_SRC5	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_MULT_PORTA_SRC4	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP2_MULT_PORTA_SRC3	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_MULT_PORTA_SRC2	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP2_MULT_PORTA_SRC1	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
12	INT_STAT_VIP2_MULT_PORTA_SRC0	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP1_PORTB_RGB	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP1_PORTA_RGB	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP1_PORTB_CHROMA	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP1_PORTB_LUMA	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP1_PORTA_CHROMA	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP1_PORTA_LUMA	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP1_MULT_ANCB_SRC15	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP1_MULT_ANCB_SRC14	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	INT_STAT_VIP1_MULT_ANCB_SRC13	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP1_MULT_ANCB_SRC12	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP1_MULT_ANCB_SRC11	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP1_MULT_ANCB_SRC10	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-366. Register Call Summary for Register VIP_INT1_CHANNEL3_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-367. VIP_INT1_CHANNEL3_INT_MASK

Address Offset	0x0000 00AC		
Physical Address	0x4897 D0AC 0x4899 D0AC 0x489B D0AC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12	INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4	INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA	INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10

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Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP2_MULT_PORTB_SRC3	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP2_MULT_PORTB_SRC2	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP2_MULT_PORTB_SRC1	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP2_MULT_PORTB_SRC0	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP2_MULT_PORTA_SRC15	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP2_MULT_PORTA_SRC14	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP2_MULT_PORTA_SRC13	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP2_MULT_PORTA_SRC12	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP2_MULT_PORTA_SRC11	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP2_MULT_PORTA_SRC10	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_VIP2_MULT_PORTA_SRC9	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP2_MULT_PORTA_SRC8	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP2_MULT_PORTA_SRC7	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP2_MULT_PORTA_SRC6	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_MULT_PORTA_SRC5	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_MULT_PORTA_SRC4	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_MULT_PORTA_SRC3	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_MULT_PORTA_SRC2	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_MULT_PORTA_SRC1	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_MULT_PORTA_SRC0	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	INT_MASK_VIP1_PORTB_RGB	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP1_PORTA_RGB	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP1_PORTB_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP1_PORTB_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP1_PORTA_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP1_PORTA_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP1_MULT_ANCB_SRC15	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP1_MULT_ANCB_SRC14	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP1_MULT_ANCB_SRC13	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP1_MULT_ANCB_SRC12	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP1_MULT_ANCB_SRC11	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP1_MULT_ANCB_SRC10	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-368. Register Call Summary for Register VIP_INT1_CHANNEL3_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-369. VIP_INT1_CHANNEL4_INT_STAT

Address Offset	0x0000 00B0		
Physical Address	0x4897 D0B0 0x4899 D0B0 0x489B D0B0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12	INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4	INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12	INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_STAT_VIP2_MULT_ANCB_SRC3	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_VIP2_MULT_ANCB_SRC2	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_VIP2_MULT_ANCB_SRC1	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_VIP2_MULT_ANCB_SRC0	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_VIP2_MULT_ANCA_SRC15	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_VIP2_MULT_ANCA_SRC14	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_VIP2_MULT_ANCA_SRC13	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
24	INT_STAT_VIP2_MULT_ANCA_SRC12	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_VIP2_MULT_ANCA_SRC11	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_VIP2_MULT_ANCA_SRC10	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_VIP2_MULT_ANCA_SRC9	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_VIP2_MULT_ANCA_SRC8	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_VIP2_MULT_ANCA_SRC7	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_VIP2_MULT_ANCA_SRC6	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_MULT_ANCA_SRC5	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_MULT_ANCA_SRC4	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	INT_STAT_VIP2_MULT_ANCA_SRC3	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_MULT_ANCA_SRC2	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP2_MULT_ANCA_SRC1	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP2_MULT_ANCA_SRC0	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP2_MULT_PORTB_SRC15	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_VIP2_MULT_PORTB_SRC14	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP2_MULT_PORTB_SRC13	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP2_MULT_PORTB_SRC12	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP2_MULT_PORTB_SRC11	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	INT_STAT_VIP2_MULT_PORTB_SRC10	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP2_MULT_PORTB_SRC9	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP2_MULT_PORTB_SRC8	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP2_MULT_PORTB_SRC7	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP2_MULT_PORTB_SRC6	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_VIP2_MULT_PORTB_SRC5	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP2_MULT_PORTB_SRC4	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-370. Register Call Summary for Register VIP_INT1_CHANNEL4_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-371. VIP_INT1_CHANNEL4_INT_MASK

Address Offset	0x0000 00B4		
Physical Address	0x4897 D0B4 0x4899 D0B4 0x489B D0B4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		

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Table 9-371. VIP_INT1_CHANNEL4_INT_MASK (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12	INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4	INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12	INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_MASK_VIP2_MULT_ANCB_SRC3	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_VIP2_MULT_ANCB_SRC2	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_VIP2_MULT_ANCB_SRC1	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_VIP2_MULT_ANCB_SRC0	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_VIP2_MULT_ANCA_SRC15	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_VIP2_MULT_ANCA_SRC14	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_VIP2_MULT_ANCA_SRC13	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VIP2_MULT_ANCA_SRC12	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	INT_MASK_VIP2_MULT_ANCA_SRC11	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_VIP2_MULT_ANCA_SRC10	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
21	INT_MASK_VIP2_MULT_ANCA_SRC9	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_VIP2_MULT_ANCA_SRC8	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_VIP2_MULT_ANCA_SRC7	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_VIP2_MULT_ANCA_SRC6	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_MULT_ANCA_SRC5	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_MULT_ANCA_SRC4	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_MULT_ANCA_SRC3	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_MULT_ANCA_SRC2	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_MULT_ANCA_SRC1	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_MULT_ANCA_SRC0	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP2_MULT_PORTB_SRC15	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP2_MULT_PORTB_SRC14	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_VIP2_MULT_PORTB_SRC13	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP2_MULT_PORTB_SRC12	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP2_MULT_PORTB_SRC11	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP2_MULT_PORTB_SRC10	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP2_MULT_PORTB_SRC9	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP2_MULT_PORTB_SRC8	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	INT_MASK_VIP2_MULT_PORTB_SRC7	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP2_MULT_PORTB_SRC6	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP2_MULT_PORTB_SRC5	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP2_MULT_PORTB_SRC4	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-372. Register Call Summary for Register VIP_INT1_CHANNEL4_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-373. VIP_INT1_CHANNEL5_INT_STAT

Address Offset	0x0000 00B8		
Physical Address	0x4897 D0B8 0x4899 D0B8 0x489B D0B8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC	RESERVED	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_OTHER	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB	INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12	INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_STAT_TRANSCODE2_CHROMA	The last write DMA transaction has completed for channel transcode2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
30	INT_STAT_TRANSCODE2_LUMA	The last write DMA transaction has completed for channel transcode2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_TRANSCODE1_CHROMA	The last write DMA transaction has completed for channel transcode1_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_TRANSCODE1_LUMA	The last write DMA transaction has completed for channel transcode1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_AUX_IN	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_PIP_FRAME	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
25	INT_STAT_POST_COMP_WR	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_VBI_SD_VENC	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	RESERVED	Reserved	R	0x0
22	INT_STAT_NF_LAST_CHROMA	The last write DMA transaction has completed for channel nf_last_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_NF_LAST_LUMA	The last write DMA transaction has completed for channel nf_last_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
20	INT_STAT_NF_WRITE_CHROMA	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_NF_WRITE_LUMA	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_OTHER	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_VIP2_PORTB_RGB	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_VIP2_PORTA_RGB	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_VIP2_PORTB_CHROMA	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_VIP2_PORTB_LUMA	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_VIP2_PORTA_CHROMA	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
12	INT_STAT_VIP2_PORTA_LUMA	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_VIP2_MULT_ANCB_SRC15	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
10	INT_STAT_VIP2_MULT_ANCB_SRC14	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_VIP2_MULT_ANCB_SRC13	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_VIP2_MULT_ANCB_SRC12	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_VIP2_MULT_ANCB_SRC11	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_VIP2_MULT_ANCB_SRC10	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_VIP2_MULT_ANCB_SRC9	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_VIP2_MULT_ANCB_SRC8	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_VIP2_MULT_ANCB_SRC7	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_VIP2_MULT_ANCB_SRC6	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
1	INT_STAT_VIP2_MULT_ANCB_SRC5	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_VIP2_MULT_ANCB_SRC4	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-374. Register Call Summary for Register VIP_INT1_CHANNEL5_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-375. VIP_INT1_CHANNEL5_INT_MASK

Address Offset	0x0000 00BC		
Physical Address	0x4897 D0BC 0x4899 D0BC 0x489B D0BC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC	RESERVED	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_OTHER	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB	INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12	INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4

Bits	Field Name	Description	Type	Reset
31	INT_MASK_TRANSCODE2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_TRANSCODE2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_TRANSCODE1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
28	INT_MASK_TRANSCODE1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_AUX_IN	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_PIP_FRAME	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_POST_COMP_WR	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VBI_SD_VENC	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	RESERVED	Reserved	R	0x0
22	INT_MASK_NF_LAST_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_NF_LAST_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_NF_WRITE_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_NF_WRITE_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_OTHER	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_VIP2_PORTB_RGB	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_PORTA_RGB	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_VIP2_PORTB_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_VIP2_PORTB_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_VIP2_PORTA_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_VIP2_PORTA_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_VIP2_MULT_ANCB_SRC15	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_VIP2_MULT_ANCB_SRC14	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
9	INT_MASK_VIP2_MULT_ANCB_SRC13	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_VIP2_MULT_ANCB_SRC12	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_VIP2_MULT_ANCB_SRC11	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_VIP2_MULT_ANCB_SRC10	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_VIP2_MULT_ANCB_SRC9	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_VIP2_MULT_ANCB_SRC8	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_VIP2_MULT_ANCB_SRC7	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_VIP2_MULT_ANCB_SRC6	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_VIP2_MULT_ANCB_SRC5	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_VIP2_MULT_ANCB_SRC4	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-376. Register Call Summary for Register VIP_INT1_CHANNEL5_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-377. VIP_INT1_CLIENT0_INT_STAT

Address Offset	0x0000 00C8		
Physical Address	0x4897 D0C8 0x4899 D0C8 0x489B D0C8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC	RESERVED	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_NF_READ	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB	INT_STAT_DEI_HQ_MV_OUT	RESERVED		INT_STAT_DEI_HQ_MV_IN	RESERVED					INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA

Bits	Field Name	Description	Type	Reset
31	INT_MASK_TRANSCODE2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_TRANSCODE2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_TRANSCODE1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_TRANSCODE1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_AUX_IN	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_PIP_FRAME	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_POST_COMP_WR	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_VBI_SD_VENC	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
23	RESERVED	Reserved	R	0x0
22	INT_MASK_NF_LAST_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_NF_LAST_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_NF_WRITE_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_NF_WRITE_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_NF_READ	The interrupt for Noise Filter Input Data 422 Interleaved should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
17	INT_MASK_VIP2_PORTB_RGB	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_VIP2_PORTA_RGB	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_STAT_DEI_HQ_MV_OUT	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_STAT_DEI_HQ_MV_IN	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_STAT_DEI_HQ_3_CHROMA	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_DEI_HQ_3_LUMA	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_DEI_HQ_2_CHROMA	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_DEI_HQ_2_LUMA	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_DEI_HQ_1_LUMA	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	INT_STAT_DEI_HQ_1_CHROMA	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

Table 9-378. Register Call Summary for Register VIP_INT1_CLIENT0_INT_STAT

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-379. VIP_INT1_CLIENT0_INT_MASK

Address Offset	0x0000 00CC		
Physical Address	0x4897 D0CC 0x4899 D0CC 0x489B D0CC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28 27 26 25 24	23 22 21	20	19	18	17	16	15 14 13	12	11 10 9 8	7 6	5	4	3	2	1	0
INT_MASK_GRPX1_DATA	INT_MASK_COMP_WRBK	INT_MASK_SC_OUT	RESERVED		INT_MASK_SC_IN_LUMA	INT_MASK_SC_IN_CHROMA	INT_MASK_PIP_WRBK	INT_MASK_DEI_SC_OUT	RESERVED	INT_MASK_DEI_HQ_MV_OUT	RESERVED	INT_MASK_DEI_HQ_MV_IN	RESERVED	INT_MASK_DEI_HQ_3_CHROMA	INT_MASK_DEI_HQ_3_LUMA	INT_MASK_DEI_HQ_2_CHROMA	INT_MASK_DEI_HQ_2_LUMA	INT_MASK_DEI_HQ_1_LUMA	INT_MASK_DEI_HQ_1_CHROMA

Bits	Field Name	Description	Type	Reset
31	INT_MASK_GRPX1_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_COMP_WRBK	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_SC_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28:21	RESERVED	Reserved	R	0x00
20	INT_MASK_SC_IN_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_SC_IN_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	INT_MASK_PIP_WRBK	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_DEI_SC_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	RESERVED	Reserved	R	0x0
15	INT_MASK_DEI_HQ_MV_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14:13	RESERVED	Reserved	R	0x0
12	INT_MASK_DEI_HQ_MV_IN	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11:6	RESERVED	Reserved	R	0x00
5	INT_MASK_DEI_HQ_3_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_DEI_HQ_3_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
3	INT_MASK_DEI_HQ_2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_DEI_HQ_2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_DEI_HQ_1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_DEI_HQ_1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-380. Register Call Summary for Register VIP_INT1_CLIENT0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-381. VIP_INT1_CLIENT1_INT_STAT

Address Offset	0x0000 00D0		
Physical Address	0x4897 D0D0 0x4899 D0D0 0x489B D0D0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA	INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	RESERVED	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT	INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y	INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	RESERVED	Reserved	R	0
29	INT_STAT_VIP2_ANC_B	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
28	INT_STAT_VIP2_ANC_A	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
27	INT_STAT_VIP1_ANC_B	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
26	INT_STAT_VIP1_ANC_A	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
25	INT_STAT_TRANS2_LUMA	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
24	INT_STAT_TRANS2_CHROMA	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
23	INT_STAT_TRANS1_LUMA	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
22	INT_STAT_TRANS1_CHROMA	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
21	INT_STAT_HDMI_WRBK_OUT	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
20	INT_STAT_VPI_CTL	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
19	INT_STAT_VBI_SDVENC	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
18	RESERVED	Reserved	R	0
17	INT_STAT_NF_420_UV_OUT	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
16	INT_STAT_NF_420_Y_OUT	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
15	INT_STAT_NF_420_UV_IN	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
14	INT_STAT_NF_420_Y_IN	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
13	INT_STAT_NF_422_IN	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
12	INT_STAT_GRPX3_ST	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
11	INT_STAT_GRPX2_ST	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
10	INT_STAT_GRPX1_ST	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
9	INT_STAT_VIP2_UP_UV	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
8	INT_STAT_VIP2_UP_Y	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
7	INT_STAT_VIP2_LO_UV	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

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Bits	Field Name	Description	Type	Reset
6	INT_STAT_VIP2_LO_Y	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
5	INT_STAT_VIP1_UP_UV	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
4	INT_STAT_VIP1_UP_Y	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
3	INT_STAT_VIP1_LO_UV	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
2	INT_STAT_VIP1_LO_Y	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
1	INT_STAT_GRPX3_DATA	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0
0	INT_STAT_GRPX2_DATA	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW W0toClr	0

Table 9-382. Register Call Summary for Register VIP_INT1_CLIENT1_INT_STAT

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

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Table 9-383. VIP_INT1_CLIENT1_INT_MASK

Address Offset	0x0000 00D4		
Physical Address	0x4897 D0D4 0x4899 D0D4 0x489B D0D4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA	INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	RESERVED	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT	INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y	INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	RESERVED	Reserved	R	0
29	INT_MASK_VIP2_ANC_B	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
28	INT_MASK_VIP2_ANC_A	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
27	INT_MASK_VIP1_ANC_B	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
26	INT_MASK_VIP1_ANC_A	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
25	INT_MASK_TRANS2_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
24	INT_MASK_TRANS2_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
23	INT_MASK_TRANS1_LUMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
22	INT_MASK_TRANS1_CHROMA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
21	INT_MASK_HDMI_WRBK_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
20	INT_MASK_VPI_CTL	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
19	INT_MASK_VBI_SDVENC	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
18	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
17	INT_MASK_NF_420_UV_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
16	INT_MASK_NF_420_Y_OUT	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
15	INT_MASK_NF_420_UV_IN	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
14	INT_MASK_NF_420_Y_IN	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
13	INT_MASK_NF_422_IN	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
12	INT_MASK_GRPX3_ST	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
11	INT_MASK_GRPX2_ST	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
10	INT_MASK_GRPX1_ST	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
9	INT_MASK_VIP2_UP_UV	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
8	INT_MASK_VIP2_UP_Y	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
7	INT_MASK_VIP2_LO_UV	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
6	INT_MASK_VIP2_LO_Y	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
5	INT_MASK_VIP1_UP_UV	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
4	INT_MASK_VIP1_UP_Y	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
3	INT_MASK_VIP1_LO_UV	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
2	INT_MASK_VIP1_LO_Y	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
1	INT_MASK_GRPX3_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0
0	INT_MASK_GRPX2_DATA	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0

Table 9-384. Register Call Summary for Register VIP_INT1_CLIENT1_INT_MASK

VIP Functional Description • VPDMA Interrupts: [0]
VIP Register Manual • VIP VPDMA Register Summary: [1]

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Table 9-385. VIP_INT1_LIST0_INT_STAT

Address Offset	0x0000 00D8		
Physical Address	0x4897 D0D8 0x4899 D0D8 0x489B D0D8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	This register gives the information of the interrupts that have triggered since last cleared by the process that is servicing vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8	INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0	INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE	INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE

Bits	Field Name	Description	Type	Reset
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
15	INT_STAT_LIST7_NOTIFY	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
14	INT_STAT_LIST7_COMPLETE	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
13	INT_STAT_LIST6_NOTIFY	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
12	INT_STAT_LIST6_COMPLETE	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
11	INT_STAT_LIST5_NOTIFY	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
10	INT_STAT_LIST5_COMPLETE	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
9	INT_STAT_LIST4_NOTIFY	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
8	INT_STAT_LIST4_COMPLETE	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
7	INT_STAT_LIST3_NOTIFY	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
6	INT_STAT_LIST3_COMPLETE	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
5	INT_STAT_LIST2_NOTIFY	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
4	INT_STAT_LIST2_COMPLETE	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
3	INT_STAT_LIST1_NOTIFY	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
2	INT_STAT_LIST1_COMPLETE	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
1	INT_STAT_LIST0_NOTIFY	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0
0	INT_STAT_LIST0_COMPLETE	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.	RW	0x0

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Table 9-386. Register Call Summary for Register VIP_INT1_LIST0_INT_STAT

VIP Functional Description

- VPDMA Interrupts: [0] [1] [2]

VIP Register Manual

- VIP VPDMA Register Summary: [3]

Table 9-387. VIP_INT1_LIST0_INT_MASK

Address Offset	0x0000 00DC		
Physical Address	0x4897 D0DC 0x4899 D0DC 0x489B D0DC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register gives the information of the interrupts that should be masked and not generate an interrupt for vpdma_int1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8	INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0	INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE	INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE

Bits	Field Name	Description	Type	Reset
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
15	INT_MASK_LIST7_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
14	INT_MASK_LIST7_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
13	INT_MASK_LIST6_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
12	INT_MASK_LIST6_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
11	INT_MASK_LIST5_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
10	INT_MASK_LIST5_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
9	INT_MASK_LIST4_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
8	INT_MASK_LIST4_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
7	INT_MASK_LIST3_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
6	INT_MASK_LIST3_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
5	INT_MASK_LIST2_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
4	INT_MASK_LIST2_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	INT_MASK_LIST1_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
2	INT_MASK_LIST1_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
1	INT_MASK_LIST0_NOTIFY	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0
0	INT_MASK_LIST0_COMPLETE	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.	RW	0x0

Table 9-388. Register Call Summary for Register VIP_INT1_LIST0_INT_MASK

VIP Functional Description
- VPDMA Interrupts: [0]

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-389. VIP_PERF_MON0

Address Offset	0x0000 0200		
Physical Address	0x4897 D200 0x4899 D200 0x489B D200	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: vip2_anc_b 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: vip2_anc_b 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0

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Bits	Field Name	Description	Type	Reset
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-390. Register Call Summary for Register VIP_PERF_MON0

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-391. VIP_PERF_MON1

Address Offset	0x0000 0204		
Physical Address	0x4897 D204 0x4899 D204 0x489B D204	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-392. Register Call Summary for Register VIP_PERF_MON1

VIP Register Manual
- VIP VPDMA Register Summary: [0]

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Table 9-393. VIP_PERF_MON2

Address Offset	0x0000 0208		
Physical Address	0x4897 D208 0x4899 D208 0x489B D208	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE		STOP_CLIENT		RESERVED		STOP_COUNT		RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-394. Register Call Summary for Register VIP_PERF_MON2

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-395. VIP_PERF_MON3

Address Offset	0x0000 020C		
Physical Address	0x4897 D20C 0x4899 D20C 0x489B D20C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-396. Register Call Summary for Register VIP_PERF_MON3

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-397. VIP_PERF_MON4

Address Offset	0x0000 0210		
Physical Address	0x4897 D210 0x4899 D210 0x489B D210	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-398. Register Call Summary for Register VIP_PERF_MON4

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-399. VIP_PERF_MON5

Address Offset	0x0000 0214		
Physical Address	0x4897 D214 0x4899 D214 0x489B D214	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				STOP_COUNT				RESERVED				START_CLIENT				RESERVED				START_COUNT			
CURR_COUNT																															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-400. Register Call Summary for Register VIP_PERF_MON5

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-401. VIP_PERF_MON6

Address Offset	0x0000 0218		
Physical Address	0x4897 D218 0x4899 D218 0x489B D218	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				STOP_COUNT				RESERVED				START_CLIENT				RESERVED				START_COUNT			
CURR_COUNT																															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-402. Register Call Summary for Register VIP_PERF_MON6

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-403. VIP_PERF_MON7

Address Offset	0x0000 021C		
Physical Address	0x4897 D21C 0x4899 D21C 0x489B D21C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-404. Register Call Summary for Register VIP_PERF_MON7

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-405. VIP_PERF_MON8

Address Offset	0x0000 0220		
Physical Address	0x4897 D220 0x4899 D220 0x489B D220	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-406. Register Call Summary for Register VIP_PERF_MON8

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-407. VIP_PERF_MON9

Address Offset	0x0000 0224		
Physical Address	0x4897 D224 0x4899 D224 0x489B D224	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-408. Register Call Summary for Register VIP_PERF_MON9

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-409. VIP_PERF_MON10

Address Offset	0x0000 0228		
Physical Address	0x4897 D228 0x4899 D228 0x489B D228	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE		STOP_CLIENT		RESERVED		STOP_COUNT		RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT																	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-410. Register Call Summary for Register VIP_PERF_MON10

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-411. VIP_PERF_MON11

Address Offset	0x0000 022C		
Physical Address	0x4897 D22C 0x4899 D22C 0x489B D22C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-412. Register Call Summary for Register VIP_PERF_MON11

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-413. VIP_PERF_MON12

Address Offset	0x0000 0230		
Physical Address	0x4897 D230 0x4899 D230 0x489B D230	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-414. Register Call Summary for Register VIP_PERF_MON12

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-415. VIP_PERF_MON13

Address Offset	0x0000 0234		
Physical Address	0x4897 D234 0x4899 D234 0x489B D234	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-416. Register Call Summary for Register VIP_PERF_MON13

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-417. VIP_PERF_MON14

Address Offset	0x0000 0238		
Physical Address	0x4897 D238 0x4899 D238 0x489B D238	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-418. Register Call Summary for Register VIP_PERF_MON14

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-419. VIP_PERF_MON15

Address Offset	0x0000 023C		
Physical Address	0x4897 D23C 0x4899 D23C 0x489B D23C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-420. Register Call Summary for Register VIP_PERF_MON15

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-421. VIP_PERF_MON16

Address Offset	0x0000 0240		
Physical Address	0x4897 D240 0x4899 D240 0x489B D240	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				STOP_COUNT				RESERVED				START_CLIENT				RESERVED				START_COUNT			
CURR_COUNT																															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-422. Register Call Summary for Register VIP_PERF_MON16

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-423. VIP_PERF_MON17

Address Offset	0x0000 0244		
Physical Address	0x4897 D244 0x4899 D244 0x489B D244	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-424. Register Call Summary for Register VIP_PERF_MON17

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-425. VIP_PERF_MON18

Address Offset	0x0000 0248		
Physical Address	0x4897 D248 0x4899 D248 0x489B D248	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-426. Register Call Summary for Register VIP_PERF_MON18

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-427. VIP_PERF_MON19

Address Offset	0x0000 024C		
Physical Address	0x4897 D24C 0x4899 D24C 0x489B D24C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-428. Register Call Summary for Register VIP_PERF_MON19

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-429. VIP_PERF_MON20

Address Offset	0x0000 0250		
Physical Address	0x4897 D250 0x4899 D250 0x489B D250	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-430. Register Call Summary for Register VIP_PERF_MON20

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-431. VIP_PERF_MON21

Address Offset	0x0000 0254		
Physical Address	0x4897 D254 0x4899 D254 0x489B D254	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				STOP_COUNT				RESERVED				START_CLIENT				RESERVED				START_COUNT			
CURR_COUNT																															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-432. Register Call Summary for Register VIP_PERF_MON21

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-433. VIP_PERF_MON22

Address Offset	0x0000 0258		
Physical Address	0x4897 D258 0x4899 D258 0x489B D258	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-434. Register Call Summary for Register VIP_PERF_MON22

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-435. VIP_PERF_MON23

Address Offset	0x0000 025C		
Physical Address	0x4897 D25C 0x4899 D25C 0x489B D25C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-436. Register Call Summary for Register VIP_PERF_MON23

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-437. VIP_PERF_MON24

Address Offset	0x0000 0260		
Physical Address	0x4897 D260 0x4899 D260 0x489B D260	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-438. Register Call Summary for Register VIP_PERF_MON24

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-439. VIP_PERF_MON25

Address Offset	0x0000 0264		
Physical Address	0x4897 D264 0x4899 D264 0x489B D264	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE		STOP_CLIENT		RESERVED		STOP_COUNT		RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-440. Register Call Summary for Register VIP_PERF_MON25

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-441. VIP_PERF_MON26

Address Offset	0x0000 0268		
Physical Address	0x4897 D268 0x4899 D268 0x489B D268	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				STOP_COUNT				RESERVED				START_CLIENT				RESERVED				START_COUNT			
CURR_COUNT																															

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-442. Register Call Summary for Register VIP_PERF_MON26

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-443. VIP_PERF_MON27

Address Offset	0x0000 026C		
Physical Address	0x4897 D26C 0x4899 D26C 0x489B D26C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-444. Register Call Summary for Register VIP_PERF_MON27

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-445. VIP_PERF_MON28

Address Offset	0x0000 0270		
Physical Address	0x4897 D270 0x4899 D270 0x489B D270	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-446. Register Call Summary for Register VIP_PERF_MON28

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-447. VIP_PERF_MON29

Address Offset	0x0000 0274		
Physical Address	0x4897 D274 0x4899 D274 0x489B D274	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-448. Register Call Summary for Register VIP_PERF_MON29

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-449. VIP_PERF_MON30

Address Offset	0x0000 0278		
Physical Address	0x4897 D278 0x4899 D278 0x489B D278	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE		STOP_CLIENT		RESERVED		STOP_COUNT		RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT																	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-450. Register Call Summary for Register VIP_PERF_MON30

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-451. VIP_PERF_MON31

Address Offset	0x0000 027C		
Physical Address	0x4897 D27C 0x4899 D27C 0x489B D27C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-452. Register Call Summary for Register VIP_PERF_MON31

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-453. VIP_PERF_MON32

Address Offset	0x0000 0280		
Physical Address	0x4897 D280 0x4899 D280 0x489B D280	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3: vip1_lo_y	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3: vip1_lo_y	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-454. Register Call Summary for Register VIP_PERF_MON32

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-455. VIP_PERF_MON33

Address Offset	0x0000 0284		
Physical Address	0x4897 D284 0x4899 D284 0x489B D284	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: vip1_lo_y 3: vip1_lo_uv	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: vip1_lo_y 3: vip1_lo_uv	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-456. Register Call Summary for Register VIP_PERF_MON33

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-457. VIP_PERF_MON34

Address Offset	0x0000 0288		
Physical Address	0x4897 D288 0x4899 D288 0x489B D288	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_lo_y 1: 2: vip1_lo_uv 3: vip1_up_y	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_lo_y 1: 2: vip1_lo_uv 3: vip1_up_y	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-458. Register Call Summary for Register VIP_PERF_MON34

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-459. VIP_PERF_MON35

Address Offset	0x0000 028C		
Physical Address	0x4897 D28C 0x4899 D28C 0x489B D28C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE			STOP_CLIENT		RESERVED		STOP_COUNT			RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT														

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_lo_uv 1: vip1_lo_y 2: vip1_up_y 3: vip1_up_uv	RW	0x0
27	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_lo_uv 1: vip1_lo_y 2: vip1_up_y 3: vip1_up_uv	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-460. Register Call Summary for Register VIP_PERF_MON35

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-461. VIP_PERF_MON36

Address Offset	0x0000 0290		
Physical Address	0x4897 D290 0x4899 D290 0x489B D290	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				START_CLIENT				RESERVED				START_COUNT				CURR_COUNT							

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_up_y 1: vip1_lo_uv 2: vip1_up_uv 3: vip2_lo_y	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_up_y 1: vip1_lo_uv 2: vip1_up_uv 3: vip2_lo_y	RW	0x0
19	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-462. Register Call Summary for Register VIP_PERF_MON36

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-463. VIP_PERF_MON37

Address Offset	0x0000 0294		
Physical Address	0x4897 D294 0x4899 D294 0x489B D294	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_up_uv 1: vip1_up_y 2: vip2_lo_y 3: vip2_lo_uv	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT		RW	0x0
23:22	RESERVED	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_up_uv 1: vip1_up_y 2: vip2_lo_y 3: vip2_lo_uv	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-464. Register Call Summary for Register VIP_PERF_MON37

VIP Register Manual
- VIP VPDMA Register Summary: [0]

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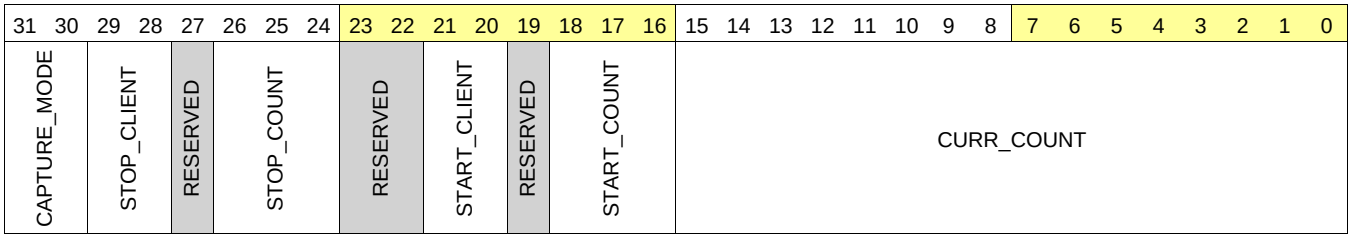
Table 9-465. VIP_PERF_MON38

Address Offset	0x0000 0298		
Physical Address	0x4897 D298 0x4899 D298 0x489B D298	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_lo_y 1: vip1_up_uv 2: vip2_lo_uv 3: vip2_up_y	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_lo_y 1: vip1_up_uv 2: vip2_lo_uv 3: vip2_up_y	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-466. Register Call Summary for Register VIP_PERF_MON38

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-467. VIP_PERF_MON39

Address Offset	0x0000 029C		
Physical Address	0x4897 D29C 0x4899 D29C 0x489B D29C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_lo_uv 1: vip2_lo_y 2: vip2_up_y 3: vip2_up_uv	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_lo_uv 1: vip2_lo_y 2: vip2_up_y 3: vip2_up_uv	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-468. Register Call Summary for Register VIP_PERF_MON39

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-469. VIP_PERF_MON40

Address Offset	0x0000 02A0		
Physical Address	0x4897 D2A0 0x4899 D2A0 0x489B D2A0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_up_y 1: vip2_lo_uv 2: vip2_up_uv 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_up_y 1: vip2_lo_uv 2: vip2_up_uv 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-470. Register Call Summary for Register VIP_PERF_MON40

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-471. VIP_PERF_MON41

Address Offset	0x0000 02A4		
Physical Address	0x4897 D2A4 0x4899 D2A4 0x489B D2A4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE				STOP_CLIENT				RESERVED				START_CLIENT				RESERVED				START_COUNT				CURR_COUNT							

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_up_uv 1: vip2_up_y 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0

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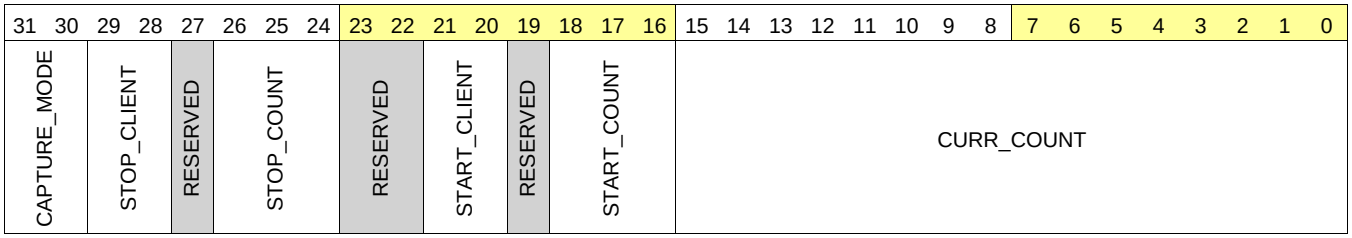
Bits	Field Name	Description	Type	Reset
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_up_uv 1: vip2_up_y 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-472. Register Call Summary for Register VIP_PERF_MON41

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-473. VIP_PERF_MON42

Address Offset	0x0000 02A8		
Physical Address	0x4897 D2A8 0x4899 D2A8 0x489B D2A8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: vip2_up_uv 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: vip2_up_uv 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-474. Register Call Summary for Register VIP_PERF_MON42

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-475. VIP_PERF_MON43

Address Offset	0x0000 02AC		
Physical Address	0x4897 D2AC 0x4899 D2AC 0x489B D2AC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-476. Register Call Summary for Register VIP_PERF_MON43

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-477. VIP_PERF_MON44

Address Offset	0x0000 02B0		
Physical Address	0x4897 D2B0 0x4899 D2B0 0x489B D2B0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-478. Register Call Summary for Register VIP_PERF_MON44

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-479. VIP_PERF_MON45

Address Offset	0x0000 02B4		
Physical Address	0x4897 D2B4 0x4899 D2B4 0x489B D2B4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-480. Register Call Summary for Register VIP_PERF_MON45

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-481. VIP_PERF_MON46

Address Offset	0x0000 02B8		
Physical Address	0x4897 D2B8 0x4899 D2B8 0x489B D2B8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-482. Register Call Summary for Register VIP_PERF_MON46

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-483. VIP_PERF_MON47

Address Offset	0x0000 02BC		
Physical Address	0x4897 D2BC 0x4899 D2BC 0x489B D2BC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-484. Register Call Summary for Register VIP_PERF_MON47

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-485. VIP_PERF_MON48

Address Offset	0x0000 02C0		
Physical Address	0x4897 D2C0 0x4899 D2C0 0x489B D2C0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-486. Register Call Summary for Register VIP_PERF_MON48

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-487. VIP_PERF_MON49

Address Offset	0x0000 02C4		
Physical Address	0x4897 D2C4 0x4899 D2C4 0x489B D2C4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-488. Register Call Summary for Register VIP_PERF_MON49

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-489. VIP_PERF_MON50

Address Offset	0x0000 02C8		
Physical Address	0x4897 D2C8 0x4899 D2C8 0x489B D2C8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3: vpi_ctl	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3: vpi_ctl	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-490. Register Call Summary for Register VIP_PERF_MON50

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-491. VIP_PERF_MON51

Address Offset	0x0000 02CC		
Physical Address	0x4897 D2CC 0x4899 D2CC 0x489B D2CC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_MODE		STOP_CLIENT		RESERVED		STOP_COUNT		RESERVED		START_CLIENT		RESERVED		START_COUNT		CURR_COUNT																	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: vpi_ctl 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: vpi_ctl 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-492. Register Call Summary for Register VIP_PERF_MON51

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-493. VIP_PERF_MON52

Address Offset	0x0000 02D0		
Physical Address	0x4897 D2D0 0x4899 D2D0 0x489B D2D0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vpi_ctl 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vpi_ctl 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-494. Register Call Summary for Register VIP_PERF_MON52

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-495. VIP_PERF_MON53

Address Offset	0x0000 02D4		
Physical Address	0x4897 D2D4 0x4899 D2D4 0x489B D2D4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: vpi_ctl 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: vpi_ctl 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-496. Register Call Summary for Register VIP_PERF_MON53

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-497. VIP_PERF_MON54

Address Offset	0x0000 02D8		
Physical Address	0x4897 D2D8 0x4899 D2D8 0x489B D2D8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-498. Register Call Summary for Register VIP_PERF_MON54

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-499. VIP_PERF_MON55

Address Offset	0x0000 02DC		
Physical Address	0x4897 D2DC 0x4899 D2DC 0x489B D2DC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-500. Register Call Summary for Register VIP_PERF_MON55

VIP Register Manual
- VIP VPDMA Register Summary: [0]

Table 9-501. VIP_PERF_MON56

Address Offset	0x0000 02E0		
Physical Address	0x4897 D2E0 0x4899 D2E0 0x489B D2E0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT		RW	0x0
27	RESERVED	Sets the client whose event stops the performance monitor counter. 0: 1: 2: 3: vip1_anc_a	R	0x0
26:24	STOP_COUNT		RW	0x0
23:22	RESERVED	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	R	0x0

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Bits	Field Name	Description	Type	Reset
21:20	START_CLIENT		RW	0x0
19	RESERVED	Sets the client whose event starts the performance monitor counter. 0: 1: 2: 3: vip1_anc_a	R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

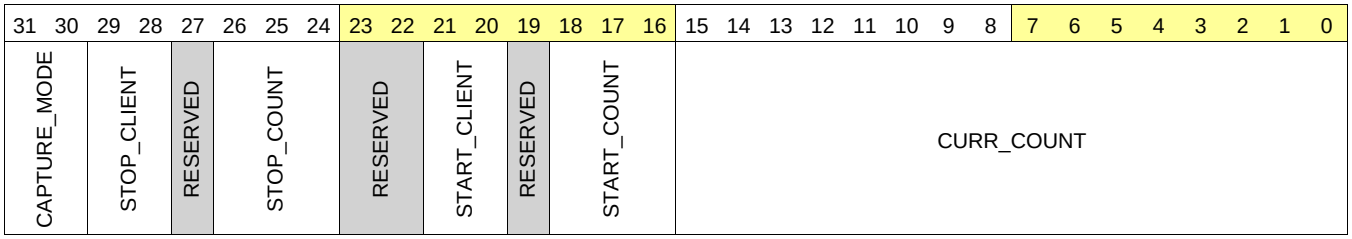
Table 9-502. Register Call Summary for Register VIP_PERF_MON56

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-503. VIP_PERF_MON57

Address Offset	0x0000 02E4		
Physical Address	0x4897 D2E4 0x4899 D2E4 0x489B D2E4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: 1: 2: vip1_anc_a 3: vip1_anc_b	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: 1: 2: vip1_anc_a 3: vip1_anc_b	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

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Table 9-504. Register Call Summary for Register VIP_PERF_MON57

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-505. VIP_PERF_MON58

Address Offset	0x0000 02E8		
Physical Address	0x4897 D2E8 0x4899 D2E8 0x489B D2E8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_anc_a 1: 2: vip1_anc_b 3: vip2_anc_a	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_anc_a 1: 2: vip1_anc_b 3: vip2_anc_a	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-506. Register Call Summary for Register VIP_PERF_MON58

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-507. VIP_PERF_MON59

Address Offset	0x0000 02EC		
Physical Address	0x4897 D2EC 0x4899 D2EC 0x489B D2EC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA

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Table 9-507. VIP_PERF_MON59 (continued)

Description	The register can be used to capture timing differences between events in the VPDMA\\n
Type	RW

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip1_anc_b 1: vip1_anc_a 2: vip2_anc_a 3: vip2_anc_b	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip1_anc_b 1: vip1_anc_a 2: vip2_anc_a 3: vip2_anc_b	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-508. Register Call Summary for Register VIP_PERF_MON59

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-509. VIP_PERF_MON60

Address Offset	0x0000 02F0		
Physical Address	0x4897 D2F0 0x4899 D2F0 0x489B D2F0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

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31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_anc_a 1: vip1_anc_b 2: vip2_anc_b 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_anc_a 1: vip1_anc_b 2: vip2_anc_b 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-510. Register Call Summary for Register VIP_PERF_MON60

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-511. VIP_PERF_MON61

Address Offset	0x0000 02F4		
Physical Address	0x4897 D2F4 0x4899 D2F4 0x489B D2F4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register can be used to capture timing differences between events in the VPDMA\\n		
Type	RW		

31 30	29 28	27	26 25 24	23 22	21 20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPTURE_MODE	STOP_CLIENT	RESERVED	STOP_COUNT	RESERVED	START_CLIENT	RESERVED	START_COUNT	CURR_COUNT	

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Bits	Field Name	Description	Type	Reset
31:30	CAPTURE_MODE	Sets how the counter should be updated. Updating this value will also clear the current counter stored value. 0: Running Average 1: Minimum Value 2: Maximum Value 3: Last Value	RW	0x0
29:28	STOP_CLIENT	Sets the client whose event stops the performance monitor counter. 0: vip2_anc_b 1: vip2_anc_a 2: 3:	RW	0x0
27	RESERVED		R	0x0
26:24	STOP_COUNT	Sets the value that stops the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
23:22	RESERVED		R	0x0
21:20	START_CLIENT	Sets the client whose event starts the performance monitor counter. 0: vip2_anc_b 1: vip2_anc_a 2: 3:	RW	0x0
19	RESERVED		R	0x0
18:16	START_COUNT	Sets the value that starts the performance monitor counter. 0: command request 1: command accept 2: data request 3: data rcvd 4: data empty 5: data full 6: frame start 7: frame end	RW	0x0
15:0	CURR_COUNT	The current value of the perfomance monitor counter	R	0x0

Table 9-512. Register Call Summary for Register VIP_PERF_MON61

VIP Register Manual

- VIP VPDMA Register Summary: [0]

Table 9-513. VIP0_LO_Y_CSTAT

Address Offset	0x0000 0388		
Physical Address	0x4897 D388 0x4899 D388 0x489B D388	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11 10	9 8	7 6 5 4 3 2 1 0
REQ_DELAY	REQ_RATE	BUSY	DMA_ACTIVE	FRAME_START	RESERVED	

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0

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Bits	Field Name	Description	Type	Reset
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-514. Register Call Summary for Register VIP0_LO_Y_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-515. VIP0_LO_UV_CSTAT

Address Offset	0x0000 038C		
Physical Address	0x4897 D38C 0x4899 D38C 0x489B D38C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:0	RESERVED		R	0x0

Table 9-516. Register Call Summary for Register VIP0_LO_UV_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-517. VIP0_UP_Y_CSTAT

Address Offset	0x0000 0390		
Physical Address	0x4897 D390 0x4899 D390 0x489B D390	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11 10	9 8	7 6 5 4 3 2 1 0
REQ_DELAY	REQ_RATE	BUSY	DMA_ACTIVE	FRAME_START		RESERVED

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

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Table 9-518. Register Call Summary for Register VIP0_UP_Y_CSTAT

VIP Functional Description • VPDMA Basic Definitions:
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-519. VIP0_UP_UV_CSTAT

Address Offset	0x0000 0394		
Physical Address	0x4897 D394 0x4899 D394 0x489B D394	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-520. Register Call Summary for Register VIP0_UP_UV_CSTAT

VIP Functional Description • VPDMA Basic Definitions:
VIP Register Manual • VIP VPDMA Register Summary: [1]

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Table 9-521. VIP1_LO_Y_CSTAT

Address Offset	0x0000 0398		
Physical Address	0x4897 D398 0x4899 D398 0x489B D398	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-522. Register Call Summary for Register VIP1_LO_Y_CSTAT

VIP Functional Description

- VPDMA Basic Definitions:

VIP Register Manual

- VIP VPDMA Register Summary: [1]

Table 9-523. VIP1_LO_UV_CSTAT

Address Offset	0x0000 039C		
Physical Address	0x4897 D39C 0x4899 D39C 0x489B D39C	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-524. Register Call Summary for Register VIP1_LO_UV_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-525. VIP1_UP_Y_CSTAT

Address Offset	0x0000 03A0		
Physical Address	0x4897 D3A0 0x4899 D3A0 0x489B D3A0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

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Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-526. Register Call Summary for Register VIP1_UP_Y_CSTAT

VIP Functional Description • VPDMA Basic Definitions:
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-527. VIP1_UP_UV_CSTAT

Address Offset	0x0000 03A4		
Physical Address	0x4897 D3A4 0x4899 D3A4 0x489B D3A4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0

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Bits	Field Name	Description	Type	Reset
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-528. Register Call Summary for Register VIP1_UP_UV_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-529. VPI_CTL_CSTAT

Address Offset	0x0000 03D0		
Physical Address	0x4897 D3D0 0x4899 D3D0 0x489B D3D0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11 10	9 8	7 6 5 4 3 2 1 0
REQ_DELAY	REQ_RATE	BUSY	DMA_ACTIVE	FRAME_START	RESERVED	

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0

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Bits	Field Name	Description	Type	Reset
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-530. Register Call Summary for Register VPI_CTL_CSTAT

VIP Functional Description • VPDMA Basic Definitions:
VIP Register Manual • VIP VPDMA Register Summary: [1]

Table 9-531. VIP0_ANC_A_CSTAT

Address Offset	0x0000 03E8		
Physical Address	0x4897 D3E8 0x4899 D3E8 0x489B D3E8	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11 10	9 8	7 6 5 4 3 2 1 0
REQ_DELAY	REQ_RATE	BUSY	DMA_ACTIVE	FRAME_START		RESERVED

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:0	RESERVED		R	0x0

Table 9-532. Register Call Summary for Register VIP0_ANC_A_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

Table 9-533. VIP0_ANC_B_CSTAT

Address Offset	0x0000 03EC		
Physical Address	0x4897 D3EC 0x4899 D3EC 0x489B D3EC	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START				RESERVED									

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

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Table 9-534. Register Call Summary for Register VIP0_ANC_B_CSTAT

VIP Functional Description
• VPDMA Basic Definitions:
VIP Register Manual
• VIP VPDMA Register Summary: [1]

Table 9-535. VIP1_ANC_A_CSTAT

Address Offset	0x0000 03F0		
Physical Address	0x4897 D3F0 0x4899 D3F0 0x489B D3F0	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles..This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-536. Register Call Summary for Register VIP1_ANC_A_CSTAT

VIP Functional Description
• VPDMA Basic Definitions:
VIP Register Manual
• VIP VPDMA Register Summary: [1]

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Table 9-537. VIP1_ANC_B_CSTAT

Address Offset	0x0000 03F4		
Physical Address	0x4897 D3F4 0x4899 D3F4 0x489B D3F4	**Instance**	VIP1_VPDMA VIP2_VPDMA VIP3_VPDMA
Description	The register holds status information and control for the client.\\n		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DELAY								REQ_RATE								BUSY	DMA_ACTIVE	FRAME_START						RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	REQ_DELAY	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.	RW	0x0
23:16	REQ_RATE	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.	R	0x0
15	BUSY	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.	R	0x0
14	DMA_ACTIVE	Signals if the client is currently actively sending DMA requests	R	0x0
13:10	FRAME_START	The source of the start frame event for the client.\\n0 : Change in value of hdmi_field_id\\n1 : Change in value of dvo2_field_id\\n2 : Change in value of hdcomp_field_id\\n3 : Change in value of sd_field_id\\n4 : Use List Manager Internal Field0\\n5 : Use List Manager Internal Field1\\n6 : Use List Manager Internal Field2\\n7 : Start on channel active	RW	0x0
9:0	RESERVED		R	0x0

Table 9-538. Register Call Summary for Register VIP1_ANC_B_CSTAT

VIP Functional Description
- VPDMA Basic Definitions:

VIP Register Manual
- VIP VPDMA Register Summary: [1]

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