2D Graphics Accelerator

This chapter describes the advanced bit blitter 2-dimensional (2D) graphics accelerator (BB2D) for the device.

NOTE: The BB2D subsystem is an instantiation by Texas Instruments of the GC320™ core from Vivante Corp.

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NOTE: This chapter describes a module (subsystem) in the superset device. The availability is device part number dependent. Refer to device Data Manual, for more information.

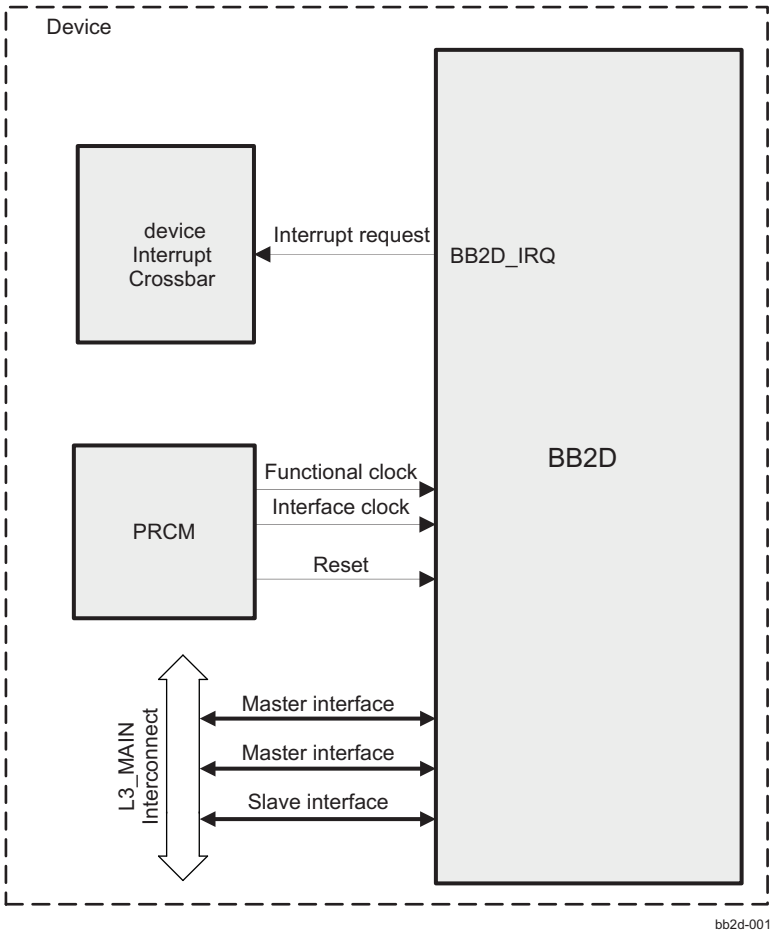
Topic **Page**

13.1 BB2D Overview

The 2D graphics accelerator subsystem accelerates 2D graphics applications. The 2D graphics accelerator subsystem is based on the GC320 2D GPU core from Vivante Corporation. The hardware acceleration is brought to numerous 2D applications, including on-screen display and touch screen user interfaces, graphical user interfaces (GUIs) and menu displays, flash animation, and gaming.

Figure 13-1 shows the BB2D subsystem.

Figure 13-1. BB2D Overview



13.1.1 BB2D Key Features Overview

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw™
- **BB2D architecture:**
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Clipping rectangle support
  - Alpha blending includes Java® 2 Porter-Duff compositing rules
  - 90-, 180-, 270-degree rotation on every primitive
  - YUV-to-RGB color space conversion
  - Programmable display format conversion with 14 source and 7 destination formats

  - High-quality 9-tap, 32-phase filter for image and video scaling at 1080p
  - Monochrome expansion for text rendering
  - 32 K × 32 K coordinate system
- **Hardware acceleration for DirectFB**:
  - High-speed video scaler
  - ROP2/3/4
  - Rectangle filling and drawing
  - Line drawing
  - Simple blitting
  - Stretch blitting
  - Blending with alpha channel (per-pixel alpha)
  - Blending with alpha factor (alpha modulation)
  - Nine source and destination blending functions
  - Porter-Duff rules support
  - Premultiplied alpha support
  - Colorized blitting (color modulation)
  - Source color keying
  - Destination color keying

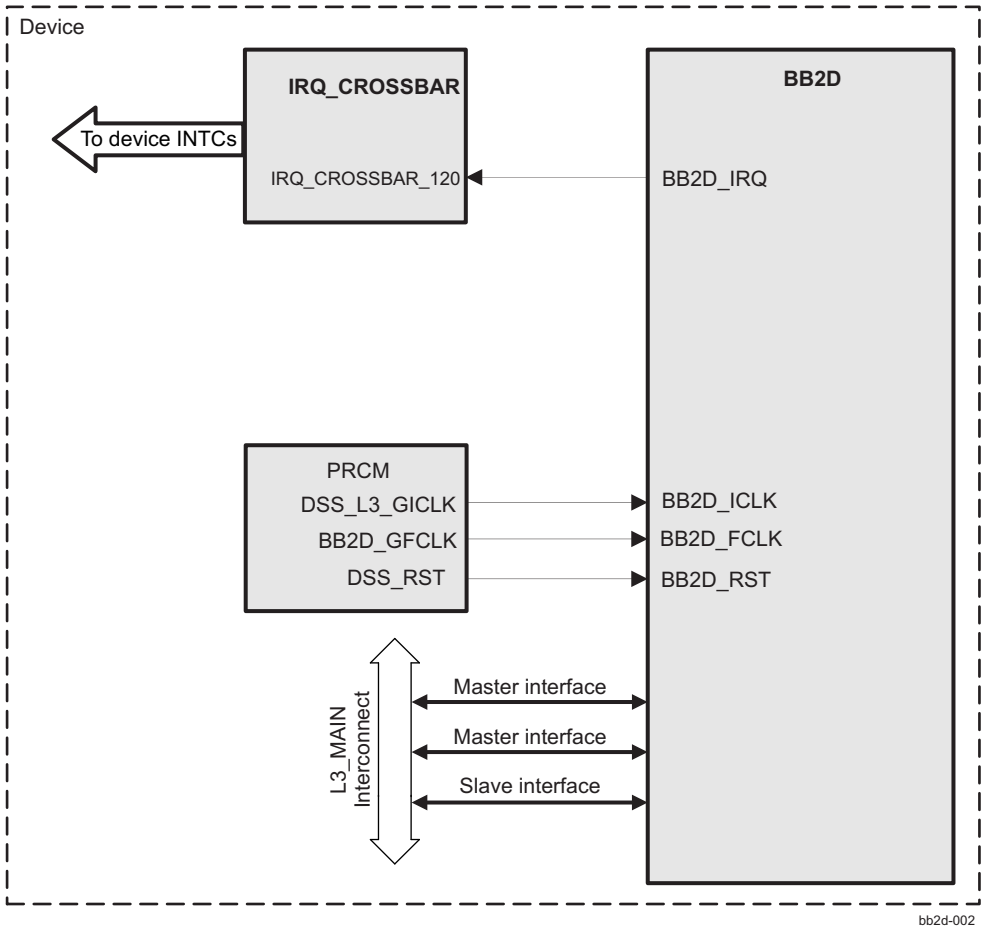
The device BB2D generates a single (aggregate) interrupt request connected to the device Interrupt Crossbar. This allows for this interrupt to be programmatically mapped to multiple device host interrupt controllers (see Section 13.2).

13.2 BB2D Integration

This section describes subsystem integration in the device, including information about clocks, resets, and hardware requests.

Figure 13-2 shows BB2D integration.

Figure 13-2. BB2D Integration



The BB2D subsystem is connected to the level 3 (L3_MAIN) interconnect by two 128-bit master interfaces and one 32-bit slave interface.

Table 13-1 through Table 13-3 summarize the integration of the subsystem in the device.

Table 13-1. BB2D Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
BB2D	PD_DSS	L3_MAIN

Table 13-2. BB2D Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
BB2D	BB2D_ICLK	DSS_L3_GICLK	PRCM	BB2D interfaces clock
	BB2D_FCLK	BB2D_GFCLK	PRCM	BB2D functional clock.
Resets				

Table 13-2. BB2D Clocks and Resets (continued)

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
BB2D	BB2D_RST	DSS_RST	PRCM	BB2D non-retention reset signal

Table 13-3. BB2D Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination IRQ_CROSSBAR Input**	**Default Mapping**	**Description**
BB2D	BB2D_IRQ	IRQ_CROSSBAR_120	MPU_IRQ_125 IPU1_IRQ_65 IPU2_IRQ_65	BB2D interrupt request to the device interrupt crossbar

NOTE: The "**Default Mapping**" column in Table 13-3, *BB2D Hardware Requests* shows the default mapping of module IRQ source signals. These IRQ source signals can also be mapped to other lines of each device Interrupt controller through the IRQ_CROSSBAR module.
For more information about the IRQ_CROSSBAR module, see Section 18.4.6.4, *IRQ_CROSSBAR Module Functional Description*, in Chapter 18, *Control Module*.
For more information about the device interrupt controllers, see Chapter 17, *Interrupt Controllers*.

NOTE: No DMA and no wake-up requests are generated by the BB2D module.

13.3 BB2D Functional Description

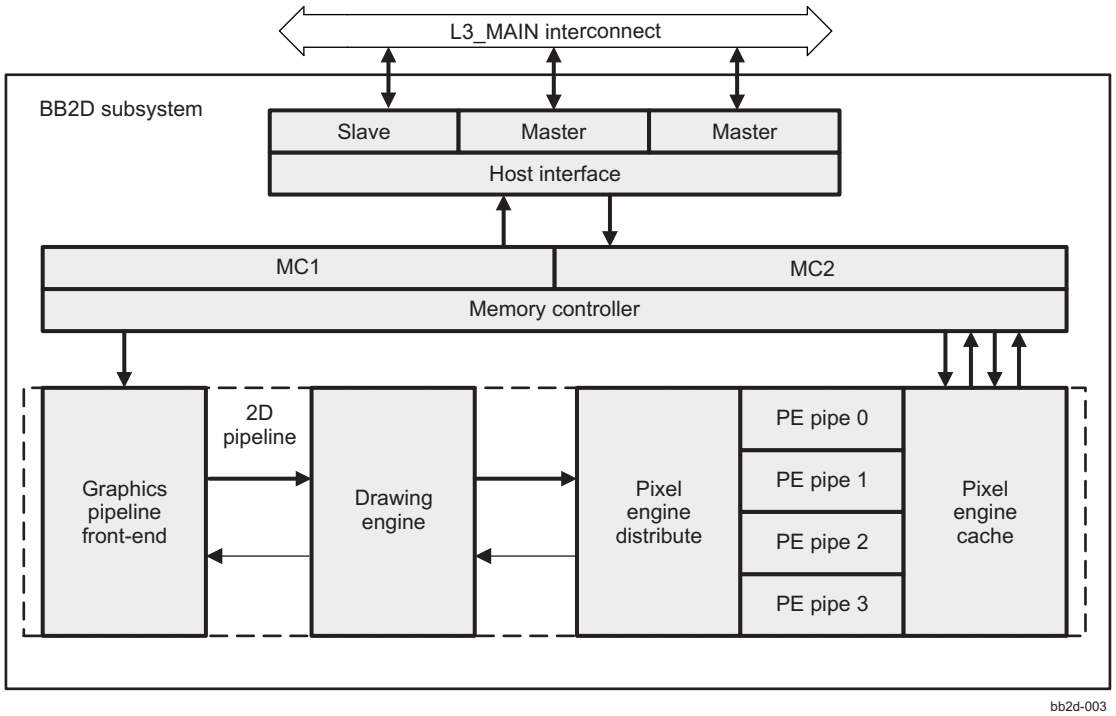
13.3.1 BB2D Block Diagram

The BB2D subsystem is based on the following main blocks:

- Host interface: Allows the BB2D core to communicate with external memory and the MPU through the L3_MAIN interconnect. In this block, data crosses clock domain boundaries.
- Memory controller: Internal memory unit that is the block-to-host interface for memory requests
- Graphics pipeline front-end: Inserts high-level primitives and commands into the graphics pipeline.
- 2D drawing and scaling engine: Draws 2D graphics primitives and rasterizes 2D images.
- Pixel engine: manipulates and filters pixels in rendered images. BB2D has four pixel pipes.

Figure 13-3 shows the BB2D top-level block diagram.

Figure 13-3. BB2D Block Diagram



13.3.2 BB2D Clock Configuration

The BB2D subsystem operates from two clocks: an interface clock (BB2D_ICLK) and functional clock (BB2D_FCLK). The power, reset, and clock management (PRCM) module generates and distributes the clocks inside the device.

- The BB2D_ICLK interface clock manages the data transfer on the L3_MAIN master and slave ports.

  The BB2D_ICLK frequency is selected based on the whole device L3_MAIN interconnect clock frequency. For more information on the interface clock, see Section 3.9.14, *CD_DSS Clock Domain* , in the chapter, *Power, Reset and Clock Management* .

  When BB2D_ICLK is no longer required by the BB2D subsystem, it can be disabled by software at the PRCM level.

  NOTE: BB2D_ICLK is cut only if the BB2D is ready to go into IDLE state.

- The BB2D_FCLK functional clock is used inside the BB2D subsystem to generate clock signals to multiple BB2D clock domains. The BB2D automatically gates clocks to domains, that are not currently in use.

Using the clock source selection and the DPLL settings, the frequency of BB2D_FCLK can be adjusted.

When BB2D_FCLK is no longer needed by the BB2D subsystem, it can be cut by software at the PRCM level, if the module is ready to enter IDLE state.

13.3.3 BB2D Software Reset

The BB2D subsystem is part of the DSS reset domain. A global reset of the BB2D is performed by activating the BB2D_RST signal in the DSS_RST domain.

NOTE: The APIs delivered with the BB2D provide a software reset functionally equivalent to a hardware reset.

13.3.4 BB2D Power Management

The BB2D subsystem is part of the DSS power domain (PD_DSS). For additional information about PD_DSS, see Section 3.10.12, *PD_DSS Description* in the Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The BB2D handles automatic clock gating performed on the multiple internal clock domains.

When 2D operations are complete, software may set the GCGPOUT0[0] GCHOLD bit to 1 to enter a low-power state. Setting GCHOLD to 1 moves the BB2D operational state into IDLE. Once in IDLE state, the system standby hardware signal (mstandby) is asserted.

13.4 BB2D Register Manual

CAUTION

All BB2D registers are limited to 32-bit data accesses; 8- and 16-bit accesses are not allowed because they can corrupt register content.

13.4.1 BB2D Instance Summary

Table 13-4. BB2D Instance Summary

Module Name	Base Address	Size
BB2D	0x5900 0000	2 KiB

13.4.2 BB2D Registers

13.4.2.1 BB2D Register Summary

Table 13-5. BB2D Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
AQHICLOCKCONTROL	RW	32	0x0000 0000	0x5900 0000
AQHIIDLE	R	32	0x0000 0004	0x5900 0004
AQAXICONFIG	RW	32	0x0000 0008	0x5900 0008
AQAXISTATUS	R	32	0x0000 000C	0x5900 000C
AQINTRACKNOWLEDGE	R	32	0x0000 0010	0x5900 0010
AQINTRENBL	RW	32	0x0000 0014	0x5900 0014
AQIDENT	R	32	0x0000 0018	0x5900 0018
GCFEATURES	R	32	0x0000 001C	0x5900 001C
GCCHIPID	R	32	0x0000 0020	0x5900 0020
GCCHIPREV	R	32	0x0000 0024	0x5900 0024
GCCHIPDATE	R	32	0x0000 0028	0x5900 0028
GCCHIPTIME	R	32	0x0000 002C	0x5900 002C
GCCHIPCUSTOMER	R	32	0x0000 0030	0x5900 0030
GCMINORFEATURES0	R	32	0x0000 0034	0x5900 0034
GCRESETMEMCOUNTERS	W	32	0x0000 003C	0x5900 003C
GCTOTALREADS	R	32	0x0000 0040	0x5900 0040
GCTOTALWRITES	R	32	0x0000 0044	0x5900 0044
GCCHIPSPECS	R	32	0x0000 0048	0x5900 0048
GCTOTALWRITEBURSTS	R	32	0x0000 004C	0x5900 004C
GCTOTALWRITEREQS	R	32	0x0000 0050	0x5900 0050
GCTOTALWRITELASTS	R	32	0x0000 0054	0x5900 0054
GCTOTALREADBURSTS	R	32	0x0000 0058	0x5900 0058
GCTOTALREADREQS	R	32	0x0000 005C	0x5900 005C
GCTOTALREADLASTS	R	32	0x0000 0060	0x5900 0060
GCGPOUT0	RW	32	0x0000 0064	0x5900 0064
RESERVED	RW	32	0x0000 0068	0x5900 0068
RESERVED	RW	32	0x0000 006C	0x5900 006C
GCAXICONTROL	RW	32	0x0000 0070	0x5900 0070
GCMINORFEATURES1	R	32	0x0000 0074	0x5900 0074

Table 13-5. BB2D Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
GCTOTALCYCLES	RW	32	0x0000 0078	0x5900 0078
GCTOTALIDLECYCLES	RW	32	0x0000 007C	0x5900 007C
GCCHIPSPECS2	R	32	0x0000 0080	0x5900 0080
GCMINORFEATURES2	R	32	0x0000 0084	0x5900 0084
GCMODULEPOWERCONTROLS	RW	32	0x0000 0100	0x5900 0100
GCMODULEPOWERMODULECONTROL	RW	32	0x0000 0104	0x5900 0104
GCMODULEPOWERMODULESTATUS	R	32	0x0000 0108	0x5900 0108
GCREGMMUSTATUS	R	32	0x0000 0188	0x5900 0188
GCREGMMUCONTROL	W	32	0x0000 018C	0x5900 018C
GCREGMMUEXCEPTION0	RW	32	0x0000 0190	0x5900 0190
GCREGMMUEXCEPTION1	RW	32	0x0000 0194	0x5900 0194
GCREGMMUEXCEPTION2	RW	32	0x0000 0198	0x5900 0198
GCREGMMUEXCEPTION3	RW	32	0x0000 019C	0x5900 019C
AQMEMORYDEBUG	RW	32	0x0000 0414	0x5900 0414
AQREGISTERTIMINGCONTROL	RW	32	0x0000 042C	0x5900 042C
RESERVED	R	32	0x0000 0430	0x5900 0430
GCDISPLAYPRIORITY	RW	32	0x0000 0434	0x5900 0434
GCDBGCYCLECOUNTER	RW	32	0x0000 0438	0x5900 0438
GCOUTSTANDINGREADS0	R	32	0x0000 043C	0x5900 043C
GCOUTSTANDINGREADS1	R	32	0x0000 0440	0x5900 0440
GCOUTSTANDINGWRITES	R	32	0x0000 0444	0x5900 0444
GCDEBUGSIGNALSRA	R	32	0x0000 0448	0x5900 0448
GCDEBUGSIGNALSTX	R	32	0x0000 044C	0x5900 044C
GCDEBUGSIGNALSFE	R	32	0x0000 0450	0x5900 0450
GCDEBUGSIGNALSPE	R	32	0x0000 0454	0x5900 0454
GCDEBUGSIGNALSDE	R	32	0x0000 0458	0x5900 0458
GCDEBUGSIGNALSSH	R	32	0x0000 045C	0x5900 045C
GCDEBUGSIGNALSPA	R	32	0x0000 0460	0x5900 0460
GCDEBUGSIGNALSSE	R	32	0x0000 0464	0x5900 0464
GCDEBUGSIGNALSMC	R	32	0x0000 0468	0x5900 0468
GCDEBUGSIGNALSHI	R	32	0x0000 046C	0x5900 046C
GCDEBUGCONTROL0	RW	32	0x0000 0470	0x5900 0470
GCDEBUGCONTROL1	RW	32	0x0000 0474	0x5900 0474
GCDEBUGCONTROL2	RW	32	0x0000 0478	0x5900 0478
GCDEBUGCONTROL3	RW	32	0x0000 047C	0x5900 047C
GCBUSCONTROL	RW	32	0x0000 0480	0x5900 0480
GCREGENDIANNESS0	RW	32	0x0000 0484	0x5900 0484
GCREGENDIANNESS1	RW	32	0x0000 0488	0x5900 0488
GCREGENDIANNESS2	RW	32	0x0000 048C	0x5900 048C
GCREGDRAWPRIMITIVESTARTTIMESTAMP	R	32	0x0000 0490	0x5900 0490
GCREGDRAWPRIMITIVEENDTIMESTAMP	R	32	0x0000 0494	0x5900 0494
GCREGCONTROL0	RW	32	0x0000 0558	0x5900 0558
AQCMDBUFFERADDR	W	32	0x0000 0654	0x5900 0654
AQCMDBUFFERCTRL	W	32	0x0000 0658	0x5900 0658
AQFESTATUS	R	32	0x0000 065C	0x5900 065C
RESERVED	R	32	0x0000 0660	0x5900 0660

Table 13-5. BB2D Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
AQFEDEBUGCURCMDADR	R	32	0x0000 0664	0x5900 0664
RESERVED	R	32	0x0000 0668	0x5900 0668
RESERVED	R	32	0x0000 066C	0x5900 066C

13.4.2.2 BB2D Register Description

Table 13-6. AQHICLOCKCONTROL

Address Offset	0x0000 0000		
Physical Address	0x5900 0000	**Instance**	BB2D
Description	Clock control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MULTI_PIPE_USE_SINGLE_AXI				MULTI_PIPE_REG_SELECT				ISOLATE_GPU	IDLE_VG	IDLE2_D	IDLE3_D	RESERVED			SOFT_RESET	DISABLE_DEBUG_REGISTERS	DISABLE_RAM_CLOCK_GATING	FSCALE_CMD_LOAD	FSCALE_VAL							CLK2D_DIS	CLK3D_DIS

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	MULTI_PIPE_USE_SINGLE_AXI	Force all the transactions to go to one AXI	RW	0x0
23:20	MULTI_PIPE_REG_SELECT	Determines which HI/MC to use while reading registers	RW	0x0
19	ISOLATE_GPU	Isolate GPU bit	RW	0
18	IDLE_VG	VG pipe is idle	R	1
17	IDLE2_D	2D pipe is idle	R	1
16	IDLE3_D	3D pipe is idle	R	1
15:13	RESERVED		R	0x0
12	SOFT_RESET	Soft resets the subsystem	RW	0
11	DISABLE_DEBUG_REGISTERS	Disable debug registers. If this bit is 1, debug registers are clock gated	RW	0
10	DISABLE_RAM_CLOCK_GATING	Disables clock gating for RAMs	RW	0
9	FSCALE_CMD_LOAD		RW	0
8:2	FSCALE_VAL		RW	0x40
1	CLK2D_DIS	Disable 2D clock	RW	0
0	CLK3D_DIS	Disable 3D clock	RW	0

Table 13-7. Register Call Summary for Register AQHICLOCKCONTROL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-8. AQHIIDLE

Address Offset	0x0000 0004		
Physical Address	0x5900 0004	**Instance**	BB2D
Description	Idle status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AXI_LP	RESERVED																			IDLE_TS	IDLE_FP	IDLE_IM	IDLE_VG	IDLE_TX	IDLE_RA	IDLE_SE	IDLE_PA	IDLE_SH	IDLE_PE	IDLE_DE	IDLE_FE

Bits	Field Name	Description	Type	Reset
31	AXI_LP	AXI is in low power mode	R	0
30:12	RESERVED	Unused bits reserved for future expansion	R	0x7 FFFF
11	IDLE_TS	TS is idle	R	1
10	IDLE_FP	FP is idle	R	1
9	IDLE_IM	IM is idle	R	1
8	IDLE_VG	VG is idle	R	1
7	IDLE_TX	TX is idle	R	1
6	IDLE_RA	RA is idle	R	1
5	IDLE_SE	SE is idle	R	1
4	IDLE_PA	PA is idle	R	1
3	IDLE_SH	SH is idle	R	1
2	IDLE_PE	PE is idle	R	1
1	IDLE_DE	DE is idle	R	1
0	IDLE_FE	FE is idle	R	1

Table 13-9. Register Call Summary for Register AQHIIDLE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-10. AQAXICONFIG

Address Offset	0x0000 0008		
Physical Address	0x5900 0008	**Instance**	BB2D
Description	AXI config		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ARCACHE				AWCACHE				ARID				AWID			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	ARCACHE		RW	0x0
11:8	AWCACHE		RW	0x0
7:4	ARID		RW	0x0
3:0	AWID		RW	0x0

Table 13-11. Register Call Summary for Register AQAXICONFIG

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-12. AQAXISTATUS

Address Offset	0x0000 000C		
Physical Address	0x5900 000C	**Instance**	BB2D
Description	AXI status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						DET_RD_ERR	DET_WR_ERR	RD_ERR_ID				WR_ERR_ID			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00 0000
9	DET_RD_ERR		R	0
8	DET_WR_ERR		R	0
7:4	RD_ERR_ID		R	0x0
3:0	WR_ERR_ID		R	0x0

Table 13-13. Register Call Summary for Register AQAXISTATUS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-14. AQINTRACKNOWLEDGE

Address Offset	0x0000 0010		
Physical Address	0x5900 0010	**Instance**	BB2D
Description	Interrupt acknowledge register. Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	INTR_VEC		R	0x0000 0000

Table 13-15. Register Call Summary for Register AQINTRACKNOWLEDGE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-16. AQINTRENBL

Address Offset	0x0000 0014		
Physical Address	0x5900 0014	**Instance**	BB2D
Description	Interrupt enable register. Each bit enables a corresponding event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_ENBL_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	INTR_ENBL_VEC		RW	0x0000 0000

Table 13-17. Register Call Summary for Register AQINTRENBL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-18. AQIDENT

Address Offset	0x0000 0018		
Physical Address	0x5900 0018	**Instance**	BB2D
Description	Identification register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAMILY								PRODUCT								REVISION				TECHNOLOGY				CUSTOMER							

Bits	Field Name	Description	Type	Reset
31:24	FAMILY	Family value 0x1: GC500 0x2: GC520 0x3: GC530 0x4: GC400 0x5: GC450 0x8: GC600 0x9: GC700 0xA: GC350 0xB: GC380 0xC: GC800 0x10: GC1000 0x14: GC2000	R	0x14
23:16	PRODUCT	Product value	R	0x01
15:12	REVISION	Revision value	R	0x0
11:8	TECHNOLOGY	Technology value	R	0x0
7:0	CUSTOMER	Customer value	R	0x00

Table 13-19. Register Call Summary for Register AQIDENT

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-20. GCFEATURES

Address Offset	0x0000 001C		
Physical Address	0x5900 001C	**Instance**	BB2D
Description	Shows which features are enabled in current subsystem implementation. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE20_BIT_INDEX	RS_YUV_TARGET	BYTE_WRITE_3D	FE20	VGTS	PIPE_VG	MEM32_BIT_SUPPORT	YUY2_RENDER_TARGET	HALF_TX_CACHE	HALF_PE_CACHE	YUY2_AVERAGING	NO_SCALER	BYTE_WRITE_2D	BUFFER_INTERLEAVING	NO422_TEXTURE	NO_EZ	MIN_AREA	MODULE_CG	YUV420_TILER	HIGH_DYNAMIC_RANGE	FAST_SCALER	ETC1_TEXTURE_COMPRESSION	PIPE_2D	DC	MSAA	YUV420_FILTER	ZCOMPRESSION	DEBUG_MODE	DXT_TEXTURE_COMPRESSION	PIPE_3D	SPECIAL_ANTI_ALIASING	FAST_CLEAR

Bits	Field Name	Description	Type	Reset
31	FE20_BIT_INDEX	Supports 20 bit index.	R	1
30	RS_YUV_TARGET	Supports resolveing into YUV target.	R	1
29	BYTE_WRITE_3D	3D PE has byte write capability.	R	1
28	FE20	FE 2.0 is present.	R	0
27	VGTS	VG tesselator is present.	R	0
26	PIPE_VG	VG pipe is present.	R	0
25	MEM32_BIT_SUPPORT	32 bit memory address support.	R	0
24	YUY2_RENDER_TARGET	YUY2 support in PE and YUY2 to RGB conversion in resolve.	R	0
23	HALF_TX_CACHE	TX cache is half.	R	0
22	HALF_PE_CACHE	PE cache is half.	R	0
21	YUY2_AVERAGING	YUY2 averaging support in resolve.	R	1
20	NO_SCALER	No 2D scaler.	R	0
19	BYTE_WRITE_2D	Supports byte write in 2D.	R	1
18	BUFFER_INTERLEAVING	Supports interleaving depth and color buffers.	R	1
17	NO422_TEXTURE	No 422 texture input format.	R	0
16	NO_EZ	No early-Z.	R	0
15	MIN_AREA	Configured to have minimum area.	R	1
14	MODULE_CG	Second level clock gating is available.	R	1
13	YUV420_TILER	YUV 4:2:0 tiler is available.	R	1
12	HIGH_DYNAMIC_RANGE	Shows if there is HDR support.	R	1
11	FAST_SCALER	Shows if there is HD scaler.	R	1
10	ETC1_TEXTURE_COMPRESSION	ETC1 texture compression.	R	1
9	PIPE_2D	Shows if there is 2D engine.	R	1
8	DC	Shows if there is a display controller.	R	0
7	MSAA	MSAA support.	R	1
6	YUV420_FILTER	YUV 4:2:0 support in filter blit.	R	1
5	ZCOMPRESSION	Depth and color compression.	R	0

Bits	Field Name	Description	Type	Reset
4	DEBUG_MODE	Debug registers.	R	0
3	DXT_TEXTURE_COMPRESSION	DXT texture compression.	R	1
2	PIPE_3D	3D pipe.	R	0
1	SPECIAL_ANTI_ALIASING	Full-screen anti-aliasing.	R	1
0	FAST_CLEAR	Fast clear.	R	0

Table 13-21. Register Call Summary for Register GCFEATURES

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-22. GCCHIPID

Address Offset	0x0000 0020		
Physical Address	0x5900 0020	**Instance**	BB2D
Description	Shows the ID for the subsystem in BCD.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															

Bits	Field Name	Description	Type	Reset
31:0	ID	Subsystem ID in BCD	R	0x0000 0320

Table 13-23. Register Call Summary for Register GCCHIPID

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-24. GCCHIPREV

Address Offset	0x0000 0024		
Physical Address	0x5900 0024	**Instance**	BB2D
Description	Shows the revision for the subsystem in BCD.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision in BCD	R	0x0000 5301

Table 13-25. Register Call Summary for Register GCCHIPREV

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-26. GCCHIPDATE

Address Offset	0x0000 0028		
Physical Address	0x5900 0028	**Instance**	BB2D
Description	Shows the release date for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATE																															

Bits	Field Name	Description	Type	Reset
31:0	DATE	Release date	R	0x2011 1103

Table 13-27. Register Call Summary for Register GCCHIPDATE

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-28. GCCHIPTIME

Address Offset	0x0000 002C		
Physical Address	0x5900 002C	**Instance**	BB2D
Description	Shows the release time for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME																															

Bits	Field Name	Description	Type	Reset
31:0	TIME	Release time	R	0x0014 0300

Table 13-29. Register Call Summary for Register GCCHIPTIME

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-30. GCCHIPCUSTOMER

Address Offset	0x0000 0030		
Physical Address	0x5900 0030	**Instance**	BB2D
Description	Shows the customer and group for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPANY																GROUP															

Bits	Field Name	Description	Type	Reset
31:16	COMPANY	Company	R	0x0000
15:0	GROUP	Group	R	0x0000

Table 13-31. Register Call Summary for Register GCCHIPCUSTOMER

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-32. GCMINORFEATURES0

Address Offset	0x0000 0034		
Physical Address	0x5900 0034	**Instance**	BB2D
Description	Shows which minor features are enabled in the subsystem. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENHANCE_VR	CORRECT_STENCIL	A8_TARGET_SUPPORT	NEW_TEXTURE	HIERARCHICAL_Z	BYPASS_IN_MSAA	VAA	BUG_FIXES0	SHADER_MSAA_SIDEBAND	MC_20	DEFAULT_REG0	EXTRA_SHADER_INSTRUCTIONS1	SHADER_GETS_W	VG_21	VG_FILTER	EXTRA_SHADER_INSTRUCTIONS0	COMPRESSION_FIFO_FIXED	TS_EXTENDED_COMMANDS	VG_20	SUPER_TILED_32X32	SEPARATE_TILE_STATUS_WHEN_INTERLEAVED	TILE_STATUS_2BITS	RENDER_8K	CORRECT_AUTO_DISABLE	PE20_2D	FAST_CLEAR_FLUSH	SPECIAL_MSAA_LOD	CORRECT_TEXTURE_CONVERTER	TEXTURE8_K	ENDIANNESS_CONFIG	DUAL_RETURN_BUS	FLIP_Y

Bits	Field Name	Description	Type	Reset
31	ENHANCE_VR	Enhance VR and add a mode to walk 16 pixels in 16-bit mode in vertical pass to improve cache hit rate when rotating 90/270.	R	1
30	CORRECT_STENCIL	Correct stencil behavior in depth only.	R	1
29	A8_TARGET_SUPPORT	2D engine supports A8 target.	R	0
28	NEW_TEXTURE	New texture unit is available.	R	0
27	HIERARCHICAL_Z	Hierarchiccal Z is supported.	R	1
26	BYPASS_IN_MSAA	Shader supports bypass mode when MSAA is enabled.	R	0
25	VAA	VAA is available or not.	R	0
24	BUG_FIXES0		R	1
23	SHADER_MSAA_SIDEBAND	Put the MSAA data into sideband fifo.	R	0
22	MC_20	New style MC with separate paths for color and depth.	R	0
21	DEFAULT_REG0	Unavailable registers will return 0.	R	1
20	EXTRA_SHADER_INSTRUCTIONS1	Sqrt, sin, cos instructions are available.	R	1
19	SHADER_GETS_W	W is sent to SH from RA.	R	1
18	VG_21	Minor updates to VG pipe (Event generation from VG, TS, PE). Tiled image support.	R	0
17	VG_FILTER	VG filter is available.	R	0
16	EXTRA_SHADER_INSTRUCTIONS0	Floor, ceil, and sign instructions are available.	R	1

Bits	Field Name	Description	Type	Reset
15	COMPRESSION_FIFO_FIXED	If this bit is not set, the FIFO counter should be set to 50. Else, the default should remain.	R	1
14	TS_EXTENDED_COMMANDS	New commands added to the tessellator.	R	0
13	VG_20	Major updates to VG pipe (TS buffer tiling. State masking.).	R	0
12	SUPER_TILED_32X32	32 × 32 super tile is available.	R	1
11	SEPARATE_TILE_STATUS_WHEN_INTERLEAVED	Use 2 separate tile status buffers in interleaved mode.	R	1
10	TILE_STATUS_2BITS	2 bits are used instead of 4 bits for tile status.	R	1
9	RENDER_8K	Supports 8K render target.	R	1
8	CORRECT_AUTO_DISABLE	Reserved.	R	0
7	PE20_2D	2D PE 2.0 is present.	R	1
6	FAST_CLEAR_FLUSH	Proper flush is done in fast clear cache.	R	1
5	SPECIAL_MSAA_LOD	Special LOD calculation when MSAA is on.	R	1
4	CORRECT_TEXTURE_CONVERTER	Driver hack is not needed.	R	1
3	TEXTURE8_K	Supports 8K × 8K textures.	R	1
2	ENDIANNESS_CONFIG	Configurable endianness support.	R	1
1	DUAL_RETURN_BUS	Dual Return Bus from HI to clients.	R	1
0	FLIP_Y	Y flipping capability is added to resolve.	R	1

Table 13-33. Register Call Summary for Register GCMINORFEATURES0

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-34. GCRESETMEMCOUNTERS

Address Offset	0x0000 003C		
Physical Address	0x5900 003C	**Instance**	BB2D
Description	Writing 1 will reset the counters and stop counting. Write 0 to start counting again.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		W	0x649C CF7F
0	RESET	1: reset the counters and stop counting 0: start counting	W	1

Table 13-35. Register Call Summary for Register GCRESETMEMCOUNTERS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-36. GCTOTALREADS

Address Offset	0x0000 0040		
Physical Address	0x5900 0040	**Instance**	BB2D
Description	Total reads in terms of 64 bits.		

Table 13-36. GCTOTALREADS (continued)

Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total reads in terms of 64 bits	R	0x0000 0000

Table 13-37. Register Call Summary for Register GCTOTALREADS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-38. GCTOTALWRITES

Address Offset	0x0000 0044		
Physical Address	0x5900 0044	**Instance**	BB2D
Description	Total writes in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total writes in terms of 64 bits	R	0x0000 0000

Table 13-39. Register Call Summary for Register GCTOTALWRITES

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-40. GCCHIPSPECS

Address Offset	0x0000 0048		
Physical Address	0x5900 0048	**Instance**	BB2D
Description	Specs for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX_OUTPUT_BUFFER_SIZE				NUM_PIXEL_PIPES				NUM_SHADER_CORES				RESERVED				VERTEX_CACHE_SIZE				THREAD_COUNT				TEMP_REGISTERS				STREAMS			

Bits	Field Name	Description	Type	Reset
31:28	VERTEX_OUTPUT_BUFFER_SIZE		R	0x0
27:25	NUM_PIXEL_PIPES		R	0x0
24:20	NUM_SHADER_CORES		R	0x00
19:17	RESERVED		R	0x0
16:12	VERTEX_CACHE_SIZE		R	0x00
11:8	THREAD_COUNT		R	0x0
7:4	TEMP_REGISTERS		R	0x0
3:0	STREAMS		R	0x0

Table 13-41. Register Call Summary for Register GCCHIPSPECS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-42. GCTOTALWRITEBURSTS

Address Offset	0x0000 004C		
Physical Address	0x5900 004C	**Instance**	BB2D
Description	Total write data count in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total write data count in terms of 64 bits	R	0x0000 0000

Table 13-43. Register Call Summary for Register GCTOTALWRITEBURSTS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-44. GCTOTALWRITEREQS

Address Offset	0x0000 0050		
Physical Address	0x5900 0050	**Instance**	BB2D
Description	Total write request count.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total write request count	R	0x0000 0000

Table 13-45. Register Call Summary for Register GCTOTALWRITEREQS

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-46. GCTOTALWRITELASTS

Address Offset	0x0000 0054		
Physical Address	0x5900 0054	**Instance**	BB2D
Description	Total WLAST count. This is used to match with GCTOTALWRITEREQS		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total WLAST count	R	0x0000 0000

Table 13-47. Register Call Summary for Register GCTOTALWRITELASTS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-48. GCTOTALREADBURSTS

Address Offset	0x0000 0058		
Physical Address	0x5900 0058	**Instance**	BB2D
Description	Total read data count in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total read data count in terms of 64 bits	R	0x0000 0000

Table 13-49. Register Call Summary for Register GCTOTALREADBURSTS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-50. GCTOTALREADREQS

Address Offset	0x0000 005C		
Physical Address	0x5900 005C	**Instance**	BB2D
Description	Total read request count.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total read request count	R	0x0000 0000

Table 13-51. Register Call Summary for Register GCTOTALREADREQS

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-52. GCTOTALREADLASTS

Address Offset	0x0000 0060		
Physical Address	0x5900 0060	**Instance**	BB2D
Description	Total RLAST count. This is used to match with GCTOTALREADREQS		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total RLAST count	R	0x0000 0000

Table 13-53. Register Call Summary for Register GCTOTALREADLASTS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-54. GCGPOUT0

Address Offset	0x0000 0064		
Physical Address	0x5900 0064	**Instance**	BB2D
Description	General purpose output register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															GCHOLD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	RW	0x0000 0000
0	GCHOLD	1 : Low power mode	RW	0

Table 13-55. Register Call Summary for Register GCGPOUT0

BB2D Functional Description

- BB2D Power Management: [0]

BB2D Register Manual

- BB2D Register Summary: [1]

Table 13-56. GCAXICONTROL

Address Offset	0x0000 0070		
Physical Address	0x5900 0070	**Instance**	BB2D
Description	Special handling on AXI Bus		

Table 13-56. GCAXICONTROL (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WR_FULL_BURST_MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WR_FULL_BURST_MODE	0: NO_BURST_RESET_VALUE 1: BURST_RESET_VALUE	RW	0

Table 13-57. Register Call Summary for Register GCAXICONTROL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-58. GCMINORFEATURES1

Address Offset	0x0000 0074		
Physical Address	0x5900 0074	Instance	BB2D
Description	Shows which features are enabled in the subsystem. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC_FLUSH_STALL	BUG_FIXES6	WIDE_LINE	MMU	OK_TO_GATE_AXI_CLOCK	RESOLVE_OFFSET	NEGATIVE_LOG_FIX	CORRECT_OVERFLOW_VG	HALTI0	LINEAR_TEXTURE_SUPPORT	NON_POWER_OF_TWO	TEXTURE_HORIZONTAL_ALIGNMENT_SELECT	NEW_FLOATING_POINT_ARITHMETIC	NEW_2D	BUG_FIXES5	DITHER_AND_FILTER_PLUS_ALPHA_2D	CORRECT_MIN_MAX_DEPTH	EXTENDED_PIXEL_FORMAT	TWO_STENCIL_REFERENCE	PIXEL_DITHER	HALF_FLOAT_PIPE	L2_WINDOWING	BUG_FIXES4	AUTO_RESTART_TS	CORRECT_AUTO_DISABLE	BUG_FIXES3	TEXTURE_STRIDE	BUG_FIXES2	BUG_FIXES1	VG_DOUBLE_BUFFER	V2_COMPRESSION	RSUV_SWIZZLE

Bits	Field Name	Description	Type	Reset
31	FC_FLUSH_STALL		R	1
30	BUG_FIXES6		R	1
29	WIDE_LINE		R	1
28	MMU		R	1
27	OK_TO_GATE_AXI_CLOCK		R	1
26	RESOLVE_OFFSET		R	1
25	NEGATIVE_LOG_FIX		R	1
24	CORRECT_OVERFLOW_VG		R	0
23	HALTI0		R	0
22	LINEAR_TEXTURE_SUPPORT		R	0
21	NON_POWER_OF_TWO		R	0
20	TEXTURE_HORIZONTAL_ALIGNMENT_SELECT		R	1
19	NEW_FLOATING_POINT_ARITHMETIC		R	1
18	NEW_2D		R	1
17	BUG_FIXES5		R	1
16	DITHER_AND_FILTER_PLUS_ALPHA_2D	Dither and filter+alpha available.	R	1
15	CORRECT_MIN_MAX_DEPTH	EEZ and HZ are correct.	R	1
14	EXTENDED_PIXEL_FORMAT		R	0
13	TWO_STENCIL_REFERENCE		R	1
12	PIXEL_DITHER		R	1
11	HALF_FLOAT_PIPE		R	0
10	L2_WINDOWING		R	0
9	BUG_FIXES4		R	1
8	AUTO_RESTART_TS		R	0
7	CORRECT_AUTO_DISABLE		R	1
6	BUG_FIXES3		R	1
5	TEXTURE_STRIDE	Texture has stride and memory addressing.	R	0
4	BUG_FIXES2		R	1
3	BUG_FIXES1		R	1
2	VG_DOUBLE_BUFFER	Double buffering support for VG (second TS-->VG semaphore is present).	R	0
1	V2_COMPRESSION	V2 compression.	R	1
0	RSUV_SWIZZLE	Resolve UV swizzle.	R	1

Table 13-59. Register Call Summary for Register GCMINORFEATURES1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-60. GCTOTALCYCLES

Address Offset	0x0000 0078		
Physical Address	0x5900 0078	**Instance**	BB2D
Description	Total cycles. This register is a free running counter. It can be reset by writing 0 to it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLES																															

Bits	Field Name	Description	Type	Reset
31:0	CYCLES	Total cycles	RW	0x0000 1DE2

Table 13-61. Register Call Summary for Register GCTOTALCYCLES

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-62. GCTOTALIDLECYCLES

Address Offset	0x0000 007C		
Physical Address	0x5900 007C	**Instance**	BB2D
Description	Total cycles where the GPU is idle. It is reset when GCTOTALCYCLES register is written to. It looks at all the blocks but FE when determining the subsystem is idle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLES																															

Bits	Field Name	Description	Type	Reset
31:0	CYCLES	Total cycles where the GPU is idle	RW	0x0000 1E08

Table 13-63. Register Call Summary for Register GCTOTALIDLECYCLES

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-64. GCCHIPSPECS2

Address Offset	0x0000 0080		
Physical Address	0x5900 0080	**Instance**	BB2D
Description	Specs for the subsystem		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUMBER_OF_CONSTANTS																INSTRUCTION_COUNT								BUFFER_SIZE							

Bits	Field Name	Description	Type	Reset
31:16	NUMBER_OF_CONSTANTS		R	0x0000
15:8	INSTRUCTION_COUNT		R	0x00
7:0	BUFFER_SIZE		R	0x00

Table 13-65. Register Call Summary for Register GCCHIPSPECS2

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-66. GCMINORFEATURES2

Address Offset	0x0000 0084		
Physical Address	0x5900 0084	**Instance**	BB2D
Description	Shows which features are enabled in the subsystem 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			NO_INDEX_PATTERN	RESERVED	NOT_USED	MIXED_STREAMS	INTERLEAVER	FLUSH_FIXED_2D	YUV_CONVERSION	MULTI_SOURCE_BLT	YUV_STANDARD	TILE_FILLER	THREAD_WALKER_IN_PS	ONE_PASS_2D_FILTER	FULL_DIRECT_FB	TX_FILTER	DYNAMIC_FREQUENCY_SCALING	TX_YUV_ASSEMBLER	RGB888	HALTI1	S1S8	END_EVENT	PE_SWIZZLE	CORRECT_AUTO_DISABLE_COUNT_WIDTH	COMPOSITION	RECT_PRIMITIVE	LINEAR_PE	SUPER_TILED_TEXTURE	SEAMLESS_CUBE_MAP	LOGIC_OP	LINE_LOOP

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28	NO_INDEX_PATTERN		R	1
27	RESERVED		R	1
26	NOT_USED		R	0
25	MIXED_STREAMS		R	1
24	INTERLEAVER		R	0
23	FLUSH_FIXED_2D		R	1
22	YUV_CONVERSION		R	1
21	MULTI_SOURCE_BLT		R	1
20	YUV_STANDARD		R	1
19	TILE_FILLER		R	1
18	THREAD_WALKER_IN_PS		R	1
17	ONE_PASS_2D_FILTER		R	1
16	FULL_DIRECT_FB		R	1
15	TX_FILTER		R	0
14	DYNAMIC_FREQUENCY_SCALING		R	1
13	TX_YUV_ASSEMBLER		R	0
12	RGB888		R	0
11	HALTI1		R	0
10	S1S8		R	0
9	END_EVENT		R	0
8	PE_SWIZZLE		R	0
7	CORRECT_AUTO_DISABLE_COUNT_WIDTH		R	1
6	COMPOSITION		R	0

Bits	Field Name	Description	Type	Reset
5	RECT_PRIMITIVE		R	0
4	LINEAR_PE		R	0
3	SUPER_TILED_TEXTURE		R	0
2	SEAMLESS_CUBE_MAP		R	0
1	LOGIC_OP		R	0
0	LINE_LOOP		R	0

Table 13-67. Register Call Summary for Register GCMINORFEATURES2

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-68. GCMODULEPOWERCONTROLS

Address Offset	0x0000 0100		
Physical Address	0x5900 0100	**Instance**	BB2D
Description	Control register for module level power controls.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TURN_OFF_COUNTER																RESERVED								TURN_ON_COUNTER				RESERVED	DISABLE_STARVE_MODULE_CLOCK_GATING	DISABLE_STALL_MODULE_CLOCK_GATING	ENABLE_MODULE_CLOCK_GATING

Bits	Field Name	Description	Type	Reset
31:16	TURN_OFF_COUNTER	Counter value for clock gating the module if the module is idle for this amount of clock cycles	RW	0x0014
15:8	RESERVED		R	0x00
7:4	TURN_ON_COUNTER	Number of clock cycles to wait after turning on the clock	RW	0x2
3	RESERVED		R	0
2	DISABLE_STARVE_MODULE_CLOCK_GATING	Disables module level clock gating for starve/idle condition	RW	0
1	DISABLE_STALL_MODULE_CLOCK_GATING	Disables module level clock gating for stall condition	RW	0
0	ENABLE_MODULE_CLOCK_GATING	Enables module level clock gating	RW	0

Table 13-69. Register Call Summary for Register GCMODULEPOWERCONTROLS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-70. GCMODULEPOWERMODULECONTROL

Address Offset	0x0000 0104		
Physical Address	0x5900 0104	**Instance**	BB2D
Description	Module level control registers.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DISABLE_MODULE_CLOCK_GATING_TX	DISABLE_MODULE_CLOCK_GATING_RA	DISABLE_MODULE_CLOCK_GATING_SE	DISABLE_MODULE_CLOCK_GATING_PA	DISABLE_MODULE_CLOCK_GATING_SH	DISABLE_MODULE_CLOCK_GATING_PE	DISABLE_MODULE_CLOCK_GATING_DE	DISABLE_MODULE_CLOCK_GATING_FE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	DISABLE_MODULE_CLOCK_GATING_TX	Disables module level clock gating for starve/idle condition	RW	0
6	DISABLE_MODULE_CLOCK_GATING_RA	Disables module level clock gating for stall condition	RW	0
5	DISABLE_MODULE_CLOCK_GATING_SE	Enables module level clock gating	RW	0
4	DISABLE_MODULE_CLOCK_GATING_PA	Counter value for clock gating the module if the module is idle for this amount of clock cycles	RW	0
3	DISABLE_MODULE_CLOCK_GATING_SH	Number of clock cycles to wait after turning on the clock	RW	0
2	DISABLE_MODULE_CLOCK_GATING_PE	Disables module level clock gating for starve/idle condition	RW	0
1	DISABLE_MODULE_CLOCK_GATING_DE	Disables module level clock gating for stall condition	RW	0
0	DISABLE_MODULE_CLOCK_GATING_FE	Enables module level clock gating	RW	0

Table 13-71. Register Call Summary for Register GCMODULEPOWERMODULECONTROL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-72. GCMODULEPOWERMODULESTATUS

Address Offset	0x0000 0108		
Physical Address	0x5900 0108	**Instance**	BB2D
Description	Module level control status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODULE_CLOCK_GATED_TX	MODULE_CLOCK_GATED_RA	MODULE_CLOCK_GATED_SE	MODULE_CLOCK_GATED_PA	MODULE_CLOCK_GATED_SH	MODULE_CLOCK_GATED_PE	MODULE_CLOCK_GATED_DE	MODULE_CLOCK_GATED_FE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	MODULE_CLOCK_GATED_TX	Module level clock gating is ON for TX	R	0
6	MODULE_CLOCK_GATED_RA	Module level clock gating is ON for RA	R	0
5	MODULE_CLOCK_GATED_SE	Module level clock gating is ON for SE	R	0
4	MODULE_CLOCK_GATED_PA	Module level clock gating is ON for PA	R	0
3	MODULE_CLOCK_GATED_SH	Module level clock gating is ON for SH	R	0
2	MODULE_CLOCK_GATED_PE	Module level clock gating is ON for PE	R	0
1	MODULE_CLOCK_GATED_DE	Module level clock gating is ON for DE	R	0
0	MODULE_CLOCK_GATED_FE	Module level clock gating is ON for FE	R	0

Table 13-73. Register Call Summary for Register GCMODULEPOWERMODULESTATUS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-74. GCREGMMUSTATUS

Address Offset	0x0000 0188		
Physical Address	0x5900 0188	**Instance**	BB2D
Description	Status register that holds which MMU generated an exception		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		EXCEPTION3		RESERVED		EXCEPTION2		RESERVED		EXCEPTION1		RESERVED		EXCEPTION0	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	NOT USED	R	0x0 0000
13:12	EXCEPTION3	MMU 3 caused an exception and the GCREGMMUEXCEPTION3 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
11:10	RESERVED	NOT USED	R	0x0

Bits	Field Name	Description	Type	Reset
9:8	EXCEPTION2	MMU 2 caused an exception and the GCREGMMUEXCEPTION2 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
7:6	RESERVED	NOT USED	R	0x0
5:4	EXCEPTION1	MMU 1 caused an exception and the GCREGMMUEXCEPTION1 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
3:2	RESERVED	NOT USED	R	0x0
1:0	EXCEPTION0	MMU 0 caused an exception and the GCREGMMUEXCEPTION0 holds the offending address: 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0

Table 13-75. Register Call Summary for Register GCREGMMUSTATUS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-76. GCREGMMUCONTROL

Address Offset	0x0000 018C		
Physical Address	0x5900 018C	**Instance**	BB2D
Description	Control register that enables the MMU (one time shot).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	NOT USED	W	0x0000 0000
0	ENABLE	Enable the MMU. For security reasons, once the MMU is enabled it cannot be disabled until reset.	W	0

Table 13-77. Register Call Summary for Register GCREGMMUCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-78. GCREGMMUEXCEPTION0

Address Offset	0x0000 0190		
Physical Address	0x5900 0190	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 13-79. Register Call Summary for Register GCREGMMUEXCEPTION0

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-80. GCREGMMUEXCEPTION1

Address Offset	0x0000 0194		
Physical Address	0x5900 0194	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 13-81. Register Call Summary for Register GCREGMMUEXCEPTION1

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-82. GCREGMMUEXCEPTION2

Address Offset	0x0000 0198		
Physical Address	0x5900 0198	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 13-83. Register Call Summary for Register GCREGMMUEXCEPTION2

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-84. GCREGMMUEXCEPTION3

Address Offset	0x0000 019C		
Physical Address	0x5900 019C	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 13-85. Register Call Summary for Register GCREGMMUEXCEPTION3

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 13-86. AQMEMORYDEBUG

Address Offset	0x0000 0414		
Physical Address	0x5900 0414	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DONT_STALL_WRITES_TO_SAME_ADDRESS	ZCOMP_LIMIT						DISABLE_WRITE_DATA_SPEEDUP	DISABLE_STALL_READS	RESERVED		LIMIT_CONTROL	RESERVED	INTERLEAVE_BUFFER_LOW_LATENCY_MODE	RESERVED	DISABLE_MINI_MMU_CACHE	RESERVED							MAX_OUTSTANDING_READS							

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	DONT_STALL_WRITES_TO_SAME_ADDRESS		RW	0
29:24	ZCOMP_LIMIT		RW	0x3C
23	DISABLE_WRITE_DATA_SPEEDUP		RW	0
22	DISABLE_STALL_READS		RW	0
21:20	RESERVED	Reserved	RW	0

Bits	Field Name	Description	Type	Reset
19	LIMIT_CONTROL	Limit control 0: REQUESTS 1: DATA	RW	0
18	RESERVED	Reserved	R	0
17	INTERLEAVE_BUFFER_LOW_LATENCY_MODE		RW	0
16:15	RESERVED	Reserved	R	0x0
14	DISABLE_MINI_MMU_CACHE		RW	0
13:8	RESERVED	Reserved	R	0x00
7:0	MAX_OUTSTANDING_READS	Limits the total number of outstanding read requests.	RW	0x00

Table 13-87. Register Call Summary for Register AQMEMORYDEBUG

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 13-88. AQREGISTERTIMINGCONTROL

Address Offset	0x0000 042C		
Physical Address	0x5900 042C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LIGHT_SLEEP	DEEP_SLEEP	POWER_DOWN	FAST_WTC		FAST_RTC		FOR_RF2P								FOR_RF1P								

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	RW	0x000
22	LIGHT_SLEEP	Light sleep	RW	0
21	DEEP_SLEEP	Deep sleep	RW	0
20	POWER_DOWN	Powerdown memory	RW	0
19:18	FAST_WTC	WTC for fast RAMs	RW	0x0
17:16	FAST_RTC	RTC for fast RAMs	RW	0x3
15:8	FOR_RF2P		RW	0x00
7:0	FOR_RF1P		RW	0x00

Table 13-89. Register Call Summary for Register AQREGISTERTIMINGCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-90. GCDISPLAYPRIORITY

Address Offset	0x0000 0434		
Physical Address	0x5900 0434	**Instance**	BB2D
Description	Controls the priority of the display controller requests. This works like a PWM. One register gives the period, and the other gives the ON time. When PWM is ON, display requests are accepted if both display and the other request is valid. If it is OFF, the other request will be accepted. If only one request is valid, it takes the bus regardless of the PWM bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HIGH								PERIOD							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	HIGH	'Duty cycle'	RW	0x01
7:0	PERIOD	Period	RW	0x02

Table 13-91. Register Call Summary for Register GCDISPLAYPRIORITY

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-92. GCDBGCYCLECOUNTER

Address Offset	0x0000 0438		
Physical Address	0x5900 0438	**Instance**	BB2D
Description	Increments every cycle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Increments every cycle	RW	0x0000 1C5E

Table 13-93. Register Call Summary for Register GCDBGCYCLECOUNTER

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-94. GCOUTSTANDINGREADS0

Address Offset	0x0000 043C		
Physical Address	0x5900 043C	**Instance**	BB2D
Description	Number of outstanding reads per client in multiples of 8 bytes.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMU								FE								PEZ								PEC							

Bits	Field Name	Description	Type	Reset
31:24	MMU	Number of outstanding MMU reads in multiples of 8 bytes	R	0x00
23:16	FE	Number of outstanding FE reads in multiples of 8 bytes	R	0x00
15:8	PEZ	Number of outstanding PEZ reads in multiples of 8 bytes	R	0x00
7:0	PEC	Number of outstanding PEC reads in multiples of 8 bytes	R	0x00

Table 13-95. Register Call Summary for Register GCOUTSTANDINGREADS0

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-96. GCOUTSTANDINGREADS1

Address Offset	0x0000 0440		
Physical Address	0x5900 0440	**Instance**	BB2D
Description	Number of outstanding reads per client in multiples of 8 bytes.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL								FC								TX								RA							

Bits	Field Name	Description	Type	Reset
31:24	TOTAL	This field keeps the value of total read requests or total requested data (in 64 bits) depending on the value of AQMEMORYDEBUG[19] LIMIT_CONTROL register field.	R	0x00
23:16	FC	Number of outstanding FC reads in multiples of 8 bytes	R	0x00
15:8	TX	Number of outstanding TX reads in multiples of 8 bytes	R	0x00
7:0	RA	Number of outstanding RA reads in multiples of 8 bytes	R	0x00

Table 13-97. Register Call Summary for Register GCOUTSTANDINGREADS1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-98. GCOUTSTANDINGWRITES

Address Offset	0x0000 0444		
Physical Address	0x5900 0444	**Instance**	BB2D
Description	Number of outstanding writes per client.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL								FC								PEZ								PEC							

Bits	Field Name	Description	Type	Reset
31:24	TOTAL	This field keeps the value of total write requests or total requested data (in 64 bits) depending on the value of AQMEMORYDEBUG[19] LIMIT_CONTROL register field.	R	0x00
23:16	FC	Number of outstanding FC writes in multiples of 8 bytes	R	0x00
15:8	PEZ	Number of outstanding PEZ writes in multiples of 8 bytes	R	0x00
7:0	PEC	Number of outstanding PEC writes in multiples of 8 bytes	R	0x00

Table 13-99. Register Call Summary for Register GCOUTSTANDINGWRITES

BB2D Register Manual • BB2D Register Summary: [0]

Table 13-100. GCDEBUGSIGNALSRA

Address Offset	0x0000 0448		
Physical Address	0x5900 0448	**Instance**	BB2D
Description	32 bit debug signal from RA.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[19:16] RA: 0x0: Valid pixel count. 0x1: Total quad count (after EEZ). 0x2: Valid quad count (after EZ and EEZ). 0x3: Total primitive count. 0x4: Various signals from input stage. See GC320 spec for details. 0x5: Various signals from input stage. See GC320 spec for details. 0x6: Various signals from render pipe. See GC320 spec for details. 0x7: Various signals from render cache. See GC320 spec for details. 0x8: Various signals from raster engine. See GC320 spec for details. 0x9: Cache miss count (in the pipeline). 0xA: Cache miss count (in the prefetcher). 0xB: EEZ culled quads. 0xF: Signature = 0x12344321.	R	0x0000 0000

Table 13-101. Register Call Summary for Register GCDEBUGSIGNALSRA

BB2D Register Manual • BB2D Register Summary: [0]

Table 13-102. GCDEBUGSIGNALSTX

Address Offset	0x0000 044C		
Physical Address	0x5900 044C	**Instance**	BB2D
Description	32 bit debug signal from TX.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[27:24] TX : 0x0: Total bilinear texture requests. 0x1: Total trilinear texture requests. 0x2: Total discarded texture requests. 0x3: Total texture requests. 0x4: Various signals from input stage. See GC320 spec for details. 0x5: Memory read count. 0x6: Memory read count in 8B. 0x7: Cache miss count (in the pipeline). 0x8: Total hitting texels (in pre-fetcher). 0x9: Total missing texels (in pre-fetcher). 0xF: Signature = 0x12211221.	R	0x0000 0000

Table 13-103. Register Call Summary for Register GCDEBUGSIGNALSTX

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-104. GCDEBUGSIGNALSFE

Address Offset	0x0000 0450		
Physical Address	0x5900 0450	**Instance**	BB2D
Description	32 bit debug signal from FE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL		R	0x0000 0000

Table 13-105. Register Call Summary for Register GCDEBUGSIGNALSFE

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-106. GCDEBUGSIGNALSPE

Address Offset	0x0000 0454		
Physical Address	0x5900 0454	**Instance**	BB2D
Description	32 bit debug signal from PE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL0[19:16] PE: 0x0: pixel count killed by color pipe 0x1: pixel count killed by depth pipe 0x2: pixel count drawn by color pipe 0x3: pixel count drawn by depth pipe 0x4: debug signals for 3d_io, 2d_filter, 2d_fsm 0x5: debug signals for cache2d_cntrl 0x6: debug signals for cache2d_tag_alloc 0x7: debug signals for cache3d_c_cntrl, cache3d_c_tag_alloc 0x8: debug signals for cache3d_z_cntrl, cache3d_z_tag_alloc 0x9: debug signals for pref_2d, pref_3d 0xA : debug signals for cmd_state 0xB: 2d pixel count drawn by 2d pipe 0xF: Signature = 0xBABEF00D.	R	0x0000 0000

Table 13-107. Register Call Summary for Register GCDEBUGSIGNALSPE

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-108. GCDEBUGSIGNALSDE

Address Offset	0x0000 0458		
Physical Address	0x5900 0458	**Instance**	BB2D
Description	32 bit debug signal from DE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL		R	0x0000 0000

Table 13-109. Register Call Summary for Register GCDEBUGSIGNALSDE

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-110. GCDEBUGSIGNALSSH

Address Offset	0x0000 045C		
Physical Address	0x5900 045C	**Instance**	BB2D
Description	32 bit debug signal from SH.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL0[27:24] SH. Please refer to GC320 spec for bit position information for all the signals 0x0 : interface signals for debug 0x1 : Instruction Sequencing and vertex input state machine 0x2 : vertex input/output buffer full/empty. Context PC. Physical page valid 0x3 : vertex/pixel, output attribute counts. Some interface signals 0x4 : Shader cycle count, for determining the shader clock 0x5 : Current pixel XY value 0x6 : Last pixels XY value 0x7 : Total pixel instructions executed 0x8 : Total pixels shaded 0x9 : Total vertex instructions executed 0xA : Total vertices shaded 0xB : Total vertex branch instructions 0xC : Total vertex texture instructions 0xD : Total pixel branch instructions 0xE : Total pixel texture instructions 0xF : Reserved signature 0xDEADBEEF	R	0x0000 0000

Table 13-111. Register Call Summary for Register GCDEBUGSIGNALSSH

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-112. GCDEBUGSIGNALSPA

Address Offset	0x0000 0460		
Physical Address	0x5900 0460	**Instance**	BB2D
Description	32 bit debug signal from PA.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[3:0] PA: 0x0: Various signals from input stage. See GC320 spec for details. 0x1: Various signals from input stage. See GC320 spec for details. 0x2: Various signals from input stage. See GC320 spec for details. 0x3: total vertex count 0x4: input primitive count 0x5: output primitive count 0x6: depth clipped primitive count 0x7: trivial rejected primitive count 0x8: culled primitive count 0xF: Signature = 0x0000AAAA	R	0x0000 0000

Table 13-113. Register Call Summary for Register GCDEBUGSIGNALSPA

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-114. GCDEBUGSIGNALSSE

Address Offset	0x0000 0464		
Physical Address	0x5900 0464	**Instance**	BB2D
Description	32 bit debug signal from SE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[11:8] SE: 0x0: culled triangles count. 0x1: culled lines count. 0x2: [31:18] goto signals, [17:8] main state machine state, [7:0] output state machine state. See GC320 spec for details. 0x3: [31:22] unused, [21] early_isTriangle, [20] isTriangle, [19] increment_pc_e0, [18:14] jump_to_signals. See GC320 spec for details. [13:12] max_x_p_e2, [11:10] mid_x_p_e2, [9:8] min_x_p_e2, [7:6] max_y_p_e2, [5:4] mid_y_p_e2. See GC320 spec for details. [3:2] min_y_p_e2, [1:0] min_z_p_e2. See GC320 spec for details. 0x4: area_e2. See GC320 spec for details. 0x5: x0_e2. See GC320 spec for details. 0x6: x1_e2. See GC320 spec for details. 0x7: x2_e2. See GC320 spec for details. 0x8: y0_e2. See GC320 spec for details. 0x9: y1_e2. See GC320 spec for details. 0xA: y2_e2. See GC320 spec for details. 0xB: init_y_e2. See GC320 spec for details. 0xC: init_y_e2. See GC320 spec for details. 0xD: y2_e2. See GC320 spec for details. 0xE: y2_e2. See GC320 spec for details. 0xF: Signature = 0x5E5E5E5E.	R	0x0000 0000

Table 13-115. Register Call Summary for Register GCDEBUGSIGNALSSE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-116. GCDEBUGSIGNALSMC

Address Offset	0x0000 0468		
Physical Address	0x5900 0468	**Instance**	BB2D
Description	32 bit debug signal from MC.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL2[3:0] MC: 0x0: Various signals from FC block. See GC320 spec for details. 0x1: Total read req in terms of 8B from pipeline. 0x2: Total read req in terms of 8B sent out from the subsystem. 0x3: Total write req in terms of 8B from pipeline. 0xF: Signature = 0x12345678.	R	0x0000 0000

Table 13-117. Register Call Summary for Register GCDEBUGSIGNALSMC

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-118. GCDEBUGSIGNALSHI

Address Offset	0x0000 046C		
Physical Address	0x5900 046C	**Instance**	BB2D
Description	32 bit debug signal from HI.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL2[11:8] HI: 0x0: Number of cycles AXI read request is stalled. 0x1: Number of cycles AXI write request is stalled. 0x2: Number of cycles AXI write data is stalled. 0xF: Signature = 0xAAAAAAAA	R	0x0000 0000

Table 13-119. Register Call Summary for Register GCDEBUGSIGNALSHI

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-120. GCDEBUGCONTROL0

Address Offset	0x0000 0470		
Physical Address	0x5900 0470	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SH				RESERVED				PE				RESERVED				DE				RESERVED				FE			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	SH	Selects which set of 32 bit data to get from SH. Resets the counters if set to 0xF	RW	0x0
23:20	RESERVED		R	0x0
19:16	PE	Selects which set of 32 bit data to get from PE. Resets the counters if set to 0xF	RW	0x0
15:12	RESERVED		R	0x0

Bits	Field Name	Description	Type	Reset
11:8	DE	Selects which set of 32 bit data to get from DE. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	FE	Selects which set of 32 bit data to get from FE. Resets the counters if set to 0xF	RW	0x0

Table 13-121. Register Call Summary for Register GCDEBUGCONTROL0

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 13-122. GCDEBUGCONTROL1

Address Offset	0x0000 0474		
Physical Address	0x5900 0474	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TX				RESERVED				RA				RESERVED				SE				RESERVED				PA			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	TX	Selects which set of 32 bit data to get from TX. Resets the counters if set to 0xF	RW	0x0
23:20	RESERVED		R	0x0
19:16	RA	Selects which set of 32 bit data to get from RA. Resets the counters if set to 0xF	RW	0x0
15:12	RESERVED		R	0x0
11:8	SE	Selects which set of 32 bit data to get from SE. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	PA	Selects which set of 32 bit data to get from PA. Resets the counters if set to 0xF	RW	0x0

Table 13-123. Register Call Summary for Register GCDEBUGCONTROL1

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2] [3] [4]

Table 13-124. GCDEBUGCONTROL2

Address Offset	0x0000 0478		
Physical Address	0x5900 0478	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				HI				RESERVED				MC			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:8	HI	Selects which set of 32 bit data to get from HI. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	MC	Selects which set of 32 bit data to get from MC. Resets the counters if set to 0xF	RW	0x0

Table 13-125. Register Call Summary for Register GCDEBUGCONTROL2

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 13-126. GCDEBUGCONTROL3

Address Offset	0x0000 047C		
Physical Address	0x5900 047C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PROBE1				RESERVED				PROBE0			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:8	PROBE1	Selects which module's output will be put in the MSB 32 bits of 64 bit debug signal. 0x0: FE 0x1: DE 0x2: PE 0x3: SH 0x4: PA 0x5: SE 0x6: RA 0x7: TX 0x8: MC	RW	0x0
7:4	RESERVED		R	0x0
3:0	PROBE0	Selects which module's output will be put in the LSB 32 bits of 64 bit debug signal. 0x0: FE 0x1: DE 0x2: PE 0x3: SH 0x4: PA 0x5: SE 0x6: RA 0x7: TX 0x8: MC	RW	0x0

Table 13-127. Register Call Summary for Register GCDEBUGCONTROL3

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-128. GCBUSCONTROL

Address Offset	0x0000 0480		
Physical Address	0x5900 0480	**Instance**	BB2D
Description	Shows which features are enabled in the subsystem. 0 : NONE 1 : AVAILABLE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FCC	TX	FC	MMU	RESERVED	FE	RESERVED	PEZ	PEC

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	FCC	Select the return bus for FCC	RW	0
7	TX	Select the return bus for TX	RW	1
6	FC	Select the return bus for FC-Depth	RW	0
5	MMU	Select the return bus for MMU	RW	1
4	RESERVED		R	0
3	FE	Select the return bus for FE	RW	1
2	RESERVED		R	0
1	PEZ	Select the return bus for PEZ	RW	0
0	PEC	Select the return bus for PEC	RW	0

Table 13-129. Register Call Summary for Register GCBUSCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-130. GCREGENDIANNESS0

Address Offset	0x0000 0484		
Physical Address	0x5900 0484	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD_SWAP																															

Bits	Field Name	Description	Type	Reset
31:0	WORD_SWAP	Flip the words of 32 bit data. 0x12345678 becomes 0x56781234	RW	0x0000 0000

Table 13-131. Register Call Summary for Register GCREGENDIANNESS0

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-132. GCREGENDIANNESS1

Address Offset	0x0000 0488		
Physical Address	0x5900 0488	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE_SWAP																															

Bits	Field Name	Description	Type	Reset
31:0	BYTE_SWAP	Flip the bytes of 16 bit data. 0x12345678 becomes 0x34127856	RW	0x0000 0000

Table 13-133. Register Call Summary for Register GCREGENDIANNESS1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-134. GCREGENDIANNESS2

Address Offset	0x0000 048C		
Physical Address	0x5900 048C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT_SWAP																															

Bits	Field Name	Description	Type	Reset
31:0	BIT_SWAP	Flip the bits of 8 bit data. 0x12345678 becomes 0x84C2A6E1	RW	0x0000 0000

Table 13-135. Register Call Summary for Register GCREGENDIANNESS2

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-136. GCREGDRAWPRIMITIVESTARTTIMESTAMP

Address Offset	0x0000 0490		
Physical Address	0x5900 0490	**Instance**	BB2D
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	START_TIME	32-bit timestamp when PE received draw_primitive_start command	R	0x0000 0000

Table 13-137. Register Call Summary for Register GCREGDRAWPRIMITIVESTARTTIMESTAMP

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-138. GCREGDRAWPRIMITIVEENDTIMESTAMP

Address Offset	0x0000 0494		
Physical Address	0x5900 0494	**Instance**	BB2D
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	END_TIME	32-bit timestamp when PE received draw_primitive_end command	R	0x0000 0000

Table 13-139. Register Call Summary for Register GCREGDRAWPRIMITIVEENDTIMESTAMP

BB2D Register Manual

- BB2D Register Summary: [0]

Table 13-140. GCREGCONTROL0

Address Offset	0x0000 0558		
Physical Address	0x5900 0558	**Instance**	BB2D
Description	Composition trigger.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC1								OUTSTANDING_READS_PER_CHANNEL								MISC0												ENABLE_UNALIGNED_WRITE_MERGE	ENABLE_WRITE_MERGE	ENABLE_UNALIGNED_MERGE	ENABLE_READ_MERGE

Bits	Field Name	Description	Type	Reset
31:26	MISC1		RW	0x00
25:16	OUTSTANDING_READS_PER_CHANNEL		RW	0x080
15:4	MISC0		RW	0x000
3	ENABLE_UNALIGNED_WRITE_MERGE		RW	0

Bits	Field Name	Description	Type	Reset
2	ENABLE_WRITE_MERGE		RW	1
1	ENABLE_UNALIGNED_MERGE		RW	0
0	ENABLE_READ_MERGE		RW	1

Table 13-141. Register Call Summary for Register GCREGCONTROL0

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-142. AQCMDBUFFERADDR

Address Offset	0x0000 0654		
Physical Address	0x5900 0654	**Instance**	BB2D
Description	Base address for the command buffer. The address must be 64-bit aligned and it is always physical. To use addresses above 0x8000_0000, program AQMemoryFE with the appropriate offset. Also, this register cannot be read. To check the value of the current fetch address use AQFEDEBUGCURCMDADR.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE	ADDRESS																														

Bits	Field Name	Description	Type	Reset
31	TYPE	0: SYSTEM 1: VIRTUAL_SYSTEM	W	0
30:0	ADDRESS	ADDRESS	W	0x0000 0000

Table 13-143. Register Call Summary for Register AQCMDBUFFERADDR

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-144. AQCMDBUFFERCTRL

Address Offset	0x0000 0658		
Physical Address	0x5900 0658	**Instance**	BB2D
Description	Command buffer control		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										ENDIAN_CONTROL		RESERVED			ENABLE	PREFETCH															

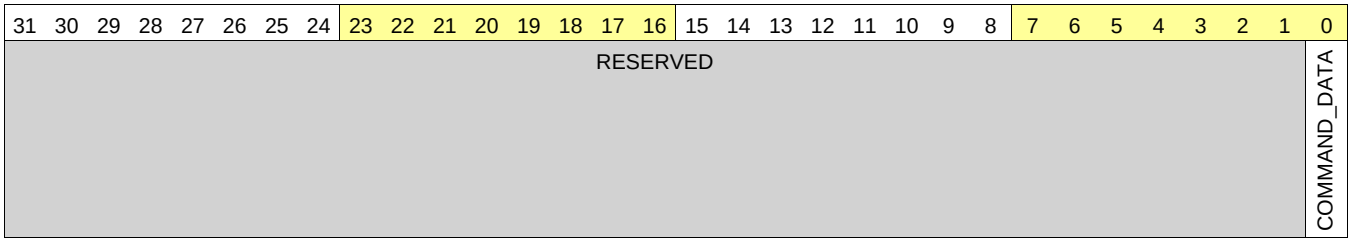
Bits	Field Name	Description	Type	Reset
31:22	RESERVED		W	0x000
21:20	ENDIAN_CONTROL	Endian control 0: NO_SWAP 1: SWAP_WORD 2: SWAP_DWORD	W	0x0
19:17	RESERVED		W	0x0
16	ENABLE	Command buffer 0: DISABLE 1: ENABLE	W	0
15:0	PREFETCH	Number of 64-bit words to fetch from the command buffer.	W	0x0000

Table 13-145. Register Call Summary for Register AQCMDBUFFERCTRL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-146. AQFESTATUS

Address Offset	0x0000 065C		
Physical Address	0x5900 065C	**Instance**	BB2D
Description	FE status		
Type	R		



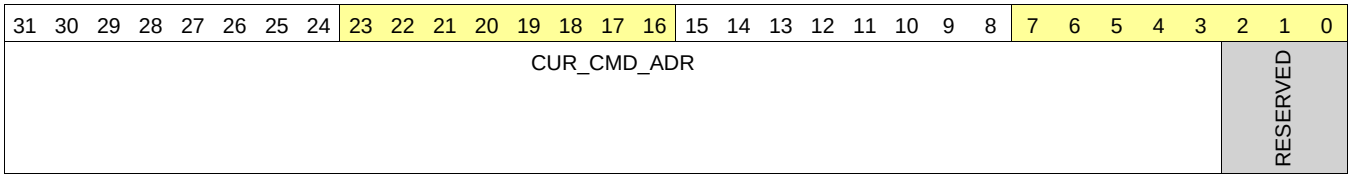
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COMMAND_DATA	Status of the command parser. 0: Idle 1: Busy	R	0

Table 13-147. Register Call Summary for Register AQFESTATUS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 13-148. AQFEDEBUGCURCMDADR

Address Offset	0x0000 0664		
Physical Address	0x5900 0664	**Instance**	BB2D
Description	This is the command decoder address. The address is always physical so the MSB should always be 0.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:3	CUR_CMD_ADR		R	0x0000 0000
2:0	RESERVED		R	0x0

Table 13-149. Register Call Summary for Register AQFEDEBUGCURCMDADR

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]