Xilinx FPGA, TI DSP·MCU
기반의 회로 설계 및 임베디드 전문가 과정

최준호

계획/성과

6주차

목차

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- FPGA 일정
  - FPGA 다음 주 목표
- 지난 주 성과

내 역할

- ~~DSP Linux Device Driver 개발 및 각 장치 구현~~
- FPGA Linux Porting 및 Linux Device Driver 개발 및 장치 개발 및 PL 구현

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Design Description

The design consists of some inputs that are logically operated on before the results are output on the LEDs as shown in **Figure 1**. Other inputs are directly connected to the corresponding output LEDs.

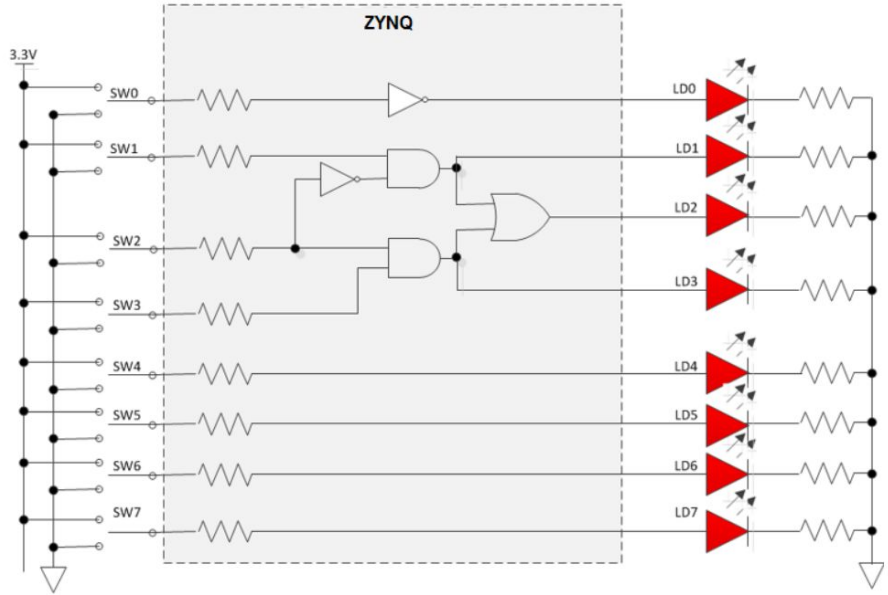

Figure 1. The Completed Design

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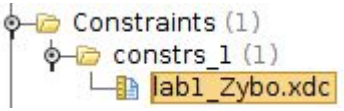
/home/peluza/Documents/Xilinx University Program Workshops/01 FPGA Design Flow using Vivado/2016_2_zynq_sources/lab1/lab1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Module Name: lab1
4  //////////////////////////////////////////////////////////////////////////////////
5
6
7  module lab1(
8      input [7:0] swt,
9       output [7:0] led
10     );
11
12     assign led[0] = ~swt[0];
13     assign led[1] = swt[1] & ~swt[2];
14     assign led[3] = swt[2] & swt[3];
15     assign led[2] = led[1] | led[3];
16
17     assign led[7:4] = swt[7:4];
18
19 endmodule
20
```



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Zybo.xdc

```
1  # ZYBO Pin Assignments
2  ############################
3  # On-board Slide Switches  #
4  ############################
5  set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { swt[0] }];
6  set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { swt[1] }];
7  set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports { swt[2] }];
8  set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCMOS33 } [get_ports { swt[3] }];
9
10 ############################
11 # On-board PMOD  JB        #
12 ############################
13 set_property -dict { PACKAGE_PIN T20   IOSTANDARD LVCMOS33 } [get_ports { swt[4] }];
14 set_property -dict { PACKAGE_PIN U20   IOSTANDARD LVCMOS33 } [get_ports { swt[5] }];
15 set_property -dict { PACKAGE_PIN V20   IOSTANDARD LVCMOS33 } [get_ports { swt[6] }];
16 set_property -dict { PACKAGE_PIN W20   IOSTANDARD LVCMOS33 } [get_ports { swt[7] }];
17
18 ############################
19 # On-board led             #
20 ############################
21 set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { led[0] }];
22 set_property -dict { PACKAGE_PIN M15   IOSTANDARD LVCMOS33 } [get_ports { led[1] }];
23 set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { led[2] }];
24 set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { led[3] }];
25
26 ############################
27 # On-board PMOD  JC        #
28 ############################
29 set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports { led[4] }];
30 set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports { led[5] }];
31 set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports { led[6] }];
32 set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { led[7] }];
```

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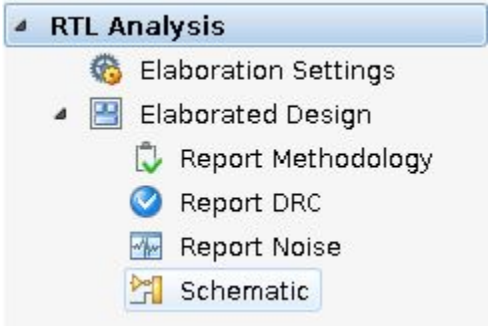
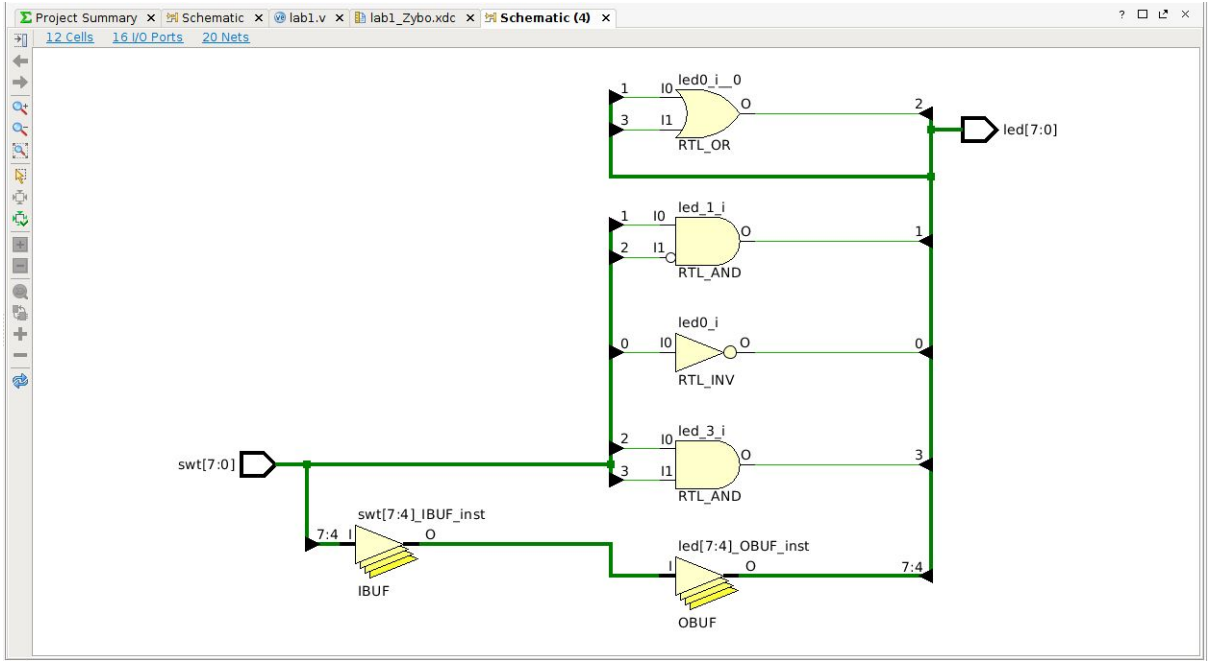

RTL Analysis
Elaboration Settings
Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic


Project Summary
Schematic
lab1.v
lab1_Zybo.xdc
Schematic (4)
12 Cells
16 I/O Ports
20 Nets
led0_i__0
RTL_OR
led[7:0]
led_1_i
RTL_AND
led0_i
RTL_INV
led_3_i
RTL_AND
swt[7:0]
swt[7:4]_IBUF_inst
IBUF
led[7:4]_OBUF_inst
OBUF

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/home/peluza/Documents/Xilinx University Program Workshops/01 FPGA Design Flow using Vivado/2016_2_zynq_sources/lab1/lab1_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////
3  // Module Name: lab1_tb
4  //////////////////////////////////////////////////////////////////
5  module lab1_tb(
6
7      );
8
9      reg [7:0] switches;
10     wire [7:0] leds;
11     reg [7:0] e_led;
12
13     integer i;
14
15     lab1 dut(.led(leds),.swt(switches));
16
17     function [7:0] expected_led;
18        input [7:0] swt;
19     begin
20        expected_led[0] = ~swt[0];
21        expected_led[1] = swt[1] & ~swt[2];
22        expected_led[3] = swt[2] & swt[3];
23        expected_led[2] = expected_led[1] | expected_led[3];
24        expected_led[7:4] = swt[7:4];
25     end
26     endfunction
27
28     initial
29     begin
30         for (i=0; i < 255; i=i+2)
31         begin
32             #50 switches=i;
33             #10 e_led = expected_led(switches);
34             if(leds == e_led)
35                 $display("LED output matched at", $time);
36             else
37                 $display("LED output mis-matched at ",$time,": expected: %b, actual: %b", e_led, leds);
38         end
39     end
40
41 endmodule
42
```

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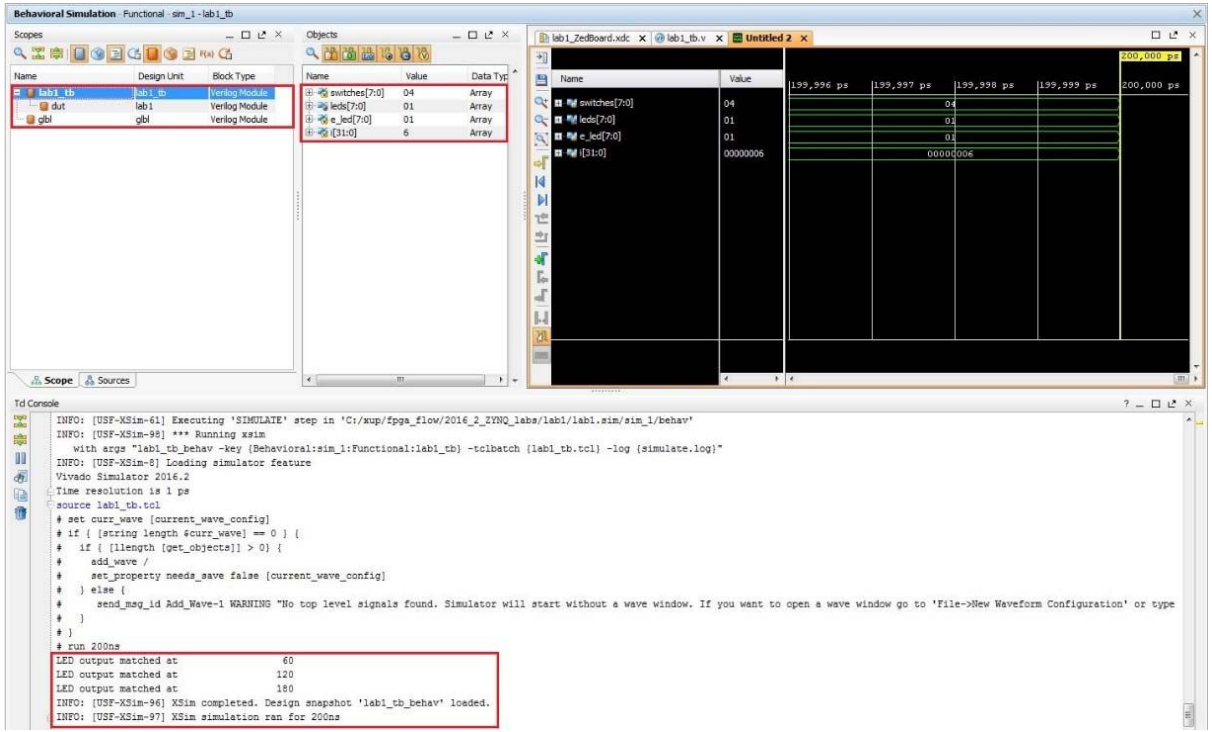
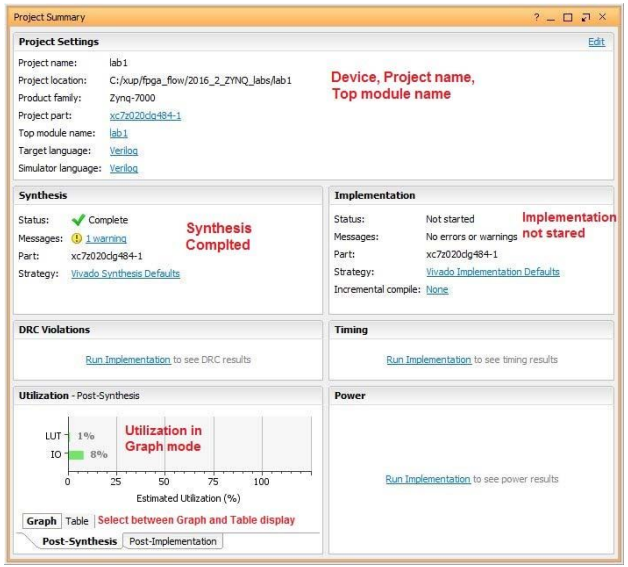

Behavioral Simulation - Functional - sim_1 - lab1_tb
Scopes
Objects
lab1_tb
dut
glbl
Verilog Module
switches[7:0]
leds[7:0]
e_led[7:0]
i[31:0]
Scope
Sources
lab1_ZedBoard.xdc
lab1_tb.v
Untitled 2
200,000 ps
199,996 ps
199,997 ps
199,998 ps
199,999 ps
00000006
Td Console
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'C:/xup/fpga_flow/2016_2_ZYNQ_labs/lab1/lab1.sim/sim_1/behav'
INFO: [USF-XSim-98] *** Running xsim
with args "lab1_tb_behav -key {Behavioral:sim_1:Functional:lab1_tb} -tclbatch {lab1_tb.tcl} -log {simulate.log}"
INFO: [USF-XSim-8] Loading simulator feature
Vivado Simulator 2016.2
Time resolution is 1 ps
source lab1_tb.tcl
set curr_wave [current_wave_config]
if { [string length $curr_wave] == 0 } {
if { [llength [get_objects]] > 0} {
add_wave /
set_property needs_save false [current_wave_config]
} else {
send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Configuration' or type
}
}
run 200ns
LED output matched at 60
LED output matched at 120
LED output matched at 180
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab1_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 200ns


Project Summary
Project Settings
Edit
Project name: lab1
Project location: C:/xup/fpga_flow/2016_2_ZYNQ_labs/lab1
Product family: Zynq-7000
Project part: xc7z020clg484-1
Top module name: lab1
Target language: Verilog
Simulator language: Verilog
Device, Project name, Top module name
Synthesis
Status: Complete
Messages: 1 warning
Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults
Synthesis Complted
Implementation
Status: Not started
Messages: No errors or warnings
Part: xc7z020clg484-1
Strategy: Vivado Implementation Defaults
Incremental compile: None
Implementation not stared
DRC Violations
Run Implementation to see DRC results
Timing
Run Implementation to see timing results
Utilization - Post-Synthesis
LUT 1%
IO 8%
0 25 50 75 100
Estimated Utilization (%)
Utilization in Graph mode
Graph Table Select between Graph and Table display
Post-Synthesis Post-Implementation
Power
Run Implementation to see power results

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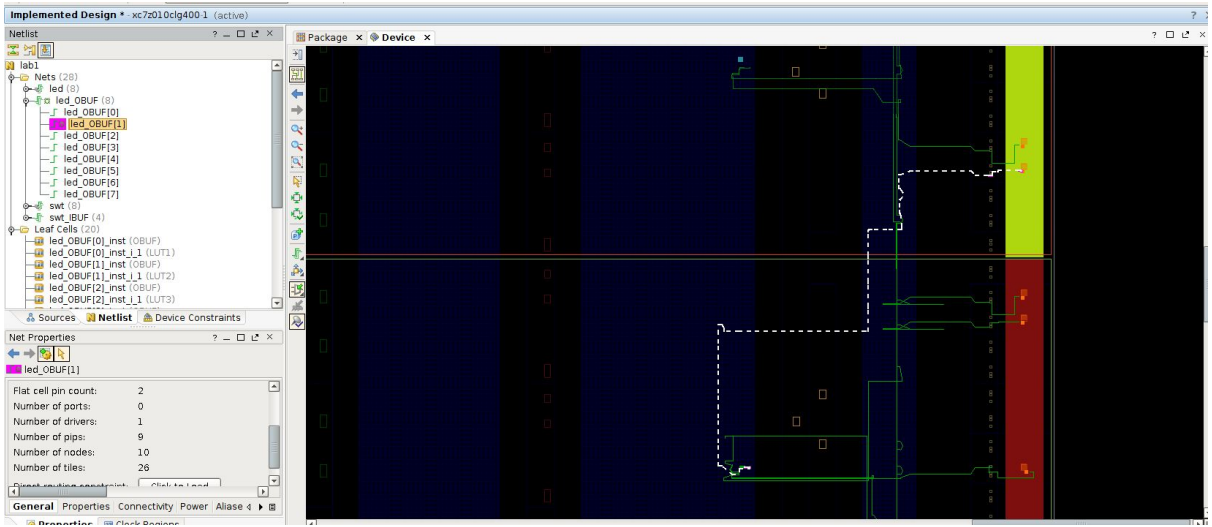
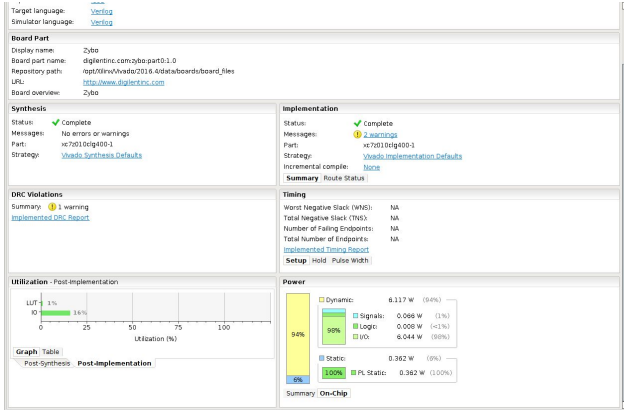

Implemented Design * - xc7z010clg400-1 (active)
Netlist
lab1
Nets (28)
led (8)
led_OBUF (8)
led_OBUF[0]
led_OBUF[1]
led_OBUF[2]
led_OBUF[3]
led_OBUF[4]
led_OBUF[5]
led_OBUF[6]
led_OBUF[7]
swt (8)
swt_IBUF (4)
Leaf Cells (20)
led_OBUF[0]_inst (OBUF)
led_OBUF[0]_inst_i_1 (LUT1)
led_OBUF[1]_inst (OBUF)
led_OBUF[1]_inst_i_1 (LUT2)
led_OBUF[2]_inst (OBUF)
led_OBUF[2]_inst_i_1 (LUT3)
Sources
Netlist
Device Constraints
Net Properties
led_OBUF[1]
Flat cell pin count: 2
Number of ports: 0
Number of drivers: 1
Number of pips: 9
Number of nodes: 10
Number of tiles: 26
General
Properties
Connectivity
Power
Package
Device


Target language: Verilog
Simulator language: Verilog
Board Part
Display name: Zybo
Board part name: digilentinc.com:zybo:part0:1.0
Repository path: /opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL: http://www.digilentinc.com
Board overview: Zybo
Synthesis
Status: Complete
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Synthesis Defaults
Implementation
Status: Complete
Messages: 2 warnings
Part: xc7z010clg400-1
Strategy: Vivado Implementation Defaults
Incremental compile: None
Summary
Route Status
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Setup
Hold
Pulse Width
Utilization - Post-Implementation
Graph
Table
Post-Synthesis
Post-Implementation
Power
Dynamic: 6.117 W (94%)
Signals: 0.066 W (1%)
Logic: 0.008 W (<1%)
I/O: 6.044 W (98%)
Static: 0.362 W (6%)
PL Static: 0.362 W (100%)
Summary
On-Chip

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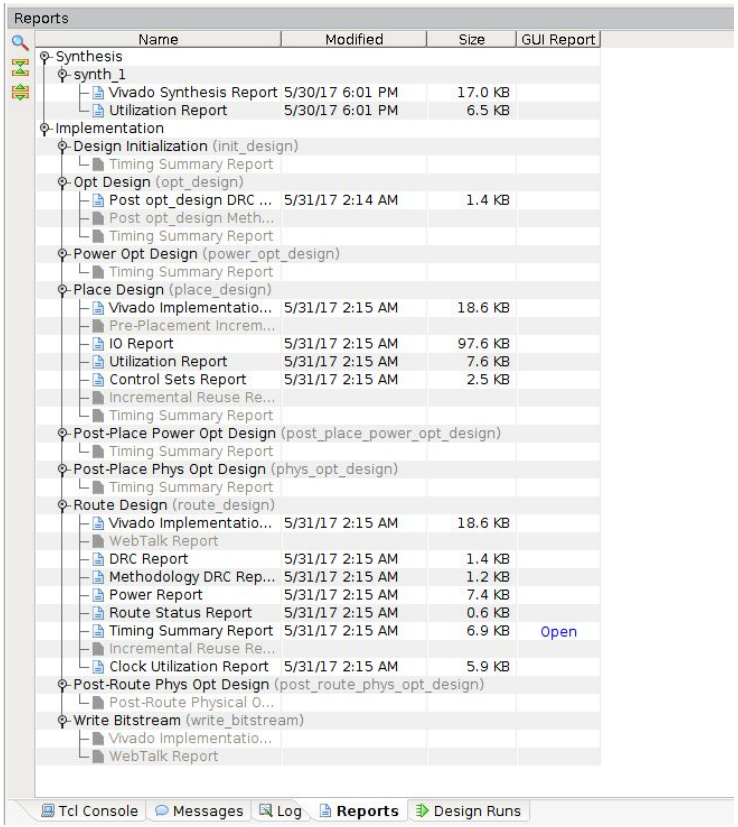
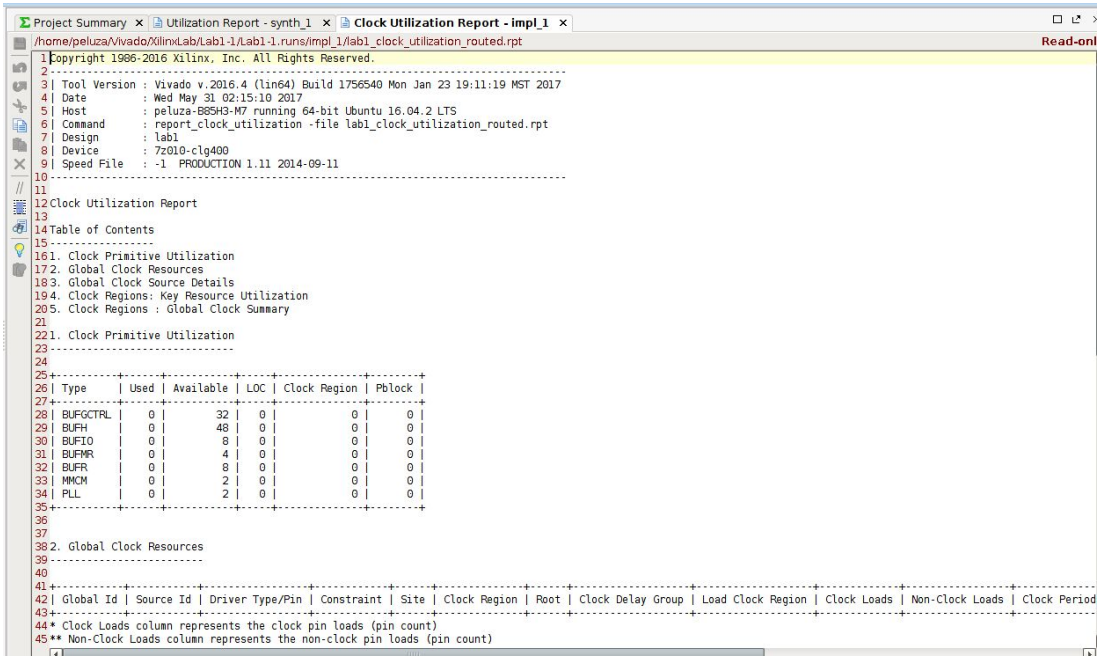

Reports
Name
Modified
Size
GUI Report
Synthesis
synth_1
Vivado Synthesis Report 5/30/17 6:01 PM 17.0 KB
Utilization Report 5/30/17 6:01 PM 6.5 KB
Implementation
Design Initialization (init_design)
Timing Summary Report
Opt Design (opt_design)
Post opt_design DRC ... 5/31/17 2:14 AM 1.4 KB
Post opt_design Meth...
Timing Summary Report
Power Opt Design (power_opt_design)
Timing Summary Report
Place Design (place_design)
Vivado Implementatio... 5/31/17 2:15 AM 18.6 KB
Pre-Placement Increm...
IO Report 5/31/17 2:15 AM 97.6 KB
Utilization Report 5/31/17 2:15 AM 7.6 KB
Control Sets Report 5/31/17 2:15 AM 2.5 KB
Incremental Reuse Re...
Timing Summary Report
Post-Place Power Opt Design (post_place_power_opt_design)
Timing Summary Report
Post-Place Phys Opt Design (phys_opt_design)
Timing Summary Report
Route Design (route_design)
Vivado Implementatio... 5/31/17 2:15 AM 18.6 KB
WebTalk Report
DRC Report 5/31/17 2:15 AM 1.4 KB
Methodology DRC Rep... 5/31/17 2:15 AM 1.2 KB
Power Report 5/31/17 2:15 AM 7.4 KB
Route Status Report 5/31/17 2:15 AM 0.6 KB
Timing Summary Report 5/31/17 2:15 AM 6.9 KB Open
Incremental Reuse Re...
Clock Utilization Report 5/31/17 2:15 AM 5.9 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)
Post-Route Physical O...
Write Bitstream (write_bitstream)
Vivado Implementatio...
WebTalk Report
Tcl Console
Messages
Log
Reports
Design Runs


Project Summary
Utilization Report - synth_1
Clock Utilization Report - impl_1
/home/peluza/Vivado/XilinxLab/Lab1-1/Lab1-1.runs/impl_1/lab1_clock_utilization_routed.rpt
Read-onl
Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.
| Tool Version : Vivado v.2016.4 (lin64) Build 1756540 Mon Jan 23 19:11:19 MST 2017
| Date : Wed May 31 02:15:10 2017
| Host : peluza-B85H3-M7 running 64-bit Ubuntu 16.04.2 LTS
| Command : report_clock_utilization -file lab1_clock_utilization_routed.rpt
| Design : lab1
| Device : 7z010-clg400
| Speed File : -1 PRODUCTION 1.11 2014-09-11
Clock Utilization Report
Table of Contents
1. Clock Primitive Utilization
2. Global Clock Resources
3. Global Clock Source Details
4. Clock Regions: Key Resource Utilization
5. Clock Regions : Global Clock Summary
1. Clock Primitive Utilization
Type	Used	Available	LOC	Clock Region	Pblock
BUFGCTRL	0	32	0	0	0
BUFH	0	48	0	0	0
BUFIO	0	8	0	0	0
BUFMR	0	4	0	0	0
BUFR	0	8	0	0	0
MMCM	0	2	0	0	0
PLL	0	2	0	0	0
2. Global Clock Resources
Global Id	Source Id	Driver Type/Pin	Constraint	Site	Clock Region	Root	Clock Delay Group	Load Clock Region	Clock Loads	Non-Clock Loads	Clock Period
* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

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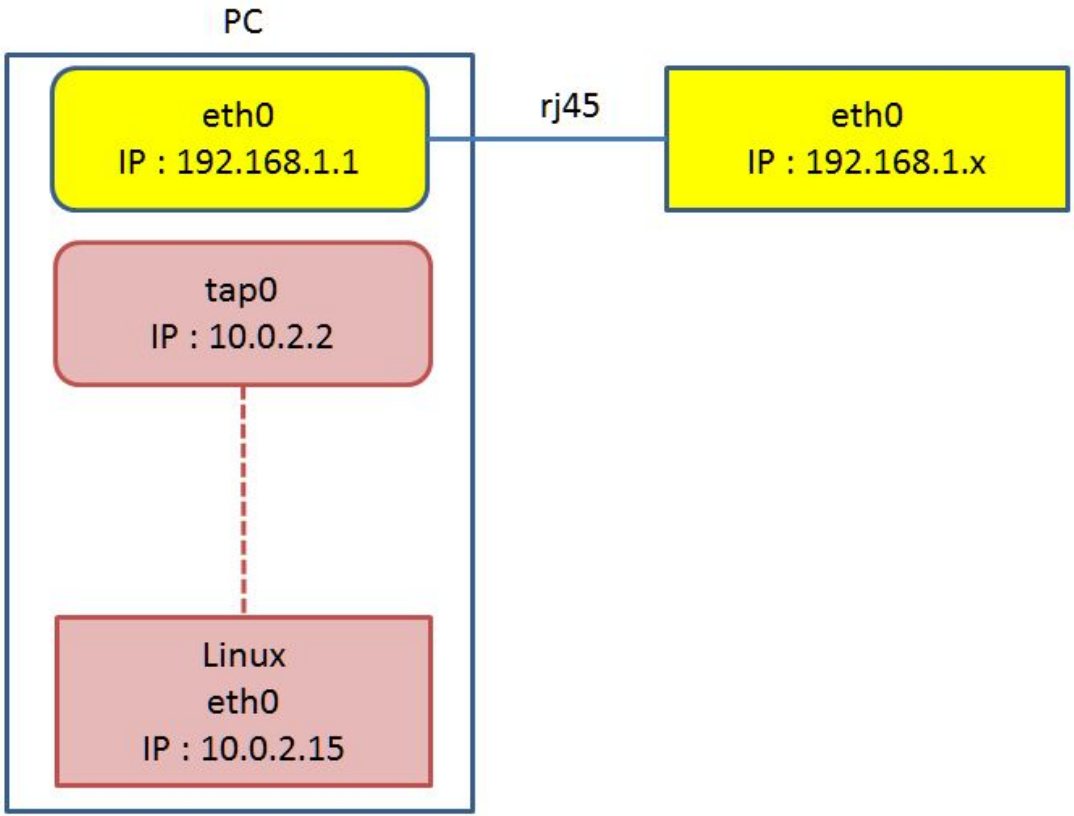
PC
eth0
IP : 192.168.1.1
rj45
eth0
IP : 192.168.1.x
tap0
IP : 10.0.2.2
Linux
eth0
IP : 10.0.2.15

감사합니다