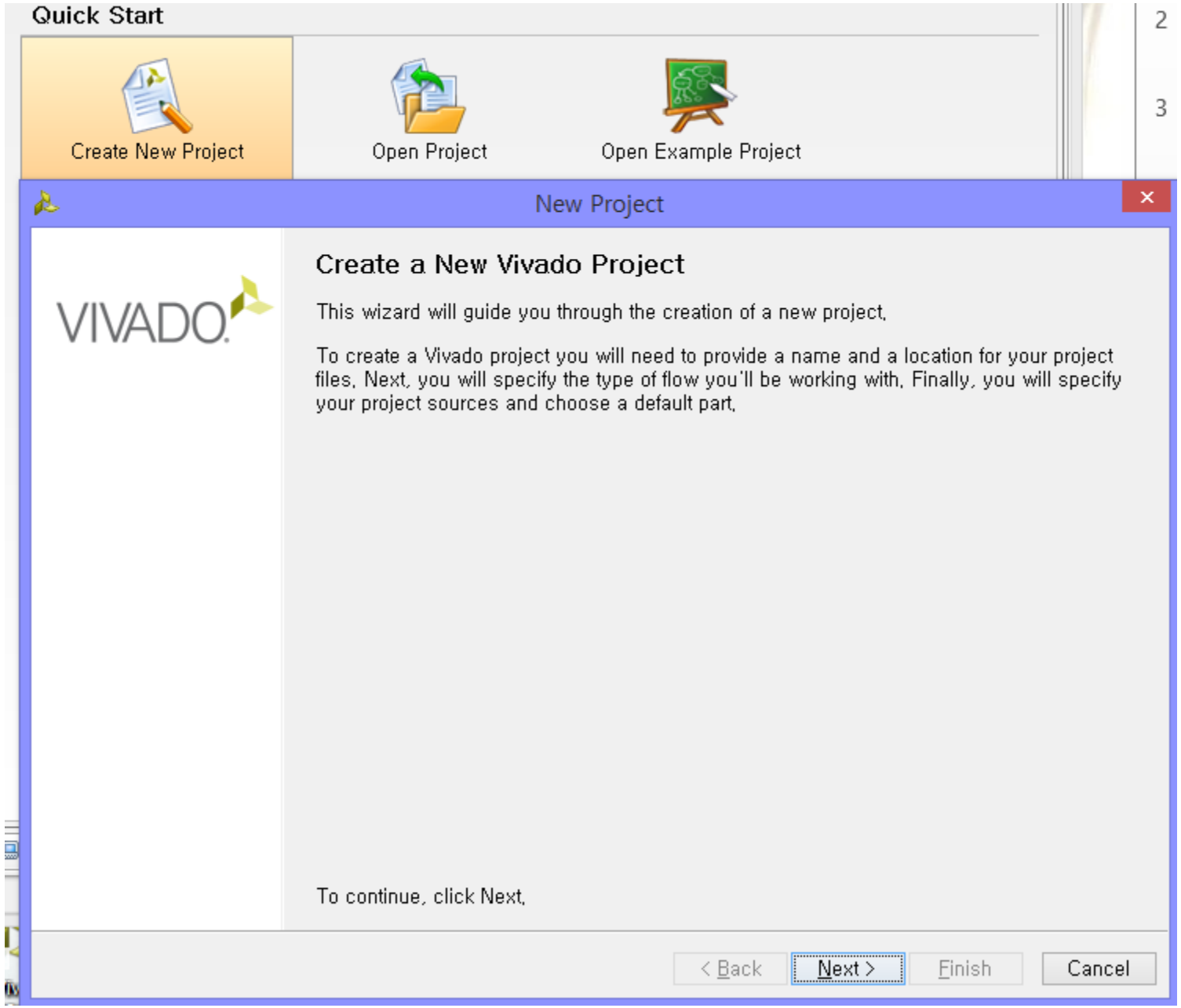
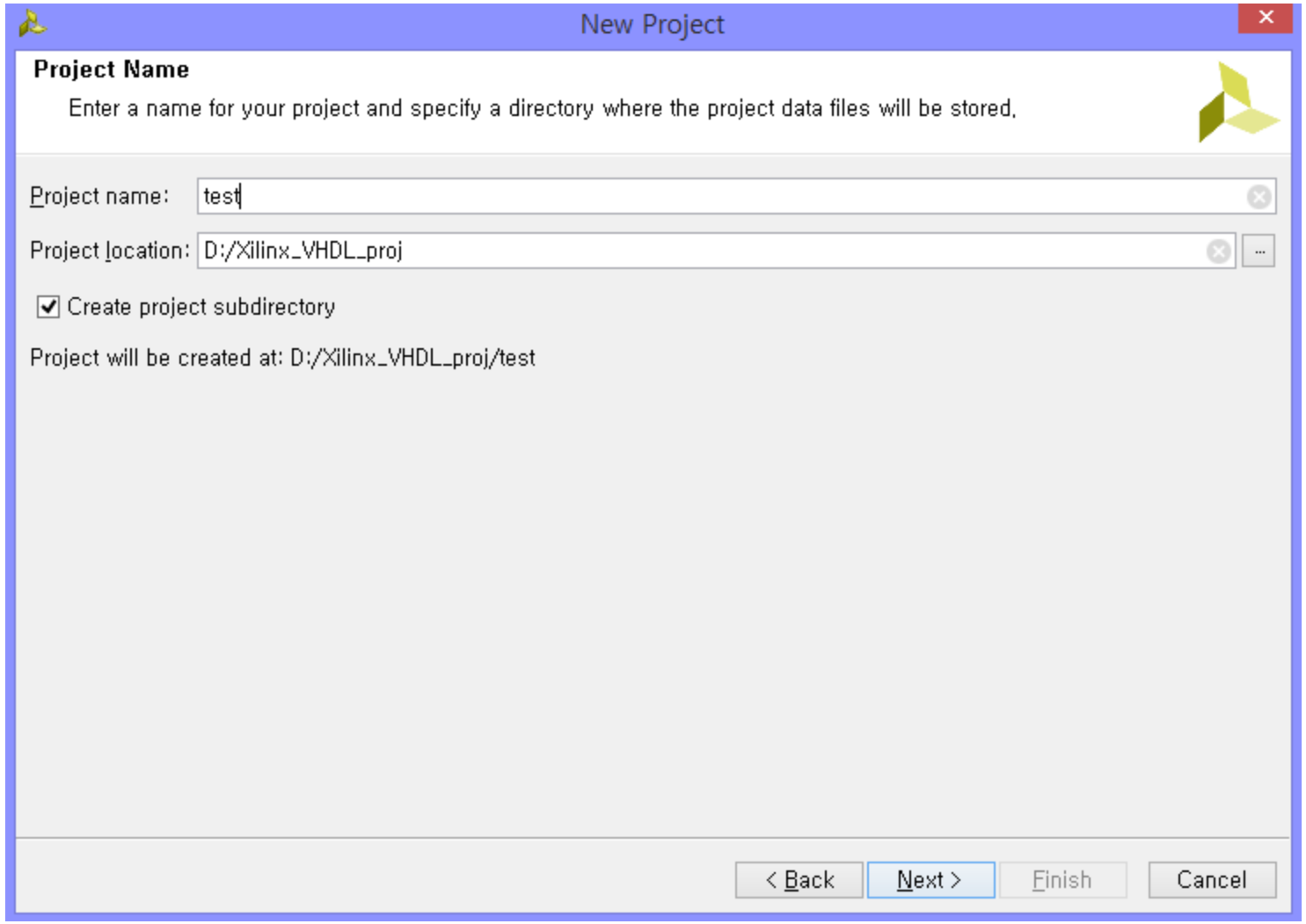
Xilinx Zynq FPGA, TI DSP, MCU 프로그래밍 및 회로 설계 전문가 과정

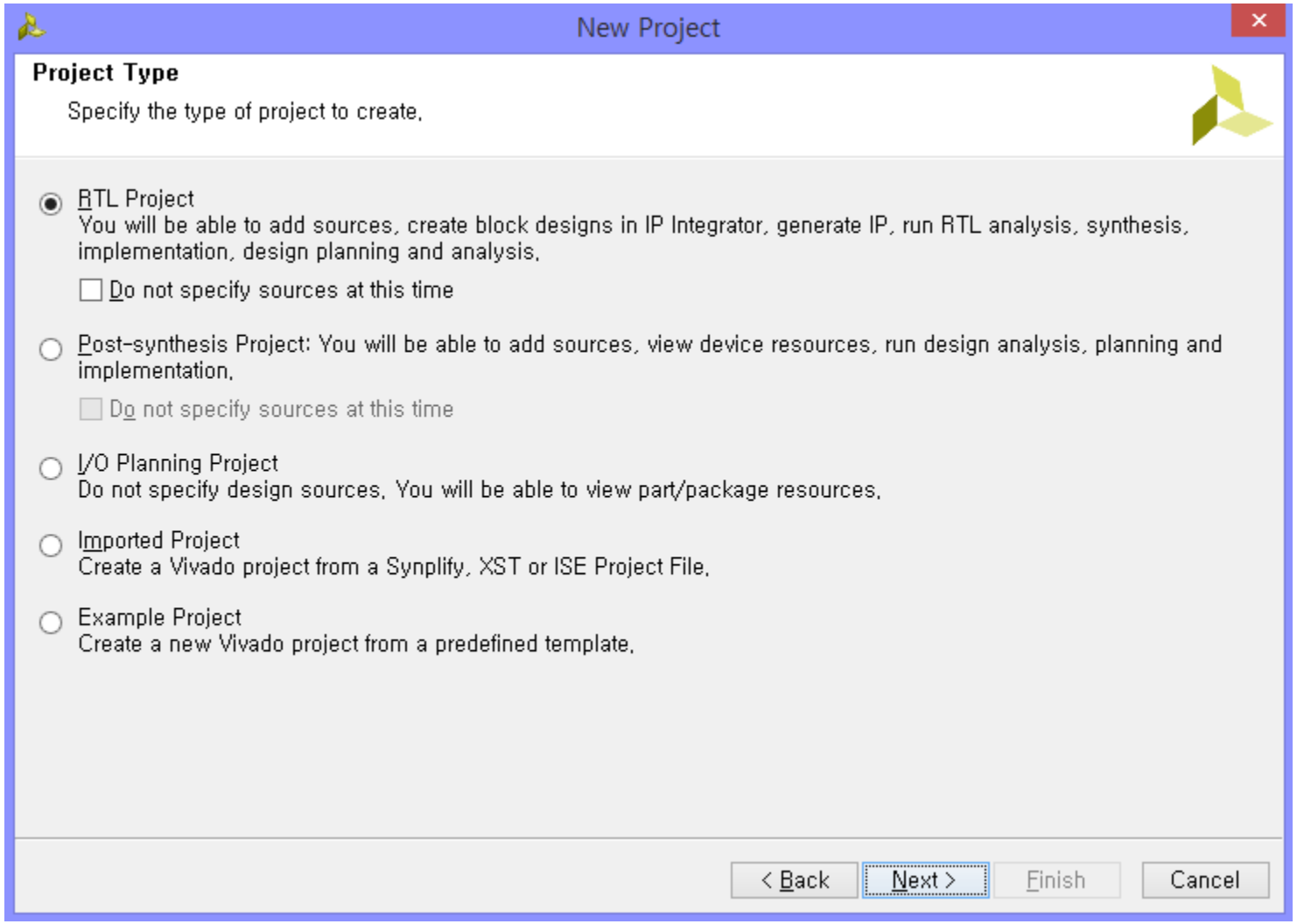
강사 – Innova Lee(이상훈)
gcccompil3r@gmail.com

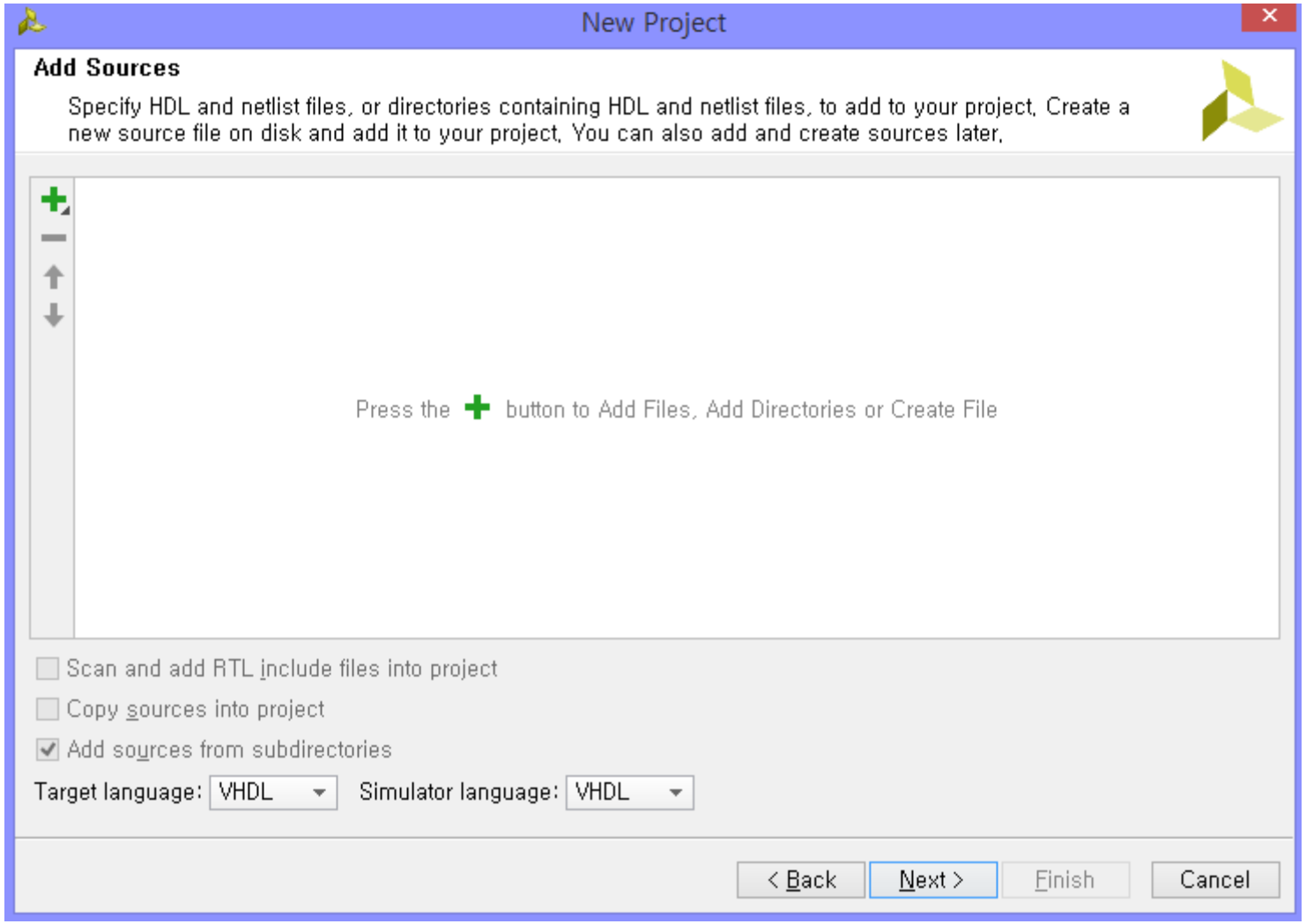
How to make VHDL Project on Vivado ?

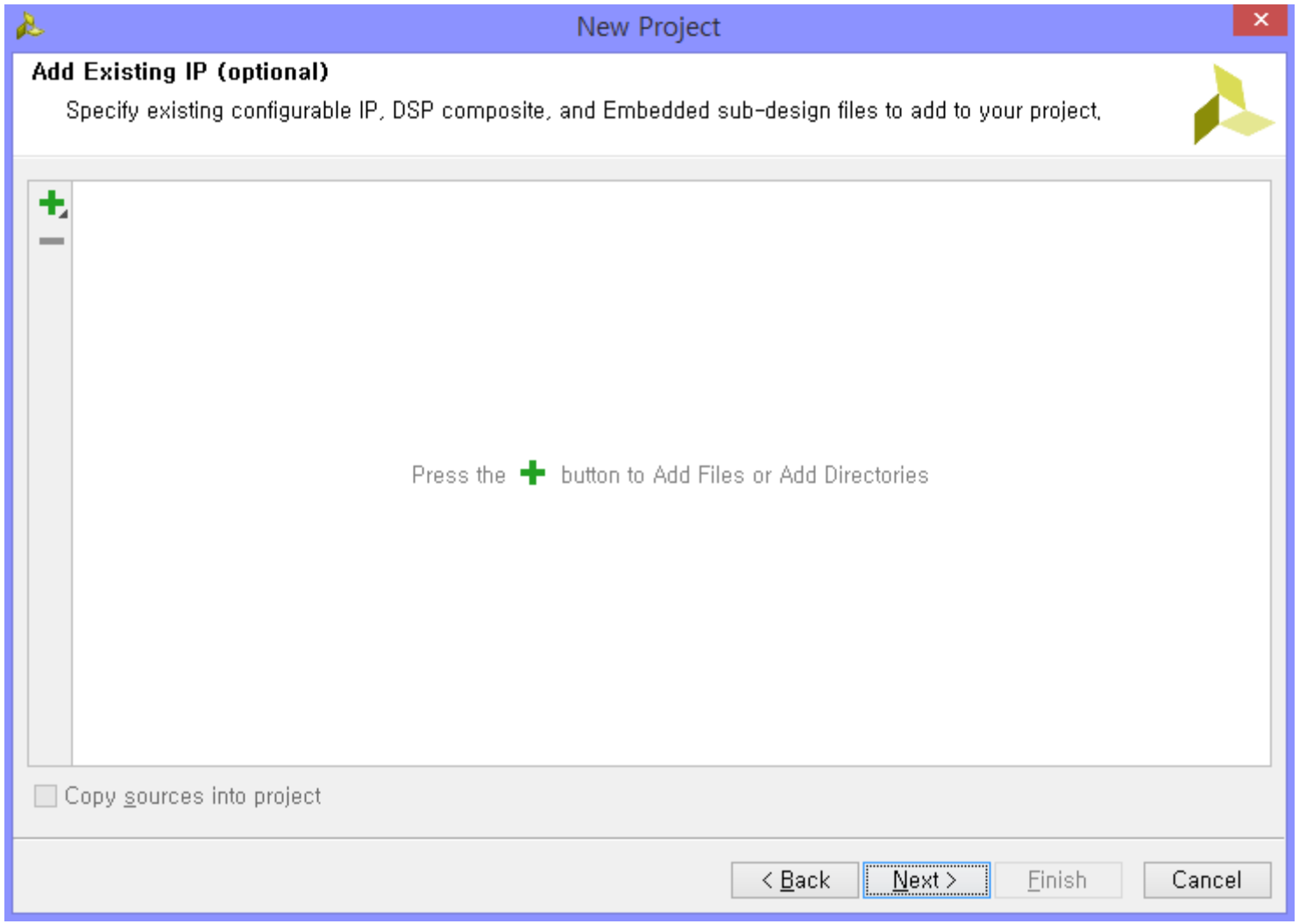

Vivado 2015.2
File
Flow
Tools
Window
Help
Search commands
VIVADO
Productivity. Multiplied.
XILINX
ALL PROGRAMMABLE.
Quick Start
Create New Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Information Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide

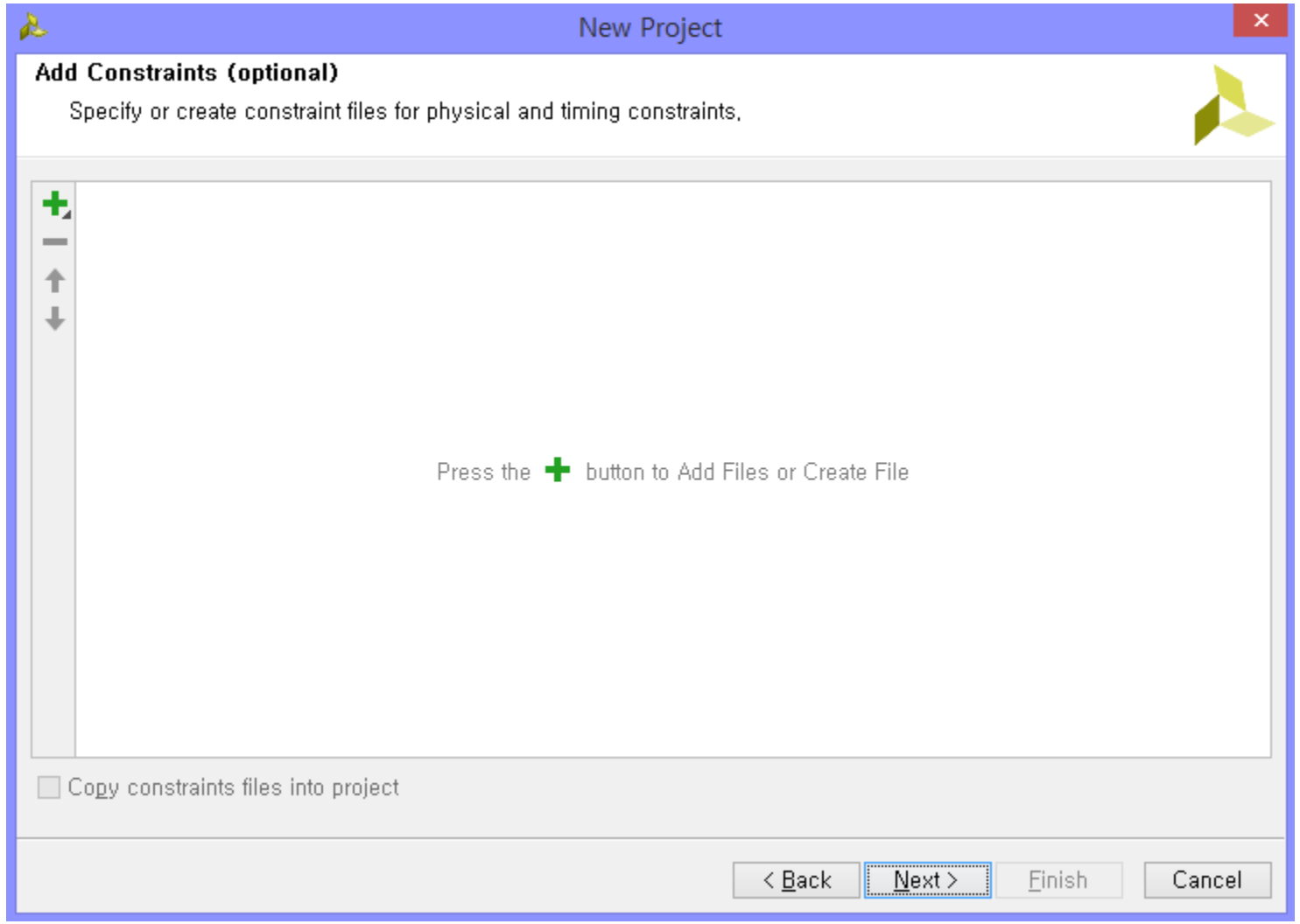

Quick Start
Create New Project
Open Project
Open Example Project
New Project
VIVADO
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
To continue, click Next.
< Back
Next >
Finish
Cancel

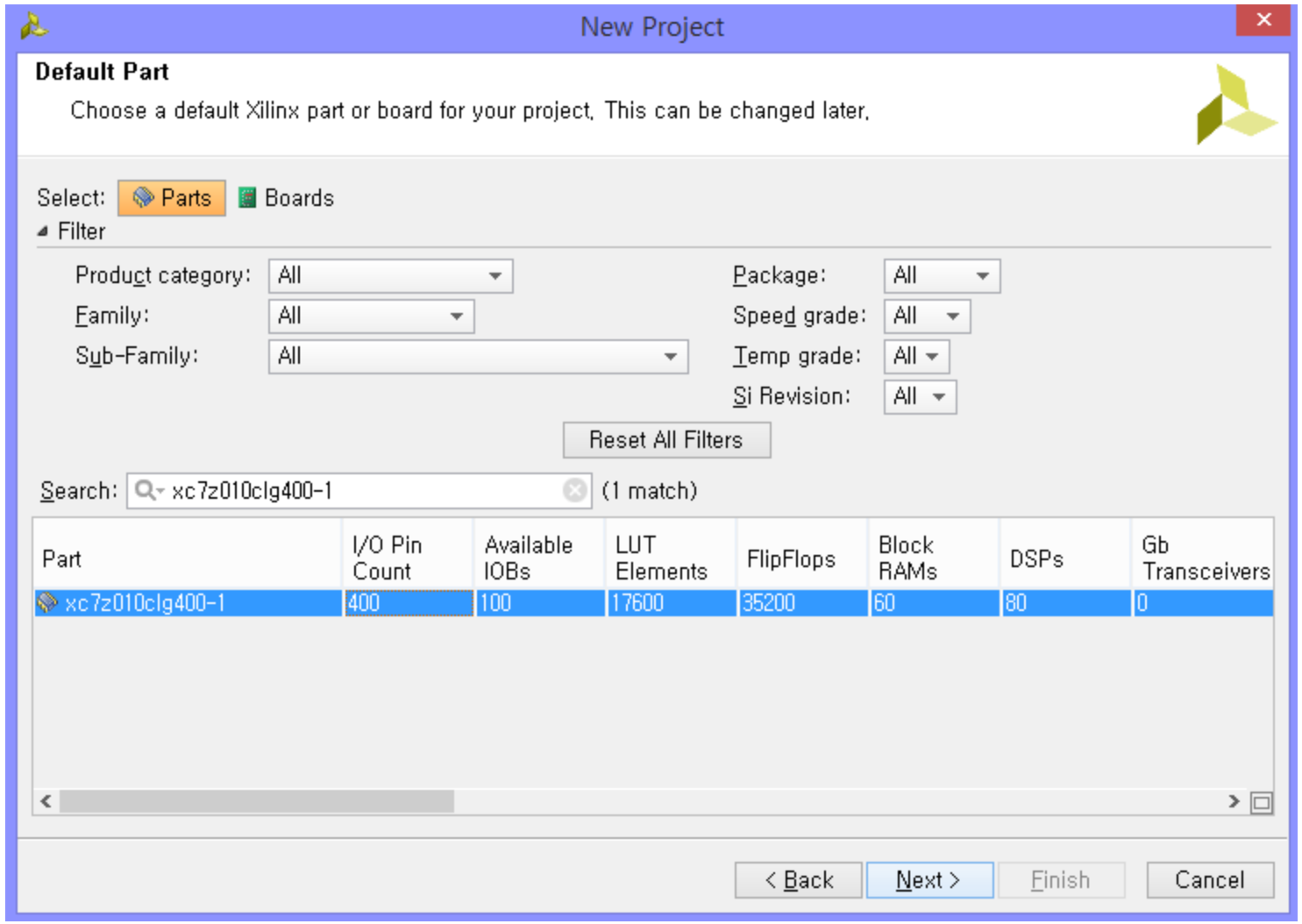

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: test
Project location: D:/Xilinx_VHDL_proj
Create project subdirectory
Project will be created at: D:/Xilinx_VHDL_proj/test
< Back
Next >
Finish
Cancel

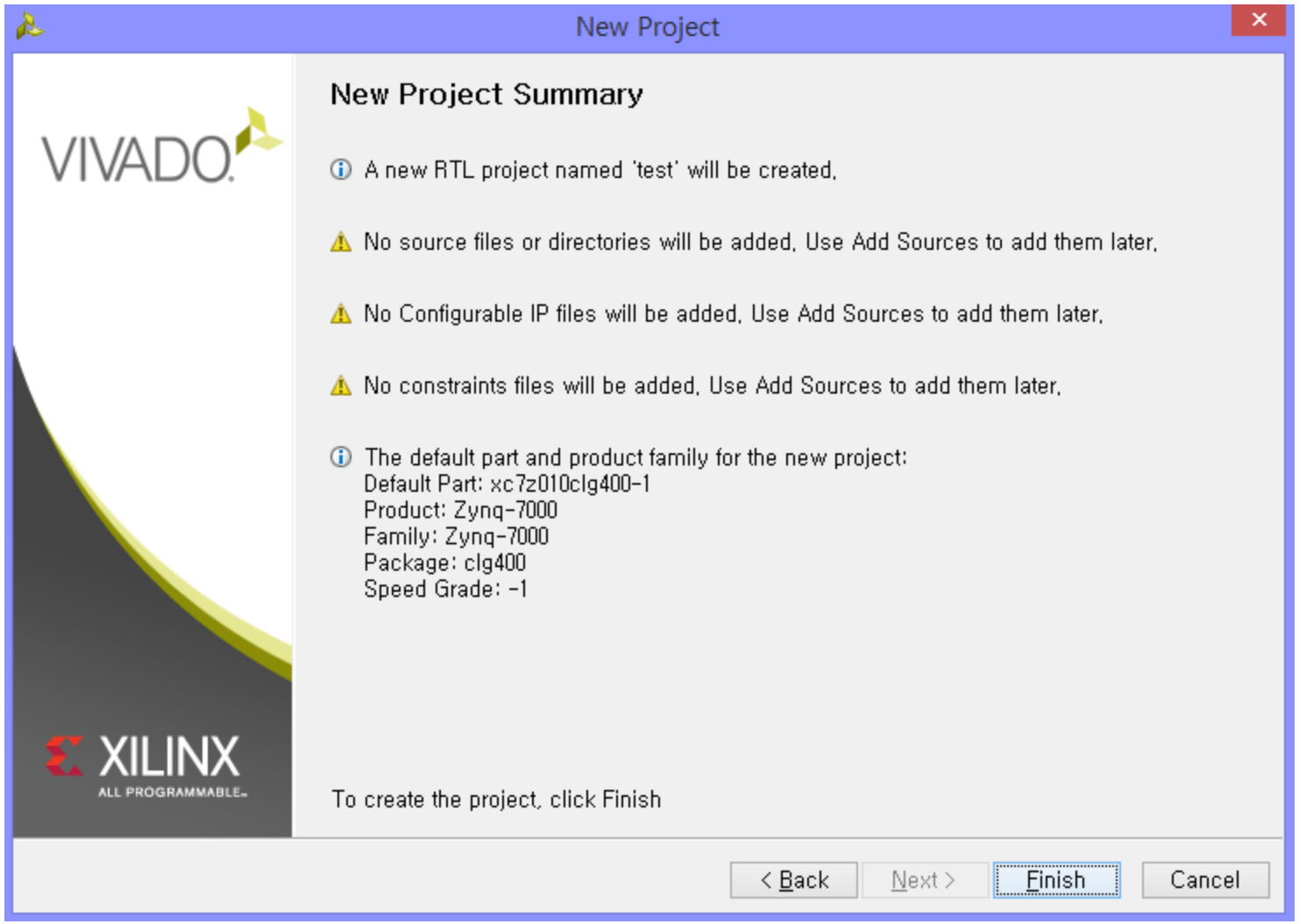

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

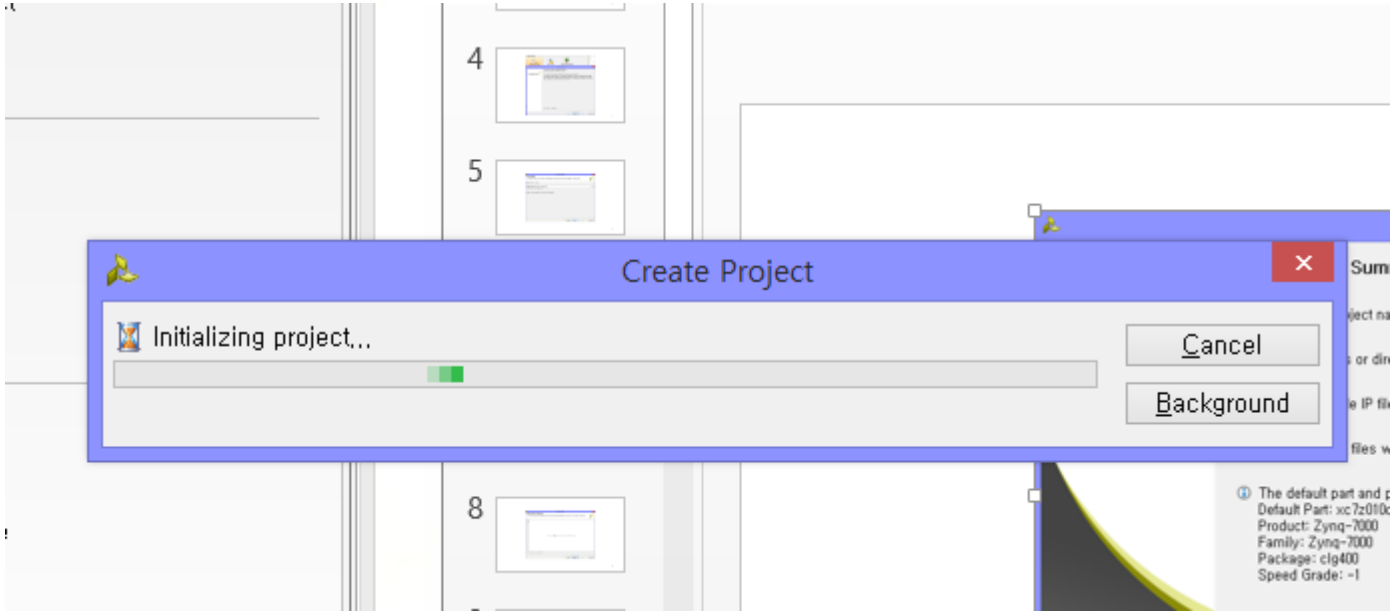

New Project
Add Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Press the + button to Add Files, Add Directories or Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

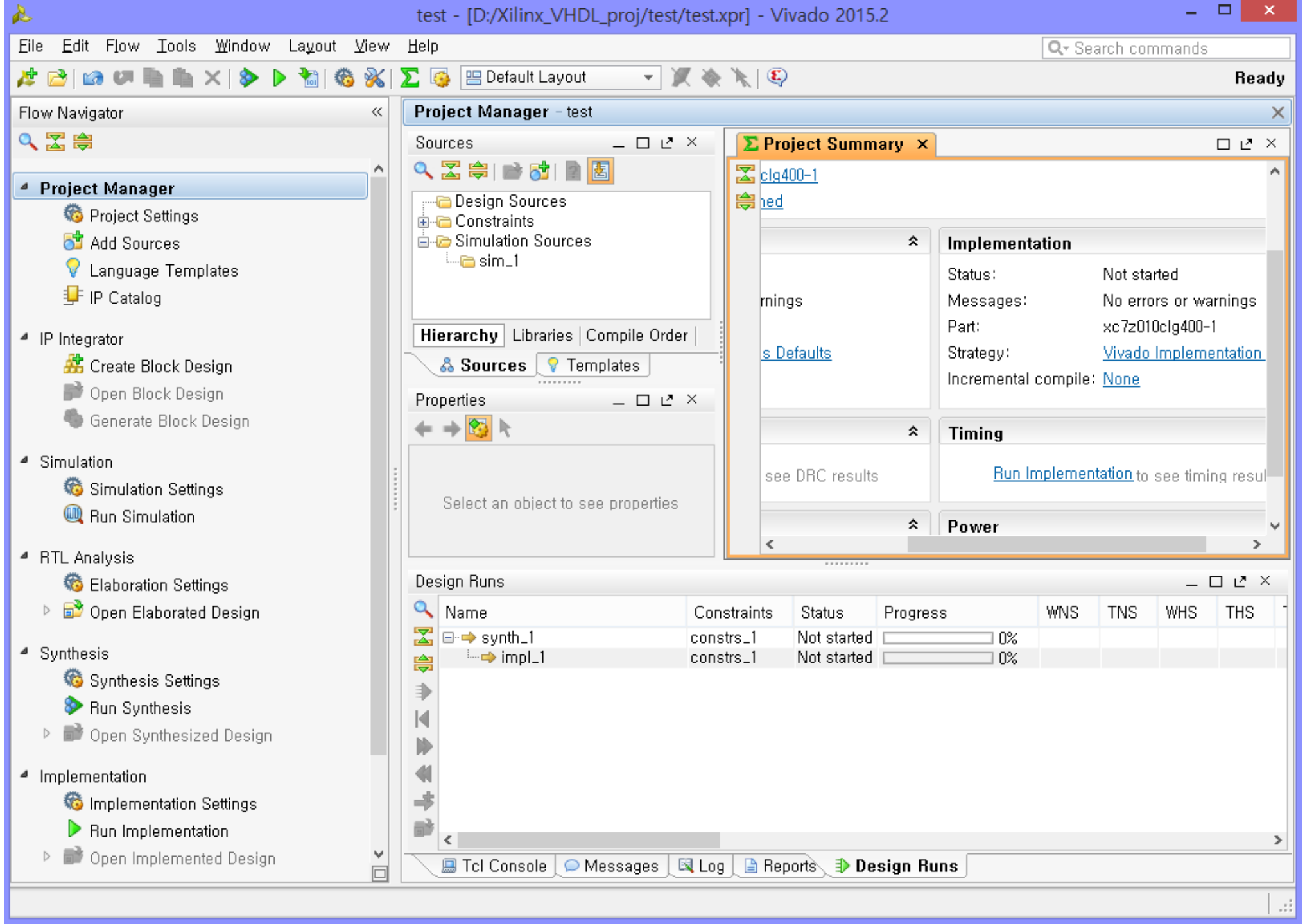

New Project
Add Existing IP (optional)
Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.
Press the button to Add Files or Add Directories
Copy sources into project
< Back
Next >
Finish
Cancel


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Press the button to Add Files or Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Select: Parts Boards
Filter
Product category: All
Family: All
Sub-Family: All
Package: All
Speed grade: All
Temp grade: All
Si Revision: All
Reset All Filters
Search: xc7z010clg400-1 (1 match)
Part
I/O Pin Count
Available IOBs
LUT Elements
FlipFlops
Block RAMs
DSPs
Gb Transceivers
xc7z010clg400-1
400
100
17600
35200
60
80
0
< Back
Next >
Finish
Cancel


New Project
VIVADO
New Project Summary
A new RTL project named 'test' will be created.
No source files or directories will be added. Use Add Sources to add them later.
No Configurable IP files will be added. Use Add Sources to add them later.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1
XILINX
ALL PROGRAMMABLE.
To create the project, click Finish
< Back
Next >
Finish
Cancel


4
5
8
Create Project
Initializing project...
Cancel
Background
Sum
The default part and
Default Part: xc7z010
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1


test - [D:/Xilinx_VHDL_proj/test/test.xpr] - Vivado 2015.2
File Edit Flow Tools Window Layout View Help
Search commands
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Project Manager - test
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Hierarchy Libraries Compile Order
Sources Templates
Properties
Select an object to see properties
Project Summary
clg400-1
Implementation
Status: Not started
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Implementation
Incremental compile: None
Timing
Run Implementation to see timing resul
Power
Design Runs
Name Constraints Status Progress WNS TNS WHS THS
synth_1 constrs_1 Not started 0%
impl_1 constrs_1 Not started 0%
Tcl Console Messages Log Reports Design Runs