Interconnect

This chapter describes the device interconnect.

NOTE: The level 3 (L3) interconnect is an instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

NOTE: The level 4 (L4) interconnects are instantiations of the Sonics3220™ interconnect from Sonics, Inc.

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SLX is an abbreviation for SonicsLX®.

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14.1 Interconnect Overview

14.1.1 Terminology

The following terminology is critical to understanding the interconnect:

- Initiator: Module able to initiate read and write requests to the chip interconnect (typically: processors, DMA, etc.).
- Target: Unlike an initiator, a target module cannot generate read/write requests to the chip interconnect, but it can respond to these requests. However, it may generate interrupts or a DMA request to the system (typically: peripherals, memory controllers).

NOTE: A module can have several separate ports; therefore, a module can be an initiator and a target.

- Agent: Each connection of one module to one interconnect is done using an agent, which is an adaptation (sometimes configurable) between the module and the interconnect. A target module is connected by a target agent (TA), and an initiator module is connected by an initiator agent (IA).
- Interconnect: The decoding, routing, and arbitration logic that enables the connection between multiple initiator modules and multiple target modules connected on it. Quality of service (QoS) is guaranteed.
- Register target (RT): Special TA used to access the interconnect internal configuration registers
- Data-flow signal: Any signal that is part of a clearly identified transfer or data flow (typically: command, address, byte enables, etc.). Signal behaviour is defined by the protocol semantics.
- Sideband signal: Any signal whose behaviour is not associated to a precise transaction or data flow.
- Out-of-band error: Any signal whose behaviour is associated to a device error-reporting scheme, as opposed to in-band errors.

NOTE: Interrupt requests and DMA requests are not routed by the interconnect in the device.

- Firewall: A programmable feature integrated in a target agent or L4 interconnect to prevent unauthorized access to or from a module. A firewall can be configured using three criteria:
  - Initiator requesting access
  - Address space access
  - Type of access
- ConnID: Any transaction in the system interconnect is tagged by an in-band qualifier ConnID, which uniquely identifies the initiator at a given interconnect point. A ConnID is transmitted in band with the request and is used for firewall and error-logging mechanism.
- Firewall comparison mechanism: A comparison made in the firewall between access in-band qualifiers and access permissions that are programmed in the firewall configuration registers. If the comparison is successful, access is allowed; otherwise, access is denied.
- MCmd qualifier: Command bus that indicates the type of transfer requested. Table 14-1 lists the commands encoded. For information specific to L3 Interconnect error logging, see *L3 Firewall Error-Logging Registers*

Table 14-1. MCmd Qualifier Description

MCmd[2:0]	Transaction Type
0 0 0	Idle
0 0 1	Write
0 1 0	Read
0 1 1	ReadEx
1 0 0	Read link
1 0 1	Write nonposted
1 1 0	Write conditional

Table 14-1. MCmd Qualifier Description (continued)

MCmd[2:0]	Transaction Type
1 1 1	Write broadcast

- MReqInfo qualifier: Four MReqInfo qualifiers describe the access during the use of the firewall comparison mechanism, as described in Table 14-2.

Table 14-2. MReqInfo Qualifier Description

Qualifiers	Description
MReqType	0: Data access
	1: Opcode fetch
MReqSupervisor	0: User mode
	1: Supervisor mode
MReqDebug	0: Functional access
	1: Debug access

- Register that configures the combination of the MReqInfo, allowing access permission to the target module (TM) based on the MReqInfo in-band qualifier values.
- SError: Target that indicates an error condition to the initiator.
- SResp qualifier: Response from the target to the initiator concerning the transaction, as described in Table 14-3.

Table 14-3. SResp Qualifier Description

SResp[1:0]	Description
0 0	No response
0 1	Data valid/accept
1 0	Not used
1 1	Error

- MTagID: Interconnect qualifier generated by the L3_MAIN masters which purpose is to identify whether reordering is allowed or not relative to other transactions. Strong ordering is ensured by using same MTagID values between transactions. Reordering is allowed by using different MTagID values between transactions.
  The MTagID values may or may not be changed by the interconnect, but the intended reordering restriction must match what came from the master. In other words, the interconnect allocates dynamically MTagID values in such a way that the intended reordering restrictions from each master are honored.

14.1.2 Architecture Overview

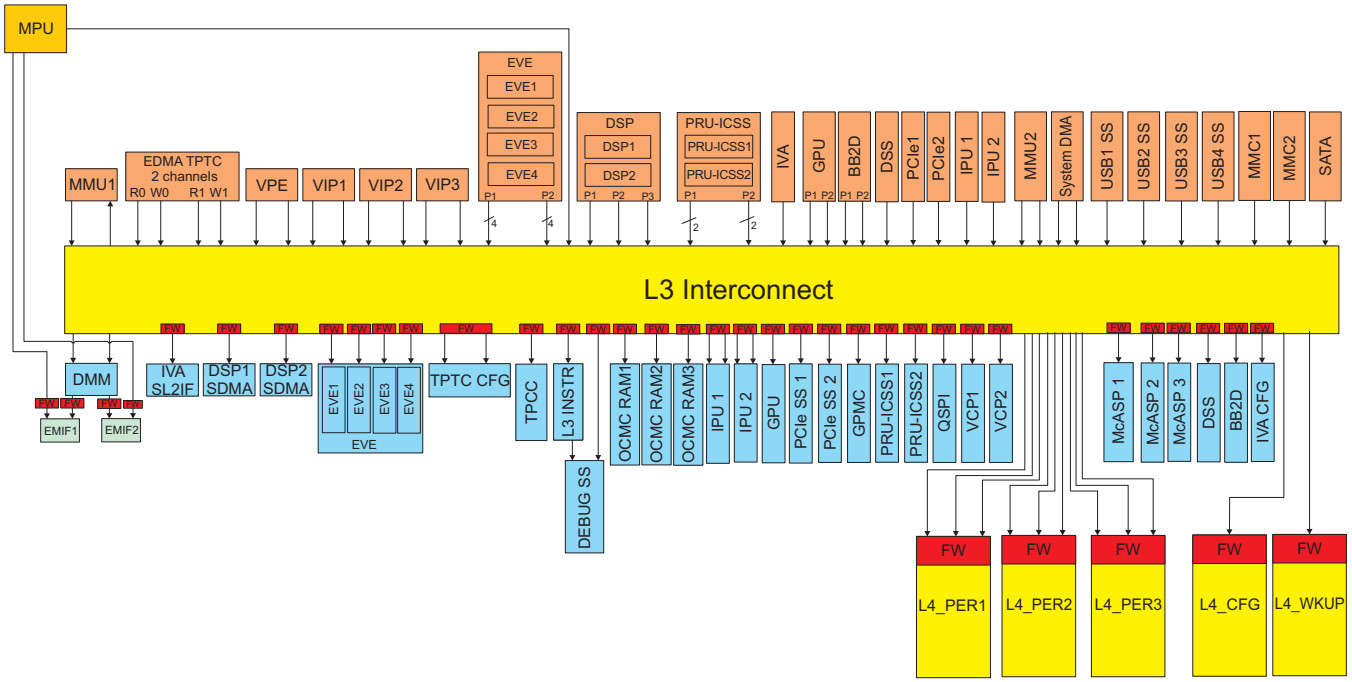
The device memory hierarchy includes four levels:

- L1 is internal to the CPUs. It concerns data exchange with the internal Level1 cache memory subsystem, and it is the closest memory to the microprocessor unit (MPU) core and the IVA core.
- L2 is included in the IPU subsystem and the MPU subsystem.
- The chip-level interconnect consists of one L3 interconnect and five L4 interconnects. It enables communication among the modules and subsystems in the device.

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Figure 14-1 shows an overview of the L3 and L4 interconnect architecture.

Figure 14-1. Interconnect Overview



- L3 handles many types of data transfers, especially exchanges with system-on-chip/external memories. L3 transfers data with a maximum width of 128 bits from the initiator to the target. The L3 interconnect is a little-endian platform
- The L4 is composed of the following:
  - L4_CFG: Includes the majority of the firewall configuration interface for level 3 (L3) system modules and peripheral interconnect;
  - L4_PER: Includes the main peripherals that require system direct memory access (sDMA) access. L4_PER has three instances L4_PER1, L4_PER2 and L4_PER3. Each of these three instances has three ports connecting it to L3_MAIN interconnect:
    - L4_PER1_P1, L4_PER1_P2, L4_PER1_P3
    - L4_PER2_P1, L4_PER2_P2, L4_PER2_P3
    - L4_PER3_P1, L4_PER3_P2, L4_PER3_P3.

    Through the L3_MAIN interconnect, different initiators can access each of these L4_PERx_Pi ports. For information regarding which L4_PERx_Pi port each initiator accesses, see .
  - L4_WKUP: Includes peripherals attached to the WKUP power domain.

Modules are connected to the interconnect through an IA for the initiator module and a TA for target modules. Each module/subsystem connection is statically configured to tune the access, depending on the characteristics of the module.

To unauthorize a module or L4 interconnect access, some TAs include configurable firewalls (FWs). A firewall restricts or filters the accesses allowed to an initiator according to different access criteria. The firewalls can usually be configured by software.

The L3 and L4 interconnect default settings are fully functional; they enable all possible functional data paths and a minimal default protection setting.

14.2 L3_MAIN Interconnect

This section describes the L3_MAIN interconnect and its components. With the exception of register points, each component includes functions for the request and response networks.

14.2.1 L3_MAIN Interconnect Overview

The L3_MAIN interconnect links cores in a flexible topology that couples low power with high performance. Innovative physical structures and advanced protocols ensure bandwidth and latency to individual IP cores, providing dedicated connections between IP cores and logical connections over a shared interconnect.

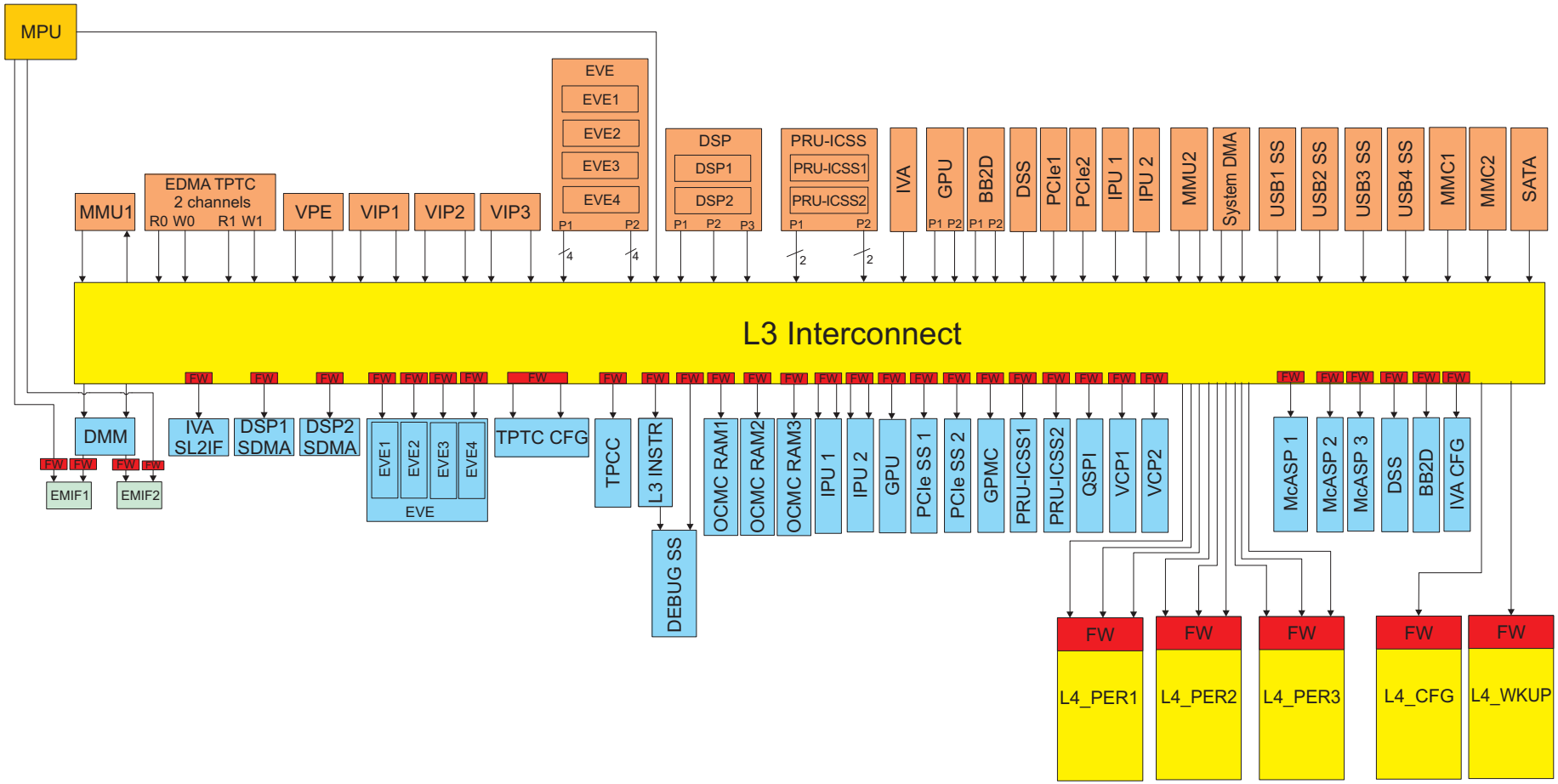
The main features of the L3_MAIN interconnects are:

- NIUs: Master NIUs for the IAs and slave NIUs for the TAs
- A partially depleted cross-bar exchange network
- A special internal slave NIU for accessing L3_MAIN interconnect configuration registers
- QoS management for real-time hardware operators, while maintaining optimal memory latency for CPU access to memory resources
- True little-endian platform
- Transaction errors tracking and logging registers
- All signaling support for chip-level power-management infrastructure
- One interrupt line signaling transaction error
- One interrupt line for reporting satistical events on the L3_MAIN interconnect

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Figure 14-2 shows an overview of the L3 interconnect and the peripherals attached to it.

Figure 14-2. L3_MAIN Interconnect Overview



14.2.2 L3_MAIN Interconnect Integration

Table 14-4 through Table 14-6 summarize the integration of the module in the device.

Table 14-4. L3_MAIN Integration Attributes

Module Instance	Attributes
	Power Domain
L3_MAIN	PD_COREAON

Table 14-5. L3_MAIN Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3_MAIN	L3_CLK1	L3MAIN1_L3_GICLK	PRCM	Functional and interface clock
	L3_CLK2	L3INSTR_L3_GICLK	PRCM	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3_MAIN_MAIN	L3_CORE_RET_RST	CORE_PWRON_RET_RST	PRCM	Reset of L3_MAIN interconnect registers
	L3_CORE_RST	CORE_RST	PRCM	Reset of L3_MAIN interconnect

Table 14-6. L3_MAIN Hardware Requests

Interrupts Requests				
Module Instance	**Source Signal Name**	**Destination IRQ_CROSSBAR Input**	**Default Mapping**	**Description**
L3_MAIN	L3_MAIN_IRQ_DBG_ERR	IRQ_CROSSBAR_4	MPU_IRQ_9	Interrupt indicating debug error occurrence.
			DSP1_IRQ_35	
			DSP2_IRQ_35	
	L3_MAIN_IRQ_APP_ERR	IRQ_CROSSBAR_5	MPU_IRQ_10[1]	Interrupt indicating application error occurrence.
			DSP1_IRQ_36	
			DSP2_IRQ_36	
			IPU1_IRQ_46	
			IPU2_IRQ_46	
			EVE1_IRQ_4	
			EVE2_IRQ_4	
			EVE3_IRQ_4	
			EVE4_IRQ_4	
	L3_MAIN_IRQ_STAT_ALARM	IRQ_CROSSBAR_11	MPU_IRQ_16	Statistic collector alarm interrupt.
			DSP1_IRQ_42	
			DSP2_IRQ_42	

(1) The L3_MAIN_IRQ_APP_ERR interrupt is directly mapped to the MPU_IRQ_10 line bypassing IRQ_CROSSBAR_5. In all other cases IRQ_CROSSBAR_5 is used to map L3_MAIN_IRQ_APP_ERR to the corresponding INTC.

NOTE: EVE1, EVE2, EVE3 and EVE4 are not supported in this family of devices.

NOTE: The "**Default Mapping**" column in Table 14-6 *L3_MAIN Hardware Requests* shows the default mapping of module IRQ source signals. These IRQ source signals can also be mapped to other lines of each device Interrupt controller through the IRQ_CROSSBAR module.
For more information about the IRQ_CROSSBAR module, see Section 18.4.6.4, *IRQ_CROSSBAR Module Functional Description*, in Chapter 18, *Control Module*.
For more information about the device interrupt controllers, see Chapter 17, *Interrupt Controllers*.

14.2.3 L3_MAIN Interconnect Functional Description

14.2.3.1 Module Use in L3_MAIN Interconnect

The L3_MAIN interconnect network components have ConnID values for each master NIU or slave NIU. The ID uniquely identifies the master NIU or the slave NIU for an interconnect transfer. The interconnect uses ConnIDs for a number of purposes, including the following:

- Slave NIUs for error logging
- Power disconnect slave NIU for error logging
- Eight FLAGMUXes to mask interrupts
- STATCOLL for configuring and monitoring: The STATCOLL components compute the traffic statistics within a user-defined window and periodically report to the user through the debug interface.
- Bandwidth regulator for configuration

14.2.3.2 Module Distribution

Master NIUs and slave NIUs provide the interface to connect the different modules to their associated interconnect.

Table 14-7 and Table 14-8 list all the modules and subsystems with their associated agents. The agents are listed for each L3_MAIN interconnect domain.

14.2.3.2.1 L3_MAIN Interconnect Agents

Any initiator or target core is connected to the L3_MAIN interconnect through an NIU. NIUs act as entry points to the L3_MAIN interconnect, and also include various programming registers. Table 14-7 lists the supported master NIU ports.

Table 14-7. Master NIUs

Master NIU	Description
MPU_INIT	MPU initiator port. One 64b OCP initiator port, and two 128b ports connected directly to the EMIF, bypassing L3
DSP1_INIT	DSP Initiator port. One 128b MDMA interconnect initiator port (used also for cache requests) One EDMA initiator port per instance
DSP2_INIT	DSP Initiator port. One 128b MDMA interconnect initiator port (used also for cache requests) One EDMA initiator port per instance
EVE1_INIT NOTE: EVE1 is not supported in this family of devices.	Embedded Vision Engine 1 (EVE1) initiator port. Two 128b interconnect initiator ports (P1/P2)
EVE2_INIT NOTE: EVE2 is not supported in this family of devices.	Embedded Vision Engine 2 (EVE2) initiator port. Two 128b interconnect initiator ports (P1/P2)
EVE3_INIT NOTE: EVE3 is not supported in this family of devices.	EVE3 initiator port. Two 128b interconnect initiator ports (P1/P2)
EVE4_INIT NOTE: EVE4 is not supported in this family of devices.	EVE4 initiator port. Two 128b interconnect intiator ports (P1/P2)
IVA_INIT	Image and video accelerator (IVA) initiator port. One 128b initiator port
GPU_P1_INIT	GPU 128b initator port 1
GPU_P2_INIT	GPU 128b initiator port 2
BB2D_P1_INIT	2D Graphics Accelerator 128b port 1
BB2D_P2_INIT	BB2D 128b port 2

Table 14-7. Master NIUs (continued)

Master NIU	Description
DSS_INIT	Display SubSystem initiator port. One 128b initiator port
VIP1_INIT	VIP initiator ports. Two 128b initiator ports
VIP2_INIT	VIP initiator ports. Two 128b initiator ports
VIP3_INIT	VIP initiator ports. Two 128b initiator ports
VPE_INIT	Video Processing engine
PCIE1_INIT	PCIe 1 64b initiator port
PCIE2_INIT	PCIe 2 64b initiator port
PRUSS1_P1_INIT	PRU-ICSS1 32b initiator port 1
PRUSS1_P2_INIT	PRU-ICSS1 32b initiator port 2
PRUSS2_P1_INIT	PRU-ICSS2 32b initiator port 1
PRUSS2_P2_INIT	PRU-ICSS2 32b initiator port 2
TPTC1_INIT	EDMA TPTC initiator port. Two 128b initiator ports(one read port and one write port)
TPTC2_INI	EDMA TPTC initiator port. Two 128b initiator ports(one read port and one write port)
MMU1_INIT	MMU initiator port.One 128b initiator port
MMU2_INIT	MMU initiator port. One 128b initiator port
IPU1_INIT	IPU initiator port. One 64b initiator port
IPU2_INIT	IPU initiator port. One 64b initiator port
DMA_SYSTEM_INIT	System Direct Memory Access engine 32 initiator port (32b initiator read port and 32b initiator write port)
MLBSS_INIT NOTE: MLB is not supported in this family of devices.	MLB 32b initiator port
GMAC_SW_INIT	GMAC_SW 32b initiator port
MMC1_INIT	MMC initiator port. One 32b initiator port
MMC2_INIT	MMC2 32b initiator port
SATA_INIT	SATA 32b initiator port
USB1_INIT	USB3.0 initiator port. One 64b OTG initiator port
USB2_INIT	USB2.0 initiator port. One 64b OTG initiator port
USB3_INIT NOTE: USB3(ULPI) is not supported in this family of devices.	USB2.0 initiator port. One 64b OTG initiator port
USB4_INIT NOTE: USB4(ULPI) is not supported in this family of devices.	USB2.0 initiator port. One 64b OTG initiator port
IEEE1500_INIT	IEEE1500 32b initiator port
DEBUGSS_INIT	Debug subsystem 32b initiator port

Table 14-8 lists the supported slave NIU ports.

Table 14-8. Slave NIUs

Slave NIU	Description
DSP1_TARG	DSP1 128b target port
DSP2_TARG	DSP2 128b target port
DMM_P1_TARG	Dynamic memory management128b target port 1
DMM_P2_TARG	Dynamic memory management 128b target port 2
IVA_CONFIG_TARG	Video accelerator subsystem 32b configuration target port

Table 14-8. Slave NIUs (continued)

Slave NIU	Description
IVA_SL2IF_TARG	Video accelerator subsystem 128b SL target port
L4_CFG_TARG	L4 CFG 32b target port
L4_WKUP_TARG	L4 WKUP 32b target port
TPTC_P1_TARG	EDMA_TPTC 32b target port 1
TPTC_P2_TARG	EDMA_TPTC 32b target port 2
TPCC_TARG	EDMA_TPCC (TPCC) 32b target port
VCP1_TARG NOTE: VCP1 is not supported in this family of devices.	VCP 64b target port 1
VCP2_TARG NOTE: VCP2 is not supported in this family of devices.	VCP 64b target port 2
OCMC_RAM1_TARG	On-chip memory controller 128b target port 1
OCMC_RAM2_TARG	On-chip memory controller 128b target port 2
OCMC_RAM3_TARG	On-chip memory controller 128b target port 3
PCIe1/2_TARG	PCIe1/2 64b target port
GPU_TARG	3D graphics accelerator 64b target port
IPU1_P1_TARG	DUAL Cortex M4 subsystem 64b target port 1
IPU1_P2_TARG	IPU1 64b target port 2
IPU2_P1_TARG	IPU2 64b target port 1
IPU2_P2_TARG	IPU2 64b target prot2
GPMC_TARG	General-purpose memory controller target port
L4_PER/1/2/3_TARG	L4 interconnect peripherals 32b initiator port
MCASP1_TARG	McASP1 32b target port
MCASP2_TARG	McASP2 32b target port
MCASP3_TARG	McASP3 32b target port
DSS_TARG	Display subsystem 64b target port
BB2D_TARG	BB2D 32b target port
QSPI_TARG	QSPI 32b target port
EVE1_TARG NOTE: EVE1 is not supported in this family of devices.	Embedded vision engine (EVE) 128b target port
EVE2_TARG NOTE: EVE2 is not supported in this family of devices.	EVE2 128b target port
EVE3_TARG NOTE: EVE3 is not supported in this family of devices.	EVE3 128b target port
EVE4_TARG NOTE: EVE4 is not supported in this family of devices.	EVE4 128b target port
MMU1_TARG	Memory management unit (MMU) 128b target port 1
MMU2_TARG	MMU 128b target port 2
PRUSS1_TARG	PRU-ICSS1 32b target port
PRUSS2_TARG	PRU-ICSS2 32b target port
L3_INSTR_TARG	L3 instrumentation 32b target port
DEBUGSS_TARG	Debug subsystem 32b target port

14.2.3.2.2 L3_MAIN Connectivity Matrix

The L3 interconnect is divided into two clock domains L3_CLK1 and L3_CLK2. CLK1 domain is further splitted into two sub groups:

- L3_CLK1_1: Low-power domain
- L3_CLK1_2: Peripherals and multimedia
- L3_CLK2: Instrumentation (debug)

The two clock elements (CLK1 and CLK2) are implemented in a different clock domain.

14.2.3.2.2.1 Clock Domain Mapping of the L3_MAIN Interconnect Modules

Each clock domain (CLK1 and CLK2) has it own host, flag mux, slave NIUs, and bandwidth regulators. Table 14-9 lists the relationships between these domains and these elements.

Table 14-9. L3_MAIN Clock Domains and Elements

Clock Domain	Elements
L3_CLK1_1	HOST_CLK1_1
	L4_WKUP
	VCP1 NOTE: VCP1 is not supported in this family of devices.
	VCP2 NOTE: VCP2 is not supported in this family of devices.
	QSPI
	L4_PER3_P1
	L4_PER3_P2
	L4_PER3_P3
	L4_PER1_P1
	L4_PER1_P2
	L4_PER1_P3
	L4_PER2_P1
	L4_PER2_P2
	L4_PER2_P3
	PRU-ICSS1
	PRU-ICSS2
	McASP1
	McASP2
	McASP3
	GPMC
	L4_CFG
	IPU1
	IPU2
	DSP1 SDMA
	DSP2 SDMA
	EVE1 NOTE: EVE1 is not supported in this family of devices.
	EVE2 NOTE: EVE2 is not supported in this family of devices.
	EVE3 NOTE: EVE3 is not supported in this family of devices.
	EVE4 NOTE: EVE4 is not supported in this family of devices.
	DSS

Table 14-9. L3_MAIN Clock Domains and Elements (continued)

Clock Domain	Elements
	IVA SL2IF
	DMM_P1
	DMM_P2
	OCMC_RAM2
	OCMC_RAM3
	IVA CFG
	BB2D
	MMU1
	OCMC_RAM1
	TPCC (EDMA_TPCC)
	TPTC1 CFG (EDMA_TPTC1)
	TPTC2 CFG (EDMA_TPTC2)
	MMU2
	PCIe 1
	PCIe 2
	GPU
L3_CLK1_2	HOST_CLK1_2
	FLAGMUX_CLK1_MERGE
	FLAGMUX_CLK1_1
	FLAGMUX_CLK1_2
	FLAGMUX_CLK1_TIMEOUT1
	FLAGMUX_CLK1_TIMEOUT2
	DSP1_EDMA_BW_REGULATOR
	DSP2_EDMA_BW_REGULATOR
	EVE1_TC0_BW_REGULATOR NOTE: EVE1 is not supported in this family of devices.
	EVE2_TC0_BW_REGULATOR NOTE: EVE2 is not supported in this family of devices.
	EVE3_TC0_BW_REGULATOR NOTE: EVE3 is not supported in this family of devices.
	EVE4_TC0_BW_REGULATOR NOTE: EVE4 is not supported in this family of devices.
	EVE1_TC1_BW_REGULATOR
	EVE2_TC1_BW_REGULATOR
	EVE3_TC1_BW_REGULATOR
	EVE4_TC1_BW_REGULATOR
	VPE_P1_BW_LIMITER
	VPE_P2_BW_LIMITER
	IVA_BW_REGULATOR
	TPTC1_RD_BW_LIMITER
	TPTC1_WR_BW_LIMITER
	TPTC2_RD_BW_LIMITER
	TPTC2_WR_BW_LIMITER
	MMU1_BW_LIMITER
	PCIESS1_BW_REGULATOR
	PCIESS2_BW_REGULATOR
	GPU_P1_BW_REGULATOR
	GPU_P2_BW_REGULATOR

Table 14-9. L3_MAIN Clock Domains and Elements (continued)

Clock Domain	Elements
	BB2D_P1_BW_REGULATOR
	BB2D_P2_BW_REGULATOR
	MMU2_BW_REGULATOR
L3_CLK2	HOST_CLK2_1
	DEBUGSS_CT_TBR_TARG
	L3_INSTR
	STATCOLL0
	STATCOLL1
	STATCOLL2
	STATCOLL3
	STATCOLL4
	STATCOLL5
	STATCOLL6
	STATCOLL7
	STATCOLL8
	STATCOLL9
	FLAGMUX_CLK2_1
	FLAGMUX_CLK2_TIMEOUT
	FLAGMUX_STATCOLLS

Figure 14-3 shows the functional paths between the L3_MAIN master NIUs and the L3_MAIN and L3 slave NIU agents. The functional paths in L3_MAIN are indicated by the following:

- A cell contains the letter C when a functional path exists.
- A cell is empty when a functional path does not exist.

Figure 14-3. Connectivity Matrix

INITIATORS	TARGETS: DMM P1	DMM P2	OCMC RAM1	OCMC RAM2	OCMC RAM3	GPMC	DSP1 SDMA	DSP2 SDMA	EVE1	EVE2	EVE3	EVE4	OCMC ROM	IPU1	IPU2	IVA1 SL2IF	MMU1	MMU2	QSPI	GPU	BB2D	TC1_EDMA	TC2_EDMA	TPCC_EDMA	IVA_CONFIG	DSS	PCIE SS1	PCIE SS2	McASP1	McASP2	McASP3	L4_PER1_P1	L4_PER1_P2	L4_PER1_P3	L4_PER2_P1	L4_PER2_P2	L4_PER2_P3	L4_PER3_P1	L4_PER3_P2	L4_PER3_P3	L4_WKUP	L4_CFG	L3_MAIN_SN	L3_INSTR	DEBUGSS_CT_TBR	PRU-ICSS1	PRU-ICSS2	VCP1	VCP2
MPU	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C	C	C	C	C	C	C	C	C	C	C	C
DSP1 MDMA	C		C	C	C	C		C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C	C	C	C	C	C	C	C	C	C	C	C
DSP1 DMA		C	C	C	C	C		C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C		C		C		C	C	C	C	C	C	C	C
DSP1 CFG									C	C	C	C										C	C	C						C																	
DSP2 MDMA		C	C	C	C	C	C		C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
DSP2 DMA	C		C	C	C	C	C		C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C		C			C		C		C	C	C	C	C	C	C	C	C
DSP2 CFG									C	C	C	C										C	C	C																							
EVE1 P1	C		C	C	C	C	C	C		C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE1 P2		C	C	C	C	C	C	C		C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE2 P1		C	C	C	C	C	C	C	C		C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE2 P2	C		C	C	C	C	C	C	C		C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE3 P1	C		C	C	C	C	C	C	C	C		C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE3 P2		C	C	C	C	C	C	C	C	C		C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE4 P1		C	C	C	C	C	C	C	C	C	C		C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
EVE4 P2	C		C	C	C	C	C	C	C	C	C		C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C			C	C	C	C
IPU1	C		C	C	C	C	C	C	C	C	C	C	C		C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
IPU2		C	C	C	C	C	C	C	C	C	C	C	C	C		C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
VIP1 P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VIP1 P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VIP2 P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VIP2 P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VIP3 P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VIP3 P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VPE P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
VPE P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
DSS	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
IVA		C	C	C	C	C	C	C	C	C	C	C	C	C	C				C																											C	C		
GPU P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
GPU P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
BB2D P1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
BB2D P2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
DMA_SYSTEM_RD	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C	C			C			C	C	C		C	C	C		C	C	C
DMA_SYSTEM_WR	C		C	C	C	C	C	C	C	C	C	C		C	C	C			C	C	C	C	C	C	C	C	C	C	C	C	C			C			C	C	C	C			C		C	C	C
EDMA_TC0_RD	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		C	C	C		C	C	C	C	C	C	C	C	C			C			C	C	C	C	C		C	C	C	C
EDMA_TC0_WR	C		C	C	C	C	C	C	C	C	C	C		C	C	C	C		C	C	C		C	C	C	C	C	C	C	C	C			C			C	C	C	C	C	C	C	C	C	C
EDMA_TC1_RD		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		C	C	C	C		C	C	C	C	C	C	C		C		C		C		C	C	C	C	C	C	C	C	C
EDMA_TC1_WR		C	C	C	C	C	C	C	C	C	C	C		C	C	C	C		C	C	C	C	C		C	C	C	C	C	C		C		C		C		C	C	C	C	C	C	C	C	C
MMU1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C	C	C	C	C	C		C	C	C	C	C	C	C			C		C		C	C	C	C	C	C	C	C	C
PCIE_SS1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C		C	C	C	C	C	C	C	C		C	C	C	C			C			C		C	C	C			C	C	C	C	C
PCIE_SS2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		C	C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C			C	C	C	C	C
MMU2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C			C	C	C	C	C
GMAC_SW		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
SATA	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
MMC1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
MMC2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
USB1	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
USB2		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																										C	C	C	C	
USB3		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		
USB4	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																										C	C	C	C	
CS_DAP	C		C	C	C	C	C	C	C	C	C	C	C	C	C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
PRU-ICSS1_PRU0	C		C	C	C	C	C	C	C	C	C	C	C		C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
PRU-ICSS1_PRU1		C	C	C	C	C	C	C	C	C	C	C	C	C		C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
PRU-ICSS2_PRU0	C		C	C	C	C	C	C	C	C	C	C	C		C	C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
PRU-ICSS2_PRU1		C	C	C	C	C	C	C	C	C	C	C	C	C		C			C	C	C	C	C	C	C	C	C	C	C	C			C			C		C	C	C	C	C	C	C	C	C	C
MLB		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			C																											C	C		

14.2.3.2.3 Master NIU Identification

A master NIU ID (ConnID) is assigned to every module in the device. The ID uniquely identifies the master NIU for an interconnect transfer (see Table 14-10). The interconnect uses ConnID values for a number of purposes, including:

- Master source identification for the protection mechanism
- Response route generation
- Firewall error logging
- L3_MAIN interconnect error logging

Table 14-10. ConnID Values

8-bit ConnID (hex)	4-bit ConnID (hex)	Master NIU
0	0	MPU
10	1	CS_DAP
20	2	DSP1 MDMA
24	2	DSP1 CFG
28	2	DSP1 DMA
2C	2	DSP2 DMA
30	3	DSP2 CFG
34	3	DSP2 MDMA
3A	3	IVA
42	4	EVE1 P1 NOTE: EVE1 is not supported in this family of devices.
46	4	EVE2 P1 NOTE: EVE2 is not supported in this family of devices.
4A	4	EVE3 P1 NOTE: EVE3 is not supported in this family of devices.
4E	4	EVE4 P1 NOTE: EVE4 is not supported in this family of devices.
50	5	PRU-ICSS1 PRU0
54	5	PRU-ICSS1 PRU1
58	5	PRU-ICSS2 PRU0
5C	5	PRU-ICSS2 PRU1
60	6	IPU1
64	6	IPU2
68	6	DMA_SYSTEM RD
6A	6	DMA_SYSTEM WR
70	7	TC1_EDMA_WR
72	7	TC1_ EDMA_RD
74	7	TC2_EDMA_WR
76	7	TC2_EDMA_RD
80	8	DSS
84	8	MLB NOTE: MLB is not supported in this family of devices.
86	8	MMU1
88	8	PCIE1
8C	8	PCIE2
8E	8	MMU2

Table 14-10. ConnID Values (continued)

8-bit ConnID (hex)	4-bit ConnID (hex)	Master NIU
90	9	VIP1 P1
92	9	VIP1 P2
94	9	VIP2 P1
96	9	VIP2 P2
98	9	VIP3 P1
9A	9	VIP3 P2
9C	9	VPE P1
9E	9	VPE P2
A0	A	MMC1
A2	A	GPU P1
A4	A	MMC2
A6	A	GPU P2
A8	A	BB2D P1
AA	A	BB2D P2
AC	A	GMAC_SW
B0	B	USB1 (USB 3.0 SS)
B4	B	USB2 (USB2.0 SS)
B8	B	USB3 (USB2_ULPI_SS1) NOTE: USB3(ULPI) is not supported in this family of devices.
BC	B	USB4 (USB2_ULPI_SS2) NOTE: USB4(ULPI) is not supported in this family of devices.
CC	C	SATA
D2	D	EVE1 P2 NOTE: EVE1 is not supported in this family of devices.
D6	D	EVE2 P2 NOTE: EVE2 is not supported in this family of devices.
DA	D	EVE3 P2 NOTE: EVE3 is not supported in this family of devices.
DE	D	EVE4 P2 NOTE: EVE4 is not supported in this family of devices.

The 8-bit ConnID values are used by error decoding to distinguish the different initiators. They are also used by the EMIF controller. The 4-bit ConnID values are used by the firewalls to allow or not an access to a slave NIU, see Table 14-18.

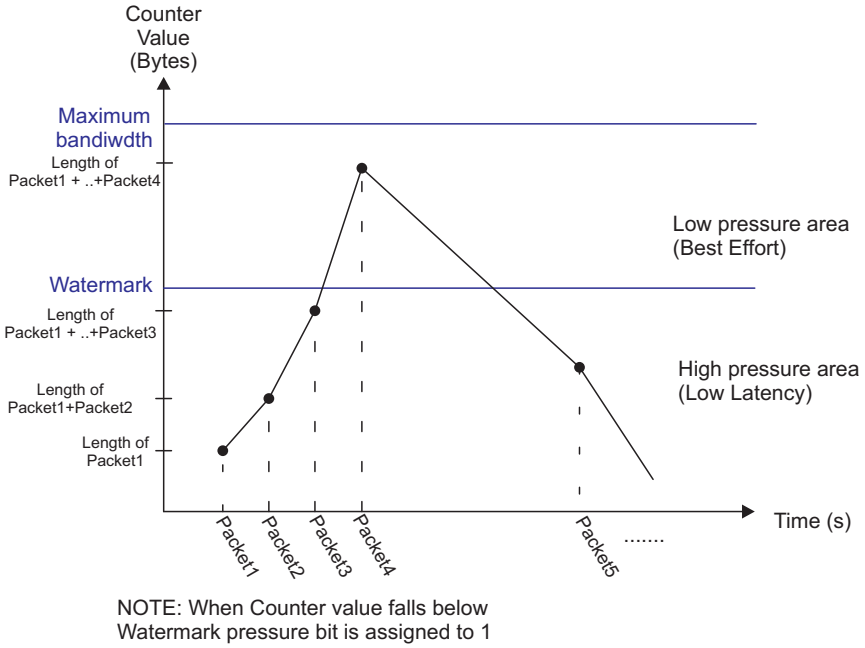
14.2.3.3 Bandwidth Regulators

The bandwidth regulators prevent master NIUs from consuming too much bandwidth of a link, or a slave NIU that is shared between several data flows: packets are then transported at a slower rate. The value of a bandwidth can be programmed in the bandwidth regulator. When the bandwidth is below the programmed value, the pressure bit is set to 1, giving priority to this master. When the bandwidth is above the programmed value, the pressure bit is set to 0 and the concerned master has the same weight as others.

A counter is used to store the sum of data lengths (in bytes) of each packet passing through the bandwidth regulator, and a value equal to the expected bandwidth is subtracted from the counter at each clock cycle. The value of the counter is compared to a programmable threshold (called Watermark), and this comparison determines whether the packet is processed with high pressure for minimum latency or low pressure for best effort processing.

The bandwidth regulator monitors the traffic using open connections between the initiators and the targets. If there is insufficient bandwidth allocated to the connection, the bandwidth regulator can increase the pressure on connections. Generally, the connection is a dataflow between master and slave NIUs. In some cases, the bandwidth regulator is attached to the master and monitors single dataflow to a target (single connection).

Figure 14-4. Bandwidth Regulator Pressure Settings



When Counter Value (bytes) falls below Watermark, the pressure bit is assigned to 1

The bandwidth regulator effective resolution is set to 8.3125 MBps. The maximum average bandwidth (max watermark value) computed in a moving window is set to up to 4096 bytes of payload. These settings are implemented by hardware.

The following is an example of bandwidth regulator settings:

Suppose the bandwidth regulator is set to run at 200 MHz and the application requires an expected bandwidth of 165.888 MBps (±5 MBps), computed through a moving window of 5 µs (1000 cycles). To attribute high pressure on all packet requests, the watermark could be set to the maximum bandwidth needed in the 5-µs window.

Considering the example, the settings of the bandwidth regulator are:

- L3_BW_REGULATOR_WATERMARK[11:0] WATERMARK = moving window × expected bandwidth = 829.44 bytes = 0x33D
- L3_BW_REGULATOR_BANDWIDTH[15:0] BANDWIDTH = ceil(165.888/8.3125) = ceil(19.956) = 20d = 0x14

The bandwidth registers regulate the packet flow by applying flow control on the RX port, thus ensuring that the traffic does not exceed the allocated bandwidth. The next packet is sent only when an internal timer expires. The registers in this group are:

- L3_BW_REGULATOR_WATERMARK: Gives the amount of data allowed to exceed the average bandwidth during a short time period
- L3_BW_REGULATOR_PRESS: Describes the pressure applied to outgoing packets
- L3_BW_REGULATOR_CLEARHISTORY: Resets the traffic counter when set to 1. This register is

used after an update in the L3_BW_REGULATOR_BANDWIDTH and L3_BW_REGULATOR_WATERMARK registers (see Section 14.2.5.1.7, *L3 BW Regulator Register Summary and Description*).

Bandwidth regulators are mainly used to give priority to the following masters: DSP1 MDMA, DSP2 MDMA, EVE1, EVE2, EVE3 and EVE4 (both ports per instance), IVA, MMU2, PCIe, DSP1 EDMA, DSP2 EDMA, GMAC SW, BB2D.

Priority to: DSP1_CFG, DSP2_CFG,DSS, GPU_P1, GPU_P2, IPU, MMU1initiator port, MPU initiator port, PCIe1 and PCIe2 initiator ports, TPTC1 and TPTC2 (RD and WR initiator ports), USB initiator ports, MLB, VIP1_P1/P2, VIP2_P1/P2, VIP3_P1/P2 initiator ports is given by setting their internal MFlag signal.

14.2.3.4 Bandwidth Limiters

The bandwidth limiter is added to control the bandwidth of GPU, EDMA_TPTC (RD and WR ports), VPE and MMU1. This prevents a large number of RD requests being processed together, thus avoiding a large number of RD responses.

The bandwidth limiter regulates the packet flow in the L3_MAIN interconnect by applying flow control when a user-defined bandwidth limit is reached. The next packet is served only after an internal timer expires, thus ensuring that traffic does not exceed the allocated bandwidth. Bandwidth limiter can be used with a watermark mechanism that allows traffic to temporarily exceeds the peak bandwidth.

The registers in this group are:

- L3_BW_LIMITER_WATERMARK_0: Gives the amount of data allowed to exceed the average bandwidth during a short time period. To set the actual watermark to n bytes, the register must be set to n + 1.
- L3_BW_LIMITER_CLEARHISTORY: Resets the traffic counter when set to 1.
- L3_BW_LIMITER_BANDWIDTH_FRACTIONAL and L3_BW_L_BANDWIDTH_INTEGER: These two registers are used to set the average payload bandwidth.

14.2.3.5 Flag Muxing

The flag mux generator collects information such as errors and interrupts from slave NIUs and the interconnect firewall. The result signals are then sent to the MPU interrupt controller (INTC) without interfering with the interconnect traffic. Using the L3_FLAGMUX_MASK registers can prevent the flag mux from seeing certain events.

The unit has a standard COREREG register for identification of the attached core type. The L3_FLAGMUX_STDHOSTHDR_VERSIONREG register identifies the characteristics of the attached core. Use unit-specific registers (MASK bit 0 or bit 1 of the flag inputs, and L3_FLAGMUX_REGERR bit 0 or bit 1) to read the input errors. Each register is dedicated to reporting the bit corresponding to the register number; for example, L3_FLAGMUX_REGERR0 reports on bit 0, and L3_FLAGMUX_REGERR1 reports on bit 1. Any given L3_FLAGMUX_REGERR register reports the same bit for all flag source inputs (see Table 14-174).

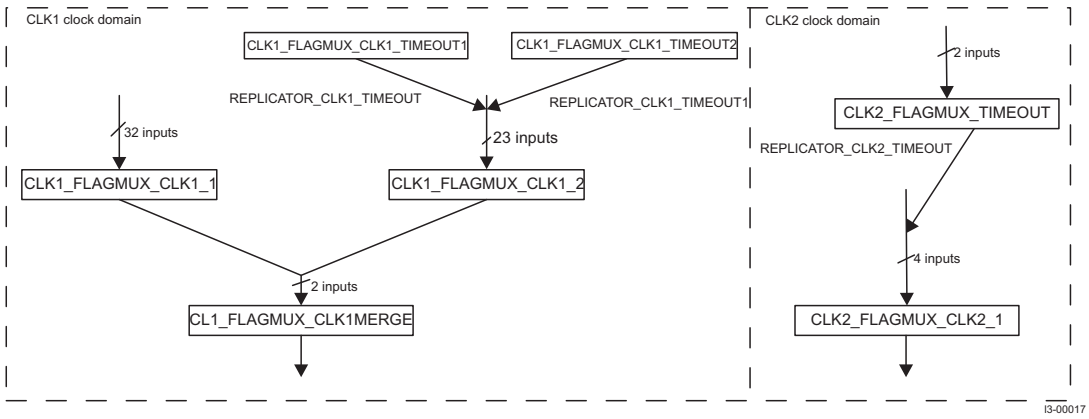
There are three flag muxs (CLK1_FLAGMUX_CLK1_1, CLK1_FLAGMUX_CLK1_2 and CLK2_FLAGMUX_CLK2_1) collecting information from targats in each clock domain in L3_MAIN interconnect (CLK1_1, CLK1_2 and CLK2_1). Both CLK1_FLAGMUX_CLK1_1 and CLK1_FLAGMUX_CLK1_2 flag muxes are located in the CLK1_2 clock domain (with base address 0x4480 0000).

Also there is a separate mux (L3_FMAGMUX_CLK1MERGE) that merges the inputs from CLK1_1 and CLK1_2 flag muxes. Its functionality is similar to the functionality of the other L3_FLAGMUXES:

- L3_FLAGMUX_CLK1MERGE_COREREG and L3_FLAGMUX_STDHOSTHDR_VERSIONREG registers are used to identify the attached core and its characteristics.
- L3_FLAGMUX_CLK1MERGE_MASK0 is used to mask (enable) application error sources
- L3_FLAGMUX_CLK1MERGE_REGERR0 is used to check which application error sources are active
- L3_FLAGMUX_CLK1MERGE_MASK1 is used to mask debug error sources
- L3_FLAGMUX_CLK1MERGE_REGERR1 is used to check which debug error sources are active

Following is a block diagram of the flag mux organization in L3_MAIN interconnect:

Figure 14-5. Flag Mux Structure



14.2.3.5.1 Flag Mux Time-out

If a target does not respond after a fixed number of clock cycles, an error time-out flag is generated, in case it is enabled. The value of the flag is always 3 if a time-out error is present.

To enable time-out for each target, set the corresponding bit in L3_FLAGMUX_TIMEOUT_MASK0 register to 1. See Table 14-11.

Table 14-11. L3 Time-out Flag Mapping

	Flag Mux Input	Source
CLK1_1 Time-out FlagMux (TIMEOUT1)	2	DSP1 SDMA
	3	DSP2 SDMA
	4	DSS
	5	EVE1 NOTE: EVE1 is not supported in this family of devices.
	6	EVE2 NOTE: EVE2 is not supported in this family of devices.
	7	EVE3 NOTE: EVE3 is not supported in this family of devices.
	8	EVE4 NOTE: EVE4 is not supported in this family of devices.
	9	GPU
	10	BB2D
	11	IPU1
	12	IPU2
	13	IVA CONFIG
	14	MMU1
	15	DMM P1
	16	DMM P2
	17	IVA SL2IF
	18	MMU2
	19	L4_PER1 P1
	20	L4_PER1 P2
	21	L4_PER1 P3
	22	L4_PER2 P2
	23	L4_PER2 P1

Table 14-11. L3 Time-out Flag Mapping (continued)

	Flag Mux Input	Source
	24	L4_PER2 P3
	25	L4_PER3 P2
	26	L4_PER3 P1
	27	L4_PER3 P3
	28	L4_CFG
	29	L4_WKUP
CLK1_2 Time-out FlagMux (TIMEOUT2)	1	PCIE1
	2	PCIE2
	6	QSPI
	8	TPCC
	9	TPTC1
	10	TPTC2
	12	OCMC_RAM3
	13	McASP1
	14	McASP2
	15	McASP3
	16	OCMC_RAM1
	17	OCMC_RAM2
	18	GPMC
	19	VCP1 NOTE: VCP1 is not supported in this family of devices.
	20	VCP2 NOTE: VCP2 is not supported in this family of devices.
CLK2_1 Time-out FlagMux	0	L3_INSTR
	1	DEBUGSS_CT_TBR

NOTE: Missing inputs in Table 14-11 are reserved locations. Writing in them has no effect.

For example, to enable all targets in CLK1_1, write 0x3FFF FFFF in L3_FLAGMUX_TIMEOUT1_MASK0; to enable all targets in CLK1_2, write 0x1F FFFF in L3_FLAGMUX_TIMEOUT2_MASK0. To enable only OCMC_RAM1 (target in CLK1_2) write 0x1 0000 in L3_FLAGMUX_TIMEOUT2_MASK0. If an error time-out occurs, read the registers L3_FLAGMUX_TIMEOUT1_REGERR0 and L3_FLAGMUX_TIMEOUT2_REGERR0 to determine the source of error concerning Table 14-11. CLK2 time-outs are reported through CLK1_FLAGMUX_CLK2_1 status registers (L3_FLAGMUX_REGERR0, L3_FLAGMUX_REGERR1) and masked through L3_FLAGMUX_MASK0 and L3_FLAGMUX_MASK1 registers.

Similarly, to enable a target in CLK2_1, write the appropriate value (as described in Table 14-11) in L3_FLAGMUX_TIMEOUT_MASK0.

If an error time-out occurs in CLK2_1, read the L3_FLAGMUX_TIMEOUT_REGERR0 register to determine the source of error concerning Table 14-11.

14.2.3.6 Statistic Collectors Group

Statistic collectors are internal masters that share the same master address as the master NIUs. These components compute the traffic statistics within a defined window and periodically report through the DEBUG interface. The key features of the statistic collector are:

- Nonintrusive monitoring
- Programmable filters and counters
- Collects results at a programmable time interval

Event detectors are programmed through the L3_STCOL_REQEVT and L3_STCOL_RSPEVT configuration registers for request and response ports, respectively. The following events can be identified:

- Word transfer
- WAIT cycles
- Flow control
- Payload transfers
- Latency measurements

Performance monitoring is enabled through the L3_STCOL_EN register. The L3_STCOL_SOFTEN register enables software to monitor the performance. Event muxes are programmed through the L3_STCOL_EVTMUX_SEL0 configuration register, which determines which port will be monitored by a filter configured by the filter registers (see Section 14.2.5.1.9).

Filters are programmed through the L3_STCOL_FILTER_i_GLOBALEN configuration register, along with additional selection criteria programmed through the mask/match registers (see Table 14-240). A filter can be configured to accept or reject:

- Read operations
- Write operations
- Errors
- Addresses

Filter operation is programmed through the L3_STCOL_OP registers (see Table 14-240).

There are ten statistic collectors used to monitor the traffic on DRAM (EMIF1, EMIF2, MA_MPU_P1 and MA_MPU_P2), MPU, MMU, TPTC, VIP, EVE Subsystem, DSP MDMA/EDMA, IVA, GPU, DSS, IPU, OCMC RAM, PCIe Subsystem, VCP, DSP CFG and GPMC ports. For more detailed descriptions of statistic collectors, see Section 34.10.7.1, *L3 Target Load Monitoring*, and Section 34.10.7.2, *L3 Master Latency Monitoring*.

14.2.3.7 L3_MAIN Protection and Firewalls

Device protection relies on L3 firewalls and their configuration.

14.2.3.7.1 L3_MAIN Firewall Reset

The values of L3_MAIN firewall registers on reset are tied in hardware or exported from the control module registers.

Values exported from the control module are intended to give defined rights to the firewalls at reset and thus ensure the content after going out of reset.

The L3_MAIN firewall registers are located in the CORE AON power domain and thus no retention capability is needed. The control module registers are reset by a cold reset only, whereas the L3_MAIN firewall registers are reset by clearing the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit. When the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit comes back automatically to 1, the exported values are loaded.

CAUTION

Before reprogramming the firewall registers and/or before using the FW_LOAD_REQ mechanism, the request must be asserted by configuring the REGUPDATE_CONTROL[0] BUSY_REQ bit.

To load the exported values at run time:

1. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x1 to ensure that no transaction can reach the slave NIU (suspend).
2. Clear the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit by writing 0x1 to it.
3. Wait until the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit is reset to 0x1 by hardware.

4. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x0 to allow transactions to reach the slave NIU (resume).

To reprogram the firewall registers at run time:

1. Write 0x1 to the REGUPDATE_CONTROL register.
2. Update the firewall registers.
3. Write 0x0 to the REGUPDATE_CONTROL register.

NOTE: While reprogramming the firewall registers at run time it must be taken into account that the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit is written as '0' because a value of '1' reloads the firewall default values.

NOTE: At reset, exported values from the control module can modify hardware reset values.

14.2.3.7.1.1 L3_MAIN Firewall – Exported Reset Values

Table 14-12 and Table 14-13 list the exported reset values and mapping, respectively.

Table 14-12. L3_MAIN Firewall Exported Reset Values

MRM_PERMISSION_REGION_LOW_j [15:12]	MRM_PERMISSION_REGION_LOW_j [11:0]
0x0	0xFFF
0xF	0xFFF
0x0	0xFFF
0x2	0xFFF

Table 14-13. L3_MAIN Firewall Exported Values Mapping

CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_LOCK_1 and CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_DBG_1 Bits	Slave NIU Firewall
[0]	GPMC
[3]	L3 RAM1
[4]	DSS
[6]	GPU
[7]	IVAHD SL2IF
[8]	IVAHD CONFIG
[11]	EMIF and MA_MPU_NTTP
[12]	DEBUGSS
[13]	CT_TBR
[16]	EVE1 NOTE: EVE1 is not supported in this family of devices.
[17]	EVE2 NOTE: EVE2 is not supported in this family of devices.
[18]	EVE3 NOTE: EVE3 is not supported in this family of devices.
[19]	EVE4 NOTE: EVE4 is not supported in this family of devices.
[20]	PCIESS1
[21]	PCIESS2
[22]	IPU1
[23]	IPU2

Table 14-13. L3_MAIN Firewall Exported Values Mapping (continued)

CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_LOCK_1 and CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_DBG_1 Bits	Slave NIU Firewall
[24]	VCP1 NOTE: VCP1 is not supported in this family of devices.
[25]	VCP2 NOTE: VCP2 is not supported in this family of devices.
[26]	McASP1
[27]	McASP2
[28]	McASP3
[31]	BB2D

Table 14-14. L3_MAIN Firewall Exported Values Mapping

CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_LOCK_2 and CONTROL_CORE_L3_HW_FW_EXPORTED_VALUES_CONF_DBG_2 Bits	Slave NIU Firewall
[0]	DSP1
[1]	DSP2
[2]	L3 RAM2
[3]	L3 RAM3
[6]	PRU-ICSS1
[7]	PRU-ICSS2
[8]	QSPI
[9]	EDMA TC
[10]	EDMA TPCC

For more information, see Chapter 18, *Control Module*.

14.2.3.7.2 Power Management

As part of the system-wide power-management scheme, the L3_MAIN interconnect goes into IDLE state after receiving a request from the power, reset, and clock management (PRCM) module after all commands are serviced. This function is handled by hardware.

To reduce power consumption, the L3_MAIN interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

L3_MAIN supports a partial retention scheme. Retention is performed on the follwoing registers:

- Statistic collectors
- Bandwidth regulators
- Firewalls

This process prevents reconfiguration after a clock domain switches off.

14.2.3.7.3 L3_MAIN Firewall Functionality

The access to the slave NIUs is granted only to master NIUs according to in-band attributes sent in each transaction crossing the L3_MAIN interconnect, such as:

- MCMD: Specifies the type of access (read or write) required by the master NIU
- ConnID: Used to determine the permission of the master NIU
- MReqInfo: Transaction attribute adding information about the access type

Table 14-15 lists the MReqInfo values.

Table 14-15. MReqInfo Values

Qualifier	Access Definition	Access Description
MReqType	00: Processor data access 01: Processor instruction access 10: DMA access 11: Other	Indicates whether the request is for processor instruction fetch, processor data access or DMA access
MReqDebug	0: Functional 1: Debug	When set, indicates that the request has been issued by a master NIU in DEBUG state
MReqSupervisor	0: User 1: Privilege	When set, indicates that the request is qualified with the supervisor attribute. It can be provided by a processor running in supervisor mode or by a module that inherited this attribute from the processor (DMA channel with a supervisor attribute).

The firewall comparison mechanism enables access to a protected slave NIU only when a correct combination of three MReqInfo in-band parameters is transmitted.

MReqInfo is a combination of a fixed 3-bit pattern that corresponds to a combination of the parameters MReqDebug, MReqType, and MReqSupervisor. See Table 14-16.

Table 14-16. L3_MAIN ReqInfo Mapping

ReqInfo Name		MReqDebug	MReqType	MReqSupervisor
Master NIUs	MPU INIT	x	x	x
	MMU1 INIT	x		x
	TPTC1_RD INIT			x
	TPTC1_WR INIT			x
	TPTC2_RD INIT			x
	TPTC2_WR INIT			x
	VPE_P1 INIT			
	VPE_P2 INIT			
	VIP1_P1 INIT			
	VIP1_P2 INIT			
	VIP2_P1 INIT			
	VIP2_P2 INIT			
	VIP3_P1 INIT			
	VIP3_P2 INIT			
	EVE1_P1 INIT NOTE: EVE1 is not supported in this family of devices.	x	x	
	EVE1_P2 INIT	x	x	
	EVE2_P1 INIT NOTE: EVE2 is not supported in this family of devices.	x	x	
	EVE2_P2 INIT	x	x	
	EVE3_P1 INIT NOTE: EVE3 is not supported in this family of devices.	x	x	
	EVE3_P2 INIT	x	x	
	EVE4_P1 INIT NOTE: EVE4 is not supported in this family of devices.	x	x	
	EVE4_P2 INIT	x	x	

Table 14-16. L3_MAIN ReqInfo Mapping (continued)

ReqInfo	Name	MReqDebug	MReqType	MReqSupervisor
	DSP1 EDMA INIT	x	x	x
	DSP1 MDMA INIT	x	x	x
	DSP2 EDMA INIT	x	x	x
	DSP2 MDMA INIT	x	x	x
	IVA INIT			
	PRU-ICSS1 PRU0			
	PRU-ICSS1 PRU1			
	PRU-ICSS2 PRU0			
	PRU-ICSS2 PRU1			
	GPU_P1 INIT			
	GPU_P2 INIT			
	BB2D_P1_INIT			
	BB2D_P2_INIT			
	DSS INIT			
	MMU2 INIT	x		x
	IPU1 INIT	x	x	x
	IPU2 INIT	x	x	x
	DMA_SYSTEM_RD		x	x
	DMA_SYSTEM_WR		x	x
	USB1 INIT			
	USB2 INIT			
	USB3 INIT NOTE: USB3(ULPI) is not supported in this family of devices.			
	USB4_INIT NOTE: USB4(ULPI) is not supported in this family of devices.			
	PCIe_SS1 INIT			
	PCIe_SS2 INIT			
	DSP1_CFG INIT	x	x	x
	DSP2_CFG_INIT	x	x	x
	GMAC SW INIT			
	MMC1 INIT			
	MMC2 INIT			
	SATA INIT			
	MLB INIT NOTE: MLB is not supported in this family of devices.			
	DAP INIT	x		x
Slave NIUs	DMM_P1 TARG	x	x	x
	DMM_P2 TARG	x	x	x
	DSP1 SDMA TARG	x	x	x
	DSP2 SDMA TARG	x	x	x
	EVE1 TARG NOTE: EVE1 is not supported in this family of devices.	x		

Table 14-16. L3_MAIN ReqInfo Mapping (continued)

ReqInfo	Name	MReqDebug	MReqType	MReqSupervisor
	EVE2 TARG NOTE: EVE2 is not supported in this family of devices.	x		
	EVE3 TARG NOTE: EVE3 is not supported in this family of devices.	x		
	EVE4 TARG NOTE: EVE4 is not supported in this family of devices.	x		
	L4_CFG TARG	x		x
	L4_WKUP TARG	x		x
	TPTC1_CFG TARG	x		x
	TPTC2_CFG TARG	x		x
	TPCC TARG	x	x	x
	L3_INSTR TARG	x		
	DEBUGSS TARG	x		
	OCMC_RAM1 TARG			
	OCMC_RAM2 TARG			
	OCMC_RAM3 TARG			
	GPU TARG			
	IPU1 TARG			
	VCP1 TARG NOTE: VCP1 is not supported in this family of devices.			
	VCP2 TARG NOTE: VCP2 is not supported in this family of devices.			
	IPU2 TARG			
	PCIESS1 TARG			
	PCESS2 TARG			
	GPMC TARG			
	L4_PER1_P1 TARG	x		x
	L4_PER1_P2 TARG	x		x
	L4_PER1_P3 TARG	x		x
	L4_PER2_P1 TARG	x		x
	L4_PER2_P2 TARG	x		x
	L4_PER2_P3 TARG	x		x
	L4_PER3_P1 TARG	x		x
	L4_PER3_P2 TARG	x		x
	L4_PER3_P3 TARG	x		x
	QSPI TARG			
	McASP1 TARG			
	McASP2 TARG			
	McASP3 TARG			
	DSS TARG			x
	BB2D TARG			
	IVA_CFG TARG	x		

Table 14-16. L3_MAIN ReqInfo Mapping (continued)

ReqInfo Name		MReqDebug	MReqType	MReqSupervisor
	MMU1 TARG	x		x
	MMU2 TARG	x		x

14.2.3.7.3.1 Protection Regions

Each slave NIU address space is subdivided into protection regions (maximum of 10). The regions are configurable with a size of 4-KiB granularity. The firewalls can also be multiport while using the description of the same regions for dual access memories or to support interleaving mechanisms on several memories.

Table 14-17 lists the number of protected regions and ports for each slave NIU.

Table 14-17. Slave NIU Firewall and Region Configuration

Domain	Slave NIU	Firewall	Number of Regions	Number of Ports
	DSP1_SDMA	DSP1_SDMA_FW	1	1
	DSP2_SDMA	DSP2_SDMA_FW	1	1
	DSS	DSS_FW	8	1
	EVE1 NOTE: EVE1 is not supported in this family of devices.	EVE1_FW	1	1
	EVE2 NOTE: EVE2 is not supported in this family of devices.	EVE2_FW	1	1
	EVE3 NOTE: EVE3 is not supported in this family of devices.	EVE3_FW	1	1
	EVE4 NOTE: EVE4 is not supported in this family of devices.	EVE4_FW	1	1
	GPMC	GPMC_FW	8	1
	GPU	GPU_FW	1	1
	IPU1	IPU1_FW	4	1
	IPU2	IPU2_FW	4	1
	PRU-ICSS1	PRUSS1_FW	1	1
	PRU-ICSS2	PRUSS2_FW	1	1
CLK1	IVA_CFG	IVA_CFG_FW	1	1
	IVA_SL2IF	IVA_SL2IF_FW	4	1
	OCMC_RAM1	OCMC_RAM1_FW	16	1
	OCMC_RAM2	OCMC_RAM2_FW	16	1
	OCMC_RAM3	OCMC_RAM3_FW	16	1
	EMIF1, EMIF2	EMIF_OCP_FW	8	2
	EMIF1, EMIF2	MA_MPU_NTTP_FW	8	2
	PCIESS1	PCIESS1_FW	8	1
	PCIESS2	PCIESS2_FW	8	1
	BB2D	BB2D_FW	1	1
	QSPI	QSPI_FW	1	1
	TPCC	TPCC_FW	1	1
	TPTC	TPTC_FW	2	2
	VCP1 NOTE: VCP is not supported in this family of devices.	VCP1_FW	1	1

Table 14-17. Slave NIU Firewall and Region Configuration (continued)

Domain	Slave NIU	Firewall	Number of Regions	Number of Ports
	VCP2	VCP2_FW	1	1
	McASP1	MCASP1_FW	1	1
	McASP2	MCASP2_FW	1	1
	McASP3	MCASP3_FW	1	1
CLK2	L3_INSTR	L3_INSTR_FW	2	1
	DEBUGSS_CT_TBR	DEBUGSS_CT_TBR_FW	1	1

Two types of regions are distinguished in a slave NIU firewall:

- Default region: Available in all slave NIUs. The default region covers the entire slave NIU address range. Other firewall-configured regions must reset or overlay the default region, because it always has the lowest priority.
- Normal region: The number of normal regions varies in a slave NIU; they have identical capabilities (see Table 14-17).

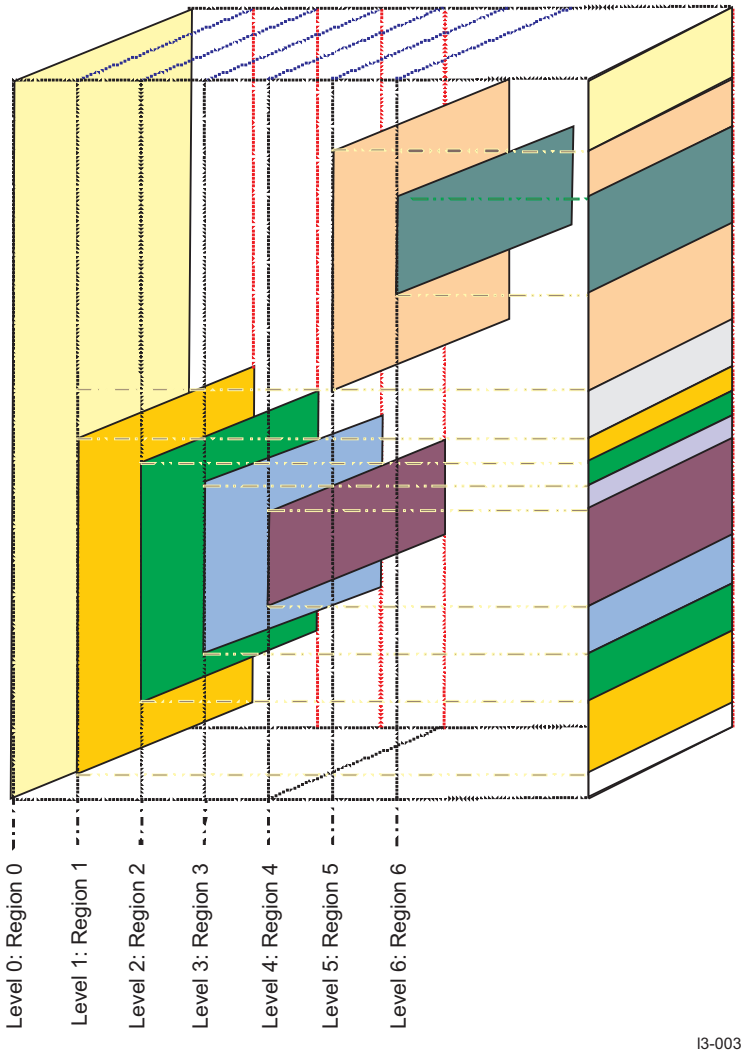
Each region has the following characteristics:

- Start address: Physical slave NIU start address
- End address: Physical slave NIU end address
- Specific access rights (see Section 14.2.3.7.3.3, *Protection Mechanism per Region Examples*)
- Priority level from 0 (lowest) to 10 (highest)

Depending on its priority level, a region can override the settings of another region; the access rights of the region with the highest priority apply. All regions have a fixed (not configurable) priority level that corresponds to their number: Region 1 has priority level 1, region 2 has priority level 2, and so on.

Figure 14-6 shows the priority level with associated regions. This priority level scheme allows multiplying the flexibility and capability of the firewall. Figure 14-6 shows a 7-region firewall setting that creates 16 regions (twice the number of regions created than originally available).

Figure 14-6. L3 Interconnect Region Overlay and Priority Level Overview



The address range covered by the regions is defined in the START_REGION_i and END_REGION_i registers. The boundary checks are done on a minimum size of 4-KiB pages; thus, bits [11:0] of those 32-bit registers are not checked.

The address space size of the slave NIUs ([bits [31:12]) depends on the size of the slave NIU to protect (that is, if a memory is only 48KiB, then the size is defined through bits [16:12] of the slave NIU start and end address registers of the firewall region (START_REGION_i[16:12] and END_REGION_i[16:12]).

On multiport firewalls (EMIF_OCP_FW), the checking of each REGION {0, n} can activate on one or several ports at the same time. However, if interleaving is not desired on some parts of the protected memory space, it is possible to apply or not apply region checking on selected ports using the region enable/disable on port instance capability of the END_REGION_i register.

Most slave NIUs support only one input port (port 0) except:

- The MA_MPU firewall (MA_MPU_NTTP_FW) which has two ports:
  - Port 0 for access from the MPU to EMIF1
  - Port 1 for access from the MPU to EMIF2
- The EMIF firewall which has two ports:
  - Port 0 for access from the DMM to EMIF1
  - Port 1 for access from the DMM to EMIF2

- The EDMA_TC firewall which has two ports:
  - Port 0 logs errors in the ERROR_LOG_0 register for the traffic to EDMA_TPTC0 module generated by the MPU, DSP1/2, EVE1/2/3/4, IPU1, PCIESS1/2, MMU1/2, PRU-ICSS1 and DAP modules.
  - Port 1 logs errors in the ERROR_LOG_1 register for the traffic to EDMA_TPTC1 module generated by the MPU, DSP1/2, EVE1/2/3/4, IPU1, PCIESS1/2, MMU1/2, PRU-ICSS1 and DAP modules.

A region can be applied or not to each port independently. To enable and disable the regions:

- For port 0: Set/clear the END_REGION_i[0] END_REGION_i_ENABLE_CORE0 bit (for all L3_MAIN firewalls).
- For port 1: Set/clear the END_REGION_i[1] END_REGION_i_ENABLE_CORE1 bit (for MA_MPU, EMIF and EDMA_TC firewalls).

The EMIF firewall (EMIF_OCP_FW) uses 16 GiB address space and protects both the SDRAM and the EMIF configuration registers. The EMIF firewall allows defining access restrictions per region. The region can apply to:

- Both EMIF1 and EMIF2 controllers (interleaving mode)
- Only the EMIF1 controller
- Only the EMIF2 controller

This per-region capability is defined by configuring the END_REGION_i[1:0] bit field for:

- Both EMIF1 and EMIF2 (interleaving mode): END_REGION_i[0] END_REGION_i_ENABLE_CORE_0 = 0x1 and END_REGION_i[1]END_REGION_i_ENABLE_CORE_1 = 0x1
- Only EMIF1: END_REGION_i[0] END_REGION_i_ENABLE_CORE_0 = 0x1
- Only EMIF2: END_REGION_i[1] END_REGION_i_ENABLE_CORE_1 = 0x1

The protection regions for EMIF firewall are configurable with a size of 4-KiB granularity (the same applies to the MA_MPU_NTTP_FW). The address range covered by the regions is defined in the START_REGION_i and END_REGION_i registers. Since EMIF firewall sees 16 GiB address space but these two registers have only 32 bits, the START_REGION_i/END_REGION_i[31] bit is mapped to bit [33] of the EMIF address space, that is, bits [31:10] of START_REGION_i/END_REGION_i are mapped to EMIF Address [33:12]. START_REGION_i/END_REGION_i [9:0] are not checked for the minimum page size of 4 KiB.

The start address in the EMIF address space for accessing the EMIF configuration registers is 0x3_0000_0000. If protection of these registers is needed, that address must be right shifted by 2 bits and then the result (0xC000_0000) must be written to the START_REGION_i register. The REGUPDATE_CONTROL[19:16] FW_ADDR_SPACE_MSB bit field indicates how many bits are shifted in the firewall address space. In case of EMIF_OCP_FW and MA_MPU_NTTP_FW, 2 bits are shifted. If target address space is ≤ 4 GiB then REGUPDATE_CONTROL[19:16] FW_ADDR_SPACE_MSB is 0x0 and the START_REGION_i/END_REGION_i [31:12] bits match target physical address [31:12]. Bits [11:0] are ignored by the firewall. These bits are not involved in the address check. To match address spaces greater than 4 GiB but keep the minimum page size of 4 KiB some of the START_REGION_i/END_REGION_i [11:0] bits must also be configured. In the EMIF case bits [11:10] are also used.

For example, the EMIF1 configuration registers are accessible through system base address 0x4C00_0000. But the EMIF_OCP_FW sees them at start address 0x3_0000_0000. As previously mentioned that address must be shifted before being programmed to the START_REGION_i register. In this case the programmed value should be 0xC000_0000. This has to be taken into account.

14.2.3.7.3.2 L3_MAIN Firewall Registers Overview

Table 14-18 and Table 14-19 list the L3_MAIN firewall permission-setting registers.

Table 14-18. L3_MAIN Firewall Read/Write Permission-Setting Register

Register Name	Bits	Field Name	4-bit ConnID Value (hex) (see Table 14-10)	Field Modifiability
MRM_PERMISSION_REGION_HIGH_j	31	W	ConnID = F write permission	RW
	30	R	ConnID = F read permission	RW
	29	W	ConnID = E write permission	RW
	28	R	ConnID = E read permission	RW
	27	W	ConnID = D write permission	RW
	26	R	ConnID = D read permission	RW
	25	W	ConnID = C write permission	RW
	24	R	ConnID = C read permission	RW
	23	W	ConnID = B write permission	RW
	22	R	ConnID = B read permission	RW
	21	W	ConnID = A write permission	RW
	20	R	ConnID = A read permission	RW
	19	W	ConnID = 9 write permission	RW
	18	R	ConnID = 9 read permission	RW
	17	W	ConnID = 8 write permission	RW
	16	R	ConnID = 8 read permission	RW
	15	W	ConnID = 7 write permission	RW
	14	R	ConnID = 7 read permission	RW
	13	W	ConnID = 6 write permission	RW
	12	R	ConnID = 6 read permission	RW
	11	W	ConnID = 5 write permission	RW
	10	R	ConnID = 5 read permission	RW
	9	W	ConnID = 4 write permission	RW
	8	R	ConnID = 4 read permission	RW
	7	W	ConnID = 3 write permission	RW
	6	R	ConnID = 3 read permission	RW
	5	W	ConnID = 2 write permission	RW
	4	R	ConnID = 2 read permission	RW
	3	W	ConnID = 1 write permission	RW
	2	R	ConnID = 1 read permission	RW
	1	W	ConnID = 0 write permission	RW
	0	R	ConnID = 0 read permission	RW

Table 14-19. L3_MAIN Firewall Permission-Setting Register

Register name	Type of Permission	Bits	Field Name	Description	Field Modifiability
MRM_PERMISSION_REGION_LOW_j	Reserved	31:16	Reserved		
	Debug	15	DEBUG	PUBLIC PRIVILEGE DOMAIN DEBUG ALLOWED	RW
		14	DEBUG	PUBLIC USER DOMAIN DEBUG ALLOWED	RW
	Reserved	13:12	Reserved		
	Access	11	READ	PUBLIC PRIVILEGE READ ACCESS ALLOWED	RW
		10	WRITE	PUBLIC PRIVILEGE WRITE ACCESS ALLOWED	RW
		9	EXE	PUBLIC PRIVILEGE EXE ACCESS ALLOWED	RW
		8	READ	PUBLIC USER READ ACCESS ALLOWED	RW
		7	WRITE	PUBLIC USER WRITE ACCESS ALLOWED	RW
		6	EXE	PUBLIC USER ECXE ACCESS ALLOWED	RW

14.2.3.7.3.3 Protection Mechanism per Region Examples

The access permission of each region is configurable and defined through the MRM_PERMISSION_REGION_HIGH_j and MRM_PERMISSION_REGION_LOW_j registers (see Section 14.2.3.7.3.2, *L3_MAIN Firewall Registers Overview*).

Master NIU permissions:

1. To give read access to the master NIU with 4-bit ConnID = n (1), set the MRM_PERMISSION_REGION_HIGH_j[n × 2] R bit.
2. To give write access to the master NIU with 4-bit ConnID = n (1), set the MRM_PERMISSION_REGION_HIGH_j[n × 2 + 1] W bit.

(1) - n should be first converted from hex to decimal value

Debug permissions:

1. To give privilege debug access, set the MRM_PERMISSION_REGION_LOW_j[15] DEBUG bit.
2. To give user debug access, set the MRM_PERMISSION_REGION_LOW_j[14] DEBUG bit.

User, read, write, and executable permissions:

1. To give privileged read access, set the MRM_PERMISSION_REGION_LOW_j[11] READ bit.
2. To give privileged write access, set the MRM_PERMISSION_REGION_LOW_j[10] WRITE bit.
3. To give privileged executable access, set the MRM_PERMISSION_REGION_LOW_j[9] EXE bit.
4. To give user read access, set the MRM_PERMISSION_REGION_LOW_j[8] READ bit.
5. To give user write access, set the MRM_PERMISSION_REGION_LOW_j[7] WRITE bit.
6. To give user executable access, set the MRM_PERMISSION_REGION_LOW_j[6] EXE bit.

Example: To provide debug write privilege access to the master NIU with 4-bit ConnID = 0x7, set the following bits:

- MRM_PERMISSION_REGION_HIGH_j[15] W
- MRM_PERMISSION_REGION_LOW_j[15] DEBUG

14.2.3.7.3.4 L3_MAIN Firewall Error Logging

If a protection violation error is detected, the following signals are generated:

- An in-band error (SRESP = ERROR) is generated to the master NIU of the access.

- An out-band error is sent to the control module
- An interrupt is generated to the Cortex-A15 INTC.

The L3_MAIN interconnect does not differentiate errors generated by firewalls from all other supported types of errors.

An in-band error is generated by modules each time an access is not allowed. When an in-band error is sent back into the transaction it is seen as an external prefetch or data abort by the initiator, depending on whether the transaction was an instruction fetch or a data access.

Information about in-band errors is logged into two registers:

- ERROR_LOG_k: Logs the information about the start/end address of the hit region and the qualifiers of the transaction
- LOGICAL_PHYSICAL_ADDRESS_ERRLOG_k[31:12]: Logs the address of the failed access

NOTE: When a multiport firewall is implemented, these registers are duplicated for each port.

Table 14-20 lists the L3_MAIN firewall error-logging registers.

Table 14-20. L3 Firewall Error-Logging Registers

Register Name	Register Field Name	Field Modifiability	Parameter Comments
ERROR_LOG_k (When multiport firewall is implemented the error log register is duplicated for each port.)	RESERVED[31:24]	Read only	Reads return 0s.
	BLK_BURST_VIOLATION[23]	Read/write	Read 0x1: 2D burst not allowed or exceeds allowed size. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	RESERVED[22]	Read only	Read return 0s.
	REGION_START_ERRLOG[21:17]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	REGION_END_ERRLOG[16:12]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	REQINFO_ERRLOG[11:0]	Read/write	Mapping of the error according to the reqinfo vector: ConnID [3:0] MCMD [0] [3] MReqDebug [1] MReqSupervisor [0] MReqType

L3 firewall errors can be cleared by writing to the ERROR_LOG_k register in the firewall that recorded the error. Clearing the ERROR_LOG_k register deasserts the corresponding error if it exists.

The L3 firewall register ERROR_LOG_k must be cleared before clearing the SEC_ERR_STATUS_FUNC_1/2 and SEC_ERR_STATUS_DEBUG_1/2 registers in the control module.

When a protection violation occurs, an interrupt is sent to the IRQ_CROSSBAR. An in-band error is sent back, and an error is logged in the SEC_ERR_STATUS_FUNC_1/2 and SEC_ERR_STATUS_DEBUG_1/2 registers, depending on the functional mode:

- In application mode:
  - SEC_ERR_STATUS_FUNC_1[1] – L3 RAM protection violation
  - SEC_ERR_STATUS_FUNC_1[2] – GPMC protection violation
  - SEC_ERR_STATUS_FUNC_1[3] – EMIF protection violation
  - SEC_ERR_STATUS_FUNC_1[4] – IVA protection violation
  - SEC_ERR_STATUS_FUNC_1[5] – IPU protection violation

- SEC_ERR_STATUS_FUNC_1[6] – IVA SL2 protection violation
- SEC_ERR_STATUS_FUNC_1[8] – SYSTEM DMA protection violation
- SEC_ERR_STATUS_FUNC_1[10] – DSPDMA slave NIU protection violation
- SEC_ERR_STATUS_FUNC_1[13] – GPU protection violation
- SEC_ERR_STATUS_FUNC_1[14] – DSS protection violation
- SEC_ERR_STATUS_FUNC_1[16] – L4_PER1 protection violation
- SEC_ERR_STATUS_FUNC_1[17] – L4_CFG protection violation
- SEC_ERR_STATUS_FUNC_1[18] – DEBUG subsystem protection violation
- SEC_ERR_STATUS_FUNC_1[22] – L4_WKUP protection violation
- SEC_ERR_STATUS_FUNC_1[23] - BB2D protection violation
- SEC_ERR_STATUS_FUNC_1[26] – CT_TBR protection violation
- SEC_ERR_STATUS_FUNC_1[28] – EVE1 protection violation
- SEC_ERR_STATUS_FUNC_1[29] – EVE2 protection violation
- SEC_ERR_STATUS_FUNC_1[30] – EVE3 protection violation
- SEC_ERR_STATUS_FUNC_1[31] – EVE4 protection violation
- SEC_ERR_STATUS_FUNC_2[0] – DSP1 protection violation
- SEC_ERR_STATUS_FUNC_2[1] – DSP2 protection violation
- SEC_ERR_STATUS_FUNC_2[2] – OCMC_RAM2 protection violation
- SEC_ERR_STATUS_FUNC_2[3] – OCMC_RAM3 protection violation
- SEC_ERR_STATUS_FUNC_2[4] – L4_PER2 protection violation
- SEC_ERR_STATUS_FUNC_2[5] – L4_PER3 protection violation
- SEC_ERR_STATUS_FUNC_2[6] - IPU2 protection violation
- SEC_ERR_STATUS_FUNC_2[7] – PCIESS1 protection violation
- SEC_ERR_STATUS_FUNC_2[8] - PCIESS2 protection violation
- SEC_ERR_STATUS_FUNC_2[11] – McASP1 protection violation
- SEC_ERR_STATUS_FUNC_2[12] – McASP2 protection violation
- SEC_ERR_STATUS_FUNC_2[13] – McASP3 protection violation
- SEC_ERR_STATUS_FUNC_2[16] – EDMA_TPTC1 protection violation
- SEC_ERR_STATUS_FUNC_2[17] – EDMA_TPCC protection violation
- SEC_ERR_STATUS_FUNC_2[20] – PRU-ICSS1 protection violation
- SEC_ERR_STATUS_FUNC_2[21] - PRU-ICSS2 protection violation
- SEC_ERR_STATUS_FUNC_2[22] – QSPI protection violation
- SEC_ERR_STATUS_FUNC_2[23] – EDMA_TPTC2 protection violation
-

- In debug mode:
  - SEC_ERR_STATUS_DEBUG_1[1] – L3 RAM protection violation
  - SEC_ERR_STATUS_DEBUG_1[2] – GPMC protection violation
  - SEC_ERR_STATUS_DEBUG_1[3] – EMIF protection violation
  - SEC_ERR_STATUS_DEBUG_1[4] – IVA protection violation
  - SEC_ERR_STATUS_DEBUG_1[5] – IPU protection violation
  - SEC_ERR_STATUS_DEBUG_1[6] – IVA SL2 protection violation
  - SEC_ERR_STATUS_DEBUG_1[8] - SYSTEM DMA protection violation
  - SEC_ERR_STATUS_DEBUG_1[10] – DSPDMA slave NIU protection violation
  - SEC_ERR_STATUS_DEBUG_1[13] – GPU protection violation
  - SEC_ERR_STATUS_DEBUG_1[14] – DSS protection violation

- SEC_ERR_STATUS_DEBUG_1[16] – L4_PER1 protection violation
- SEC_ERR_STATUS_DEBUG_1[17] – L4_CFG protection violation
- SEC_ERR_STATUS_DEBUG_1[18] – DEBUG subsystem protection violation
- SEC_ERR_STATUS_DEBUG_1[22] – L4_WKUP protection violation
- SEC_ERR_STATUS_DEBUG_1[23] - BB2D protection violation
- SEC_ERR_STATUS_DEBUG_1[26] – CT_TBR protection violation
- SEC_ERR_STATUS_DEBUG_1[28] – EVE1 protection violation
- SEC_ERR_STATUS_DEBUG_1[29] – EVE2 protection violation
- SEC_ERR_STATUS_DEBUG_1[30] – EVE3 protection violation
- SEC_ERR_STATUS_DEBUG_1[31] – EVE4 protection violation
- SEC_ERR_STATUS_DEBUG_2[0] – DSP1 protection violation
- SEC_ERR_STATUS_DEBUG_2[1] – DSP2 protection violation
- SEC_ERR_STATUS_DEBUG_2[2] – OCMC_RAM2 protection violation
- SEC_ERR_STATUS_DEBUG_2[3] – OCMC_RAM3 protection violation
- SEC_ERR_STATUS_DEBUG_2[4] – L4_PER2 protection violation
- SEC_ERR_STATUS_DEBUG_2[5] – L4_PER3 protection violation
- SEC_ERR_STATUS_DEBUG_2[6] - IPU2 protection violation
- SEC_ERR_STATUS_DEBUG_2[7] – PCIESS1 protection violation
- SEC_ERR_STATUS_DEBUG_2[8] - PCIESS2 protection violation
- SEC_ERR_STATUS_DEBUG_2[11] – McASP1 protection violation
- SEC_ERR_STATUS_DEBUG_2[12] – McASP2 protection violation
- SEC_ERR_STATUS_DEBUG_2[13] – McASP3 protection violation
- SEC_ERR_STATUS_DEBUG_2[16] – EDMA_TPTC1 protection violation
- SEC_ERR_STATUS_DEBUG_2[17] – EDMA_TPCC protection violation
- SEC_ERR_STATUS_DEBUG_2[20] – PRU-ICSS1 protection violation
- SEC_ERR_STATUS_DEBUG_2[21] - PRU-ICSS2 protection violation
- SEC_ERR_STATUS_DEBUG_2[22] – QSPI protection violation
- SEC_ERR_STATUS_DEBUG_2[23] – EDMA_TPTC2 protection violation
- For more information, see Chapter 18, *Control Module*.

14.2.3.7.3.5 L3_MAIN Firewall Default Configuration

Table 14-21 summarizes the configuration of the L3_MAIN firewalls.

Table 14-21. L3_MAIN Firewalls Default Configurations

Device/Region: 0						
Permission Type	**Reset Value**	**Reset Value**	**Reset Type**	**Run Time**	**Firewall Register (where j = 0)**	**Control Module Register**
ACCESS_ PERMISSION	All	0xFFF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[11:0]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF_LOC K_1[k] CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF_LOC K_2[j]
DEBUG_ PERMISSION	All	0xF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[15:12]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF_LOC K_1[k] CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_CONF_LOC K_2[j]
INITIATOR_ PERMISSION	All	0xFFF FFFFF	Tied	Configurable	MRM_PERMISSION_REGION_HIGH_j[31:0]	N/A

NOTE: For the values of k and j see Table 14-22, Table 14-13 and Table 14-14.

Table 14-22. Control Module Register – Factorization

Variable Value	Module Name	Regions
k		
[0]	GPMC	8
[3]	OCMC RAM1	16
[4]	DSS	8
[6]	GPU	1
[7]	IVAHD SL2IF	4
[8]	IVAHD CONFIG	1
[11]	EMIF	8
[12]	DEBUGSS	1
[13]	CT_TBR	1
[16]	EVE1 NOTE: EVE1 is not supported in this family of devices.	1
[17]	EVE2 NOTE: EVE2 is not supported in this family of devices.	1
[18]	EVE3 NOTE: EVE3 is not supported in this family of devices.	1
[19]	EVE4 NOTE: EVE4 is not supported in this family of devices.	1
[20]	PCIESS1	8
[21]	PCIESS2	8
[22]	IPU1	4
[23]	IPU2	4
[24]	VCP1 NOTE: VCP1 is not supported in this family of devices.	1
[25]	VCP2 NOTE: VCP2 is not supported in this family of devices.	1
[26]	McASP1	1
[27]	McASP2	1
[28]	McASP3	1
[31]	BB2D	1
j		
[0]	DSP1	1
[1]	DSP2	1
[2]	OCMC RAM2	16
[3]	OCMC RAM3	16
[6]	PRU-ICSS1	1
[7]	PRU-ICSS2	1
[8]	QSPI	1
[9]	EDMA TC	1
[10]	EDMA TPCC	1

14.2.3.8 L3_MAIN Interconnect Error Handling

Error logging is enabled in the L3_MAIN interconnect. The three major types of errors are:

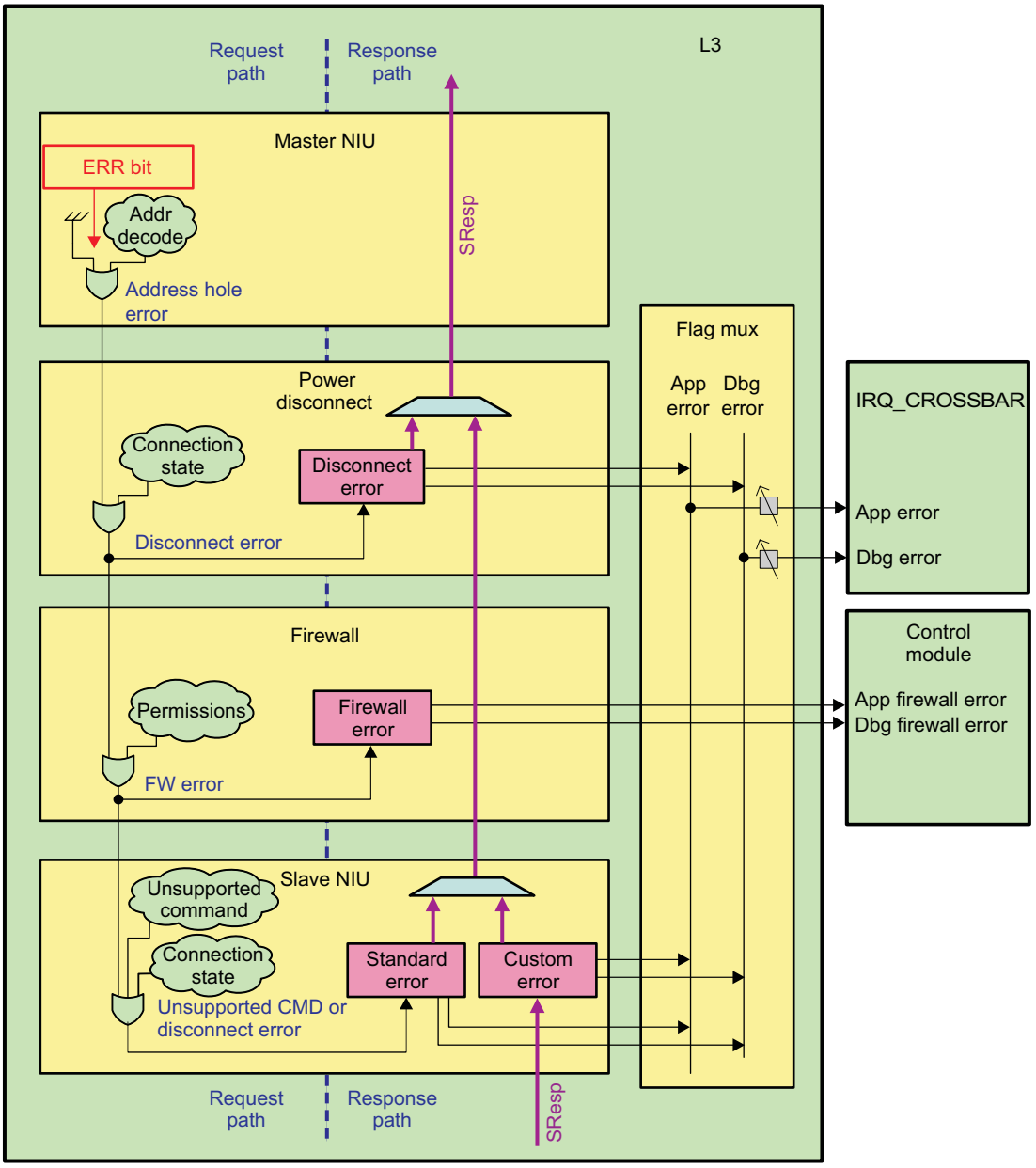
- Slave NIU errors
- Firewall errors (see Section 14.2.3.7.3.4, *L3_MAIN Firewall Error Logging*)

- Flag mux errors

14.2.3.8.1 Global Error-Routing Scheme

Figure 14-7 shows the L3_MAIN global error-routing scheme.

Figure 14-7. L3_MAIN Global Error-Routing Scheme



14.2.3.8.2 Slave NIU Error Logging

Error logging is implemented only at slave NIUs. Because the interconnect does not support master NIU error logging, an erroneous packet must be created and sent to one of the slave NIUs. The slave NIU that receives an erroneous packet is predictable but can change per master (see Table 14-23).

Table 14-23. L3_MAIN Connectivity and Holes Error Routing

Master	Connectivity and Holes Errors Logged Into Slave NIUs
All initiators except DSP1_CFG and DSP2_CFG	GPMC_TARG
DSP1_CFG	EVE1_TARG
DSP2_CFG	

The slave NIU can be configured to report standard errors (errors generated within the interconnect):

- Firewall error: Protection violation; this error indicates that a request was rejected by a firewall and is reported to the control module. For more information, see Section 14.2.3.7.3.4, *L3_MAIN Firewall Error Logging.*
- Address hole: This error reports an unknown address for a request. The address map is local to each master NIU; therefore, an address hole error is reported each time a master NIU requests an access to a slave NIU to which it is not logically connected, even if this address exists in the global L3_MAIN address map. This error is detected only once per burst.
- Unsupported commands: This error reports that the master NIU sent a command that cannot be processed, because the slave NIU cannot accept it and no conversion to another command is possible. This error is detected only once per burst.
- Report custom errors: Basically, when the slave answer is SResp = ERR
- Report severity level, for standard error and custom errors:
  - None: Error logging for this type of error is disabled.
  - Error: Error is logged for this type of error.
  - Fault: Error is logged and interrupt is generated for this type of error.
- Generate interrupt on 2 bits depending on the MReqDebug qualifier:
  - Application error - FAULT[0]
  - Debug error - FAULT[1]

  By default, all slave NIUs are configured with standard and custom error levels set to FAULT. The errors are reported on the two flag muxes (see Figure 14-7), depending on the access type, application or debug. For more information, see Section 14.2.3.8.3, *Flag Mux Error Logging*.

  The slave NIU power-disconnect component also has error logging enabled, because in this case the slave NIU is in a clock domain that is switched off and therefore cannot catch the error. By nature, this component can generate only standard errors. By default, it is configured with the error level set to FAULT.

  Wake up on demand: If an error packet reaches a slave NIU that is set with MDiscBehave = 1 (wake up on demand), then the active signal is asserted and L3 processes the error generation when the slave is awake. Although this is inefficient, it simplifies NIU implementation and should not be a problem because errors are supposed to occur only during software debug.

14.2.3.8.3 Flag Mux Error Logging

All fault signals are sent to a flag mux component. There are four important FLAGMUX registers:

- L3_FLAGMUX_MASK0: Masks application error sources
- L3_FLAGMUX_MASK1: Masks debug error sources
- L3_FLAGMUX_REGERR0: Checks which application error sources are active
- L3_FLAGMUX_REGERR1: Checks which debug error sources are active

The two L3_FLAGMUX_MASK registers mask bit 0 or bit 1 of the flag inputs, and the L3_FLAGMUX_REGERR registers read input errors. Each register is dedicated to reporting the bit corresponding to the register number.

Table 14-24 describes the mapping of the flags to the corresponding sources.

Table 14-24. Interconnect Flag Mapping

	Flag Mux Input	Source
CLK1_1 Flag Mux	1	DMM_P1
	2	DSP2 SDMA
	3	EVE2 NOTE: EVE2 is not supported in this family of devices.
	4	DMM_P2
	6	DSP1 SDMA
	7	EVE1 NOTE: EVE1 is not supported in this family of devices.
	8	EVE3 NOTE: EVE3 is not supported in this family of devices.
	9	EVE4 NOTE: EVE4 is not supported in this family of devices.
	10	DSS
	11	GPMC
	12	PCIE SS1
	13	IVA_CFG
	14	IVA_SL2IF
	15	L4_CFG
	16	L4_WKUP
	17	PCIESS2
	19	GPU
	20	IPU1
	21	IPU2
	22	EDMA TPCC
	23	EDMA TC1
	24	EDMA TC2
	25	VCP1 NOTE: VCP1 is not supported in this family of devices.
	26	L4_PER2_P3
	27	L4_PER3_P3
	28	MMU1
	29	PRU-ICSS1
	30	PRU-ICSS2
	31	VCP2 NOTE: VCP2 is not supported in this family of devices.
CLK1_2 Flag Mux	0	HOST_CLK1_1
	1	HOST_CLK1_2
	2	REPLICATOR_CLK1_TIMEOUT
	4	BB2D
	5	REPLICATOR_CLK1_TIMEOUT1
	6	L4_PER1_P3
	7	L4_PER1_P1
	8	L4_PER1_P2
	9	L4_PER2_P1

Table 14-24. Interconnect Flag Mapping (continued)

	Flag Mux Input	Source
	10	L4_PER2_P2
	11	L4_PER3_P1
	12	L4_PER3_P2
	13	McASP1
	14	McASP2
	15	McASP3
	16	MMU2
	17	OCMC_RAM1
	18	OCMC_RAM2
	19	OCMC_RAM3
	21	QSPI
	23	CLK1_TARG_PWR_DISC_CLK2
CLK2_1 Flag Mux	0	L3_INSTR
	1	DEBUGSS_CT_TBR
	2	HOST_CLK2_1
	3	REPLICATOR_CLK2_TIMEOUT

NOTE: Missing inputs in Table 14-24 are reserved. Writing inside the reserved spaces has no effect.

14.2.3.8.4 Severity Level of Standard and Custom Errors

The slave NIU registers are important for error logging.

- The L3_TARG_STDERRLOG_SVRTSTDLVL register shows the severity level for standard errors. According to the severity level, error logging is disabled, enabled with level ERROR, or enabled with level ERROR and flag FAULT.
- The L3_TARG_STDERRLOG_SVRTCUSTOMLVL register shows the severity level for custom errors.
- The L3_TARG_STDERRLOG_MAIN register (the main register for error-logging management) shows the validity of the logged information, standard or custom.
- The L3_TARG_STDERRLOG_HDR register stores packets in case of a standard error.
- The L3_TARG_STDERRLOG_MSTADDR register returns the MSTADDR field of the logged packet.
- The L3_TARG_STDERRLOG_SLVADDR register returns the SLVADDR field of the stored packet.
- The L3_TARG_STDERRLOG_INFO register saves the information field of the logged packet.

14.2.4 L3_MAIN Interconnect Programming Guide

14.2.4.1 L3 _MAIN Interconnect Low-Level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L3_MAIN interconnect module.

14.2.4.1.1 Global Initialization

14.2.4.1.1.1 Global Initialization of Surrounding Modules

This section identifies the requirements for initializing the surrounding modules when the L3_MAIN interconnect module is to be used for the first time after a device reset. The initialization of surrounding modules is based on the integration and environment of the L3_MAIN interconnect. For more information, see Section 14.2.2, *L3_MAIN Interconnect Integration* .

Table 14-25. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For information about the configuration of the PRCM module, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	For information about the configuration of the control module, see Chapter 18, *Control Module*.
Device INTCs	Device INTCs must be configured to enable the interrupt request generation. For more information see Chapter 17, *Interrupt Controllers*.
IRQ_CROSSBAR	IRQ_CROSSBAR configuration must be done to allow module IRQs to be mapped to certain device INTC line. For more information see Section 18.4.6.4, *IRQ_CROSSBAR Module Functional Description*, in Chapter 18, *Control Module*.

14.2.4.2 Operational Modes Configuration

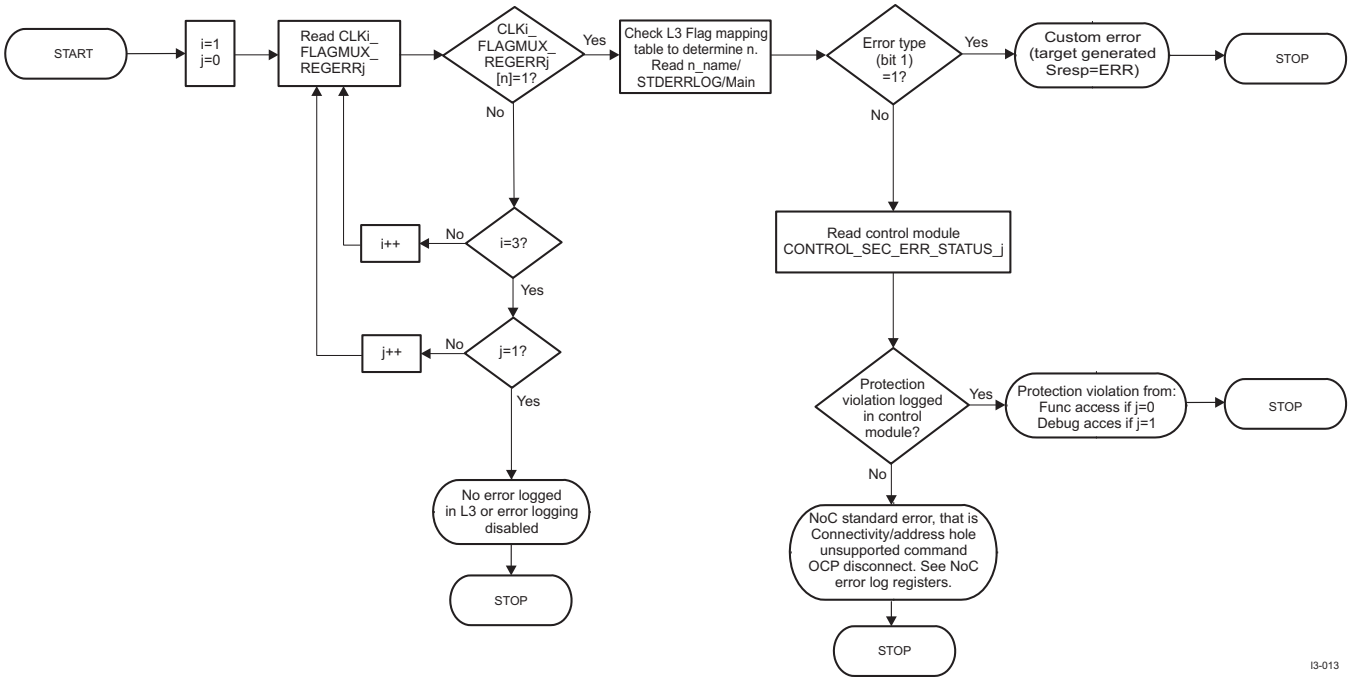
14.2.4.2.1 L3_MAIN Interconnect Error Analysis Mode

14.2.4.2.1.1 Main Sequence: L3_MAIN Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers. The number of registers to access depends on the error source.

Figure 14-8 shows the software sequence required in most cases.

Figure 14-8. Typical Error Analysis Sequence



NOTE: In case flag is set due to timeout flagmux, the user can check the status in CONTROL_SEC_ERR_STATUS for that timeout flagmux.

Table 14-26 lists the subprocess call summary for error analysis mode in the main sequence.

Table 14-26. Subprocess Call Summary for Main Sequence – Error Analysis Mode

Subprocess	Cross-Reference
L3 interconnect error analysis	See Section 14.2.4.2.1, *L3_MAIN Interconnect Error Analysis Mode.*
L3_MAIN interconnect protection violation error identification	See Section 14.2.4.2.1.1.2, *Subsequence: L3_MAIN Interconnect Protection Violation Error Identification.*
L3_MAIN interconnect unsupported command/address hole error identification	See Section 14.2.4.2.1.1.3, *Subsequence: L3_MAIN Interconnect Standard Error Identification.*
L3_MAIN interconnect reset FLAGMUX and module	See Section 14.2.4.2.1.1.4, *Subsequence: L3_MAIN Interconnect FLAGMUX Configuration.*

14.2.4.2.1.1.1 Subsequence: L3_MAIN Custom Error Identification

The procedure listed in Table 14-27 describes custom error identification.

Table 14-27. Custom Error Identification

Step	Register/Bit Field/Programming Model	Value
IF: Is custom error detected?	L3_TARG_STDERRLOG_MAIN[1] STDERRLOG_MAIN_ERRTYPE	=0x1
Read information field of the response packet.	L3_TARG_STDERRLOG_CUSTOMINFO_INFO[7:0] STDERRLOG_CUSTOMINFO_INFO	xxx
Read the address of the initiator that caused error.	L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR[10:0] STDERRLOG_CUSTOMINFO_MSTADDR	xxx
Read the type of operation (read/write).	L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE[1:0] STDERRLOG_CUSTOMINFO_OPCODE	xxx
ENDIF		

14.2.4.2.1.1.2 Subsequence: L3_MAIN Interconnect Protection Violation Error Identification

The procedure listed in Table 14-28 describes protection violation error identification and where it is logged in the control module registers. Two types of errors are logged: application errors and debug errors.

Table 14-28. L3_MAIN Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read the burst violation.	ERROR_LOG_k[23] 2D_BURST_VIOLATION	xxx
Read the initiator ID.	ERROR_LOG_k[3:0] ConnID	xxx
Read the command that caused the error.	ERROR_LOG_k[7] MCMD	xxx
Read the address of the request that caused the error.	ERROR_LOG_k[31:12] SLVOFS_LOGICAL	xxx
IF: Is it an application error?	L3_FLAGMUX_REGERR0 [31:0] REGERROR0	0x0
Read the status bits to see which module firewall has worked.	CONTROL.SEC_ERR_STATUS_FUNC_1[20:0]	xxx
Clear the status bits.	CONTROL.SEC_ERR_STATUS_FUNC_1[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN [31] STDERRLOG_MAIN_CLRLOG	0x0
ELSE IF	L3_FLAGMUX_REGERR1[7:0] REGERROR1	= 0x1
Read the status bits to see the module.	CONTROL.SEC_ERR_STATUS_DEBUG_1[20:0]	xxx
Clear the status bits.	CONTROL.SEC_ERR_STATUS_DEBUG_1[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
ENDIF		
Clear the burst violation.	ERROR_LOG_k[23] 2D_BURST_VIOLATION	0x0
Clear the error status.	ERROR_LOG_k[21:17] REGION_START_ERRLOG	0x00

14.2.4.2.1.1.3 Subsequence: L3_MAIN Interconnect Standard Error Identification

The procedure listed in Table 14-29 describes the identification of standard errors inside the L3_MAIN interconnect. The standard errors are: unsupported command, address hole, and disconnect.

Table 14-29. L3_MAIN Standard Error Identification

Step	Register/Bit Field/Programming Model	Value
IF: Is an error detected?	L3_TARG_STDERRLOG_MAIN[18] STDERRLOG_MAIN_ERRCNT	= 0x1
Read the corresponding flag.	L3_FLAGMUX_REGERR0[31:0] REGERROR0	xxx
Read the corresponding flag.	L3_FLAGMUX_REGERR1[31:0] REGERROR1	xxx
Localize the slave NIU that generated the error.	See Table 14-24.	
ELSE		
Clear the error log.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
Clear the severity error status.	L3_TARG_STDERRLOG_SVRTSTDLVL[1:0] STDERRLOG_SVRTSTDLVL_0	0x2
ENDIF		

14.2.4.2.1.1.4 Subsequence: L3_MAIN Interconnect FLAGMUX Configuration

The procedures listed in Table 14-30 and Table 14-31 give information about the configuration of FLAGMUX masks.

Table 14-30. FLAGMUX Configuration

Step	Register/Bit Field/Programming Model	Value
Set the FLAGMUX masks to mask an event.	L3_FLAGMUX_MASK031:0] MASK0 L3_FLAGMUX_MASK1[31:0] MASK1	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_REGERR0[31:0] REGERR0 L3_FLAGMUX_REGERR1[31:0] REGERR1	xxx
Clear the slave NIU error log and the FLAGMUX error.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_SVRTSTDLVL_0	0x1

Table 14-31. FLAGMUX Time-out1/2 Configuration (fro CLK1_1 and CLK1_2)

Step	Register/Bit Field/Programming Model	Value
Enable time-out for target.	L3_FLAGMUX_TIMEOUTx_MASK0[24:0] MASK0 (1)	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_TIMEOUTx_REGERR0[24:0] REGERR0 (1)	xxx

(1) x = 1 for CLK1_FLAGMUX_CLK1_1
x=2 for CLK1_FLAGMUX_CLK1_2
Bit fields are [24:0] for CLK1_FLAGMUX_CLK1_1, [20:0] for CLK1_FLAGMUX_CLK1_2

Table 14-32. FLAGMUX Time-out Configuration (for CLK2_1)

Step	Register/Bit Field/Programming Model	Value
Enable time-out for target.	L3_FLAGMUX_TIMEOUT_MASK0[1:0] MASK0	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_TIMEOUT_REGERR0[1:0] REGERR0	xxx

14.2.5 L3_MAIN Interconnect Register Manual

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

14.2.5.1 L3_MAIN Register Group Summary

The registers in the L3 interconnect are divided into eight groups:

- Firewall registers (see Table 14-34)
- HOST registers (see Table 14-62)
- TARG registers (see Table 14-98)
- FLAGMUX registers (see Section 14.2.5.1.4 thru Section 14.2.5.1.6)
- BW registers (see Table 14-201)
- STATCOLL registers (see Table 14-240)

14.2.5.1.1 L3_MAIN Firewall Registers Summary and Description

Table 14-33. L3_MAIN Firewall Instance Summary

Module Name	Base Address	Size
DEBUGSS_CT_TBR_FW	0x4A22 4000	4KiB
DSP1_SDMA_FW	0x4A17 1000	4KiB
DSP2_SDMA_FW	0x4A17 3000	4KiB
DSS_FW	0x4A21 C000	4KiB
EVE1_FW	0x4A15 1000	4KiB
EVE2_FW	0x4A15 3000	4KiB
EVE3_FW	0x4A15 5000	4KiB
EVE4_FW	0x4A15 7000	4KiB
GPMC_FW	0x4A21 0000	4KiB
GPU_FW	0x4A21 4000	4KiB
IPU1_FW	0x4A15 B000	4KiB
IVA_CONFIG_FW	0x4A22 0000	4KiB
IVA_SL2IF_FW	0x4A21 E000	4KiB
L3_INSTR_FW	0x4A22 6000	4KiB
OCMC_RAM1_FW	0x4A21 2000	4KiB
OCMC_RAM2_FW	0x4A20 E000	4KiB
OCMC_RAM3_FW	0x4A22 A000	4KiB
EMIF_OCP_FW	0x4A20 C000	4KiB
MA_MPU_NTTP_FW	0x4A20 A000	4KiB
PCIE1_FW	0x4A16 5000	4KiB
PRUSS1_FW	0x4A17 5000	4KiB
QSPI_FW	0x4A17 9000	4KiB
EDMA_TPCC_FW	0x4A16 1000	4KiB
TPTC_FW	0x4A16 3000	4KiB
IPU2_FW	0x4A21 8000	4KiB
PRUSS2_FW	0x4A17 7000	4KiB
PCIESS2_FW	0x4A15 9000	4KiB
BB2D_FW	0x4A21 A000	4KiB
MCASP1_FW	0x4A16 7000	4KiB
MCASP2_FW	0x4A16 9000	4KiB

Table 14-33. L3_MAIN Firewall Instance Summary (continued)

Module Name	Base Address	Size
MCASP3_FW	0x4A16 B000	4KiB
VCP1_FW	0x4A15 D000	4KiB
VCP2_FW	0x4A15 F000	4KiB

14.2.5.1.1.1 L3_MAIN Firewall Registers Summary

Table 14-34. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DEBUGSS_CT_TBR_FW L3_MAIN Physical Address	DSP1_SDMA_FW L3_MAIN Physical Address	DSP2_SDMA_FW L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A22 4000 + (0x10*k)	0x4A17 1000 + (0x10*k)	0x4A17 3000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A22 4004 + (0x10*k)	0x4A17 1004 + (0x10*k)	0x4A17 3004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A22 4040	0x4A17 1040	0x4A17 3040
START_REGION_i	RW	32	0x080+(0x10*i)	-	-	-
END_REGION_i	RW	32	0x084+(0x10*i)	-	-	-
MRM_PERMISSION_REGION_HIGH_j [2]	RW	32	0x08C+(0x10*j)	0x4A22 408C + (0x10*j)	0x4A17 108C + (0x10*j)	0x4A17 308C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j [2]	RW	32	0x088+(0x10*j)	0x4A22 4088 + (0x10*j)	0x4A17 1088 + (0x10*j)	0x4A17 3088 + (0x10*j)

(1) k = 0 for DEBUGSS_CT_TBR_FW
k = 0 for DSP1_SDMA_FW
k = 0 for DSP2_SDMA_FW

(2) j = 0 for DEBUGSS_CT_TBR_FW
j = 0 for DSP1_SDMA_FW
j = 0 for DSP2_SDMA_FW

Table 14-35. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_FW L3_MAIN Physical Address	EVE1_FW L3_MAIN Physical Address	EVE2_FW L3_MAIN Physical Address	GPMC_FW L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21 C000 + (0x10*k)	0x4A15 1000 + (0x10*k)	0x4A15 3000 + (0x10*k)	0x4A21 0000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21 C004 + (0x10*k)	0x4A15 1004 + (0x10*k)	0x4A15 3004 + (0x10*k)	0x4A21 0004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 C040	0x4A15 1040	0x4A15 3040	0x4A21 0040
START_REGION_i [2]	RW	32	0x080+(0x10*i)	0x4A21 C080 + (0x10*i)	-	-	0x4A21 0080 + (0x10*i)
END_REGION_i [2]	RW	32	0x084+(0x10*i)	0x4A21 C084 + (0x10*i)	-	-	0x4A21 0084 + (0x10*i)
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A21 C08C + (0x10*j)	0x4A15 108C + (0x10*j)	0x4A15 308C+ (0x10*j)	0x4A21 008C + (0x10*j)

(1) k = 0 for DSS_FW
k = 0 for EVE1_FW
k = 0 for EVE2_FW
k = 0 for GPMC_FW

(2) i = 1 to 7 for DSS_FW
i = 1 to 7 for GPMC_FW

(3) j = 0 to 7 for DSS_FW
j = 0 for EVE1_FW
j = 0 for EVE2_FW
j = 0 to 7 for GPMC_FW

Table 14-35. L3_MAIN Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSS_FW L3_MAIN Physical Address	EVE1_FW L3_MAIN Physical Address	EVE2_FW L3_MAIN Physical Address	GPMC_FW L3_MAIN Physical Address
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A21 C088 + (0x10*j)	0x4A15 1088 + (0x10*j)	0x4A15 3088+ (0x10*j)	0x4A21 0088 + (0x10*j)

Table 14-36. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPU_FW L3_MAIN Physical Address	EVE3_FW L3_MAIN Physical Address	IPU1_FW L3_MAIN Physical Address	EVE4_FW L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21 4000 + (0x10*k)	0x4A15 5000 + (0x10*k)	0x4A15 B000 + (0x10*k)	0x4A15 7000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21 4004 + (0x10*k)	0x4A15 5004 + (0x10*k)	0x4A15 B004 + (0x10*k)	0x4A15 7004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 4040	0x4A15 5040	0x4A15 B040	0x4A15 7040
START_REGION_i	RW	32	0x080+(0x10*i)	-	-	0x4A15 B080 + (0x10*i)	-
END_REGION_i	RW	32	0x084+(0x10*i)	-	-	0x4A15 B084 + (0x10*i)	-
MRM_PERMISSION_REGION_HIGH_j [2]	RW	32	0x08C+(0x10*j)	0x4A21 408C + (0x10*j)	0x4A15 508C + (0x10*j)	0x4A15 B08C + (0x10*j)	0x4A15 708C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j [2]	RW	32	0x088+(0x10*j)	0x4A21 4088 + (0x10*j)	0x4A15 5088 + (0x10*j)	0x4A15 B088 + (0x10*j)	0x4A15 7088 + (0x10*j)

(1) k = 0 for GPU_FW
k = 0 for EVE3_FW
k = 0 for IPU1_FW
k = 0 for EVE4_FW

(2) j = 0 for GPU_FW
j = 0 for EVE3_FW
j = 0 to 3 for IPU1_FW
j = 0 for EVE4_FW

Table 14-37. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVA_CONFIG_FW L3_MAIN Physical Address	IVA_SL2IF_FW L3_MAIN Physical Address	L3_INSTR_FW L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A22 0000 + (0x10*k)	0x4A21 E000 + (0x10*k)	0x4A22 6000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A22 0004 + (0x10*k)	0x4A21 E004 + (0x10*k)	0x4A22 6004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A22 0040	0x4A21 E040	0x4A22 6040
START_REGION_i [2]	RW	32	0x080+(0x10*i)	-	0x4A21 E080 + (0x10*i)	-
END_REGION_i [2]	RW	32	0x084+(0x10*i)	-	0x4A21 E084 + (0x10*i)	-
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A22 008C + (0x10*j)	0x4A21 E08C + (0x10*j)	0x4A22 608C + (0x10*j)

(1) k = 0 for IVA_CONFIG_FW
k = 0 for IVA_SL2IF_FW
k = 0 for L3_INSTR_FW

(2) i = 1 to 3 for IVA_SL2IF_FW

(3) j = 0 for IVA_CONFIG_FW
j = 0 to 3 for IVA_SL2IF_FW
j= 0 for L3_INSTR_FW

Table 14-37. L3_MAIN Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	IVA_CONFIG_FW L3_MAIN Physical Address	IVA_SL2IF_FW L3_MAIN Physical Address	L3_INSTR_FW L3_MAIN Physical Address
MRM_PERMISSION_REGION_LOW_j (3)	RW	32	0x088+(0x10*j)	0x4A22 0088 + (0x10*j)	0x4A21 E088 + (0x10*j)	0x4A22 6088 + (0x10*j)

Table 14-38. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	OCMC_RAM1_FW L3_MAIN Physical Address	OCMC_RAM2_FW L3_MAIN Physical Address	OCMC_RAM3_FW L3_MAIN Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A21 2000 + (0x10*k)	0x4A20 E000 + (0x10*k)	0x4A22 A000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A21 2004 + (0x10*k)	0x4A20 E004 + (0x10*k)	0x4A22 A004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 2040	0x4A20 E040	0x4A22 A040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A21 2080 + (0x10*i)	0x4A20 E080 + (0x10*i)	0x4A22 A080 + (0x10*i)
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A21 2084 + (0x10*i)	0x4A20 E084 + (0x10*i)	0x4A22 A084 + (0x10*i)
MRM_PERMISSION_REGION_HIGH_j (3)	RW	32	0x08C+(0x10*j)	0x4A21 208C + (0x10*j)	0x4A20 E08C + (0x10*j)	0x4A22 A08C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j (3)	RW	32	0x088+(0x10*j)	0x4A21 2088 + (0x10*j)	0x4A20 E088 + (0x10*j)	0x4A22 A088 + (0x10*j)

(1) k = 0 for OCMC_RAM1_FW
k = 0 for OCMC_RAM2_FW
k = 0 for OCMC_RAM3_FW

(2) i =1 to 15 for OCMC_RAM1_FW
i = 1 to 15 for OCMC_RAM2_FW
i = 1 to 15 for OCMC_RAM3_FW

(3) j = 0 to 15 for OCMC_RAM1_FW
j = 0 to 15 for OCMC_RAM2_FW
j = 0 to 15 for OCMC_RAM3_FW

Table 14-39. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF_OCP_FW L3_MAIN Physical Address	MA_MPU_NTTP_FW L3_MAIN Physical Address	PCIE1_FW L3_MAIN Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A20 C000 + (0x10*k)	0x4A20 A000 + (0x10*k)	0x4A16 5000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A20 C004 + (0x10*k)	0x4A20 A004 + (0x10*k)	0x4A16 5004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A20 C040	0x4A20 A040	0x4A16 5040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A20 C080 + (0x10*i)	0x4A20 A080 + (0x10*i)	0x4A16 5080 + (0x10*i)
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A20 C084 + (0x10*i)	0x4A20 A084 + (0x10*i)	0x4A16 5084 + (0x10*i)
MRM_PERMISSION_REGION_HIGH_j (3)	RW	32	0x08C+(0x10*j)	0x4A20 C08C + (0x10*j)	0x4A20 A08C + (0x10*j)	0x4A16 508C + (0x10*j)

(1) k = 0 to 1 for EMIF_OCP_FW
k = 0 to 1 for MA_MPU_NTTP_FW
k = 0 for PCIE1_FW

(2) i= 1 to 7 for EMIF_OCP_FW
i = 1 to 7 for MA_MPU_NTTP_FW
i = 1 to 7 for PCIE1_FW

(3) j = 0 to 7 for EMIF_OCP_FW
j = 0 to 7 for MA_MPU_NTTP_FW
j = 0 to 7 for PCIE1_FW

Table 14-39. L3_MAIN Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF_OCP_FW L3_MAIN Physical Address	MA_MPU_NTTP_FW L3_MAIN Physical Address	PCIE1_FW L3_MAIN Physical Address
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A20 C088 + (0x10*j)	0x4A20 A088 + (0x10*j)	0x4A16 5088 + (0x10*j)

Table 14-40. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRUSS1_FW L3_MAIN Physical Address	QSPI_FW L3_MAIN Physical Address	EDMA_TPCC_FW L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A17 5000 + (0x10*k)	0x4A17 9000 + (0x10*k)	0x4A16 1000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A17 5004 + (0x10*k)	0x4A17 9004 + (0x10*k)	0x4A16 1004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A17 5040	0x4A17 9040	0x4A16 1040
START_REGION_i	RW	32	0x080+(0x10*i)	-	-	-
END_REGION_i	RW	32	0x084+(0x10*i)	-	-	-
MRM_PERMISSION_REGION_HIGH_j [2]	RW	32	0x08C+(0x10*j)	0x4A17 508C + (0x10*j)	0x4A17 908C + (0x10*j)	0x4A16 108C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j [2]	RW	32	0x088+(0x10*j)	0x4A17 5088 + (0x10*j)	0x4A17 9088 + (0x10*j)	0x4A16 1088 + (0x10*j)

(1) k = 0 for PRUSS1_FW
k = 0 for QSPI_FW
k = 0 for EDMA_TPCC_FW

(2) j = 0 for PRUSS1_FW
j = 0 for QSPI_FW
j = 0 for EDMA_TPCC_FW

Table 14-41. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TPTC_FW L3_MAIN Physical Address	VCP1_FW L3_MAIN Physical Address	VCP2_FW L3_MAIN Physical Address
ERROR_LOG_k	RW	32	0x000+(0x10*k)	0x4A16 3000+(0x10*k)	0x4A15 D000+(0x10*k)	0x4A15 F000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k	RO	32	0x004+(0x10*k)	0x4A16 3004+(0x10*k)	0x4A15 D004+(0x10*k)	0x4A15 F004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A16 3040	0x4A15 D040	0x4A15 F040
START_REGION_i [1]	RW	32	0x080+(0x10*i)	0x4A16 3080+(0x10*i)	-	-
END_REGION_i [1]	RW	32	0x084+(0x10*i)	0x4A16 3084+(0x10*i)	-	-
MRM_PERMISSION_REGION_HIGH_j	RW	32	0x08C+(0x10*j)	0x4A16 308C+(0x10*j)	0x4A15 D08C+(0x10*j)	0x4A15 F08C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j	RW	32	0x088+(0x10*j)	0x4A16 3088+(0x10*j)	0x4A15 D088+(0x10*j)	0x4A15 F088+(0x10*j)

(1) i =1 for TPTC_FW

Table 14-42. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IPU2_FW L3_MAIN Physical Address	PRUSS2_FW L3_MAIN Physical Address	PCIESS2_FW L3_MAIN Physical Address	BB2D_FW L3_MAIN Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A21 8000+(0x10*k)	0x4A17 7000+(0x10*k)	0x4A15 9000+(0x10*k)	0x4A21 A000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A21 8004+(0x10*k)	0x4A17 7004+(0x10*k)	0x4A15 9004+(0x10*k)	0x4A21 A004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 8040	0x4A17 7040	0x4A15 9040	0x4A21 A040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A21 8080+(0x10*i)	-	0x4A15 9080+(0x10*i)	-
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A21 8084+(0x10*i)	-	0x4A15 9084+(0x10*i)	-
MRM_PERMISSION_REGION_HIGH_j (3)	RW	32	0x08C+(0x10*j)	0x4A21 808C+(0x10*j)	0x4A17 708C+(0x10*j)	0x4A15 908C+(0x10*i)	0x4A21 A08C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (3)	RW	32	0x088+(0x10*j)	0x4A21 8088+(0x10*j)	0x4A17 7088+(0x10*j)	0x4A15 9088+(0x10*i)	0x4A21 A088+(0x10*j)

(1) k = 0 for IPU2_FW
k = 0 for PRUSS2_FW
k = 0 for PCIESS2_FW
k = 0 for BB2D_FW

(2) i = 1 to 3 for IPU2_FW
i = 1 to 7 for PCIESS2_FW

(3) j = 0 to 3 for IPU2_FW
j = 0 for PRUSS2_FW
j = 0 to 7 for PCIESS2_FW
j = 0 for BB2D_FW

Table 14-43. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MCASP1_FW L3_MAIN Physical Address	MCASP2_FW L3_MAIN Physical Address	MCASP3_FW L3_MAIN Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A16 7000+(0x10*k)	0x4A16 9000+(0x10*k)	0x4A16 B000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A16 7004+(0x10*k)	0x4A16 9004+(0x10*k)	0x4A16 B004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A16 7040	0x4A16 9040	0x4A16 B040
START_REGION_i	RW	32	0x080+(0x10*i)	-	-	-
END_REGION_i	RW	32	0x084+(0x10*i)	-	-	-
MRM_PERMISSION_REGION_HIGH_j (2)	RW	32	0x08C+(0x10*j)	0x4A16 708C+(0x10*j)	0x4A16 908C+(0x10*j)	0x4A16 B08C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (2)	RW	32	0x088+(0x10*j)	0x4A16 7088+(0x10*j)	0x4A16 9088+(0x10*j)	0x4A16 B088+(0x10*j)

(1) k = 0 for MCASP1_FW
k = 0 for MCASP2_FW
k = 0 for MCASP3_FW

(2) j = 0 for MCASP1_FW
j = 0 for MCASP2_FW
j = 0 for MCASP3_FW

14.2.5.1.1.2 L3_MAIN Firewall Registers Description

NOTE: Hardware reset values can be modified by exported values from the control module at reset.

Table 14-44. ERROR_LOG_k

Address Offset	0x0000 0000+(0x10*k)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	See Table 14-34 to Table 14-43.	**Instance**	See Table 14-34 to Table 14-43.
Description	Error log register for port k		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BLK_BURST_VIOLATION	RESERVED	REGION_START_ERRLOG						REGION_END_ERRLOG				REQINFO_ERRLOG											

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0s.	R	0x00
23	BLK_BURST_VIOLATION	Read 0x1: 2D burst not allowed or exceeding allowed size Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0
22	RESERVED	Reads return 0s.	R	0
21:17	REGION_START_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
16:12	REGION_END_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
11:0	REQINFO_ERRLOG	Read: Error in reqinfo vector mapped as follows: [11: 8] ConnID [3:0] [7] MCMD [0] [6:4] Reserved [3] MReqDebug [2] Reserved [1] MReqSupervisor [0] MReqType Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x000

Table 14-45. Register Call Summary for Register ERROR_LOG_k

L3_MAIN Interconnect

- L3_MAIN Firewall Functionality: [0] [1] [2] [3] [4]
- L3_MAIN Interconnect Error Analysis Mode: [5] [6] [7] [8] [9] [10]
- L3_MAIN Firewall Registers Summary and Description: [11] [12] [13] [14] [15] [16] [17] [19] [20] [22] [23] [24] [25] [26]

Table 14-46. LOGICAL_ADDR_ERRLOG_k

Address Offset	0x0000 0004+(0x10*k)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	See Table 14-34 to Table 14-43.	**Instance**	See Table 14-34 to Table 14-43.
Description	Logical Physical Address Error log register for port k		
Type	RO		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLVOFS_LOGICAL																															

Bits	Field Name	Description	Type	Reset
31[(1)]:0	SLVOFS_LOGICAL	Address generated by the Initiator before being translated	R	0x00000

(1) * = Size of the target

Table 14-47. Register Call Summary for Register LOGICAL_ADDR_ERRLOG_k

L3_MAIN Interconnect
- L3_MAIN Firewall Registers Summary and Description: [0] [1] [2] [3] [4] [5] [6] [8] [9] [11] [12] [13] [14] [15]

Table 14-48. REGUPDATE_CONTROL

Address Offset	0x0000 0040		
Physical Address	See Table 14-34 to Table 14-43.	**Instance**	See Table 14-34 to Table 14-43.
Description	Register update control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FW_ADDR_SPACE_MSB				RESERVED														FW_LOAD_REQ	BUSY_REQ

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads return 0s.	R	0x0000 0000
19:16	FW_ADDR_SPACE_MSB	Address space size	R	0x2
15:2	RESERVED	Reserved	R	0x0000 0000
1	FW_LOAD_REQ	Writing '1' to this bit causes the bit to self-clear and triggers the reload of L3 firewall default values. This bit will subsequently self-set when the reload procedure is complete. Writing '0' has no effect.	RW W1toClr	0x1
0	BUSY_REQ	Busy request 0x0: Allow transactions to reach the slave NIU (resume) 0x1: No transaction can reach the slave NIU (suspend)	RW	0x0

Table 14-49. Register Call Summary for Register REGUPDATE_CONTROL

L3_MAIN Interconnect
- L3_MAIN Firewall Reset: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- L3_MAIN Firewall Functionality: [10] [11]
- L3_MAIN Firewall Registers Summary and Description: [12] [13] [14] [15] [16] [17] [18] [20] [21] [23]

Table 14-50. START_REGION_i

Address Offset	0x0000 0080+(0x10*i)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	0x4A21 C080 + (0x10*i) 0x4A21 0080 + (0x10*i) 0x4A15 B080 + (0x10*i) 0x4A21 E080 + (0x10*i) 0x4A21 2080 + (0x10*i) 0x4A20 E080 + (0x10*i) 0x4A22 A080 + (0x10*i) 0x4A20 C080 + (0x10*i) 0x4A20 A080 + (0x10*i) 0x4A16 5080 + (0x10*i) 0x4A16 3080+(0x10*i) 0x4A21 8080+(0x10*i) 0x4A15 9080+(0x10*i)	**Instance**	DSS_FW GPMC_FW IPU1_FW IVA_SL2IF_FW OCMC_RAM1_FW OCMC_RAM2_FW OCMC_RAM3_FW EMIF_OCP_FW MA_MPU_NTTP_FW PCIE1_FW TPTC_FW IPU2_FW PCIESS2_FW
Description	Start physical address of region i		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_REGION																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:10	START_REGION	Physical target start address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:10]. See Table 14-52. Each of the LSbits is assumed to be 0.The programmed address is included in the region i boundary.	RW	0x00000
9:0	RESERVED	Reads return 0s.	R	0x0000

Table 14-51. Register Call Summary for Register START_REGION_i

L3_MAIN Interconnect

- L3_MAIN Firewall Functionality: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- L3_MAIN Firewall Registers Summary and Description: [10] [11] [12] [13] [14] [15] [16] [18] [19] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34]

Table 14-52. Size of START_REGION_i[] START_REGION Bit Field

Firewall	Bit Field
DSS_FW	START_REGION_i[22:12] START_REGION
GPMC_FW	START_REGION_i[30:12] START_REGION
IPU1_FW	START_REGION_i[22:12] START_REGION
IVA_SL2IF_FW	START_REGION_i[17:12] START_REGION
OCMC_RAM1_FW	START_REGION_i[18:12] START_REGION
OCMC_RAM2_FW	START_REGION_i[19:12] START_REGION
OCMC_RAM3_FW	START_REGION_i[19:12] START_REGION
EMIF_OCP_FW	START_REGION_i[31:10] START_REGION
MA_MPU_NTTP_FW	START_REGION_i[31:10] START_REGION
PCIE1_FW	START_REGION_i[27:12] START_REGION
TPTC_FW	START_REGION_i[19:12] START_REGION
IPU2_FW	START_REGION_i[22:12] START_REGION
PCIESS2_FW	START_REGION_i[27:12] START_REGION

Table 14-53. END_REGION_i

Address Offset	0x0000 0084+(0x10*i)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	0x4A21 C084 + (0x10*i) 0x4A21 0084 + (0x10*i) 0x4A15 B084 + (0x10*i) 0x4A21 E084 + (0x10*i) 0x4A21 2084 + (0x10*i) 0x4A20 E084 + (0x10*i) 0x4A22 A084 + (0x10*i) 0x4A20 C084 + (0x10*i) 0x4A20 A084 + (0x10*i) 0x4A16 5084 + (0x10*i) 0x4A16 3084+(0x10*i) 0x4A21 8084+(0x10*i) 0x4A15 9084+(0x10*i)	**Instance**	DSS_FW GPMC_FW IPU1_FW IVA_SL2IF_FW OCMC_RAM1_FW OCMC_RAM2_FW OCMC_RAM3_FW EMIF_OCP_FW MA_MPU_NTTP_FW PCIE1_FW TPTC_FW IPU2_FW PCIESS2_FW
Description	End physical address of region i		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_REGION																						RESERVED								END_REGION_i_ENABLE_CORE1	END_REGION_i_ENABLE_CORE0

Bits	Field Name	Description	Type	Reset
31:10	END_REGION	Physical target end address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:10]. See Table 14-55. Each of the LSbits is assumed to be 1.The programmed address is included in the region i boundary.	RW	0x00000
9:2	RESERVED	Reads return 0s.	R	0x0000
1	END_REGION_i_ENABLE_CORE1	Enable this region for port 1[(1)].	RW	0x0
0	END_REGION_i_ENABLE_CORE0	Enable this region for port 0.	RW	0x0

(1) Only for multiport firewalls

Table 14-54. Register Call Summary for Register END_REGION_i

L3_MAIN Interconnect

- L3_MAIN Firewall Functionality: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- L3_MAIN Firewall Registers Summary and Description: [22] [23] [24] [25] [26] [27] [28] [30] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46]

Table 14-55. Size of END_REGION_i[] END_REGION Bit Field

Firewall	Bit Field
DSS_FW	END_REGION_i[22:12] END_REGION
GPMC_FW	END_REGION_i[30:12] END_REGION
IPU1_FW	END_REGION_i[22:12] END_REGION
IVA_SL2IF_FW	END_REGION_i[17:12] END_REGION

Table 14-55. Size of END_REGION_i[] END_REGION Bit Field (continued)

Firewall	Bit Field
OCMC_RAM1_FW	END_REGION_i[18:12] END_REGION
OCMC_RAM2_FW	END_REGION_i[19:12] END_REGION
OCMC_RAM3_FW	END_REGION_i[19:12] END_REGION
EMIF_OCP_FW	END_REGION_i[31:10] END_REGION
MA_MPU_NTTP_FW	END_REGION_i[31:10] END_REGION
PCIE1_FW	END_REGION_i[27:12] END_REGION
TPTC_FW	END_REGION_i[19:12] END_REGION
IPU2_FW	END_REGION_i[22:12] START_REGION
PCIESS2_FW	END_REGION_i[27:12] START_REGION

Table 14-56. MRM_PERMISSION_REGION_HIGH_j

Address Offset	0x0000 008C+(0x10*i)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	See Table 14-34 to Table 14-43.	**Instance**	See Table 14-34 to Table 14-43.
Description	Region j Permission High		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W15	R15	W14	R14	W13	R13	W12	R12	W11	R11	W10	R10	W9	R9	W8	R8	W7	R7	W6	R6	W5	R5	W4	R4	W3	R3	W2	R2	W1	R1	W0	R0

Bits	Field Name	Description	Type	Reset
31	W15	Master NIU ConnID = 115 write permission	RW	0x1
30	R15	Master NIU ConnID = 115 read permission	RW	0x1
29	W14	Master NIU ConnID = 14 write permission	RW	0x1
28	R14	Master NIU ConnID = 14 read permission	RW	0x1
27	W13	Master NIU ConnID = 13 write permission	RW	0x1
26	R13	Master NIU ConnID = 13 read permission	RW	0x1
25	W12	Master NIU ConnID = 12 write permission	RW	0x1
24	R12	Master NIU ConnID = 12 read permission	RW	0x1
23	W11	Master NIU ConnID = 11 write permission	RW	0x1
22	R11	Master NIU ConnID = 11 read permission	RW	0x1
21	W10	Master NIU ConnID = 10 write permission	RW	0x1
20	R10	Master NIU ConnID = 10 read permission	RW	0x1
19	W9	Master NIU ConnID = 9 write permission	RW	0x1
18	R9	Master NIU ConnID = 9 read permission	RW	0x1
17	W8	Master NIU ConnID = 8 write permission	RW	0x1
16	R8	Master NIU ConnID = 8 read permission	RW	0x1
15	W7	Master NIU ConnID = 7 write permission	RW	0x1
14	R7	Master NIU ConnID = 7 read permission	RW	0x1
13	W6	Master NIU ConnID = 6 write permission	RW	0x1
12	R6	Master NIU ConnID = 6 read permission	RW	0x1
11	W5	Master NIU ConnID = 5 write permission	RW	0x1
10	R5	Master NIU ConnID = 5 read permission	RW	0x1
9	W4	Master NIU ConnID = 4 write permission	RW	0x1
8	R4	Master NIU ConnID = 4 read permission	RW	0x1
7	W3	Master NIU ConnID = 3 write permission	RW	0x1
6	R3	Master NIU ConnID = 3 read permission	RW	0x1

Bits	Field Name	Description	Type	Reset
5	W2	Master NIU ConnID = 2 write permission	RW	0x1
4	R2	Master NIU ConnID = 2 read permission	RW	0x1
3	W1	Master NIU ConnID = 1 write permission	RW	0x1
2	R1	Master NIU ConnID = 1 read permission	RW	0x1
1	W0	Master NIU ConnID = 0 write permission	RW	0x1
0	R0	Master NIU ConnID = 0 read permission	RW	0x1

Table 14-57. Register Call Summary for Register MRM_PERMISSION_REGION_HIGH_j

L3_MAIN Interconnect
- L3_MAIN Firewall Functionality: [0] [1] [2] [3] [4] [5]
- L3_MAIN Firewall Registers Summary and Description: [6] [7] [8] [9] [10] [11] [12] [14] [15] [17]

Table 14-58. MRM_PERMISSION_REGION_LOW_j

Address Offset	0x0000 0088+(0x10*i)	**Index**	See Table 14-34 to Table 14-43.
Physical Address	See Table 14-34 to Table 14-43.	**Instance**	See Table 14-34 to Table 14-43.
Description	Region j Permission Low		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PUB_PRV_DEBUG	PUB_USR_DEBUG	RESERVED		PUB_PRV_WRITE	PUB_PRV_READ	PUB_PRV_EXE	PUB_USR_WRITE	PUB_USR_READ	PUB_USR_EXE	RESERVED					

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	RESERVED	R	See Table 14-60.
15	PUB_PRV_DEBUG	Public Privilege Debug Allowed	RW	See Table 14-60.
14	PUB_USR_DEBUG	Public User Debug Allowed	RW	See Table 14-60.
13:12	RESERVED	RESERVED	R	See Table 14-60.
11	PUB_PRV_WRITE	Public Privilege Write Allowed	RW	See Table 14-60.
10	PUB_PRV_READ	Public Privilege Read Allowed	RW	See Table 14-60.
9	PUB_PRV_EXE	Public Privilege Exe Allowed	RW	See Table 14-60.
8	PUB_USR_WRITE	Public User Write Access Allowed	RW	See Table 14-60.
7	PUB_USR_READ	Public User Read Access Allowed	RW	See Table 14-60.
6	PUB_USR_EXE	Public User Exe Access Allowed	RW	See Table 14-60.
5:0	RESERVED	RESERVED	R	See Table 14-60.

Table 14-59. Register Call Summary for Register MRM_PERMISSION_REGION_LOW_j

L3_MAIN Interconnect
- L3_MAIN Firewall Reset: [0] [1]
- L3_MAIN Firewall Functionality: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- L3_MAIN Firewall Registers Summary and Description: [15] [16] [17] [18] [19] [20] [21] [23] [24] [26]

Table 14-60. Reset Value for MRM_PERMISSION_REGION_LOW_j

Region	Reset Value
Region j = 0 (except EMIF firewall)	0xFFFF0000
Region j = 0 (for EMIF firewall)	0xFFFFFFFF
Region j 0 (for all firewalls)	0xFFFFFFFF

14.2.5.1.2 L3_MAIN Host Register Summary and Description

Table 14-61. HOST Instance Summary

Module Name	Base Address	Size
CLK1_HOST_CLK1_1	0x4400 0000	8MiB
CLK1_HOST_CLK1_2	0x4480 0000	8MiB
CLK2_HOST_CLK2_1	0x4500 0000	8MiB

14.2.5.1.2.1 L3_MAIN HOST Register Summary

Table 14-62. HOST Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_HOST_CLK1_1 L3_MAIN Physical Address	CLK1_HOST_CLK1_2 L3_MAIN Physical Address	CLK2_HOST_CLK2_1 L3_MAIN Physical Address
L3_HOST_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0000	0x4480 0000	0x4500 0000
L3_HOST_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0004	0x4480 0004	0x4500 0004
L3_HOST_STDHOSTHDR_MAINCTLREG	R	32	0x0000 0008	0x4400 0008	0x4480 0008	0x4500 0008
L3_HOST_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0040	0x4480 0040	0x4500 0040
L3_HOST_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0044	0x4480 0044	0x4500 0044
L3_HOST_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0048	0x4480 0048	0x4500 0048
L3_HOST_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 004C	0x4480 004C	0x4500 004C
L3_HOST_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0050	0x4480 0050	0x4500 0050
L3_HOST_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0054	0x4480 0054	0x4500 0054
L3_HOST_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0058	0x4480 0058	0x4500 0058
L3_HOST_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 005C	0x4480 005C	0x4500 005C
L3_HOST_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0060	0x4480 0060	0x4500 0060
L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0064	0x4400 0064	0x4480 0064	0x4500 0064
L3_HOST_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0068	0x4400 0068	0x4480 0068	0x4500 0068
L3_HOST_STDERRLOG_CUSTOMINFO_WR	R	32	0x0000 006C	0x4400 006C	0x4480 006C	0x4500 006C
L3_HOST_STDERRLOG_CUSTOMINFO_ADDR	R	32	0x0000 0070	0x4400 0070	0x4480 0070	0x4500 0070

Table 14-62. HOST Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_HOST_CLK1_1 L3_MAIN Physical Address	CLK1_HOST_CLK1_2 L3_MAIN Physical Address	CLK2_HOST_CLK2_1 L3_MAIN Physical Address
L3_HOST_STDERRLOG_CUSTOMINFO_DECERR	R	32	0x0000 0074	0x4400 0074	0x4480 0074	0x4500 0074

14.2.5.1.2.2 L3_MAIN HOST Register Description

Table 14-63. L3_HOST_STDHOSTHDR_COREREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0000 0x4480 0000 0x4500 0000	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x1A.	R	0x1A
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-64. Register Call Summary for Register L3_HOST_STDHOSTHDR_COREREG

L3_MAIN Interconnect
- L3_MAIN Host Register Summary and Description: [0]

Table 14-65. L3_HOST_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0004 0x4480 0004 0x4500 0004	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-66. Register Call Summary for Register L3_HOST_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-67. L3_HOST_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0008 0x4480 0008 0x4500 0008	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													STDHOSTHDR_MAINCTLREG_FLT	RESERVED	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Fault is asserted when the Fault Control register field indicates a Fault, and de-asserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1:0	RESERVED		R	0x0

Table 14-68. Register Call Summary for Register L3_HOST_STDHOSTHDR_MAINCTLREG

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-69. L3_HOST_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 14-62.		
Physical Address	0x4400 0040 0x4480 0040 0x4500 0040	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTSTDLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-70. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTSTDLVL

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-71. L3_HOST_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 14-62.		
Physical Address	0x4400 0044 0x4480 0044 0x4500 0044	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTCUSTOMLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-72. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTCUSTOMLVL

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-73. L3_HOST_STDERRLOG_MAIN

Address Offset	See Table 14-62.		
Physical Address	0x4400 0048 0x4480 0048 0x4500 0048	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears "Error Logging Valid" bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED		R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED		R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

Table 14-74. Register Call Summary for Register L3_HOST_STDERRLOG_MAIN

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [1]

Table 14-75. L3_HOST_STDERRLOG_HDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 004C 0x4480 004C 0x4500 004C	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11	10 9 8	7 6	5 4	3 2 1 0
RESERVED	STDERRLOG_HDR_LEN1	RESERVED	STDERRLOG_HDR_STOPOFSWRPSZ	STDERRLOG_HDR_ERR	RESERVED	STDERRLOG_HDR_PRESSURE	RESERVED	STDERRLOG_HDR_OPCODE

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x00
27:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED		R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:8	RESERVED		R	0x0
7:6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED		R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 14-76. Register Call Summary for Register L3_HOST_STDERRLOG_HDR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-77. L3_HOST_STDERRLOG_MSTADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0050 0x4480 0050 0x4500 0050	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-78. Register Call Summary for Register L3_HOST_STDERRLOG_MSTADDR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-79. L3_HOST_STDERRLOG_SLVADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0054 0x4480 0054 0x4500 0054	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SLVADDR	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-80. Register Call Summary for Register L3_HOST_STDERRLOG_SLVADDR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-81. L3_HOST_STDERRLOG_INFO

Address Offset	See Table 14-62.		
Physical Address	0x4400 0058 0x4480 0058 0x4500 0058	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-82. Register Call Summary for Register L3_HOST_STDERRLOG_INFO

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-83. L3_HOST_STDERRLOG_SLVOFSLSB

Address Offset	See Table 14-62.		
Physical Address	0x4400 005C 0x4480 005C 0x4500 005C	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the "slave offset" field, concatenated with "start offset" field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 14-84. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSLSB

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-85. L3_HOST_STDERRLOG_SLVOFSMSB

Address Offset	See Table 14-62.		
Physical Address	0x4400 0060 0x4480 0060 0x4500 0060	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the "slave offset" field of the logged packet (according to NTTP packet format, this register field may exceed the actual "slave offset" size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 14-86. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSMSB

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-87. L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0064 0x4480 0064 0x4500 0064	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_CUSTOMINFO_MSTADDR	Type: Status. Reset value: X.	R	0x00

Table 14-88. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-89. L3_HOST_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 14-62.		
Physical Address	0x4400 0068 0x4480 0068 0x4500 0068	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Type: Status. Reset value: X.	R	0x00

Table 14-90. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_INFO

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-91. L3_HOST_STDERRLOG_CUSTOMINFO_WR

Address Offset	See Table 14-62.		
Physical Address	0x4400 006C 0x4480 006C 0x4500 006C	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_CUSTOMINFO_WR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_WR	Type: Status. Reset value: X.	R	0

Table 14-92. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_WR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-93. L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0070 0x4480 0070 0x4500 0070	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											STDERRLOG_CUSTOMINFO_ADDR																					

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:0	STDERRLOG_CUSTOMINFO_ADDR	Type: Status. Reset value: X.	R	0x000000

Table 14-94. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

Table 14-95. L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0074 0x4480 0074 0x4500 0074	**Instance**	CLK1_HOST_CLK1_1 CLK1_HOST_CLK1_2 CLK2_HOST_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_CUSTOMINFO_DECERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_DECERR	Type: Status. Reset value: X.	R	0

Table 14-96. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

L3_MAIN Interconnect

- L3_MAIN Host Register Summary and Description: [0]

14.2.5.1.3 L3_MAIN TARG Register Summary and Description

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-97. L3_MAIN TARG Instance Summary

Module Name	Base Address	Size
GPMC_TARG	0x4400 0100	4KiB
DMM_P1_TARG	0x4400 0200	4KiB
DSP1_SDMA_TARG	0x4400 0300	4KiB
L4_CFG_TARG	0x4400 0500	4KiB
DSP2_SDMA_TARG	0x4400 0600	4KiB
VCP1_TARG	0x4400 0700	4KiB
VCP2_TARG	0x4400 0800	4KiB
BB2D_TARG	0x4400 0900	4KiB
IPU2_TARG	0x4400 1100	4KiB
PRUSS2_TARG	0x4400 1500	4KiB
MCASP1_TARG	0x4400 2F00	4KiB

Table 14-97. L3_MAIN TARG Instance Summary (continued)

Module Name	Base Address	Size
MCASP2_TARG	0x4400 3000	4KiB
MCASP3_TARG	0x4400 3100	4KiB
PCIE2_TARG	0x4400 3800	4KiB
EVE1_TARG	0x4400 0A00	4KiB
EVE2_TARG	0x4400 0B00	4KiB
EVE3_TARG	0x4400 0C00	4KiB
EVE4_TARG	0x4400 0D00	4KiB
L4_PER3_P3_TARG	0x4400 0E00	4KiB
OCMC_RAM1_TARG	0x4400 0F00	4KiB
IPU1_TARG	0x4400 1000	4KiB
GPU_TARG	0x4400 1200	4KiB
DMM_P2_TARG	0x4400 1300	4KiB
PRUSS1_TARG	0x4400 1400	4KiB
IVA_CONFIG_TARG	0x4400 1600	4KiB
OCMC_RAM2_TARG	0x4400 1700	4KiB
IVA_SL2IF_TARG	0x4400 1800	4KiB
OCMC_RAM3_TARG	0x4400 1900	4KiB
L4_PER1_P1_TARG	0x4400 1C00	4KiB
L4_WKUP_TARG	0x4400 1D00	4KiB
L4_PER1_P2_TARG	0x4400 1F00	4KiB
TPCC_TARG	0x4400 2000	4KiB
L4_PER1_P3_TARG	0x4400 2100	4KiB
MMU1_TARG	0x4400 2200	4KiB
L4_PER2_P1_TARG	0x4400 2300	4KiB
L4_PER2_P2_TARG	0x4400 2400	4KiB
L4_PER2_P3_TARG	0x4400 2500	4KiB
L4_PER3_P1_TARG	0x4400 2600	4KiB
L4_PER3_P2_TARG	0x4400 2700	4KiB
MMU2_TARG	0x4400 2800	4KiB
DSS_TARG	0x4400 2900	4KiB
TPTC2_TARG	0x4400 2B00	4KiB
TPTC1_TARG	0x4400 2E00	4KiB
PCIE1_TARG	0x4400 3700	4KiB
QSPI_TARG	0x4400 3900	4KiB
L3_INSTR	0x4500 0100	4KiB
DEBUGSS_CT_TBR_TARG	0x4500 0300	4KiB

14.2.5.1.3.1 L3_MAIN TARG Register Summary

Table 14-98. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPMC_TARG L3_MAIN Physical Address	DMM_P1_TARG L3_MAIN Physical Address	DSP1_SDMA_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0100	0x4400 0200	0x4400 0300
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0104	0x4400 0204	0x4400 0304
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0108	0x4400 0208	0x4400 0308
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0110	0x4400 0210	0x4400 0310
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0140	0x4400 0240	0x4400 0340
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0144	0x4400 0244	0x4400 0344
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0148	0x4400 0248	0x4400 0348
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 014C	0x4400 024C	0x4400 034C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0150	0x4400 0250	0x4400 0350
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0154	0x4400 0254	0x4400 0354
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0158	0x4400 0258	0x4400 0358
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 015C	0x4400 025C	0x4400 035C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0160	0x4400 0260	0x4400 0360
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0164	0x4400 0264	0x4400 0364
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0168	0x4400 0268	0x4400 0368
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 016C	0x4400 026C	0x4400 036C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0180	0x4400 0280	0x4400 0380

Table 14-99. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	L4_CFG_TARG L3_MAIN Physical Address	DSP2_SDMA_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0500	0x4400 0600
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0504	0x4400 0604
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0508	0x4400 0608
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0510	0x4400 0610
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0540	0x4400 0640
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0544	0x4400 0644
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0548	0x4400 0648
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 054C	0x4400 064C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0550	0x4400 0650

Table 14-99. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L4_CFG_TARG L3_MAIN Physical Address	DSP2_SDMA_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0554	0x4400 0654
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0558	0x4400 0658
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 055C	0x4400 065C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0560	0x4400 0660
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0564	0x4400 0664
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0568	0x4400 0668
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 056C	0x4400 066C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0580	0x4400 0680

Table 14-100. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	VCP1_TARG L3_MAIN Physical Address	VCP2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0700	0x4400 0800
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0704	0x4400 0804
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0708	0x4400 0808
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0710	0x4400 0810
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0740	0x4400 0840
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0744	0x4400 0844
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0748	0x4400 0848
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 074C	0x4400 084C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0750	0x4400 0850
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0754	0x4400 0854
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0758	0x4400 0858
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 075C	0x4400 085C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0760	0x4400 0860
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0764	0x4400 0864
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0768	0x4400 0868
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 076C	0x4400 086C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0780	0x4400 0880

Table 14-101. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	BB2D_TARG L3_MAIN Physical Address	IPU2_TARG L3_MAIN Physical Address	PRUSS2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0900	0x4400 1100	0x4400 1500
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0904	0x4400 1104	0x4400 1504
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0908	0x4400 1108	0x4400 1508
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0910	0x4400 1110	0x4400 1510
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0940	0x4400 1140	0x4400 1540
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0944	0x4400 1144	0x4400 1544
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0948	0x4400 1148	0x4400 1548
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 094C	0x4400 114C	0x4400 154C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0950	0x4400 1150	0x4400 1550
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0954	0x4400 1154	0x4400 1554
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0958	0x4400 1158	0x4400 1558
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 095C	0x4400 115C	0x4400 155C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0960	0x4400 1160	0x4400 1560
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0964	0x4400 1164	0x4400 1564
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0968	0x4400 1168	0x4400 1568
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 096C	0x4400 116C	0x4400 156C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0980	0x4400 1180	0x4400 1580

Table 14-102. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	MCASP1_TARG L3_MAIN Physical Address	MCASP2_TARG L3_MAIN Physical Address	MCASP3_TARG L3_MAIN Physical Address	PCIE2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 2F00	0x4400 3000	0x4400 3100	0x4400 3800
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 2F04	0x4400 3004	0x4400 3104	0x4400 3804
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 2F08	0x4400 3008	0x4400 3108	0x4400 3808
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 2F10	0x4400 3010	0x4400 3110	0x4400 3810
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 2F40	0x4400 3040	0x4400 3140	0x4400 3840
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 2F44	0x4400 3044	0x4400 3144	0x4400 3844
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 2F48	0x4400 3048	0x4400 3148	0x4400 3848
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 2F4C	0x4400 304C	0x4400 314C	0x4400 384C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 2F50	0x4400 3050	0x4400 3150	0x4400 3850
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 2F54	0x4400 3054	0x4400 3154	0x4400 3854

Table 14-102. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MCASP1_TARG L3_MAIN Physical Address	MCASP2_TARG L3_MAIN Physical Address	MCASP3_TARG L3_MAIN Physical Address	PCIE2_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 2F58	0x4400 3058	0x4400 3158	0x4400 3858
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 2F5C	0x4400 305C	0x4400 315C	0x4400 385C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 2F60	0x4400 3060	0x4400 3160	0x4400 3860
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 2F64	0x4400 3064	0x4400 3164	0x4400 3864
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 2F68	0x4400 3068	0x4400 3168	0x4400 3868
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 2F6C	0x4400 306C	0x4400 316C	0x4400 386C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 2F80	0x4400 3080	0x4400 3180	0x4400 3880

Table 14-103. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	EVE4_TARG L3_MAIN Physical Address	EVE3_TARG L3_MAIN Physical Address	EVE1_TARG L3_MAIN Physical Address	EVE2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0D00	0x4400 0C00	0x4400 0A00	0x4400 0B00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0D04	0x4400 0C04	0x4400 0A04	0x4400 0B04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0D08	0x4400 0C08	0x4400 0A08	0x4400 0B08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0D10	0x4400 0C10	0x4400 0A10	0x4400 0B10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0D40	0x4400 0C40	0x4400 0A40	0x4400 0B40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0D44	0x4400 0C44	0x4400 0A44	0x4400 0B44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0D48	0x4400 0C48	0x4400 0A48	0x4400 0B48
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 0D4C	0x4400 0C4C	0x4400 0A4C	0x4400 0B4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0D50	0x4400 0C50	0x4400 0A50	0x4400 0B50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0D54	0x4400 0C54	0x4400 0A54	0x4400 0B54
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0D58	0x4400 0C58	0x4400 0A58	0x4400 0B58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 0D5C	0x4400 0C5C	0x4400 0A5C	0x4400 0B5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0D60	0x4400 0C60	0x4400 0A60	0x4400 0B60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0D64	0x4400 0C64	0x4400 0A64	0x4400 0B64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0D68	0x4400 0C68	0x4400 0A68	0x4400 0B68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 0D6C	0x4400 0C6C	0x4400 0A6C	0x4400 0B6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0D80	0x4400 0C80	0x4400 0A80	0x4400 0B80

Table 14-104. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	L4_PER3_P3_TARG L3_MAIN Physical Address	OCMC_RAM1_TARG L3_MAIN Physical Address	IPU1_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0E00	0x4400 0F00	0x4400 1000
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0E04	0x4400 0F04	0x4400 1004
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 0E08	0x4400 0F08	0x4400 1008
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 0E10	0x4400 0F10	0x4400 1010
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0E40	0x4400 0F40	0x4400 1040
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0E44	0x4400 0F44	0x4400 1044
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0E48	0x4400 0F48	0x4400 1048
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 0E4C	0x4400 0F4C	0x4400 104C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0E50	0x4400 0F50	0x4400 1050
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0E54	0x4400 0F54	0x4400 1054
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0E58	0x4400 0F58	0x4400 1058
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 0E5C	0x4400 0F5C	0x4400 105C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0E60	0x4400 0F60	0x4400 1060
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 0E64	0x4400 0F64	0x4400 1064
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 0E68	0x4400 0F68	0x4400 1068
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 0E6C	0x4400 0F6C	0x4400 106C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 0E80	0x4400 0F80	0x4400 1080

Table 14-105. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPU_TARG L3_MAIN Physical Address	DMM_P2_TARG L3_MAIN Physical Address	PRUSS1_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 1200	0x4400 1300	0x4400 1400
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 1204	0x4400 1304	0x4400 1404
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 1208	0x4400 1308	0x4400 1408
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 1210	0x4400 1310	0x4400 1410
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 1240	0x4400 1340	0x4400 1440
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 1244	0x4400 1344	0x4400 1444
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 1248	0x4400 1348	0x4400 1448
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 124C	0x4400 134C	0x4400 144C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 1250	0x4400 1350	0x4400 1450
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 1254	0x4400 1354	0x4400 1454
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 1258	0x4400 1358	0x4400 1458

Table 14-105. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPU_TARG L3_MAIN Physical Address	DMM_P2_TARG L3_MAIN Physical Address	PRUSS1_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 125C	0x4400 135C	0x4400 145C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 1260	0x4400 1360	0x4400 1460
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 1264	0x4400 1364	0x4400 1464
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 1268	0x4400 1368	0x4400 1468
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 126C	0x4400 136C	0x4400 146C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 1280	0x4400 1380	0x4400 1480

Table 14-106. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVA_CONFIG_TARG L3_MAIN Physical Address	OCMC_RAM2_TARG L3_MAIN Physical Address	IVA_SL2IF_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 1600	0x4400 1700	0x4400 1800
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 1604	0x4400 1704	0x4400 1804
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 1608	0x4400 1708	0x4400 1808
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 1610	0x4400 1710	0x4400 1810
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 1640	0x4400 1740	0x4400 1840
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 1644	0x4400 1744	0x4400 1844
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 1648	0x4400 1748	0x4400 1848
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 164C	0x4400 174C	0x4400 184C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 1650	0x4400 1750	0x4400 1850
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 1654	0x4400 1754	0x4400 1854
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 1658	0x4400 1758	0x4400 1858
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 165C	0x4400 175C	0x4400 185C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 1660	0x4400 1760	0x4400 1860
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 1664	0x4400 1764	0x4400 1864
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 1668	0x4400 1768	0x4400 1868
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 166C	0x4400 176C	0x4400 186C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 1680	0x4400 1780	0x4400 1880

Table 14-107. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	OCMC_RAM3_TARG L3_MAIN Physical Address	L4_PER1_P1_TARG L3_MAIN Physical Address	L4_WKUP_TARG L3_MAIN Physical Address	L4_PER1_P2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 1900	0x4400 1C00	0x4400 1D00	0x4400 1F00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 1904	0x4400 1C04	0x4400 1D04	0x4400 1F04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 1908	0x4400 1C08	0x4400 1D08	0x4400 1F08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 1910	0x4400 1C10	0x4400 1D10	0x4400 1F10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 1940	0x4400 1C40	0x4400 1D40	0x4400 1F40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 1944	0x4400 1C44	0x4400 1D44	0x4400 1F44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 1948	0x4400 1C48	0x4400 1D48	0x4400 1F48
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 194C	0x4400 1C4C	0x4400 1D4C	0x4400 1F4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 1950	0x4400 1C50	0x4400 1D50	0x4400 1F50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 1954	0x4400 1C54	0x4400 1D54	0x4400 1F54
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 1958	0x4400 1C58	0x4400 1D58	0x4400 1F58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 195C	0x4400 1C5C	0x4400 1D5C	0x4400 1F5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 1960	0x4400 1C60	0x4400 1D60	0x4400 1F60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 1964	0x4400 1C64	0x4400 1D64	0x4400 1F64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 1968	0x4400 1C68	0x4400 1D68	0x4400 1F68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 196C	0x4400 1C6C	0x4400 1D6C	0x4400 1F6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 1980	0x4400 1C80	0x4400 1D80	0x4400 1F80

Table 14-108. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	TPCC_TARG L3_MAIN Physical Address	L4_PER1_P3_TARG L3_MAIN Physical Address	MMU1_TARG L3_MAIN Physical Address	L4_PER2_P1_TARG L3_MAIN Physical Address	L4_PER2_P2_TARG L3_MAIN Physical Address	L4_PER2_P3_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 2000	0x4400 2100	0x4400 2200	0x4400 2300	0x4400 2400	0x4400 2500
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 2004	0x4400 2104	0x4400 2204	0x4400 2304	0x4400 2404	0x4400 2504
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 2008	0x4400 2108	0x4400 2208	0x4400 2308	0x4400 2408	0x4400 2508
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 2010	0x4400 2110	0x4400 2210	0x4400 2310	0x4400 2410	0x4400 2510

Table 14-108. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TPCC_TARG L3_MAIN Physical Address	L4_PER1_P3_TARG L3_MAIN Physical Address	MMU1_TARG L3_MAIN Physical Address	L4_PER2_P1_TARG L3_MAIN Physical Address	L4_PER2_P2_TARG L3_MAIN Physical Address	L4_PER2_P3_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 2040	0x4400 2140	0x4400 2240	0x4400 2340	0x4400 2440	0x4400 2540
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 2044	0x4400 2144	0x4400 2244	0x4400 2344	0x4400 2444	0x4400 2544
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 2048	0x4400 2148	0x4400 2248	0x4400 2348	0x4400 2448	0x4400 2548
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 204C	0x4400 214C	0x4400 224C	0x4400 234C	0x4400 244C	0x4400 254C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 2050	0x4400 2150	0x4400 2250	0x4400 2350	0x4400 2450	0x4400 2550
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 2054	0x4400 2154	0x4400 2254	0x4400 2354	0x4400 2454	0x4400 2554
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 2058	0x4400 2158	0x4400 2258	0x4400 2358	0x4400 2458	0x4400 2558
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 205C	0x4400 215C	0x4400 225C	0x4400 235C	0x4400 245C	0x4400 255C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 2060	0x4400 2160	0x4400 2260	0x4400 2360	0x4400 2460	0x4400 2560
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 2064	0x4400 2164	0x4400 2264	0x4400 2364	0x4400 2464	0x4400 2564
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 2068	0x4400 2168	0x4400 2268	0x4400 2368	0x4400 2468	0x4400 2568
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 206C	0x4400 216C	0x4400 226C	0x4400 236C	0x4400 246C	0x4400 256C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 2080	0x4400 2180	0x4400 2280	0x4400 2380	0x4400 2480	0x4400 2580

Table 14-109. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	L4_PER3_P1_TARG L3_MAIN Physical Address	L4_PER3_P2_TARG L3_MAIN Physical Address	MMU2_TARG L3_MAIN Physical Address	DSS_TARG L3_MAIN Physical Address	TPTC2_TARGL3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 2600	0x4400 2700	0x4400 2800	0x4400 2900	0x4400 2B00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 2604	0x4400 2704	0x4400 2804	0x4400 2904	0x4400 2B04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 2608	0x4400 2708	0x4400 2808	0x4400 2908	0x4400 2B08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 2610	0x4400 2710	0x4400 2810	0x4400 2910	0x4400 2B10

Table 14-109. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L4_PER3_P1_TARG L3_MAIN Physical Address	L4_PER3_P2_TARG L3_MAIN Physical Address	MMU2_TARG L3_MAIN Physical Address	DSS_TARG L3_MAIN Physical Address	TPTC2_TARGL3_MAIN Physical Address
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 2640	0x4400 2740	0x4400 2840	0x4400 2940	0x4400 2B40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 2644	0x4400 2744	0x4400 2844	0x4400 2944	0x4400 2B44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 2648	0x4400 2748	0x4400 2848	0x4400 2948	0x4400 2B48
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 264C	0x4400 274C	0x4400 284C	0x4400 294C	0x4400 2B4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 2650	0x4400 2750	0x4400 2850	0x4400 2950	0x4400 2B50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 2654	0x4400 2754	0x4400 2854	0x4400 2954	0x4400 2B54
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 2658	0x4400 2758	0x4400 2858	0x4400 2958	0x4400 2B58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 265C	0x4400 275C	0x4400 285C	0x4400 295C	0x4400 2B5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 2660	0x4400 2760	0x4400 2860	0x4400 2960	0x4400 2B60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 2664	0x4400 2764	0x4400 2864	0x4400 2964	0x4400 2B64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 2668	0x4400 2768	0x4400 2868	0x4400 2968	0x4400 2B68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 266C	0x4400 276C	0x4400 286C	0x4400 296C	0x4400 2B6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 2680	0x4400 2780	0x4400 2880	0x4400 2980	0x4400 2B80

Table 14-110. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	TPTC1_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 2E00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 2E04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 2E08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 2E10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 2E40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 2E44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 2E48
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 2E4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 2E50

Table 14-110. L3_MAIN TARG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TPTC1_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 2E54
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 2E58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 2E5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 2E60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 2E64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 2E68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 2E6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 2E80

Table 14-111. L3_MAIN TARG Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	PCIE1_TARG L3_MAIN Physical Address	QSPI_TARG L3_MAIN Physical Address	L3_INSTR_TARG L3_MAIN Physical Address	DEBUGSS_CT_TBR_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 3700	0x4400 3900	0x4500 0100	0x4500 0300
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 3704	0x4400 3904	0x4500 0104	0x4500 0304
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0008	0x4400 3708	0x4400 3908	0x4500 0108	0x4500 0308
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0010	0x4400 3710	0x4400 3910	0x4500 0110	0x4500 0310
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 3740	0x4400 3940	0x4500 0140	0x4500 0340
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 3744	0x4400 3944	0x4500 0144	0x4500 0344
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 3748	0x4400 3948	0x4500 0148	0x4500 0348
L3_TARG_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 374C	0x4400 394C	0x4500 014C	0x4500 034C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 3750	0x4400 3950	0x4500 0150	0x4500 0350
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 3754	0x4400 3954	0x4500 0154	0x4500 0354
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 3758	0x4400 3958	0x4500 0158	0x4500 0358
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 375C	0x4400 395C	0x4500 015C	0x4500 035C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 3760	0x4400 3960	0x4500 0160	0x4500 0360
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0064	0x4400 3764	0x4400 3964	0x4500 0164	0x4500 0364
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0068	0x4400 3768	0x4400 3968	0x4500 0168	0x4500 0368
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 006C	0x4400 376C	0x4400 396C	0x4500 016C	0x4500 036C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0080	0x4400 3780	0x4400 3980	0x4500 0180	0x4500 0380

14.2.5.1.3.2 L3_MAIN TARG Register Description

Table 14-112. L3_TARG_STDHOSTHDR_COREREG

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_ CORECODE								RESERVED								STDHOSTHDR_COREREG_ VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_ CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x13.	R	0x13
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_ VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-113. Register Call Summary for Register L3_TARG_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 14-114. L3_TARG_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-115. Register Call Summary for Register L3_TARG_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 14-116. L3_TARG_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STDHOSTHDR_MAINCTLREG_CM	STDHOSTHDR_MAINCTLREG_FLT	RESERVED	STDHOSTHDR_MAINCTLREG_EN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	STDHOSTHDR_MAINCTLREG_CM	Reserved for internal testing. Must be set to 0. Type: Control. Reset value: 0x0.	R	0
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1	RESERVED	Reserved	R	0
0	STDHOSTHDR_MAINCTLREG_EN	Sets the global core enable. Note: A disabled master does not generate any NTTP requests, and a disabled slave replies with an error packet to any request it receives. Type: Control. Reset value: 0x1.	RW	1

Table 14-117. Register Call Summary for Register L3_TARG_STDHOSTHDR_MAINCTLREG

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 14-118. L3_TARG_STDHOSTHDR_NTTPADDR_0

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDHOSTHDR_NTTPADDR_0							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	STDHOSTHDR_NTTPADDR_0	Shows the Rx port address. Type: Control. Reset value: 0x15.	R	See (1)

(1) GPMC- 0xC; DMM_P1 – 0x2; DSP1_SDMA - 0x4; L4_CFG - 0x14; DSP2_SDMA - 0x5; MCASP1 - 0x1F; EVE1 - 0x7; EVE2 - 0x8; EVE3 - 0x9; EVE4 - 0xA; L4_PER3_P3 – 0x1; OCMC_RAM1 - 0x24; IPU1 - 0x10; IPU2 - 0x11; BB2D – 0xB;GPU- 0xD; DMM_P2 - 0x3; PRU-ICSS1 - 0x2A, PRU-ICSS2 -0x2B ; IVA_CONFIG - 0x12; OCMC_RAM2 - 0x25; IVA_SL2IF - 0x13; OCMC_RAM3 - 0x26; L4_PER1_P1 - 0x16; L4_WKUP - 0x1E; L4_PER1_P2 - 0x17; TPCC - 0x30; L4_PER1_P3 - 0x18; MMU1 - 0x22; L4_PER2_P1 - 0x18; L4_PER2_P2 - 0x42; L4_PER2_P3 - 0x1A; L4_PER3_P1 - 0x1B; L4_PER3_P2 - 0x1C; MMU2 - 0x23; DSS - 0x6; TPTC2 - 0x32; TPTC1 - 0x31; PCIE1 - 0x28; PCIE2 - 0x29; QSPI - 0x39; L3_INSTR- 0x19; DEBUGSS - 0x41.

Table 14-119. Register Call Summary for Register L3_TARG_STDHOSTHDR_NTTPADDR_0

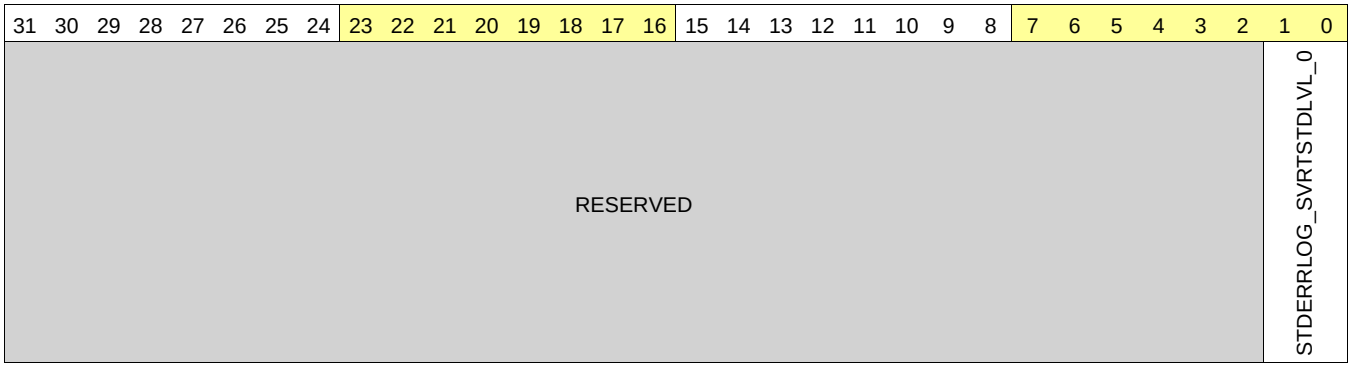
L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-120. L3_TARG_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

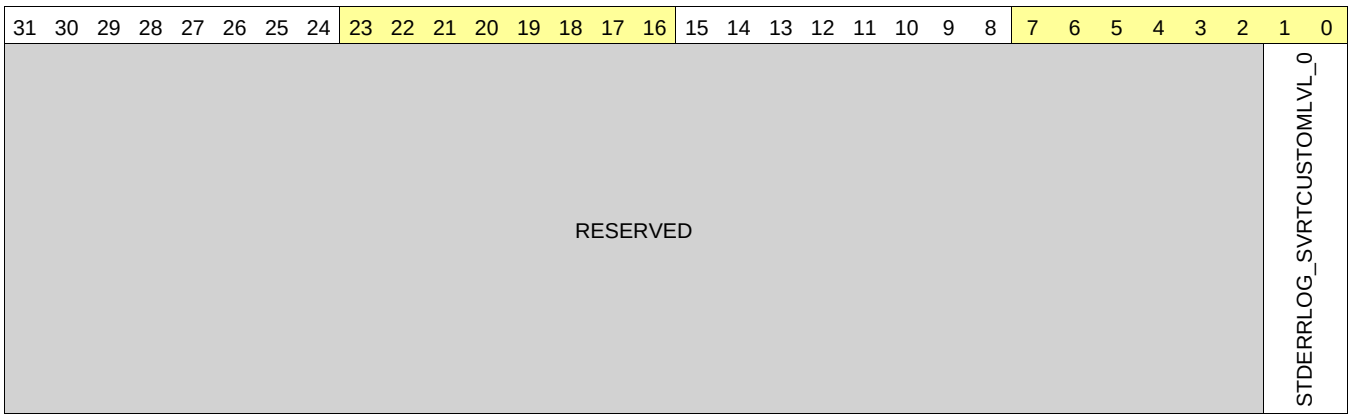
Table 14-121. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTSTDLVL

L3_MAIN Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN TARG Register Summary and Description: [2] [3] [4] [5] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Table 14-122. L3_TARG_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

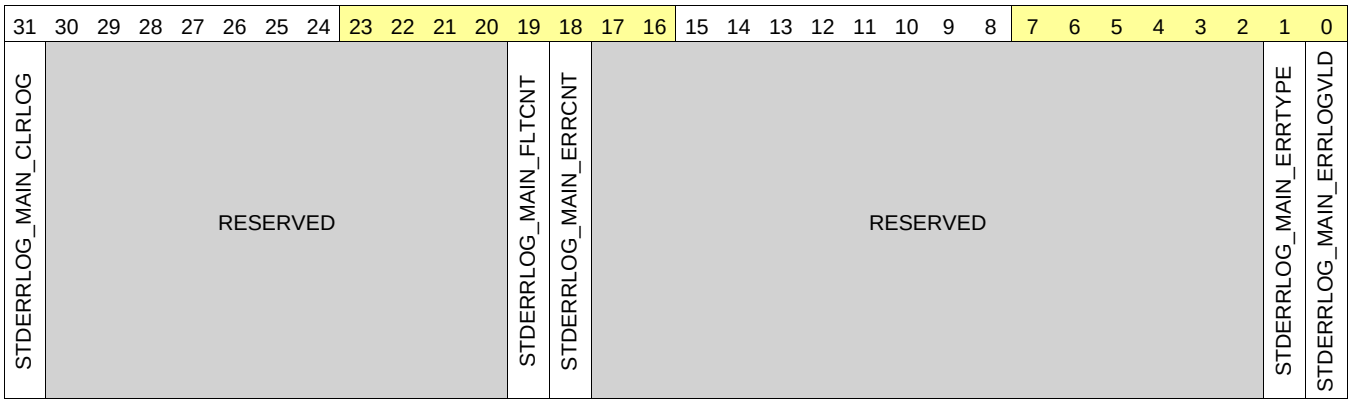
Table 14-123. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTCUSTOMLVL

L3_MAIN Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Register Summary and Description: [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 14-124. L3_TARG_STDERRLOG_MAIN

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears "Error Logging Valid" bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED	Reserved	R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED	Reserved	R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

Table 14-125. Register Call Summary for Register L3_TARG_STDERRLOG_MAIN

L3_MAIN Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN Interconnect Error Analysis Mode: [2] [3] [4] [5] [6] [7]
- L3_MAIN TARG Register Summary and Description: [8] [9] [10] [11] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]

Table 14-126. L3_TARG_STDERRLOG_HDR

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				STDERRLOG_HDR_LEN1										RESERVED		STDERRLOG_HDR_STOPOFSWRPSZ				STDERRLOG_HDR_ERR	RESERVED			STDERRLOG_HDR_PRESSURE		RESERVED		STDERRLOG_HDR_OPCODE			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED	Reserved	R	0x0

Bits	Field Name	Description	Type	Reset
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:8	RESERVED	Reserved	R	0x0
7:6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED	Reserved	R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 14-127. Register Call Summary for Register L3_TARG_STDERRLOG_HDR

L3_MAIN Interconnect
- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Register Summary and Description: [2] [3] [4] [5] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Table 14-128. L3_TARG_STDERRLOG_MSTADDR

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-129. Register Call Summary for Register L3_TARG_STDERRLOG_MSTADDR

L3_MAIN Interconnect
- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Register Summary and Description: [2] [3] [4] [5] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Table 14-130. L3_TARG_STDERRLOG_SLVADDR

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SLVADDR	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-131. Register Call Summary for Register L3_TARG_STDERRLOG_SLVADDR

L3_MAIN Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Register Summary and Description: [2] [3] [4] [5] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Table 14-132. L3_TARG_STDERRLOG_INFO

Address Offset	See Table 14-98.		
Physical Address		**Instance**	
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-133. Register Call Summary for Register L3_TARG_STDERRLOG_INFO

L3_MAIN Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Register Summary and Description: [2] [3] [4] [5] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Table 14-134. L3_TARG_STDERRLOG_SLVOFSLSB

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the "slave offset" field, concatenated with "start offset" field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 14-135. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSLSB

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 14-136. L3_TARG_STDERRLOG_SLVOFSMSB

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the "slave offset" field of the logged packet (according to NTTP packet format, this register field may exceed the actual "slave offset" size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 14-137. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSMSB

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 14-138. L3_TARG_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Info field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 14-139. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_INFO

L3_MAIN Interconnect
- L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Register Summary and Description: [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 14-140. L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_MSTADDR							

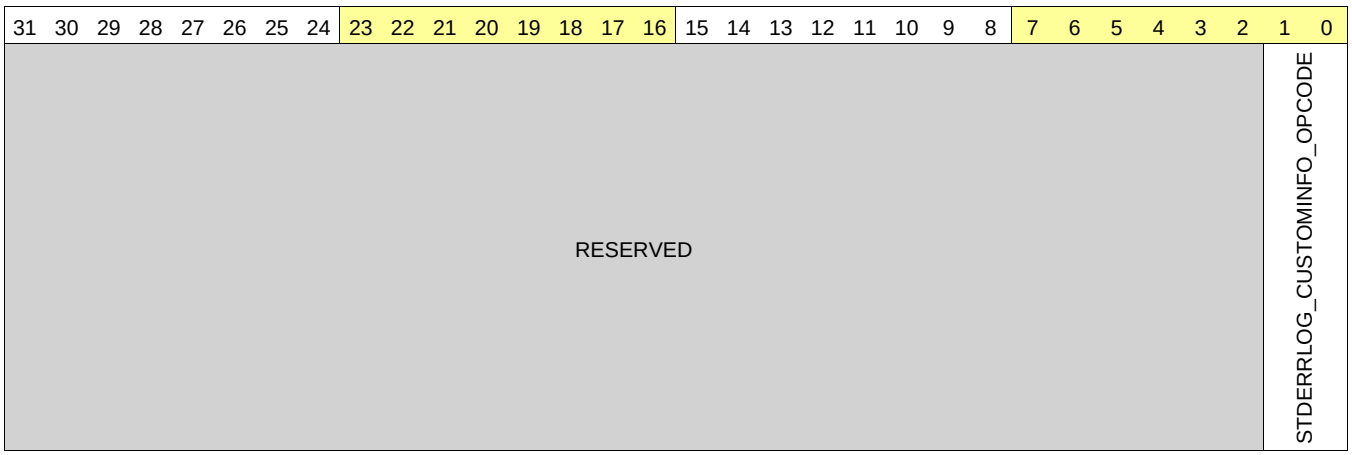
Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_CUSTOMINFO_MSTADDR	MstAddr field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 14-141. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

L3_MAIN Interconnect
- L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Register Summary and Description: [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 14-142. L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_CUSTOMINFO_OPCODE	Opcode of the response packet. Type: Status. Reset value: X.	R	0x0

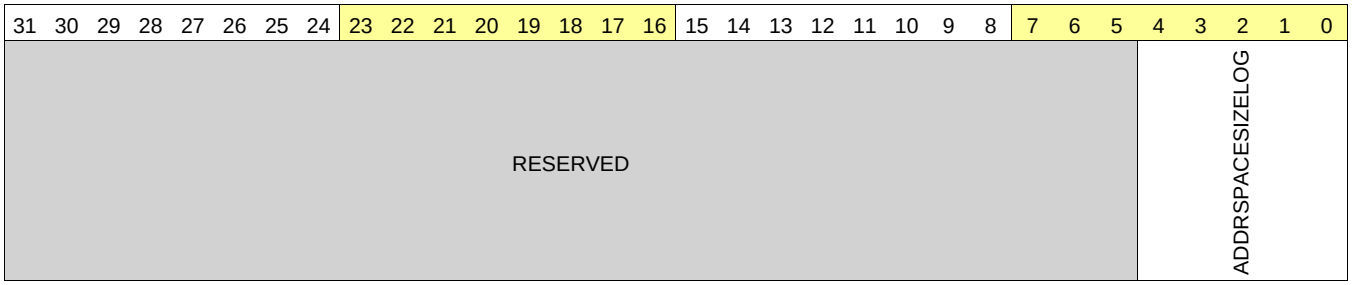
Table 14-143. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

L3_MAIN Interconnect

- L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Register Summary and Description: [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 14-144. L3_TARG_ADDRSPACESIZELOG

Address Offset	See Table 14-98.		
Physical Address	See Table 14-98 to Table 14-111	**Instance**	See Table 14-98 to Table 14-111
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	ADDRSPACESIZELOG	The address space size is equal to 2**AddrSpaceSizeLog * 4K in bytes. Type: Control. Reset value: 0x1F.	RW	0x1F

Table 14-145. Register Call Summary for Register L3_TARG_ADDRSPACESIZELOG

L3_MAIN Interconnect

- L3_MAIN TARG Register Summary and Description: [0] [1] [2] [3] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

14.2.5.1.4 L3_MAIN FLAGMUX Registers Summary and Description

Table 14-146. FLAGMUX Instance Summary

Module Name	Base Address	Size
CLK1_FLAGMUX_CLK1_1	0x4480 3500	4KiB
CLK1_FLAGMUX_CLK1_2	0x4480 3600	4KiB
CLK2_FLAGMUX_CLK2_1	0x4500 0200	4KiB

14.2.5.1.4.1 L3_MAIN FLAGMUX Registers Summary

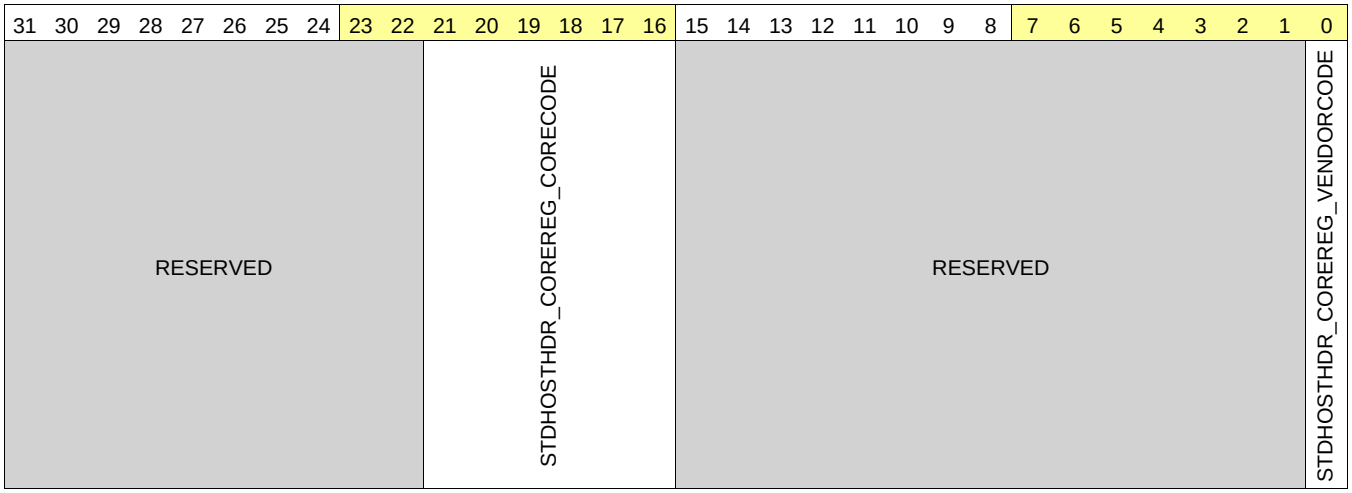
Table 14-147. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_FLAGMUX_CLK1_1 L3_MAIN Physical Address	CLK1_FLAGMUX_CLK1_2 L3_MAIN Physical Address	CLK2_FLAGMUX_CLK2_1 L3_MAIN Physical Address
L3_FLAGMUX_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 3500	0x4480 3600	0x4500 0200
L3_FLAGMUX_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 3504	0x4480 3604	0x4500 0204
L3_FLAGMUX_MASK0	RW	32	0x0000 0008	0x4480 3508	0x4480 3608	0x4500 0208
L3_FLAGMUX_REGERR0	R	32	0x0000 000C	0x4480 350C	0x4480 360C	0x4500 020C
L3_FLAGMUX_MASK1	RW	32	0x0000 0010	0x4480 3510	0x4480 3610	0x4500 0210
L3_FLAGMUX_REGERR1	RW	32	0x0000 0014	0x4480 3514	0x4480 3614	0x4500 0214

14.2.5.1.4.2 L3_MAIN FLAGMUX Rebisters Description

Table 14-148. L3_FLAGMUX_STDHOSTHDR_COREREG

Address Offset	See Table 14-147		
Physical Address	0x4480 3500 0x4480 3600 0x4500 0200	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-149. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX Registers Summary and Description: [0]

Table 14-150. L3_FLAGMUX_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-147		
Physical Address	0x4480 3504 0x4480 3604 0x4500 0204	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-151. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- Flag Muxing: [0] [1]
- L3_MAIN FLAGMUX Registers Summary and Description: [2]

Table 14-152. L3_FLAGMUX_MASK0

Address Offset	See Table 14-147		
Physical Address	0x4480 3508 0x4480 3608 0x4500 0208	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK0																															

Bits	Field Name	Description	Type	Reset
31:0 (1)	MASK0	Mask flag inputs 0 Type: Control.	RW	See (2)

(1) For CLK1_1 bit field is [31:0]; for CLK1_2 bit field is [22:0]; for CLK2 bit field is [3:0]

(2) Reset is 0xFFFFFFFF for CLK1_1; reset is 0x7FFFFF for CLK1_2; for CLK2 reset is 0xF

Table 14-153. Register Call Summary for Register L3_FLAGMUX_MASK0

L3_MAIN Interconnect

- Flag Mux Time-out: [0]
- Flag Mux Error Logging: [1]
- L3_MAIN Interconnect Error Analysis Mode: [2]
- L3_MAIN FLAGMUX Registers Summary and Description: [3]

Table 14-154. L3_FLAGMUX_REGERR0

Address Offset	See Table 14-147		
Physical Address	0x4480 350C 0x4480 360C 0x4500 020C	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REGERR0																															

Bits	Field Name	Description	Type	Reset
31:0	REGERR0	Flag inputs 0 Type: Status. Reset value: X.	R	0x00000

Table 14-155. Register Call Summary for Register L3_FLAGMUX_REGERR0

L3_MAIN Interconnect

- Flag Muxing: [0]
- Flag Mux Time-out: [1]
- Flag Mux Error Logging: [2]
- L3_MAIN Interconnect Error Analysis Mode: [3] [4] [5]
- L3_MAIN FLAGMUX Registers Summary and Description: [6]

Table 14-156. L3_FLAGMUX_MASK1

Address Offset	See Table 14-147		
Physical Address	0x4480 3510 0x4480 3610 0x4500 0210	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK1																															

Bits	Field Name	Description	Type	Reset
31:0 [1]	MASK1	Mask flag inputs 1 Type: Control. Reset value: 0x7FFFFF.	RW	See [2]

(1) For CLK1_1 bit field is [31:0]; for CLK1_2 bit field is [22:0]; for CLK2 bit field is [3:0]

(2) Reset is 0xFFFFFFFF for CLK1_1; reset is 0x7FFFFF for CLK1_2; for CLK2 reset is 0xF

Table 14-157. Register Call Summary for Register L3_FLAGMUX_MASK1

L3_MAIN Interconnect
- Flag Mux Time-out: [0]
- Flag Mux Error Logging: [1]
- L3_MAIN Interconnect Error Analysis Mode: [2]
- L3_MAIN FLAGMUX Registers Summary and Description: [3]

Table 14-158. L3_FLAGMUX_REGERR1

Address Offset	See Table 14-147		
Physical Address	0x4480 3514 0x4480 3614 0x4500 0214	**Instance**	CLK1_FLAGMUX_CLK1_1 CLK1_FLAGMUX_CLK1_2 CLK2_FLAGMUX_CLK2_1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REGERR1																															

Bits	Field Name	Description	Type	Reset
31:0	REGERR1	Flag inputs 1 Type: Status. Reset value: X.	R	0x00000

Table 14-159. Register Call Summary for Register L3_FLAGMUX_REGERR1

L3_MAIN Interconnect
- Flag Muxing: [0]
- Flag Mux Time-out: [1]
- Flag Mux Error Logging: [2]
- L3_MAIN Interconnect Error Analysis Mode: [3] [4] [5]
- L3_MAIN FLAGMUX Registers Summary and Description: [6]

14.2.5.1.5 L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description

Table 14-160. Instance Summary

Module Name	Base Address	Size
CLK1_FLAGMUX_CLK1MERGE	0x4400 0000	4KiB

14.2.5.1.5.1 L3_MAIN FLAGMUX CLK1MERGE Registers Summary

Table 14-161. FLAGMUX CLK1MERGE Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_FLAGMUX_CLK1MERGE L3_MAIN Physical Address
L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_COREREG	R	32	0x0080 0400	0x4480 0400
L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_VERSIONREG	R	32	0x0080 0404	0x4480 0404
L3_FLAGMUX_CLK1MERGE_MASK0	RW	32	0x0080 0408	0x4480 0408
L3_FLAGMUX_CLK1MERGE_REGERR0	R	32	0x0080 040C	0x4480 040C
L3_FLAGMUX_CLK1MERGE_MASK1	RW	32	0x0080 0410	0x4480 0410
L3_FLAGMUX_CLK1MERGE_REGERR1	R	32	0x0080 0414	0x4480 0414

14.2.5.1.5.2 L3_MAIN FLAGMUX CLK1MERGE Registers Description

Table 14-162. L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_COREREG

Address Offset	See Table 14-161.		
Physical Address	0x4480 0400	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-163. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [0]

Table 14-164. L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-161.		
Physical Address	0x4480 0404	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-165. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [0]

Table 14-166. L3_FLAGMUX_CLK1MERGE_MASK0

Address Offset	See Table 14-161.		
Physical Address	0x4480 0408	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MASK0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0
1:0	MASK0	Mask flag inputs 0 Type: Control. Reset value: 0x3	RW	0x3

Table 14-167. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_MASK0

L3_MAIN Interconnect

- Flag Muxing: [0]
- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [1]

Table 14-168. L3_FLAGMUX_CLK1MERGE_REGERR0

Address Offset	See Table 14-161.		
Physical Address	0x4480 040C	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REGERR0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0
1:0	REGERR0	Flag inputs 0 Type: Control. Reset value: X	RW	0x0

Table 14-169. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_REGERR0

L3_MAIN Interconnect

- Flag Muxing: [0]
- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [1]

Table 14-170. L3_FLAGMUX_CLK1MERGE_MASK1

Address Offset	See Table 14-161.		
Physical Address	0x4480 0410	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MASK1	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0
1:0	MASK1	Mask flag inputs 0 Type: Control. Reset value: 0x3	RW	0x3

Table 14-171. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_MASK1

L3_MAIN Interconnect

- Flag Muxing: [0]
- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [1]

Table 14-172. L3_FLAGMUX_CLK1MERGE_REGERR1

Address Offset	See Table 14-161.		
Physical Address	0x4480 0414	**Instance**	CLK1_FLAGMUX_CLK1MERGE
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REGERR1	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0
1:0	REGERR1	Flag inputs 0 Type: Control. Reset value: X	RW	0x0

Table 14-173. Register Call Summary for Register L3_FLAGMUX_CLK1MERGE_REGERR1

L3_MAIN Interconnect
- Flag Muxing: [0]
- L3_MAIN FLAGMUX CLK1MERGE Registers Summary and Description: [1]

14.2.5.1.6 L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description

Table 14-174. FLAGMUX TIMEOUT Instance Summary

Module Name	Base Address	Size
CLK1_FLAGMUX_CLK1	0x4400 0000	4KiB
CLK2_FLAGMUX_CLK2 (1)	0x4500 0000	4KiB

(1) clk2_flagmux_clk2 refers to CLK2_1 clock domain

14.2.5.1.6.1 L3_MAIN FLAGMUX TIMEOUT Registers Summary

Table 14-175. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_FLAGMUX_CLK1 L3_MAIN Physical Address	CLK2_FLAGMUX_CLK2 L3_MAIN Physical Address
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG	R	32	0x0000 0400	N/A	0x4500 0400
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG	R	32	0x0000 0404	N/A	0x4500 0404
L3_FLAGMUX_TIMEOUT_MASK0	RW	32	0x0000 0408	N/A	0x4500 0408
L3_FLAGMUX_TIMEOUT_REGERR0	R	32	0x0000 040C	N/A	0x4500 040C
L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_COREREG	R	32	0x0080 5700	0x4480 5700	N/A
L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_VERSIONREG	R	32	0x0080 5704	0x4480 5704	N/A
L3_FLAGMUX_TIMEOUT1_MASK0	RW	32	0x0080 5708	0x4480 5708	N/A
L3_FLAGMUX_TIMEOUT1_REGERR0	R	32	0x0080 570C	0x4480 570C	N/A
L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_COREREG	R	32	0x0080 5800	0x4480 5800	N/A

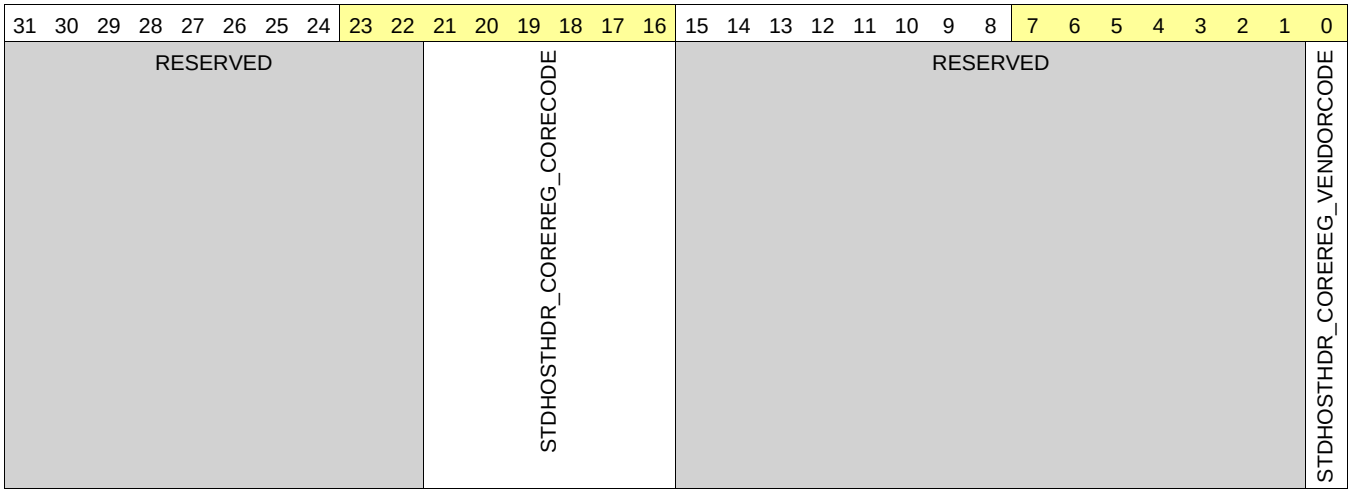
Table 14-175. FLAGMUX Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_FLAGMUX_CLK1 L3_MAIN Physical Address	CLK2_FLAGMUX_CLK2 L3_MAIN Physical Address
L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_VERSIONREG	R	32	0x0080 5804	0x4480 5804	N/A
L3_FLAGMUX_TIMEOUT2_MASK0	RW	32	0x0080 5808	0x4480 5808	N/A
L3_FLAGMUX_TIMEOUT2_REGERR0	R	32	0x0080 580C	0x4480 580C	N/A

14.2.5.1.6.2 L3_MAIN FLAGMUX TIMEOUT Registers Description

Table 14-176. L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG

Address Offset	See Table 14-175.		
Physical Address	0x4500 0400	**Instance**	CLK2_FLAGMUX_CLK2
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0bxx xxxx xxxx
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED		R	0bxxx xxxx xxxx xxxx
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-177. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-178. L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-175.		
Physical Address	0x4500 0404	**Instance**	CLK2_FLAGMUX_CLK2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x-- ----

Table 14-179. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-180. L3_FLAGMUX_TIMEOUT_MASK0

Address Offset	See Table 14-175.		
Physical Address	0x4500 0408	**Instance**	CLK2_FLAGMUX_CLK2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MASK0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
1:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x0.	RW	0x3

Table 14-181. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_MASK0

L3_MAIN Interconnect
- Flag Mux Time-out: [0] [1]
- L3_MAIN Interconnect Error Analysis Mode: [2]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [3]

Table 14-182. L3_FLAGMUX_TIMEOUT_REGERR0

Address Offset	See Table 14-175.		
Physical Address	0x4500 040C	**Instance**	CLK2_FLAGMUX_CLK2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REGERR0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
1:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0bx xxxx

Table 14-183. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_REGERR0

L3_MAIN Interconnect
- Flag Mux Time-out: [0]
- L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [2]

Table 14-184. L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_COREREG

Address Offset	See Table 14-175.		
Physical Address	0x4480 5700	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0bxx xxxx xxxx
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED		R	0bxxx xxxx xxxx xxxx
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-185. Register Call Summary for Register L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-186. L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-175.		
Physical Address	0x4480 5704	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x-- ----

Table 14-187. Register Call Summary for Register L3_FLAGMUX_TIMEOUT1_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-188. L3_FLAGMUX_TIMEOUT1_MASK0

Address Offset	See Table 14-175.		
Physical Address	0x4480 5708	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MASK0																							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
29:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x0.	RW	0x3FFFFFFF

Table 14-189. Register Call Summary for Register L3_FLAGMUX_TIMEOUT1_MASK0

L3_MAIN Interconnect

- Flag Mux Time-out: [0]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [1]

Table 14-190. L3_FLAGMUX_TIMEOUT1_REGERR0

Address Offset	See Table 14-175.		
Physical Address	0x4480 570C	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REGERR0																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
24:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0bx xxxx

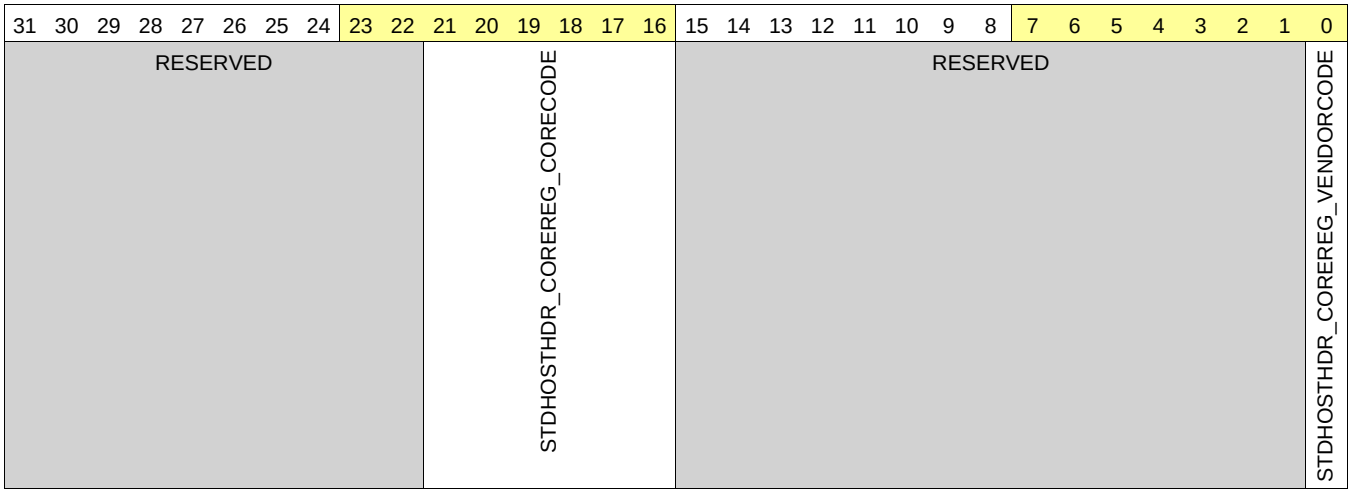
Table 14-191. Register Call Summary for Register L3_FLAGMUX_TIMEOUT1_REGERR0

L3_MAIN Interconnect

- Flag Mux Time-out: [0]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [1]

Table 14-192. L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_COREREG

Address Offset	See Table 14-175.		
Physical Address	0x4480 5800	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0bxx xxxx xxxx
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED		R	0bxxx xxxx xxxx xxxx
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-193. Register Call Summary for Register L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_COREREG

L3_MAIN Interconnect
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-194. L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-175.		
Physical Address	0x4480 5804	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x-- ----

Table 14-195. Register Call Summary for Register L3_FLAGMUX_TIMEOUT2_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [0]

Table 14-196. L3_FLAGMUX_TIMEOUT2_MASK0

Address Offset	See Table 14-175.		
Physical Address	0x4480 5808	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MASK0																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx
20:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x0.	RW	0x1FFFFFFF

Table 14-197. Register Call Summary for Register L3_FLAGMUX_TIMEOUT2_MASK0

L3_MAIN Interconnect

- Flag Mux Time-out: [0] [1]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [2]

Table 14-198. L3_FLAGMUX_TIMEOUT2_REGERR0

Address Offset	See Table 14-175.		
Physical Address	0x4480 580C	**Instance**	CLK1_FLAGMUX_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REGERR0																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx
20:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0bx xxxx

Table 14-199. Register Call Summary for Register L3_FLAGMUX_TIMEOUT2_REGERR0

L3_MAIN Interconnect

- Flag Mux Time-out: [0]
- L3_MAIN FLAGMUX TIMEOUT Registers Summary and Description: [1]

14.2.5.1.7 L3_MAIN BW Regulator Register Summary and Description

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-200. BW_REGULATOR Instance Summary

Module Name	Base Address	Size
CLK1_2_MMU2_BW_REGULATOR	0x4480 3B00	4KiB
CLK1_2_EVE1_TC0_BW_REGULATOR	0x4480 4200	4KiB
CLK1_2_EVE2_TC0_BW_REGULATOR	0x4480 4300	4KiB
CLK1_2_EVE3_TC0_BW_REGULATOR	0x4480 4400	4KiB
CLK1_2_EVE4_TC0_BW_REGULATOR	0x4480 4500	4KiB
CLK1_2_EVE1_TC1_BW_REGULATOR	0x4480 4600	4KiB
CLK1_2_EVE2_TC1_BW_REGULATOR	0x4480 4700	4KiB
CLK1_2_EVE3_TC1_BW_REGULATOR	0x4480 4800	4KiB
CLK1_2_EVE4_TC1_BW_REGULATOR	0x4480 4900	4KiB
CLK1_2_DSP2_EDMA_BW_REGULATOR	0x4480 4A00	4KiB
CLK1_2_DSP1_EDMA_BW_REGULATOR	0x4480 4B00	4KiB
CLK1_2_DSP1_MDMA_BW_REGULATOR	0x4480 4C00	4KiB
CLK1_2_DSP2_MDMA_BW_REGULATOR	0x4480 4D00	4KiB
CLK1_2_IVA_BW_REGULATOR	0x4480 5000	4KiB
CLK1_2_GPU_P1_BW_REGULATOR	0x4480 5200	4KiB
CLK1_2_GPU_P2_BW_REGULATOR	0x4480 5300	4KiB
CLK1_2_BB2D_P1_BW_REGULATOR	0x4480 4E00	4KiB
CLK1_2_BB2D_P2_BW_REGULATOR	0x4480 5100	4KiB
CLK1_2_PCIESS2_BW_REGULATOR	0x4480 5400	4KiB
CLK1_2_PCIESS1_BW_REGULATOR	0x4480 5500	4KiB
CLK1_2_GMAC_SW_BW_REGULATOR	0x4480 5600	4KiB

14.2.5.1.7.1 L3_MAIN BW_REGULATOR Register Summary

Table 14-201. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_MMU2_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 3B00
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 3B04
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 3B08
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 3B0C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 3B10
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 3B14

Table 14-202. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_EVE3_TC0_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_EVE4_TC0_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_EVE1_TC0_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4400	0x4480 4500	0x4480 4200
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4404	0x4480 4504	0x4480 4204
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4408	0x4480 4508	0x4480 4208
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 440C	0x4480 450C	0x4480 420C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4410	0x4480 4510	0x4480 4210
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4414	0x4480 4514	0x4480 4214

Table 14-203. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_EVE2_TC0_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_EVE1_TC1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_EVE2_TC1_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4300	0x4480 4600	0x4480 4700
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4304	0x4480 4604	0x4480 4704
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4308	0x4480 4608	0x4480 4708
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 430C	0x4480 460C	0x4480 470C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4310	0x4480 4610	0x4480 4710
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4314	0x4480 4614	0x4480 4714

Table 14-204. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_DSP2_EDMA_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_DSP1_EDMA_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_DSP1_MDMA_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4A00	0x4480 4B00	0x4480 4C00
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4A04	0x4480 4B04	0x4480 4C04
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4A08	0x4480 4B08	0x4480 4C08
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 4A0C	0x4480 4B0C	0x4480 4C0C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4A10	0x4480 4B10	0x4480 4C10
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4A14	0x4480 4B14	0x4480 4C14

Table 14-205. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_DSP2_MDMA_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_EVE3_TC1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_IVA_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4D00	0x4480 4800	0x4480 5000
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4D04	0x4480 4804	0x4480 5004
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4D08	0x4480 4808	0x4480 5008
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 4D0C	0x4480 480C	0x4480 500C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4D10	0x4480 4810	0x4480 5010
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4D14	0x4480 4814	0x4480 5014

Table 14-206. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_EVE4_TC1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_GPU_P1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_GPU_P2_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4900	0x4480 5200	0x4480 5300
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4904	0x4480 5204	0x4480 5304
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4908	0x4480 5208	0x4480 5308
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 490C	0x4480 520C	0x4480 530C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4910	0x4480 5210	0x4480 5310
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4914	0x4480 5214	0x4480 5314

Table 14-207. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_BB2D_P1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_BB2D_P2_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_PCIESS2_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4E00	0x4480 5100	0x4480 5400
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4E04	0x4480 5104	0x4480 5404
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 4E08	0x4480 5108	0x4480 5408
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 4E0C	0x4480 510C	0x4480 540C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 4E10	0x4480 5110	0x4480 5410
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4E14	0x4480 5114	0x4480 5414

Table 14-208. BW_REGULATOR Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CLK1_2_PCIESS1_BW_REGULATOR L3_MAIN Physical Address	CLK1_2_GMAC_SW_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 5500	0x4480 5600
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 5504	0x4480 5604
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0000 0008	0x4480 5508	0x4480 5608
L3_BW_REGULATOR_WATERMARK	RW	32	0x0000 000C	0x4480 550C	0x4480 560C
L3_BW_REGULATOR_PRESS	R	32	0x0000 0010	0x4480 5510	0x4480 5610
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0000 0014	0x4480 5514	0x4480 5614

14.2.5.1.7.2 L3_MAIN BW_REGULATOR Register Description

Table 14-209. L3_BW_REGULATOR_STDHOSTHDR_COREREG

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B00 0x4480 4400 0x4480 4500 0x4480 4200 0x4480 4300 0x4480 4600 0x4480 4700 0x4480 4A00 0x4480 4B00 0x4480 4C00 0x4480 4D00 0x4480 4800 0x4480 5000 0x4480 4900 0x4480 5200 0x4480 5300 0x4480 4E00 0x4480 5100 0x4480 5500 0x4480 5600	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x31.	R	0x31
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-210. Register Call Summary for Register L3_BW_REGULATOR_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN BW Regulator Register Summary and Description: [0] [1] [2] [3] [4] [5] [6] [7]

Table 14-211. L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B04 0x4480 4404 0x4480 4504 0x4480 4204 0x4480 4304 0x4480 4604 0x4480 4704 0x4480 4A04 0x4480 4B04 0x4480 4C04 0x4480 4D04 0x4480 4804 0x4480 5004 0x4480 4904 0x4480 5204 0x4480 5304 0x4480 4E04 0x4480 5104 0x4480 5504 0x4480 5604	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-212. Register Call Summary for Register L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN BW Regulator Register Summary and Description: [0] [1] [2] [3] [4] [5] [6] [7]

Table 14-213. L3_BW_REGULATOR_BANDWIDTH

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B08 0x4480 4408 0x4480 4508 0x4480 4208 0x4480 4308 0x4480 4608 0x4480 4708 0x4480 4A08 0x4480 4B08 0x4480 4C08 0x4480 4D08 0x4480 4808 0x4480 5008 0x4480 4908 0x4480 5208 0x4480 5308 0x4480 4E08 0x4480 5108 0x4480 5508 0x4480 5608	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BANDWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	BANDWIDTH	Bandwidth, in bytes per second. Type: Control. Reset value: 0x0.	RW	0x0000

Table 14-214. Register Call Summary for Register L3_BW_REGULATOR_BANDWIDTH

L3_MAIN Interconnect
- Bandwidth Regulators: [0] [1]
- L3_MAIN BW Regulator Register Summary and Description: [2] [3] [4] [5] [6] [7] [8] [9]

Table 14-215. L3_BW_REGULATOR_WATERMARK

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B0C 0x4480 440C 0x4480 450C 0x4480 420C 0x4480 430C 0x4480 460C 0x4480 470C 0x4480 4A0C 0x4480 4B0C 0x4480 4C0C 0x4480 4D0C 0x4480 480C 0x4480 500C 0x4480 490C 0x4480 520C 0x4480 530C 0x4480 4E0C 0x4480 510C 0x4480 550C 0x4480 560C	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				WATERMARK											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	WATERMARK	Peak permissible bandwidth, in bytes. Type: Control. Reset value: 0x1.	RW	0x001

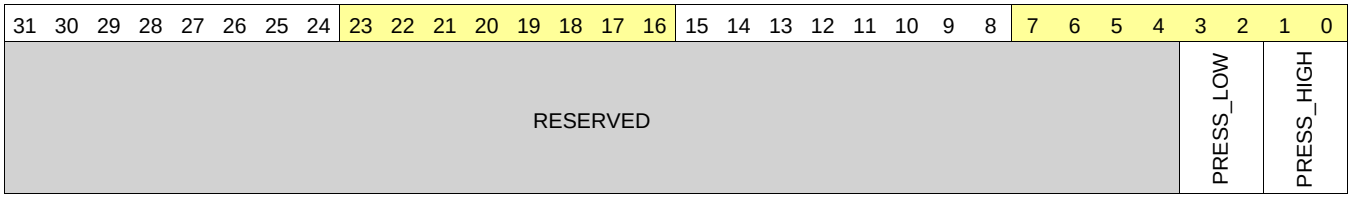
Table 14-216. Register Call Summary for Register L3_BW_REGULATOR_WATERMARK

L3_MAIN Interconnect

- Bandwidth Regulators: [0] [1] [2]
- L3_MAIN BW Regulator Register Summary and Description: [3] [4] [5] [6] [7] [8] [9] [10]

Table 14-217. L3_BW_REGULATOR_PRESS

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B10 0x4480 4410 0x4480 4510 0x4480 4210 0x4480 4310 0x4480 4610 0x4480 4710 0x4480 4A10 0x4480 4B10 0x4480 4C10 0x4480 4D10 0x4480 4810 0x4480 5010 0x4480 4910 0x4480 5210 0x4480 5310 0x4480 4E10 0x4480 5110 0x4480 5510 0x4480 5610	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:2	PRESS_LOW	Pressure value inserted if the measured bandwidth is over the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x0.	R	0

Bits	Field Name	Description	Type	Reset
1:0	PRESS_HIGH	Pressure value inserted if the measured bandwidth is under the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x1.	R	0x3

Table 14-218. Register Call Summary for Register L3_BW_REGULATOR_PRESS

L3_MAIN Interconnect

- Bandwidth Regulators: [0]
- L3_MAIN BW Regulator Register Summary and Description: [1] [2] [3] [4] [5] [6] [7] [8]

Table 14-219. L3_BW_REGULATOR_CLEARHISTORY

Address Offset	See Table 14-201 to Table 14-208		
Physical Address	0x4480 3B14 0x4480 4414 0x4480 4514 0x4480 4214 0x4480 4314 0x4480 4614 0x4480 4714 0x4480 4A14 0x4480 4B14 0x4480 4C14 0x4480 4D14 0x4480 4814 0x4480 5014 0x4480 4914 0x4480 5214 0x4480 5314 0x4480 4E14 0x4480 5114 0x4480 5514 0x4480 5614	**Instance**	CLK1_2_MMU2_BW_REGULATOR CLK1_2_EVE3_TC0_BW_REGULATOR CLK1_2_EVE4_TC0_BW_REGULATOR CLK1_2_EVE1_TC0_BW_REGULATOR CLK1_2_EVE2_TC0_BW_REGULATOR CLK1_2_EVE1_TC1_BW_REGULATOR CLK1_2_EVE2_TC1_BW_REGULATOR CLK1_2_DSP2_EDMA_BW_REGULATOR CLK1_2_DSP1_EDMA_BW_REGULATOR CLK1_2_DSP1_MDMA_BW_REGULATOR CLK1_2_DSP2_MDMA_BW_REGULATOR CLK1_2_EVE3_TC1_BW_REGULATOR CLK1_2_IVA_BW_REGULATOR CLK1_2_EVE4_TC1_BW_REGULATOR CLK1_2_GPU_P1_BW_REGULATOR CLK1_2_GPU_P2_BW_REGULATOR CLK1_2_BB2D_P1_BW_REGULATOR CLK1_2_BB2D_P2_BW_REGULATOR CLK1_2_PCIESS1_BW_REGULATOR CLK1_2_GMAC_SW_BW_REGULATOR
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEARHISTORY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	CLEARHISTORY	Write a 1 clear the traffic counter Type: Give_AutoCleared. Reset value: 0x0.	RW	0

Table 14-220. Register Call Summary for Register L3_BW_REGULATOR_CLEARHISTORY

L3_MAIN Interconnect
- Bandwidth Regulators: [0]
- L3_MAIN BW Regulator Register Summary and Description: [1] [2] [3] [4] [5] [6] [7] [8]

14.2.5.1.8 L3_MAIN Bandwidth Limiter Register Summary and Description

Table 14-221. BW_LIMITER Instance Summary

Module Name	Base Address	Size
CLK1_2_GPU_P1_BW_LIMITER	0x4480 5B00	256B
CLK1_2_GPU_P2_BW_LIMITER	0x4480 5C00	256B
CLK1_2_TPTC1_RD_BW_LIMITER	0x4480 3C00	256B
CLK1_2_TPTC2_RD_BW_LIMITER	0x4480 3D00	256B
CLK1_2_TPTC1_WR_BW_LIMITER	0x4480 3E00	256B
CLK1_2_TPTC2_WR_BW_LIMITER	0x4480 3F00	256B
CLK1_2_VPE_P2_BW_LIMITER	0x4480 4000	256B
CLK1_2_VPE_P1_BW_LIMITER	0x4480 4100	256B
CLK1_2_BB2D_P1_BW_LIMITER	0x4480 5900	256B
CLK1_2_BB2D_P2_BW_LIMITER	0x4480 5A00	256B
CLK1_2_MMU1_BW_LIMITER	0x4480 3A00	256B

14.2.5.1.8.1 L3_MAIN BW Limiter Register Summary

Table 14-222. BW_LIMITER Register Summary

Register Name	Type	Register Width (Bits)	Address offset	CLK1_2_GPU_P1_BW_LIMITER L3_MAIN Physical Address	CLK1_2_GPU_P2_BW_LIMITER L3_MAIN Physical Address	CLK1_2_TPTC1_RD_BW_LIMITER L3_MAIN Physical Address
L3_BW_LIMITER_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 5B00	0x4480 5C00	0x4480 3C00
L3_BW_LIMITER_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 5B04	0x4480 5C04	0x4480 3C04
L3_BW_LIMITER_BANDWIDTH_FRACTIONAL	RW	32	0x0000 0008	0x4480 5B08	0x4480 5C08	0x4480 3C08
L3_BW_LIMITER_BANDWIDTH_INTEGER	RW	32	0x0000 000C	0x4480 5B0C	0x4480 5C0C	0x4480 3C0C
L3_BW_LIMITER_WATERMARK_0	RW	32	0x0000 0010	0x4480 5B10	0x4480 5C10	0x4480 3C10
L3_BW_LIMITER_CLEARHISTORY	RW	32	0x0000 0014	0x4480 5B14	0x4480 5C14	0x4480 3C14

Table 14-223. BW_LIMITER Register Summary

Register Name	Type	Register Width (Bits)	Address offset	CLK1_2_TPTC2_RD_BW_LIMITER L3_MAIN Physical Address	CLK1_2_TPTC1_WR_BW_LIMITER L3_MAIN Physical Address	CLK1_2_TPTC2_WR_BW_LIMITER L3_MAIN Physical Address
L3_BW_LIMITER_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 3D00	0x4480 3E00	0x4480 3F00
L3_BW_LIMITER_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 3D04	0x4480 3E04	0x4480 3F04
L3_BW_LIMITER_BANDWIDTH_FRACTIONAL	RW	32	0x0000 0008	0x4480 3D08	0x4480 3E08	0x4480 3F08
L3_BW_LIMITER_BANDWIDTH_INTEGER	RW	32	0x0000 000C	0x4480 3D0C	0x4480 3E0C	0x4480 3F0C
L3_BW_LIMITER_WATERMARK_0	RW	32	0x0000 0010	0x4480 3D10	0x4480 3E10	0x4480 3F10
L3_BW_LIMITER_CLEARHISTORY	RW	32	0x0000 0014	0x4480 3D14	0x4480 3E14	0x4480 3F14

Table 14-224. BW_LIMITER Register Summary

Register Name	Type	Register Width (Bits)	Address offset	CLK1_2_VPE_P2_BW_LIMITER L3_MAIN Physical Address	CLK1_2_VPE_P1_BW_LIMITER L3_MAIN Physical Address
L3_BW_LIMITER_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 4000	0x4480 4100
L3_BW_LIMITER_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 4004	0x4480 4104
L3_BW_LIMITER_BANDWIDTH_FRACTIONAL	RW	32	0x0000 0008	0x4480 4008	0x4480 4108
L3_BW_LIMITER_BANDWIDTH_INTEGER	RW	32	0x0000 000C	0x4480 400C	0x4480 410C
L3_BW_LIMITER_WATERMARK_0	RW	32	0x0000 0010	0x4480 4010	0x4480 4110
L3_BW_LIMITER_CLEARHISTORY	RW	32	0x0000 0014	0x4480 4014	0x4480 4114

Table 14-225. BW_LIMITER Register Summary

Register Name	Type	Register Width (Bits)	Address offset	CLK1_2_MMU1_BW_LIMITER L3_MAIN Physical Address	CLK1_2_BB2D_P1_BW_LIMITER L3_MAIN Physical Address	CLK1_2_BB2D_P2_BW_LIMITER L3_MAIN Physical Address
L3_BW_LIMITER_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4480 3A00	0x4480 5900	0x4480 5A00
L3_BW_LIMITER_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4480 3A04	0x4480 5904	0x4480 5A04
L3_BW_LIMITER_BANDWIDTH_FRACTIONAL	RW	32	0x0000 0008	0x4480 3A08	0x4480 5908	0x4480 5A08
L3_BW_LIMITER_BANDWIDTH_INTEGER	RW	32	0x0000 000C	0x4480 3A0C	0x4480 590C	0x4480 5A0C
L3_BW_LIMITER_WATERMARK_0	RW	32	0x0000 0010	0x4480 3A10	0x4480 5910	0x4480 5A10
L3_BW_LIMITER_CLEARHISTORY	RW	32	0x0000 0014	0x4480 3A14	0x4480 5914	0x4480 5A14

14.2.5.1.8.2 L3_MAIN BW Limiter Register Description

Table 14-226. L3_BW_LIMITER_STDHOSTHDR_COREREG

Address Offset	See Table 14-222		
Physical Address	0x4480 5B00 0x4480 5C00 0x4480 3C00 0x4480 3D00 0x4480 3E00 0x4480 3F00 0x4480 4000 0x4480 4100 0x4480 3A00 0x4480 5900 0x4480 5A00	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x2C.	R	0x2C
15:1	RESERVED		R	0x0
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-227. Register Call Summary for Register L3_BW_LIMITER_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN Bandwidth Limiter Register Summary and Description: [0] [1] [2] [3]

Table 14-228. L3_BW_LIMITER_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-222		
Physical Address	0x4480 5B04 0x4480 5C04 0x4480 3C04 0x4480 3D04 0x4480 3E04 0x4480 3F04 0x4480 4004 0x4480 4104 0x4480 3A04 0x4480 5904 0x4480 5A04	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x0

Table 14-229. Register Call Summary for Register L3_BW_LIMITER_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN Bandwidth Limiter Register Summary and Description: [0] [1] [2] [3]

Table 14-230. L3_BW_LIMITER_BANDWIDTH_FRACTIONAL

Address Offset	See Table 14-222		
Physical Address	0x4480 5B08 0x4480 5C08 0x4480 3C08 0x4480 3D08 0x4480 3E08 0x4480 3F08 0x4480 4008 0x4480 4108 0x4480 3A08 0x4480 5908 0x4480 5A08	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BANDWIDTH_FRACTIONAL							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0
4:0	BANDWIDTH_FRACTIONAL	Fractional part of bandwitdh in terms of bytes per second Type: Control. Reset value: 0x0.	RW	0x0

Table 14-231. Register Call Summary for Register L3_BW_LIMITER_BANDWIDTH_FRACTIONAL

L3_MAIN Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN Bandwidth Limiter Register Summary and Description: [3] [4] [5] [6]

Table 14-232. L3_BW_LIMITER_BANDWIDTH_INTEGER

Address Offset	See Table 14-222		
Physical Address	0x4480 5B0C 0x4480 5C0C 0x4480 3C0C 0x4480 3D0C 0x4480 3E0C 0x4480 3F0C 0x4480 400C 0x4480 410C 0x4480 3A0C 0x4480 590C 0x4480 5A0C	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BANDWIDTH_INTEGER							

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0
3:0	BANDWIDTH_INTEGER	Integer part of bandwitdh in terms of bytes per second Type: Control. Reset value: 0x0.	RW	0x0

Table 14-233. Register Call Summary for Register L3_BW_LIMITER_BANDWIDTH_INTEGER

L3_MAIN Interconnect

- Bandwidth Limiters:
- L3_MAIN Bandwidth Limiter Register Summary and Description: [2] [3] [4] [5]

Table 14-234. L3_BW_LIMITER_WATERMARK_0

Address Offset	See Table 14-222		
Physical Address	0x4480 5B10 0x4480 5C10 0x4480 3C10 0x4480 3D10 0x4480 3E10 0x4480 3F10 0x4480 4010 0x4480 4110 0x4480 3A10 0x4480 5910 0x4480 5A10	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WATERMARK_0															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0
13:0	WATERMARK_0	Peak bandwidth allowed Type: Control. Reset value: 0x3FF.	RW	0x3FFF

Table 14-235. Register Call Summary for Register L3_BW_LIMITER_WATERMARK_0

L3_MAIN Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN Bandwidth Limiter Register Summary and Description: [2] [3] [4] [5]

Table 14-236. L3_BW_LIMITER_CLEARHISTORY

Address Offset	See Table 14-222		
Physical Address	0x4480 5B14 0x4480 5C14 0x4480 3C14 0x4480 3D14 0x4480 3E14 0x4480 3F14 0x4480 4014 0x4480 4114 0x4480 3A14 0x4480 5914 0x4480 5A14	**Instance**	CLK1_2_GPU_P1_BW_LIMITER CLK1_2_GPU_P2_BW_LIMITER CLK1_2_TPTC1_RD_BW_LIMITER CLK1_2_TPTC2_RD_BW_LIMITER CLK1_2_TPTC1_WR_BW_LIMITER CLK1_2_TPTC2_WR_BW_LIMITER CLK1_2_VPE_P2_BW_LIMITER CLK1_2_VPE_P1_BW_LIMITER CLK1_2_MMU1_BW_LIMITER CLK1_2_BB2D_P1_BW_LIMITER CLK1_2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEARHISTORY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0
0	CLEARHISTORY	Write a 1 clear the traffic counter Type: Give_AutoCleared. Reset value: 0x0.	RW	0

Table 14-237. Register Call Summary for Register L3_BW_LIMITER_CLEARHISTORY

L3_MAIN Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN Bandwidth Limiter Register Summary and Description: [1] [2] [3] [4]

14.2.5.1.9 L3_MAIN STATCOLL Register Summary and Description

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-238. STATCOLL Instance Summary

Module Name	Base Address	Size
CLK2_FLAGMUX_STATCOLL	0x4500 0500	512 bytes
CLK2_STATCOLL0	0x4500 1000	512 bytes
CLK2_STATCOLL1	0x4500 2000	512 bytes
CLK2_STATCOLL2	0x4500 3000	512 bytes

Table 14-238. STATCOLL Instance Summary (continued)

Module Name	Base Address	Size
CLK2_STATCOLL3	0x4500 4000	512 bytes
CLK2_STATCOLL4	0x4500 5000	512 bytes
CLK2_STATCOLL5	0x4500 6000	512 bytes
CLK2_STATCOLL6	0x4500 7000	512 bytes
CLK2_STATCOLL7	0x4500 8000	512 bytes
CLK2_STATCOLL8	0x4500 9000	512 bytes
CLK2_STATCOLL9	0x4500 A000	512 bytes

14.2.5.1.9.1 L3_MAIN STATCOLL Register Summary

Table 14-239. STATCOLL Register Summary

Register Name	Type	Register Width (bits)	Address offset for FIAGMUX	CLK2_FLAGMUX_STATCOLL L3_MAIN Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 0500	0x4500 0500
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 0504	0x4500 0504
L3_STCOL_MASK0	RW	32	0x0100 0508	0x4500 0508
L3_STCOL_REGERR0	R	32	0x0100 050C	0x4500 050C

Table 14-240. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL0 L3_MAIN Physical Address	CLK2_STATCOLL1 L3_MAIN Physical Address	CLK2_STATCOLL 2 L3_MAIN Physical Address	CLK2_STATCOLL3 L3_MAIN Physical Address	CLK2_STATCOLL4 L3_MAIN Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4500 1 000	0x4500 2000	0x4500 3000	0x4500 4000	0x4500 5000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4500 1004	0x4500 2004	0x4500 3004	0x4500 4004	0x4500 5004
L3_STCOL_EN	RW	32	0x0000 0008	0x4500 1008	0x4500 2008	0x4500 3008	0x4500 4008	0x4500 5008
L3_STCOL_SOFTEN	RW	32	0x0000 000C	0x4500 100C	0x4500 200C	0x4500 300C	0x4500 400C	0x4500 500C
L3_STCOL_IGNORESUSPEND	RW	32	0x0000 0010	0x4500 1010	0x4500 2010	0x4500 3010	0x4500 4010	0x4500 5010
L3_STCOL_TRIGEN	RW	32	0x0000 0014	0x4500 1014	0x4500 2014	0x4500 3014	0x4500 4014	0x4500 5014
L3_STCOL_REQEVT	RW	32	0x0000 0018	0x4500 1018	0x4500 2018	0x4500 3018	0x4500 4018	0x4500 5018
L3_STCOL_RSPEVT	RW	32	0x0000 001C	0x4500 101C	0x4500 201C	0x4500 301C	0x4500 401C	0x4500 501C
L3_STCOL_EVTMUX_SEL0	RW	32	0x0000 0020	0x45001020	0x4500 2020	0x4500 3020	0x4500 4020	0x4500 5020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0000 0024	0x4500 1024	0x4500 2024	0x4500 3024	0x4500 4024	0x4500 5024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0000 0028	0x4500 1028	0x4500 2028	0x4500 3028	0x4500 4028	0x4500 5028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0000 002C	0x4500 102C	0x4500 202C	0x4500 302C	0x4500 402C	0x4500 502C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0000 0030	0x4500 1030	0x4500 2030	N/A	0x4500 4030	N/A
L3_STCOL_EVTMUX_SEL5	RW	32	0x0000 0034	0x4500 1034	0x4500 2034	N/A	0x4500 4034	N/A
L3_STCOL_EVTMUX_SEL6	RW	32	0x0000 0038	0x4500 1038	N/A	N/A	0x4500 4038	N/A
L3_STCOL_EVTMUX_SEL7	RW	32	0x0000 003C	0x4500 103C	N/A	N/A	0x4500 403C	N/A
L3_STCOL_DUMP_IDENTIFIER	R	32	0x0000 0040	0x4500 1040	0x4500 2040	0x4500 3040	0x4500 4040	0x4500 5040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x0000 0044	0x4500 1044	0x4500 2044	0x4500 3044	0x4500 4044	0x4500 5044
L3_STCOL_DUMP_SLVADDR	R	32	0x0000 0048	0x4500 1048	0x4500 2048	0x4500 3048	0x4500 4048	0x4500 5048
L3_STCOL_DUMP_MSTADDR	R	32	0x0000 004C	0x4500 104C	0x4500 204C	0x4500 304C	0x4500 404C	0x4500 504C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0000 0050	0x4500 1050	0x4500 2050	0x4500 3050	0x4500 4050	0x4500 5050
L3_STCOL_DUMP_MODE	RW	32	0x0000 0054	0x4500 1054	0x4500 2054	0x4500 3054	0x4500 4054	0x4500 5054
L3_STCOL_DUMP_SEND	RW	32	0x0000 0058	0x4500 1058	0x4500 2058	0x4500 3058	0x4500 4058	0x4500 5058
L3_STCOL_DUMP_DISABLE	RW	32	0x0000 005C	0x4500 105C	0x4500 205C	0x4500 305C	0x4500 405C	0x4500 505C
L3_STCOL_DUMP_ALARM_TRIG	RW	32	0x0000 0060	0x4500 1060	0x4500 2060	0x4500 3060	0x4500 4060	0x4500 5060
L3_STCOL_DUMP_ALARM_MINVAL	RW	32	0x0000 0064	0x4500 1064	0x4500 2064	0x4500 3064	0x4500 4064	0x4500 5064
L3_STCOL_DUMP_ALARM_MAXVAL	RW	32	0x0000 0068	0x4500 1068	0x4500 2068	0x4500 3068	0x4500 4068	0x4500 5068
L3_STCOL_DUMP_ALARM_MODE0	RW	32	0x0000 006C	0x4500 106C	0x4500 206C	0x4500 306C	0x4500 406C	0x4500 506C
L3_STCOL_DUMP_ALARM_MODE1	RW	32	0x0000 0070	0x4500 1070	0x4500 2070	0x4500 3070	0x4500 4070	0x4500 5070
L3_STCOL_DUMP_ALARM_MODE2	RW	32	0x0000 0074	0x4500 1074	0x4500 2074	0x4500 3074	0x4500 4074	0x4500 5074
L3_STCOL_DUMP_ALARM_MODE3	RW	32	0x0000 0078	0x4500 1078	0x4500 2078	0x4500 3078	0x4500 4078	0x4500 5078

Table 14-240. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL0 L3_MAIN Physical Address	CLK2_STATCOLL1 L3_MAIN Physical Address	CLK2_STATCOLL2 L3_MAIN Physical Address	CLK2_STATCOLL3 L3_MAIN Physical Address	CLK2_STATCOLL4 L3_MAIN Physical Address
L3_STCOL_DUMP_ALARM_MODE4	RW	32	0x0000 007C	0x4500 107C	0x4500 207C	N/A	0x4500 407C	N/A
L3_STCOL_DUMP_ALARM_MODE5	RW	32	0x0000 0080	0x4500 1080	0x4500 2080	N/A	0x4500 4080	N/A
L3_STCOL_DUMP_ALARM_MODE6	RW	32	0x0000 0084	0x4500 1084	N/A	N/A	0x4500 4084	N/A
L3_STCOL_DUMP_ALARM_MODE7	RW	32	0x0000 0088	0x4500 1088	N/A	N/A	0x4500 4088	N/A
L3_STCOL_DUMP_CNT0	R	32	0x0000 008C	0x4500 108C	0x4500 208C	0x4500 308C	0x4500 408C	0x4500 508C
L3_STCOL_DUMP_CNT1	R	32	0x0000 0090	0x4500 1090	0x4500 2090	0x4500 3090	0x4500 4090	0x4500 5090
L3_STCOL_DUMP_CNT2	R	32	0x0000 0094	0x4500 1094	0x4500 2094	0x4500 3094	0x4500 4094	0x4500 5094
L3_STCOL_DUMP_CNT3	R	32	0x0000 0098	0x4500 1098	0x4500 2098	0x4500 3098	0x4500 4098	0x4500 5098
L3_STCOL_DUMP_CNT4	R	32	0x0000 009C	0x4500 109C	0x4500 209C	N/A	0x4500 409C	N/A
L3_STCOL_DUMP_CNT5	R	32	0x0000 00A0	0x4500 10A0	0x4500 20A0	N/A	0x4500 40A0	N/A
L3_STCOL_DUMP_CNT6	R	32	0x0000 00A4	0x4500 10A4	N/A	N/A	0x4500 40A4	N/A
L3_STCOL_DUMP_CNT7	R	32	0x0000 00A8	0x4500 10A8	N/A	N/A	0x4500 40A8	N/A
L3_STCOL_FILTER_i_GLOBALEN (1)	RW	32	0x0000 00AC + (0x158*i)	0x4500 10AC + (0x158*i)	0x4500 20AC + (0x158*i)	0x4500 30AC + (0x158*i)	0x4500 40AC + (0x158*i)	0x4500 50AC + (0x158*i)
L3_STCOL_FILTER_i_ADDRMIN(1)	RW	32	0x0000 00B0 + (0x158*i)	0x4500 10B0 + (0x158*i)	0x4500 20B0 + (0x158*i)	0x4500 30B0 + (0x158*i)	0x4500 40B0 + (0x158*i)	0x4500 50B0 + (0x158*i)
L3_STCOL_FILTER_i_ADDRMAX(1)	RW	32	0x0000 00B4 + (0x158*i)	0x4500 10B4 + (0x158*i)	0x4500 20B4 + (0x158*i)	0x4500 30B4 + (0x158*i)	0x4500 40B4 + (0x158*i)	0x4500 50B4 + (0x158*i)
L3_STCOL_FILTER_i_ADDREN(1)	RW	32	0x0000 00B8 + (0x158*i)	0x4500 10B8 + (0x158*i)	0x4500 20B8 + (0x158*i)	0x4500 30B8 + (0x158*i)	0x4500 40B8 + (0x158*i)	0x4500 50B8 + (0x158*i)
L3_STCOL_FILTER_i_EN_k (1)(2)	RW	32	0x0000 00BC + (0x158*i) + (0x44*k)	0x4500 10BC + (0x158*i) + (0x44*k)	0x4500 20BC + (0x158*i) + (0x44*k)	0x4500 30BC + (0x158*i) + (0x44*k)	0x4500 40BC + (0x158*i) + (0x44*k)	0x4500 50BC + (0x158*i) + (0x44*k)

(1) i = 0 to 7 for CLK2_STATCOLL0
i = 0 to 5 for CLK2_STATCOLL1
i = 0 to 3 for CLK2_STATCOLL2
i = 0 to 7 for CLK2_STATCOLL3
i = 0 to 3 for CLK2_STATCOLL4

(2) k = 0 to 1 for CLK2_STATCOLL0
k = 0 for CLK2_STATCOLL1
k = 0 for CLK2_STATCOLL2
k = 0 for CLK2_STATCOLL3
k = 0 for CLK2_STATCOLL4

Table 14-240. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL0 L3_MAIN Physical Address	CLK2_STATCOLL1 L3_MAIN Physical Address	CLK2_STATCOLL 2 L3_MAIN Physical Address	CLK2_STATCOLL3 L3_MAIN Physical Address	CLK2_STATCOLL4 L3_MAIN Physical Address
L3_STCOL_FILTER_i_MASK_m_RD (3)(4)	RW	32	0x0000 00C0 + (0x158*i) + (0x44*m)	0x4500 10C0 + (0x158*i) + (0x44*m)	0x4500 20C0 + (0x158*i) + (0x44*m)	0x4500 30C0 + (0x158*i) + (0x44*m)	0x4500 40C0 + (0x158*i) + (0x44*m)	0x4500 50C0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_WR (3)(4)	RW	32	0x0000 00C4 + (0x158*i) + (0x44*m)	0x4500 10C4 + (0x158*i) + (0x44*m)	0x4500 20C4 + (0x158*i) + (0x44*m)	0x4500 30C4 + (0x158*i) + (0x44*m)	0x4500 40C4 + (0x158*i) + (0x44*m)	0x4500 50C4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_MSTADDR (3)(4)	RW	32	0x0000 00C8 + (0x158*i) + (0x44*m)	0x4500 10C8 + (0x158*i) + (0x44*m)	0x4500 20C8 + (0x158*i) + (0x44*m)	0x4500 30C8 + (0x158*i) + (0x44*m)	0x4500 40C8 + (0x158*i) + (0x44*m)	0x4500 50C8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_SLVADDR (3)(4)	RW	32	0x0000 00CC + (0x158*i) + (0x44*m)	N/A	0x4500 20CC + (0x158*i) + (0x44*m)	0x4500 30CC + (0x158*i) + (0x44*m)	0x4500 40CC + (0x158*i) + (0x44*m)	0x4500 50CC + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_ERR (3)(4)	RW	32	0x0000 00D0 + (0x158*i) + (0x44*m)	0x4500 10D0 + (0x158*i) + (0x44*m)	0x4500 20D0 + (0x158*i) + (0x44*m)	0x4500 30D0 + (0x158*i) + (0x44*m)	0x4500 40D0 + (0x158*i) + (0x44*m)	0x4500 50D0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_USERINFO (3)(4)	RW	32	0x0000 00D4 + (0x158*i) + (0x44*m)	0x4500 10D4 + (0x158*i) + (0x44*m)	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MASK_m_REQUSERINFO (3)(4)	RW	32	0x0000 00D4 + (0x158*i) + (0x44*m)	N/A	0x4500 20D4 + (0x158*i) + (0x44*m)	0x4500 30D4 + (0x158*i) + (0x44*m)	0x4500 40D4 + (0x158*i) + (0x44*m)	0x4500 50D4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO (3)(4)	RW	32	0x0000 00D8 + (0x158*i) + (0x44*m)	N/A	0x4500 20D8 + (0x158*i) + (0x44*m)	0x4500 30D8 + (0x158*i) + (0x44*m)	0x4500 40D8 + (0x158*i) + (0x44*m)	0x4500 50D8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_RD (3)(4)	RW	32	0x0000 00E0 + (0x158*i) + (0x44*m)	0x4500 10E0 + (0x158*i) + (0x44*m)	0x4500 20E0 + (0x158*i) + (0x44*m)	0x4500 30E0 + (0x158*i) + (0x44*m)	0x4500 40E0 + (0x158*i) + (0x44*m)	0x4500 50E0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_WR (3)(4)	RW	32	0x0000 00E4 + (0x158*i) + (0x44*m)	0x4500 10E4 + (0x158*i) + (0x44*m)	0x4500 20E4 + (0x158*i) + (0x44*m)	0x4500 30E4 + (0x158*i) + (0x44*m)	0x4500 40E4 + (0x158*i) + (0x44*m)	0x4500 50E4 + (0x158*i) + (0x44*m)

(3) i = 0 to 7 for CLK2_STATCOLL0
i = 0 to 5 for CLK2_STATCOLL1
i = 0 to 3 for CLK2_STATCOLL2
i = 0 to 7 for CLK2_STATCOLL3
i = 0 to 3 for CLK2_STATCOLL4

(4) m = 0 to 1 for CLK2_STATCOLL0
m = 0 for CLK2_STATCOLL1
m = 0 for CLK2_STATCOLL2
m = 0 for CLK2_STATCOLL3
m = 0 for CLK2_STATCOLL4

Table 14-240. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL0 L3_MAIN Physical Address	CLK2_STATCOLL1 L3_MAIN Physical Address	CLK2_STATCOLL 2 L3_MAIN Physical Address	CLK2_STATCOLL3 L3_MAIN Physical Address	CLK2_STATCOLL4 L3_MAIN Physical Address
L3_STCOL_FILTER_i_MATCH_m_MSTADDR [3][4]	RW	32	0x0000 00E8 + (0x158*i) + (0x44*m)	0x4500 10E8 + (0x158*i) + (0x44*m)	0x4500 20E8 + (0x158*i) + (0x44*m)	0x4500 30E8 + (0x158*i) + (0x44*m)	0x4500 40E8 + (0x158*i) + (0x44*m)	0x4500 50E8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_SLVADDR [3][4]	RW	32	0x0000 00EC + (0x158*i) + (0x44*m)	N/A	0x4500 20EC + (0x158*i) + (0x44*m)	0x4500 30EC + (0x158*i) + (0x44*m)	0x4500 40EC + (0x158*i) + (0x44*m)	0x4500 50EC + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_ERR [3][4]	RW	32	0x0000 00F0 + (0x158*i) + (0x44*m)	0x4500 10F0 + (0x158*i) + (0x44*m)	0x4500 20F0 + (0x158*i) + (0x44*m)	0x4500 30F0 + (0x158*i) + (0x44*m)	0x4500 40F0 + (0x158*i) + (0x44*m)	0x4500 50F0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_USERINFO [3][4]	RW	32	0x0000 00F4+ (0x158*i) + (0x44*m)	0x4500 10F4 + (0x158*i) + (0x44*m)	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO [3][4]	RW	32	0x0000 00F4 + (0x158*i) + (0x44*m)	N/A	0x4500 20F4 + (0x158*i) + (0x44*m)	0x4500 30F4 + (0x158*i) + (0x44*m)	0x4500 40F4 + (0x158*i) + (0x44*m)	0x4500 50F4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO [5][6]	RW	32	0x0000 00F8 + (0x158*i) + (0x44*m)	N/A	0x4500 20F8 + (0x158*i) + (0x44*m)	0x4500 30F8 + (0x158*i) + (0x44*m)	0x4500 40F8 + (0x158*i) + (0x44*m)	0x4500 50F8 + (0x158*i) + (0x44*m)
L3_STCOL_OP_i_THRESHOLD_MINVAL [5]	RW	32	0x0000 01F0 + (0x158*i)	0x4500 11F0 + (0x158*i)	0x4500 21F0 + (0x158*i)	0x4500 31F0 + (0x158*i)	0x4500 41F0 + (0x158*i)	0x4500 51F0 + (0x158*i)
L3_STCOL_OP_i_THRESHOLD_MAXVAL [5]	RW	32	0x0000 01F4 + (0x158*i)	0x4500 11F4 + (0x158*i)	0x4500 21F4 + (0x158*i)	0x4500 31F4 + (0x158*i)	0x4500 41F4 + (0x158*i)	0x4500 51F4 + (0x158*i)
L3_STCOL_OP_i_EVTINFOSEL [5]	RW	32	0x0000 01F8 + (0x158*i)	0x4500 11F8 + (0x158*i)	0x4500 21F8 + (0x158*i)	0x4500 31F8 + (0x158*i)	0x4500 41F8 + (0x158*i)	0x4500 51F8 + (0x158*i)
L3_STCOL_OP_i_SEL [5]	RW	32	0x0000 01FC + (0x158*i)	0x4500 11FC + (0x158*i)	0x4500 21FC + (0x158*i)	0x4500 31FC + (0x158*i)	0x4500 41FC + (0x158*i)	0x4500 51FC + (0x158*i)

(5) i = 0 to 7 for CLK2_STATCOLL0
i = 0 to 5 for CLK2_STATCOLL1
i = 0 to 3 for CLK2_STATCOLL2
i = 0 to 7 for CLK2_STATCOLL3
i = 0 to 3 for CLK2_STATCOLL4

(6) m = 0 to 1 for CLK2_STATCOLL0
m = 0 for CLK2_STATCOLL1
m = 0 for CLK2_STATCOLL2
m = 0 for CLK2_STATCOLL3
m = 0 for CLK2_STATCOLL4

Table 14-241. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL5 L3_MAIN Physical Address	CLK2_STATCOLL6 L3_MAIN Physical Address	CLK2_STATCOLL 7 L3_MAIN Physical Address	CLK2_STATCOLL8 L3_MAIN Physical Address	CLK2_STATCOLL9 L3_MAIN Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4500 6000	0x4500 7000	0x4500 8000	0x4500 9000	0x4500 A000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4500 6004	0x4500 7004	0x4500 8004	0x4500 9004	0x4500 A004
L3_STCOL_EN	RW	32	0x0000 0008	0x4500 61008	0x4500 7008	0x4500 8008	0x4500 9008	0x4500 A008
L3_STCOL_SOFTEN	RW	32	0x0000 000C	0x4500 600C	0x4500 700C	0x4500 800C	0x4500 900C	0x4500 A00C
L3_STCOL_IGNORESUSPEND	RW	32	0x0000 0010	0x4500 6010	0x4500 7010	0x4500 8010	0x4500 9010	0x4500 A010
L3_STCOL_TRIGEN	RW	32	0x0000 0014	0x4500 6014	0x4500 7014	0x4500 8014	0x4500 9014	0x4500 A014
L3_STCOL_REQEVT	RW	32	0x0000 0018	0x4500 6018	0x4500 7018	0x4500 8018	0x4500 9018	0x4500 A018
L3_STCOL_RSPEVT	RW	32	0x0000 001C	0x4500 601C	0x4500 701C	0x4500 801C	0x4500 901C	0x4500 A01C
L3_STCOL_EVTMUX_SEL0	RW	32	0x0000 0020	0x4500 6020	0x4500 7020	0x4500 8020	0x4500 9020	0x4500 A020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0000 0024	0x4500 6024	0x4500 7024	0x4500 8024	0x4500 9024	0x4500 A024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0000 0028	0x4500 6028	0x4500 7028	0x4500 8028	0x4500 9028	0x4500 A028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0000 002C	0x4500 602C	0x4500 702C	0x4500 802C	0x4500 902C	0x4500 A02C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0000 0030	N/A	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL5	RW	32	0x0000 0034	N/A	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL6	RW	32	0x0000 0038	N/A	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL7	RW	32	0x0000 003C	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_IDENTIFIER	R	32	0x0000 0040	0x4500 6040	0x4500 7040	0x4500 8040	0x4500 9040	0x4500 A040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x0000 0044	0x4500 6044	0x4500 7044	0x4500 8044	0x4500 9044	0x4500 A044
L3_STCOL_DUMP_SLVADDR	R	32	0x0000 0048	0x4500 6048	0x4500 7048	0x4500 8048	0x4500 9048	0x4500 A048
L3_STCOL_DUMP_MSTADDR	R	32	0x0000 004C	0x4500 604C	0x4500 704C	0x4500 804C	0x4500 904C	0x4500 A04C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0000 0050	0x4500 6050	0x4500 7050	0x4500 8050	0x4500 9050	0x4500 A050
L3_STCOL_DUMP_MODE	RW	32	0x0000 0054	0x4500 6054	0x4500 7054	0x4500 8054	0x4500 9054	0x4500 A054
L3_STCOL_DUMP_SEND	RW	32	0x0000 0058	0x4500 6058	0x4500 7058	0x4500 8058	0x4500 9058	0x4500 A058
L3_STCOL_DUMP_DISABLE	RW	32	0x0000 005C	0x4500 605C	0x4500 705C	0x4500 805C	0x4500 905C	0x4500 A05C
L3_STCOL_DUMP_ALARM_TRIG	RW	32	0x0000 0060	0x4500 6060	0x4500 7060	0x4500 8060	0x4500 9060	0x4500 A060
L3_STCOL_DUMP_ALARM_MINVAL	RW	32	0x0000 0064	0x4500 6064	0x4500 7064	0x4500 8064	0x4500 9064	0x4500 A064
L3_STCOL_DUMP_ALARM_MAXVAL	RW	32	0x0000 0068	0x4500 6068	0x4500 7068	0x4500 8068	0x4500 9068	0x4500 A068
L3_STCOL_DUMP_ALARM_MODE0	RW	32	0x0000 006C	0x4500 606C	0x4500 706C	0x4500 806C	0x4500 906C	0x4500 A06C
L3_STCOL_DUMP_ALARM_MODE1	RW	32	0x0000 0070	0x4500 6070	0x4500 7070	0x4500 8070	0x4500 9070	0x4500 A070
L3_STCOL_DUMP_ALARM_MODE2	RW	32	0x0000 0074	0x4500 6074	0x4500 7074	0x4500 8074	0x4500 9074	0x4500 A074
L3_STCOL_DUMP_ALARM_MODE3	RW	32	0x0000 0078	0x4500 6078	0x4500 7078	0x4500 8078	0x4500 9078	0x4500 A078

Table 14-241. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL5 L3_MAIN Physical Address	CLK2_STATCOLL6 L3_MAIN Physical Address	CLK2_STATCOLL 7 L3_MAIN Physical Address	CLK2_STATCOLL8 L3_MAIN Physical Address	CLK2_STATCOLL9 L3_MAIN Physical Address
L3_STCOL_DUMP_ALARM_MODE4	RW	32	0x0000 007C	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE5	RW	32	0x0000 0080	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE6	RW	32	0x0000 0084	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE7	RW	32	0x0000 0088	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT0	R	32	0x0000 008C	0x4500 608C	0x4500 708C	0x4500 808C	0x4500 908C	0x4500 A08C
L3_STCOL_DUMP_CNT1	R	32	0x0000 0090	0x4500 6090	0x4500 7090	0x4500 8090	0x4500 9090	0x4500 A090
L3_STCOL_DUMP_CNT2	R	32	0x0000 0094	0x4500 6094	0x4500 7094	0x4500 8094	0x4500 9094	0x4500 A094
L3_STCOL_DUMP_CNT3	R	32	0x0000 0098	0x4500 6098	0x4500 7098	0x4500 8098	0x4500 9098	0x4500 A098
L3_STCOL_DUMP_CNT4	R	32	0x0000 009C	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT5	R	32	0x0000 00A0	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT6	R	32	0x0000 00A4	N/A	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT7	R	32	0x0000 00A8	N/A	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_GLOBALEN (1)	RW	32	0x0000 00AC + (0x158*i)	0x4500 60AC + (0x158*i)	0x4500 70AC + (0x158*i)	0x4500 80AC + (0x158*i)	0x4500 90AC + (0x158*i)	0x4500 A0AC + (0x158*i)
L3_STCOL_FILTER_i_ADDRMIN(1)	RW	32	0x0000 00B0 + (0x158*i)	0x4500 60B0 + (0x158*i)	0x4500 70B0 + (0x158*i)	0x4500 80B0 + (0x158*i)	0x4500 90B0 + (0x158*i)	0x4500 A0B0 + (0x158*i)
L3_STCOL_FILTER_i_ADDRMAX(1)	RW	32	0x0000 00B4 + (0x158*i)	0x4500 60B4 + (0x158*i)	0x4500 70B4 + (0x158*i)	0x4500 80B4 + (0x158*i)	0x4500 90B4 + (0x158*i)	0x4500 A0B4 + (0x158*i)
L3_STCOL_FILTER_i_ADDREN(1)	RW	32	0x0000 00B8 + (0x158*i)	0x4500 60B8 + (0x158*i)	0x4500 70B8 + (0x158*i)	0x4500 80B8 + (0x158*i)	0x4500 90B8 + (0x158*i)	0x4500 A0B8 + (0x158*i)
L3_STCOL_FILTER_i_EN_k (1)(2)	RW	32	0x0000 00BC + (0x158*i) + (0x44*k)	0x4500 60BC + (0x158*i) + (0x44*k)	0x4500 70BC + (0x158*i) + (0x44*k)	0x4500 80BC + (0x158*i) + (0x44*k)	0x4500 90BC + (0x158*i) + (0x44*k)	0x4500 A0BC + (0x158*i) + (0x44*k)

(1) i = 0 to 3 for CLK2_STATCOLL5
i = 0 to 3 for CLK2_STATCOLL6
i = 0 to 3 for CLK2_STATCOLL7
i = 0 to 3 for CLK2_STATCOLL8
i = 0 to 3 for CLK2_STATCOLL9

(2) k = 0 for CLK2_STATCOLL5
k = 0 for CLK2_STATCOLL6
k = 0 for CLK2_STATCOLL7
k = 0 for CLK2_STATCOLL8
k = 0 for CLK2_STATCOLL9

Table 14-241. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL5 L3_MAIN Physical Address	CLK2_STATCOLL6 L3_MAIN Physical Address	CLK2_STATCOLL7 L3_MAIN Physical Address	CLK2_STATCOLL8 L3_MAIN Physical Address	CLK2_STATCOLL9 L3_MAIN Physical Address
L3_STCOL_FILTER_i_MASK_m_RD[3][4]	RW	32	0x0000 00C0 + (0x158*i) + (0x44*m)	0x4500 60C0 + (0x158*i) + (0x44*m)	0x4500 70C0 + (0x158*i) + (0x44*m)	0x4500 80C0 + (0x158*i) + (0x44*m)	0x4500 90C0 + (0x158*i) + (0x44*m)	0x4500 A0C0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_WR[3][4]	RW	32	0x0000 00C4 + (0x158*i) + (0x44*m)	0x4500 60C4 + (0x158*i) + (0x44*m)	0x4500 70C4 + (0x158*i) + (0x44*m)	0x4500 80C4 + (0x158*i) + (0x44*m)	0x4500 90C4 + (0x158*i) + (0x44*m)	0x4500 A0C4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_MSTADDR[3][4]	RW	32	0x0000 00C8 + (0x158*i) + (0x44*m)	0x4500 60C8 + (0x158*i) + (0x44*m)	0x4500 70C8 + (0x158*i) + (0x44*m)	0x4500 80C8 + (0x158*i) + (0x44*m)	0x4500 90C8 + (0x158*i) + (0x44*m)	0x4500 A0C8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_SLVADDR[3][4]	RW	32	0x0000 00CC + (0x158*i) + (0x44*m)	0x4500 60CC + (0x158*i) + (0x44*m)	0x4500 70CC + (0x158*i) + (0x44*m)	0x4500 80CC + (0x158*i) + (0x44*m)	0x4500 90CC + (0x158*i) + (0x44*m)	0x4500 A0CC + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_ERR[3][4]	RW	32	0x0000 00D0 + (0x158*i) + (0x44*m)	0x4500 60D0 + (0x158*i) + (0x44*m)	0x4500 70D0 + (0x158*i) + (0x44*m)	0x4500 80D0 + (0x158*i) + (0x44*m)	0x4500 90D0 + (0x158*i) + (0x44*m)	0x4500 A0D0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_USERINFO[3][4]	RW	32	0x0000 00D4 + (0x158*i) + (0x44*m)	N/A	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MASK_m_REQUSERINFO[3][4]	RW	32	0x0000 00D4 + (0x158*i) + (0x44*m)	0x4500 60D4 + (0x158*i) + (0x44*m)	0x4500 70D4 + (0x158*i) + (0x44*m)	0x4500 80D4 + (0x158*i) + (0x44*m)	0x4500 90D4 + (0x158*i) + (0x44*m)	0x4500 A0D4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO[3][4]	RW	32	0x0000 00D8 + (0x158*i) + (0x44*m)	0x4500 60D8 + (0x158*i) + (0x44*m)	0x4500 70D8 + (0x158*i) + (0x44*m)	0x4500 80D8 + (0x158*i) + (0x44*m)	0x4500 90D8 + (0x158*i) + (0x44*m)	0x4500 A0D8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_RD[3][4]	RW	32	0x0000 00E0 + (0x158*i) + (0x44*m)	0x4500 60E0 + (0x158*i) + (0x44*m)	0x4500 70E0 + (0x158*i) + (0x44*m)	0x4500 80E0 + (0x158*i) + (0x44*m)	0x4500 90E0 + (0x158*i) + (0x44*m)	0x4500 A0E0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_WR[3][4]	RW	32	0x0000 00E4 + (0x158*i) + (0x44*m)	0x4500 60E4 + (0x158*i) + (0x44*m)	0x4500 70E4 + (0x158*i) + (0x44*m)	0x4500 80E4 + (0x158*i) + (0x44*m)	0x4500 90E4 + (0x158*i) + (0x44*m)	0x4500 A0E4 + (0x158*i) + (0x44*m)

(3) i = 0 to 3 for CLK2_STATCOLL5
i = 0 to 3 for CLK2_STATCOLL6
i = 0 to 3 for CLK2_STATCOLL7
i = 0 to 3 for CLK2_STATCOLL8
i = 0 to 3 for CLK2_STATCOLL9

(4) m = 0 for CLK2_STATCOLL5
m = 0 for CLK2_STATCOLL6
m = 0 for CLK2_STATCOLL7
m = 0 for CLK2_STATCOLL8
m = 0 for CLK2_STATCOLL9

Table 14-241. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK2_STATCOLL5 L3_MAIN Physical Address	CLK2_STATCOLL6 L3_MAIN Physical Address	CLK2_STATCOLL 7 L3_MAIN Physical Address	CLK2_STATCOLL8 L3_MAIN Physical Address	CLK2_STATCOLL9 L3_MAIN Physical Address
L3_STCOL_FILTER_i_MATCH_m_MSTADDR (3)(4)	RW	32	0x0000 00E8 + (0x158*i) + (0x44*m)	0x4500 60E8 + (0x158*i) + (0x44*m)	0x4500 70E8 + (0x158*i) + (0x44*m)	0x4500 80E8 + (0x158*i) + (0x44*m)	0x4500 90E8 + (0x158*i) + (0x44*m)	0x4500 A0E8 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_SLVADDR (3)(4)	RW	32	0x0000 00EC + (0x158*i) + (0x44*m)	0x4500 60EC + (0x158*i) + (0x44*m)	0x4500 70EC + (0x158*i) + (0x44*m)	0x4500 80EC + (0x158*i) + (0x44*m)	0x4500 90EC + (0x158*i) + (0x44*m)	0x4500 A0EC + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_ERR (3)(4)	RW	32	0x0000 00F0 + (0x158*i) + (0x44*m)	0x4500 60F0 + (0x158*i) + (0x44*m)	0x4500 70F0 + (0x158*i) + (0x44*m)	0x4500 80F0 + (0x158*i) + (0x44*m)	0x4500 90F0 + (0x158*i) + (0x44*m)	0x4500 A0F0 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_USERINFO (3)(4)	RW	32	0x0000 00F4+ (0x158*i) + (0x44*m)	N/A	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO (3)(4)	RW	32	0x0000 00F4 + (0x158*i) + (0x44*m)	0x4500 260F4 + (0x158*i) + (0x44*m)	0x4500 70F4 + (0x158*i) + (0x44*m)	0x4500 80F4 + (0x158*i) + (0x44*m)	0x4500 90F4 + (0x158*i) + (0x44*m)	0x4500 A0F4 + (0x158*i) + (0x44*m)
L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO (5)(6)	RW	32	0x0000 00F8 + (0x158*i) + (0x44*m)	0x4500 60F8 + (0x158*i) + (0x44*m)	0x4500 70F8 + (0x158*i) + (0x44*m)	0x4500 80F8 + (0x158*i) + (0x44*m)	0x4500 90F8 + (0x158*i) + (0x44*m)	0x4500 A0F8 + (0x158*i) + (0x44*m)
L3_STCOL_OP_i_THRESHOLD_MINVAL (5)	RW	32	0x0000 01F0 + (0x158*i)	0x4500 61F0 + (0x158*i)	0x4500 71F0 + (0x158*i)	0x4500 81F0 + (0x158*i)	0x4500 91F0 + (0x158*i)	0x4500 A1F0 + (0x158*i)
L3_STCOL_OP_i_THRESHOLD_MAXVAL (5)	RW	32	0x0000 01F4 + (0x158*i)	0x4500 61F4 + (0x158*i)	0x4500 71F4 + (0x158*i)	0x4500 81F4 + (0x158*i)	0x4500 91F4 + (0x158*i)	0x4500 A1F4 + (0x158*i)
L3_STCOL_OP_i_EVTINFOSEL (5)	RW	32	0x0000 01F8 + (0x158*i)	0x4500 61F8 + (0x158*i)	0x4500 71F8 + (0x158*i)	0x4500 81F8 + (0x158*i)	0x4500 91F8 + (0x158*i)	0x4500 A1F8 + (0x158*i)
L3_STCOL_OP_i_SEL (5)	RW	32	0x0000 01FC + (0x158*i)	0x4500 61FC + (0x158*i)	0x4500 71FC + (0x158*i)	0x4500 81FC + (0x158*i)	0x4500 91FC + (0x158*i)	0x4500 A1FC + (0x158*i)

(5) i = 0 to 3 for CLK2_STATCOLL5
i = 0 to 3 for CLK2_STATCOLL6
i = 0 to 3 for CLK2_STATCOLL7
i = 0 to 3 for CLK2_STATCOLL8
i = 0 to 3 for CLK2_STATCOLL9

(6) m = 0 for CLK2_STATCOLL5
m = 0 for CLK2_STATCOLL6
m = 0 for CLK2_STATCOLL7
m = 0 for CLK2_STATCOLL8
m = 0 for CLK2_STATCOLL9

14.2.5.1.9.2 L3_MAIN STATCOLL Register Description

Table 14-242. L3_STCOL_STDHOSTHDR_COREREG

Address Offset	See Table 14-240.		
Physical Address	0x4500 0500	**Instance**	CLK2_FLAGMUX_STATCOLL
	0x4500 1 000		CLK2_STATCOLL0
	0x4500 2000		CLK2_STATCOLL1
	0x4500 3000		CLK2_STATCOLL2
	0x4500 4000		CLK2_STATCOLL3
	0x4500 5000		CLK2_STATCOLL4
	0x4500 6000		CLK2_STATCOLL5
	0x4500 7000		CLK2_STATCOLL6
	0x4500 8000		CLK2_STATCOLL7
	0x4500 9000		CLK2_STATCOLL8
	0x4500 A000		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x3A. (When the instance is CLK2_FLAGMUX_STATCOLL reset value is 0x37)	R	0x3A
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R1	1

Table 14-243. Register Call Summary for Register L3_STCOL_STDHOSTHDR_COREREG

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1] [2]

Table 14-244. L3_STCOL_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-240.		
Physical Address	0x4500 0504	**Instance**	CLK2_FLAGMUX_STATCOLL
	0x4500 1004		CLK2_STATCOLL0
	0x4500 2004		CLK2_STATCOLL1
	0x4500 3004		CLK2_STATCOLL2
	0x4500 4004		CLK2_STATCOLL3
	0x4500 5004		CLK2_STATCOLL4
	0x4500 6004		CLK2_STATCOLL5
	0x4500 7004		CLK2_STATCOLL6
	0x4500 8004		CLK2_STATCOLL7
	0x4500 9004		CLK2_STATCOLL8
	0x4500 A004		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x1.	R	0x1
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-245. Register Call Summary for Register L3_STCOL_STDHOSTHDR_VERSIONREG

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1] [2]

Table 14-246. L3_STCOL_MASK0

Address Offset	See Table 14-239.		
Physical Address	0x4500 0508	**Instance**	CLK2_FLAGMUX_STATCOLL
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						MASK0									

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0000 0000
9:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x7.	RW	0x3ff

Table 14-247. Register Call Summary for Register L3_STCOL_MASK0

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0]

Table 14-248. L3_STCOL_REGERR0

Address Offset	See Table 14-239.		
Physical Address	0x4500 050C	**Instance**	CLK2_FLAGMUX_STATCOLL
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REGERR0							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0000 0000
9:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0x0000 0000

Table 14-249. Register Call Summary for Register L3_STCOL_REGERR0

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0]

Table 14-250. L3_STCOL_EN

Address Offset	See Table 14-240.		
Physical Address	0x4500 1008 0x4500 2008 0x4500 3008 0x4500 4008 0x4500 5008 0x4500 61008 0x4500 7008 0x4500 8008 0x4500 9008 0x4500 A008	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	EN	Enable performance monitoring, this will also shut down the clock if En = 0 Type: Control. Reset value: 0x0.	RW	0

Table 14-251. Register Call Summary for Register L3_STCOL_EN

L3_MAIN Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-252. L3_STCOL_SOFTEN

Address Offset	See Table 14-240.		
Physical Address	0x4500 100C	**Instance**	CLK2_STATCOLL0
	0x4500 200C		CLK2_STATCOLL1
	0x4500 300C		CLK2_STATCOLL2
	0x4500 400C		CLK2_STATCOLL3
	0x4500 500C		CLK2_STATCOLL4
	0x4500 600C		CLK2_STATCOLL5
	0x4500 700C		CLK2_STATCOLL6
	0x4500 800C		CLK2_STATCOLL7
	0x4500 900C		CLK2_STATCOLL8
	0x4500 A00C		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SOFTEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SOFTEN	Software enable for performance monitoring Type: Control. Reset value: 0x0.	RW	0

Table 14-253. Register Call Summary for Register L3_STCOL_SOFTEN

L3_MAIN Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-254. L3_STCOL_IGNORESUSPEND

Address Offset	See Table 14-240.		
Physical Address	0x4500 1010	**Instance**	CLK2_STATCOLL0
	0x4500 2010		CLK2_STATCOLL1
	0x4500 3010		CLK2_STATCOLL2
	0x4500 4010		CLK2_STATCOLL3
	0x4500 5010		CLK2_STATCOLL4
	0x4500 6010		CLK2_STATCOLL5
	0x4500 7010		CLK2_STATCOLL6
	0x4500 8010		CLK2_STATCOLL7
	0x4500 9010		CLK2_STATCOLL8
	0x4500 A010		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															IGNORESUSPEND

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	IGNORESUSPEND	Ignore suspend if set to one for suspend mechanism Type: Control. Reset value: 0x0.	RW	0

Table 14-255. Register Call Summary for Register L3_STCOL_IGNORESUSPEND

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-256. L3_STCOL_TRIGEN

Address Offset	See Table 14-240.		
Physical Address	0x4500 1014	**Instance**	CLK2_STATCOLL0
	0x4500 2014		CLK2_STATCOLL1
	0x4500 3014		CLK2_STATCOLL2
	0x4500 4014		CLK2_STATCOLL3
	0x4500 5014		CLK2_STATCOLL4
	0x4500 6014		CLK2_STATCOLL5
	0x4500 7014		CLK2_STATCOLL6
	0x4500 8014		CLK2_STATCOLL7
	0x4500 9014		CLK2_STATCOLL8
	0x4500 A014		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TRIGEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	TRIGEN	TrigEn when set, it enable the external trigger start and stop Type: Control. Reset value: 0x0.	RW	0

Table 14-257. Register Call Summary for Register L3_STCOL_TRIGEN

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-258. L3_STCOL_REQEVT

Address Offset	See Table 14-240.		
Physical Address	0x4500 1018	**Instance**	CLK2_STATCOLL0
	0x4500 2018		CLK2_STATCOLL1
	0x4500 3018		CLK2_STATCOLL2
	0x4500 4018		CLK2_STATCOLL3
	0x4500 5018		CLK2_STATCOLL4
	0x4500 6018		CLK2_STATCOLL5
	0x4500 7018		CLK2_STATCOLL6
	0x4500 8018		CLK2_STATCOLL7
	0x4500 9018		CLK2_STATCOLL8
	0x4500 A018		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												REQEVT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	REQEVT	Req event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring aN NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 14-259. Register Call Summary for Register L3_STCOL_REQEVT

L3_MAIN Interconnect
- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-260. L3_STCOL_RSPEVT

Address Offset	See Table 14-240.		
Physical Address	0x4500 101C	**Instance**	CLK2_STATCOLL0
	0x4500 201C		CLK2_STATCOLL1
	0x4500 301C		CLK2_STATCOLL2
	0x4500 401C		CLK2_STATCOLL3
	0x4500 501C		CLK2_STATCOLL4
	0x4500 601C		CLK2_STATCOLL5
	0x4500 701C		CLK2_STATCOLL6
	0x4500 801C		CLK2_STATCOLL7
	0x4500 901C		CLK2_STATCOLL8
	0x4500 A01C		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RSPEVT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	RSPEVT	Rsp event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring a NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 14-261. Register Call Summary for Register L3_STCOL_RSPEVT

L3_MAIN Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-262. L3_STCOL_EVTMUX_SEL0

Address Offset	See Table 14-240.		
Physical Address	0x45001020 0x4500 2020 0x4500 3020 0x4500 4020 0x4500 5020 0x4500 6020 0x4500 7020 0x4500 8020 0x4500 9020 0x4500 A020	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL0	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL0	The select of the mux 0 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-263. Register Call Summary for Register L3_STCOL_EVTMUX_SEL0

L3_MAIN Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-264. L3_STCOL_EVTMUX_SEL1

Address Offset	See Table 14-240.		
Physical Address	0x4500 1024 0x4500 2024 0x4500 3024 0x4500 4024 0x4500 5024 0x4500 6024 0x4500 7024 0x4500 8024 0x4500 9024 0x4500 A024	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL1	

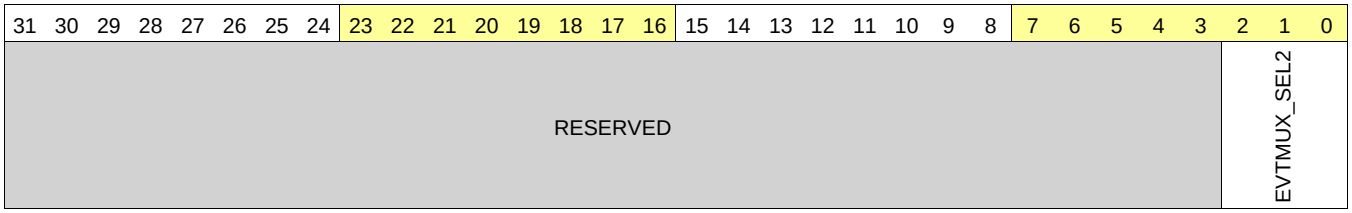
Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL1	The select of the mux 1 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-265. Register Call Summary for Register L3_STCOL_EVTMUX_SEL1

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-266. L3_STCOL_EVTMUX_SEL2

Address Offset	See Table 14-240.		
Physical Address	0x4500 1028	**Instance**	CLK2_STATCOLL0
	0x4500 2028		CLK2_STATCOLL1
	0x4500 3028		CLK2_STATCOLL2
	0x4500 4028		CLK2_STATCOLL3
	0x4500 5028		CLK2_STATCOLL4
	0x4500 6028		CLK2_STATCOLL5
	0x4500 7028		CLK2_STATCOLL6
	0x4500 8028		CLK2_STATCOLL7
	0x4500 9028		CLK2_STATCOLL8
	0x4500 A028		CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL2	The select of the mux 2 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-267. Register Call Summary for Register L3_STCOL_EVTMUX_SEL2

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-268. L3_STCOL_EVTMUX_SEL3

Address Offset	See Table 14-240.		
Physical Address	0x4500 102C 0x4500 202C 0x4500 302C 0x4500 402C 0x4500 502C 0x4500 602C 0x4500 702C 0x4500 802C 0x4500 902C 0x4500 A02C	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL3	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL3	The select of the mux 3 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-269. Register Call Summary for Register L3_STCOL_EVTMUX_SEL3

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-270. L3_STCOL_EVTMUX_SEL4

Address Offset	See Table 14-240.		
Physical Address	0x4500 1030 0x4500 2030 0x4500 4030	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL4	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL4	The select of the mux 4 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-271. Register Call Summary for Register L3_STCOL_EVTMUX_SEL4

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-272. L3_STCOL_EVTMUX_SEL5

Address Offset	See Table 14-240.		
Physical Address	0x4500 1034 0x4500 2034 0x4500 4034	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL5	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL5	The select of the mux 5 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-273. Register Call Summary for Register L3_STCOL_EVTMUX_SEL5

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-274. L3_STCOL_EVTMUX_SEL6

Address Offset	See Table 14-240.		
Physical Address	0x4500 1038 0x4500 4038	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL6	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL6	The select of the mux 6 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-275. Register Call Summary for Register L3_STCOL_EVTMUX_SEL6

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-276. L3_STCOL_EVTMUX_SEL7

Address Offset	See Table 14-240.		
Physical Address	0x4500 103C 0x4500 403C	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL7	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	EVTMUX_SEL7	The select of the mux 7 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-277. Register Call Summary for Register L3_STCOL_EVTMUX_SEL7

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-278. L3_STCOL_DUMP_IDENTIFIER

Address Offset	See Table 14-240.		
Physical Address	0x4500 1040 0x4500 2040 0x4500 3040 0x4500 4040 0x4500 5040 0x4500 6040 0x4500 7040 0x4500 8040 0x4500 9040 0x4500 A040	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DUMP_IDENTIFIER			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	DUMP_IDENTIFIER	Probe identifier Type: Control. Reset value: 0x0.	R	0x0

Table 14-279. Register Call Summary for Register L3_STCOL_DUMP_IDENTIFIER

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-280. L3_STCOL_DUMP_COLLECTTIME

Address Offset	See Table 14-240.		
Physical Address	0x4500 1044	**Instance**	CLK2_STATCOLL0
	0x4500 2044		CLK2_STATCOLL1
	0x4500 3044		CLK2_STATCOLL2
	0x4500 4044		CLK2_STATCOLL3
	0x4500 5044		CLK2_STATCOLL4
	0x4500 6044		CLK2_STATCOLL5
	0x4500 7044		CLK2_STATCOLL6
	0x4500 8044		CLK2_STATCOLL7
	0x4500 9044		CLK2_STATCOLL8
	0x4500 A044		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_COLLECTTIME																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_COLLECTTIME	Number of cycle to wait between two statistics frame Type: Control. Reset value: 0x0.	RW	0x0000

Table 14-281. Register Call Summary for Register L3_STCOL_DUMP_COLLECTTIME

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-282. L3_STCOL_DUMP_SLVADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 1048	**Instance**	CLK2_STATCOLL0
	0x4500 2048		CLK2_STATCOLL1
	0x4500 3048		CLK2_STATCOLL2
	0x4500 4048		CLK2_STATCOLL3
	0x4500 5048		CLK2_STATCOLL4
	0x4500 6048		CLK2_STATCOLL5
	0x4500 7048		CLK2_STATCOLL6
	0x4500 8048		CLK2_STATCOLL7
	0x4500 9048		CLK2_STATCOLL8
	0x4500 A048		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DUMP_SLVADDR							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	DUMP_SLVADDR	Dump slave address Type: Control. Reset value: 0x19.	R	0x19

Table 14-283. Register Call Summary for Register L3_STCOL_DUMP_SLVADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-284. L3_STCOL_DUMP_MSTADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 104C	**Instance**	CLK2_STATCOLL0
	0x4500 204C		CLK2_STATCOLL1
	0x4500 304C		CLK2_STATCOLL2
	0x4500 404C		CLK2_STATCOLL3
	0x4500 504C		CLK2_STATCOLL4
	0x4500 604C		CLK2_STATCOLL5
	0x4500 704C		CLK2_STATCOLL6
	0x4500 804C		CLK2_STATCOLL7
	0x4500 904C		CLK2_STATCOLL8
	0x4500 A04C		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DUMP_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	DUMP_MSTADDR	Dump master address Type: Control. Reset value: 0xE0.	R	0x380

Table 14-285. Register Call Summary for Register L3_STCOL_DUMP_MSTADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-286. L3_STCOL_DUMP_SLVOFS

Address Offset	See Table 14-240.		
Physical Address	0x4500 1050	**Instance**	CLK2_STATCOLL0
	0x4500 2050		CLK2_STATCOLL1
	0x4500 3050		CLK2_STATCOLL2
	0x4500 4050		CLK2_STATCOLL3
	0x4500 5050		CLK2_STATCOLL4
	0x4500 6050		CLK2_STATCOLL5
	0x4500 7050		CLK2_STATCOLL6
	0x4500 8050		CLK2_STATCOLL7
	0x4500 9050		CLK2_STATCOLL8
	0x4500 A050		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_SLVOFS																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_SLVOFS	Dump slave offset Type: Control. Reset value: 0x800.	RW	0x0000 0800

Table 14-287. Register Call Summary for Register L3_STCOL_DUMP_SLVOFS

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-288. L3_STCOL_DUMP_MODE

Address Offset	See Table 14-240.		
Physical Address	0x4500 1054	**Instance**	CLK2_STATCOLL0
	0x4500 2054		CLK2_STATCOLL1
	0x4500 3054		CLK2_STATCOLL2
	0x4500 4054		CLK2_STATCOLL3
	0x4500 5054		CLK2_STATCOLL4
	0x4500 6054		CLK2_STATCOLL5
	0x4500 7054		CLK2_STATCOLL6
	0x4500 8054		CLK2_STATCOLL7
	0x4500 9054		CLK2_STATCOLL8
	0x4500 A054		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_MODE_CONDITIONAL	DUMP_MANUAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	DUMP_MODE_CONDITIONAL	Define the stat conditional dump, if one a dump will be generated when alarm is trigged Type: Control. Reset value: 0x0.	RW	0
0	DUMP_MODE_MANUAL	Define the dump mode: if != 0 the dump is controlled by the Send register. Type: Control. Reset value: 0x0.	RW	0

Table 14-289. Register Call Summary for Register L3_STCOL_DUMP_MODE

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-290. L3_STCOL_DUMP_SEND

Address Offset	See Table 14-240.		
Physical Address	0x4500 1058	**Instance**	CLK2_STATCOLL0
	0x4500 2058		CLK2_STATCOLL1
	0x4500 3058		CLK2_STATCOLL2
	0x4500 4058		CLK2_STATCOLL3
	0x4500 5058		CLK2_STATCOLL4
	0x4500 6058		CLK2_STATCOLL5
	0x4500 7058		CLK2_STATCOLL6
	0x4500 8058		CLK2_STATCOLL7
	0x4500 9058		CLK2_STATCOLL8
	0x4500 A058		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_SEND

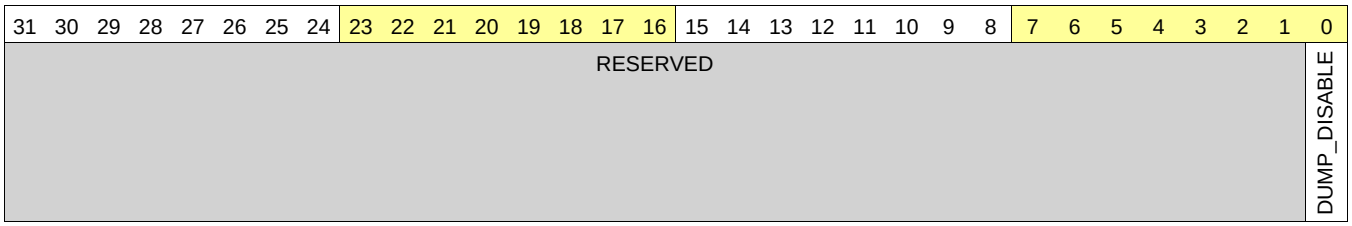
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DUMP_SEND	In manual mode, is used to send the dump content and initialize the counters. Type: Give_AutoCleared. Reset value: 0x0. • Dumping can be performed only if monitoring is enabled • For “one shot metrics dump” the DUMP_SEND command has to be issued before disabling monitoring	RW	0

Table 14-291. Register Call Summary for Register L3_STCOL_DUMP_SEND

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-292. L3_STCOL_DUMP_DISABLE

Address Offset	See Table 14-240.		
Physical Address	0x4500 105C	**Instance**	CLK2_STATCOLL0
	0x4500 205C		CLK2_STATCOLL1
	0x4500 305C		CLK2_STATCOLL2
	0x4500 405C		CLK2_STATCOLL3
	0x4500 505C		CLK2_STATCOLL4
	0x4500 605C		CLK2_STATCOLL5
	0x4500 705C		CLK2_STATCOLL6
	0x4500 805C		CLK2_STATCOLL7
	0x4500 905C		CLK2_STATCOLL8
	0x4500 A05C		CLK2_STATCOLL9
Description			
Type	RW		



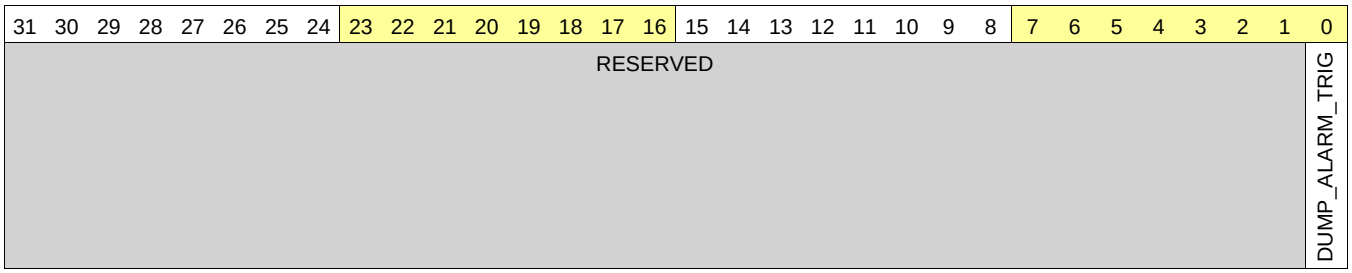
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DUMP_DISABLE	If 1, the dump frame will be disabled, but counters still active.This is typically used when counters monitoring is enabled Type: Control. Reset value: 0x0.	RW	0

Table 14-293. Register Call Summary for Register L3_STCOL_DUMP_DISABLE

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-294. L3_STCOL_DUMP_ALARM_TRIG

Address Offset	See Table 14-240.		
Physical Address	0x4500 1060	**Instance**	CLK2_STATCOLL0
	0x4500 2060		CLK2_STATCOLL1
	0x4500 3060		CLK2_STATCOLL2
	0x4500 4060		CLK2_STATCOLL3
	0x4500 5060		CLK2_STATCOLL4
	0x4500 6060		CLK2_STATCOLL5
	0x4500 7060		CLK2_STATCOLL6
	0x4500 8060		CLK2_STATCOLL7
	0x4500 9060		CLK2_STATCOLL8
	0x4500 A060		CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
0	DUMP_ALARM_TRIG	In Alarm Mode, is used to reset Alarm Type: Take. Reset value: 0x0.	RW	0

Table 14-295. Register Call Summary for Register L3_STCOL_DUMP_ALARM_TRIG

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-296. L3_STCOL_DUMP_ALARM_MINVAL

Address Offset	See Table 14-240.		
Physical Address	0x4500 1064	**Instance**	CLK2_STATCOLL0
	0x4500 2064		CLK2_STATCOLL1
	0x4500 3064		CLK2_STATCOLL2
	0x4500 4064		CLK2_STATCOLL3
	0x4500 5064		CLK2_STATCOLL4
	0x4500 6064		CLK2_STATCOLL5
	0x4500 7064		CLK2_STATCOLL6
	0x4500 8064		CLK2_STATCOLL7
	0x4500 9064		CLK2_STATCOLL8
	0x4500 A064		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_ALARM_MINVAL																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_ALARM_MINVAL	In Alarm Mode, used to trig an alert if any of counter value is less than AlarmMinVal Type: Control. Reset value: 0x0.	RW	0x0000 0000

Table 14-297. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MINVAL

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-298. L3_STCOL_DUMP_ALARM_MAXVAL

Address Offset	See Table 14-240.		
Physical Address	0x4500 1068	**Instance**	CLK2_STATCOLL0
	0x4500 2068		CLK2_STATCOLL1
	0x4500 3068		CLK2_STATCOLL2
	0x4500 4068		CLK2_STATCOLL3
	0x4500 5068		CLK2_STATCOLL4
	0x4500 6068		CLK2_STATCOLL5
	0x4500 7068		CLK2_STATCOLL6
	0x4500 8068		CLK2_STATCOLL7
	0x4500 9068		CLK2_STATCOLL8
	0x4500 A068		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_ALARM_MAXVAL																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_ALARM_MAXVAL	In Alarm Mode, used to trig an alert if any of counter value is larger or equal to AlarmMaxVal Type: Control. Reset value: 0x0.	RW	0x0000 0000

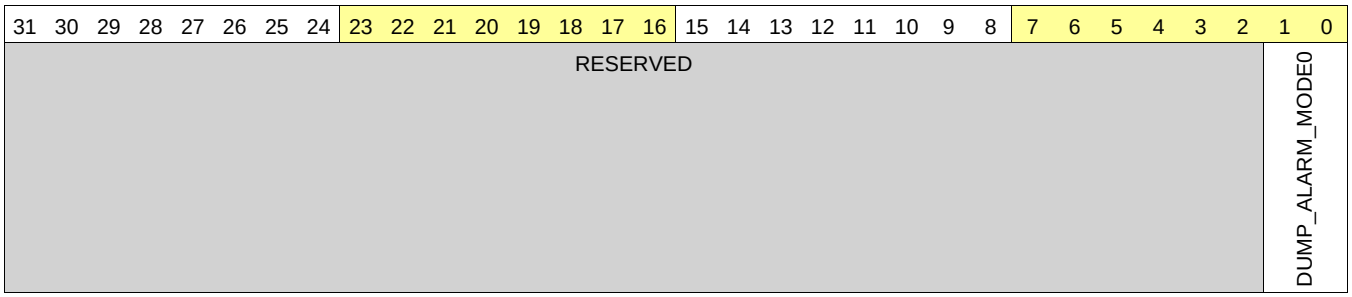
Table 14-299. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MAXVAL

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-300. L3_STCOL_DUMP_ALARM_MODE0

Address Offset	See Table 14-240.		
Physical Address	0x4500 106C	**Instance**	CLK2_STATCOLL0
	0x4500 206C		CLK2_STATCOLL1
	0x4500 306C		CLK2_STATCOLL2
	0x4500 406C		CLK2_STATCOLL3
	0x4500 506C		CLK2_STATCOLL4
	0x4500 606C		CLK2_STATCOLL5
	0x4500 706C		CLK2_STATCOLL6
	0x4500 806C		CLK2_STATCOLL7
	0x4500 906C		CLK2_STATCOLL8
	0x4500 A06C		CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE0	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0.	RW	0x0
		0x0: OFF		
		0x1: MIN		
		0x3: MAX		
		0x2: BOTH		

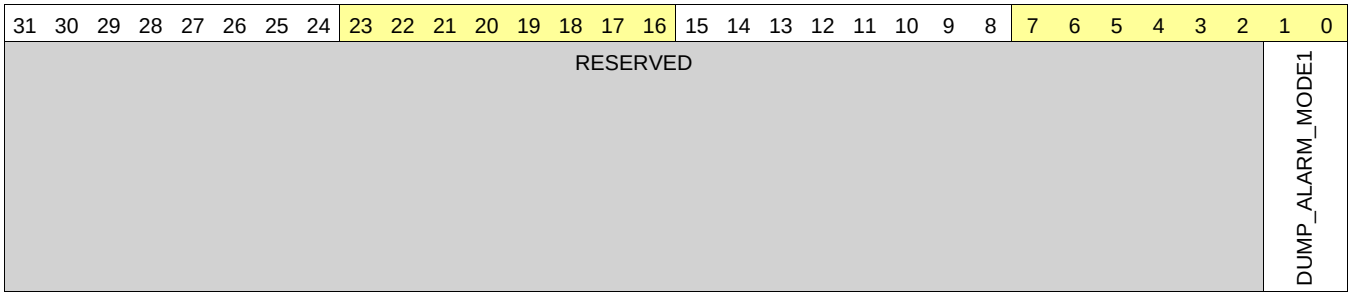
Table 14-301. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE0

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-302. L3_STCOL_DUMP_ALARM_MODE1

Address Offset	See Table 14-240.		
Physical Address	0x4500 1070	**Instance**	CLK2_STATCOLL0
	0x4500 2070		CLK2_STATCOLL1
	0x4500 3070		CLK2_STATCOLL2
	0x4500 4070		CLK2_STATCOLL3
	0x4500 5070		CLK2_STATCOLL4
	0x4500 6070		CLK2_STATCOLL5
	0x4500 7070		CLK2_STATCOLL6
	0x4500 8070		CLK2_STATCOLL7
	0x4500 9070		CLK2_STATCOLL8
	0x4500 A070		CLK2_STATCOLL9
Description			
Type	RW		



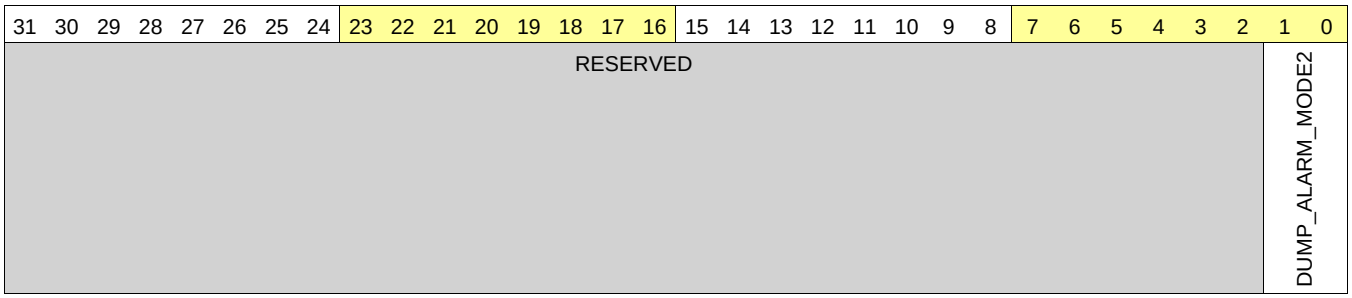
Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE1	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-303. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE1

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-304. L3_STCOL_DUMP_ALARM_MODE2

Address Offset	See Table 14-240.		
Physical Address	0x4500 1074	**Instance**	CLK2_STATCOLL0
	0x4500 2074		CLK2_STATCOLL1
	0x4500 3074		CLK2_STATCOLL2
	0x4500 4074		CLK2_STATCOLL3
	0x4500 5074		CLK2_STATCOLL4
	0x4500 6074		CLK2_STATCOLL5
	0x4500 7074		CLK2_STATCOLL6
	0x4500 8074		CLK2_STATCOLL7
	0x4500 9074		CLK2_STATCOLL8
	0x4500 A074		CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE2	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-305. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE2

L3_MAIN Interconnect • L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-306. L3_STCOL_DUMP_ALARM_MODE3

Address Offset	See Table 14-240.		
Physical Address	0x4500 1078 0x4500 2078 0x4500 3078 0x4500 4078 0x4500 5078 0x4500 6078 0x4500 7078 0x4500 8078 0x4500 9078 0x4500 A078	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE3	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE3	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-307. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE3

L3_MAIN Interconnect • L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-308. L3_STCOL_DUMP_ALARM_MODE4

Address Offset	See Table 14-240.		
Physical Address	0x4500 107C 0x4500 207C 0x4500 407C	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE4	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE4	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-309. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE4

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-310. L3_STCOL_DUMP_ALARM_MODE5

Address Offset	See Table 14-240.		
Physical Address	0x4500 1080 0x4500 2080 0x4500 4080	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE5	

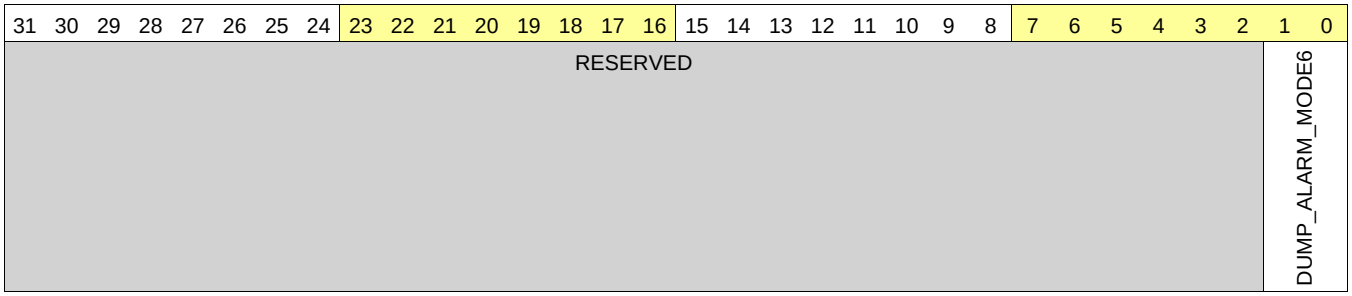
Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE5	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-311. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE5

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-312. L3_STCOL_DUMP_ALARM_MODE6

Address Offset	See Table 14-240.		
Physical Address	0x4500 1084 0x4500 4084	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	RW		



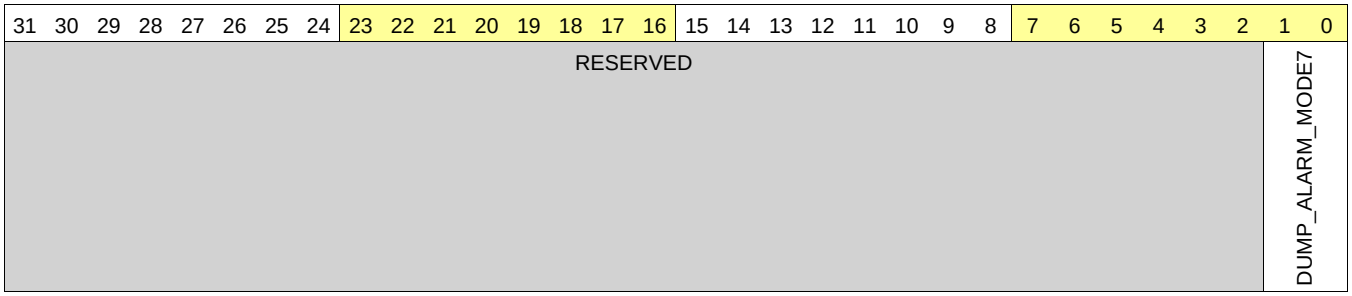
Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE6	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-313. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE6

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-314. L3_STCOL_DUMP_ALARM_MODE7

Address Offset	See Table 14-240.		
Physical Address	0x4500 1088 0x4500 4088	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	RW		



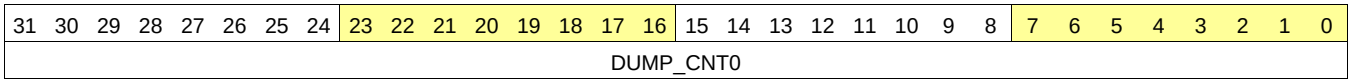
Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE7	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: 0x1: 0x3: 0x2:	RW	0x0

Table 14-315. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE7

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-316. L3_STCOL_DUMP_CNT0

Address Offset	See Table 14-240.		
Physical Address	0x4500 108C	**Instance**	CLK2_STATCOLL0
	0x4500 208C		CLK2_STATCOLL1
	0x4500 308C		CLK2_STATCOLL2
	0x4500 408C		CLK2_STATCOLL3
	0x4500 508C		CLK2_STATCOLL4
	0x4500 608C		CLK2_STATCOLL5
	0x4500 708C		CLK2_STATCOLL6
	0x4500 808C		CLK2_STATCOLL7
	0x4500 908C		CLK2_STATCOLL8
	0x4500 A08C		CLK2_STATCOLL9
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT0	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-317. Register Call Summary for Register L3_STCOL_DUMP_CNT0

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-318. L3_STCOL_DUMP_CNT1

Address Offset	See Table 14-240.		
Physical Address	0x4500 1090	**Instance**	CLK2_STATCOLL0
	0x4500 2090		CLK2_STATCOLL1
	0x4500 3090		CLK2_STATCOLL2
	0x4500 4090		CLK2_STATCOLL3
	0x4500 5090		CLK2_STATCOLL4
	0x4500 6090		CLK2_STATCOLL5
	0x4500 7090		CLK2_STATCOLL6
	0x4500 8090		CLK2_STATCOLL7
	0x4500 9090		CLK2_STATCOLL8
	0x4500 A090		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT1																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT1	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-319. Register Call Summary for Register L3_STCOL_DUMP_CNT1

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-320. L3_STCOL_DUMP_CNT2

Address Offset	See Table 14-240.		
Physical Address	0x4500 1094	**Instance**	CLK2_STATCOLL0
	0x4500 2094		CLK2_STATCOLL1
	0x4500 3094		CLK2_STATCOLL2
	0x4500 4094		CLK2_STATCOLL3
	0x4500 5094		CLK2_STATCOLL4
	0x4500 6094		CLK2_STATCOLL5
	0x4500 7094		CLK2_STATCOLL6
	0x4500 8094		CLK2_STATCOLL7
	0x4500 9094		CLK2_STATCOLL8
	0x4500 A094		CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT2																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT2	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-321. Register Call Summary for Register L3_STCOL_DUMP_CNT2

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-322. L3_STCOL_DUMP_CNT3

Address Offset	See Table 14-240.		
Physical Address	0x4500 1098 0x4500 2098 0x4500 3098 0x4500 4098 0x4500 5098 0x4500 6098 0x4500 7098 0x4500 8098 0x4500 9098 0x4500 A098	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT3																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT3	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-323. Register Call Summary for Register L3_STCOL_DUMP_CNT3

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-324. L3_STCOL_DUMP_CNT4

Address Offset	See Table 14-240.		
Physical Address	0x4500 109C 0x4500 209C 0x4500 409C	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT4																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT4	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-325. Register Call Summary for Register L3_STCOL_DUMP_CNT4

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-326. L3_STCOL_DUMP_CNT5

Address Offset	See Table 14-240.		
Physical Address	0x4500 10A0 0x4500 20A0 0x4500 40A0	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT5																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT5	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-327. Register Call Summary for Register L3_STCOL_DUMP_CNT5

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-328. L3_STCOL_DUMP_CNT6

Address Offset	See Table 14-240.		
Physical Address	0x4500 10A4 0x4500 40A4	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT6																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT6	Dump counter value Type: Status. Reset value: X.	R	0x---- ----

Table 14-329. Register Call Summary for Register L3_STCOL_DUMP_CNT6

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-330. L3_STCOL_DUMP_CNT7

Address Offset	See Table 14-240.		
Physical Address	0x4500 10A8 0x4500 40A8	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT7																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT7	Dump counter value Type: Status. Reset value: X.	R	0x---- ----

Table 14-331. Register Call Summary for Register L3_STCOL_DUMP_CNT7

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-332. L3_STCOL_FILTER_i_GLOBALEN

Address Offset	See Table 14-240.		
Physical Address	0x4500 10AC + (0x158*i) 0x4500 20AC + (0x158*i) 0x4500 30AC + (0x158*i) 0x4500 40AC + (0x158*i) 0x4500 50AC + (0x158*i) 0x4500 60AC + (0x158*i) 0x4500 70AC + (0x158*i) 0x4500 80AC + (0x158*i) 0x4500 90AC + (0x158*i) 0x4500 A0AC + (0x158*i)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_GLOBALEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_GLOBALEN	Filter global enable Type: Control. Reset value: 0x0.	RW	0

Table 14-333. Register Call Summary for Register L3_STCOL_FILTER_i_GLOBALEN

L3_MAIN Interconnect
- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary and Description: [1] [2]

Table 14-334. L3_STCOL_FILTER_i_ADDRMIN

Address Offset	See Table 14-240.		
Physical Address	0x4500 10B0 + (0x158*i) 0x4500 20B0 + (0x158*i) 0x4500 30B0 + (0x158*i) 0x4500 40B0 + (0x158*i) 0x4500 50B0 + (0x158*i) 0x4500 60B0 + (0x158*i) 0x4500 70B0 + (0x158*i) 0x4500 80B0 + (0x158*i) 0x4500 90B0 + (0x158*i) 0x4500 A0B0 + (0x158*i)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_ADDRMIN																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x0000 0000
22:0	FILTER0_ADDRMIN	Min addr range Type: Control. Reset value: 0x0.	RW	0x00 0000

Table 14-335. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMIN

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-336. L3_STCOL_FILTER_i_ADDRMAX

Address Offset	See Table 14-240.		
Physical Address	0x4500 10B4 + (0x158*i)	**Instance**	CLK2_STATCOLL0
	0x4500 20B4 + (0x158*i)		CLK2_STATCOLL1
	0x4500 30B4 + (0x158*i)		CLK2_STATCOLL2
	0x4500 40B4 + (0x158*i)		CLK2_STATCOLL3
	0x4500 50B4 + (0x158*i)		CLK2_STATCOLL4
	0x4500 60B4 + (0x158*i)		CLK2_STATCOLL5
	0x4500 70B4 + (0x158*i)		CLK2_STATCOLL6
	0x4500 80B4 + (0x158*i)		CLK2_STATCOLL7
	0x4500 90B4 + (0x158*i)		CLK2_STATCOLL8
	0x4500 A0B4 + (0x158*i)		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_ADDRMAX																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x0000 0000
22:0	FILTER0_ADDRMAX	Max addr range Type: Control. Reset value: 0x0.	RW	0x00 0000

Table 14-337. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMAX

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-338. L3_STCOL_FILTER_i_ADDREN

Address Offset	See Table 14-240.		
Physical Address	0x4500 10B8 + (0x158*i)	**Instance**	CLK2_STATCOLL0
	0x4500 20B8 + (0x158*i)		CLK2_STATCOLL1
	0x4500 30B8 + (0x158*i)		CLK2_STATCOLL2
	0x4500 40B8 + (0x158*i)		CLK2_STATCOLL3
	0x4500 50B8 + (0x158*i)		CLK2_STATCOLL4
	0x4500 60B8 + (0x158*i)		CLK2_STATCOLL5
	0x4500 70B8 + (0x158*i)		CLK2_STATCOLL6
	0x4500 80B8 + (0x158*i)		CLK2_STATCOLL7
	0x4500 90B8 + (0x158*i)		CLK2_STATCOLL8
	0x4500 A0B8 + (0x158*i)		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER0_ADDREN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
0	FILTER0_ADDREN	max filtering enable Type: Control. Reset value: 0x0.	RW	0

Table 14-339. Register Call Summary for Register L3_STCOL_FILTER_i_ADDREN

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-340. L3_STCOL_FILTER_i_EN_k

Address Offset See Table 14-240.

Physical Address 0x4500 10BC + (0x158*i) + (0x44*k)
0x4500 20BC + (0x158*i) + (0x44*k)
0x4500 30BC + (0x158*i) + (0x44*k)
0x4500 40BC + (0x158*i) + (0x44*k)
0x4500 50BC + (0x158*i) + (0x44*k)
0x4500 60BC + (0x158*i) + (0x44*k)
0x4500 70BC + (0x158*i) + (0x44*k)
0x4500 80BC + (0x158*i) + (0x44*k)
0x4500 90BC + (0x158*i) + (0x44*k)
0x4500 A0BC + (0x158*i) + (0x44*k)

Instance CLK2_STATCOLL0
CLK2_STATCOLL1
CLK2_STATCOLL2
CLK2_STATCOLL3
CLK2_STATCOLL4
CLK2_STATCOLL5
CLK2_STATCOLL6
CLK2_STATCOLL7
CLK2_STATCOLL8
CLK2_STATCOLL9

Description

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_EN0

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_EN0	Enable filter stage 0 Type: Control. Reset value: 0x0.	RW	0

Table 14-341. Register Call Summary for Register L3_STCOL_FILTER_i_EN_k

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-342. L3_STCOL_FILTER_i_MASK_m_MSTADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10C8 + (0x158*i) + (0x44*m) 0x4500 20C8 + (0x158*i) + (0x44*m) 0x4500 30C8 + (0x158*i) + (0x44*m) 0x4500 40C8 + (0x158*i) + (0x44*m) 0x4500 50C8 + (0x158*i) + (0x44*m) 0x4500 60C8 + (0x158*i) + (0x44*m) 0x4500 70C8 + (0x158*i) + (0x44*m) 0x4500 80C8 + (0x158*i) + (0x44*m) 0x4500 90C8 + (0x158*i) + (0x44*m) 0x4500 A0C8 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FILTER_i_MASK_m_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MASK_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 14-343. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_MSTADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-344. L3_STCOL_FILTER_i_MASK_m_RD

Address Offset	See Table 14-240.		
Physical Address	0x4500 10C0 + (0x158*i) + (0x44*m) 0x4500 20C0 + (0x158*i) + (0x44*m) 0x4500 30C0 + (0x158*i) + (0x44*m) 0x4500 40C0 + (0x158*i) + (0x44*m) 0x4500 50C0 + (0x158*i) + (0x44*m) 0x4500 60C0 + (0x158*i) + (0x44*m) 0x4500 70C0 + (0x158*i) + (0x44*m) 0x4500 80C0 + (0x158*i) + (0x44*m) 0x4500 90C0 + (0x158*i) + (0x44*m) 0x4500 A0C0 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MASK_m_RD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

Table 14-345. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_RD

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-346. L3_STCOL_FILTER_i_MASK_m_WR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10C4 + (0x158*i) + (0x44*m) 0x4500 20C4 + (0x158*i) + (0x44*m) 0x4500 30C4 + (0x158*i) + (0x44*m) 0x4500 40C4 + (0x158*i) + (0x44*m) 0x4500 50C4 + (0x158*i) + (0x44*m) 0x4500 60C4 + (0x158*i) + (0x44*m) 0x4500 70C4 + (0x158*i) + (0x44*m) 0x4500 80C4 + (0x158*i) + (0x44*m) 0x4500 90C4 + (0x158*i) + (0x44*m) 0x4500 A0C4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MASK_m_WR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

Table 14-347. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_WR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-348. L3_STCOL_FILTER_i_MASK_m_ERR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10D0 + (0x158*i) + (0x44*m) 0x4500 20D0 + (0x158*i) + (0x44*m) 0x4500 30D0 + (0x158*i) + (0x44*m) 0x4500 40D0 + (0x158*i) + (0x44*m) 0x4500 50D0 + (0x158*i) + (0x44*m) 0x4500 60D0 + (0x158*i) + (0x44*m) 0x4500 70D0 + (0x158*i) + (0x44*m) 0x4500 80D0 + (0x158*i) + (0x44*m) 0x4500 90D0 + (0x158*i) + (0x44*m) 0x4500 A0D0 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MASK_m_ERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

Table 14-349. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_ERR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-350. L3_STCOL_FILTER_i_MASK_m_USERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 10D4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FILTER_i_MASK_m_USERINFO															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MASK_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

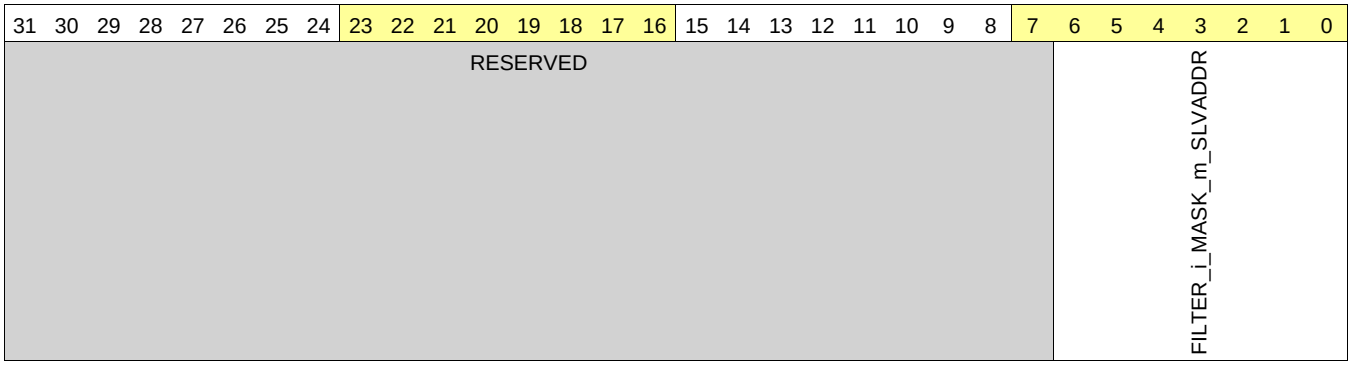
Table 14-351. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_USERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-352. L3_STCOL_FILTER_i_MASK_m_SLVADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 20CC + (0x158*i) + (0x44*m) 0x4500 30CC + (0x158*i) + (0x44*m) 0x4500 40CC + (0x158*i) + (0x44*m) 0x4500 50CC + (0x158*i) + (0x44*m) 0x4500 60CC + (0x158*i) + (0x44*m) 0x4500 70CC + (0x158*i) + (0x44*m) 0x4500 80CC + (0x158*i) + (0x44*m) 0x4500 90CC + (0x158*i) + (0x44*m) 0x4500 A0CC + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000 0000
6:0	FILTER_i_MASK_m_SLVADDR	Mask/Match of SlvAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 14-353. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_SLVADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-354. L3_STCOL_FILTER_i_MASK_m_REQUSERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 20D4 + (0x158*i) + (0x44*m) 0x4500 30D4 + (0x158*i) + (0x44*m) 0x4500 40D4 + (0x158*i) + (0x44*m) 0x4500 50D4 + (0x158*i) + (0x44*m) 0x4500 60D4 + (0x158*i) + (0x44*m) 0x4500 70D4 + (0x158*i) + (0x44*m) 0x4500 80D4 + (0x158*i) + (0x44*m) 0x4500 90D4 + (0x158*i) + (0x44*m) 0x4500 A0D4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_MASK0_REQUSERINFO																									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0000 0000
27:0	FILTER_i_MASK_m_REQUSERINFO	Mask/Match of ReqUserInfo Type: Control. Reset value: 0x0.	RW	0x00

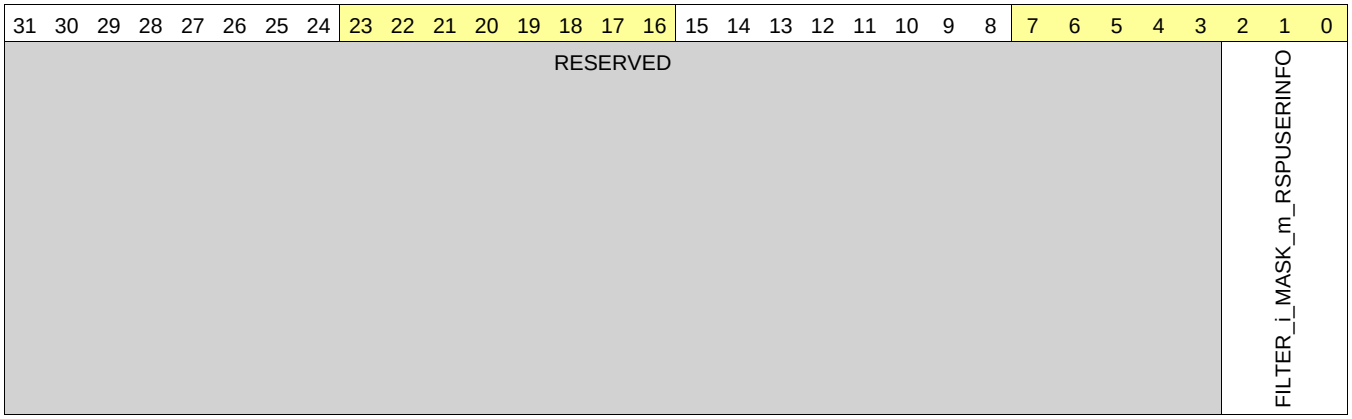
Table 14-355. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_REQUSERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-356. L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 20D8 + (0x158*i) + (0x44*m) 0x4500 30D8 + (0x158*i) + (0x44*m) 0x4500 40D8 + (0x158*i) + (0x44*m) 0x4500 50D8 + (0x158*i) + (0x44*m) 0x4500 60D8 + (0x158*i) + (0x44*m) 0x4500 70D8 + (0x158*i) + (0x44*m) 0x4500 80D8 + (0x158*i) + (0x44*m) 0x4500 90D8 + (0x158*i) + (0x44*m) 0x4500 A0D8 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	FILTER_i_MASK_m_RSPUSERINFO	Mask/Match of RspUserInfo Type: Control. Reset value: 0x0.	RW	0x0

Table 14-357. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-358. L3_STCOL_FILTER_i_MATCH_m_MSTADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10E8 + (0x158*i) + (0x44*m) 0x4500 20E8 + (0x158*i) + (0x44*m) 0x4500 30E8 + (0x158*i) + (0x44*m) 0x4500 40E8 + (0x158*i) + (0x44*m) 0x4500 50E8 + (0x158*i) + (0x44*m) 0x4500 60E8 + (0x158*i) + (0x44*m) 0x4500 70E8 + (0x158*i) + (0x44*m) 0x4500 80E8 + (0x158*i) + (0x44*m) 0x4500 90E8 + (0x158*i) + (0x44*m) 0x4500 A0E8 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FILTER_i_MATCH_m_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MATCH_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

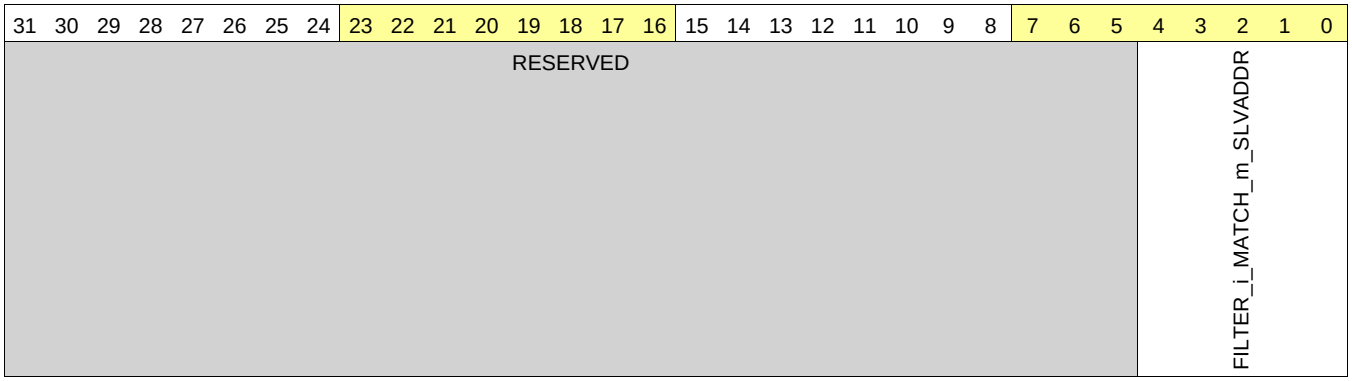
Table 14-359. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_MSTADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-360. L3_STCOL_FILTER_i_MATCH_m_SLVADDR

Address Offset	See Table 14-240.		
Physical Address	0x4500 20EC + (0x158*i) + (0x44*m) 0x4500 30EC + (0x158*i) + (0x44*m) 0x4500 40EC + (0x158*i) + (0x44*m) 0x4500 50EC + (0x158*i) + (0x44*m) 0x4500 60EC + (0x158*i) + (0x44*m) 0x4500 70EC + (0x158*i) + (0x44*m) 0x4500 80EC + (0x158*i) + (0x44*m) 0x4500 90EC + (0x158*i) + (0x44*m) 0x4500 A0EC + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000 0000
4:0	FILTER0_MATCH0_SLVADDR	Mask/Match of SlvAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 14-361. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_SLVADDR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-362. L3_STCOL_FILTER_i_MATCH_m_RD

Address Offset	See Table 14-240.		
Physical Address	0x4500 10E0 + (0x158*i) + (0x44*m) 0x4500 20E0 + (0x158*i) + (0x44*m) 0x4500 30E0 + (0x158*i) + (0x44*m) 0x4500 40E0 + (0x158*i) + (0x44*m) 0x4500 50E0 + (0x158*i) + (0x44*m) 0x4500 60E0 + (0x158*i) + (0x44*m) 0x4500 70E0 + (0x158*i) + (0x44*m) 0x4500 80E0 + (0x158*i) + (0x44*m) 0x4500 90E0 + (0x158*i) + (0x44*m) 0x4500 A0E0 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_RD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

Table 14-363. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_RD

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-364. L3_STCOL_FILTER_i_MATCH_m_WR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10E4 + (0x158*i) + (0x44*m) 0x4500 20E4 + (0x158*i) + (0x44*m) 0x4500 30E4 + (0x158*i) + (0x44*m) 0x4500 40E4 + (0x158*i) + (0x44*m) 0x4500 50E4 + (0x158*i) + (0x44*m) 0x4500 60E4 + (0x158*i) + (0x44*m) 0x4500 70E4 + (0x158*i) + (0x44*m) 0x4500 80E4 + (0x158*i) + (0x44*m) 0x4500 90E4 + (0x158*i) + (0x44*m) 0x4500 A0E4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_WR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

Table 14-365. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_WR

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-366. L3_STCOL_FILTER_i_MATCH_m_ERR

Address Offset	See Table 14-240.		
Physical Address	0x4500 10F0 + (0x158*i) + (0x44*m) 0x4500 20F0 + (0x158*i) + (0x44*m) 0x4500 30F0 + (0x158*i) + (0x44*m) 0x4500 40F0 + (0x158*i) + (0x44*m) 0x4500 50F0 + (0x158*i) + (0x44*m) 0x4500 60F0 + (0x158*i) + (0x44*m) 0x4500 70F0 + (0x158*i) + (0x44*m) 0x4500 80F0 + (0x158*i) + (0x44*m) 0x4500 90F0 + (0x158*i) + (0x44*m) 0x4500 A0F0 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_ERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

Table 14-367. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_ERR

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-368. L3_STCOL_FILTER_i_MATCH_m_USERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 10F4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL0
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FILTER_i_MATCH_m_USERINFO															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MATCH_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

Table 14-369. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_USERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-370. L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 20F4 + (0x158*i) + (0x44*m) 0x4500 30F4 + (0x158*i) + (0x44*m) 0x4500 40F4 + (0x158*i) + (0x44*m) 0x4500 50F4 + (0x158*i) + (0x44*m) 0x4500 260F4 + (0x158*i) + (0x44*m) 0x4500 70F4 + (0x158*i) + (0x44*m) 0x4500 80F4 + (0x158*i) + (0x44*m) 0x4500 90F4 + (0x158*i) + (0x44*m) 0x4500 A0F4 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_MASK0_REQUSERINFO																									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0000 0000
27:0	FILTER_i_MASK_m_REQUSERINFO	Mask/Match of ReqUserInfo Type: Control. Reset value: 0x0.	RW	0x00

Table 14-371. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-372. L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO

Address Offset	See Table 14-240.		
Physical Address	0x4500 20F8 + (0x158*i) + (0x44*m) 0x4500 30F8 + (0x158*i) + (0x44*m) 0x4500 40F8 + (0x158*i) + (0x44*m) 0x4500 50F8 + (0x158*i) + (0x44*m) 0x4500 60F8 + (0x158*i) + (0x44*m) 0x4500 70F8 + (0x158*i) + (0x44*m) 0x4500 80F8 + (0x158*i) + (0x44*m) 0x4500 90F8 + (0x158*i) + (0x44*m) 0x4500 A0F8 + (0x158*i) + (0x44*m)	**Instance**	CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														FILTER_i_MASK_m_RSPUSERINFO	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	FILTER_i_MASK_m_RSPUSERINFO	Mask/Match of RspUserInfo Type: Control. Reset value: 0x0.	RW	0x0

Table 14-373. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-374. L3_STCOL_OP_i_THRESHOLD_MINVAL

Address Offset	See Table 14-240.		
Physical Address	0x4500 11F0 + (0x158*i) 0x4500 21F0 + (0x158*i) 0x4500 31F0 + (0x158*i) 0x4500 41F0 + (0x158*i) 0x4500 51F0 + (0x158*i) 0x4500 61F0 + (0x158*i) 0x4500 71F0 + (0x158*i) 0x4500 81F0 + (0x158*i) 0x4500 91F0 + (0x158*i) 0x4500 A1F0 + (0x158*i)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								OP_i_THRESHOLD_MINVAL							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	OP_i_THRESHOLD_MINVAL	Min value Type: Control. Reset value: 0x0.	RW	0x000

Table 14-375. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MINVAL

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-376. L3_STCOL_OP_i_THRESHOLD_MAXVAL

Address Offset	See Table 14-240.		
Physical Address	0x4500 11F4 + (0x158*i) 0x4500 21F4 + (0x158*i) 0x4500 31F4 + (0x158*i) 0x4500 41F4 + (0x158*i) 0x4500 51F4 + (0x158*i) 0x4500 61F4 + (0x158*i) 0x4500 71F4 + (0x158*i) 0x4500 81F4 + (0x158*i) 0x4500 91F4 + (0x158*i) 0x4500 A1F4 + (0x158*i)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								OP_i_THRESHOLD_MAXVAL							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	OP_i_THRESHOLD_MAXVAL	Max value Type: Control. Reset value: 0x0.	RW	0x000

Table 14-377. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MAXVAL

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-378. L3_STCOL_OP_i_EVTINFOSEL

Address Offset	See Table 14-240.		
Physical Address	0x4500 11F8 + (0x158*i)	**Instance**	CLK2_STATCOLL0
	0x4500 21F8 + (0x158*i)		CLK2_STATCOLL1
	0x4500 31F8 + (0x158*i)		CLK2_STATCOLL2
	0x4500 41F8 + (0x158*i)		CLK2_STATCOLL3
	0x4500 51F8 + (0x158*i)		CLK2_STATCOLL4
	0x4500 61F8 + (0x158*i)		CLK2_STATCOLL5
	0x4500 71F8 + (0x158*i)		CLK2_STATCOLL6
	0x4500 81F8 + (0x158*i)		CLK2_STATCOLL7
	0x4500 91F8 + (0x158*i)		CLK2_STATCOLL8
	0x4500 A1F8 + (0x158*i)		CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														OP_i_EVTINFOSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	OP_i_EVTINFOSEL	Select event info data to add to counter (len/press or latency) Type: Control. Reset value: 0x0. 0x0: Select len from event info list 0x1: Select pressure if available from event info list 0x2: Select latency if available from event info list	RW	0x0

Table 14-379. Register Call Summary for Register L3_STCOL_OP_i_EVTINFOSEL

L3_MAIN Interconnect

- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

Table 14-380. L3_STCOL_OP_i_SEL

Address Offset	See Table 14-240.		
Physical Address	0x4500 11FC + (0x158*i) 0x4500 21FC + (0x158*i) 0x4500 31FC + (0x158*i) 0x4500 41FC + (0x158*i) 0x4500 51FC + (0x158*i) 0x4500 61FC + (0x158*i) 0x4500 71FC + (0x158*i) 0x4500 81FC + (0x158*i) 0x4500 91FC + (0x158*i) 0x4500 A1FC + (0x158*i)	**Instance**	CLK2_STATCOLL0 CLK2_STATCOLL1 CLK2_STATCOLL2 CLK2_STATCOLL3 CLK2_STATCOLL4 CLK2_STATCOLL5 CLK2_STATCOLL6 CLK2_STATCOLL7 CLK2_STATCOLL8 CLK2_STATCOLL9
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OP_i_SEL			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	OP_i_SEL	Select logical operation Type: Control. Reset value: 0x0. 0x0: Increment counter on each mask/match filter hit 0x1: Increment counter on each min/max level hit 0x2: Add to counter the selected event info value (len/press or latency) 0x3: increment counter when all filter event hits (And(Fi)) 0x4: Increment counter if any of filter event hits (Or(Fi)) 0x5: Add to counter the number of current request event that hit 0x6: Add to counter the number of current response event that hit 0x7: Add to counter the number of all event that hit 0x8:Increment counter on each selected external event hit	RW	0x0

Table 14-381. Register Call Summary for Register L3_STCOL_OP_i_SEL

L3_MAIN Interconnect
- L3_MAIN STATCOLL Register Summary and Description: [0] [1]

14.3 L4 Interconnects

This section details the device L4 interconnects.

14.3.1 L4 Interconnect Overview

The device uses three separate L4 interconnect structures to connect peripheral modules. All L4s handle transfers with peripherals but are located in distinct power domains.

Figure 14-9 is an overview of the L4 interconnects and the peripherals attached to them.

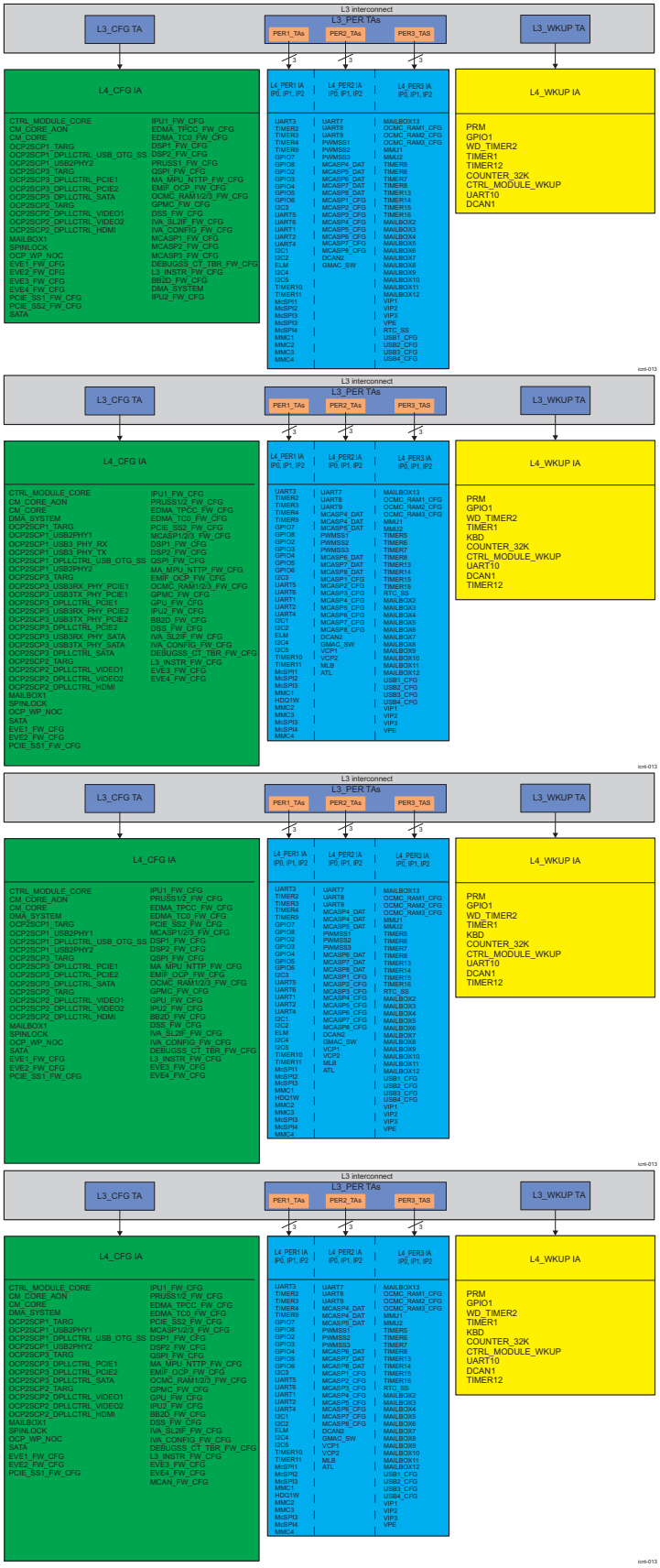
The L4 interconnect is composed of the following interconnects:

- L4_CFG: Includes the majority of the configuration interface for L3_MAIN system modules and peripheral interconnect
- L4 PER: Includes the main peripherals in the device. L4_PER is further divided into three sub-interconnects: L4_PER1, L4_PER2 and L4_PER3. As shown in Figure 14-9, each of these L4_PERx sub-interconnects is connected to L3_MAIN initiators via three ports:
  - L4_PER1_P1, L4_PER1_P2, L4_PER1_P3
  - L4_PER2_P1, L4_PER2_P2, L4_PER2_P3
  - L4_PER3_P1, L4_PER3_P2, L4_PER3_P3

  L3_MAIN initiators access the L4_PERx peripherals through these ports. All peripherals attached to L4_PER1 are visible from all three L4_PER1 ports; this is also correct for L4_PER2 and L4_PER3. For information on which initiator can access which L4_PERx port, see .
- L4_WKUP: Includes peripherals attached to the WKUP power domain

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Figure 14-9. L4 Interconnect Overview



The main features of the L4 interconnects are:

- Eleven ports from L3_MAIN interconnect onto 5 parallel L4 interconnects
- From one to three 32-bit initiator ports for each L4 interconnect instance (11 in total)
- 8-, 16-, or 32-bit data, single, or burst transactions
- Little-endian platform
- Non-blocking architecture with fair arbitration between masters
- Target interfaces: Fully synchronous or divided synchronous clock frequencies
- L4_CFG and L4_PER1, L4_PER2, L4_PER3 frequency equals half of L3 frequency
- Protection logic that provides user-configurable access control to targets by each initiator

14.3.2 L4 Interconnect Integration

Table 14-382 and Table 14-383 summarize the integration of the module in the device.

Table 14-382. Integration Attributes

Module Instance	Attributes
	Power Domain
L4_PER1, L4_PER2, L4_PER3	PD_COREAON
L4_CFG	PD_COREAON
L4_WKUP	PD_WKUPAON

Table 14-383. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER1	L4_PER1_CLK	L4PER_L3_GICLK	PRCM module	Functional and interface clock
L4_PER2	L4_PER2_CLK	L4PER_L3_GICLK	PRCM module	Functional and interface clock
L4_PER3	L4_PER3_CLK	L4PER_L3_GICLK	PRCM module	Functional and interface clock
L4_CFG	L4_CFG_CLK	L4CFG_L3_GICLK	PRCM module	Functional and interface clock
L4_WKUP	L4_WKUP_CLK	WKUPAON_GICLK	PRCM module	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER1, L4_PER2, L4_PER3	L4_PER_RST	L4_PER_RST	PRCM module	Reset of L4_PERx interconnect
	L4_PER_RET_RST	L4_PER_PWRON_RET_RST	PRCM module	Reset of L4_PERx interconnect retention registers. For information about retention reset, see Chapter 3, *Power, Reset, and Clock Management*.
L4_CFG	L4_CFG_RST	CORE_RST	PRCM module	Reset of L4_CFG interconnect.
	L4_CFG_RET_RST	CORE_PWRON_RET_RST	PRCM module	Reset of L4_CFG interconnect retention registers. For information about retention reset, see Chapter 3, *Power, Reset, and Clock Management*.
L4_WKUP	L4_WKUP_RST	WKUPAON_RST	PRCM module	Reset of L4_WKUP interconnect
	L4_WKUP_RET_RST	L4_WKUP_RET_RST	PRCM module	Reset of L4_WKUP interconnect. For information about retention reset, see Chapter 3, *Power, Reset, and Clock Management*.

14.3.3 L4 Interconnect Functional Description

14.3.3.1 Module Distribution

IAs and TAs provide the interface to connect the different modules to their associated interconnect.

Table 14-384 through Table 14-393 list all the modules and subsystems with their associated agents. The agents are listed for each L4 interconnect domain.

14.3.3.1.1 L4_PER1 Interconnect Agents

The L4_PER1 interconnect handles transfers only to peripherals in the PER power domain. Table 14-384 lists the L4_PER1 TAs.

Table 14-384. L4_PER1 TAs

Module Target Name	Description
UART3_TARG	Universal Asynchronous Receiver/Transmitter target port
TIMER2_TARG	General Purpose Timer 2 target port
TIMER3_TARG	TIMER3 target port
TIMER4_TARG	TIMER4 target port
TIMER9_TARG	TIMER9 target port
GPIO7_TARG	General-Purpose Interface 7 target port
GPIO8_TARG	GPIO8 target port
GPIO2_TARG	GPIO2 target port
GPIO3_TARG	GPIO3 target port
GPIO4_TARG	GPIO4 target port
GPIO5_TARG	GPIO5 target port
GPIO6_TARG	GPIO6 target port
I2C3_TARG	Inter-Integrated Circuit 3 target port
UART5_TARG	UART5 target port
UART6_TARG	UART6 target port
UART1_TARG	UART1 target port
UART2_TARG	UART2 target port
UART4_TARG	UART4 target port
I2C1_TARG	I2C1 target port
I2C2_TARG	I2C2 target port
ELM_TARG	Error Location Module target port
I2C4_TARG	I2C4 target port
I2C5_TARG	I2C5 target port
TIMER10_TARG	TIMER10 target port
TIMER11_TARG	TIMER11 target port
MCSPI1_TARG	Multi-channel Serial Peripheral Interface 1 (McSPI1) target port
MCSPI2_TARG	McSPI2 target port
MMC1_TARG	MMC1 target port
MMC2_TARG	MMC2 target port
MMC3_TARG	MMC3 target port
HDQ1W_TARG	HDQ1W target port
MCSPI3_TARG	McSPI3 target port
MCSPI4_TARG	McSPI4 target port
MMC4_TARG	MMC4 target port

Four ports communicate between the L3_MAIN interconnect and the L4_PER1 interconnect to allow the L3_MAIN initiators to access the L4_PER1 targets. Table 14-385 lists the L4_PER1 initiator TAs.

For the list of initiators authorized to access the L4_PER1 peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-385. L4_PER1 IAs

Module Iniator Name	Description
L3_MAIN_IP0_INIT	L3 sDMA RD interconnect port
L3_MAIN_IP1_INIT	L3 sDMA WR interconnect port
L3_MAIN_IP2_INIT	L3 MPU subsystem interconnect port

14.3.3.1.2 L4_PER2 Interconnect Agents

The L4_PER2 interconnect handles transfers only to peripherals in the PER power domain. Table 14-386 lists the L4_PER2 TAs.

Table 14-386. L4_PER2 TAs

Module Target Name	Description
UART7_TARG	UART7 target port
UART8_TARG	UART8 target port
UART9_TARG	UART9 target port
MCASP4_DAT_TARG	Multi-Channel Audio Serial Port - DAT target port
MCASP5_DAT_TARG	MCASP5_DAT target port
MCASP6_DAT_TARG	MCASP6_DAT target port
MCASP7_DAT_TARG	MCASP7_DAT target port
MCASP8_DAT_TARG	MCASP8_DAT target port
MCASP1_CFG_TARG	MCASP1_CFG target port
MCASP2_CFG_TARG	MCASP2_CFG target port
MCASP3_CFG_TARG	MCASP3_CFG target port
MCASP4_CFG_TARG	MCASP4_CFG target port
MCASP5_CFG_TARG	MCASP5_CFG target port
MCASP6_CFG_TARG	MCASP6_CFG target port
MCASP7_CFG_TARG	MCASP7_CFG target port
MCASP8_CFG_TARG	MCASP8_CFG target port
PWM1_TARG	Pulse-Width Modulation 1 target port
PWM2_TARG	PWM2 target port
PWM3_TARG	PWM3 target port
VCP1_CFG_TARG NOTE: VCP1 is not supported in this family of devices.	Viterby Coder/Decoder 1 target port
VCP2_CFG_TARG NOTE: VCP2 is not supported in this family of devices.	Viterby Coder/Decoder 2 target port
MLB_TARG NOTE: MLB is not supported in this family of devices.	Media Local Bus target port
ATL_TARG NOTE: ATL is not supported in this family of devices.	Audio Tracking Logic target port
DCAN2_TARG	DCAN2 target port
GMAC_SW_TARG	Ethernet Controller target port

Three ports communicate between the L3_MAIN interconnect and the L4_PER2 interconnect to allow the L3_MAIN initiators to access the L4_PER2 targets. Table 14-387 lists the L4_PER2 initiator TAs.

For the list of initiators authorized to access the L4_PER2 peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-387. L4_PER2 IAs

Module Iniator Name	Description
L3_MAIN_IP0_INIT	L3 sDMA RD interconnect port
L3_MAIN_IP1_INIT	L3 sDMA WR interconnect port
L3_MAIN_IP2_INIT	L3 MPU subsystem interconnect port

14.3.3.1.3 L4_PER3 Interconnect Agents

The L4_PER3 interconnect handles transfers only to peripherals in the PER power domain. Table 14-388 lists the L4_PER3 TAs.

Table 14-388. L4_PER3 TAs

Module Target Name	Description
TIMER5_TARG	TIMER5 target port
TIMER6_TARG	TIMER6 target port
TIMER7_TARG	TIMER7 target port
TIMER8_TARG	TIMER8 target port
TIMER13_TARG	TIMER13 target port
TIMER14_TARG	TIMER14 target port
TIMER15_TARG	TIMER15 target port
TIMER16_TARG	TIMER16 target port
VIP1_TARG	Video Input Parser(VIP) 1 target port
VIP2_TARG	VIP2 target port
VIP3_TARG	VIP3 target port
VPE_TARG	Video Processing Engine target port
RTC_TARG	Real-Time Clock target port
MBX2_TARG	Mailbox 2 target port
MBX3_TARG	Mailbox 3 target port
MBX4_TARG	Mailbox 4 target port
MBX5_TARG	Mailbox 5 target port
MBX6_TARG	Mailbox 6 target port
MBX7_TARG	Mailbox 7 target port
MBX8_TARG	Mailbox 8 target port
MBX12_TARG	Mailbox 12 target port
MBX9_TARG	Mailbox 9 target port
MBX10_TARG	Mailbox 10 target port
MBX11_TARG	Mailbox 11 target port
USB4_CFG_TARG NOTE: USB4(ULPI) is not supported in this family of devices.	USB4 configuration port
SATA_TARG	SATA target port
USB2_CFG_TARG	USB2 configuration port
OCMC_RAM1_TARG	On-Chip Memory Controller RAM1 target port
USB1_CFG_TARG	USB1 configuration target port

Table 14-388. L4_PER3 TAs (continued)

Module Target Name	Description
USB3_CFG_TARG NOTE: USB3(ULPI) is not supported in this family of devices.	USB3 configuration target port
OCMC_RAM2_TARG	OCMC_RAM2 target port
OCMC_RAM3_TARG	OCMC_RAM3 target port
MMU1_TARG	Memory Management Unit 1 target port
MMU2_TARG	MMU2 target port
MBX13_TARG	Mailbox 13 target port

Three ports communicate between the L3_MAIN interconnect and the L4_PER3 interconnect to allow the L3_MAIN initiators to access the L4_PER3 targets. Table 14-389 lists the L4_PER3 initiator TAs.

For the list of initiators authorized to access the L4_PER3 peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-389. L4_PER3 IAs

Module Iniator Name	Description
L3_MAIN_IP0_INIT	L3 sDMA RD interconnect port
L3_MAIN_IP1_INIT	L3 sDMA WR interconnect port
L3_MAIN_IP2_INIT	L3 MPU subsystem interconnect port

14.3.3.1.4 L4_CFG Interconnect Agents

The L4_CFG interconnect handles only transfers to peripherals in the CORE power domain. Table 14-390 lists the TAs.

Table 14-390. L4_CFG TAs

Module Target Name	Description
CTRL_MODULE_CORE_TARG	Control Module core target
CM_CORE_AON_TARG	CORE_AON module
CM_CORE_TARG	CM_CORE module
DMA_SYSTEM_TARG	System DMA
SCP1_TARG	SCP1 module
SCP2_TARG	SCP2 module
MAILBOX_TARG	Mailbox module
SPINLOCK_TARG	Spinlock module
OCP_WP_NOC_TARG	OCP watchpoint module
SATA_TARG	SATA controller module
EVE1_FW_CFG_TARG NOTE: EVE1 is not supported in this family of devices.	Embedded Vision Engine firewall
EVE2_FW_CFG_TARG NOTE: EVE2 is not supported in this family of devices.	EVE2 firewall
EVE3_FW_CFG_TARG NOTE: EVE3 is not supported in this family of devices.	EVE3 firewall
EVE4_FW_CFG_TARG NOTE: EVE4 is not supported in this family of devices.	EVE4 firewall
IPU1_FW_CFG_TARG	Image Processing Unit (IPU) 1 firewall
IPU2_FW_CFG_TARG	IPU 2 firewall
TPCC_FW_CFG_TARG	EDMA Channel Controller firewall
TPTC_FW_CFG_TARG	EDMA Transfer Controller firewall

Table 14-390. L4_CFG TAs (continued)

Module Target Name	Description
PCIESS1_FW_CFG_TARG	PCIE1 firewall
MCASP1_FW_CFG_TARG	McASP1 firewall
SCP3_TARG	SCP3 module
OCP2SCP1_USB2PHY1	OCP2SCP1_USB2PHY1 core target port
OCP2SCP1_DPLLCTRL_USB_OTG_SS_TARG	USB OTG Subsystem DPLLCTRL target port
OCP2SCP3_USB2PHY2	USB2PHY2 target port
VCP1_FW_CFG_TARG NOTE: VCP1 is not supported in this family of devices.	Viterby Coder/Decoder 1 firewall
VCP2_FW_CFG_TARG NOTE: VCP2 is not supported in this family of devices.	VCP2 module firewall
OCP2SCP3_DPLLCTRL_PCIE1_TARG	PCIE1 DPLL CTRL target port
OCP2SCP3_DPLLCTRL_PCIE2_TARG	PCIE2 DPLL CTRL target port
OCP2SCP3_DPLLCTRL_SATA_TARG	SATA DPLL CTRL target port
OCP2SCP2_DPLLCTRL_VIDEO1_TARG	VIDEO1 DPLL CTRL target port
OCP2SCP2_DPLLCTRL_VIDEO2_TARG	VIDEO2 DPLL CTRL target port
OCP2SCP2_DPLLCTRL_HDMI_TARG	HDMI DPLL CTRL target port
DSP1_SDMA_FW_CFG_TARG	DSP1 firewall
DSP2_SDMA_FW_CFG_TARG	DSP2 firewall
PRUSS1_FW_CFG_TARG	PRU-ICSS1 firewall
PRUSS2_FW_CFG_TARG	PRU-ICSS2 firewall
MA_MPU_NTTP_FW_CFG_TARG	MA_MPU firewall
EMIF_OCP_FW_CFG_TARG	EMIF firewall
OCMC_RAM2_FW_CFG_TARG	OCMC_RAM2 firewall
GPMC_FW_CFG_TARG	GPMC firewall
OCMC_RAM1_FW_CFG_TARG	OCMC_RAM1 firewall
GPU_FW_CFG_TARG	GPU firewall
BB2D_FW_CFG_TARG	2D Graphics Accelerator firewall
OCMC_RAM3_FW_CFG_TARG	OCMC_RAM3 firewall
DSS_FW_CFG_TARG	DSS firewall
IVA_SL2IF_FW_CFG_TARG	IVA SL2IF firewall
IVA_CONFIG_FW_CFG_TARG	IVA Config firewall
DEBUGSS_CT_TBR_FW_CFG_TARG	Debug subsystem firewall
L3_INSTR_FW_CFG_TARG	L3 Instrumentation firewall
MCASP2_FW_CFG_TARG	McASP2 firewall
QSPI_FW_CFG_TARG	QSPI firewall
MCASP3_FW_CFG_TARG	McASP3 firewall
PCIESS2_FW_CFG_TARG	PCIE2 firewall

A unique port, L3_MAIN_INIT, communicates between the L3 interconnect and the L4_CFG interconnect to allow the L3 initiators to access the L4_CFG targets (see Table 14-391).

For the list of initiators authorized to access the L4_CFG peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-391. L4_CFG IAs

Module Iniator Name	Description
L3_MAIN_IP0	L3 interconnect port

14.3.3.1.5 L4_WKUP Interconnect Agents

The L4-WKUP interconnect handles transfers only to peripherals in the WKUP power domain. Table 14-392 lists the TAs. Table 14-393 lists the L4 WKUP IAs.

Table 14-392. L4_WKUP TAs

Module Target Name	Description
PRM_TARG	PRM module
GPIO1_TARG	GPIO1 module
WD_TIMER2_TARG	Watchdog Timer 2
TIMER1_TARG	Timer 1
TIMER12_TARG	Timer 12
KBD_TARG	Keyboard controller
COUNTER_32K_TARG	Counter 32k timer
CTRL_MODULE_WKUP_TARG	Control Module Wakeup module
UART10_TARG	UART10 module
DCAN1_TARG	CAN1 module

Table 14-393. L4_WKUP IAs

Module Iniator Name	Description
L3_MAIN_IP0	L3 interconnect port

14.3.3.2 Power Management

As part of the system-wide power-management scheme, the L4 interconnects go into IDLE state after receiving a request from the PRCM module after all commands are serviced. This function is handled by hardware. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

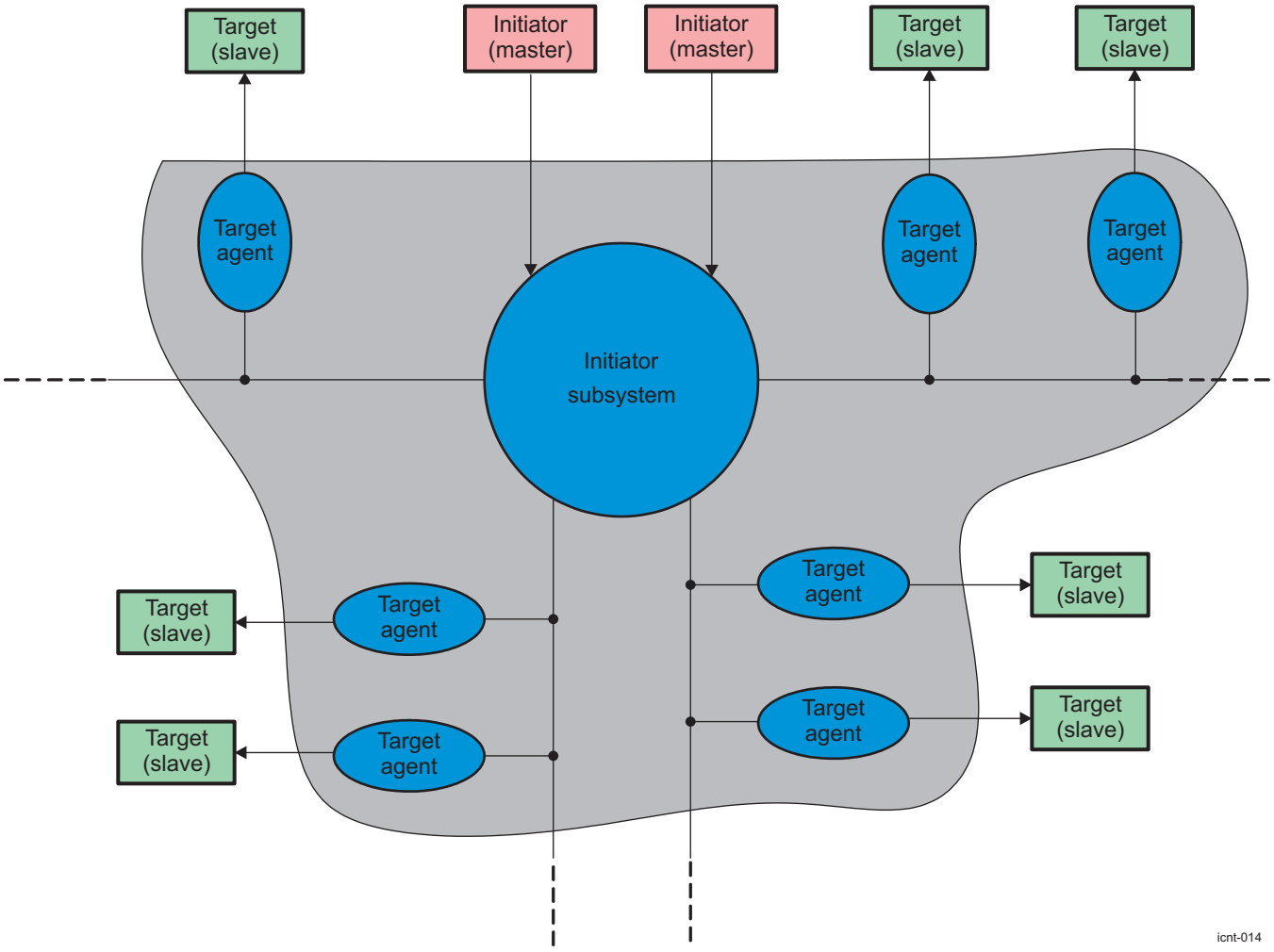
To reduce power consumption, each L4 interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

L4_CFG, L4_PER1, L4_PER2, L4_PER3, and L4_WKUP are located in the always-on power domain and no retention is needed for these L4 interconnects.

14.3.3.3 L4 Firewalls

Figure 14-10 is an internal view of the L4 interconnects in the overall interconnect. This architecture, with one initiator subsystem centralizing all initiator master requests and distributing them to all target modules (peripherals), enables the L4 interconnect firewall functions to be centralized at the L4 initiator subsystem level. The L4 firewall filters the accesses based on the configurable protection groups defined in the L4 address protection (AP) registers. Each module or TA is assigned to a protection group. The configuration is also defined in the L4 AP and is programmable on a module-per-module basis.

Figure 14-10. L4 Initiator-Target Connectivity



NOTE: As Figure 14-10 shows, targets are attached to branches. Branches do not impact the function of the L4 interconnect but are present to simplify timing closure and reduce active power consumption.

Because of the large address spaces and the number of peripherals connected to an L4 interconnect, two parameters are used to set up access permission:

- Programmable groups for initiators:
  - Eight protection groups for the L4 interconnect
- Segments divided into regions
  - 85 regions for the L4_PER1 interconnect
  - 63 regions for the L4_PER2 interconnect
  - 97 regions for the L4_PER3 interconnect
  - 129 regions for the L4_CFG interconnect
  - 44 regions for the L4_WKUP interconnect

Protection group members are TAs with the same protection settings. A region is programmed to allow access to a unique selectable protection group. For better protection, different regions are grouped into protection group regions and associated with a protection group member.

14.3.3.3.1 Protection Group

A protection group is defined by its initiators (or members) and MReqInfo is allowed. Two registers define these two settings:

- The 64-bit CONNID_BIT_VECTOR field L4_AP_PROT_GROUP_MEMBERS_k_L and L4_AP_PROT_GROUP_MEMBERS_k_H registers define which initiator belongs to a group. A protection group is accessible by an initiator when the bit position corresponding to its ConnID is set to 1 in the CONNID_BIT_VECTOR field. Table 14-394 lists all the ConnIDs available at the L4 levels.
- The ENABLE field L4_AP_PROT_GROUP_ROLES_k_L register lists all possible MReqInfo combinations associated with the L4_AP_PROT_GROUP_MEMBERS register. Setting a Req bit in this register determines the initiators type of access. For more information, see Section 14.2.3.7, *L3 Firewall Functionality*. Two MReqInfos are used in L4 interconnects: MReqDebug and MReqSupervisor.

NOTE: Permissions are identical for read and write accesses in L4 interconnect.

k indicates the protection group number.

L indicates the region number.

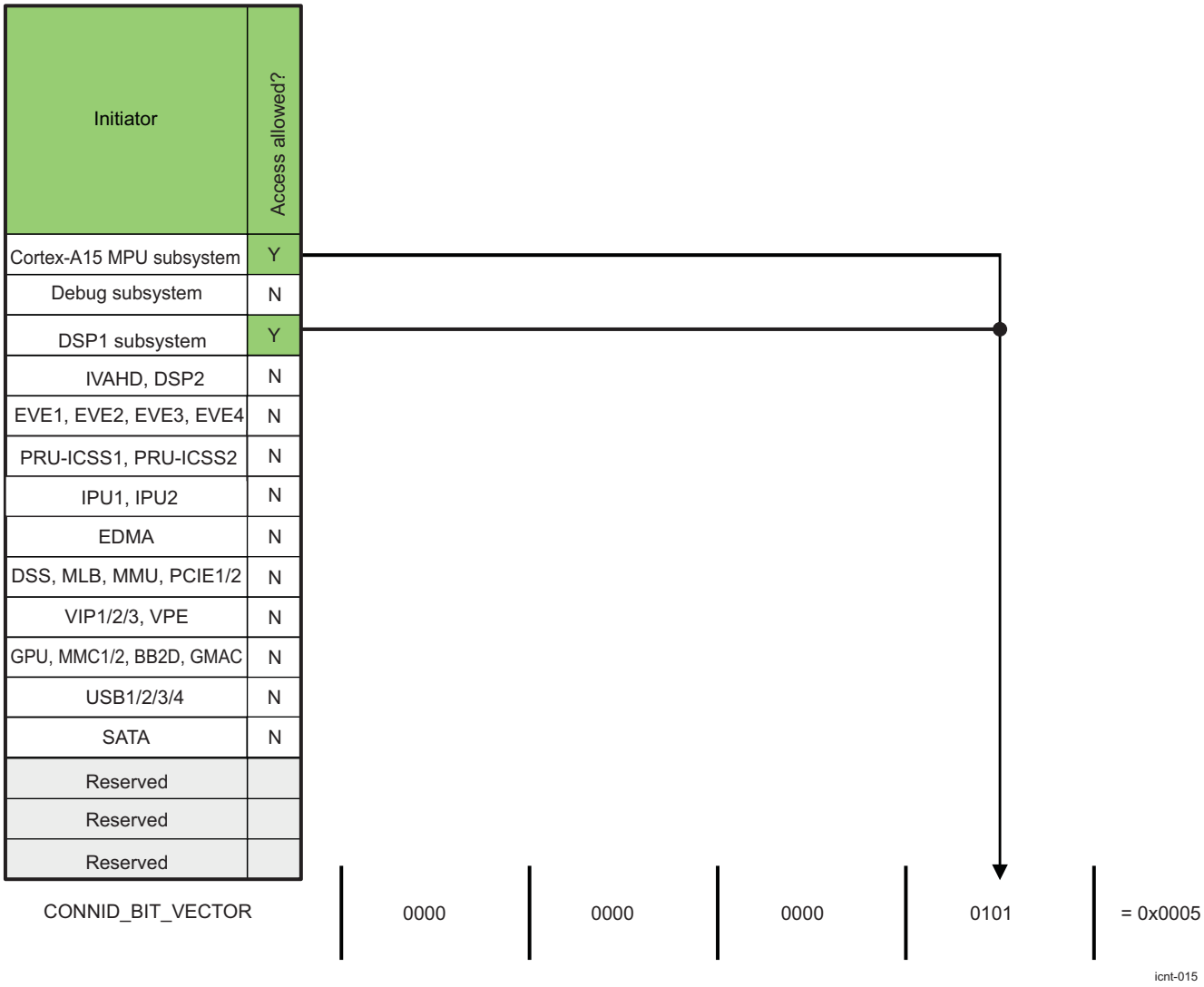
Table 14-394. L4 ConnID Definition

ConnID	Initiator
0	Cortex-A15 MPU subsystem
1	Debug subsystem
2	DSP1 subsystem (CFG, EDMA, MDMA), DSP2 (EDMA)
3	IVAHD, DSP2(CFG, MDMA)
4	EVE1, EVE2, EVE3, EVE4
5	PRU-ICSS1, PRU-ICSS2
6	IPU1/2; SYSTEM_DMA
7	EDMA
8	DSS, MLB, MMU1, MMU2, PCIE1 and PCIE2
9	VIP1, VIP2, VIP3, VPE
A	MMC1, MMC2, GPU, BB2D, GMAC
B	USB1, USB2, USB3, USB4
C	SATA
D	Reserved
E	Reserved
F	Reserved

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Figure 14-11 is an example of CONNID_BIT_VECTOR.

Figure 14-11. Example of CONNID_BIT_VECTOR L4_AP_PROT_GROUP_MEMBERS_k



Setting bits 0 and 2 in the PROT_GROUP_MEMBERS_L register defines a group initiator that can access targets in protection group 1, and includes the following:

- Cortex-A15 MPU subsystem
- DSP subsystem

Protection group 1 can be applied to multiple protection regions with no limitation. Each protection region that is configured with protection group 1 enables permission access only to the two initiators.

The L4_AP_REGION_i_H PROT_GROUP_ID field determines the region to which the protection group member is attached.

The values of some CONNID_BIT_VECTOR and ENABLE fields are exported by the system control module (SCM) at reset or are user writable (see Figure 14-11 for more information).

Table 14-395 and Table 14-398 list the default configuration of the various groups for each L4 interconnect. For each group, some modules or regions are associated with it using default initiator members.

Table 14-395. L4_PER1 Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	L4_PER1_AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_ROLES_0_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_H	No	EXPORTED
Group 1	Reserved	L4_AP_PROT_GROUP_ROLES_1_L	No	EXPORTED
		L4_AP_PROT_GROUP_ROLES_1_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_1_L	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_1_H	No	EXPORTED
Group 2–7	PER1 peripherals	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 2 to 7	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 2 to 7	Yes	0xFFFF (all)

Table 14-396. L4_PER2 Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	L4_PER2_AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_ROLES_0_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_H	No	EXPORTED
Group 1 - 7 L4_PER2 peripherals	PER2 peripherals	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 1 to 7	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 1 to 7	Yes	0xFFFF (all)

Table 14-397. L4_PER3 Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	L4_PER_AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_ROLES_0_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_H	No	EXPORTED
Group 1 - 7 L4_PER3 peripherals	PER3 peripherals	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 1 to 7	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 1 to 7	Yes	0xFFFF (all)

Table 14-398. L4_CFG Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L L4_AP_PROT_GROUP_ROLES_0_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_L L4_AP_PROT_GROUP_MEMBERS_0_H	No	EXPORTED
Group 1	L3 firewall registers	L4_AP_PROT_GROUP_ROLES_1_L L4_AP_PROT_GROUP_ROLES_1_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_1_L L4_AP_PROT_GROUP_MEMBERS_1_H	No	EXPORTED
Group 5 Free	CPFROM	L4_AP_PROT_GROUP_ROLES_5_L L4_AP_PROT_GROUP_ROLES_5_H	Yes	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_5_L L4_AP_PROT_GROUP_MEMBERS_5_H	Yes	EXPORTED
Group 2, 3, 4 Free	No modules attached	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_L where k = 2, 3, 4 and 6	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 2, 3 and 4	Yes	0xFFFF (all)

Table 14-398. L4_CFG Firewall Default Configuration (continued)

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 6, 7 Other modules	Other L4_CFG modules	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 6 and 7	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 6 and 7	Yes	0xFFFF (all)

Table 14-399. L4_WKUP Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L L4_AP_PROT_GROUP_ROLES_0_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_0_L L4_AP_PROT_GROUP_MEMBERS_0_H	No	EXPORTED
Group 1	Reserved	L4_AP_PROT_GROUP_ROLES_1_L L4_AP_PROT_GROUP_ROLES_1_H	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_1_L L4_AP_PROT_GROUP_MEMBERS_1_H	No	EXPORTED
Group 2	No Modules Attached	L4_AP_PROT_GROUP_ROLES_2_L L4_AP_PROT_GROUP_ROLES_2_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_2_L L4_AP_PROT_GROUP_MEMBERS_2_H	Yes	0xFFFF (all)
Group 3 Free	Reserved	L4_AP_PROT_GROUP_ROLES_3_L L4_AP_PROT_GROUP_ROLES_3_L	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_3_L L4_AP_PROT_GROUP_MEMBERS_3_H	No	0xFFFF (all)
Group 4 Free	Reserved	L4_AP_PROT_GROUP_ROLES_4_L L4_AP_PROT_GROUP_ROLES_4_L	No	EXPORTED
		L4_AP_PROT_GROUP_MEMBERS_4_L L4_AP_PROT_GROUP_MEMBERS_4_H	No	EXPORTED

Table 14-399. L4_WKUP Firewall Default Configuration (continued)

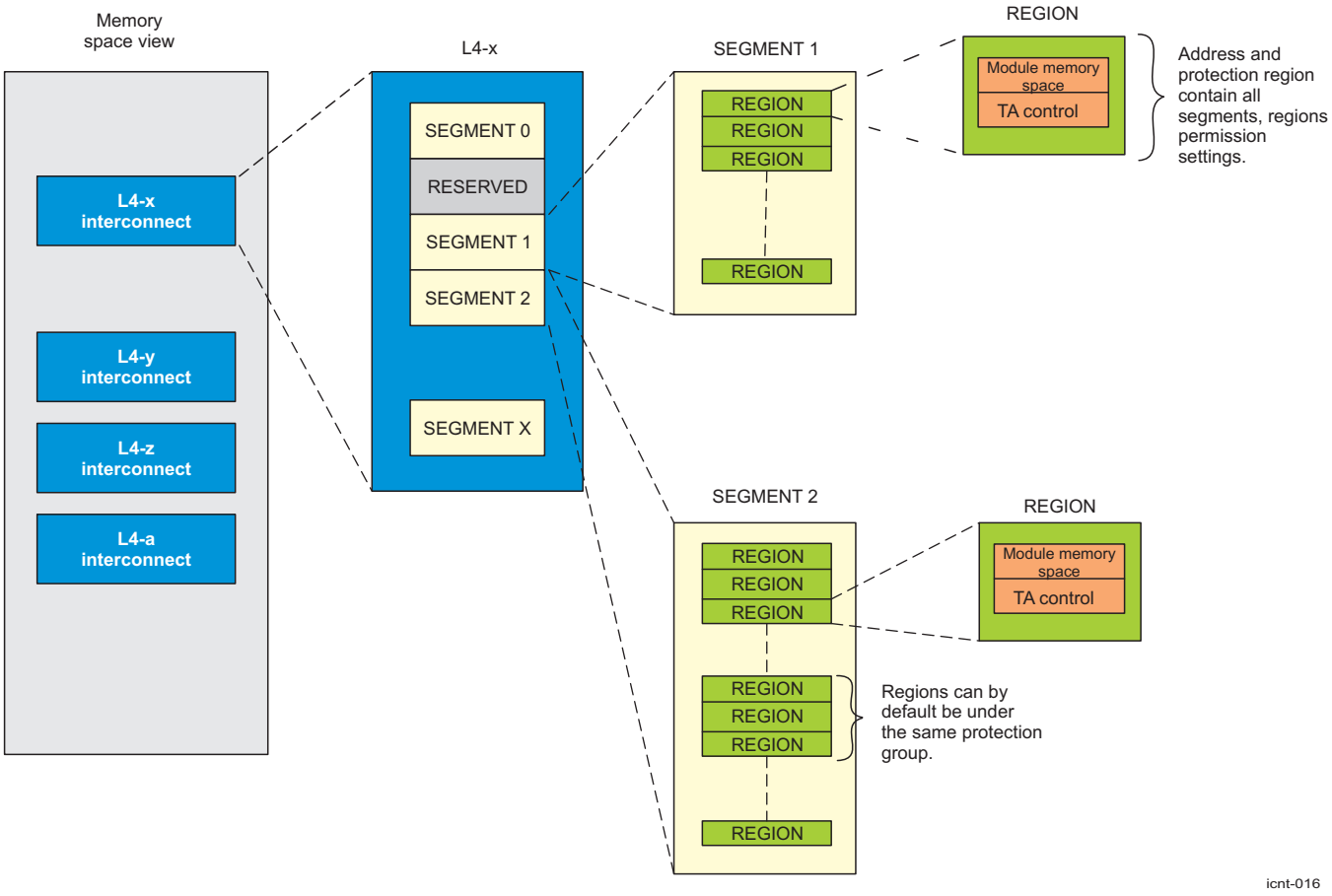
Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 5-7 Other modules	Other L4_WKUP modules	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 5, 6, 7	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 5, 6, 7	Yes	0xFFFF (all)

NOTE: For EXPORTED default values see CONTROL_SEC_ LOAD_FW_EXPORTED_VALUE register in Chapter 18, *Control Module*

14.3.3.3.2 Segments and Regions

The protection mechanism for L4 interconnects is based on a hierarchical segmentation, as shown in Figure 14-12. By default, some regions are attached to specific protection group members. This specificity lets users set up the permission access to certain types of modules requiring the same access protection without managing region allocation.

Figure 14-12. L4 Segmentation



All interconnect address spaces are covered by regions. Table 14-400 through Table 14-404 list the module mapping with their addresses, region numbers, and default protection group allocated to them.

NOTE: Module refers to the configuration registers of the module.

TA (Target Agent) refers to the interconnect configuration registers of the TA associated with the module.

Table 14-400. Region Allocations for L4_PER1 Interconnect

Module	Region	Description
L4_PER1_CONFIG	0	Address Protection
	1	L3_MAIN_IP0 initiator port
	2	Link Agent
UART3_TARG	3	Module
	4	TA
TIMER2_TARG	5	Module
	6	TA
TIMER3_TARG	7	Module
	8	TA
TIMER4_TARG	9	Module
	10	TA
TIMER9_TARG	11	Module
	12	TA
GPIO2_TARG	13	Module
	14	TA
GPIO3_TARG	15	Module
	16	TA
GPIO4_TARG	17	Module
	18	TA
GPIO5_TARG	19	Module
	20	TA
GPIO6_TARG	21	Module
	22	TA
I2C3	23	Module
UART1_TARG	24	Module
	25	TA
UART2_TARG	26	Module
	27	TA
UART4_TARG	28	Module
	29	TA
I2C1_TARG	30	Module
	31	TA
I2C2_TARG	32	Module
	33	TA
I2C3_TARG	34	TA
GPIO8_TARG	35	Module
	36	TA
HDQ1W_TARG	37	Module
	38	TA
TIMER10_TARG	41	Module
	42	TA

Table 14-400. Region Allocations for L4_PER1 Interconnect (continued)

Module	Region	Description
TIMER11_TARG	43	Module
	44	TA
GPIO7_TARG	45	Module
	46	TA
MCSPI1_TARG	47	Module
	48	TA
MCSPI2_TARG	49	Module
	50	TA
MMC1_TARG	51	Module
	52	TA
UART6_TARG	53	Module
	54	TA
MMC3_TARG	61	Module
	62	TA
UART5_TARG	63	Module
	64	TA
MMC2_TARG	65	Module
	66	TA
MCSPI3_TARG	67	Module
	68	TA
MCSPI4_TARG	69	Module
	70	TA
MMC4_TARG	71	Module
	72	TA
L4_PER1 CONFIG	77	L3_MAIN_IP1
	78	L3_MAIN_IP2
I2C4_TARG	81	Module
	82	TA
I2C5_TARG	83	Module
	84	TA

Table 14-401. Region Allocations for L4_PER2 Interconnect

Module	Region	Description
L4_PER2_CONFIG	0	Address Protection
	1	L3_MAIN_IP0 initiator port
	2	Link Agent
GMAC_TARG	3	Module
L4_PER2_CONFIG	4	L3_MAIN_IP1 initiator port
	5	L3_MAIN_IP2 initiator port
GMAC_TARG	6	TA
MLB_TARG	7	Module
NOTE: MLB is not supported in this family of devices.	8	TA
MCASP1_CFG_TARG	9	Module
	10	TA
MCASP2_CFG_TARG	11	Module
	12	TA

Table 14-401. Region Allocations for L4_PER2 Interconnect (continued)

Module	Region	Description
MCASP3_CFG_TARG	13	Module
	14	TA
MCASP4_CFG_TARG	15	Module
	16	TA
MCASP4_DAT_TARG	17	Module
	18	TA
MCASP5_CFG_TARG	19	Module
	20	TA
MCASP5_DAT_TARG	21	Module
	22	TA
PWM1_TARG	25	Module
	26	TA
PWM2_TARG	27	Module
	28	TA
PWM3_TARG	29	Module
	30	TA
DCAN2_TARG	31	Module
	32	TA
MCASP6_CFG_TARG	35	Module
	36	TA
MCASP7_DAT_TARG	37	Module
	38	TA
MCASP7_CFG_TARG	39	Module
	40	TA
MCASP8_DAT_TARG	41	Module
	42	TA
MCASP8_CFG_TARG	43	Module
	44	TA
MCASP6_DAT_TARG	45	Module
	46	TA
UART7_TARG	47	Module
	48	TA
UART8_TARG	49	Module
	50	TA
UART9_TARG	51	Module
	52	TA
VCP1_CFG_TARG NOTE: VCP1 is not supported in this family of devices.	53	Module
	54	TA
VCP2_CFG_TARG NOTE: VCP2 is not supported in this family of devices.	55	Module
	56	TA

Table 14-402. Region Allocations for L4_PER3 Interconnect

Module	Region	Description
L4_PER3_CONFIG	0	Address Protection
	1	Link Agent
	2	L3_MAIN_IP0 initiator port
	3	L3_MAIN_IP1 initiator port
	4	L3_MAIN_IP2 initiator port
TIMER5_TARG	5	Module
	6	TA
TIMER6_TARG	7	Module
	8	TA
TIMER7_TARG	9	Module
	10	TA
TIMER8_TARG	11	Module
	12	TA
TIMER13_TARG	13	Module
	14	TA
TIMER14_TARG	15	Module
	16	TA
TIMER15_TARG	17	Module
	18	TA
TIMER16_TARG	19	Module
	20	TA
VIP1_TARG	21	Module
	22	TA
VIP2_TARG	23	Module
	24	TA
VIP3_TARG	25	Module
	26	TA
VPE_TARG	27	Module
	28	TA
RTC_TARG	29	Module
	30	TA
MBX2_TARG	33	Module
	34	TA
MBX3_TARG	35	Module
	36	TA
MBX4_TARG	37	Module
	38	TA
MBX5_TARG	39	Module
	40	TA
MBX6_TARG	41	Module
	42	TA
MBX7_TARG	43	Module
	44	TA
MBX8_TARG	45	Module
	46	TA
MBX12_TARG	67	Module
	68	TA

Table 14-402. Region Allocations for L4_PER3 Interconnect (continued)

Module	Region	Description
MBX9_TARG	69	Module
	70	TA
MBX10_TARG	71	Module
	72	TA
MBX11_TARG	73	Module
	74	TA
USB4_CFG_TARG NOTE: USB4(ULPI) is not supported in this family of devices.	75	Module
	76	TA
USB2_CFG_TARG	79	Module
	80	TA
OCMC_RAM1_TARG	81	Module
	82	TA
USB1_CFG_TARG	83	Module
	84	TA
USB3_CFG_TARG NOTE: USB3(ULPI) is not supported in this family of devices.	85	Module
	86	TA
OCMC_RAM3_TARG	87	Module
	88	TA
MMU1_TARG	91	Module
	92	TA
MMU2_TARG	93	Module
	94	TA
MBX13_TARG	95	Module
	96	TA

Table 14-403. Region Allocations for L4_CFG Interconnect

Module	Region	Description
L4_CFG Configuration	0	AP
	1	LA
	2	IP0
CTRL_MODULE_CORE_TARG	3	Module
	4	TA
CM_CORE_AON_TARG	5	Module
	6	TA
CM_CORE_TARG	7	Module
	8	TA
DMA_SYSTEM_TARG	9	Module
	10	TA
SCP1_TARG	13	Module
	14	TA
SCP2_TARG	15	Module
	16	TA
MAILBOX_TARG	23	Module
	24	TA

Table 14-403. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
SPINLOCK_TARG	25	Module
	26	TA
OCP_WP_NOC_TARG	27	Module
	28	TA
SATA_TARG	31	Module
	32	TA
EVE1_FW_CFG_TARG NOTE: EVE1 is not supported in this family of devices.	33	Module
	34	TA
EVE2_FW_CFG_TARG NOTE: EVE2 is not supported in this family of devices.	35	Module
	36	TA
EVE3_FW_CFG_TARG NOTE: EVE3 is not supported in this family of devices.	37	Module
	38	TA
EVE4_FW_CFG_TARG NOTE: EVE4 is not supported in this family of devices.	39	Module
	40	TA
IPU1_FW_CFG_TARG	41	Module
	42	TA
IPU2_FW_CFG_TARG	43	Module
	44	TA
VCP1_FW_CFG_TARG NOTE: VCP1 is not supported in this family of devices.	45	Module
	46	TA
VCP2_FW_CFG_TARG NOTE: VCP2 is not supported in this family of devices.	47	Module
	48	TA
TPCC_FW_CFG_TARG	49	Module
	50	TA
TPTC_FW_CFG_TARG	51	Module
	52	TA
PCIESS1_FW_CFG_TARG	53	Module
	54	TA
MCASP1_FW_CFG_TARG	55	Module
	56	TA
SCP3_TARG	59	Module
	60	TA
DSP1_SDMA_FW_CFG_TARG	61	Module
	62	TA
DSP2_SDMA_FW_CFG_TARG	63	Module
	64	TA
PRUSS1_FW_CFG_TARG	65	Module
	66	TA
PRUSS2_FW_CFG_TARG	67	Module
	68	TA
MA_MPU_NTTP_FW_CFG_TARG	79	Module
	80	TA
EMIF_OCP_FW_CFG_TARG	81	Module
	82	TA

Table 14-403. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
OCMC_RAM2_FW_CFG_TARG	83	Module
	84	TA
GPMC_FW_CFG_TARG	85	Module
	86	TA
OCMC_RAM1_FW_CFG_TARG	87	Module
	88	TA
GPU_FW_CFG_TARG	89	Module
	90	TA
OCMC_RAM3_FW_CFG	91	Module
	92	TA
DSS_FW_CFG_TARG	93	Module
	94	TA
IVA_SL2IF_FW_CFG_TARG	95	Module
	96	TA
IVA_CONFIG_FW_CFG_TARG	97	Module
	98	TA
DEBUGSS_CT_TBR_FW_CFG_TARG	99	Module
	100	TA
L3_INSTR_FW_CFG_TARG	101	Module
	102	TA
MCASP2_FW_CFG_TARG	103	Module
	104	TA
QSPI_FW_CFG_TARG	105	Module
	106	TA
MCASP3_FW_CFG_TARG	107	Module
	108	TA
PCIESS2_FW_CFG_TARG	125	Module
	126	TA

Table 14-404. Region Allocations for L4_WKUP Interconnect

Module	Region	Description
L4 WKUP	0	AP
	1	IP0
	2	LA
PRM_TARG	3	Module
	4	TA
GPIO1_TARG	5	Module
	6	TA
WD_TIMER2_TARG	7	Module
	8	TA
TIMER1_TARG	9	Module
	10	TA
KBD_TARG	11	Module
	12	TA
COUNTER_32K	15	Module
	16	TA

Table 14-404. Region Allocations for L4_WKUP Interconnect (continued)

Module	Region	Description
CTRL_MODULE_WKUP	17	Module
	18	TA
TIMER12	19	Module
	20	TA
UART10_TARG	28	Module
	29	TA
DCAN1_TARG	30	Module
	31	TA

14.3.3.3.3 L4 Firewall Address and Protection Register Settings

Table 14-405 lists the settings of the AP registers relative to an L4 interconnect firewall. These values are computed based on the physical implementation of each L4 interconnect.

Table 14-405. L4 Firewall Register Description Overview

Register Type	Register Name	Bits	Field	Description
Segment	L4_AP_SEGMENT_i_L (1)	31:0	BASE	Segment base address
	L4_AP_SEGMENT_i_H (1)	5:0	SIZE	Segment size equals to 2^{SIZE}
Protection groups	L4_AP_PROT_GROUP_MEMBERS_k_L (2)	15:0	CONNID_BIT_VECTOR	For L4ConnID, see Table 14-394.
	L4_AP_PROT_GROUP_ROLES_k_L (2) L4_AP_PROT_GROUP_ROLES_k_H	31:0	ENABLE	See Section 14.2.3.7.3 for REQ_INFO description. (3)
Region setting	L4_AP_REGION_l_L (4)	20:0	BASE	Defines the base address of region with respect to its segment base address
	L4_AP_REGION_l_H (4)	31:28	MADDRSPACE	Target interconnect MAddrSpace
		26:24	SEGMENT_ID	Segment ID number of the region
		22:20	PROT_GROUP_ID	Protection group member attached to the region
		18:17	BYTE_DATA_WIDTH_EXP	Determines the number of bytes in an access
		14:8	PHY_TARGET_ID	Physical target ID
		6:1	SIZE	Size of the region equals to 2^{SIZE}
		0	ENABLE	Enables the region protection

(1) i = 0 to 1 for PER1_AP
i = 0 for PER2_AP
i = 0 for PER3_AP
i = 0 to 2 for CFG_AP
i = 0 to 3 for WKUP_AP

(2) k = 0 to 7 for PER1_AP
k = 0 to 7 for PER2_AP
k = 0 to 7 for PER3_AP
k = 0 to 7 for CFG_AP
k = 0 to 7 for WKUP_AP

(3) For L4 interconnects, only MReqDebug and MReqSupervisor are available.

(4) l = 0 to 84 for PER1_AP
l = 0 to 62 for PER2_AP
l = 0 to 96 for PER3_AP
l = 0 to 128 for CFG_AP
l = 0 to 43 for WKUP_AP

14.3.3.4 L4 Error Detection and Reporting

14.3.3.4.1 IA and TA Error Detection and Logging

The L4 interconnect provides mechanisms for handling internally detected errors or errors reported by modules attached to the L4 target ports.

NOTE: L4_IA denotes the IA for all L4 interconnects: L4_PER1, L4_PER2, L4_PER3, L4_CFG, and L4_WKUP.

L4_TA denotes the TA for all L4 interconnects: L4_PER1, L4_PER2, L4_PER3, L4_CFG, and L4_WKUP.

The L4 interconnects handle four types of errors:

- No target core found or address hole, detected and logged at IA
- Unsupported command, detected and logged at IA
- Protection violation, detected and logged at IA (see Section 14.3.3.3, *L4 Firewalls*)
- Target does not service a request before a time-out expires. The error is detected and logged at TA (see Section 14.3.3.4.2, *Time-Out*).

Table 14-406 lists the value of the L4_IA_ERROR_LOG_L[25:24] CODE bit field stored when an error occurs.

Table 14-406. L4 CODE Bit Field Definition

CODE (bits 1:0)	Error Type	REQ_INFO	Secondary	ConnID	CMD
0	No error				
1	Unsupported command	x	x	x	x
2	Address hole	x	x	x	x
3	Protection violation	x		x	x

- No target core found/address hole: This error indicates that a request was addressed to a hole in the L4 address map. When this error occurs, an in-band error response is returned to the L3 level. The error is also logged into the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. Additionally, an address hole error code is logged to the L4_IA_ERROR_LOG_L[25:24] CODE bit field.
- Unsupported command: This error indicates that the command type of the request is not supported by the accessed target register. The error is logged into the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. An unsupported command error code is written to the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the initiator interface.
- Protection violation: This error indicates that a request is not issued from an allowed initiator member or is issued with the inappropriate ReqInfo qualifiers associated with the target region. This error is reported using an in-band error and is written to the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. A protection violation error code is saved into the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the same initiator interface. A protection violation is also logged in the L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY or [30] PROT_ERROR_PRIMARY bit when in debug or applicative mode, respectively.

  The L4_IA_ERROR_LOG_L[30] SECONDARY bit indicates whether the error occurred in application or debug.

  The L4_IA_ERROR_LOG_H[15:0] REQ_INFO bit field returns the type of access (REQ_INFO qualifier) that caused the error.

  The L4_IA_ERROR_LOG_L[13:8] CONNID bit field returns the ID of the initiator that caused the error.

  The L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR register logs the address for error conditions.

14.3.3.4.2 Time-Out

A time-out mechanism can be enabled at the interconnect level and on a per-target basis. If the mechanism is enabled for a TA and interconnect and commands are not accepted or responses are not returned within the expected delay, the L4 interconnect generates an error event.

NOTE: The time-out mechanism is not available on the L4_WKUP interconnect, but L4_WKUP time-outs are detected in CFG_TA_L4WKUP of the L4_CFG interconnect.

The error is logged in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit. The affected TA enters an error state that causes it to send an error response to any new request targeted at it. To recover from this state, system software must reset the TA. The time-out is counted starting from the moment a command is presented to the target, regardless of the target response to this command.

The L4 interconnect implements a centralized time-base circuit that broadcasts a set of four periodic pulse signals to all connected TAs. The time-base circuit offers four possible sets of four time-base signals. The time-base signals are selected by programming the L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE bit field.

The selected time-base signals are available at any TA. Each TA can be programmed to refer to one of these four time-base signals, using the L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT bit field. These four signals are referred to as 1X time-base, 4X time-base, 16X time-base, and 64X time-base.

Table 14-407 lists all values in number of L4 clock cycles.

Table 14-407. L4 Time-out Link and TA Programming

	L4_TA_AGENT_CONTROL_L [10:8] REQ_TIMEOUT				
L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	**0**	**1**	**2**	**3**	**4**
0	All L4 time-out features are disabled.				
1	Locally disabled	64	256	1024	4096
2		256	1024	4096	16,384
3		1024	4096	16,384	65,536
4		4096	16,384	65,536	262,144

The default reset value is 0x2 for REQ_TIMEOUT and 0x4 for TIMEOUT_BASE, implying 16,384 clock cycles.

A time-out condition is detected when the command acceptance or the response is not received after a delay of from one to three time-base periods.

Example:

- L4 frequency = 65-MHz, 15.3-µs period
- TIMEOUT_BASE = 4 in the L4_LA_NETWORK_CONTROL_L register
- REQ_TIMEOUT = 2 in the L4_TA_AGENT_CONTROL_L for TA A
- REQ_TIMEOUT = 4 in the L4_TA_AGENT_CONTROL_L for TA B

At agent A, the time-base unit is 16,384 cycles. A time-out is issued when a request to the attached module is not accepted, or no response is sent after a delay of 252 µs to 756 µs.

At agent B, the time-base unit is 262,144 cycles. A time-out is issued when a request to the attached module is not accepted or no response is sent after a delay of 4 ms to 12 ms.

When a time-out condition is detected, the TA logs the error in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit, and it also reports the error to the IA, which forwards it to the L3 interconnects.

After the time-out is detected and logged, the behavior of the attached module is ignored. A new request targeting the module arriving at the timed-out TA receives an error response. If the request is addressed to the agent internal registers, it is processed normally.

To recover from a time-out error, software is assumed to first reset the faulty module and then the TA using the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit.

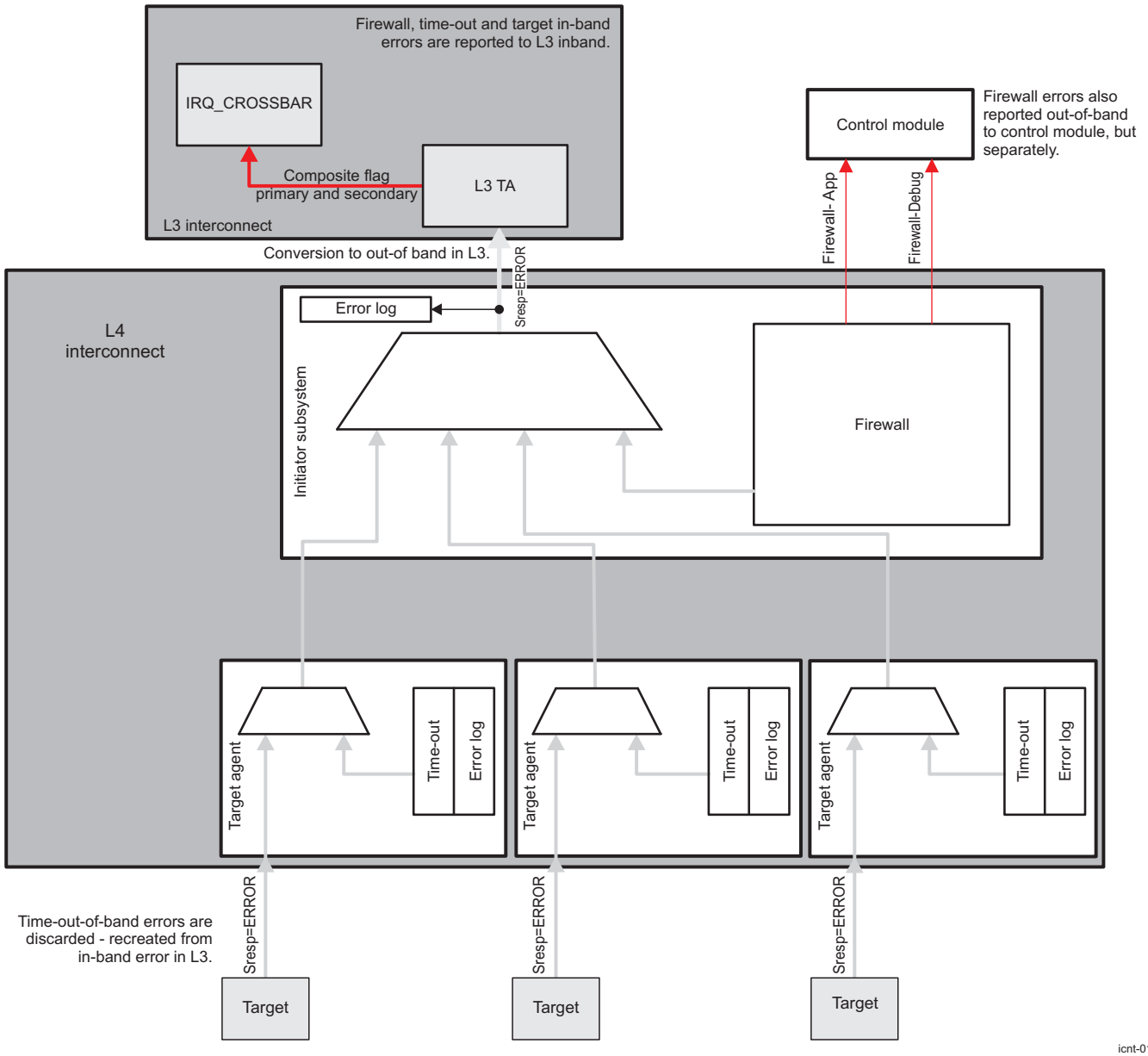
14.3.3.4.3 Error Reporting

Figure 14-13 shows the error-reporting scheme used in the L4 interconnects. All L4 in-band errors are reported to their respective L3 TA, where errors are converted in an out-of band error signal (the L3 applicative and debug composite flags) going to the L3 INTCs.

Two levels of mask are present to report the error at INTC level:

- At the applicative and debug composite flag, to enable interrupt reporting, the following bits must be set:
  - L4_CFG in L3_FLAGMUX_MASK0 and L3_FLAGMUX_STATUS1
  - L4_PER in L3_FLAGMUX_MASK0 and L3_FLAGMUX_STATUS1
- At the L3 TA level, see Section 14.2.1, *L3 Interconnect*.

Figure 14-13. L4 Error Reporting



14.3.3.4.4 Error Recovery

Setting the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit to 1 initiates the software reset period. Software reset must be asserted for at least 16 cycles of the target module interface clock, which can be a divided clock with respect to the L4 clock.

During the software reset period:

- Requests sent to the target module receive error responses. Therefore, if the faulty request is part of a DMA transfer, it is necessary to stop the DMA to prevent unwanted errors.
- Requests sent to the TA register block are processed as usual.
- The L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT status bit is cleared.

Setting the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit to 0 terminates the software reset period.

Reset the attached module to complete the recovery.

14.3.3.4.5 Firewall Error Logging in the Control Module

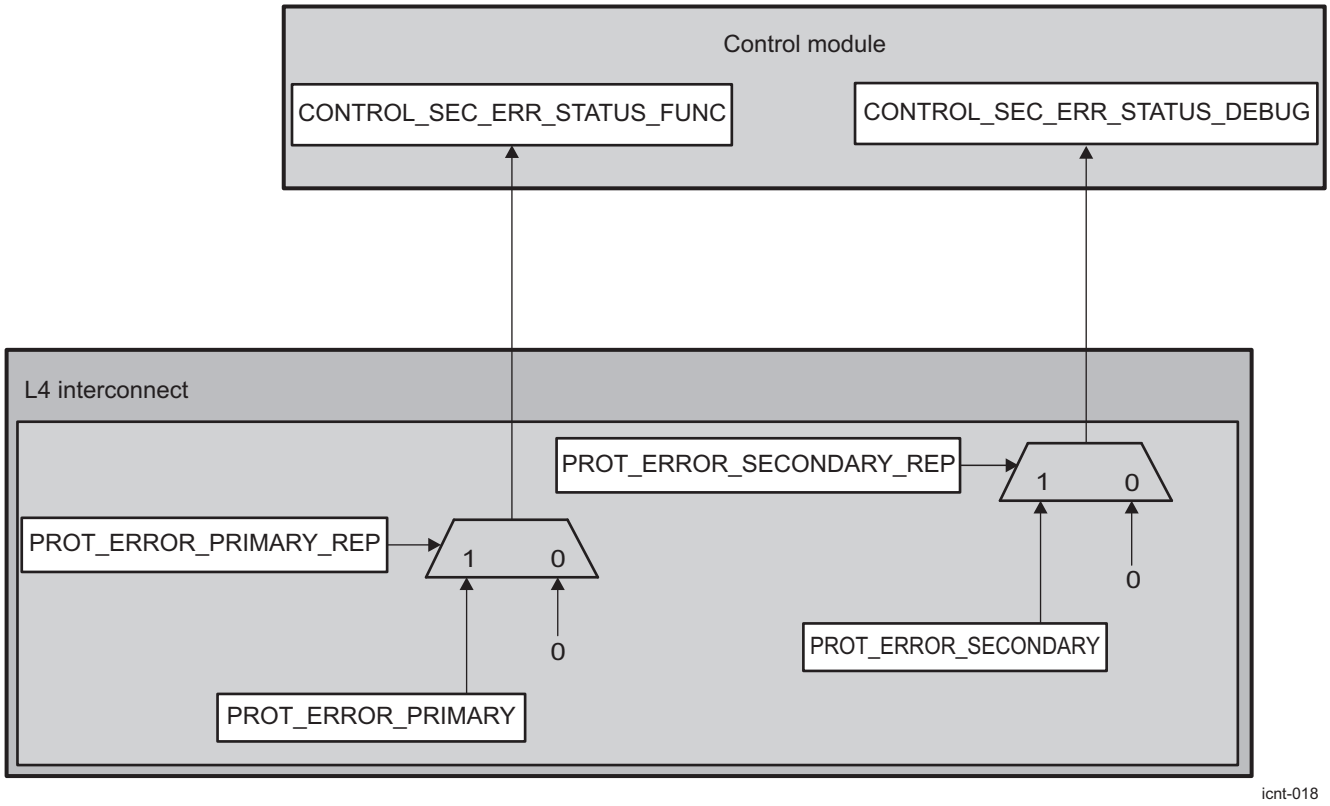
When a protection violation occurs, an interrupt is send to the INTCs (if enabled). An in-band error is sent back to L3 IA and an out-of-band error can also be logged in the CONTROL.CONTROL_SEC_ERR_STATUS register in the SCM. These out-of-band errors are enabled and disabled at the L4 IA level by setting the L4_IA_AGENT_CONTROL_L[31][30] PROT_ERROR_SECONDARY_REP or PROT_ERROR_PRIMARY_REP bit to 1 for debug and application mode, respectively.

At the control module level, two logging registers are used, depending on the mode:

- In application mode or primary error reporting:
  - SEC_ERR_STATUS_FUNC_1[16] = L4_PER1 protection violation
  - SEC_ERR_STATUS_FUNC_2[4] = L4_PER2 protection violation
  - SEC_ERR_STATUS_FUNC_2[5] = L4_PER3 protection violation
  - SEC_ERR_STATUS_FUNC_1[17] = L4_CFG protection violation
  - SEC_ERR_STATUS_FUNC_1[22] = L4_WKUP protection violation
- In debug mode or secondary error reporting:
  - SEC_ERR_STATUS_DEBUG_1[16] = L4_PER1 protection violation
  - SEC_ERR_STATUS_DEBUG_2[4] = L4_PER2 protection violation
  - SEC_ERR_STATUS_DEBUG_2[5] = L4_PER3 protection violation
  - SEC_ERR_STATUS_DEBUG_1[17] = L4_CFG protection violation
  - SEC_ERR_STATUS_DEBUG_1[22] = L4_WKUP protection violation

Figure 14-14 shows the global protection error reporting to the control module.

Figure 14-14. Protection Violation Out-of-Band Error Reporting



14.3.4 L4 Interconnect Programming Guide

14.3.4.1 L4 Interconnect Low-level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L4 interconnect module.

14.3.4.1.1 Global Initialization

14.3.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the L4 interconnect module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the L4 interconnect. For more information, see Section 14.3.2, *L4 Interconnect Integration*.

Table 14-408 lists the surrounding modules.

Table 14-408. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For more information about the configuration of the module, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	For more information about the configuration of the module, see Chapter 18, *Control Module*.
Device INTCs	Device INTCs must be configured to enable the interrupt request generation. For more information see Chapter 17, *Interrupt Controllers*.
IRQ_CROSSBAR	IRQ_CROSSBAR configuration must be done to allow module IRQs to be mapped to certain device INTC line. For more information see Section 18.4.6.4, *IRQ_CROSSBAR Module Functional Description*, in Chapter 18, *Control Module*.
L3 interconnect	For more information about the interconnect configuration, see Section 14.2, *L3 Interconnect*.

14.3.4.1.2 Operational Modes Configuration

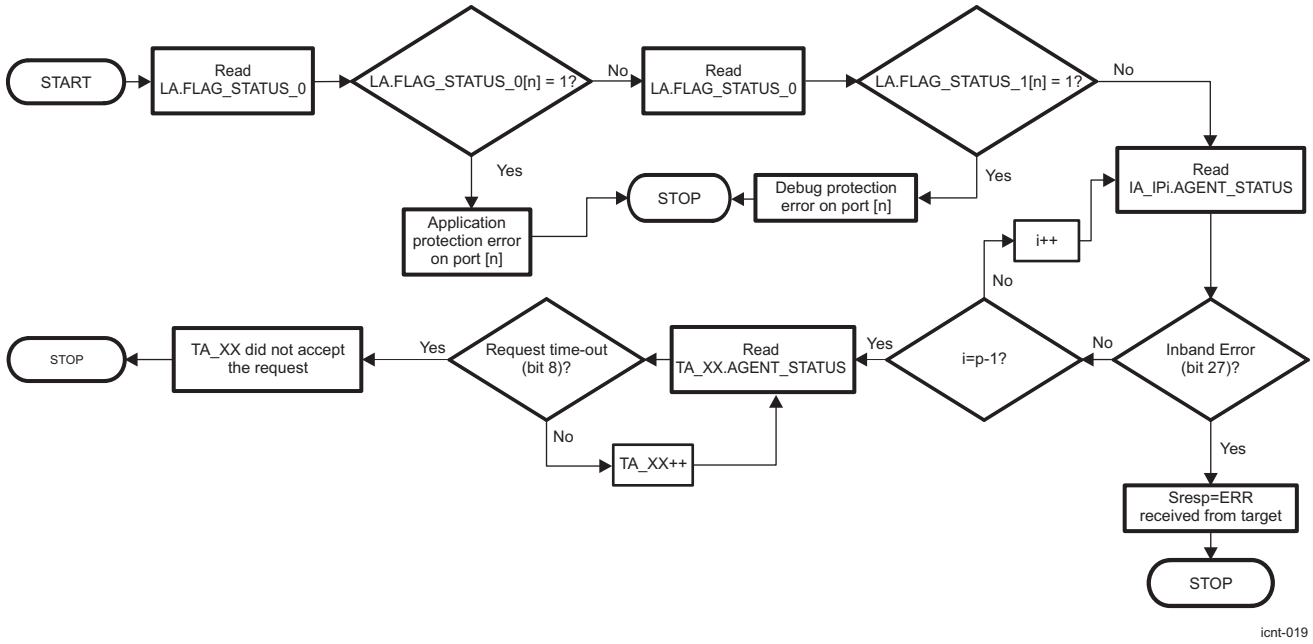
14.3.4.1.2.1 L4 Interconnect Error Analysis Mode

14.3.4.1.2.1.1 Main Sequence: L4 Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers. The number of registers to access depends on the error source.

Figure 14-15 shows the software sequence required in most cases.

Figure 14-15. Typical Error Analysis Sequence



NOTE: L4 interconnects don't log any address or other specific information for a custom error returned from any target IP. They rather pass an error response up to the master supposed to analyze it.

In case of posted writes, the master access completes before it actually completed at the end slave level, this way no error response is sent back to the master, making it impossible to have a direct way of uderstanding the origin of L4 error during posted writes. However, even though no address is logged, an error flag is generated and needs to be processed.

14.3.4.1.2.1.2 Subsequence: L4 Interconnect Protection Violation Error Identification

This procedure describes the protection violation error identification (see Table 14-409).

Table 14-409. Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	x
Read initiator ID.	L4_IA_ERROR_LOG_L[13:8] CONNID	xxxxx
Read command that cause the error.	L4_IA_ERROR_LOG_L[2:0] CMD	xxx
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	xxxxxxxxx
IF: Is it a primary error?	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	=0x1
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC	xx
Write 1 to clear status bits.	CONTROL.SEC_ERR_STATUS_FUNC_1 [16][17][22] CONTROL.SEC_ERR_STATUS_FUNC_2 [4][5]	xxxx
Write 1 to clear IA status bit.	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	0x1
ELSE		
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG	xx

Table 14-409. Protection Violation Error Identification (continued)

Step	Register/Bit Field/Programming Model	Value
Write 1 to clear status bits.	CONTROL.SEC_ERR_STATUS_DEBUG_1 [16][17][22] CONTROL.SEC_ERR_STATUS_DEBUG_2 [4][5]	xxx
Write 1 to clear IA status bit	L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY	0x1
ENDIF		
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear in-band error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

14.3.4.1.2.1.3 Subsequence: L4 Interconnect Unsupported Command/Address Hole Error Identification

This procedure describes the identification of unsupported command/address hole error (see Table 14-410).

Table 14-410. Unsupported Command/Address Hole Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	x
Read initiator ID.	L4_IA_ERROR_LOG_L[11:8] CONNID	xxxx
Read command that caused the error.	L4_IA_ERROR_LOG_L[2:0] CMD	xxx
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	xxxxxxxx
Read secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	x
Write 1 to clear secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	0x1
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear inband error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

14.3.4.1.2.1.4 Subsequence: L4 Interconnect Reset TA and Module

This procedure describes the reset TA and module (see Table 14-411).

Table 14-411. Reset TA and Module

Step	Register/Bit Field/Programming Model	Value
Reset TA.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x1
Wait until target module clock = 16 cycles.		
Write 0 to clear TA time-out status.	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	0x0
Write 0 to clear TA reset.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x0
Reset the attached module.(1)		

(1) For more information, see the respective module chapter.

14.3.4.1.2.2 L4 Interconnect Time-Out Configuration Mode

14.3.4.1.2.2.1 Main Sequence: L4 Interconnect Time-Out Configuration Mode

This procedure describes the time-out configuration sequence (see Table 14-412).

Table 14-412. Time-Out Configuration

Step	Register/Bit Field/Programming Model	Value
Disable time-out.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	0x0

Table 14-412. Time-Out Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Clear TA time-out error status.(1)	L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT	0x1
Set time-out at TA level.(1)	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	xxx
Set time-out base.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	xxx

(1) Required for each TA.

14.3.4.1.2.3 L4 Interconnect Firewall Configuration Mode

14.3.4.1.2.3.1 Main Sequence: L4 Interconnect Firewall Configuration Mode

This procedure describes the firewall configuration sequence (see Table 14-413).

Table 14-413. Firewall Configuration

Step	Register/Bit Field/Programming Model	Value
Define the members of protection group k.(1)	L4_AP_PROT_GROUP_MEMBERS_k_L[15:0] CONNID_BIT_VECTOR	xxx
Define the access type of a protection group k.(1)	L4_AP_PROT_GROUP_ROLES_k_L[15:0] ENABLE	xx
Set region affiliation to protection group.(2)	L4_AP_REGION_I_L[22:20] PROT_GROUP_ID	xxx

(1) Required for each protection group.
(2) Required for each region.

14.3.5 L4 Interconnects Register Manual

Table 14-414 through Table 14-418 list all L4 register blocks for IA, TA, AP, and LA. Each module instance is shown with the module register mapping and bit and bit field definitions.

14.3.5.1 L4 Interconnects Instance Summary

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-414. L4_PER1 Instance Summary

Module Name	L3_MAIN Base Address	Size
PER1_AP	0x4800 0000	2KB
PER1_LA	0x4800 0800	512B
PER1_IA_IP0	0x4800 1000	128B
PER1_IA_IP1	0x4800 1400	128B
PER1_IA_IP2	0x4800 1800	128B
UART3_TARG	0x4802 1000	64B
TIMER2_TARG	0x4803 3000	64B
TIMER3_TARG	0x4803 5000	64B
TIMER4_TARG	0x4803 7000	64B
TIMER9_TARG	0x4803 F000	64B
GPIO7_TARG	0x4805 2000	64B
GPIO8_TARG	0x4805 4000	64B
GPIO2_TARG	0x4805 6000	64B
GPIO3_TARG	0x4805 8000	64B
GPIO4_TARG	0x4805 A000	64B
GPIO5_TARG	0x4805 C000	64B
GPIO6_TARG	0x4805 E000	64B
I2C3_TARG	0x4806 1000	64B
UART5_TARG	0x4806 7000	64B
UART6_TARG	0x4806 9000	64B
UART1_TARG	0x4806 B000	64B
UART2_TARG	0x4806 D000	64B
UART4_TARG	0x4806 F000	64B
I2C1_TARG	0x4807 1000	64B
I2C2_TARG	0x4807 3000	64B
ELM_TARG	0x4807 9000	64B
I2C4_TARG	0x4807 B000	64B
I2C5_TARG	0x4807 D000	64B
TIMER10_TARG	0x4808 7000	64B
TIMER11_TARG	0x4808 9000	64B
MCSPI1_TARG	0x4809 9000	64B
MCSPI2_TARG	0x4809 B000	64B
MCSPI3_TARG	0x480B 9000	64B
MCSPI4_TARG	0x480B B000	64B
HDQ1W_TARG	0x480B 3000	64B
MMC1_TARG	0x4809 D000	64B
MMC2_TARG	0x480B 5000	64B
MMC3_TARG	0x480A E000	64B

Table 14-414. L4_PER1 Instance Summary (continued)

Module Name	L3_MAIN Base Address	Size
MMC4_TARG	0x480D 2000	64B

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-415. L4_PER2 Instance Summary

Module Name	L3_MAIN Base Address	Size
PER2_AP	0x4840 0000	2KBytes
PER2_LA	0x4840 0800	512Bytes
PER2_IA_IP0	0x4840 1000	128Bytes
PER2_IA_IP1	0x4840 1400	128Bytes
PER2_IA_IP2	0x4840 1800	128Bytes
UART7_TARG	0x4842 1000	64Bytes
UART8_TARG	0x4842 3000	64Bytes
UART9_TARG	0x4842 5000	64Bytes
MLB_TARG	0x4842 D000	64Bytes
MCASP4_DAT_TARG	0x4843 7000	64Bytes
MCASP5_DAT_TARG	0x4843 B000	64Bytes
MCASP6_DAT_TARG	0x4844 D000	64Bytes
MCASP7_DAT_TARG	0x4845 1000	64Bytes
MCASP8_DAT_TARG	0x4845 5000	64Bytes
MCASP1_CFG_TARG	0x4846 2000	64Bytes
MCASP2_CFG_TARG	0x4846 6000	64Bytes
MCASP3_CFG_TARG	0x4846 A000	64Bytes
MCASP4_CFG_TARG	0x4846 E000	64Bytes
MCASP5_CFG_TARG	0x4847 2000	64Bytes
MCASP6_CFG_TARG	0x4847 6000	64Bytes
MCASP7_CFG_TARG	0x4847 A000	64Bytes
MCASP8_CFG_TARG	0x4847 E000	64Bytes
ATL_TARG	0x4843 D000	64Bytes
PWM1_TARG	0x4843 F000	64Bytes
PWM2_TARG	0x4844 1000	64Bytes
PWM3_TARG	0x4844 3000	64Bytes
VCP1_CFG_TARG	0x4844 7000	64Bytes
VCP2_CFG_TARG	0x4844 9000	64Bytes
DCAN2_TARG	0x4848 2000	64Bytes
GMAC_TARG	0x4848 8000	64Bytes

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-416. L4_PER3 Instance Summary

Module Name	L3_MAIN Base Address	Size
PER3_AP	0x4880 0000	2KBytes
PER3_LA	0x4880 0800	512Bytes

Table 14-416. L4_PER3 Instance Summary (continued)

Module Name	L3_MAIN Base Address	Size
PER3_IA_IP0	0x4880 1000	128Bytes
PER3_IA_IP1	0x4880 1400	128Bytes
PER3_IA_IP2	0x4880 1800	128Bytes
MBX13_TARG	0x4880 3000	64Bytes
OCMC_RAM1_TARG	0x4880 5000	64Bytes
OCMC_RAM2_TARG	0x4880 B000	64Bytes
OCMC_RAM3_TARG	0x4881 1000	64Bytes
MMU1_TARG	0x4881 D000	64Bytes
MMU2_TARG	0x4881 F000	64Bytes
TIMER5_TARG	0x4882 1000	64Bytes
TIMER6_TARG	0x4882 3000	64Bytes
TIMER7_TARG	0x4882 5000	64Bytes
TIMER8_TARG	0x4882 7000	64Bytes
TIMER13_TARG	0x4882 9000	64Bytes
TIMER14_TARG	0x4882 B000	64Bytes
TIMER15_TARG	0x4882 D000	64Bytes
TIMER16_TARG	0x4882 F000	64Bytes
MBX2_TARG	0x4883 B000	64Bytes
MBX3_TARG	0x4883 D000	64Bytes
MBX4_TARG	0x4883 F000	64Bytes
MBX5_TARG	0x4884 1000	64Bytes
MBX6_TARG	0x4884 3000	64Bytes
MBX7_TARG	0x4884 5000	64Bytes
MBX8_TARG	0x4884 7000	64Bytes
MBX9_TARG	0x4885 F000	64Bytes
MBX10_TARG	0x4886 1000	64Bytes
MBX11_TARG	0x4886 3000	64Bytes
MBX12_TARG	0x4886 5000	64Bytes
VIP1_TARG	0x4898 0000	64Bytes
VIP2_TARG	0x489A 0000	64Bytes
VIP3_TARG	0x489C 0000	64Bytes
VPE_TARG	0x489E 0000	64Bytes
RTC_TARG	0x4883 9000	64Bytes
USB4_TARG	0x4896 0000	64Bytes
USB2_TARG	0x488E 0000	64Bytes
USB1_TARG	0x488A 0000	64Bytes
USB3_TARG	0x4892 0000	64Bytes

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-417. L4_CFG Instance Summary

Module Name	L3_MAIN Base Address	Size
CFG_AP	0x4A00 0000	2KBytes
CFG_LA	0x4A00 0800	64Bytes
CFG_IA_IP0	0x4A00 1000	128Bytes

Table 14-417. L4_CFG Instance Summary (continued)

Module Name	L3_MAIN Base Address	Size
CTRL_MODULE_CORE_TARG	0x4A00 4000	64Bytes
CM_CORE_AON_TARG	0x4A00 6000	64Bytes
CM_CORE_TARG	0x4A00 A000	64Bytes
SCP1_TARG	0x4A08 8000	64Bytes
SCP3_TARG	0x4A09 8000	64Bytes
SCP2_TARG	0x4A0A 8000	64Bytes
MAILBOX_TARG	0x4A0F 5000	64Bytes
SPINLOCK_TARG	0x4A0F 7000	64Bytes
OCP_WP_NOC_TARG	0x4A10 3000	64Bytes
EVE1_FW_CFG_TARG	0x4A15 2000	64Bytes
EVE2_FW_CFG_TARG	0x4A15 4000	64Bytes
EVE3_FW_CFG_TARG	0x4A15 6000	64Bytes
EVE4_FW_CFG_TARG	0x4A15 8000	64Bytes
IPU1_FW_CFG_TARG	0x4A15 C000	64Bytes
VCP1_FW_CFG_TARG	0x4A15 E000	64Bytes
VCP2_FW_CFG_TARG	0x4A16 0000	64Bytes
TPCC_FW_CFG_TARG	0x4A16 2000	64Bytes
TPTC_FW_CFG_TARG	0x4A16 4000	64Bytes
PCIESS1_FW_CFG_TARG	0x4A16 6000	64Bytes
DSP1_SDMA_FW_CFG_TARG	0x4A17 2000	64Bytes
DSP2_SDMA_FW_CFG_TARG	0x4A17 4000	64Bytes
PRUSS1_FW_CFG_TARG	0x4A17 6000	64Bytes
QSPI_FW_CFG_TARG	0x4A17 A000	64Bytes
MA_MPU_NTTP_FW_CFG_TARG	0x4A20 B000	64Bytes
EMIF_OCP_FW_CFG_TARG	0x4A20 D000	64Bytes
OCMC_RAM2_FW_CFG_TARG	0x4A20 F000	64Bytes
GPMC_FW_CFG_TARG	0x4A21 1000	64Bytes
OCMC_RAM1_FW_CFG_TARG	0x4A21 3000	64Bytes
GPU_FW_CFG_TARG	0x4A21 5000	64Bytes
DSS_FW_CFG_TARG	0x4A21 D000	64Bytes
IVA_SL2IF_FW_CFG_TARG	0x4A21 F000	64Bytes
IVA_CONFIG_FW_CFG_TARG	0x4A22 1000	64Bytes
DEBUGSS_CT_TBR_FW_CFG_TARG	0x4A22 5000	64Bytes
L3_INSTR_FW_CFG_TARG	0x4A22 7000	64Bytes
OCMC_RAM3_FW_CFG_TARG	0x4A22 B000	64Bytes
DMA_SYSTEM_TARG	0x4A05 7000	64Bytes
PCIESS2_FW_CFG_TARG	0x4A15 A000	64Bytes
PRUSS2_FW_CFG_TARG	0x4A17 8000	64Bytes
MCASP1_FW_CFG_TARG	0x4A16 8000	64Bytes
MCASP2_FW_CFG_TARG	0x4A16 A000	64Bytes
MCASP3_FW_CFG_TARG	0x4A16 C000	64Bytes
IPU2_FW_CFG_TARG	0x4A21 9000	64Bytes

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 14-418. L4_WKUP Instance Summary

Module Name	L3_MAIN Base Address	Size
WKUP_AP	0x4AE0 0000	2KBytes
WKUP_LA	0x4AE0 0800	64Bytes
WKUP_IA_IP0	0x4AE0 1000	128Bytes
COUNTER_32K_TARG	0x4AE0 5000	64Bytes
PRM_TARG	0x4AE0 8000	64Bytes
CTRL_MODULE_WKUP_TARG	0x4AE0 D000	64Bytes
GPIO1_TARG	0x4AE1 1000	64Bytes
WD_TIMER2_TARG	0x4AE1 5000	64Bytes
TIMER1_TARG	0x4AE1 9000	64Bytes
KBD_TARG	0x4AE1 D000	64Bytes
TIMER12_TARG	0x4AE2 1000	64Bytes
UART10_TARG	0x4AE2 C000	64Bytes
DCAN1_TARG	0x4AE3 E000	64Bytes

14.3.5.2 L4 Initiator Agent (L4 IA)

14.3.5.2.1 L4 Initiator Agent (L4 IA) Register Summary

Table 14-419 summarizes the L4 IA register mapping.

Table 14-419. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER1_IA_IP0 L3_MAIN Physical Address	PER1_IA_IP1 L3_MAIN Physical Address	PER1_IA_IP2 L3_MAIN Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4800 1000	0x4800 1400	0x4800 1800
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4800 1004	0x4800 1404	0x4800 1804
L4_IA_CORE_L	R	32	0x0000 0018	0x4800 1018	0x4800 1418	0x4800 1818
L4_IA_CORE_H	R	32	0x0000 001C	0x4800 101C	0x4800 141C	0x4800 181C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4800 1020	0x4800 1420	0x4800 1820
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4800 1024	0x4800 1424	0x4800 1824
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4800 1028	0x4800 1428	0x4800 1828
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4800 102C	0x4800 142C	0x4800 182C
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4800 1058	0x4800 1458	0x4800 1858
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4800 105C	0x4800 145C	0x4800 185C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4800 1060	0x4800 1460	0x4800 1860
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4800 1064	0x4800 1464	0x4800 1864

Table 14-420. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER2_IA_IP0 L3_MAIN Physical Address	PER2_IA_IP1 L3_MAIN Physical Address	PER2_IA_IP2 L3_MAIN Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4840 1000	0x4840 1400	0x4840 1800
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4840 1004	0x4840 1404	0x4840 1804
L4_IA_CORE_L	R	32	0x0000 0018	0x4840 1018	0x4840 1418	0x4840 1818
L4_IA_CORE_H	R	32	0x0000 001C	0x4840 101C	0x4840 141C	0x4840 181C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4840 1020	0x4840 1420	0x4840 1820
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4840 1024	0x4840 1424	0x4840 1824
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4840 1028	0x4840 1428	0x4840 1828
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4840 102C	0x4840 142C	0x4840 182C

Table 14-420. IA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER2_IA_IP0 L3_MAIN Physical Address	PER2_IA_IP1 L3_MAIN Physical Address	PER2_IA_IP2 L3_MAIN Physical Address
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4840 1058	0x4840 1458	0x4840 1858
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4840 105C	0x4840 145C	0x4840 185C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4840 1060	0x4840 1460	0x4840 1860
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4840 1064	0x4840 1464	0x4840 1864

Table 14-421. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER3_IA_IP0 L3_MAIN Physical Address	PER3_IA_IP1 L3_MAIN Physical Address	PER3_IA_IP2 L3_MAIN Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4880 1000	0x4880 1400	0x4880 1800
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4880 1004	0x4880 1404	0x4880 1804
L4_IA_CORE_L	R	32	0x0000 0018	0x4880 1018	0x4880 1418	0x4880 1818
L4_IA_CORE_H	R	32	0x0000 001C	0x4880 101C	0x4880 141C	0x4880 181C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4880 1020	0x4880 1420	0x4880 1820
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4880 1024	0x4880 1424	0x4880 1824
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4880 1028	0x4880 1428	0x4880 1828
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4880 102C	0x4880 142C	0x4880 182C
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4880 1058	0x4880 1458	0x4880 1858
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4880 105C	0x4880 145C	0x4880 185C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4880 1060	0x4880 1460	0x4880 1860
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4880 1064	0x4880 1464	0x4880 1864

Table 14-422. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CFG_IA_IP0 L3_MAIN Physical Address	WKUP_IA_IP0 L3_MAIN Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4A00 1000	0x4AE0 1000
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4A00 1004	0x4AE0 1004
L4_IA_CORE_L	R	32	0x0000 0018	0x4A00 1018	0x4AE0 1018
L4_IA_CORE_H	R	32	0x0000 001C	0x4A00 101C	0x4AE0 101C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A00 1020	0x4AE0 1020
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A00 1024	0x4AE0 1024
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4A00 1028	0x4AE0 1028
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A00 102C	0x4AE0 102C
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4A00 1058	0x4AE0 1058
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4A00 105C	0x4AE0 105C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4A00 1060	0x4AE0 1060
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4A00 1064	0x4AE0 1064

14.3.5.2.2 L4 Initiator Agent (L4 IA) Register Description

Table 14-423 through Table 14-445 describe the L4 IA registers.

Table 14-423. L4_IA_COMPONENT_L

Address Offset	0x0000 0000		
Physical Address	0x4800 1000	**Instance**	PER1_IA_IP0
	0x4800 1400		PER1_IA_IP1
	0x4800 1800		PER1_IA_IP2
	0x4840 1000		PER2_IA_IP0
	0x4840 1400		PER2_IA_IP1
	0x4840 1800		PER2_IA_IP2
	0x4880 1000		PER3_IA_IP0
	0x4880 1400		PER3_IA_IP1
	0x4880 1800		PER3_IA_IP2
	0x4A00 1000		CFG_IA_IP0
	0x4AE0 1000		WKUP_IA_IP0
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R	See(1).

(1) TI Internal Data

Table 14-424. Register Call Summary for Register L4_IA_COMPONENT_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-425. L4_IA_COMPONENT_H

Address Offset	0x0000 0004		
Physical Address	0x4800 1004	**Instance**	PER1_IA_IP0
	0x4800 1404		PER1_IA_IP1
	0x4800 1804		PER1_IA_IP2
	0x4840 1004		PER2_IA_IP0
	0x4840 1404		PER2_IA_IP1
	0x4840 1804		PER2_IA_IP2
	0x4880 1004		PER3_IA_IP0
	0x4880 1404		PER3_IA_IP1
	0x4880 1804		PER3_IA_IP2
	0x4A00 1004		CFG_IA_IP0
	0x4AE0 1004		WKUP_IA_IP0
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000

Table 14-426. Register Call Summary for Register L4_IA_COMPONENT_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-427. L4_IA_CORE_L

Address Offset	0x0000 0018		
Physical Address	0x4800 1018	**Instance**	PER1_IA_IP0
	0x4800 1418		PER1_IA_IP1
	0x4800 1818		PER1_IA_IP2
	0x4840 1018		PER2_IA_IP0
	0x4840 1418		PER2_IA_IP1
	0x4840 1818		PER2_IA_IP2
	0x4880 1018		PER3_IA_IP0
	0x4880 1418		PER3_IA_IP1
	0x4880 1818		PER3_IA_IP2
	0x4A00 1018		CFG_IA_IP0
	0x4AE0 1018		WKUP_IA_IP0
Description	Provide information about the core initiator		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																REV_CODE															

Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See(1).

(1) TI Internal Data

Table 14-428. Register Call Summary for Register L4_IA_CORE_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-429. L4_IA_CORE_H

Address Offset	0x0000 001C		
Physical Address	0x4800 101C	**Instance**	PER1_IA_IP0
	0x4800 141C		PER1_IA_IP1
	0x4800 181C		PER1_IA_IP2
	0x4840 101C		PER2_IA_IP0
	0x4840 141C		PER2_IA_IP1
	0x4840 181C		PER2_IA_IP2
	0x4880 101C		PER3_IA_IP0
	0x4880 141C		PER3_IA_IP1
	0x4880 181C		PER3_IA_IP2
	0x4A00 101C		CFG_IA_IP0
	0x4AE0 101C		WKUP_IA_IP0
Description	Provide information about the core initiator		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 14-430. Register Call Summary for Register L4_IA_CORE_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-431. L4_IA_AGENT_CONTROL_L

Address Offset	0x0000 0020		
Physical Address	0x4800 1020	**Instance**	PER1_IA_IP0
	0x4800 1420		PER1_IA_IP1
	0x4800 1820		PER1_IA_IP2
	0x4840 1020		PER2_IA_IP0
	0x4840 1420		PER2_IA_IP1
	0x4840 1820		PER2_IA_IP2
	0x4880 1020		PER3_IA_IP0
	0x4880 1420		PER3_IA_IP1
	0x4880 1820		PER3_IA_IP2
	0x4A00 1020		CFG_IA_IP0
	0x4AE0 1020		WKUP_IA_IP0
Description	Core control for an initiator OCP interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY_REP	PROT_ERROR_PRIMARY_REP	RESERVED		INBAND_ERROR_REP	RESERVED		MERROR_REP	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY_REP	Out-of-band reporting of protection mechanism secondary errors	RW	1
30	PROT_ERROR_PRIMARY_REP	Out-of-band reporting of protection mechanism primary errors	RW	1
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR_REP	Setting this field to 1 reports on in-band errors using the INBAND_ERROR log bit of IA.AGENT_STATUS register. The error reporting mechanism is enabled when the INBAND_ERROR_REP bit field is set to 1.	RW	1
26:25	RESERVED	Read returns 0.	R	0x0
24	MERROR_REP	OCP MError reporting control. The out-of-band OCP MError reporting mechanism is enabled when the MERROR_REP bit field is set to 1.	R	0
23:0	RESERVED		R	0x0

Table 14-432. Register Call Summary for Register L4_IA_AGENT_CONTROL_L

L4 Interconnects

- Firewall Error Logging in the Control Module: [0]
- L4 Initiator Agent (L4 IA) Register Summary: [1] [2] [3] [4]

Table 14-433. L4_IA_AGENT_CONTROL_H

Address Offset	0x0000 0024		
Physical Address	0x4800 1024	**Instance**	PER1_IA_IP0
	0x4800 1424		PER1_IA_IP1
	0x4800 1824		PER1_IA_IP2
	0x4840 1024		PER2_IA_IP0
	0x4840 1424		PER2_IA_IP1
	0x4840 1824		PER2_IA_IP2
	0x4880 1024		PER3_IA_IP0
	0x4880 1424		PER3_IA_IP1
	0x4880 1824		PER3_IA_IP2
	0x4A00 1024		CFG_IA_IP0
	0x4AE0 1024		WKUP_IA_IP0
Description	Enable error reporting on an initiator interface.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-434. Register Call Summary for Register L4_IA_AGENT_CONTROL_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-435. L4_IA_AGENT_STATUS_L

Address Offset	0x0000 0028		
Physical Address	0x4800 1028	**Instance**	PER1_IA_IP0
	0x4800 1428		PER1_IA_IP1
	0x4800 1828		PER1_IA_IP2
	0x4840 1028		PER2_IA_IP0
	0x4840 1428		PER2_IA_IP1
	0x4840 1828		PER2_IA_IP2
	0x4880 1028		PER3_IA_IP0
	0x4880 1428		PER3_IA_IP1
	0x4880 1828		PER3_IA_IP2
	0x4A00 1028		CFG_IA_IP0
	0x4AE0 1028		WKUP_IA_IP0
Description	Stores status information for an initiator. The INBAND_ERROR and MERROR fields are read/write and are implemented as log bits.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY	PROT_ERROR_PRIMARY	RESERVED		INBAND_ERROR	RESERVED		MERROR	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY	0x0: Secondary Protection error not present.0x1: Secondary Protection error present	RW W1toClr	0
30	PROT_ERROR_PRIMARY	0x0: Primary Protection error not present.0x1: Primary Protection error present	RW W1toClr	0
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR	0x0 No In-Band error present.0x1 In-Band error present.	RW W1toClr	0
26:25	RESERVED	Read returns 0.	R	0x0
24	MERROR	Value of the OCP MError signal	R	0
23:0	RESERVED	Read returns 0	R	0X0

Table 14-436. Register Call Summary for Register L4_IA_AGENT_STATUS_L

L4 Interconnects
- IA and TA Error Detection and Logging: [0] [1] [2] [3]
- Operational Modes Configuration: [4] [5] [6] [7] [8]
- L4 Initiator Agent (L4 IA) Register Summary: [9] [10] [11] [12]

Table 14-437. L4_IA_AGENT_STATUS_H

Address Offset	0x0000 002C		
Physical Address	0x4800 102C 0x4800 142C 0x4800 182C 0x4840 102C 0x4840 142C 0x4840 182C 0x4880 102C 0x4880 142C 0x4880 182C 0x4A00 102C 0x4AE0 102C	**Instance**	PER1_IA_IP0 PER1_IA_IP1 PER1_IA_IP2 PER2_IA_IP0 PER2_IA_IP1 PER2_IA_IP2 PER3_IA_IP0 PER3_IA_IP1 PER3_IA_IP2 CFG_IA_IP0 WKUP_IA_IP0
Description	Stores status information for an initiator.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-438. Register Call Summary for Register L4_IA_AGENT_STATUS_H

L4 Interconnects
- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

Table 14-439. L4_IA_ERROR_LOG_L

Address Offset	0x0000 0058		
Physical Address	0x4800 1058	**Instance**	PER1_IA_IP0
	0x4800 1458		PER1_IA_IP1
	0x4800 1858		PER1_IA_IP2
	0x4840 1058		PER2_IA_IP0
	0x4840 1458		PER2_IA_IP1
	0x4840 1858		PER2_IA_IP2
	0x4880 1058		PER3_IA_IP0
	0x4880 1458		PER3_IA_IP1
	0x4880 1858		PER3_IA_IP2
	0x4A00 1058		CFG_IA_IP0
	0x4AE0 1058		WKUP_IA_IP0
Description	Log information about error conditions. The CODE field logs any protection violation or address hole errors detected by the initiator subsystem while decoding a request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTI	SECONDARY	RESERVED				CODE		RESERVED								CONNID								RESERVED						CMD	

Bits	Field Name	Description	Type	Reset
31	MULTI	Multiple errors detected	RW W1toClr	0
30	SECONDARY	Indicates whether protection violation was a primary or secondary error	RW W1toClr	0
29:26	RESERVED	Read returns 0.	R	0x0
25:24	CODE	The error code of an initiator request. 0x00: No errors 0x01: Reserved 0x10: Address hole 0x11: Protection violation	RW W1toClr	0x0
23:14	RESERVED	Read returns 0.	R	0x000
13:8	CONNID	ConnID of request causing the error, refer to Table 14-394	R	0x00
7:3	RESERVED	Read returns 0.	R	0x00
2:0	CMD	Command that caused error	R	0x0

Table 14-440. Register Call Summary for Register L4_IA_ERROR_LOG_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0] [1] [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- L4 Initiator Agent (L4 IA) Register Summary: [16] [17] [18] [19]

Table 14-441. L4_IA_ERROR_LOG_H

Address Offset	0x0000 005C		
Physical Address	0x4800 105C	**Instance**	PER1_IA_IP0
	0x4800 145C		PER1_IA_IP1
	0x4800 185C		PER1_IA_IP2
	0x4840 105C		PER2_IA_IP0
	0x4840 145C		PER2_IA_IP1
	0x4840 185C		PER2_IA_IP2
	0x4880 105C		PER3_IA_IP0
	0x4880 145C		PER3_IA_IP1
	0x4880 185C		PER3_IA_IP2
	0x4A00 105C		CFG_IA_IP0
	0x4AE0 105C		WKUP_IA_IP0
Description	Log information about error conditions.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REQ_INFO															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0x0000
15:0	REQ_INFO	MReqInfo bits of request that caused the error REQ_INFO[0] = supervisor, REQ_INFO[1] = Debug	R	0x0000

Table 14-442. Register Call Summary for Register L4_IA_ERROR_LOG_H

L4 Interconnects

- IA and TA Error Detection and Logging: [0]
- L4 Initiator Agent (L4 IA) Register Summary: [1] [2] [3] [4]

Table 14-443. L4_IA_ERROR_LOG_ADDR_L

Address Offset	0x0000 0060		
Physical Address	0x4800 1060	**Instance**	PER1_IA_IP0
	0x4800 1460		PER1_IA_IP1
	0x4800 1860		PER1_IA_IP2
	0x4840 1060		PER2_IA_IP0
	0x4840 1460		PER2_IA_IP1
	0x4840 1860		PER2_IA_IP2
	0x4880 1060		PER3_IA_IP0
	0x4880 1460		PER3_IA_IP1
	0x4880 1860		PER3_IA_IP2
	0x4A00 1060		CFG_IA_IP0
	0x4AE0 1060		WKUP_IA_IP0
Description	Extended error log (address information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Address of request that caused the error. N is the number MAddr bits.	R	0x0000 0000

Table 14-444. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_L

L4 Interconnects
- IA and TA Error Detection and Logging: [0]
- Operational Modes Configuration: [1] [2]
- L4 Initiator Agent (L4 IA) Register Summary: [3] [4] [5] [6]

Table 14-445. L4_IA_ERROR_LOG_ADDR_H

Address Offset	0x0000 0064		
Physical Address	0x4800 1064	**Instance**	PER1_IA_IP0
	0x4800 1464		PER1_IA_IP1
	0x4800 1864		PER1_IA_IP2
	0x4840 1064		PER2_IA_IP0
	0x4840 1464		PER2_IA_IP1
	0x4840 1864		PER2_IA_IP2
	0x4880 1064		PER3_IA_IP0
	0x4880 1464		PER3_IA_IP1
	0x4880 1864		PER3_IA_IP2
	0x4A00 1064		CFG_IA_IP0
	0x4AE0 1064		WKUP_IA_IP0
Description	Extended error log (address information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-446. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_H

L4 Interconnects
- L4 Initiator Agent (L4 IA) Register Summary: [0] [1] [2] [3]

14.3.5.3 L4 Target Agent (L4 TA)

14.3.5.3.1 L4 Target Agent (L4 TA) Register Summary

Table 14-447 through Table 14-491 summarizes the L4 TA mapping of the CFG_TA, PER_TA, and WKUP_TA registers.

Table 14-447. CFG_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE _CORE_TARG L3_MAIN Physical Address	CM_CORE_AON _TARG L3_MAIN Physical Address	CM_CORE_TAR GL3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A00 4000	0x4A00 6000	0x4A00 A000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A00 4004	0x4A00 6004	0x4A00 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A00 4018	0x4A00 6018	0x4A00 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A00 401C	0x4A00 601C	0x4A00 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A00 4020	0x4A00 6020	0x4A00 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A00 4024	0x4A00 6024	0x4A00 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A00 4028	0x4A00 6028	0x4A00 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A00 402C	0x4A00 602C	0x4A00 A02C

Table 14-448. CFG_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	SCP1_TARG L3_MAIN Physical Address	SCP3_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A08 8000	0x4A09 8000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A08 8004	0x4A09 8004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A08 8018	0x4A09 8018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A08 801C	0x4A09 801C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A08 8020	0x4A09 8020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A08 8024	0x4A09 8024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A08 8028	0x4A09 8028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A08 802C	0x4A09 802C

Table 14-449. CFG_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	SCP2_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A0A 8000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A0A 8004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0A 8018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0A 801C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0A 8020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0A 8024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0A 8028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0A 802C

Table 14-450. CFG_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	MAILBOX_TARG L3_MAIN Physical Address	SPINLOCK_TARG L3_MAIN Physical Address	OCP_WP_NOC_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A0F 5000	0x4A0F 7000	0x4A10 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A0F 5004	0x4A0F 7004	0x4A10 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0F 5018	0x4A0F 7018	0x4A10 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0F 501C	0x4A0F 701C	0x4A10 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0F 5020	0x4A0F 7020	0x4A10 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0F 5024	0x4A0F 7024	0x4A10 3024
L4_TA_AGENT_STATUS_H	R	32	0x0000 0028	0x4A0F 5028	0x4A0F 7028	0x4A10 3028
L4_TA_AGENT_STATUS_L	R	32	0x0000 002C	0x4A0F 502C	0x4A0F 702C	0x4A10 302C

Table 14-451. CFG_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	EVE1_FW_CFG_TARG L3_MAIN Physical Address	EVE2_FW_CFG_TARG L3_MAIN Physical Address	EVE3_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A15 2000	0x4A15 4000	0x4A15 6000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A15 2004	0x4A15 4004	0x4A15 6004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A15 2018	0x4A15 4018	0x4A15 6018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A15 201C	0x4A15 401C	0x4A15 601C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A15 2020	0x4A15 4020	0x4A15 6020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A15 2024	0x4A15 4024	0x4A15 6024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A15 2028	0x4A15 4028	0x4A15 6028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A15 202C	0x4A15 402C	0x4A15 602C

Table 14-452. CFG_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	IPU1_FW_CFG_TARG L3_MAIN Physical Address	EVE4_FW_CFG_TARG L3_MAIN Physical Address	PRUSS1_FW_CFG_TARG L3_MAIN Physical Address	VCP1_FW_CFG_TARG L3_MAIN Physical Address	VCP2_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A15 C000	0x4A15 8000	0x4A17 6000	0x4A15 E000	0x4A16 0000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A15 C004	0x4A15 8004	0x4A17 6004	0x4A15 E004	0x4A16 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A15 C018	0x4A15 8018	0x4A17 6018	0x4A15 E018	0x4A16 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A15 C01C	0x4A15 801C	0x4A17 601C	0x4A15 E01C	0x4A16 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A15 C020	0x4A15 8020	0x4A17 6020	0x4A15 E020	0x4A16 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A15 C024	0x4A15 8024	0x4A17 6024	0x4A15 E024	0x4A16 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A15 C028	0x4A15 8028	0x4A17 6028	0x4A15 E028	0x4A16 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A15 C02C	0x4A15 802C	0x4A17 602C	0x4A15 E02C	0x4A16 002C

Table 14-453. CFG_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	TPCC_FW_CFG_TARG L3_MAIN Physical Address	TPTC_FW_CFG_TARG L3_MAIN Physical Address	PCIESS1_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A16 2000	0x4A16 4000	0x4A16 6000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A16 2004	0x4A16 4004	0x4A16 6004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A16 2018	0x4A16 4018	0x4A16 6018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A16 201C	0x4A16 401C	0x4A16 601C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A16 2020	0x4A16 4020	0x4A16 6020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A16 2024	0x4A16 4024	0x4A16 6024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A16 2028	0x4A16 4028	0x4A16 6028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A16 202C	0x4A16 402C	0x4A16 602C

Table 14-454. CFG_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	DSP1_SDMA_FW_CFG_TARG L3_MAIN Physical Address	DSP2_SDMA_FW_CFG_TARG L3_MAIN Physical Address	QSPI_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A17 2000	0x4A17 4000	0x4A17 A000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A17 2004	0x4A17 4004	0x4A17 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A17 2018	0x4A17 4018	0x4A17 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A17 201C	0x4A17 401C	0x4A17 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A17 2020	0x4A17 4020	0x4A17 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A17 2024	0x4A17 4024	0x4A17 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A17 2028	0x4A17 4028	0x4A17 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A17 202C	0x4A17 402C	0x4A17 A02C

Table 14-455. CFG_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	MA_MPU_NTTP_FW_CFG_TARG L3_MAIN Physical Address	EMIF_OCP_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A20 B000	0x4A20 D000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A20 B004	0x4A20 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A20 B018	0x4A20 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A20 B01C	0x4A20 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A20 B020	0x4A20 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A20 B024	0x4A20 D024

Table 14-455. CFG_TA Register Mapping Summary 9 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MA_MPU_NTTP_FW_CFG_TARG L3_MAIN Physical Address	EMIF_OCP_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A20 B028	0x4A20 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A20 B02C	0x4A20 D02C

Table 14-456. CFG_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	OCMC_RAM2_FW_CFG_TARG L3_MAIN Physical Address	GPMC_FW_CFG_TARG L3_MAIN Physical Address	OCMC_RAM1_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A20 F000	0x4A21 1000	0x4A21 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A20 F004	0x4A21 1004	0x4A21 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A20 F018	0x4A21 1018	0x4A21 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A20 F01C	0x4A21 101C	0x4A21 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A20 F020	0x4A21 1020	0x4A21 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A20 F024	0x4A21 1024	0x4A21 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A20 F028	0x4A21 1028	0x4A21 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A20 F02C	0x4A21 102C	0x4A21 302C

Table 14-457. CFG_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	GPU_FW_CFG_TARG L3_MAIN Physical Address	DSS_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A21 5000	0x4A21 D000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A21 5004	0x4A21 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 5018	0x4A21 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 501C	0x4A21 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 5020	0x4A21 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 5024	0x4A21 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 5028	0x4A21 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 502C	0x4A21 D02C

Table 14-458. CFG_TA Register Mapping Summary 12

Register Name	Type	Register Width (Bits)	Address Offset	IVA_SL2IF_FW_CFG_TARG L3_MAIN Physical Address	IVA_CONFIG_FW_CFG_TARG L3_MAIN Physical Address	DEBUGSS_CT_TBR_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A21 F000	0x4A22 1000	0x4A22 5000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A21 F004	0x4A22 1004	0x4A22 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 F018	0x4A22 1018	0x4A22 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 F01C	0x4A22 101C	0x4A22 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 F020	0x4A22 1020	0x4A22 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 F024	0x4A22 1024	0x4A22 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 F028	0x4A22 1028	0x4A22 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 F02C	0x4A22 102C	0x4A22 502C

Table 14-459. CFG_TA Register Mapping Summary 13

Register Name	Type	Register Width (Bits)	Address Offset	L3_INSTR_FW_CFG_TARG L3_MAIN Physical Address	OCMC_RAM3_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A22 7000	0x4A22 B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A22 7004	0x4A22 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A22 7018	0x4A22 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A22 701C	0x4A22 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A22 7020	0x4A22 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A22 7024	0x4A22 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A22 7028	0x4A22 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A22 702C	0x4A22 B02C

Table 14-460. CFG_TA Register Mapping Summary 14

Register Name	Type	Register Width (Bits)	Address Offset	DMA_SYSTEM_TARG L3_MAIN Physical Address	PCIESS2_FW_CFG_TARG L3_MAIN Physical Address	PRUSS2_FW_CFG_TARG L3_MAIN Physical Address	MCASP1_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A05 7000	0x4A15 A000	0x4A17 8000	0x4A16 8000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A05 7004	0x4A15 A004	0x4A17 8004	0x4A16 8004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A05 7018	0x4A15 A018	0x4A17 8018	0x4A16 8018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A05 701C	0x4A15 A01C	0x4A17 801C	0x4A16 801C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A05 7020	0x4A15 A020	0x4A17 8020	0x4A16 8020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A05 7024	0x4A15 A024	0x4A17 8024	0x4A16 8024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A05 7028	0x4A15 A028	0x4A17 8028	0x4A16 8028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A05 702C	0x4A15 A02C	0x4A17 802C	0x4A16 802C

Table 14-461. CFG_TA Register Mapping Summary 15

Register Name	Type	Register Width (Bits)	Address Offset	MCASP2_FW_CFG_TARG L3_MAIN Physical Address	MCASP3_FW_CFG_TARG L3_MAIN Physical Address	IPU2_FW_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A16 A000	0x4A16 C000	0x4A21 9000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4A16 A004	0x4A16 C004	0x4A21 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A16 A018	0x4A16 C018	0x4A21 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A16 A01C	0x4A16 C01C	0x4A21 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A16 A020	0x4A16 C020	0x4A21 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A16 A024	0x4A16 C024	0x4A21 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A16 A028	0x4A16 C028	0x4A21 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A16 A02C	0x4A16 C02C	0x4A21 902C

Table 14-462. PER1_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	UART3_TARG L3_MAIN Physical Address	TIMER2_TARG L3_MAIN Physical Address	TIMER3_TARG L3_MAIN Physical Address	TIMER4_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4802 1000	0x4803 3000	0x4803 5000	0x4803 7000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4802 1004	0x4803 3004	0x4803 5004	0x4803 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4802 1018	0x4803 3018	0x4803 5018	0x4803 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4802 101C	0x4803 301C	0x4803 501C	0x4803 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4802 1020	0x4803 3020	0x4803 5020	0x4803 7020

Table 14-462. PER1_TA Register Mapping Summary 1 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART3_TARG L3_MAIN Physical Address	TIMER2_TAR G L3_MAIN Physical Address	TIMER3_TAR G L3_MAIN Physical Address	TIMER4_TAR G L3_MAIN Physical Address
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4802 1024	0x4803 3024	0x4803 5024	0x4803 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4802 1028	0x4803 3028	0x4803 5028	0x4803 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4802 102C	0x4803 302C	0x4803 502C	0x4803 702C

Table 14-463. PER1_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	TIMER9_TAR G L3_MAIN Physical Address	GPIO7_TAR G L3_MAIN Physical Address	GPIO8_TAR G L3_MAIN Physical Address	GPIO2_TAR G L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4803 F000	0x4805 2000	0x4805 4000	0x4805 6000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4803 F004	0x4805 2004	0x4805 4004	0x4805 6004
L4_TA_CORE_L	R	32	0x0000 0018	0x4803 F018	0x4805 2018	0x4805 4018	0x4805 6018
L4_TA_CORE_H	R	32	0x0000 001C	0x4803 F01C	0x4805 201C	0x4805 401C	0x4805 601C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4803 F020	0x4805 2020	0x4805 4020	0x4805 6020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4803 F024	0x4805 2024	0x4805 4024	0x4805 6024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4803 F028	0x4805 2028	0x4805 4028	0x4805 6028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4803 F02C	0x4805 202C	0x4805 402C	0x4805 602C

Table 14-464. PER1_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	GPIO3_TAR G L3_MAIN Physical Address	GPIO4_TAR G L3_MAIN Physical Address	GPIO5_TAR G L3_MAIN Physical Address	GPIO6_TAR G L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4805 8000	0x4805 A000	0x4805 C000	0x4805 E000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4805 8004	0x4805 A004	0x4805 C004	0x4805 E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4805 8018	0x4805 A018	0x4805 C018	0x4805 E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4805 801C	0x4805 A01C	0x4805 C01C	0x4805 E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4805 8020	0x4805 A020	0x4805 C020	0x4805 E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4805 8024	0x4805 A024	0x4805 C024	0x4805 E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4805 8028	0x4805 A028	0x4805 C028	0x4805 E028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4805 802C	0x4805 A02C	0x4805 C02C	0x4805 E02C

Table 14-465. PER1_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	I2C3_TARG L3_MAIN Physical Address	UART5_TA RG L3_MAIN Physical Address	UART6_TA RG L3_MAIN Physical Address	UART1_TA RG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4806 1000	0x4806 7000	0x4806 9000	0x4806 B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4806 1004	0x4806 7004	0x4806 9004	0x4806 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4806 1018	0x4806 7018	0x4806 9018	0x4806 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4806 101C	0x4806 701C	0x4806 901C	0x4806 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4806 1020	0x4806 7020	0x4806 9020	0x4806 B020

Table 14-465. PER1_TA Register Mapping Summary 4 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	I2C3_TARG L3_MAIN Physical Address	UART5_TARG L3_MAIN Physical Address	UART6_TARG L3_MAIN Physical Address	UART1_TARG L3_MAIN Physical Address
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4806 1024	0x4806 7024	0x4806 9024	0x4806 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4806 1028	0x4806 7028	0x4806 9028	0x4806 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4806 102C	0x4806 702C	0x4806 902C	0x4806 B02C

Table 14-466. PER1_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	UART2_TARG L3_MAIN Physical Address	UART4_TARG L3_MAIN Physical Address	I2C1_TARG L3_MAIN Physical Address	I2C2_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4806 D000	0x4806 F000	0x4807 1000	0x4807 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4806 D004	0x4806 F004	0x4807 1004	0x4807 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4806 D018	0x4806 F018	0x4807 1018	0x4807 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4806 D01C	0x4806 F01C	0x4807 101C	0x4807 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4806 D020	0x4806 F020	0x4807 1020	0x4807 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4806 D024	0x4806 F024	0x4807 1024	0x4807 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4806 D028	0x4806 F028	0x4807 1028	0x4807 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4806 D02C	0x4806 F02C	0x4807 102C	0x4807 302C

Table 14-467. PER1_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	ELM_TARG L3_MAIN Physical Address	I2C4_TARG L3_MAIN Physical Address	I2C5_TARG L3_MAIN Physical Address	TIMER10_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4807 9000	0x4807 B000	0x4807 D000	0x4808 7000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4807 9004	0x4807 B004	0x4807 D004	0x4808 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4807 9018	0x4807 B018	0x4807 D018	0x4808 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4807 901C	0x4807 B01C	0x4807 D01C	0x4808 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4807 9020	0x4807 B020	0x4807 D020	0x4808 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4807 9024	0x4807 B024	0x4807 D024	0x4808 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4807 9028	0x4807 B028	0x4807 D028	0x4808 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4807 902C	0x4807 B02C	0x4807 D02C	0x4808 702C

Table 14-468. PER1_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	TIMER11_TARG L3_MAIN Physical Address	MCSPI1_TARG L3_MAIN Physical Address	MCSPI2_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4808 9000	0x4809 9000	0x4809 B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4808 9004	0x4809 9004	0x4809 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4808 9018	0x4809 9018	0x4809 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4808 901C	0x4809 901C	0x4809 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4808 9020	0x4809 9020	0x4809 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4808 9024	0x4809 9024	0x4809 B024

Table 14-468. PER1_TA Register Mapping Summary 7 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TIMER11_TARG L3_MAIN Physical Address	MCSPI1_TARG L3_MAIN Physical Address	MCSPI2_TARG L3_MAIN Physical Address
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4808 9028	0x4809 9028	0x4809 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4808 902C	0x4809 902C	0x4809 B02C

Table 14-469. PER1_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	MCSPI3_TARG L3_MAIN Physical Address	HDQ1W_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x480B 9000	0x480B 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x480B 9004	0x480B 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B 9018	0x480B 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B 901C	0x480B 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B 9020	0x480B 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B 9024	0x480B 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B 9028	0x480B 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B 902C	0x480B 302C

Table 14-470. PER1_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	MCSPI4_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x480B B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x480B B004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B B018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B B02C

Table 14-471. PER1_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	MMC1_TARG L3_MAIN Physical Address	MMC2_TARG L3_MAIN Physical Address	MMC3_TARG L3_MAIN Physical Address	MMC4_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4809 D000	0x480B 5000	0x480A E000	0x480D 2000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4809 D004	0x480B 5004	0x480A E004	0x480D 2004
L4_TA_CORE_L	R	32	0x0000 0018	0x4809 D018	0x480B 5018	0x480A E018	0x480D 2018
L4_TA_CORE_H	R	32	0x0000 001C	0x4809 D01C	0x480B 501C	0x480A E01C	0x480D 201C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4809 D020	0x480B 5020	0x480A E020	0x480D 2020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4809 D024	0x480B 5024	0x480A E024	0x480D 2024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4809 D028	0x480B 5028	0x480A E028	0x480D 2028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4809 D02C	0x480B 502C	0x480A E02C	0x480D 202C

Table 14-472. PER2_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	UART7_TARG L3_MAIN Physical Address	UART8_TARG L3_MAIN Physical Address	UART9_TARG L3_MAIN Physical Address	MLB_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4842 1000	0x4842 3000	0x4842 5000	0x4842 D000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4842 1004	0x4842 3004	0x4842 5004	0x4842 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4842 1018	0x4842 3018	0x4842 5018	0x4842 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4842 101C	0x4842 301C	0x4842 501C	0x4842 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4842 1020	0x4842 3020	0x4842 5020	0x4842 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4842 1024	0x4842 3024	0x4842 5024	0x4842 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4842 1028	0x4842 3028	0x4842 5028	0x4842 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4842 102C	0x4842 302C	0x4842 502C	0x4842 D02C

Table 14-473. PER2_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	DCAN2_TARG L3_MAIN Physical Address	ATL_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4848 2000	0x4843 D000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4848 2004	0x4843 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4848 2018	0x4843 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4848 201C	0x4843 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4848 2020	0x4843 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4848 2024	0x4843 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4848 2028	0x4843 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4848 202C	0x4843 D02C

Table 14-474. PER2_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	GMAC_TARG L3_MAIN Physical Address	VCP1_CFG_TARG L3_MAIN Physical Address	VCP2_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4848 8000	0x4844 7000	0x4844 9000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4848 8004	0x4844 7004	0x4844 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4848 8018	0x4844 7018	0x4844 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4848 801C	0x4844 701C	0x4844 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4848 8020	0x4844 7020	0x4844 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4848 8024	0x4844 7024	0x4844 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4848 8028	0x4844 7028	0x4844 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4848 802C	0x4844 702C	0x4844 902C

Table 14-475. PER2_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	MCASP4_DAT_TARG L3_MAIN Physical Address	MCASP5_DAT_TARG L3_MAIN Physical Address	MCASP6_DAT_TARG L3_MAIN Physical Address	MCASP7_DAT_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4843 7000	0x4843 B000	0x4844 D000	0x4845 1000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4843 7004	0x4843 B004	0x4844 D004	0x4845 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4843 7018	0x4843 B018	0x4844 D018	0x4845 1018

Table 14-475. PER2_TA Register Mapping Summary 4 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MCASP4_DAT_TARG L3_MAIN Physical Address	MCASP5_DAT_TARG L3_MAIN Physical Address	MCASP6_DAT_TARG L3_MAIN Physical Address	MCASP7_DAT_TARG L3_MAIN Physical Address
L4_TA_CORE_H	R	32	0x0000 001C	0x4843 701C	0x4843 B01C	0x4844 D01C	0x4845 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4843 7020	0x4843 B020	0x4844 D020	0x4845 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4843 7024	0x4843 B024	0x4844 D024	0x4845 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4843 7028	0x4843 B028	0x4844 D028	0x4845 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4843 702C	0x4843 B02C	0x4844 D02C	0x4845 102C

Table 14-476. PER2_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	MCASP8_DAT_TARG L3_MAIN Physical Address	MCASP1_CFG_TARG L3_MAIN Physical Address	MCASP2_CFG_TARG L3_MAIN Physical Address	MCASP3_CFG_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4845 5000	0x4846 2000	0x4846 6000	0x4846 A000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4845 5004	0x4846 2004	0x4846 6004	0x4846 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4845 5018	0x4846 2018	0x4846 6018	0x4846 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4845 501C	0x4846 201C	0x4846 601C	0x4846 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4845 5020	0x4846 2020	0x4846 6020	0x4846 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4845 5024	0x4846 2024	0x4846 6024	0x4846 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4845 5028	0x4846 2028	0x4846 6028	0x4846 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4845 502C	0x4846 202C	0x4846 602C	0x4846 A02C

Table 14-477. PER2_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	MCASP4_CFG_TARG L3_MAIN Physical Address	MCASP5_CFG_TARG L3_MAIN Physical Address	MCASP6_CFG_TARG L3_MAIN Physical Address	MCASP7_CFG_TARG L3_MAIN Physical Adrress
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4846 E000	0x4847 2000	0x4847 6000	0x4847 A000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4846 E004	0x4847 2004	0x4847 6004	0x4847 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4846 E018	0x4847 2018	0x4847 6018	0x4847 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4846 E01C	0x4847 201C	0x4847 601C	0x4847 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4846 E020	0x4847 2020	0x4847 6020	0x4847 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4846 E024	0x4847 2024	0x4847 6024	0x4847 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4846 E028	0x4847 2028	0x4847 6028	0x4847 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4846 E02C	0x4847 202C	0x4847 602C	0x4847 A02C

Table 14-478. PER2_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	MCASP8_CFG_TARG L3_MAIN Physical Address	PWM1_TARG L3_MAIN Physical Address	PWM2_TARG L3_MAIN Physical Address	PWM3_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4848 8000	0x4843 F000	0x4844 1000	0x4844 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4848 8004	0x4843 F004	0x4844 1004	0x4844 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4848 8018	0x4843 F018	0x4844 1018	0x4844 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4848 801C	0x4843 F01C	0x4844 101C	0x4844 301C

Table 14-478. PER2_TA Register Mapping Summary 7 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MCASP8_CFG_TARG L3_MAIN Physical Address	PWM1_TARG L3_MAIN Physical Address	PWM2_TARG L3_MAIN Physical Address	PWM3_TARG L3_MAIN Physical Address
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4848 8020	0x4843 F020	0x4844 1020	0x4844 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4848 8024	0x4843 F024	0x4844 1024	0x4844 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4848 8028	0x4843 F028	0x4844 1028	0x4844 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4848 802C	0x4843 F02C	0x4844 102C	0x4844 302C

Table 14-479. PER3_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)3_TAs)	Address Offset	MBX13_TARG L3_MAIN Physical Address	OCMC_RAM1_TARG L3_MAIN Physical Address	OCMC_RAM2_TARG L3_MAIN Physical Address	OCMC_RAM3_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4880 3000	0x4880 5000	0x4880 B000	0x4881 1000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4880 3004	0x4880 5004	0x4880 B004	0x4881 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4880 3018	0x4880 5018	0x4880 B018	0x4881 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4880 301C	0x4880 501C	0x4880 B01C	0x4881 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4880 3020	0x4880 5020	0x4880 B020	0x4881 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4880 3024	0x4880 5024	0x4880 B024	0x4881 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4880 3028	0x4880 5028	0x4880 B028	0x4881 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4880 302C	0x4880 502C	0x4880 B02C	0x4881 302C

Table 14-480. PER3_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	MMU1_TARG L3_MAIN Physical Address	MMU2_TARG L3_MAIN Physical Address	TIMER5_TARG L3_MAIN Physical Address	TIMER6_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4881 D000	0x4881 F000	0x4882 1000	0x4882 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4881 D004	0x4881 F004	0x4882 1004	0x4882 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4881 D018	0x4881 F018	0x4882 1018	0x4882 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4881 D01C	0x4881 F01C	0x4882 101C	0x4882 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4881 D020	0x4881 F020	0x4882 1020	0x4882 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4881 D024	0x4881 F024	0x4882 1024	0x4882 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4881 D028	0x4881 F028	0x4882 1028	0x4882 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4881 D02C	0x4881 F02C	0x4882 102C	0x4882 302C

Table 14-481. PER3_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	TIMER7_TARG L3_MAIN Physical Address	TIMER8_TARG L3_MAIN Physical Address	TIMER13_TARG L3_MAIN Physical Address	TIMER14_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4882 5000	0x4882 7000	0x4882 9000	0x4882 B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4882 5004	0x4882 7004	0x4882 9004	0x4882 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4882 5018	0x4882 7018	0x4882 9018	0x4882 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4882 501C	0x4882 701C	0x4882 901C	0x4882 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4882 5020	0x4882 7020	0x4882 9020	0x4882 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4882 5024	0x4882 7024	0x4882 9024	0x4882 B024

Table 14-481. PER3_TA Register Mapping Summary 3 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TIMER7_TARG L3_MAIN Physical Address	TIMER8_TARG L3_MAIN Physical Address	TIMER13_TARG L3_MAIN Physical Address	TIMER14_TARG L3_MAIN Physical Address
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4882 5028	0x4882 7028	0x4882 9028	0x4882 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4882 502C	0x4882 702C	0x4882 902C	0x4882 B02C

Table 14-482. PER3_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	TIMER15_TARG L3_MAIN Physical Address	TIMER16_TARG L3_MAIN Physical Address	MBX2_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4882 D000	0x4882 F000	0x4883 B000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4882 D004	0x4882 F004	0x4883 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4882 D018	0x4882 F018	0x4883 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4882 D01C	0x4882 F01C	0x4883 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4882 D020	0x4882 F020	0x4883 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4882 D024	0x4882 F024	0x4883 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4882 D028	0x4882 F028	0x4883 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4882 D02C	0x4882 F02C	0x4883 B02C

Table 14-483. PER3_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	MBX3_TARG L3_MAIN Physical Address	MBX4_TARG L3_MAIN Physical Address	MBX5_TARG L3_MAIN Physical Address	MBX6_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4883 D000	0x4883 F000	0x4884 1000	0x4884 3000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4883 D004	0x4883 F004	0x4884 1004	0x4884 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4883 D018	0x4883 F018	0x4884 1018	0x4884 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4883 D01C	0x4883 F01C	0x4884 101C	0x4884 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4883 D020	0x4883 F020	0x4884 1020	0x4884 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4883 D024	0x4883 F024	0x4884 1024	0x4884 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4883 D028	0x4883 F028	0x4884 1028	0x4884 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4883 D02C	0x4883 F02C	0x4884 102C	0x4884 302C

Table 14-484. PER3_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	MBX7_TARG L3_MAIN Physical Address	MBX8_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4884 5000	0x4884 7000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4884 5004	0x4884 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4884 5018	0x4884 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4884 501C	0x4884 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4884 5020	0x4884 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4884 5024	0x4884 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4884 5028	0x4884 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4884 502C	0x4884 702C

Table 14-485. PER3_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	MBX9_TARG L3_MAIN Physical Address	MBX10_TARG L3_MAIN Physical Address	MBX11_TARG L3_MAIN Physical Address	MBX12_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4885 F000	0x4886 1000	0x4886 3000	0x4886 5000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4885 F004	0x4886 1004	0x4886 3004	0x4886 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4885 F018	0x4886 1018	0x4886 3018	0x4886 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4885 F01C	0x4886 101C	0x4886 301C	0x4886 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4885 F020	0x4886 1020	0x4886 3020	0x4886 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4885 F024	0x4886 1024	0x4886 3024	0x4886 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4885 F028	0x4886 1028	0x4886 3028	0x4886 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4885 F02C	0x4886 102C	0x4886 302C	0x4886 502C

Table 14-486. PER3_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	VIP1_TARG L3_MAIN Physical Address	VIP2_TARG L3_MAIN Physical Address	VIP3_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4898 0000	0x489A 0000	0x489C 0000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4898 0004	0x489A 0004	0x489C 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x4898 0018	0x489A 0018	0x489C 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4898 001C	0x489A 001C	0x489C 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4898 0020	0x489A 0020	0x489C 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4898 0024	0x489A 0024	0x489C 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4898 0028	0x489A 0028	0x489C 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4898 002C	0x489A 002C	0x489C 002C

Table 14-487. PER3_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	VPE_TARG L3_MAIN Physical Address	RTC_TARG L3_MAIN Physical Address	USB4_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x489E 0000	0x4883 9000	0x4896 0000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x489E 0004	0x4883 9004	0x4896 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x489E 0018	0x4883 9018	0x4896 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x489E 001C	0x4883 901C	0x4896 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x489E 0020	0x4883 9020	0x4896 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x489E 0024	0x4883 9024	0x4896 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x489E 0028	0x4883 9028	0x4896 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x489E 002C	0x4883 902C	0x4896 002C

Table 14-488. PER3_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	USB2_TARG L3_MAIN Physical Address	USB1_TARG L3_MAIN Physical Address	USB3_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x488E 0000	0x488A 0000	0x4892 0000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x488E 0004	0x488A 0004	0x4892 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x488E 0018	0x488A 0018	0x4892 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x488E 001C	0x488A 001C	0x4892 001C

Table 14-488. PER3_TA Register Mapping Summary 10 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	USB2_TARG L3_MAIN Physical Address	USB1_TARG L3_MAIN Physical Address	USB3_TARG L3_MAIN Physical Address
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x488E 0020	0x488A 0020	0x4892 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x488E 0024	0x488A 0024	0x4892 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x488E 0028	0x488A 0028	0x4892 0028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x488E 002C	0x488A 002C	0x4892 002C

Table 14-489. WKUP_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	COUNTER_32K_TARG L3_MAIN Physical Address	PRM_TARG L3_MAIN Physical Address	CTRL_MODULE_WKUP_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4AE0 5000	0x4AE0 8000	0x4AE0 D000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4AE0 5004	0x4AE0 8004	0x4AE0 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE0 5018	0x4AE0 8018	0x4AE0 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE0 501C	0x4AE0 801C	0x4AE0 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE0 5020	0x4AE0 8020	0x4AE0 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE0 5024	0x4AE0 8024	0x4AE0 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE0 5028	0x4AE0 8028	0x4AE0 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE0 502C	0x4AE0 802C	0x4AE0 D02C

Table 14-490. WKUP_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	GPIO1_TARG L3_MAIN Physical Address	WD_TIMER2_TARG L3_MAIN Physical Address	TIMER1_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4AE1 1000	0x4AE1 5000	0x4AE1 9000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4AE1 1004	0x4AE1 5004	0x4AE1 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE1 1018	0x4AE1 5018	0x4AE1 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE1 101C	0x4AE1 501C	0x4AE1 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE1 1020	0x4AE1 5020	0x4AE1 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE1 1024	0x4AE1 5024	0x4AE1 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE1 1028	0x4AE1 5028	0x4AE1 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE1 102C	0x4AE1 502C	0x4AE1 902C

Table 14-491. WKUP_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	KBD_TARG L3_MAIN Physical Address	TIMER12_TARG L3_MAIN Physical Address	UART10_TARG L3_MAIN Physical Address	DCAN1_TARG L3_MAIN Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4AE1 D000	0x4AE2 1000	0x4AE2 C000	0x4AE3 E000
L4_TA_COMPONENT_H	R	32	0x0000 0004	0x4AE1 D004	0x4AE2 1004	0x4AE2 C004	0x4AE3 E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE1 D018	0x4AE2 1018	0x4AE2 C018	0x4AE3 E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE1 D01C	0x4AE2 101C	0x4AE2 C01C	0x4AE3 E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE1 D020	0x4AE2 1020	0x4AE2 C020	0x4AE3 E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE1 D024	0x4AE2 1024	0x4AE2 C024	0x4AE3 E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE1 D028	0x4AE2 1028	0x4AE2 C028	0x4AE3 E028

Table 14-491. WKUP_TA Register Mapping Summary 3 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	KBD_TARG L3_MAIN Physical Address	TIMER12_TARG L3_MAIN Physical Address	UART10_TARG L3_MAIN Physical Address	DCAN1_TARG L3_MAIN Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE1 D02C	0x4AE2 102C	0x4AE2 C02C	0x4AE3 E02C

14.3.5.3.2 L4 Target Agent (L4 TA) Register Description

Table 14-492 through Table 14-506 describe the L4 TA registers.

Table 14-492. L4_TA_COMPONENT_H

Address Offset	0x0000 0004		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Contains a component code and revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 14-493. Register Call Summary for Register L4_TA_COMPONENT_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

Table 14-494. L4_TA_COMPONENT_L

Address Offset	0x0000 0000		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Contains a component code and revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

(1) TI Internal Data

Table 14-495. Register Call Summary for Register L4_TA_COMPONENT_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

Table 14-496. L4_TA_CORE_L

Address Offset	0x0000 0018		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Contains a component code and revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																REV_CODE															

Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See (1).

(1) TI Internal Data

Table 14-497. Register Call Summary for Register L4_TA_CORE_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

Table 14-498. L4_TA_CORE_H

Address Offset	0x0000 001C		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Contains a component code and revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 14-499. Register Call Summary for Register L4_TA_CORE_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

Table 14-500. L4_TA_AGENT_CONTROL_L

Address Offset	0x0000 0020		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Enable error reporting		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SERROR_REP	RESERVED													REQ_TIMEOUT			RESERVED							OCP_RESET

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	SERROR_REP	Enable logging of error	R	0x0
23:11	RESERVED	Read returns 0.	R	0x0
10:8	REQ_TIMEOUT	Time-out Bound. Values are: 0 - No time-out 1 - 1x base cycles. 2 - 4x base cycles. 3 - 16x base cycles. 4 - 64x base cycles.	RW	0x0
7:1	RESERVED	Read returns 0.	R	0x00
0	OCP_RESET	The OCP_RESET field controls the OCP reset signal to the attached core. Setting this bit clears any pending transfers and resets the OCP interface. The bit must be cleared to deassert the OCP reset signal. When the software reset feature is available on a target agent, the target agent OCP must also have a reset signal directed to the target core.	RW	0

Table 14-501. Register Call Summary for Register L4_TA_AGENT_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2] [3] [4]
- Error Recovery: [5] [6]
- Operational Modes Configuration: [7] [8] [9] [10]
- L4 Target Agent (L4 TA) Register Summary: [11] [12] [13] [14] [15] [17] [18] [19] [20] [21] [22] [23] [24] [26] [27] [28] [29] [30] [31] [32] [33] [34] [36] [37] [38] [40] [42] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [62]

Table 14-502. L4_TA_AGENT_CONTROL_H

Address Offset	0x0000 0024		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Enable clock power management		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						AUTO_WAKEUP_RESP_CODE	EXT_CLOCK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Read returns 0.	R	0x000000
9	AUTO_WAKEUP_RESP_CODE		R	0
8	EXT_CLOCK	When set to 1, the ext_clk_off_i signal on a target agent indicates when the target agent should shut off.	R	0
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-503. Register Call Summary for Register L4_TA_AGENT_CONTROL_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

Table 14-504. L4_TA_AGENT_STATUS_L

Address Offset	0x0000 0028		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Error reporting		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SERROR	RESERVED															REQ_TIMEOUT	RESERVED							0CP_RESET

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	SERROR	Value of OCP SError signal	R	0
23:9	RESERVED	Read returns 0.	R	0x0000

Bits	Field Name	Description	Type	Reset
8	REQ_TIMEOUT	Time-out status: 0x0: No request time-out 0x1: A request time-out has occurred	R 1toCLR	0
7:1	RESERVED	Read returns 0.	R	0x00
0	OCP_RESET	L3 Reset	R	0

Table 14-505. Register Call Summary for Register L4_TA_AGENT_STATUS_L

L4 Interconnects
- Time-Out: [0] [1]
- Error Recovery: [2]
- Operational Modes Configuration: [3]
- L4 Target Agent (L4 TA) Register Summary: [4] [5] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [19] [20] [21] [22] [23] [24] [25] [26] [27] [29] [30] [31] [33] [35] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [55]

Table 14-506. L4_TA_AGENT_STATUS_H

Address Offset	0x0000 002C		
Physical Address	See Table 14-447 to Table 14-491	**Instance**	See Table 14-447 to Table 14-491
Description	Error reporting		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 14-507. Register Call Summary for Register L4_TA_AGENT_STATUS_H

L4 Interconnects
- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [9] [10] [11] [12] [13] [15] [16] [17] [18] [19] [20] [21] [22] [23] [25] [26] [27] [29] [31] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [51]

14.3.5.4 L4 Link Agent (L4 LA)

14.3.5.4.1 L4 Link Agent (L4 LA) Register Summary

Table 14-508 summarizes the L4 LA register mapping.

Table 14-508. LA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER1_LA L3_MAIN Physical Address	PER2_LA L3_MAIN Physical Address	PER3_LA L3_MAIN Physical Address
L4_LA_COMPONENT_L	R	32	0x0000 0000	0x4800 0800	0x4840 0800	0x4880 0800
L4_LA_COMPONENT_H	R	32	0x0000 0004	0x4800 0804	0x4840 0804	0x4880 0804
L4_LA_NETWORK_L	R	32	0x0000 0010	0x4800 0810	0x4840 0810	0x4880 0810
L4_LA_NETWORK_H	R	32	0x0000 0014	0x4800 0814	0x4840 0814	0x4880 0814
L4_LA_INITIATOR_INFO_L	R	32	0x0000 0018	0x4800 0818	0x4840 0818	0x4880 0818
L4_LA_INITIATOR_INFO_H	R	32	0x0000 001C	0x4800 081C	0x4840 081C	0x4880 081C

Table 14-508. LA Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER1_LA L3_MAIN Physical Address	PER2_LA L3_MAIN Physical Address	PER3_LA L3_MAIN Physical Address
L4_LA_NETWORK_CONTROL_L	RW	32	0x0000 0020	0x4800 0820	0x4840 0820	0x4880 0820
L4_LA_NETWORK_CONTROL_H	RW	32	0x0000 0024	0x4800 0824	0x4840 0824	0x4880 0824
L4_LA_FLAG_MASK_j_L[(1)]	RW	32	0x0000 0100 + (0x20*j)	0x4800 0900 + (0x20*j)	0x4840 0900 + (0x20*j)	0x4880 0900 + (0x20*j)
L4_LA_FLAG_MASK_j_H[(1)]	RW	32	0x0000 0104 + (0x20*j)	0x4800 0904 + (0x20*j)	0x4840 0904 + (0x20*j)	0x4880 0904 + (0x20*j)
L4_LA_FLAG_STATUS_j_L[(1)]	R	32	0x0000 0110 + (0x20*j)	0x4800 0910 + (0x20*j)	0x4840 0910 + (0x20*j)	0x4880 0910 + (0x20*j)
L4_LA_FLAG_STATUS_j_H[(1)]	R	32	0x0000 0114 + (0x20*j)	0x4800 0914 + (0x20*j)	0x4840 0914 + (0x20*j)	0x4880 0914 + (0x20*j)

(1) j = 0 to 1 for PER1_LA
j = 0 to 1 for PER2_LA
j = 0 to 1 for PER3_LA

Table 14-509. LA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CFG_LA L3_MAIN Physical Address	WKUP_LA L3_MAIN Physical Address
L4_LA_COMPONENT_L	R	32	0x0000 0000	0x4A00 0800	0x4AE0 0800
L4_LA_COMPONENT_H	R	32	0x0000 0004	0x4A00 0804	0x4AE0 0804
L4_LA_NETWORK_L	R	32	0x0000 0010	0x4A00 0810	0x4AE0 0810
L4_LA_NETWORK_H	R	32	0x0000 0014	0x4A00 0814	0x4AE0 0814
L4_LA_INITIATOR_INFO_L	R	32	0x0000 0018	0x4A00 0818	0x4AE0 0818
L4_LA_INITIATOR_INFO_H	R	32	0x0000 001C	0x4A00 081C	0x4AE0 081C
L4_LA_NETWORK_CONTROL_L	RW	32	0x0000 0020	0x4A00 0820	0x4AE0 0820
L4_LA_NETWORK_CONTROL_H	RW	32	0x0000 0024	0x4A00 0824	0x4AE0 0824

14.3.5.4.2 L4 Link Agent (L4 LA) Register Description

Table 14-510 through Table 14-535 describe the L4 LA registers.

Table 14-510. L4_LA_COMPONENT_L

Address Offset	0x0000 0000		
Physical Address	0x4800 0800 0x4840 0800 0x4880 0800 0x4A00 0800 0x4AE0 0800	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Contain a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

(1) TI Internal Data

Table 14-511. Register Call Summary for Register L4_LA_COMPONENT_L

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-512. L4_LA_COMPONENT_H

Address Offset	0x0000 0004		
Physical Address	0x4800 0804 0x4840 0804 0x4880 0804 0x4A00 0804 0x4AE0 0804	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Contain a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-513. Register Call Summary for Register L4_LA_COMPONENT_H

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-514. L4_LA_NETWORK_L

Address Offset	0x0000 0010		
Physical Address	0x4800 0810 0x4840 0810 0x4880 0810 0x4A00 0810 0x4AE0 0810	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Identify the interconnect		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-515. Register Call Summary for Register L4_LA_NETWORK_L

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-516. L4_LA_NETWORK_H

Address Offset	0x0000 0014		
Physical Address	0x4800 0814 0x4840 0814 0x4880 0814 0x4A00 0814 0x4AE0 0814	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Identify the interconnect		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															

Bits	Field Name	Description	Type	Reset
31:0	ID	The ID field uniquely identifies this interconnect.	R	0x00000000

Table 14-517. Register Call Summary for Register L4_LA_NETWORK_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-518. L4_LA_INITIATOR_INFO_L

Address Offset	0x0000 0018		
Physical Address	0x4800 0818 0x4840 0818 0x4880 0818 0x4A00 0818 0x4AE0 0818	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Contain initiator subsystem information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PROT_GROUPS				NUMBER_REGIONS								RESERVED												SEGMENTS			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:24	PROT_GROUPS	Number of protection group of in the current L4 0x0: No protection group 0x1: 1 protection group 0x2: 2 protection groups .... 0x8: 8 protection groups 0x9 to 0xF: Reserved	R	see Table 14-520
23:16	NUMBER_REGIONS	Number of regions in the current L4 0x0: Reserved 0x1: 1 region 0x2: 2 regions .... Max regions +1 to 0xFF: Reserved, maximum regions is listed in Table 14-520	R	see Table 14-520
15:4	RESERVED	Read returns 0.	R	0x000

Bits	Field Name	Description	Type	Reset
3:0	SEGMENTS	Number of segments in the current L4 0x0: Reserved 0x1: 1 segment 0x2: 2 segments .... 0x8: 8 segments	R	see Table 14-520

Table 14-519. Register Call Summary for Register L4_LA_INITIATOR_INFO_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-520. Reset value for L4_LA_INITIATOR_INFO_L

Field Name	L4 PER1	L4 PER2	L4 PER3	L4 CFG	L4 WKUP
PROT_GROUPS	0x8	0x8	0x8	0x8	0x8
NUMBER_REGIONS	0x55	0x3F	0x61	0x81	0x2C
SEGMENTS	0x2	0x1	0x1	0x3	0x4

Table 14-521. L4_LA_INITIATOR_INFO_H

Address Offset	0x0000 001C		
Physical Address	0x4800 081C 0x4840 081C 0x4880 081C 0x4A00 081C 0x4AE0 081C	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Contain initiator subsystem information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													THREADS			RESERVED		CONNID_WIDTH		RESERVED		BYTE_DATA_WIDTH_EXP		RESERVED				ADDR_WIDTH			

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Read returns 0.	R	0x0000
18:16	THREADS	The THREADS field specifies the number of initiator threads connected to the interconnect. The field contains read-only configuration information for the initiator subsystem.	R	see Table 14-523
15	RESERVED	Read returns 0.	R	0
14:12	CONNID_WIDTH	The initiator subsystem ConnID width. The CONNID_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 14-523
11	RESERVED	Read returns 0.	R	0

Bits	Field Name	Description	Type	Reset
10:8	BYTE_DATA_WIDTH_EXP	This field specifies the initiator subsystem data width.The BYTE_DATA_WIDTH_EXP field contains read-only configuration information for the initiator subsystem. 0x1: 16-bit data width is specified 0x2: 32-bit data width is specified	R	see Table 14-523
7:6	RESERVED	Read returns 0.	R	0x0
5:0	ADDR_WIDTH	This field specifies the initiator subsystem address width. The ADDR_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 14-523

Table 14-522. Register Call Summary for Register L4_LA_INITIATOR_INFO_H

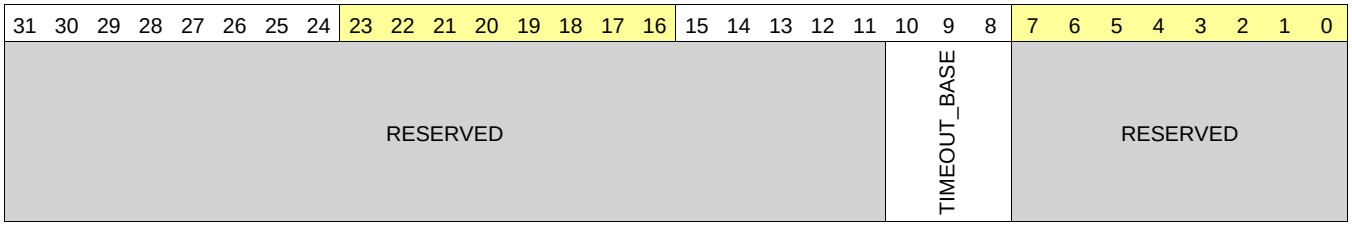
L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-523. Reset value for L4_LA_INITIATOR_INFO_H

Field Name	L4 PER1	L4 PER2	L4 PER3	L4 CFG	L4 WKUP
THREADS	0x4	0x3	0x3	0x1	0x1
CONNID_WIDTH	0x4	0x4	0x5	0x4	0x4
BYTE_DATA_WIDTH_EXP	0x2	0x2	0x2	0x2	0x2
ADDR_WIDTH	0x18	0x18	0x18	0x18	0x15

Table 14-524. L4_LA_NETWORK_CONTROL_L

Address Offset	0x0000 0020		
Physical Address	0x4800 0820 0x4840 0820 0x4880 0820 0x4A00 0820 0x4AE0 0820	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Control interconnect minimum timeout values.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Read returns 0.	R	0x000000
10:8	TIMEOUT_BASE	The TIMEOUT_BASE field indicates the time-out period (that is, base cycles) for the highest frequency time-base signal sent from the L4 initiator subsystem to all target agents that have time-out enabled. Values for the field are: 0 - Time-out disabled 1 - L4 interconnect clock cycles divided by 64 2 - L4 interconnect clock cycles divided by 256 3 - L4 interconnect clock cycles divided by 1024 4 - L4 interconnect clock cycles divided by 4096	RW	0x4
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-525. Register Call Summary for Register L4_LA_NETWORK_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2]
- Operational Modes Configuration: [3] [4]
- L4 Link Agent (L4 LA) Register Summary: [5] [6]

Table 14-526. L4_LA_NETWORK_CONTROL_H

Address Offset	0x0000 0024		
Physical Address	0x4800 0824 0x4840 0824 0x4880 0824 0x4A00 0824 0x4AE0 0824	**Instance**	PER1_LA PER2_LA PER3_LA CFG_LA WKUP_LA
Description	Control interconnect global power control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLOCK_GATE_DISABLE	RESERVED			THREAD0_PRI	RESERVED											EXT_CLOCK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	CLOCK_GATE_DISABLE	When set to 1 this field disables all clock gating.	RW	0
23:21	RESERVED	Read returns 0.	R	0x0
20	THREAD0_PRI	Sets thread priority. If the field is set to 0, the default, all initiator threads are treated the same. Setting the THREAD0_PRI field to 1 assigns a higher arbitration priority to thread 0 of the first initiator OCP interface. To avoid starvation, arbitration is imposed by the initiator subsystem. When multiple requests from different initiator threads are dispatched to targets simultaneously, the oldest request is dispatched first. If thread 0 is assigned a higher priority, a request on thread 0 always wins arbitration. Assigning thread 0 of the first initiator OCP the highest priority on a request or response can result in the starvation of other threads.	R	1
19:9	RESERVED	Read returns 0.	R	0x000
8	EXT_CLOCK	Global external clock control. When set to 1, the ext_clk_off_i signal on the initiator subsystem instructs the entire L4 to shut off.	R	1
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-527. Register Call Summary for Register L4_LA_NETWORK_CONTROL_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0] [1]

Table 14-528. L4_LA_FLAG_MASK_j_L

Address Offset	0x0000 0100 + (0x20*j)		
Physical Address	0x4800 0900 + (0x20*j) 0x4840 0900 + (0x20*j) 0x4880 0900 + (0x20*j)	**Instance**	PER1_LA PER2_LA PER3_LA
Description	Mask of composite sideband flag(0)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MASK			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Read returns 0	R	0x0000 0000
3:0	MASK	Number of input sideband signals	RW	0xF

Table 14-529. Register Call Summary for Register L4_LA_FLAG_MASK_j_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-530. Reset Value for L4_LA_FLAG_MASK_j_L

Initiator	Bit Field (MASK)	Reset
L4_PER1	[3:0]	0xF
L4_PER2	[2:0]	0x7
L4_PER3	[2:0]	0x7

Table 14-531. L4_LA_FLAG_MASK_j_H

Address Offset	0x0000 0104 + (0x20*j)		
Physical Address	0x4800 0904 + (0x20*j) 0x4840 0904 + (0x20*j) 0x4880 0904 + (0x20*j)	**Instance**	PER1_LA PER2_LA PER3_LA
Description	Status of composite sideband flag(0)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-532. Register Call Summary for Register L4_LA_FLAG_MASK_j_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-533. L4_LA_FLAG_STATUS_j_L

Address Offset	0x0000 0110 + (0x20*j)		
Physical Address	0x4800 0910 + (0x20*j) 0x4840 0910 + (0x20*j) 0x4880 0910 + (0x20*j)	**Instance**	PER1_LA PER2_LA PER3_LA

Table 14-533. L4_LA_FLAG_STATUS_j_L (continued)

Description	Mask of composite sideband flag(1)
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STATUS			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Read returns 0	R	0x0000 0000
3:0	STATUS	Status of input sideband signals	RW	0x0

Table 14-534. Register Call Summary for Register L4_LA_FLAG_STATUS_j_L

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-535. L4_LA_FLAG_STATUS_j_H

Address Offset	0x0000 0114 + (0x20*j)		
Physical Address	0x4800 0914 + (0x20*j) 0x4840 0914 + (0x20*j) 0x4880 0914 + (0x20*j)	**Instance**	PER1_LA PER2_LA PER3_LA
Description	Status of composite sideband flag(1)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x000 0000 0000 0000

Table 14-536. Register Call Summary for Register L4_LA_FLAG_STATUS_j_H

L4 Interconnects
- L4 Link Agent (L4 LA) Register Summary: [0]

14.3.5.5 L4 Address Protection (L4 AP)

14.3.5.5.1 L4 Address Protection (L4 AP) Register Summary

Table 14-537 and Table 14-538 summarizes the L4 AP register mapping.

Table 14-537. L4 AP Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER1_AP Physical Address	PER2_AP Physical Address	PER3_AP Physical Address
L4_AP_COMPONENT_L	R	32	0x0000 0000	0x4800 0 000	0x4840 0 000	0x4880 0 000
L4_AP_COMPONENT_H	R	32	0x0000 0004	0x4800 0004	0x4840 0004	0x4880 0004

Table 14-537. L4 AP Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER1_AP Physical Address	PER2_AP Physical Address	PER3_AP Physical Address
L4_AP_SEGMENT_i_L (1)	RW	32	0x0000 0100 + (0x08*i)	0x4800 0100 + (0x08*i)	0x4840 0100 + (0x08*i)	0x4880 0100 + (0x08*i)
L4_AP_SEGMENT_i_H (1)	RW	32	0x0000 0104 + (0x08*i)	0x4800 0104 + (0x08*i)	0x4840 0104 + (0x08*i)	0x4880 0104 + (0x08*i)
L4_AP_PROT_GROUP_MEMBERS_k_L (2)	R	32	0x0000 0200 + (0x08*k)	0x4800 0200 + (0x08*k)	0x4840 0200 + (0x08*k)	0x4880 0200 + (0x08*k)
L4_AP_PROT_GROUP_MEMBERS_k_H (2)	R	32	0x0000 0204 + (0x08*k)	0x4800 0204 + (0x08*k)	0x4840 0204 + (0x08*k)	0x4880 0204 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_L (2)	R	32	0x0000 0280 + (0x08*k)	0x4800 0280 + (0x08*k)	0x4840 0280 + (0x08*k)	0x4880 0280 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_H (2)	R	32	0x0000 0284 + (0x08*k)	0x4800 0284 + (0x08*k)	0x4840 0284 + (0x08*k)	0x4880 0284 + (0x08*k)
L4_AP_REGION_l_L (3)	RW	32	0x0000 0300 + (0x08*l)	0x4800 0300 + (0x08*l)	0x4840 0300 + (0x08*l)	0x4880 0300 + (0x08*l)
L4_AP_REGION_l_H (3)	RW	32	0x0000 0304 + (0x08*l)	0x4800 0304 + (0x08*l)	0x4840 0304 + (0x08*l)	0x4880 0304 + (0x08*l)

(1) i = 0 to 1 for PER1_AP
i = 0 for PER2_AP
i = 0 for PER3_AP
(2) k = 0 to 7 for PER1_AP
k = 0 to 7 for PER2_AP
k = 0 to 7 for PER3_AP
(3) l = 0 to 84 for PER1_AP
l = 0 to 62 for PER2_AP
l = 0 to 96 forPER3_AP

Table 14-538. L4 AP Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	CFG_AP Physical Address	WKUP_AP Physical Address
L4_AP_COMPONENT_L	R	32	0x0000 0000	0x4A00 0 000	0x4AE0 0 000
L4_AP_COMPONENT_H	R	32	0x0000 0004	0x4A00 0004	0x4AE0 0004
L4_AP_SEGMENT_i_L (1)	RW	32	0x0000 0100 + (0x08*i)	0x4A00 0100 + (0x08*i)	0x4AE0 0100 + (0x08*i)
L4_AP_SEGMENT_i_H (1)	RW	32	0x0000 0104 + (0x08*i)	0x4A00 0104 + (0x08*i)	0x4AE0 0104 + (0x08*i)
L4_AP_PROT_GROUP_MEMBERS_k_L (2)	R	32	0x0000 0200 + (0x08*k)	0x4A00 0200 + (0x08*k)	0x4AE0 0200 + (0x08*k)
L4_AP_PROT_GROUP_MEMBERS_k_H (2)	R	32	0x0000 0204 + (0x08*k)	0x4A00 0204 + (0x08*k)	0x4AE0 0204 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_L (2)	R	32	0x0000 0280 + (0x08*k)	0x4A00 0280 + (0x08*k)	0x4AE0 0280 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_H (2)	R	32	0x0000 0284 + (0x08*k)	0x4A00 0284 + (0x08*k)	0x4AE0 0284 + (0x08*k)
L4_AP_REGION_l_L (3)	RW	32	0x0000 0300 + (0x08*l)	0x4A00 0300 + (0x08*l)	0x4AE0 0300 + (0x08*l)
L4_AP_REGION_l_H (3)	RW	32	0x0000 0304 + (0x08*l)	0x4A00 0304 + (0x08*l)	0x4AE0 0304 + (0x08*l)

(1) i = 0 to 1 for PER1_AP
i = 0 for PER2_AP
i = 0 for PER3_AP
(2) k = 0 to 7 for PER1_AP
k = 0 to 7 for PER2_AP
k = 0 to 7 for PER3_AP
(3) l = 0 to 84 for PER1_AP
l = 0 to 62 for PER2_AP
l = 0 to 96 forPER3_AP

14.3.5.5.2 L4 Address Protection (L4 AP) Register Description

Table 14-539 through Table 14-564 describe the L4 AP registers.

Table 14-539. L4_AP_COMPONENT_L

Address Offset	0x000		
Physical Address	0x4800 0 000 0x4840 0 000 0x4880 0 000 0x4A00 0 000 0x4AE0 0 000	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Contains a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R(2)	See (1).

(1) TI Internal Data

(2) For L4_PER1 and L4_WKUP, when k = 2 to 7 the access type of CONNID_BIT_VECTOR is RW.
For L4_PER2, L4_PER3 and L4_CFG, when k = 1 to 7 the access type of CONNID_BIT_VECTOR is RW.

Table 14-540. Register Call Summary for Register L4_AP_COMPONENT_L

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0] [1]

Table 14-541. L4_AP_COMPONENT_H

Address Offset	0x004		
Physical Address	0x4800 0004 0x4840 0004 0x4880 0004 0x4A00 0004 0x4AE0 0004	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Contains a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-542. Register Call Summary for Register L4_AP_COMPONENT_H

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0] [1]

Table 14-543. L4_AP_SEGMENT_i_L

Address Offset	0x100 + (0x08*i)	**Index**	
Physical Address	0x4800 0100 + (0x08*i) 0x4840 0100 + (0x08*i) 0x4880 0100 + (0x08*i) 0x4A00 0100 + (0x08*i) 0x4AE0 0100 + (0x08*i)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define the base address of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																															

Bits	Field Name	Description	Type	Reset
31:0	BASE	The base address of the segment (with 0s from bit 0 to bit SIZE-1).	R	see Table 14-547

Table 14-544. Register Call Summary for Register L4_AP_SEGMENT_i_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1] [2]

Table 14-545. L4_AP_SEGMENT_i_H

Address Offset	0x104 + (0x08*i)	**Index**	
Physical Address	0x4800 0104 + (0x08*i) 0x4840 0104 + (0x08*i) 0x4880 0104 + (0x08*i) 0x4A00 0104 + (0x08*i) 0x4AE0 0104 + (0x08*i)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define the size of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														SIZE	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Read returns 0.	R	0x0000000
4:0	SIZE	Segment size is a power of 2, where 2^{SIZE} is the byte size of a segment (all segment registers use the same size).	R	see Table 14-547

Table 14-546. Register Call Summary for Register L4_AP_SEGMENT_i_H

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1] [2]

Table 14-547. Reset Value for L4_AP_SEGMENT_i

i	L4 PER1		L4 PER2		L4 PER3		L4 CFG		L4 WKUP	
	BASE	SIZE	BASE	SIZE	BASE	SIZE	BASE	SIZE	BASE	SIZE
0	0x0000 0000	0x15	0x0000 0000	0x16	0x0000 0000	0x15	0x0000 0000	0x14	0x0000 0000	0x10
1	0x0020 0000	0x15	-	-	-	-	0x0010 0000	0x14	0x0001 0000	0x10

Table 14-547. Reset Value for L4_AP_SEGMENT_i (continued)

i	L4 PER1		L4 PER2		L4 PER3		L4 CFG		L4 WKUP	
	BASE	SIZE	BASE	SIZE	BASE	SIZE	BASE	SIZE	BASE	SIZE
2	-	-	-	-	-	-	0x0020 0000	0x14	0x0002 0000	0x10
3	-	-	-	-	-	-	-	-	0x0003 0000	0x10

Table 14-548. L4_AP_PROT_GROUP_MEMBERS_k_L

Address Offset	0x200 + (0x08*k)	**Index**	
Physical Address	0x4800 0200 + (0x08*k) 0x4840 0200 + (0x08*k) 0x4880 0200 + (0x08*k) 0x4A00 0200 + (0x08*k) 0x4AE0 0200 + (0x08*k)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CONNID_BIT_VECTOR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x000000000000
15:0	CONNID_BIT_VECTOR	Specifies protection group members N is 2**W, where W is the connID width	R[(1)]	0xFFFF

(1) For L4_PER1 and L4_WKUP, when k = 2 to 7 the access type of CONNID_BIT_VECTOR is RW.
For L4_PER2, L4_PER3 and L4_CFG, when k = 1 to 7 the access type of CONNID_BIT_VECTOR is RW.

Table 14-549. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_L

L4 Interconnects

- Protection Group: [0] [1] [2] [3] [4] [5] [6]
- L4 Firewall Address and Protection Register Settings: [7]
- Operational Modes Configuration: [8]
- L4 Address Protection (L4 AP) Register Summary: [9] [10]

Table 14-550. L4_AP_PROT_GROUP_MEMBERS_k_H

Address Offset	0x204 + (0x08*k)	**Index**	
Physical Address	0x4800 0204 + (0x08*k) 0x4840 0204 + (0x08*k) 0x4880 0204 + (0x08*k) 0x4A00 0204 + (0x08*k) 0x4AE0 0204 + (0x08*k)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0's	R	0x0000 0000

Table 14-551. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_H

L4 Interconnects

- Protection Group: [0] [1] [2] [3] [4] [5] [6]
- L4 Address Protection (L4 AP) Register Summary: [7] [8]

Table 14-552. L4_AP_PROT_GROUP_ROLES_k_L

Address Offset	0x200 + (0x08*k)	**Index**	
Physical Address	0x4800 0280 + (0x08*k) 0x4840 0280 + (0x08*k) 0x4880 0280 + (0x08*k) 0x4A00 0280 + (0x08*k) 0x4AE0 0280 + (0x08*k)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define MReqInfo bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															

Bits	Field Name	Description	Type	Reset
31:0	ENABLE	Enabled bits N is 2**W, where W (W is less than or equal to 6) is the number of MReqInfo bits configured for role checking	R	0xFFFF

Table 14-553. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_L

L4 Interconnects

- Protection Group: [0] [1] [2] [3] [4] [5] [6] [7]
- L4 Firewall Address and Protection Register Settings: [8]
- Operational Modes Configuration: [9]
- L4 Address Protection (L4 AP) Register Summary: [10] [11]

Table 14-554. Reset Value for L4_AP_PROT_GROUP_ROLES_k

k	L4_PER		L4_CFG		L4_WKUP	
	Type	Reset Value	Type	Reset Value	Type	Reset value
0	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
1	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
2	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
3	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
4	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
5	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF
6	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF
7	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF

(1) Value exported from SCM and valid for GP device only (see *Chapter 18, Control Module*). The values of the other protection registers can be modified during run time.

Table 14-555. L4_AP_PROT_GROUP_ROLES_k_H

Address Offset	0x204 + (0x08*k)	**Index**	
Physical Address	0x4800 0284 + (0x08*k) 0x4840 0284 + (0x08*k) 0x4880 0284 + (0x08*k) 0x4A00 0284 + (0x08*k) 0x4AE0 0284 + (0x08*k)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															

Bits	Field Name	Description	Type	Reset
31:0	ENABLE	Enabled bits N is 2**W, where W (W is less than or equal to 6) is the number of MReqInfo bits configured for role checking	R	0xFFFF

Table 14-556. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_H

L4 Interconnects

- Protection Group: [0] [1] [2] [3] [4]
- L4 Firewall Address and Protection Register Settings: [5]
- L4 Address Protection (L4 AP) Register Summary: [6] [7]

Table 14-557. L4_AP_REGION_l_L

Address Offset	0x300 + (0x08*l)	**Index**	
Physical Address	0x4800 0300 + (0x08*l) 0x4840 0300 + (0x08*l) 0x4880 0300 + (0x08*l) 0x4A00 0300 + (0x08*l) 0x4AE0 0300 + (0x08*l)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define the base address of the region in respect to the segment it belongs to.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BASE																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Read returns 0.	R	0x00
20:0	BASE	Sets the base address of the region relative to its segment base.	R	See Table 14-561 to Table 14-565

Table 14-558. Register Call Summary for Register L4_AP_REGION_l_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- Operational Modes Configuration: [1]
- L4 Address Protection (L4 AP) Register Summary: [2] [3]

Table 14-559. L4_AP_REGION_I_H

Address Offset	0x304 + (0x08*I)	**Index**	
Physical Address	0x4800 0304 + (0x08*I) 0x4840 0304 + (0x08*I) 0x4880 0304 + (0x08*I) 0x4A00 0304 + (0x08*I) 0x4AE0 0304 + (0x08*I)	**Instance**	PER1_AP PER2_AP PER3_AP CFG_AP WKUP_AP
Description	Define the size, protection group and segment ID of the region		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MADDRSPACE				RESERVED	SEGMENT_ID			RESERVED	PROT_GROUP_ID			RESERVED	BYTE_DATA_WIDTH_EXP		RESERVED	PHY_TARGET_ID								RESERVED	SIZE						ENABLE

Bits	Field Name	Description	Type	Reset
31:28	MADDRSPACE	Target interconnect MAddrSpace	R	See Table 14-561 to Table 14-565
27	RESERVED	Read returns 0	R	0x0
26:24	SEGMENT_ID	Segment ID of the region	R	See Table 14-561 to Table 14-565
23	RESERVED	Read returns 0	R	0x0
22:20	PROT_GROUP_ID	Protection group ID	RW	See Table 14-561 to Table 14-565
19	RESERVED	Read returns 0	R	0x0
18:17	BYTE_DATA_WIDTH_EXP	Target data byte width	R	See Table 14-561 to Table 14-565
16:15	RESERVED	Read returns 0	R	0x0
14:8	PHY_TARGET_ID	Physical target ID	R	See Table 14-561 to Table 14-565
7	RESERVED	Read returns 0.	R	0x0
6:1	SIZE	Define the size of the region in bytes. 2^{SIZE} equals the region.	R	See Table 14-561 to Table 14-565
0	ENABLE	0x0: Disable the region, no access allows 0x1: Enable the region, with access as define in registers	R	0x1

Table 14-560. Register Call Summary for Register L4_AP_REGION_I_H

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1] [2]

Table 14-561. L4_AP_REGION_I Reset Value for L4 PER1

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x00 0000
1	0x1	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x00 0800
3	0x0	0x0	0x7	0x2	0x04	0x0C	0x1	0x02 0000

Table 14-561. L4_AP_REGION_l Reset Value for L4 PER1 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
4	0x0	0x0	0x7	0x2	0x05	0x0C	0x1	0x02 1000
5	0x0	0x0	0x7	0x2	0x3E	0x0C	0x1	0x03 2000
6	0x0	0x0	0x7	0x2	0x3F	0x0C	0x1	0x03 3000
7	0x0	0x0	0x7	0x2	0x46	0x0C	0x1	0x03 4000
8	0x0	0x0	0x7	0x2	0x47	0x0C	0x1	0x03 5000
9	0x0	0x0	0x7	0x2	0x4E	0x0C	0x1	0x03 6000
10	0x0	0x0	0x7	0x2	0x4F	0x0C	0x1	0x03 7000
11	0x0	0x0	0x7	0x2	0x56	0x0C	0x1	0x03 E000
12	0x0	0x0	0x7	0x2	0x57	0x0C	0x1	0x03 F000
13	0x0	0x0	0x7	0x2	0x0E	0x0C	0x1	0x05 5000
14	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x05 6000
15	0x0	0x0	0x7	0x2	0x06	0x0C	0x1	0x05 7000
16	0x0	0x0	0x7	0x2	0x07	0x0C	0x1	0x05 8000
17	0x0	0x0	0x7	0x2	0x16	0x0C	0x1	0x05 9000
18	0x0	0x0	0x7	0x2	0x17	0x0C	0x1	0x05 A000
19	0x0	0x0	0x7	0x2	0x1E	0x0C	0x1	0x05 B000
20	0x0	0x0	0x7	0x2	0x1F	0x0C	0x1	0x05 C000
21	0x0	0x0	0x7	0x2	0x26	0x0C	0x1	0x05 D000
22	0x0	0x0	0x7	0x2	0x27	0x0C	0x1	0x05 E000
23	0x0	0x0	0x7	0x2	0x32	0x0C	0x1	0x06 0000
24	0x0	0x0	0x7	0x2	0x24	0x0C	0x1	0x06 A000
25	0x0	0x0	0x7	0x2	0x25	0x0C	0x1	0x06 B000
26	0x0	0x0	0x7	0x2	0x2C	0x0C	0x1	0x06 C000
27	0x0	0x0	0x7	0x2	0x2D	0x0C	0x1	0x06 D000
28	0x1	0x0	0x7	0x2	0x0C	0x0C	0x1	0x06 E000
29	0x0	0x0	0x7	0x2	0x0D	0x0C	0x1	0x06 F000
30	0x0	0x0	0x7	0x2	0x22	0x0C	0x1	0x07 0000
31	0x0	0x0	0x7	0x2	0x23	0x0C	0x1	0x07 1000
32	0x0	0x0	0x7	0x2	0x2A	0x0C	0x1	0x07 2000
33	0x0	0x0	0x7	0x2	0x2B	0x0C	0x1	0x07 3000
34	0x0	0x0	0x7	0x2	0x33	0x0C	0x1	0x06 1000
35	0x0	0x0	0x7	0x2	0x36	0x0C	0x1	0x05 3000
36	0x0	0x0	0x7	0x2	0x37	0x0C	0x1	0x05 4000
37	0x0	0x0	0x7	0x2	0x52	0x0C	0x1	0x0B 2000
38	0x0	0x0	0x7	0x2	0x53	0x0C	0x1	0x0B 3000
39	0x0	0x0	0x7	0x2	0x0A	0x0C	0x1	0x07 8000
40	0x0	0x0	0x7	0x2	0x0B	0x0C	0x1	0x07 9000
41	0x0	0x0	0x7	0x2	0x5E	0x0C	0x1	0x08 6000
42	0x0	0x0	0x7	0x2	0x5F	0x0C	0x1	0x08 7000
43	0x0	0x0	0x7	0x2	0x66	0x0C	0x1	0x08 8000
44	0x0	0x0	0x7	0x2	0x67	0x0C	0x1	0x08 9000
45	0x0	0x0	0x7	0x2	0x2E	0x0C	0x1	0x05 1000
46	0x0	0x0	0x7	0x2	0x2F	0x0C	0x1	0x05 2000
47	0x0	0x0	0x7	0x2	0x08	0x0C	0x1	0x09 8000
48	0x0	0x0	0x7	0x2	0x09	0x0C	0x1	0x09 9000
49	0x0	0x0	0x7	0x2	0x10	0x0C	0x1	0x09 A000
50	0x0	0x0	0x7	0x2	0x11	0x0C	0x1	0x09 B000

Table 14-561. L4_AP_REGION_l Reset Value for L4 PER1 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
51	0x0	0x0	0x7	0x2	0x38	0x0C	0x1	0x09 C000
52	0x0	0x0	0x7	0x2	0x39	0x0C	0x1	0x09 D000
53	0x0	0x0	0x7	0x2	0x1C	0x0C	0x1	0x06 8000
54	0x0	0x0	0x7	0x2	0x1D	0x0C	0x1	0x06 9000
55	0x0	0x0	0x1	0x2	0x12	0x0D	0x1	0x09 0000
56	0x0	0x0	0x7	0x2	0x13	0x0C	0x1	0x09 2000
57	0x0	0x0	0x1	0x2	0x42	0x0C	0x1	0x0A 4000
58	0x0	0x0	0x7	0x2	0x43	0x0C	0x1	0x0A 6000
59	0x0	0x0	0x1	0x2	0x1A	0x0E	0x1	0x0A 8000
60	0x0	0x0	0x7	0x2	0x1B	0x0C	0x1	0x0A C000
61	0x0	0x0	0x7	0x2	0x20	0x0C	0x1	0x0A D000
62	0x0	0x0	0x7	0x2	0x21	0x0C	0x1	0x0A E000
63	0x0	0x0	0x7	0x2	0x14	0x0C	0x1	0x06 6000
64	0x0	0x0	0x7	0x2	0x15	0x0C	0x1	0x06 7000
65	0x0	0x0	0x7	0x2	0x40	0x0C	0x1	0x0B 4000
66	0x0	0x0	0x7	0x2	0x41	0x0C	0x1	0x0B 5000
67	0x0	0x0	0x7	0x2	0x48	0x0C	0x1	0x0B 8000
68	0x0	0x0	0x7	0x2	0x49	0x0C	0x1	0x0B 9000
69	0x0	0x0	0x7	0x2	0x18	0x0C	0x1	0x0B A000
70	0x0	0x0	0x7	0x2	0x19	0x0C	0x1	0x0B B000
71	0x0	0x0	0x7	0x2	0x28	0x0C	0x1	0x0D 1000
72	0x0	0x0	0x7	0x2	0x29	0x0C	0x1	0x0D 2000
73	0x0	0x0	0x7	0x2	0x30	0x0C	0x1	0x0D 5000
74	0x0	0x0	0x7	0x2	0x31	0x0C	0x1	0x0D 6000
75	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x0A 2000
76	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x0A 3000
77	0x2	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1400
78	0x3	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1800
79	0x4	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1C00
80	0x1	0x0	0x1	0x2	0x42	0x0C	0x1	0x0A 5000
81	0x0	0x0	0x7	0x2	0x3A	0x0C	0x1	0x07 A000
82	0x0	0x0	0x7	0x2	0x3B	0x0C	0x1	0x07 B000
83	0x0	0x0	0x7	0x2	0x4A	0x0C	0x1	0x07 C000
84	0x0	0x0	0x7	0x2	0x4B	0x0C	0x1	0x07 D000

Table 14-562. L4_AP_REGION_l Reset Value for L4 PER2

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x00 0000
1	0x1	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x00 0800
3	0x0	0x0	0x7	0x2	0x0E	0x0C	0x1	0x08 4000
4	0x2	0x0	0x7	0x2	0x0A	0x0C	0x1	0x00 1400
5	0x3	0x0	0x7	0x2	0x0A	0x0C	0x1	0x00 1800
6	0x0	0x0	0x7	0x2	0x11	0x0C	0x1	0x08 8000
7	0x0	0x0	0x7	0x2	0x18	0x0C	0x1	0x02 C000

Table 14-562. L4_AP_REGION_l Reset Value for L4 PER2 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
8	0x0	0x0	0x7	0x2	0x19	0x0C	0x1	0x02 D000
9	0x0	0x0	0x7	0x2	0x0E	0x0D	0x1	0x06 0000
10	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x06 2000
11	0x0	0x0	0x7	0x2	0x1E	0x0D	0x1	0x06 4000
12	0x0	0x0	0x7	0x2	0x1F	0x0C	0x1	0x06 6000
13	0x0	0x0	0x7	0x2	0x26	0x0C	0x1	0x06 8000
14	0x0	0x0	0x7	0x2	0x27	0x0C	0x1	0x06 A000
15	0x0	0x0	0x7	0x2	0x2E	0x0D	0x1	0x06 C000
16	0x0	0x0	0x7	0x2	0x2F	0x0C	0x1	0x6 E000
17	0x0	0x0	0x7	0x2	0x06	0x0C	0x1	0x03 6000
18	0x0	0x0	0x7	0x2	0x07	0x0C	0x1	0x03 8000
19	0x0	0x0	0x7	0x2	0x36	0x0D	0x1	0x07 0000
20	0x0	0x0	0x7	0x2	0x37	0x0C	0x1	0x07 2000
21	0x0	0x0	0x7	0x2	0x3E	0x0C	0x1	0x03 A000
22	0x0	0x0	0x7	0x2	0x3F	0x0C	0x1	0x03 B000
23	0x0	0x0	0x7	0x2	0x08	0x0C	0x1	0x03 C000
24	0x0	0x0	0x7	0x2	0x09	0x0C	0x1	0x03 D000
25	0x0	0x0	0x7	0x2	0x30	0x0C	0x1	0x03 E000
26	0x0	0x0	0x7	0x2	0x31	0x0C	0x1	0x03 F000
27	0x0	0x0	0x7	0x2	0x38	0x0C	0x1	0x04 0000
28	0x1	0x0	0x7	0x2	0x39	0x0C	0x1	0x04 1000
29	0x0	0x0	0x7	0x2	0x20	0x0C	0x1	0x04 2000
30	0x0	0x0	0x7	0x2	0x21	0x0C	0x1	0x04 3000
31	0x0	0x0	0x7	0x2	0x16	0x0D	0x1	0x08 0000
32	0x0	0x0	0x7	0x2	0x17	0x0C	0x1	0x08 2000
33	0x0	0x0	0x7	0x2	0x1A	0x0C	0x1	0x04 A000
34	0x0	0x0	0x7	0x2	0x1B	0x0C	0x1	0x04 B000
35	0x0	0x0	0x7	0x2	0x14	0x0D	0x1	0x07 4000
36	0x0	0x0	0x7	0x2	0x15	0x0C	0x1	0x07 6000
37	0x0	0x0	0x7	0x2	0x24	0x0C	0x1	0x05 0000
38	0x0	0x0	0x7	0x2	0x25	0x0C	0x1	0x05 1000
39	0x0	0x0	0x7	0x2	0x0C	0x0D	0x1	0x07 8000
40	0x0	0x0	0x7	0x2	0x0D	0x0C	0x1	0x07 A000
41	0x0	0x0	0x7	0x2	0x2C	0x0C	0x1	0x05 4000
42	0x0	0x0	0x7	0x2	0x2D	0x0C	0x1	0x05 5000
43	0x0	0x0	0x7	0x2	0x04	0x0D	0x1	0x07 C000
44	0x0	0x0	0x7	0x2	0x05	0x0C	0x1	0x07 E000
45	0x0	0x0	0x7	0x2	0x1C	0x0C	0x1	0x04 C000
46	0x0	0x0	0x7	0x2	0x1D	0x0C	0x1	0x04 D000
47	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x02 0000
48	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x02 1000
49	0x0	0x0	0x7	0x2	0x0A	0x0C	0x1	0x02 2000
50	0x0	0x0	0x7	0x2	0x0B	0x0C	0x1	0x02 3000
51	0x0	0x0	0x7	0x2	0x12	0x0C	0x1	0x02 4000
52	0x0	0x0	0x7	0x2	0x13	0x0C	0x1	0x02 5000
53	0x0	0x0	0x7	0x2	0x40	0x0C	0x1	0x04 6000
54	0x0	0x0	0x7	0x2	0x41	0x0C	0x1	0x04 7000

Table 14-562. L4_AP_REGION_l Reset Value for L4 PER2 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
55	0x0	0x0	0x1	0x2	0x48	0x0C	0x1	0x04 8000
56	0x0	0x0	0x7	0x2	0x49	0x0C	0x1	0x04 9000
57	0x0	0x0	0x1	0x2	0x28	0x0D	0x1	0x05 8000
58	0x0	0x0	0x7	0x2	0x29	0x0C	0x1	0x05 A000
59	0x0	0x0	0x1	0x2	0x46	0x0C	0x1	0x05 B000
60	0x0	0x0	0x7	0x2	0x47	0x0C	0x1	0x05 C000
61	0x0	0x0	0x7	0x2	0x22	0x0C	0x1	0x05 D000
62	0x0	0x0	0x7	0x2	0x23	0x0C	0x1	0x05 E000

Table 14-563. L4_AP_REGION_l Reset Value for L4 PER3

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x00 0000
1	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x00 0800
2	0x1	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1000
3	0x2	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1400
4	0x3	0x0	0x7	0x2	0x0A	0x0C	0x1	0x00 1800
5	0x0	0x0	0x7	0x2	0x08	0x0C	0x1	0x02 0000
6	0x0	0x0	0x7	0x2	0x09	0x0C	0x1	0x02 1000
7	0x0	0x0	0x7	0x2	0x24	0x0C	0x1	0x02 2000
8	0x0	0x0	0x7	0x2	0x25	0x0C	0x1	0x02 3000
9	0x0	0x0	0x7	0x2	0x26	0x0C	0x1	0x02 4000
10	0x0	0x0	0x7	0x2	0x27	0x0C	0x1	0x02 5000
11	0x0	0x0	0x7	0x2	0x0C	0x0C	0x1	0x02 6000
12	0x0	0x0	0x7	0x2	0x0D	0x0C	0x1	0x02 7000
13	0x0	0x0	0x7	0x2	0x16	0x0C	0x1	0x02 8000
14	0x0	0x0	0x7	0x2	0x17	0x0C	0x1	0x02 9000
15	0x0	0x0	0x7	0x2	0x10	0x0C	0x1	0x02 A000
16	0x0	0x0	0x7	0x2	0x11	0x0C	0x1	0x02 B000
17	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x02 C000
18	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x02 D000
19	0x0	0x0	0x7	0x2	0x14	0x0C	0x1	0x02 E000
20	0x0	0x0	0x7	0x2	0x15	0x0C	0x1	0x02 F000
21	0x0	0x0	0x7	0x2	0x0A	0x10	0x1	0x17 0000
22	0x0	0x0	0x7	0x2	0x0B	0x0C	0x1	0x18 0000
23	0x0	0x0	0x7	0x2	0x2E	0x0C	0x1	0x19 0000
24	0x0	0x0	0x7	0x2	0x2F	0x0C	0x1	0x1A 0000
25	0x0	0x0	0x7	0x2	0x34	0x10	0x1	0x1B 0000
26	0x0	0x0	0x7	0x2	0x35	0x0C	0x1	0x1C 0000
27	0x0	0x0	0x7	0x2	0x30	0x0C	0x1	0x1D 0000
28	0x1	0x0	0x7	0x2	0x31	0x0C	0x1	0x1E 0000
29	0x0	0x0	0x7	0x2	0x12	0x0C	0x1	0x03 8000
30	0x0	0x0	0x7	0x2	0x13	0x0C	0x1	0x03 9000
31	0x0	0x0	0x7	0x2	0x32	0x0D	0x1	0x05 C000
32	0x0	0x0	0x7	0x2	0x33	0x0C	0x1	0x05 D000
33	0x0	0x0	0x7	0x2	0x3E	0x0C	0x1	0x03 A000

Table 14-563. L4_AP_REGION_l Reset Value for L4 PER3 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
34	0x0	0x0	0x7	0x2	0x3F	0x0C	0x1	0x03 B000
35	0x0	0x0	0x7	0x2	0x3A	0x0D	0x1	0x03 C000
36	0x0	0x0	0x7	0x2	0x3B	0x0C	0x1	0x03 D000
37	0x0	0x0	0x7	0x2	0x46	0x0C	0x1	0x03 E000
38	0x0	0x0	0x7	0x2	0x47	0x0C	0x1	0x03 F000
39	0x0	0x0	0x7	0x2	0x64	0x0D	0x1	0x04 0000
40	0x0	0x0	0x7	0x2	0x65	0x0D	0x1	0x04 1000
41	0x0	0x0	0x7	0x2	0x4E	0x0C	0x1	0x04 2000
42	0x0	0x0	0x7	0x2	0x4F	0x0C	0x1	0x04 3000
43	0x0	0x0	0x7	0x2	0x42	0x0C	0x1	0x04 4000
44	0x0	0x0	0x7	0x2	0x43	0x0C	0x1	0x04 5000
45	0x0	0x0	0x7	0x2	0x48	0x0C	0x1	0x04 6000
46	0x0	0x0	0x7	0x2	0x49	0x0C	0x1	0x04 7000
47	0x0	0x0	0x7	0x2	0x46	0x0C	0x1	0x04 8000
48	0x0	0x0	0x7	0x2	0x37	0x0C	0x1	0x04 9000
49	0x0	0x0	0x7	0x2	0x38	0x0C	0x1	0x04 A000
50	0x0	0x0	0x7	0x2	0x39	0x0C	0x1	0x04 B000
51	0x0	0x0	0x7	0x2	0x44	0x0C	0x1	0x04 C000
52	0x0	0x0	0x7	0x2	0x45	0x0C	0x1	0x04 D000
53	0x0	0x0	0x7	0x2	0x4C	0x0C	0x1	0x04 E000
54	0x0	0x0	0x7	0x2	0x4D	0x0C	0x1	0x04 F000
55	0x0	0x0	0x7	0x2	0x40	0x0C	0x1	0x05 0000
56	0x0	0x0	0x7	0x2	0x41	0x0C	0x1	0x05 1000
57	0x0	0x0	0x1	0x2	0x54	0x0C	0x1	0x05 2000
58	0x0	0x0	0x7	0x2	0x55	0x0C	0x1	0x05 3000
59	0x0	0x0	0x1	0x2	0x1A	0x0C	0x1	0x05 4000
60	0x0	0x0	0x7	0x2	0x1B	0x0C	0x1	0x05 5000
61	0x0	0x0	0x7	0x2	0x22	0x0C	0x1	0x05 6000
62	0x0	0x0	0x7	0x2	0x23	0x0C	0x1	0x05 7000
63	0x0	0x0	0x7	0x2	0x2A	0x0C	0x1	0x05 8000
64	0x0	0x0	0x7	0x2	0x2B	0x0C	0x1	0x05 9000
65	0x0	0x0	0x7	0x2	0x5C	0x0C	0x1	0x05 A000
66	0x0	0x0	0x7	0x2	0x5D	0x0C	0x1	0x05 B000
67	0x0	0x0	0x7	0x2	0x52	0x0C	0x1	0x06 4000
68	0x0	0x0	0x7	0x2	0x53	0x0C	0x1	0x06 5000
69	0x0	0x0	0x7	0x2	0x6C	0x0C	0x1	0x05 E000
70	0x0	0x0	0x7	0x2	0x6D	0x0C	0x1	0x05 F000
71	0x0	0x0	0x7	0x2	0x4A	0x0C	0x1	0x06 0000
72	0x0	0x0	0x7	0x2	0x4B	0x0C	0x1	0x06 1000
73	0x0	0x0	0x7	0x2	0x74	0x0C	0x1	0x06 2000
74	0x0	0x0	0x7	0x2	0x75	0x0C	0x1	0x06 3000
75	0x0	0x0	0x7	0x2	0x3C	0x0C	0x1	0x14 0000
76	0x0	0x0	0x7	0x2	0x3D	0x0C	0x1	0x16 0000
77	0x0	0x0	0x7	0x2	0x1E	0x0C	0x1	0x01 6000
78	0x0	0x0	0x7	0x2	0x1F	0x0C	0x1	0x01 7000
79	0x0	0x0	0x7	0x2	0x06	0x11	0x1	0x0C 0000
80	0x0	0x0	0x7	0x2	0x07	0x0C	0x1	0x0E 0000

Table 14-563. L4_AP_REGION_l Reset Value for L4 PER3 (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
81	0x0	0x0	0x7	0x2	0x20	0x0C	0x1	0x00 4000
82	0x0	0x0	0x7	0x2	0x21	0x0C	0x1	0x00 5000
83	0x0	0x0	0x7	0x2	0x0E	0x11	0x1	0x08 0000
84	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x0A 0000
85	0x0	0x0	0x7	0x2	0x01	0x11	0x1	0x10 0000
86	0x0	0x0	0x7	0x2	0x05	0x0C	0x1	0x12 0000
87	0x0	0x0	0x7	0x2	0x28	0x0C	0x1	0x01 0000
88	0x0	0x0	0x7	0x2	0x29	0x0C	0x1	0x01 1000
89	0x0	0x0	0x7	0x2	0x18	0x0C	0x1	0x00 A000
90	0x0	0x0	0x7	0x2	0x19	0x0C	0x1	0x00 B000
91	0x0	0x0	0x7	0x2	0x1C	0x0C	0x1	0x01 C000
92	0x0	0x0	0x7	0x2	0x1D	0x0C	0x1	0x01 D000
93	0x0	0x0	0x7	0x2	0x2C	0x0C	0x1	0x01 E000
94	0x0	0x0	0x7	0x2	0x2D	0x0C	0x1	0x01 F000
95	0x0	0x0	0x7	0x2	0x7C	0x0C	0x1	0x00 2000
96	0x0	0x0	0x7	0x2	0x7D	0x0C	0x1	0x00 3000

Table 14-564. L4_AP_REGION_l Reset Value for L4 CFG

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x0 0000
1	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x0 0800
2	0x1	0x0	0x7	0x2	0x00	0x0C	0x1	0x0 1000
3	0x0	0x0	0x7	0x2	0x08	0x0D	0x1	0x0 2000
4	0x0	0x0	0x7	0x2	0x09	0x0C	0x1	0x0 4000
5	0x0	0x0	0x7	0x2	0x10	0x0C	0x1	0x0 5000
6	0x0	0x0	0x7	0x2	0x11	0x0C	0x1	0x0 6000
7	0x0	0x0	0x7	0x2	0x0E	0x0D	0x1	0x0 8000
8	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x0 A000
9	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x5 6000
10	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x5 7000
11	0x0	0x0	0x7	0x2	0x1A	0x0D	0x1	0x5 E000
12	0x0	0x0	0x7	0x2	0x1B	0x0C	0x1	0x6 0000
13	0x0	0x0	0x7	0x2	0x20	0x0F	0x1	0x8 0000
14	0x0	0x0	0x7	0x2	0x21	0x0C	0x1	0x8 8000
15	0x0	0x0	0x7	0x2	0x40	0x0F	0x1	0xA 0000
16	0x0	0x0	0x7	0x2	0x41	0x0C	0x1	0xA 8000
17	0x0	0x0	0x7	0x2	0x72	0x0C	0x1	0xD 9000
18	0x0	0x0	0x7	0x2	0x73	0x0C	0x1	0xD A000
19	0x0	0x0	0x7	0x2	0x18	0x0C	0x1	0xD D000
20	0x0	0x0	0x7	0x2	0x19	0x0C	0x1	0xD E000
21	0x0	0x0	0x5	0x2	0x28	0x0C	0x1	0xE 0000
22	0x0	0x0	0x7	0x2	0x29	0x0C	0x1	0xE 1000
23	0x0	0x0	0x7	0x2	0x04	0x0C	0x1	0xF 4000
24	0x0	0x0	0x7	0x2	0x05	0x0C	0x1	0xF 5000
25	0x0	0x0	0x7	0x2	0x78	0x0C	0x1	0xF 6000

Table 14-564. L4_AP_REGION_l Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
26	0x0	0x0	0x7	0x2	0x79	0x0C	0x1	0xF 7000
27	0x0	0x1	0x7	0x2	0x3C	0x0C	0x1	0x0 2000
28	0x0	0x1	0x7	0x2	0x3D	0x0C	0x1	0x0 3000
29	0x0	0x1	0x7	0x2	0x1E	0x0C	0x1	0x0 8000
30	0x0	0x1	0x7	0x2	0x1F	0x0C	0x1	0x0 9000
31	0x0	0x1	0x7	0x2	0x06	0x10	0x1	0x4 0000
32	0x0	0x1	0x7	0x2	0x07	0x0C	0x1	0x5 0000
33	0x0	0x1	0x1	0x2	0x50	0x0C	0x1	0x5 1000
34	0x0	0x1	0x7	0x2	0x51	0x0C	0x1	0x5 2000
35	0x0	0x1	0x1	0x2	0x54	0x0C	0x1	0x5 3000
36	0x0	0x1	0x7	0x2	0x55	0x0C	0x1	0x5 4000
37	0x0	0x1	0x1	0x2	0x46	0x0C	0x1	0x5 5000
38	0x0	0x1	0x7	0x2	0x47	0x0C	0x1	0x5 6000
39	0x0	0x1	0x1	0x2	0x58	0x0C	0x1	0x5 7000
40	0x0	0x1	0x7	0x2	0x59	0x0C	0x1	0x5 8000
41	0x0	0x1	0x1	0x2	0x60	0x0C	0x1	0x5 B000
42	0x0	0x1	0x7	0x2	0x61	0x0C	0x1	0x5 C000
43	0x0	0x2	0x1	0x2	0x12	0x0C	0x1	0x1 8000
44	0x0	0x2	0x7	0x2	0x13	0x0C	0x1	0x1 9000
45	0x0	0x1	0x1	0x2	0x3A	0x0C	0x1	0x5 D000
46	0x0	0x1	0x7	0x2	0x3B	0x0C	0x1	0x5 E000
47	0x0	0x1	0x1	0x2	0x56	0x0C	0X1	0x5 F000
48	0x0	0x1	0x7	0x2	0x57	0x0C	0x1	0x6 0000
49	0x0	0x1	0x1	0x2	0x32	0x0C	0x1	0x6 1000
50	0x0	0x1	0x7	0x2	0x33	0x0C	0x1	0x6 2000
51	0x0	0x1	0x1	0x2	0x5C	0x0C	0x1	0x6 3000
52	0x0	0x1	0x7	0x2	0x5D	0x0C	0x01	0x6 4000
53	0x0	0x1	0x1	0x2	0x4E	0x0C	0x01	0x6 5000
54	0x0	0x1	0x7	0x2	0x4F	0x0C	0x01	0x6 6000
55	0x0	0x1	0x1	0x2	0x5E	0x0C	0X01	0x6 7000
56	0x0	0x1	0x7	0x2	0x5F	0x0C	0x01	0x6 8000
57	0x0	0x1	0x1	0x2	0x68	0x0C	0x01	0x6 D000
58	0x0	0x1	0x7	0x2	0x69	0x0C	0x01	0x6 E000
59	0x0	0x0	0x7	0x2	0x42	0x0F	0x01	0x9 0000
60	0x0	0x0	0x7	0x2	0x43	0x0C	0x01	0x9 8000
61	0x0	0x1	0x1	0x2	0x48	0x0C	0x01	0x7 1000
62	0x0	0x1	0x7	0x2	0x49	0x0C	0x01	0x7 2000
63	0x0	0x1	0x1	0x2	0x2A	0x0C	0x01	0x7 3000
64	0x0	0x1	0x7	0x2	0x2B	0x0C	0x01	07 4000
65	0x0	0x1	0x1	0x2	0x64	0x0C	0x01	0x7 5000
66	0x0	0x1	0x7	0x2	0x65	0x0C	0x01	0x7 6000
67	0x0	0x1	0x1	0x2	0x66	0x0C	0x01	0x7 7000
68	0x0	0x1	0x7	0x2	0x67	0x0C	0x01	0x7 8000
69	0x0	0x1	0x7	0x2	0x26	0x0C	0x01	0x8 1000
70	0x0	0x1	0x7	0x2	0x27	0x0C	0x01	0x8 2000
71	0x0	0x1	0x7	0x2	0x2E	0x0C	0x01	0x8 3000
72	0x0	0x1	0x7	0x2	0x2F	0x0C	0x01	0x8 4000

Table 14-564. L4_AP_REGION_l Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
73	0x0	0x1	0x7	0x2	0x36	0x0C	0x01	0x8 5000
74	0x0	0x1	0x7	0x2	0x37	0x0C	0x01	0x8 6000
75	0x0	0x1	0x7	0x2	0x74	0x0C	0x01	0x8 7000
76	0x0	0x1	0x7	0x2	0x75	0x0C	0x01	0x8 8000
77	0x0	0x2	0x1	0x2	0x3E	0x0C	0x01	0x0 0000
78	0x0	0x2	0x7	0x2	0x3F	0x0C	0x01	0x0 1000
79	0x0	0x2	0x1	0x2	0x30	0x0C	0x01	0x0 A000
80	0x0	0x2	0x7	0x2	0x31	0x0C	0x01	0x0 B000
81	0x0	0x2	0x1	0x2	0x0C	0x0C	0x01	0x0 C000
82	0x0	0x2	0x7	0x2	0x0D	0x0C	0x01	0x0 D000
83	0x0	0x2	0x1	0x2	0x22	0x0C	0x01	0x0 E000
84	0x0	0x2	0x7	0x2	0x23	0x0C	0x01	0x0 F000
85	0x0	0x2	0x1	0x2	0x14	0x0C	0x01	0x1 0000
86	0x0	0x2	0x7	0x2	0x15	0x0C	0x01	0x1 1000
87	0x0	0x2	0x1	0x2	0x16	0x0C	0x01	0x1 2000
88	0x0	0x2	0x7	0x2	0x17	0x0C	0x01	0x1 3000
89	0x0	0x2	0x1	0x2	0x1C	0x0C	0x01	0x1 4000
90	0x0	0x2	0x7	0x2	0x1D	0x0C	0x01	0x1 5000
91	0x0	0x2	0x1	0x2	0x4C	0x0C	0x01	0x2 A000
92	0x0	0x2	0x7	0x2	0x4D	0x0C	0x01	0x2 B000
93	0x0	0x2	0x1	0x2	0x38	0x0C	0x01	0x1 C000
94	0x0	0x2	0x7	0x2	0x39	0x0C	0X01	0x1 D000
95	0x0	0x2	0x1	0x2	0x0A	0x0C	0x01	0x1 E000
96	0x0	0x2	0x7	0x2	0x0B	0x0C	0x01	0x1 F000
97	0x0	0x2	0x1	0x2	0x24	0x0C	0x01	0x2 0000
98	0x0	0x2	0x7	0x2	0x25	0x0C	0x01	0x2 1000
99	0x0	0x2	0x1	0x2	0x44	0x0C	0x01	0x2 4000
100	0x0	0x2	0x7	0x2	0x45	0x0C	0x01	0x2 5000
101	0x0	0x2	0x1	0x2	0x2C	0x0C	0x01	0x2 6000
102	0x0	0x2	0x7	0x2	0x2D	0x0C	0x01	0x2 7000
103	0x0	0x1	0x1	0x2	0x4A	0x0C	0x01	0x6 9000
104	0x0	0x1	0x7	0x2	0x4B	0x0C	0x01	0x6 A000
105	0x0	0x1	0x1	0x2	0x34	0x0C	0x01	0x7 9000
106	0x0	0x1	0x7	0x2	0x35	0x0C	0x01	0x7 A000
107	0x0	0x1	0x1	0x2	0x52	0x0C	0x01	0x6 B000
108	0x0	0x1	0x7	0x2	0x53	0x0C	0x01	0x6 C000
109	0x0	0x2	0x1	0x2	0x6C	0x0C	0x01	0x2 C000
110	0x0	0x2	0x7	0x2	0x6D	0x0C	0x01	0x2 D000
111	0x0	0x2	0x1	0x2	0x6E	0x0C	0x01	0x2 E000
112	0x0	0x2	0x7	0x2	0x6F	0x0C	0x01	0x2 F000
113	0x0	0x2	0x1	0x2	0x70	0x0C	0x01	0x3 0000
114	0x0	0x2	0x7	0x2	0x71	0x0C	0x01	0x3 1000
115	0x0	0x2	0x1	0x2	0x5A	0x0C	0x01	0x3 2000
116	0x0	0x2	0x7	0x2	0x5B	0x0C	0x01	0x3 3000
117	0x1	0x2	0x1	0x2	0x76	0x0C	0x01	0x3 4000
118	0x0	0x2	0x7	0x2	0x77	0x0C	0x01	0x3 5000
119	0x0	0x2	0x1	0x2	0x62	0x0C	0x01	0x3 6000

Table 14-564. L4_AP_REGION_I Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
120	0x0	0x2	0x7	0x2	0x63	0x0C	0x01	0x3 7000
121	0x0	0x1	0x7	0x2	0x7C	0x0C	0x01	0x7 B000
122	0x0	0x1	0x7	0x2	0x7D	0x0C	0x01	0x7 C000
123	0x0	0x1	0x7	0x2	0x7E	0x0C	0x01	0x7 D000
124	0x0	0x1	0x7	0x2	0x7F	0x0C	0x01	0x7 E000
125	0x0	0x1	0x1	0x2	0x6A	0x0C	0x01	0x5 9000
126	0x0	0x1	0x7	0x2	0x6B	0x0C	0x01	0x5 A000
127	0x0	0x2	0x1	0x2	0x7A	0x0C	0x01	0x1 A000
128	0x0	0x2	0x7	0x2	0x7B	0x0C	0x01	0x1 B000

Table 14-565. L4_AP_REGION_I Reset values for L4 WKUP

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x0	0x0B	0x01	0x0000
1	0x1	0x0	0x7	0x2	0x0	0x0C	0x01	0x1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x01	0x0800
3	0x0	0x0	0x7	0x2	0x10	0x0D	0x01	0x6000
4	0x0	0x0	0x7	0x2	0x11	0x0C	0x01	0x8000
5	0x0	0x1	0x7	0x2	0x20	0x0C	0x01	0x0000
6	0x0	0x1	0x7	0x2	0x21	0x0C	0x01	0x1000
7	0x0	0x1	0x7	0x2	0x28	0x0C	0x01	0x4000
8	0x0	0x1	0x7	0x2	0x29	0x0C	0x01	0x5000
9	0x0	0x1	0x7	0x2	0x30	0x0C	0x01	0x8000
10	0x0	0x1	0x7	0x2	0x31	0x0C	0x01	0x9000
11	0x0	0x1	0x7	0x2	0x38	0x0C	0x01	0xC000
12	0x0	0x1	0x7	0x2	0x39	0x0C	0x01	0xD000
13	0x0	0x2	0x7	0x2	0x48	0x0C	0x01	0x6000
14	0x0	0x2	0x7	0x2	0x49	0x0C	0x01	0xA000
15	0x0	0x0	0x7	0x2	0x40	0x0C	0x01	0x4000
16	0x0	0x0	0x7	0x2	0x41	0x0C	0x01	0x5000
17	0x0	0x0	0x7	0x2	0x50	0x0C	0x01	0xC000
18	0x0	0x0	0x7	0x2	0x51	0x0C	0x01	0xD000
19	0x0	0x2	0x1	0x2	0x08	0x0C	0x01	0x0000
20	0x0	0x2	0x7	0x2	0x09	0x0C	0x01	0x1000
21	0x0	0x2	0x1	0x2	0x18	0x0C	0x01	0x2000
22	0x0	0x2	0x7	0x2	0x19	0x0C	0x01	0x3000
23	0x1	0x2	0x3	0x2	0x48	0x0A	0x01	0x7000
24	0x2	0x2	0x1	0x2	0x48	0x0B	0x01	0x8000
25	0x5	0x2	0x4	0x2	0x48	0x08	0x01	0x9000
26	0x3	0x2	0x1	0x2	0x48	0x09	0x01	0x8800
27	0x4	0x2	0x1	0x2	0x48	0x08	0x01	0x8A00
28	0x0	0x2	0x7	0x2	0x02	0x0C	0x01	0xB000
29	0x0	0x2	0x7	0x2	0x03	0x0C	0x01	0xC000
30	0x0	0x3	0x7	0x2	0x04	0x0D	0x01	0xC000
31	0x0	0x3	0x7	0x2	0x05	0x0C	0x01	0xE000
32	0x0	0x2	0x7	0x2	0x58	0x0C	0x01	0xF000

Table 14-565. L4_AP_REGION_I Reset values for L4 WKUP (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
33	0x0	0x3	0x7	0x2	0x59	0x0C	0x01	0x0000
34	0x0	0x3	0x7	0x2	0x60	0x0C	0x01	0x1000
35	0x0	0x3	0x7	0x2	0x61	0x0C	0x01	0x2000
36	0x0	0x3	0x7	0x2	0x0A	0x0C	0x01	0x3000
37	0x0	0x3	0x7	0x2	0x0B	0x0C	0x01	0x4000
38	0x0	0x3	0x7	0x2	0x0C	0x0C	0x01	0x5000
39	0x0	0x3	0x7	0x2	0x0D	0x0C	0x01	0x6000
40	0x0	0x3	0x7	0x2	0x68	0x0C	0x01	0x7000
41	0x0	0x3	0x7	0x2	0x69	0x0C	0x01	0x8000
42	0x0	0x3	0x7	0x2	0x70	0x0C	0x01	0x9000
43	0x0	0x3	0x7	0x2	0x71	0x0C	0x01	0xA000