Memory Mapping

This chapter describes the memory mapping in the device.

NOTE: ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

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2.1 Introduction

The microprocessor unit (MPU) has a 32-bit address port, which allows it to handle a 4-GiB space divided into several regions, depending on the target type.

The memory map has the following features that are shared among the initiators, such as the MPU subsystem:

- Memory space: General-purpose memory controller (GPMC)
- Dynamic memory management (DMM) controller
- Register spaces: Level 3 (L3) and level 4 (L4) interconnects
- Dedicated spaces: EVE/IPU/DSP subsystem.

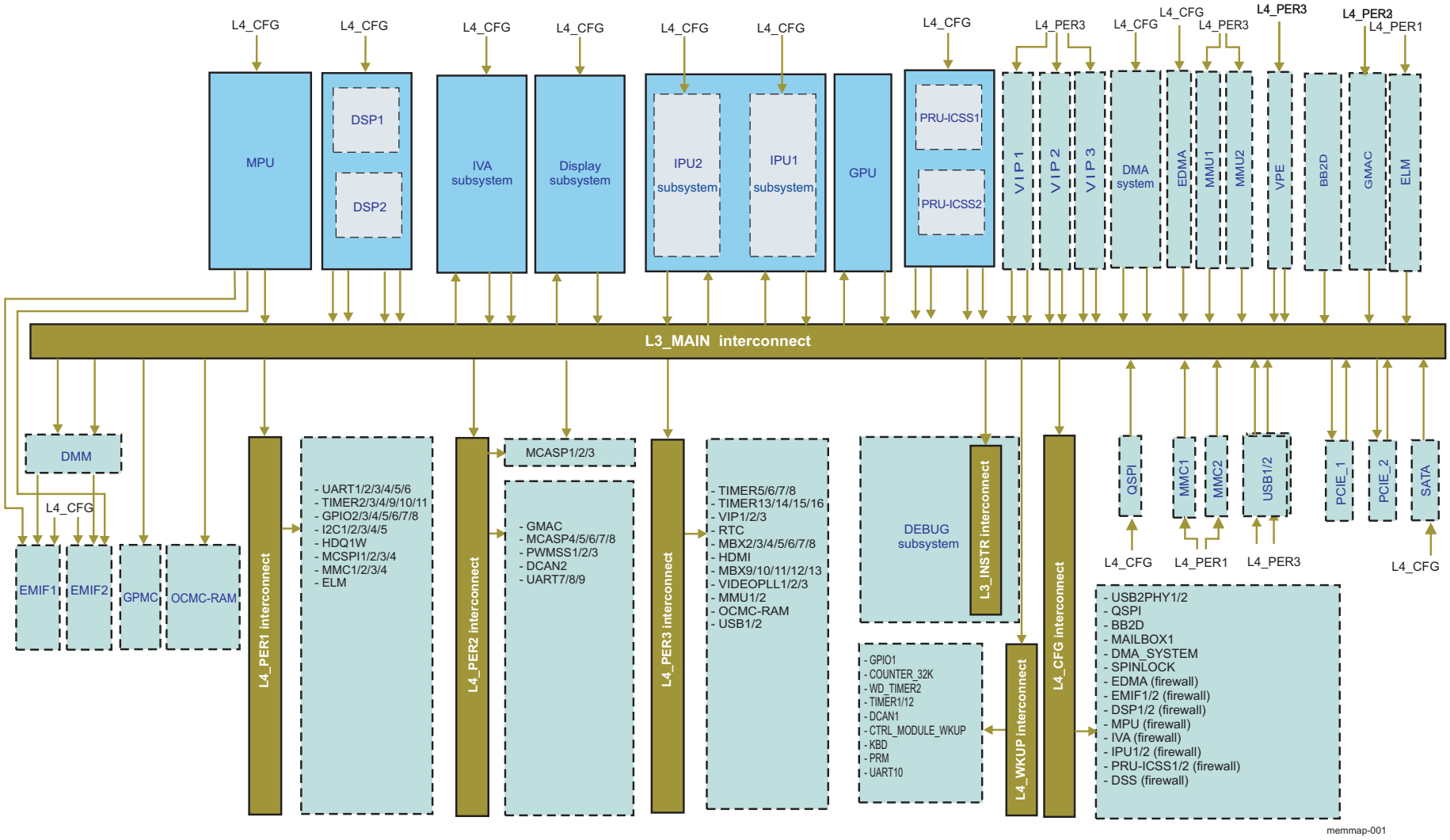
The GPMC and DMM are dedicated to memory connection. The GPMC is used for NOR and NAND flash and static random access memories (SRAMs). The DMM is used for synchronous dynamic random access memories (SDRAMs), such as DDR. For more information, see Section 15.2, *Dynamic Memory Manager*, and Section 15.3, *EMIF Controller*.

The L3 interconnect allows the sharing of resources, such as peripherals and external or on-chip memories, among all the initiators of the platform. The L4 interconnects control access to the peripherals.

Transfers across the platform between initiators and targets are physically conditioned by the chip interconnect and can be logically conditioned by firewalls. For more information about the intercommunication (L3 and L4 interconnects) and protection mechanisms implemented in the device, see Section 14.2, *L3 Interconnect*, and Section 14.3, *L4 Interconnect*.

Figure 2-1 shows the interconnect of the device and the main modules and subsystems in the platform.

Figure 2-1. Interconnect Overview



2.2 L3_MAIN Memory Map

The memory space system is hierarchical: level 1 (L1), level 2 (L2), L3_MAIN, and L4. L1 and L2 are memories in the MPU, IPU, and digital signal processor (DSP) subsystems. L3_MAIN handles many types of data transfers, including data exchange with system on-chip/external memories. The chip-level interconnect, which consists of one L3_MAIN and five L4s, enables communication among all modules and subsystems.

This section provides a global view of the memory mapping of the device at the L3_MAIN interconnect and describes the boot, GPMC, and SDRAM controller (SDRC) (EMIF/DMM) spaces.

The system memory mapping is flexible, with two levels of granularity for target address space allocation:

- L1: The four quarters are labeled Q0, Q1, Q2, and Q3. Each quarter corresponds to a 1-GiB address space (the total low-address space is 4 GiB, 32-bit). The CPU extended address range is labeled as high memory (Q8 – Q15) and provides a total of 8 GiB.
- L2: Each quarter is divided into eight blocks of 32 MiB, with target spaces mapped in the blocks.

This organization allows the decoding of all target spaces based on the 7 most-significant bits (MSBs) of the 32-bit address ([31:25]).

- Boot space:

  When booting from the on-chip ROM with the appropriate external sys_boot pin configuration, the lowest 1-MiB memory space [0x0000 0000–0x000F FFFF] is redirected to the on-chip boot ROM address space [0x4000 0000–0x400F FFFF].

  When booting from the GPMC, the memory space is part of the GPMC address space. At reset, the 0x0000 0000 address is available on chip-select 0 (CS0) for a memory size of 16 MiB.

  For more information about the sys_boot pins configuration, see Section 15.4, *General-Purpose Memory Controller*, and Chapter 33, *Initialization*.
- GPMC space:

  Eight independent GPMC chip-selects (CS0 to CS7) are available in the first quarter (Q0) of the addressing space to access NOR/NAND flash and SRAM. The chip-selects have a programmable start address and programmable size (up to 128 MiB) in a total memory space of (Q0) 1GiB, but limited now to 512 MiB.
- EMIF1/EMIF2 CS0 space:

  Q2 addressing space is interleaved on two DDR-memory controllers (EMIF1 and EMIF2), each activating its CS0 line. These chip-selects can be programmed to 64, 128, 256, 512, 1024, and 2048 MiB. Interleaving occurs at 128-byte granularity.

  The EMIF1-CS0 base address is always 0x8000 0000 at reset, and occupies a 1-GiB address space at reset (interleaving is disabled at reset).

  Q3 addressing space is interleaved on two SDRAM controllers (EMIF1 and EMIF2), each activating its CS0 line. These chip-selects can be programmed to 64, 128, 256, 512, and 1024 MiB. Interleaving occurs at 128-byte granularity.

  EMIF1-CS0 and EMIF2-CS0 in Q3 space are disabled at reset. Their base address is programmable to achieve a continuous address space with the respective CS0 in Q2 space, regardless of the address range programmed.
- TILER space:

  Q3 addressing space is also used to access the TILER system. This space is visible only for the Display Subsystem (DSS). See Table 2-12.
- 8 GiB of SDRAM virtualization (only 4 GiB are physically available; the other 4 GiB are reserved):

  This is a high address range (Q8 – Q15) that requires an address greater than 32 bits. This space is visible only for the MPU Subsystem. See Table 2-8.

Table 2-1 describes the global memory map.

Table 2-1. L3_MAIN Memory Map

Quarter	Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
Q0 (1GiB)	GPMC[1]	0x0000_0000	0x1FFF_FFFF	512MiB	8/16 Ex[2]/R/W
	PCIE_SS1	0x2000_0000	0x2FFF_FFFF	256MiB	PCIe_SS1 Configuration space
	PCIE_SS2	0x3000_0000	0x3FFF_FFFF	256MiB	PCIe_SS2 Configuration space
Q1 (1GiB)	Reserved	0x4000_0000	0x402F_FFFF	3MiB	Reserved
	OCMC_RAM1	0x4030_0000	0x4037_FFFF	512KiB	32bit Ex[2]/R/W
	Reserved	0x4038_0000	0x403F_FFFF	512KiB	Reserved
	OCMC_RAM2	0x4040_0000	0x404F_FFFF	1MiB	32bit Ex[2]/R/W
	OCMC_RAM3	0x4050_0000	0x405F_FFFF	1MiB	32bit Ex[2]/R/W
	Reserved	0x4060_0000	0x407F_FFFF	2MiB	Reserved
	DSP1_L2_SRAM	0x4080_0000	0x4084_7FFF	288KiB	DSP1 L2 SRAM and cache. See Table 2-10.
	Reserved	0x4084_8000	0x40CF_FFFF	4832KiB	Reserved
	DSP1_SYSTEM	0x40D0_0000	0x40D0_0FFF	4KiB	DSP1 System MMR block
	DSP1_MMU0CFG	0x40D0_1000	0x40D0_1FFF	4KiB	DSP1 MMU0 configuration
	DSP1_MMU1CFG	0x40D0_2000	0x40D0_2FFF	4KiB	DSP1 MMU1 configuration
	DSP1_FW0CFG	0x40D0_3000	0x40D0_3FFF	4KiB	DSP1 Firewall 0 config
	DSP1_FW1CFG	0x40D0_4000	0x40D0_4FFF	4KiB	DSP1 Firewall 1 config
	DSP1_EDMA_TC0	0x40D0_5000	0x40D0_5FFF	4KiB	DSP1 EDMA Transfer Controller 0
	DSP1_EDMA_TC1	0x40D0_6000	0x40D0_6FFF	4KiB	DSP1 EDMA Transfer Controller 1
	DSP1_NoC	0x40D0_7000	0x40D0_7FFF	4KiB	DSP1 interconnect registers
	Reserved	0x40D0_8000	0x40D0_FFFF	32KiB	Reserved
	DSP1_EDMA_CC	0x40D1_0000	0x40D1_7FFF	32KiB	DSP1 EDMA Channel Controller
	Reserved	0x40D1_8000	0x40DF_FFFF	928KiB	Reserved
	DSP1_L1P_SRAM	0x40E0_0000	0x40E0_7FFF	32KiB	DSP1 L1P Cache/RAM
	Reserved	0x40E0_8000	0x40EF_FFFF	992KiB	Reserved
	DSP1_L1D_SRAM	0x40F0_0000	0x40F0_7FFF	32KiB	DSP1 L1D Cache/RAM
	Reserved	0x40F0_8000	0x40FF_FFFF	992KiB	Reserved
	DSP2_L2_SRAM	0x4100_0000	0x4104_7FFF	288KiB	DSP2 L2 SRAM and cache. See Table 2-10.
	Reserved	0x4104_8000	0x414F_FFFF	4832KiB	Reserved
	DSP2_SYSTEM	0x4150_0000	0x4150_0FFF	4KiB	DSP2 System MMR block
	DSP2_MMU0CFG	0x4150_1000	0x4150_1FFF	4KiB	DSP2 MMU0 configuration
	DSP2_MMU1CFG	0x4150_2000	0x4150_2FFF	4KiB	DSP2 MMU1 configuration
	DSP2_FW0CFG	0x4150_3000	0x4150_3FFF	4KiB	DSP2 Firewall 0 config
	DSP2_FW1CFG	0x4150_4000	0x4150_4FFF	4KiB	DSP2 Firewall 1 config
	DSP2_EDMA_TC0	0x4150_5000	0x4150_5FFF	4KiB	DSP2 EDMA Transfer Controller 0
	DSP2_EDMA_TC1	0x4150_6000	0x4150_6FFF	4KiB	DSP2 EDMA Transfer Controller 1
	DSP2_NoC	0x4150_7000	0x4150_7FFF	4KiB	DSP2 interconnect registers
	Reserved	0x4150_8000	0x4150_FFFF	32KiB	Reserved
	DSP2_EDMA_CC	0x4151_0000	0x4151_7FFF	32KiB	DSP2 EDMA Channel Controller
	Reserved	0x4151_8000	0x415F_FFFF	928KiB	Reserved
	DSP2_L1P_SRAM	0x4160_0000	0x4160_7FFF	32KiB	DSP2 L1P Cache/RAM
	Reserved	0x4160_8000	0x416F_FFFF	992KiB	Reserved
	DSP2_L1D_SRAM	0x4170_0000	0x4170_7FFF	32KiB	DSP2 L1D Cache/RAM
	Reserved	0x4170_8000	0x417F_FFFF	992KiB	Reserved

(1) Boot space location depends on the external sys_boot [5:0] pins.
(2) Ex = Executable

Table 2-1. L3_MAIN Memory Map (continued)

Quarter	Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
	OCMC_RAM1_CBUF	0x4180_0000	0x41FF_FFFF	8MiB	OCMC RAM1 CBUF virtual address space (Bit 31 needs to be set on the OCMC data interface)
	EVE1[3]	0x4200_0000	0x420F_FFFF	1MiB	EVE1 configuration space
	EVE2[3]	0x4210_0000	0x421F_FFFF	1MiB	EVE2 configuration space
	EVE3[3]	0x4220_0000	0x422F_FFFF	1MiB	EVE3 configuration space
	EVE4[3]	0x4230_0000	0x423F_FFFF	1MiB	EVE4 configuration space
	Reserved	0x4240_0000	0x432F_FFFF	15MiB	Reserved
	EDMA_TPCC	0x4330_0000	0x433F_FFFF	1MiB	EDMA TPCC configuration space
	EDMA_TC0	0x4340_0000	0x434F_FFFF	1MiB	EDMA TPTC1 configuration space
	EDMA_TC1	0x4350_0000	0x435F_FFFF	1MiB	EDMA TPTC2 configuration space
	Reserved	0x4360_0000	0x43FF_FFFF	10MiB	Reserved
	L3_MAIN_SN	0x4400_0000	0x457F_FFFF	24MiB	L3 configuration registers (Service Network)
	McASP1	0x4580_0000	0x45BF_FFFF	4MiB	McASP1 data port
	McASP2	0x45C0_0000	0x45FF_FFFF	4MiB	McASP2 data port
	McASP3	0x4600_0000	0x463F_FFFF	4MiB	McASP3 data port
	VCP1[3]	0x4640_0000	0x4640_FFFF	64KiB	VCP1 configuration space
	Reserved	0x4641_0000	0x467F_FFFF	4MiB	Reserved
	VCP2[3]	0x4680_0000	0x4680_FFFF	64KiB	VCP2 configuration space
	Reserved	0x4681_0000	0x47FF_FFFF	24MiB	Reserved
	L4_PER1	0x4800_0000	0x481F_FFFF	2MiB	L4_PER1 domain. See Table 2-5
	Reserved	0x4820_0000	0x483F_FFFF	2MiB	MPU private memory space. See Table 2-8
	L4_PER2	0x4840_0000	0x487F_FFFF	4MiB	L4_PER2 domain. See Table 2-6
	L4_PER3	0x4880_0000	0x48FF_FFFF	8MiB	L4_PER3 domain. See Table 2-7
	OCMC_RAM2_CBUF	0x4900_0000	0x497F_FFFF	8MiB	OCMC RAM2 CBUF virtual address space (Bit 31 needs to be set on the OCMC data interface)
	OCMC_RAM3_CBUF	0x4980_0000	0x49FF_FFFF	8MiB	OCMC RAM3 CBUF virtual address space (Bit 31 needs to be set on the OCMC data interface)
	L4_CFG	0x4A00_0000	0x4ADF_FFFF	14MiB	L4_CFG domain. See Table 2-3
	L4_WKUP	0x4AE0_0000	0x4AFF_FFFF	2MiB	L4_WKUP domain. See Table 2-4
	Reserved	0x4B00_0000	0x4B1F_FFFF	2MiB	Reserved
	PRU-ICSS1	0x4B20_0000	0x4B27_FFFF	512KiB	PRU-ICSS1 configuration registers
	PRU-ICSS2	0x4B28_0000	0x4B2F_FFFF	512KiB	PRU-ICSS2 configuration registers
	QSPI_ADDRSP0	0x4B30_0000	0x4B3F_FFFF	1MiB	QSPI MMR space (Maddrspace 0)
	Reserved	0x4B40_0000	0x4BFF_FFFF	12MiB	Reserved
	EMIF1	0x4C00_0000	0x4CFF_FFFF	16MiB	EMIF1 configuration registers
	EMIF2	0x4D00_0000	0x4DFF_FFFF	16MiB	EMIF2 configuration registers
	DMM	0x4E00_0000	0x4FFF_FFFF	32MiB	DMM configuration registers
	GPMC	0x5000_0000	0x50FF_FFFF	16MiB	GPMC configuration registers
	PCIE_SS1	0x5100_0000	0x517F_FFFF	8MiB	PCIE_SS1 configuration registers
	PCIE_SS2	0x5180_0000	0x51FF_FFFF	8MiB	PCIE_SS2 configuration registers
	Reserved	0x5200_0000	0x53FF_FFFF	32MiB	Reserved
	L3_INSTR	0x5400_0000	0x547F_FFFF	8MiB	Emulation domain. See Table 2-2
	CT_TBR	0x5480_0000	0x54FF_FFFF	8MiB	Emulation domain. See Table 2-2
	IPU2_ROM[4]	0x5500_0000	0x5500_3FFF	16KiB	IPU2_ROM
	Reserved	0x5500_4000	0x5501_FFFF	112KiB	Reserved
	IPU2_RAM[4]	0x5502_0000	0x5502_FFFF	64KiB	IPU2_RAM

(3) ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.
(4) IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing.

Table 2-1. L3_MAIN Memory Map (continued)

Quarter	Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
	Reserved	0x5503_0000	0x5507_FFFF	320KiB	Reserved
	IPU2_UNICACHE_MMU [4]	0x5508_0000	0x5508_0FFF	4KiB	IPU2_UNICACHE_MMU config registers
	IPU2_WUGEN [4]	0x5508_1000	0x5508_1FFF	4KiB	IPU2_WUGEN config registers
	IPU2_MMU [4]	0x5508_2000	0x5508_2FFF	4KiB	IPU2_MMU config registers
	Reserved	0x5508_3000	0x55FF_FFFF	15860KB	Reserved
	GPU	0x5600_0000	0x57FF_FFFF	32MiB	3D GPU domain
	DSS	0x5800_0000	0x587F_FFFF	8MiB	DSS domain
	IPU1_ROM	0x5880_0000	0x58FF_FFFF	16KiB	IPU1_ROM
	Reserved	0x5880_4000	0x5881_FFFF	112KiB	Reserved
	IPU1_RAM	0x5882_0000	0x5882_FFFF	64KiB	IPU1_RAM
	Reserved	0x5883_0000	0x5887_FFFF	320KiB	Reserved
	IPU1_UNICACHE_MMU	0x5888_0000	0x5888_0FFF	4KiB	IPU1_UNICACHE_MMU config registers
	IPU1_WUGEN	0x5888_1000	0x5888_1FFF	4KiB	IPU1_WUGEN config registers
	IPU1_MMU	0x5888_2000	0x5888_2FFF	4KiB	IPU1_MMU config registers
	Reserved	0x5888_3000	0x58FF_FFFF	8MiB	Reserved
	BB2D	0x5900_0000	0x59FF_FFFF	16MiB	2D graphics accelerator
	IVA_CONFIG	0x5A00_0000	0x5A3F_FFFF	4MiB	IVA CONFIG domain
	Reserved	0x5A40_0000	0x5AFF_FFFF	12MiB	Reserved
	IVA_SL2IF	0x5B00_0000	0x5B3F_FFFF	4MiB	IVA SL2IF domain
	Reserved	0x5B40_0000	0x5BFF_FFFF	12MiB	Reserved
	QSPI_ADDRSP1	0x5C00_0000	0x5FFF_FFFF	64MiB	QSPI CS0/CS1/CS2/CS3 space (Maddrspace 1)
	TILER	0x6000_0000	0x7FFF_FFFF	512MiB	SDRAM addressing through DMM with TILER off
Q2 [5] (1GiB)	DDR-SDRAM address space				
	EMIF1_SDRAM_CS0	0x8000_0000	0xBFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR
	EMIF2_SDRAM_CS0	0x8000_0000	0xBFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR
Q3 [6] (1GiB)	EMIF1_SDRAM_CS0	0xC000_0000	0xFFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR
	EMIF2_SDRAM_CS0	0xC000_0000	0xFFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR

[5] Depending on the DMM_LISA_MAP_i settings the Q2 address space can be configured in the following ways:
- Allocated only to EMIF1_SDRAM_CS0
- Allocated only to EMIF2_SDRAM_CS0
- Shared between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0 but not interleaved
- Interleaved between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0

The same applies to the Q3 address space.

[6] Depending on the DMM_LISA_MAP_i settings the Q2 address space can be configured in the following ways:
- Allocated only to EMIF1_SDRAM_CS0
- Allocated only to EMIF2_SDRAM_CS0
- Shared between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0 but not interleaved
- Interleaved between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0

The same applies to the Q3 address space.

2.2.1 L3_INSTR Memory Map

The L3_INSTR interconnect is a 8-MiB space composed of the L3_INSTR interconnect configuration registers and module registers.

Table 2-2 describes the mapping of the registers for the L3_INSTR interconnect.

Table 2-2. L3_INSTR Memory Map

Region name	Start_address (hex)	End_address (hex)	Size	Description
CT_STM_ADD_SP_0	0x5400_0000	0x540F_FFFF	1MiB	MIPI_STM - System Trace (address space 0)
CT_STM_ADD_SP_1	0x5410_0000	0x5413_FFFF	256KiB	MIPI_STM - System Trace (address space 1)
MPU_C0_DEBUG	0x5414_0000	0x5414_1FFF	8KiB	MPU_C0 Debug Performance Monitoring Unit
MPU_C1_DEBUG	0x5414_2000	0x5414_3FFF	8KiB	MPU_C1 Debug Performance Monitoring Unit
Reserved	0x5414_4000	0x5414_7FFF	16KiB	Reserved
MPU_C0_CS_CTI_MPU	0x5414_8000	0x5414_8FFF	4KiB	Cross Triggering Interface (CTI0 component)
MPU_C1_CS_CTI_MPU	0x5414_9000	0x5414_9FFF	4KiB	Cross Triggering Interface (CTI1 component)
Reserved	0x5414_A000	0x5414_BFFF	8KiB	Reserved
MPU_C0_CS_PTM_MPU	0x5414_C000	0x5414_CFFF	4KiB	Processor Trace Macrocell Component 0
MPU_C1_CS_PTM_MPU	0x5414_D000	0x5414_DFFF	4KiB	Processor Trace Macrocell Component 1
Reserved	0x5414_E000	0x5415_7FFF	40KiB	Reserved
MPU_CS_TF	0x5415_8000	0x5415_8FFF	4KiB	CS_TF (APBv3) - Trace Funnel for MPU
DAP_PC	0x5415_9000	0x5415_9FFF	4KiB	DAP_PC
MPU_CS_STM	0x5415_A000	0x5415_AFFF	4KiB	CoreSight™ System Trace Module
ATB_FIFO_SGU	0x5415_B000	0x5415_BFFF	4KiB	AMBA® Trace Buffer Static Gathering Unit
Reserved	0x5415_C000	0x5415_EFFF	12KiB	Reserved
T2ASYNC_APB_MPU_DEBUG _MPU_MPU	0x5415_F000	0x5415_FFFF	4KiB	APB Bridge control and time-out register
DRM	0x5416_0000	0x5416_0FFF	4KiB	DRM (OCP) - Debug Register Mapping
CT_STM_CONF_PORT	0x5416_1000	0x5416_1FFF	4KiB	MIPI_STM(OCP) configuration port - System Trace
Reserved	0x5416_2000	0x5416_2FFF	4KiB	Reserved
CS_TPIU	0x5416_3000	0x5416_3FFF	4KiB	CS_TPIU (APBv3) - Trace Port Interface Unit
DEBUGSS_CS_TF_1	0x5416_4000	0x5416_4FFF	4KiB	CS_TF (APBv3) - Trace Funnel for DEBUGSS
Reserved	0x5416_5000	0x5416_6FFF	8KiB	Reserved
CT_TBR	0x5416_7000	0x5416_7FFF	4KiB	C-Tools Trace Buffer
CT_UART	0x5416_8000	0x5416_8FFF	4KiB	C-Tools UART
DEBUGSS_CS_CTI	0x5416_9000	0x5416_9FFF	4KiB	Cross Triggering Interface
DEBUGSS_CS_CTM	0x5416_A000	0x5416_AFFF	4KiB	Core Sight -System Trace Module
MASTER_TIMESTAMP	0x5416_B000	0x5416_BFFF	4KiB	Master Time Stamp
Reserved	0x5416_C000	0x5417_0FFF	20KiB	Reserved
DEBUGSS_OCP2SCP	0x5417_1000	0x5417_1FFF	4KiB	Interconnect registers
L4_CFG_EMU	0x5417_2000	0x5417_2FFF	4KiB	Interconnect registers
Reserved	0x5417_3000	0x5417_FFFF	52KiB	Reserved
L3_INSTR_EMU	0x5418_0000	0x5418_0FFF	4KiB	Interconnect registers
Reserved	0x5418_1000	0x547F_FFFF	6652KiB	Reserved

2.3 L4 Memory Map

The L4 interconnects handle transfers with peripherals. The L4 interconnect comprises the following interconnects:

- L4_CFG
- L4_WKUP
- L4_PER1
- L4_PER2
- L4_PER3

The L4 interconnect can be configured to tune the access according to the characteristics of each module.

The following sections describe the register mapping of the L4 interconnect. Software configures these registers.

2.3.1 L4_CFG Memory Map

The L4_CFG interconnect is a 12-MiB space composed of the L4_CFG interconnect configuration registers and the module registers.

Table 2-3 describes the mapping of the registers for the L4_CFG interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_CFG interconnect. All other accesses are internal to the L4_CFG interconnect.

Table 2-3. L4_CFG Memory Map

Module name	Region Name	Start_address (hex)	End_address (hex)	Size	Description
L4_CFG	L4_CFG_AP	0x4A00_0000	0x4A00_07FF	2KiB	Address protection
	L4_CFG_LA	0x4A00_0800	0x4A00_0FFF	2KiB	Link agent
	L4_CFG_IA_IP0	0x4A00_1000	0x4A00_1FFF	4KiB	Initiator port
CTRL_MODULE_CORE	TP_CTRL_MODULE_CORE_TARG	0x4A00_2000	0x4A00_3FFF	8KiB	Module target port
	TA_CTRL_MODULE_CORE_TARG	0x4A00_4000	0x4A00_4FFF	4KiB	L4 target agent
CM_CORE_AON	TP_CM_CORE_AON_TARG	0x4A00_5000	0x4A00_5FFF	4KiB	Module target port
	TA_CM_CORE_AON_TARG	0x4A00_6000	0x4A00_6FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A00_7000	0x4A00_7FFF	4KiB	Reserved
CM_CORE	TP_CM_CORE_TARG	0x4A00_8000	0x4A00_9FFF	8KiB	Module target port
	TA_CM_CORE_TARG	0x4A00_A000	0x4A00_AFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A00_B000	0x4A05_5FFF	148KiB	Reserved
DMA_SYSTEM	TP_DMA_SYSTEM_TARG	0x4A05_6000	0x4A05_6FFF	4KiB	Module target port
	TA_DMA_SYSTEM_TARG	0x4A05_7000	0x4A05_7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A05_8000	0x4A07_FFFF	156KiB	Reserved
OCP2SCP1	TP_OCP2SCP1_TARG	0x4A08_0000	0x4A08_3FFF	16KiB	Module target port - OCP2SCP module registers
	TP_OCP2SCP1_USB_PHY1_CORE_TARG	0x4A08_4000	0x4A08_43FF	1KiB	Module target port - OCP2SCP target - USB2PHY1
	Reserved	0x4A08_4400	0x4A08_47FF	1KiB	Reserved
	Reserved	0x4A08_4800	0x4A08_4BFF	1KiB	Reserved
	TP_OCP2SCP1_DPLLCTRL_USB_OTG_SS_TARG	0x4A08_4C00	0x4A08_4FFF	1KiB	Module target port - OCP2SCP target- DPLLCTRL_USB_OTG_SS
	TP_OCP2SCP1_USB_PHY2_CORE_TARG	0x4A08_5000	0x4A08_53FF	1KiB	Module target port - OCP2SCP target - USB2PHY2

Table 2-3. L4_CFG Memory Map (continued)

Module name	Region Name	Start_address (hex)	End_address (hex)	Size	Description
Reserved	Reserved	0x4A08_5400	0x4A08_7FFF	11KiB	Reserved
L4_CFG	TA_OCP2SCP1_TARG	0x4A08_8000	0x4A08_8FFF	4Kib	L4 target agent
Reserved	Reserved	0x4A08_9000	0x4A08_FFFF	28KiB	Reserved
OCP2SCP3	TP_OCP2SCP3_TARG	0x4A09_0000	0x4A09_3FFF	16KiB	Module target port - OCP2SCP module registers
	Reserved	0x4A09_4000	0x4A09_43FF	1KiB	Reserved
	Reserved	0x4A09_4400	0x4A09_47FF	1KiB	Reserved
	TP_OCP2SCP3_DPLLCTRL_PCIE1_TARG	0x4A09_4800	0x4A09_4BFF	1KiB	Module target port - OCP2SCP target-DPLLCTRL_PCIE
Reserved	Reserved	0x4A09_4C00	0x4A09_4FFF	1KiB	Reserved
OCP2SCP3	Reserved	0x4A09_5000	0x4A09_53FF	1KiB	Reserved
	Reserved	0x4A09_5400	0x4A09_57FF	1KiB	Reserved
Reserved	Reserved	0x4A09_5800	0x4A09_5FFF	2KiB	Reserved
OCP2SCP3	Reserved	0x4A09_6000	0x4A09_63FF	1KiB	Reserved
	Reserved	0x4A09_6400	0x4A09_67FF	1KiB	Reserved
	TP_OCP2SCP3_DPLLCTRL_SATA_TARG	0x4A09_6800	0x4A09_6BFF	1KiB	Module target port - OCP2SCP target-DPLLCTRL_SATA
Reserved	Reserved	0x4A09_6C00	0x4A09_7FFF	5KiB	Reserved
L4_CFG	TA_OCP2SCP3_TARG	0x4A09_8000	0x4A09_8FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A09_9000	0x4A09_FFFF	28KiB	Reserved
OCP2SCP2	TP_OCP2SCP2_TARG	0x4A0A_0000	0x4A0A_3FFF	16KiB	Module target port - OCP2SCP module registers
	TP_OCP2SCP2_DPLLCTRL_VIDEO1_TARG	0x4A0A_4000	0x4A0A_43FF	1KiB	Module target port - OCP2SCP target - DPLLCTRL_VIDEO1
Reserved	Reserved	0x4A0A_4400	0x4A0A_4FFF	3KiB	Reserved
OCP2SCP2	TP_OCP2SCP2_DPLLCTRL_VIDEO2_TARG	0x4A0A_5000	0x4A0A_53FF	1KiB	Module target port - OCP2SCP target - DPLLCTRL_VIDEO2
Reserved	Reserved	0x4A0A_5400	0x4A0A_5FFF	3KiB	Reserved
OCP2SCP2	TP_OCP2SCP2_DPLLCTRL_HDMI_TARG	0x4A0A_6000	0x4A0A_63FF	1KiB	Module target port - OCP2SCP target - DPLLCTRL_HDMI
Reserved	Reserved	0x4A0A_6400	0x4A0A_7FFF	7KiB	Reserved
L4_CFG	TA_OCP2SCP2_TARG	0x4A0A_8000	0x4A0A_8FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A0A_9000	0x4A0F_3FFF	300KiB	Reserved
MAILBOX1	TP_MAILBOX1_TARG	0x4A0F_4000	0x4A0F_4FFF	4KiB	Module target port
	TA_MAILBOX1_TARG	0x4A0F_5000	0x4A0F_5FFF	4KiB	L4 target agent
SPINLOCK	TP_SPINLOCK_TARG	0x4A0F_6000	0x4A0F_6FFF	4KiB	Module target port
	TA_SPINLOCK_TARG	0x4A0F_7000	0x4A0F_7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A0F_8000	0x4A10_1FFF	40KiB	Reserved
OCP_WP_NOC	TP_OCP_WP_NOC_TARG	0x4A10_2000	0x4A10_2FFF	4KiB	Module target port
	TA_OCP_WP_NOC_TARG	0x4A10_3000	0x4A10_3FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A10_4000	0x4A13_FFFF	240KiB	Reserved
SATA	TP_SATA_TARG	0x4A14_0000	0x4A14_FFFF	64KiB	Module target port
	TA_SATA_TARG	0x4A15_0000	0x4A15_0FFF	4KiB	L4 target agent

Table 2-3. L4_CFG Memory Map (continued)

Module name	Region Name	Start_address (hex)	End_address (hex)	Size	Description
EVE1 (1)	TP_EVE1_FW_CFG_TARG	0x4A15_1000	0x4A15_1FFF	4KiB	Module target port
	TA_EVE1_FW_CFG_TARG	0x4A15_2000	0x4A15_2FFF	4KiB	L4 target agent
EVE2 (1)	TP_EVE2_FW_CFG_TARG	0x4A15_3000	0x4A15_3FFF	4KiB	Module target port
	TA_EVE2_FW_CFG_TARG	0x4A15_4000	0x4A15_4FFF	4KiB	L4 target agent
EVE3 (1)	TP_EVE3_FW_CFG_TARG	0x4A15_5000	0x4A15_5FFF	4KiB	Module target port
	TA_EVE3_FW_CFG_TARG	0x4A15_6000	0x4A15_6FFF	4KiB	L4 target agent
EVE4 (1)	TP_EVE4_FW_CFG_TARG	0x4A15_7000	0x4A15_7FFF	4KiB	Module target port
	TA_EVE4_FW_CFG_TARG	0x4A15_8000	0x4A15_8FFF	4KiB	L4 target agent
PCIE_SS2	TP_PCIE_SS2_FW_CFG_TARG	0x4A15_9000	0x4A15_9FFF	4KiB	Module target port
	TA_PCIE_SS2_FW_CFG_TARG	0x4A15_A000	0x4A15_AFFF	4KiB	L4 target agent
IPU1	TP_IPU1_FW_CFG_TARG	0x4A15_B000	0x4A15_BFFF	4KiB	Module target port
	TA_IPU1_FW_CFG_TARG	0x4A15_C000	0x4A15_CFFF	4KiB	L4 target agent
VCP1 (1)	TP_VCP1_FW_CFG_TARG	0x4A15_D000	0x4A15_DFFF	4KiB	Module target port
	TA_VCP1_FW_CFG_TARG	0x4A15_E000	0x4A15_EFFF	4KiB	L4 target agent
VCP2 (1)	TP_VCP2_FW_CFG_TARG	0x4A15_F000	0x4A15_FFFF	4KiB	Module target port
	TA_VCP2_FW_CFG_TARG	0x4A16_0000	0x4A16_0FFF	4KiB	L4 target agent
EDMA_TPCC	TP_EDMA_TPCC_FW_CFG _TARG	0x4A16_1000	0x4A16_1FFF	4KiB	Module target port
	TA_EDMA_TPCC_FW_CFG_TARG	0x4A16_2000	0x4A16_2FFF	4KiB	L4 target agent
EDMA_TC0	TP_EDMA_TC0_FW_CFG_TARG	0x4A16_3000	0x4A16_3FFF	4KiB	Module target port
	TA_EDMA_TC0_FW_CFG_TARG	0x4A16_4000	0x4A16_4FFF	4KiB	L4 target agent
PCIE_SS1	TP_PCIE_SS1_FW_CFG_TARG	0x4A16_5000	0x4A16_5FFF	4KiB	Module target port
	TA_PCIE_SS1_FW_CFG_TARG	0x4A16_6000	0x4A16_6FFF	4KiB	L4 target agent
McASP1	TP_MCASP1_FW_CFG_TARG	0x4A16_7000	0x4A16_7FFF	4KiB	Module target port
	TA_MCASP1_FW_CFG_TARG	0x4A16_8000	0x4A16_8FFF	4KiB	L4 target agent
McASP2	TP_MCASP2_FW_CFG_TARG	0x4A16_9000	0x4A16_9FFF	4KiB	Module target port
	TA_MCASP2_FW_CFG_TARG	0x4A16_A000	0x4A16_AFFF	4KiB	L4 target agent
McASP3	TP_MCASP3_FW_CFG_TARG	0x4A16_B000	0x4A16_BFFF	4KiB	Module target port
	TA_MCASP3_FW_CFG_TARG	0x4A16_C000	0x4A16_CFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A16_D000	0x4A17_0FFF	16KiB	Reserved
DSP1	TP_DSP1_FW_CFG_TARG	0x4A17_1000	0x4A17_1FFF	4KiB	Module target port
	TA_DSP1_FW_CFG_TARG	0x4A17_2000	0x4A17_2FFF	4KiB	L4 target agent
DSP2	TP_DSP2_FW_CFG_TARG	0x4A17_3000	0x4A17_3FFF	4KiB	Module target port
	TA_DSP2_FW_CFG_TARG	0x4A17_4000	0x4A17_4FFF	4KiB	L4 target agent
PRU-ICSS1	TP_PRUSS1_FW_CFG_TARG	0x4A17_5000	0x4A17_5FFF	4KiB	Module target port
	TA_PRUSS1_FW_CFG_TARG	0x4A17_6000	0x4A17_6FFF	4KiB	L4 target agent
PRU-ICSS2	TP_PRUSS2_FW_CFG_TARG	0x4A17_7000	0x4A17_7FFF	4KiB	Module target port
	TA_PRUSS2_FW_CFG_TARG	0x4A17_8000	0x4A17_8FFF	4KiB	L4 target agent
QSPI	TP_QSPI_FW_CFG_TARG	0x4A17_9000	0x4A17_9FFF	4KiB	Module target port
	TA_QSPI_FW_CFG_TARG	0x4A17_A000	0x4A17_AFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A17_B000	0x4A20_9FFF	572KiB	Reserved
MA_MPU_NTTP	TP_MA_MPU_NTTP_FW_CFG_TARG	0x4A20_A000	0x4A20_AFFF	4KiB	Module target port
	TA_MA_MPU_NTTP_FW_CFG_TARG	0x4A20_B000	0x4A20_BFFF	4KiB	L4 target agent
EMIF_OCP_FW	TP_EMIF_OCP_FW_CFG_TARG	0x4A20_C000	0x4A20_CFFF	4KiB	Module target port
	TA_EMIF_OCP_FW_CFG_TARG	0x4A20_D000	0x4A20_DFFF	4KiB	L4 target agent
OCMC_RAM2	TP_OCMC_RAM2_FW_CFG_TARG	0x4A20_E000	0x4A20_EFFF	4KiB	Module target port
	TA_OCMC_RAM2_FW_CFG_TARG	0x4A20_F000	0x4A20_FFFF	4KiB	L4 target agent

(1) ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 2-3. L4_CFG Memory Map (continued)

Module name	Region Name	Start_address (hex)	End_address (hex)	Size	Description
GPMC	TP_GPMC_FW_CFG_TARG	0x4A21_0000	0x4A21_0FFF	4KiB	Module target port
	TA_GPMC_FW_CFG_TARG	0x4A21_1000	0x4A21_1FFF	4KiB	L4 target agent
OCMC_RAM1	TP_OCMC_RAM1_FW_CFG_TARG	0x4A21_2000	0x4A21_2FFF	4KiB	Module target port
	TA_OCMC_RAM1_FW_CFG_TARG	0x4A21_3000	0x4A21_3FFF	4KiB	L4 target agent
GPU	TP_GPU_FW_CFG_TARG	0x4A21_4000	0x4A21_4FFF	4KiB	Module target port
	TA_GPU_FW_CFG_TARG	0x4A21_5000	0x4A21_5FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A21_6000	0x4A21_7FFF	8KiB	Reserved
IPU2[(2)]	TP_IPU2_FW_CFG_TARG	0x4A21_8000	0x4A21_8FFF	4KiB	Module target port
	TA_IPU2_FW_CFG_TARG	0x4A21_9000	0x4A21_9FFF	4KiB	L4 target agent
BB2D	TP_BB2D_FW_CFG_TARG	0x4A21_A000	0x4A21_AFFF	4KiB	Module target port
	TA_BB2D_FW_CFG_TARG	0x4A21_B000	0x4A21_BFFF	4KiB	L4 target agent
DSS	TP_DSS_FW_CFG_TARG	0x4A21_C000	0x4A21_CFFF	4KiB	Module target port
	TA_DSS_FW_CFG_TARG	0x4A21_D000	0x4A21_DFFF	4KiB	L4 target agent
IVA	TP_IVA_SL2IF_FW_CFG_TARG	0x4A21_E000	0x4A21_EFFF	4KiB	Module target port
	TA_IVA_SL2IF_FW_CFG_TARG	0x4A21_F000	0x4A21_FFFF	4KiB	L4 target agent
IVA	TP_IVA_CONFIG_FW_CFG_TARG	0x4A22_0000	0x4A22_0FFF	4KiB	Module target port
	TA_IVA_CONFIG_FW_CFG_TARG	0x4A22_1000	0x4A22_1FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A22_2000	0x4A22_3FFF	8KiB	Reserved
DEBUGSS	TP_DEBUGSS_CT_TBR _FW_CFG_TARG	0x4A22_4000	0x4A22_4FFF	4KiB	Module target port. See Table 2-2
	TA_DEBUGSS_CT_TBR _FW_CFG_TARG	0x4A22_5000	0x4A22_5FFF	4KiB	L4 target agent
L3_INSTR	TP_L3_INSTR_FW_CFG_TARG	0x4A22_6000	0x4A22_6FFF	4KiB	Module target port
	TA_L3_INSTR_FW_CFG_TARG	0x4A22_7000	0x4A22_7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A22_8000	0x4A22_9FFF	8MiB	Reserved
OCMC_RAM3	TP_OCMC_RAM3_FW_CFG_TARG	0x4A22_A000	0x4A22_AFFF	4MiB	Module target port
	TA_OCMC_RAM3_FW_CFG_TARG	0x4A22_B000	0x4A22_BFFF	4MiB	L4 target agent
Reserved	Reserved	0x4A22_C000	0x4ADF_FFFF	12112MiB	Reserved

(2) IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing.

2.3.2 L4_WKUP Memory Map

The L4_WKUP interconnect is a 256-KiB space composed of the L4_WKUP interconnect configuration registers and the module registers.

Table 2-4 describes the mapping of the registers for the L4_WKUP interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_WKUP interconnect. All other accesses are internal to the L4_WKUP interconnect.

Table 2-4. L4_WKUP Memory Map

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
L4_WKUP	L4_WKUP_AP	0x4AE0_0000	0x4AE0_07FF	2 KiB	Address protection
	L4_WKUP_LA	0x4AE0_0800	0x4AE0_0FFF	2 KiB	Link agent
	L4_WKUP_IA_IP0	0x4AE0_1000	0x4AE0_1FFF	4 KiB	Initiator port
Reserved	Reserved	0x4AE0_2000	0x4AE0_3FFF	8 KiB	Reserved

Table 2-4. L4_WKUP Memory Map (continued)

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
COUNTER_32K	TP_COUNTER_32K_TARG	0x4AE0_4000	0x4AE0_4FFF	4 KiB	Module target port
	TA_COUNTER_32K_TARG	0x4AE0_5000	0x4AE0_5FFF	4 KiB	L4 target agent
PRM	TP_PRM_TARG	0x4AE0_6000	0x4AE0_7FFF	8 KiB	Module target port
	TA_PRM_TARG	0x4AE0_8000	0x4AE0_8FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE0_9000	0x4AE0_BFFF	12 KiB	Reserved
CTRL_MODULE_WKUP	TP_CTRL_MODULE_WKUP_TARG	0x4AE0_C000	0x4AE0_CFFF	4 KiB	Module target port
	TA_CTRL_MODULE_WKUP_TARG	0x4AE0_D000	0x4AE0_DFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE0_E000	0x4AE0_FFFF	8 KiB	Reserved
GPIO1	TP_GPIO1_TARG	0x4AE1_0000	0x4AE1_0FFF	4 KiB	Module target port
	TP_GPIO1_TARG	0x4AE1_1000	0x4AE1_1FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE1_2000	0x4AE1_3FFF	8 KiB	Reserved
WD_TIMER2	TP_WD_TIMER2_TARG	0x4AE1_4000	0x4AE1_4FFF	4 KiB	Module target port
	TA_WD_TIMER2_TARG	0x4AE1_5000	0x4AE1_5FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE1_6000	0x4AE1_7FFF	8 KiB	Reserved
TIMER1	TP_TIMER1_TARG	0x4AE1_8000	0x4AE1_8FFF	4 KiB	Module target port
	TA_TIMER1_TARG	0x4AE1_9000	0x4AE1_9FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE1_A000	0x4AE1_BFFF	8 KiB	Reserved
KBD	TP_KBD_TARG	0x4AE1_C000	0x4AE1_CFFF	4 KiB	Module target port
	TA_KBD_TARG	0x4AE1_D000	0x4AE1_DFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE1_E000	0x4AE1_FFFF	8 KiB	Reserved
TIMER12	TP_TIMER12_TARG	0x4AE2 0000	0x4AE2 0FFF	4 KiB	Module target port
	TA_TIMER12_TARG	0x4AE2 1000	0x4AE2 1FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE2_2000	0x4AE2_5FFF	16 KiB	Reserved
SAR_RAM	TP_SAR_RAM_SPACE1_TARG	0x4AE2_6000	0x4AE2_6FFF	4 KiB	Module target port
Reserved	Reserved	0x4AE2_7000	0x4AE2_9FFF	12 KiB	Reserved
SAR_RAM	TP_SAR_RAM_TARG	0x4AE2_A000	0x4AE2_AFFF	4 KiB	L4 target agent
UART10	TP_UART10_TARG	0x4AE2_B000	0x4AE2_BFFF	4 KiB	Module target port
	TA_UART10_TARG	0x4AE2_C000	0x4AE2_CFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE2_D000	0x4AE3_BFFF	60 KiB	Reserved
DCAN1	TP_DCAN1_TARG	0x4AE3_C000	0x4AE3_DFFF	8 KiB	Module target port
	TA_DCAN1_TARG	0x4AE3_E000	0x4AE3_EFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4AE3_F000	0x4AFF_FFFF	1796 KiB	Reserved

NOTE: 8- and 16-bit peripherals are aligned on 32-bit address boundaries.

2.3.3 L4_PER Memory Map

The L4_PER interconnect has three memory spaces:

- L4_PER1 memory space (Table 2-5)
- L4_PER2 memory space (Table 2-6)
- L4_PER3 memory space (Table 2-7)

The L4_PER interconnects are composed of the L4_PER interconnect confguration registers and the module registers.

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_PER interconnects. All other accesses are internal to the L4_PER interconnects.

2.3.3.1 L4_PER1 Memory Map

Table 2-5 describes the mapping of the registers for the L4_PER1 interconnect.

Table 2-5. L4_PER1 Memory Map

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
L4_PER1 interconnect	L4_PER1_AP	0x4800_0000	0x4800_07FF	2KiB	Address protection
	L4_PER1_LA	0x4800_0800	0x4800_0FFF	2KiB	Link agent
	L4_PER1_IA_IP0	0x4800_1000	0x4800_13FF	1KiB	Initiator port 0
	L4_PER1_IA_IP1	0x4800_1400	0x4800_17FF	1KiB	Initiator port 1
	L4_PER1_IA_IP2	0x4800_1800	0x4800_1BFF	1KiB	Initiator port 2
	L4_PER1_IA_IP3	0x4800_1C00	0x4800_1FFF	1KiB	Initiator port 3
Reserved	Reserved	0x4800_2000	0x4801_FFFF	121KiB	Reserved
UART3	TP_UART3_TARG	0x4802_0000	0x4802_0FFF	4KiB	Module target port
	TA_UART3_TARG	0x4802_1000	0x4802_1FFF	4KiB	L4 target agent
Reserved	Reserved	0x4802_2000	0x4803_1FFF	64KiB	Reserved
TIMER2	TP_TIMER2_TARG	0x4803_2000	0x4803_2FFF	4KiB	Module target port
	TA_TIMER2_TARG	0x4803_3000	0x4803_3FFF	4KiB	L4 target agent
TIMER3	TP_TIMER3_TARG	0x4803_4000	0x4803_4FFF	4KiB	Module target port
	TA_TIMER3_TARG	0x4803_5000	0x4803_5FFF	4KiB	L4 target agent
TIMER4	TP_TIMER4_TARG	0x4803_6000	0x4803_6FFF	4KiB	Module target port
	TA_TIMER4_TARG	0x4803_7000	0x4803_7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4803_8000	0x4803_DFFF	24KiB	Reserved
TIMER9	TP_TIMER9_TARG	0x4803_E000	0x4803_EFFF	4KiB	Module target port
	TA_TIMER9_TARG	0x4803_F000	0x4803_FFFF	4KiB	L4 target agent
Reserved	Reserved	0x4804_0000	0x4805_0FFF	68KiB	Reserved
GPIO7	TP_GPIO7_TARG	0x4805_1000	0x4805_1FFF	4KiB	Module target port
	TA_GPIO7_TARG	0x4805_2000	0x4805_2FFF	4KiB	L4 target agent
GPIO8	TP_GPIO8_TARG	0x4805_3000	0x4805_3FFF	4KiB	Module target port
	TA_GPIO8_TARG	0x4805_4000	0x4805_4FFF	4KiB	L4 target agent
GPIO2	TP_GPIO2_TARG	0x4805_5000	0x4805_5FFF	4KiB	Module target port
	TA_GPIO2_TARG	0x4805_6000	0x4805_6FFF	4KiB	L4 target agent
GPIO3	TP_GPIO3_TARG	0x4805_7000	0x4805_7FFF	4KiB	Module target port
	TA_GPIO3_TARG	0x4805_8000	0x4805_8FFF	4KiB	L4 target agent
GPIO4	TP_GPIO4_TARG	0x4805_9000	0x4805_9FFF	4KiB	Module target port
	TA_GPIO4_TARG	0x4805_A000	0x4805_AFFF	4KiB	L4 target agent

Table 2-5. L4_PER1 Memory Map (continued)

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
GPIO5	TP_GPIO5_TARG	0x4805_B000	0x4805_BFFF	4KiB	Module target port
	TA_GPIO5_TARG	0x4805_C000	0x4805_CFFF	4KiB	L4 target agent
GPIO6	TP_GPIO6_TARG	0x4805_D000	0x4805_DFFF	4KiB	Module target port
	TA_GPIO6_TARG	0x4805_E000	0x4805_EFFF	4KiB	L4 target agent
Reserved	Reserved	0x4805_F000	0x4805_FFFF	4KiB	Reserved
I2C3	TP_I2C3_TARG	0x4806_0000	0x4806_0FFF	4KiB	Module target port
	TA_I2C3_TARG	0x4806_1000	0x4806_1FFF	4KiB	L4 target agent
Reserved	Reserved	0x4806_2000	0x4806_5FFF	16KiB	L4 interconnect target agent
UART5	TP_UART5_TARG	0x4806_6000	0x4806_6FFF	4KiB	Module target port
	TA_UART5_TARG	0x4806_7000	0x4806_7FFF	4KiB	L4 target agent
UART6	TP_UART6_TARG	0x4806_8000	0x4806_8FFF	4KiB	Module target port
	TA_UART6_TARG	0x4806_9000	0x4806_9FFF	4KiB	L4 target agent
UART1	TP_UART1_TARG	0x4806_A000	0x4806_AFFF	4KiB	Module target port
	TA_UART1_TARG	0x4806_B000	0x4806_BFFF	4KiB	L4 target agent
UART2	TP_UART2_TARG	0x4806_C000	0x4806_CFFF	4KiB	Module target port
	TA_UART2_TARG	0x4806_D000	0x4806_DFFF	4KiB	L4 target agent
UART4	TP_UART4_TARG	0x4806_E000	0x4806_EFFF	4KiB	Module target port
	TA_UART4_TARG	0x4806_F000	0x4806_FFFF	4KiB	L4 target agent
I2C1	TP_I2C1_TARG	0x4807_0000	0x4807_0FFF	4KiB	Module target port
	TA_I2C1_TARG	0x4807_1000	0x4807_1FFF	4KiB	L4 target agent
I2C2	TP_I2C2_TARG	0x4807_2000	0x4807_2FFF	4KiB	Module target port
	TA_I2C2_TARG	0x4807_3000	0x4807_3FFF	4KiB	L4 target agent
Reserved	Reserved	0x4807_4000	0x4807_7FFF	16KiB	Reserved
ELM	TP_ELM_TARG	0x4807_8000	0x4807_8FFF	4KiB	Module target port
	TA_ELM_TARG	0x4807_9000	0x4807_9FFF	4KiB	L4 target agent
I2C4	TP_I2C4_TARG	0x4807_A000	0x4807_AFFF	4KiB	Module target port
	TA_I2C4_TARG	0x4807_B000	0x4807_BFFF	4KiB	L4 target agent
I2C5	TP_I2C5_TARG	0x4807_C000	0x4807_CFFF	4KiB	Module target port
	TA_I2C5_TARG	0x4807_D000	0x4807_DFFF	4KiB	L4 target agent
Reserved	Reserved	0x4807_E000	0x4808_5FFF	32KiB	Reserved
TIMER10	TP_TIMER10_TARG	0x4808_6000	0x4808_6FFF	4KiB	Module target port
	TA_TIMER10_TARG	0x4808_7000	0x4808_7FFF	4KiB	L4 target agent
TIMER11	TP_TIMER11_TARG	0x4808_8000	0x4808_8FFF	4KiB	Module target port
	TA_TIMER11_TARG	0x4808_9000	0x4808_9FFF	4KiB	L4 target agent
Reserved	Reserved	0x4808_A000	0x4809_7FFF	56KiB	Reserved
McSPI1	TP_MCSPI1_TARG	0x4809_8000	0x4809_8FFF	4KiB	Module target port
	TA_MCSPI1_TARG	0x4809_9000	0x4809_9FFF	4KiB	L4 target agent
McSPI2	TP_MCSPI2_TARG	0x4809_A000	0x4809_AFFF	4KiB	Module target port
	TA_MCSPI2_TARG	0x4809_B000	0x4809_BFFF	4KiB	L4 target agent
MMC1	TP_MMC1_TARG	0x4809_C000	0x4809_CFFF	4KiB	Module target port
	TA_MMC1_TARG	0x4809_D000	0x4809_DFFF	4KiB	L4 target agent
Reserved	Reserved	0x4809_E000	0x480A_CFFF	60KiB	Reserved
MMC3	TP_MMC3_TARG	0x480A_D000	0x480A_DFFF	4KiB	Module target port
	TA_MMC3_TARG	0x480A_E000	0x480A_EFFF	4KiB	L4 target agent
Reserved	Reserved	0x480A_F000	0x480B_1FFF	12KiB	Reserved
HDQ1W	TP_HDQ1W_TARG	0x480B_2000	0x480B_2FFF	4KiB	Module target port
	TA_HDQ1W_TARG	0x480B_3000	0x480B_3FFF	4KiB	L4 target agent

Table 2-5. L4_PER1 Memory Map (continued)

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
MMC2	TP_MMC2_TARG	0x480B_4000	0x480B_4FFF	4KiB	Module target port
	TA_MMC2_TARG	0x480B_5000	0x480B_5FFF	4KiB	L4 target agent
Reserved	Reserved	0x480B_6000	0x480B_7FFF	8KiB	Reserved
McSPI3	TP_MCSPI3_TARG	0x480B_8000	0x480B_8FFF	4KiB	Module target port
	TA_MCSPI3_TARG	0x480B_9000	0x480B_9FFF	4KiB	L4 target agent
McSPI4	TP_MCSPI4_TARG	0x480B_A000	0x480B_AFFF	4KiB	Module target port
	TA_MCSPI4_TARG	0x480B_B000	0x480B_BFFF	4KiB	L4 target agent
Reserved	Reserved	0x480B_C000	0x480D_0FFF	84KiB	Reserved
MMC4	TP_MMC4_TARG	0x480D_1000	0x480D_1FFF	4KiB	Module target port
	TA_MMC4_TARG	0x480D_2000	0x480D_2FFF	4KiB	L4 target agent
Reserved	Reserved	0x480D_3000	0x483F_FFFF	3252KiB	Reserved

2.3.3.2 L4_PER2 Memory Map

Table 2-6 describes the mapping of the register for the L4_PER2 interconnect.

Table 2-6. L4_PER2 Memory Map

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
L4_PER2 interconnect	L4_PER2_AP	0x4840_0000	0x4840_07FF	2KiB	Address protection
	L4_PER2_LA	0x4840_0800	0x4840_0FFF	2KiB	Link Agent
	L4_PER2_IA_IP0	0x4840_1000	0x4840_13FF	1KiB	Initiator Port 0
	L4_PER2_IA_IP1	0x4840_1400	0x4840_17FF	1KiB	Initiator Port 1
	L4_PER2_IA_IP2	0x4840_1800	0x4840_1BFF	1KiB	Initiator Port 2
Reserved	Reserved	0x4840_1C00	0x4841_FFFF	121KiB	Reserved
UART7	TP_UART7_TARG	0x4842_0000	0x4842_0FFF	4KiB	Module target port
	TA_UART7_TARG	0x4842_1000	0x4842_1FFF	4KiB	L4 interconnect target agent
UART8	TP_UART8_TARG	0x4842_2000	0x4842_2FFF	4KiB	Module target port
	TA_UART8_TARG	0x4842_3000	0x4842_3FFF	4KiB	L4 interconnect target agent
UART9	TP_UART9_TARG	0x4842_4000	0x4842_4FFF	4KiB	Module target port
	TA_UART9_TARG	0x4842_5000	0x4842_5FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4842_6000	0x4842_BFFF	24KiB	Reserved
MLB[(1)]	TP_MLB_TARG	0x4842_C000	0x4842_CFFF	4KiB	Module target port
	TA_MLB_TARG	0x4842_D000	0x4842_DFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4842_E000	0x4843_5FFF	32KiB	Reserved
McASP4	TP_MCASP4_DAT_TARG	0x4843_6000	0x4843_6FFF	4KiB	Module target port
	TA_MCASP4_DAT_TARG	0x4843_7000	0x4843_7FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4843_8000	0x4843_9FFF	8KiB	Reserved
McASP5	TP_MCASP5_DAT_TARG	0x4843_A000	0x4843_AFFF	4KiB	Module target port
	TA_MCASP5_DAT_TARG	0x4843_B000	0x4843_BFFF	4KiB	L4 interconnect target agent
ATL[(1)]	TP_ATL_TARG	0x4843_C000	0x4843_CFFF	4KiB	Module target port
	TA_ATL_TARG	0x4843_D000	0x4843_DFFF	4KiB	L4 interconnect target agent
PWMSS1	TP_PWMSS1_TARG	0x4843_E000	0x4843_EFFF	4KiB	Module target port
	TA_PWMSS1_TARG	0x4843_F000	0x4843_FFFF	4KiB	L4 interconnect target agent
PWMSS2	TP_PWMSS2_TARG	0x4844_0000	0x4844_0FFF	4KiB	Module target port
	TA_PWMSS2_TARG	0x4844_1000	0x4844_1FFF	4KiB	L4 interconnect target agent

(1) ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 2-6. L4_PER2 Memory Map (continued)

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
PWMSS3	TP_PWMSS3_TARG	0x4844_2000	0x4844_2FFF	4KiB	Module target port
	TA_PWMSS3_TARG	0x4844_3000	0x4844_3FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4844_4000	0x4844_BFFF	8KiB	Reserved
VCP1[(1)]	TP_VCP1_CFG_TARG	0x4844_6000	0x4844_6FFF	4KiB	Module target port
	TA_VCP1_CFG_TARG	0x4844_7000	0x4844_7FFF	4KiB	L4 interconnect target agent
VCP2[(1)]	TP_VCP2_CFG_TARG	0x4844_8000	0x4844_8FFF	4KiB	Module target port
	TA_VCP2_CFG_TARG	0x4844_9000	0x4844_9FFF	4KiB	L4 interconnect target agent
IODELAYCONFIG	TP_DELAYLINE_TARG	0x4844_A000	0x4844_AFFF	4KiB	Module target port
Reserved	Reserved	0x4844_B000	0x4844_BFFF	4KiB	Reserved
McASP6	TP_MCASP6_DAT_TARG	0x4844_C000	0x4844_CFFF	4KiB	Module target port
	TA_MCASP6_DAT_TARG	0x4844_D000	0x4844_DFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4844_E000	0x4844_FFFF	8KiB	Reserved
McASP7	TP_MCASP7_DAT_TARG	0x4845_0000	0x4845_0FFF	4KiB	Module target port
	TA_MCASP7_DAT_TARG	0x4845_1000	0x4845_1FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4845_2000	0x4845_3FFF	8KiB	Reserved
McASP8	TP_MCASP8_DAT_TARG	0x4845_4000	0x4845_4FFF	4KiB	Module target port
	TA_MCASP8_DAT_TARG	0x4845_5000	0x4845_5FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4845_6000	0x4845_FFFF	40KiB	Reserved
McASP1	TP_MCASP1_CFG_TARG	0x4846_0000	0x4846_1FFF	8KiB	Module target port
	TA_MCASP1_CFG_TARG	0x4846_2000	0x4846_2FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4846_3000	0x4846_3FFF	4KiB	Reserved
McASP2	TP_MCASP2_CFG_TARG	0x4846_4000	0x4846_5FFF	8KiB	Module target port
	TA_MCASP2_CFG_TARG	0x4846_6000	0x4846_6FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4846_7000	0x4846_7FFF	4KiB	Reserved
McASP3	TP_MCASP3_CFG_TARG	0x4846_8000	0x4846_9FFF	8KiB	Module target port
	TA_MCASP3_CFG_TARG	0x4846_A000	0x4846_AFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4846_B000	0x4846_BFFF	4KiB	Reserved
McASP4	TP_MCASP4_CFG_TARG	0x4846_C000	0x4846_DFFF	8KiB	Module target port
	TA_MCASP4_CFG_TARG	0x4846_E000	0x4846_EFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4846_F000	0x4846_FFFF	4KiB	Reserved
McASP5	TP_MCASP5_CFG_TARG	0x4847_0000	0x4847_1FFF	8KiB	Module target port
	TA_MCASP5_CFG_TARG	0x4847_2000	0x4847_2FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4847_3000	0x4847_3FFF	4KiB	Reserved
McASP6	TP_MCASP6_CFG_TARG	0x4847_4000	0x4847_5FFF	8KiB	Module target port
	TA_MCASP6_CFG_TARG	0x4847_6000	0x4847_6FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4847_7000	0x4847_7FFF	4KiB	Reserved
McASP7	TP_MCASP7_CFG_TARG	0x4847_8000	0x4847_9FFF	8KiB	Module target port
	TA_MCASP7_CFG_TARG	0x4847_A000	0x4847_AFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4847_B000	0x4847_BFFF	4KiB	Reserved
McASP8	TP_MCASP8_CFG_TARG	0x4847_C000	0x4847_DFFF	8KiB	Module target port
	TA_MCASP8_CFG_TARG	0x4847_E000	0x4847_EFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4847_F000	0x4847_FFFF	4KiB	Reserved
DCAN2	TP_DCAN2_TARG	0x4848_0000	0x4848_1FFF	8KiB	Module target port
	TA_DCAN2_TARG	0x4848_2000	0x4848_2FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4848_3000	0x4848_3FFF	4KiB	Reserved

Table 2-6. L4_PER2 Memory Map (continued)

Module name	Region name	Start_address (hex)	End_address (hex)	Size	Description
GMAC_SW	TP_GMAC_SW_TARG	0x4848_4000	0x4848_7FFF	16KiB	Module target port
	TA_GMAC_SW_TARG	0x4848_8000	0x4848_8FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4848_9000	0x487F_FFFF	3548KiB	Reserved

2.3.3.3 L4_PER3 Memory Map

Table 2-7 describes the mapping of the register for the L4_PER3 interconnect.

Table 2-7. L4_PER3 Memory Map

Module name	Region name tag	Start_address (hex)	End_address (hex)	Size	Description
L4_PER3 interconnect	L4_PER3_AP	0x4880_0000	0x4880_07FF	2KiB	Address protection
	L4_PER3_LA	0x4880_0800	0x4880_0FFF	2KiB	Link agent
	L4_PER3_IA_IP0	0x4880_1000	0x4880_13FF	1KiB	Initiator Port 0
	L4_PER3_IA_IP1	0x4880_1400	0x4880_17FF	1KiB	Initiator Port 1
	L4_PER3_IA_IP2	0x4880_1800	0x4880_1BFF	1KiB	Initiator Port 2
Reserved	Reserved	0x4880_1C00	0x4880_1FFF	1KiB	Reserved
MAILBOX13	TP_MAILBOX13_TARG	0x4880_2000	0x4880_2FFF	4KiB	Module target port
	TA_MAILBOX13_TARG	0x4880_3000	0x4880_3FFF	4KiB	L4 interconnect target agent
OCMC_RAM1	TP_OCMC_RAM1_CFG_TARG	0x4880_4000	0x4880_4FFF	4KiB	Module target port
	TA_OCMC_RAM1_CFG_TARG	0x4880_5000	0x4880_5FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4880_6000	0x4880_9FFF	16KiB	Reserved
OCMC_RAM2	TP_OCMC_RAM2_CFG_TARG	0x4880_A000	0x4880_AFFF	4KiB	Module target port
	TA_OCMC_RAM2_CFG_TARG	0x4880_B000	0x4880_BFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4880_C000	0x4880_FFFF	16KiB	Reserved
OCMC_RAM3	TP_OCMC_RAM3_CFG_TARG	0x4881_0000	0x4881_0FFF	4KiB	Module target port
	TA_OCMC_RAM3_CFG_TARG	0x4881_1000	0x4881_1FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4881_2000	0x4881_BFFF	40KiB	Reserved
MMU1	TP_MMU1_TARG	0x4881_C000	0x4881_CFFF	4KiB	Module target port
	TA_MMU1_TARG	0x4881_D000	0x4881_DFFF	4KiB	L4 interconnect target agent
MMU2	TP_MMU2_TARG	0x4881_E000	0x4881_EFFF	4KiB	Module target port
	TA_MMU2_TARG	0x4881_F000	0x4881_FFFF	4KiB	L4 interconnect target agent
TIMER5	TP_TIMER5_TARG	0x4882_0000	0x4882_0FFF	4KiB	Module target port
	TA_TIMER5_TARG	0x4882_1000	0x4882_1FFF	4KiB	L4 interconnect target agent
TIMER6	TP_TIMER6_TARG	0x4882_2000	0x4882_2FFF	4KiB	Module target port
	TA_TIMER6_TARG	0x4882_3000	0x4882_3FFF	4KiB	L4 interconnect target agent
TIMER7	TP_TIMER7_TARG	0x4882_4000	0x4882_4FFF	4KiB	Module target port
	TA_TIMER7_TARG	0x4882_5000	0x4882_5FFF	4KiB	L4 interconnect target agent
TIMER8	TP_TIMER8_TARG	0x4882_6000	0x4882_6FFF	4KiB	Module target port
	TA_TIMER8_TARG	0x4882_7000	0x4882_7FFF	4KiB	L4 interconnect target agent
TIMER13	TP_TIMER13_TARG	0x4882_8000	0x4882_8FFF	4KiB	Module target port
	TA_TIMER13_TARG	0x4882_9000	0x4882_9FFF	4KiB	L4 interconnect target agent

Table 2-7. L4_PER3 Memory Map (continued)

Module name	Region name tag	Start_address (hex)	End_address (hex)	Size	Description
TIMER14	TP_TIMER14_TARG	0x4882_A000	0x4882_AFFF	4KiB	Module target port
	TA_TIMER14_TARG	0x4882_B000	0x4882_BFFF	4KiB	L4 interconnect target agent
TIMER15	TP_TIMER15_TARG	0x4882_C000	0x4882_CFFF	4KiB	Module target port
	TA_TIMER15_TARG	0x4882_D000	0x4882_DFFF	4KiB	L4 interconnect target agent
TIMER16	TP_TIMER16_TARG	0x4882_E000	0x4882_EFFF	4KiB	Module target port
	TA_TIMER16_TARG	0x4882_F000	0x4882_FFFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4883_0000	0x4883_7FFF	32KiB	Reserved
RTC_SS	TP_RTC_SS_TARG	0x4883_8000	0x4883_8FFF	4KiB	Module target port
	TA_RTC_SS_TARG	0x4883_9000	0x4883_9FFF	4KiB	L4 interconnect target agent
MAILBOX2	TP_MAILBOX2_TARG	0x4883_A000	0x4883_AFFF	4KiB	Module target port
	TA_MAILBOX2_TARG	0x4883_B000	0x4883_BFFF	4KiB	L4 interconnect target agent
MAILBOX3	TP_MAILBOX3_TARG	0x4883_C000	0x4883_CFFF	4KiB	Module target port
	TA_MAILBOX3_TARG	0x4883_D000	0x4883_DFFF	4KiB	L4 interconnect target agent
MAILBOX4	TP_MAILBOX4_TARG	0x4883_E000	0x4883_EFFF	4KiB	Module target port
	TA_MAILBOX4_TARG	0x4883_F000	0x4883_FFFF	4KiB	L4 interconnect target agent
MAILBOX5	TP_MAILBOX5_TARG	0x4884_0000	0x4884_0FFF	4KiB	Module target port
	TA_MAILBOX5_TARG	0x4884_1000	0x4884_1FFF	4KiB	L4 interconnect target agent
MAILBOX6	TP_MAILBOX6_TARG	0x4884_2000	0x4884_2FFF	4KiB	Module target port
	TA_MAILBOX6_TARG	0x4884_3000	0x4884_3FFF	4KiB	L4 interconnect target agent
MAILBOX7	TP_MAILBOX7_TARG	0x4884_4000	0x4884_4FFF	4KiB	Module target port
	TA_MAILBOX7_TARG	0x4884_5000	0x4884_5FFF	4KiB	L4 interconnect target agent
MAILBOX8	TP_MAILBOX8_TARG	0x4884_6000	0x4884_6FFF	4KiB	Module target port
	TA_MAILBOX8_TARG	0x4884_7000	0x4884_7FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4884_8000	0x4885_DFFF	88KiB	Reserved
MAILBOX9	TP_MAILBOX9_TARG	0x4885_E000	0x4885_EFFF	4KiB	Module target port
	TA_MAILBOX9_TARG	0x4885_F000	0x4885_FFFF	4KiB	L4 interconnect target agent
MAILBOX10	TP_MAILBOX10_TARG	0x4886_0000	0x4886_0FFF	4KiB	Module target port
	TA_MAILBOX10_TARG	0x4886_1000	0x4886_1FFF	4KiB	L4 interconnect target agent
MAILBOX11	TP_MAILBOX11_TARG	0x4886_2000	0x4886_2FFF	4KiB	Module target port
	TA_MAILBOX11_TARG	0x4886_3000	0x4886_3FFF	4KiB	L4 interconnect target agent
MAILBOX12	TP_MAILBOX12_TARG	0x4886_4000	0x4886_4FFF	4KiB	Module target port
	TA_MAILBOX12_TARG	0x4886_5000	0x4886_5FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4886_6000	0x4887_FFFF	104KiB	Reserved
USB1	TP_USB1_CFG_TARG	0x4888_0000	0x4889_FFFF	128KiB	Module target port
	TA_USB1_CFG_TARG	0x488A_0000	0x488A_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x488A_1000	0x488B_FFFF	124KiB	Reserved
USB2	TP_USB2_CFG_TARG	0x488C_0000	0x488D_FFFF	128KiB	Module target port
	TA_USB2_CFG_TARG	0x488E_0000	0x488E_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x488E_1000	0x488F_FFFF	124KiB	Reserved
USB3[(1)]	TP_USB3_CFG_TARG	0x4890_0000	0x4891_FFFF	128KiB	Module target port
	TA_USB3_CFG_TARG	0x4892_0000	0x4892_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4892_1000	0x4893_FFFF	124KiB	Reserved
USB4[(1)]	TP_USB4_CFG_TARG	0x4894_0000	0x4895_FFFF	128KiB	Module target port
	TA_USB4_CFG_TARG	0x4896_0000	0x4896_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4896_1000	0x4896_FFFF	60KiB	Reserved

(1) ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

Table 2-7. L4_PER3 Memory Map (continued)

Module name	Region name tag	Start_address (hex)	End_address (hex)	Size	Description
VIP1	TP_VIP1_TARG	0x4897_0000	0x4897_FFFF	64KiB	Module target port
	TA_VIP1_TARG	0x4898_0000	0x4898_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x4898_1000	0x4898_FFFF	60KiB	Reserved
VIP2	TP_VIP2_TARG	0x4899_0000	0x4899_FFFF	64KiB	Module target port
	TA_VIP2_TARG	0x489A_0000	0x489A_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x489A_1000	0x489A_FFFF	60KiB	Reserved
VIP3	TP_VIP3_TARG	0x489B_0000	0x489B_FFFF	64KiB	Module target port
	TA_VIP3_TARG	0x489C_0000	0x489C_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x489C_1000	0x489C_FFFF	60KiB	Reserved
VPE	TP_VPE_TARG	0x489D_0000	0x489D_FFFF	64KiB	Module target port
	TA_VPE_TARG	0x489E_0000	0x489E_0FFF	4KiB	L4 interconnect target agent
Reserved	Reserved	0x489E_1000	0x48FF_FFFF	6268KiB	Reserved

2.4 MPU Memory Map

Table 2-8 describes the MPU memory mapping.

Table 2-8. MPU Memory Map

Quarter	Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
Q0	L3_MAIN map	0x00_0000_0000	0x00_3FFF_FFFF	1GiB	See Table 2-1
Q1	Reserved	0x00_4000_0000	0x00_4003_7FFF	224KiB	Reserved
	MPU_ROM(1)	0x00_4003_8000	0x00_4004_3FFF	48KiB	MPU internal boot ROM: 32bit Ex(2)/R
	Reserved	0x00_4004_4000	0x00_402F_FFFF	2800KiB	Reserved
	L3_MAIN map	0x00_4030_0000	0x00_46FF_FFFF	114MiB	See Table 2-1
	MPU_CS_STM	0x00_4700_0000	0x00_47FF_FFFF	16MiB	MPU_CS_STM config registers
	L3_MAIN map	0x00_4800_0000	0x00_481F_FFFF	2MiB	See Table 2-1
	Reserved	0x00_4820_0000	0x00_4820_FFFF	64KiB	Reserved
	MPU_INTC	0x00_4821_0000	0x00_4821_7FFF	32KiB	MPU_INTC config registers
	Reserved	0x00_4821_8000	0x00_4824_2FFF	172KiB	Reserved
	MPU_PRCM	0x00_4824_3000	0x00_4824_3FFF	4KiB	MPU_PRCM config registers
	Reserved	0x00_4824_4000	0x00_4828_0FFF	242KiB	Reserved
	MPU_CMU	0x00_4829_0000	0x00_4829_FFFF	64KiB	MPU_CMU config registers
	MPU_AXI2OCP	0x00_482A_0000	0x00_482A_EFFF	60KiB	MPU_AXI2OCP config registers
	MPU_MA	0x00_482A_F000	0x00_482A_FFFF	4KiB	MPU_MA config registers
	Reserved	0x00_482B_0000	0x00_483F_FFFF	1344KiB	Reserved
	L3_MAIN map	0x00_4840_0000	0x00_7FFF_FFFF	892MiB	See Table 2-1
Q2, Q3	L3_MAIN map	0x00_8000_0000	0x00_FFFF_FFFF	2GiB	See Table 2-1
	8 GiB(3) of SDRAM virtualization when interleaving(4) is disabled.				
Q8	EMIF1_SDRAM_CS0	0x02_0000_0000	0x02_3FFF_FFFF	1GiB	EMIF1 CS0: Access to DDR
Q9	Reserved	0x02_4000_0000	0x02_7FFF_FFFF	1GiB	Reserved
Q10(5)	EMIF1_SDRAM_CS0	0x02_8000_0000	0x02_BFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR. Alias of Q2 (see Table 2-1).
	EMIF2_SDRAM_CS0	0x02_8000_0000	0x02_BFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR. Alias of Q2 (see Table 2-1).
Q11(5)	EMIF1_SDRAM_CS0	0x02_C000_0000	0x02_FFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR. Alias of Q3 (see Table 2-1).
	EMIF2_SDRAM_CS0	0x02_C000_0000	0x02_FFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR. Alias of Q3 (see Table 2-1).
Q12	Reserved	0x03_0000_0000	0x03_3FFF_FFFF	1GiB	Reserved
Q13	Reserved	0x03_4000_0000	0x03_7FFF_FFFF	1GiB	Reserved
Q14	Reserved	0x03_8000_0000	0x03_BFFF_FFFF	1GiB	Reserved
Q15	EMIF2_SDRAM_CS0	0x03_C000_0000	0x03_FFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR
	8 GiB(3) of SDRAM virtualization when interleaving(4) is enabled.				
Q8	EMIF1_SDRAM_CS0	0x02_0000_0000	0x02_3FFF_FFFF	1GiB(6)	EMIF1 CS0: Access to DDR
	EMIF2_SDRAM_CS0	0x02_0000_0000	0x02_3FFF_FFFF	1GiB(6)	EMIF2 CS0: Access to DDR

(1) Boot space location depends on the external sys_boot [5:0] pins.

(2) Ex = Executable

(3) Only 4 GiB are physically available within this 8-GiB address range.

(4) Interleaving is configurable with one setting in the MPU memory adapter (MPU_MA) for all 8 GiB of SDRAM high memory. For more information about interleaving, see Section 4.3.4, *Memory Adapter*.

(5) As Q10 is alias of Q2, depending on the DMM_LISA_MAP_i settings the Q10 address space can be configured in the following ways:
- Allocated only to EMIF1_SDRAM_CS0
- Allocated only to EMIF2_SDRAM_CS0
- Shared between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0 but not interleaved
- Interleaved between EMIF1_SDRAM_CS0 and EMIF2_SDRAM_CS0

The same applies to the Q11 address space, as it is alias of Q3.

(6) Because of the fixed MPU-to-EMIF address mapping with high-order interleaving enabled only 512MiB of this address space are used by EMIF1_SDRAM_CS0. The other 512MiB are used by EMIF2_SDRAM_CS0.

Table 2-8. MPU Memory Map (continued)

Quarter	Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
Q9	EMIF1_SDRAM_CS0	0x02_4000_0000	0x02_7FFF_FFFF	1GiB[6]	EMIF1 CS0: Access to DDR
	EMIF2_SDRAM_CS0	0x02_4000_0000	0x02_7FFF_FFFF	1GiB[6]	EMIF2 CS0: Access to DDR
Q10[5]	EMIF1_SDRAM_CS0	0x02_8000_0000	0x02_BFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR. Alias of Q2 (see Table 2-1).
	EMIF2_SDRAM_CS0	0x02_8000_0000	0x02_BFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR. Alias of Q2 (see Table 2-1).
Q11[5]	EMIF1_SDRAM_CS0	0x02_C000_0000	0x02_FFFF_FFFF	1GiB	EMIF1 CS0: Access to DDR. Alias of Q3 (see Table 2-1).
	EMIF2_SDRAM_CS0	0x02_C000_0000	0x02_FFFF_FFFF	1GiB	EMIF2 CS0: Access to DDR. Alias of Q3 (see Table 2-1).
Q12	Reserved	0x03_0000_0000	0x03_3FFF_FFFF	1GiB	Reserved
Q13	Reserved	0x03_4000_0000	0x03_7FFF_FFFF	1GiB	Reserved
Q14	Reserved	0x03_8000_0000	0x03_BFFF_FFFF	1GiB	Reserved
Q15	Reserved	0x03_C000_0000	0x03_FFFF_FFFF	1GiB	Reserved

Legend: = MPU private memory space

= Reserved memory space

2.5 IPU Memory Map

The device implements two IPU subsystems (IPU1, IPU2). For more information about IPU, see Chapter 7.

NOTE: IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing.

Table 2-9 describes the IPU memory mapping.

Table 2-9. IPU Memory Map

Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
IPU_BOOT_SPACE(1)	0x0000_0000	0x0000_3FFF	16KiB	IPU boot space
L3_MAIN map	0x0000_0000	0x1FFF_FFFF	512KiB	See Table 2-1
IPU_BITBAND_REGION1	0x2000_0000	0x200F_FFFF	1MiB	IPU bit-band region 1
Reserved	0x2010_0000	0x21FF_FFFF	31MiB	Reserved
IPU_BITBAND_ALIAS1	0x2200_0000	0x23FF_FFFF	32MiB	IPU bit-band alias 1
L3_MAIN map	0x2400_0000	0x3FFF_FFFF	448MiB	See Table 2-1
IPU_BITBAND_REGION2	0x4000_0000	0x400F_FFFF	1MiB	IPU bit-band region 2
Reserved	0x4010_0000	0x402F_FFFF	2MiB	Reserved
L3_MAIN map	0x4030_0000	0x41FF_FFFF	30MiB	See Table 2-1
IPU_BITBAND_ALIAS2	0x4200_0000	0x43FF_FFFF	32MiB	IPU bit-band alias 2
L3_MAIN map	0x4400_0000	0x54FF_FFFF	285MiB	See Table 2-1
IPU_ROM(2)	0x5500_0000	0x5500_3FFF	16KiB	IPU_ROM
IPU_RAM(2)	0x5502_0000	0x5502_FFFF	64KiB	IPU_RAM
IPU_UNICACHE_MMU(2)	0x5508_0000	0x5508_0FFF	4KiB	IPU_UNICACHE_MMU config registers
IPU_WUGEN(2)	0x5508_1000	0x5508_1FFF	4KiB	IPU_WUGEN config registers
IPU_MMU(2)	0x5508_2000	0x5508_2FFF	4KiB	IPU_MMU config registers
Reserved	0x5508_3000	0x55FF_FFFF	16MiB	Reserved
L3_MAIN map	0x5600_0000	0xDFFF_FFFF	2,3GiB	See Table 2-1
Reserved	0xE000_0000	0xE000_0FFF	4KiB	Reserved
IPU_C0_DWT	0xE000_1000	0xE000_1FFF	4KiB	IPU_C0_DWT config registers
IPU_C0_FPB	0xE000_2000	0xE000_2FFF	4KiB	IPU_C0_FPB config registers
IPU_C0_INTC	0xE000_E000	0xE000_EFFF	4KiB	IPU_C0_INTC config registers
IPU_C0_ICECRUSHER	0xE004_2000	0xE004_2FFF	4KiB	IPU_C0_ICECRUSHER config registers
IPU_C0_RW_TABLE	0xE00F_E000	0xE00F_EFFF	4KiB	IPU_C0 RW table
IPU_C0_ROM_TABLE	0xE00F_F000	0xE00F_FFFF	4KiB	IPU_C0 ROM table
IPU_C1_DWT	0xE000_1000	0xE000_1FFF	4KiB	IPU_C1_DWT config registers
IPU_C1_FPB	0xE000_2000	0xE000_2FFF	4KiB	IPU_C1_FPB config registers
IPU_C1_INTC	0xE000_E000	0xE000_EFFF	4KiB	IPU_C1_INTC config registers
IPU_C1_ICECRUSHER	0xE004_2000	0xE004_2FFF	4KiB	IPU_C1_ICECRUSHER config registers
IPU_C1_RW_TABLE	0xE00F_E000	0xE00F_EFFF	4KiB	IPU_C1 RW table
IPU_C1_ROM_TABLE	0xE00F_F000	0xE00F_FFFF	4KiB	IPU_C1 ROM table
L3_MAIN map	0xE010_0000	0xFFFF_FFFF	511MiB	See Table 2-1

Legend:		
		= IPU private memory space
		= Reserved memory space

(1) At reset, the MMU is loaded with page 0, which forces the L2 RAM to be address 0x0. Page 1 is loaded with the physical address of the shared cashe MMU register and WUGEN_IPU registers to the virtual address 0x4000 0000.

(2) Can also be accessed from L3_MAIN (by other initiators, such as: MPU, DSP, etc).

2.6 DSP Memory Map

The device implements two DSP subsystems (DSP1, DSP2). For more information about DSP, see Chapter 5.

Table 2-10 describes the DSP memory mapping.

Table 2-10. DSP Memory Map

Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
Reserved	0x0000_0000	0x007F_FFFF	8MiB	Reserved
DSP_L2(1)	0x0080_0000	0x0084_7FFF	288KiB	DSP L2 SRAM and cache. The L2 SRAM starts at 0x0080_0000 address.
Reserved	0x0084_8000	0x00DF_FFFF	5856KiB	Reserved
DSP_L1P(1)	0x00E0_0000	0x00E0_7FFF	32KiB	DSP L1P SRAM
Reserved	0x00E0_8000	0x00EF_FFFF	992KiB	Reserved
DSP_L1D(1)	0x00F0_0000	0x00F0_7FFF	32KiB	DSP L1D SRAM
Reserved	0x00F0_8000	0x00FF_FFFF	992KiB	Reserved
DSP_ICFG(1)	0x0100_0000	0x01BF_FFFF	12MiB	DSP internal CFG
Reserved	0x01C0_0000	0x01CF_FFFF	1MiB	Reserved
DSP_SYSTEM(1)	0x01D0_0000	0x01D0_0FFF	4KiB	DSP system registers block
DSP_MMU0CFG(1)	0x01D0_1000	0x01D0_1FFF	4KiB	DSP MMU0 configuration
DSP_MMU1CFG(1)	0x01D0_2000	0x01D0_2FFF	4KiB	DSP MMU1 configuration
DSP_FW0CFG(1)	0x01D0_3000	0x01D0_3FFF	4KiB	DSP firewall 0 config
DSP_FW1CFG(1)	0x01D0_4000	0x01D0_4FFF	4KiB	DSP firewall 1 config
DSP_EDMA_TC0(1)	0x01D0_5000	0x01D0_5FFF	4KiB	DSP EDMA transfer controller 0
DSP_EDMA_TC1(1)	0x01D0_6000	0x01D0_6FFF	4KiB	DSP EDMA transfer controller 1
DSP_NoC(1)	0x01D0_7000	0x01D0_7FFF	4KiB	DSP interconnect registers
Reserved	0x01D0_8000	0x01D0_FFFF	32KiB	Reserved
DSP_EDMA_CC(1)	0x01D1_0000	0x01D1_7FFF	32KiB	DSP EDMA channel controller
Reserved	0x01D1_8000	0x01FF_FFFF	2976KiB	Reserved
EVE1(2)	0x0200_0000	0x020F_FFFF	1MiB	EVE1 configuration space
EVE2(2)	0x0210_0000	0x021F_FFFF	1MiB	EVE2 configuration space
Reserved	0x0220_0000	0x032F_FFFF	17MiB	Reserved
EDMA_TPCC	0x0330_0000	0x033F_FFFF	1MiB	EDMA_TPCC configuration space
EDMA_TC0	0x0340_0000	0x034F_FFFF	1MiB	EDMA_TC0 configuration space
EDMA_TC1	0x0350_0000	0x035F_FFFF	1MiB	EDMA_TC1 configuration space
Reserved	0x0360_0000	0x07FF_FFFF	74MiB	Reserved
DSP_XMC_CTRL(1)	0x0800_0000	0x0800_FFFF	64KiB	DSP XMC control registers
DSP_EDI(1)	0x0801_0000	0x0801_FFFF	64KiB	DSP internal EDI translation region
L3_MAIN map	0x1400_0000	0xFFFF_FFFF	3,8GiB	See Table 2-1

Legend:		
		= DSP private memory space
		= Reserved memory space

(1) DSP subsystem internal resources. DSP accesses in ranges [0x0080_0000 – 0x01D1_7FFF] and [0x0800_0000 – 0x0801_FFFF] are performed locally within the DSP subsystem.

(2) ATL, VCP, EVE, MLB, USB3 (ULPI) and USB4 (ULPI) are not supported in this family of devices.

2.7 EVE Memory Map

NOTE: EVE is not supported in this family of devices

2.8 PRU-ICSS Memory Map

The device implements two PRU subsystems (PRU-ICSS1, PRU-ICSS2). For more information about PRU-ICSS, see Chapter 30.

Table 2-11 describes the PRU-ICSS memory mapping.

Table 2-11. PRU-ICSS Memory Map

Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
PRUSS_DATA_RAM0	0x0000_0000	0x0000_1FFF	8KiB	PRU-ICSS Data RAM0
PRUSS_DATA_RAM1	0x0000_2000	0x0000_3FFF	8KiB	PRU-ICSS Data RAM1
Reserved	0x0000_4000	0x0000_FFFF	48KiB	Reserved
PRUSS_DATA_RAM2	0x0001_0000	0x0001_FFFF	64KiB	PRU-ICSS Data RAM2 (shared) (32KiB implemented)
PRUSS_INTC	0x0002_0000	0x0002_1FFF	8KiB	PRU-ICSS INTC configuration
PRUSS_PRU0_CONTROL	0x0002_2000	0x0002_23FF	1KiB	PRU-ICSS PRU0 control
Reserved	0x0002_2400	0x0002_3FFF	7KiB	Reserved
PRUSS_PRU1_CONTROL	0x0002_4000	0x0002_43FF	1KiB	PRU-ICSS PRU1 control
Reserved	0x0002_4400	0x0002_5FFF	7KiB	Reserved
PRUSS_CFG	0x0002_6000	0x0002_7FFF	8KiB	PRU-ICSS CFG
PRUSS_UART0	0x0002_8000	0x0002_9FFF	8KiB	PRU-ICSS UART0 configuration
Reserved	0x0002_A000	0x0002_DFFF	16KiB	Reserved
PRUSS_IEP	0x0002_E000	0x0002_FFFF	8KiB	PRU-ICSS IEP configuration
PRUSS_ECAP_0	0x0003_0000	0x0003_1FFF	8KiB	PRU-ICSS ECAP configuration
PRUSS_MII_RT	0x0003_2000	0x0003_23FF	1KiB	PRU-ICSS MII_RT configuration
PRUSS_MII_MDIO	0x0003_2400	0x0003_3FFF	7KiB	PRU-ICSS MII_MDIO configuration
Reserved	0x0003_4000	0x0003_6FFF	12KiB	Reserved
Reserved	0x0003_7000	0x0003_7FFF	4KiB	Reserved
Reserved	0x0003_8000	0x0003_AFFF	12KiB	Reserved
Reserved	0x0003_B000	0x1FFF_FFFF	524MiB	Reserved
L3_MAIN map	0x2000 0000	0xFFFF FFFF	3.4GiB	See Table 2-1

Legend:		= PRU-ICSS private memory space
		= Reserved memory space

2.9 TILER View Memory Map

Table 2-12 describes the TILER view memory mapping.

Table 2-12. TILER View Memory Map

Region Name	Start_Address (hex)	End_Address (hex)	Size	Description
TILER_VIEW_0	0x01_0000_0000	0x01_1FFF_FFFF	512MiB	Natural view
TILER_VIEW_1	0x01_2000_0000	0x01_3FFF_FFFF	512MiB	0° view with vertical mirror
TILER_VIEW_2	0x01_4000_0000	0x01_5FFF_FFFF	512MiB	0° view with horizontal mirror
TILER_VIEW_3	0x01_6000_0000	0x01_7FFF_FFFF	512MiB	180° view
TILER_VIEW_4	0x01_8000_0000	0x01_9FFF_FFFF	512MiB	90° view with vertical mirror
TILER_VIEW_5	0x01_A000_0000	0x01_BFFF_FFFF	512MiB	270° view
TILER_VIEW_6	0x01_C000_0000	0x01_DFFF_FFFF	512MiB	90° view
TILER_VIEW_7	0x01_E000_0000	0x01_FFFF_FFFF	512MiB	90° view with horizontal mirror

NOTE: TILER view memory space is only visible for Display Subsystem (DSS).