Introduction

This chapter introduces the features, subsystems, and architecture of the AM572x high-performance processor.

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1.1 AM572x Overview

AM572x is a high-performance, Sitara™ device, integrated on a 28-nm technology.

- The architecture is designed for embedded applications including industrial communication, Human Machine Interface (HMI), automation and control, and other high performance and general use applications, and best-in-class CPU performance, video, image, and graphics processing sufficient to support:
  - Streaming video up to full high definition (Full-HD) (1920×1080p, 60fps)
  - 2-dimensional (2D) and 3-dimensional (3D) graphics and composition

NOTE: The supported set of features and peripherals is device part number dependent. Refer to device Data Manual, for more information.

- The device is composed of the following main subsystems:
  - Dual Cortex®-A15 microprocessor unit (MPU) subsystem, incorporating two ARM® Cortex-A15 cores
  - Two digital signal processor (DSP) C66x subsystems
  - Image and video accelerator high-definition (IVA-HD) subsystem
  - Two Dual Cortex®-M4 image processing unit (IPU) subsystems, each incorporating two ARM Cortex-M4 microprocessors
    - IPU1 subsystem is available for general purpose usage
    - IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing
  - Display subsystem (DSS)
  - Video Processing subsystem (VPE)
  - Video Input Capture (VIP)
  - 3D-graphics processing unit (GPU) subsystem, including POWERVR™ SGX544 dual-core
  - 2D-graphics accelerator (BB2D) subsystem, including Vivante™ GC320 core
  - Three pulse-width modulation (PWM) subsystems
  - Real-time clock (RTC) subsystem
  - Two dual-core Programmable Real-time Unit and Industrial Communication Subsystems (PRU-ICSS).
  - Debug subsystem
- The device provides a rich set of connectivity peripherals, including among others:
  - One USB3.0 and one USB2.0 subsystem
  - SATA 2 subsystem
  - Two PCI Express Gen2 subsystems
  - Gigabit Ethernet Switch subsystem, providing two external Ethernet ports and one internal CPPI interface port
  - Two Controller Area Network (DCAN) subsystems
- The device includes support for:
  - Error Detection and Correction:
    - Parity bit per byte on C66x DSP L1 program cache (L1P), and Single-Error Correction Dual-Error Detection (SECDED) on L2 memories on the DSP
    - SECDED on Large L3 memory
  - MMU/MPU
    - MMU used for key masters (Cortex-A15 MPU, Cortex-M4 IPU, C66x DSP, EDMA)
    - Memory protection of C66x cores
    - MMU inside the Dynamic Memory Manager
- The device includes state-of-the-art integrated power-management techniques required for high-

performance embedded products.

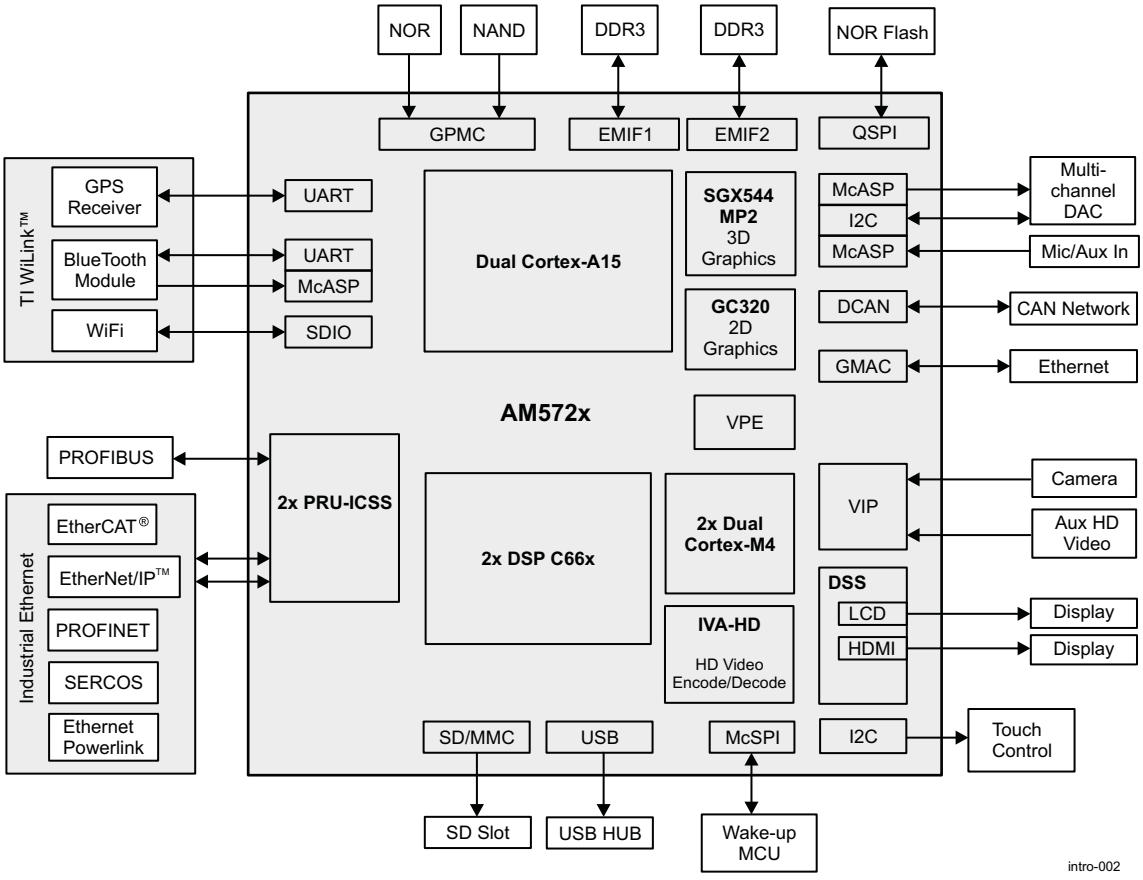
- The device also integrates:
  - On-chip memory
  - External memory interfaces
  - Memory management
  - Level 3 (L3) and level 4 (L4) interconnects
  - System and serial peripherals

1.2 AM572x Environment

This section provides an overview of the AM572x environment.

Figure 1-1 is an example for a non-exhaustive environment for the AM572x device.

Figure 1-1. AM572x Sample Environment Diagram

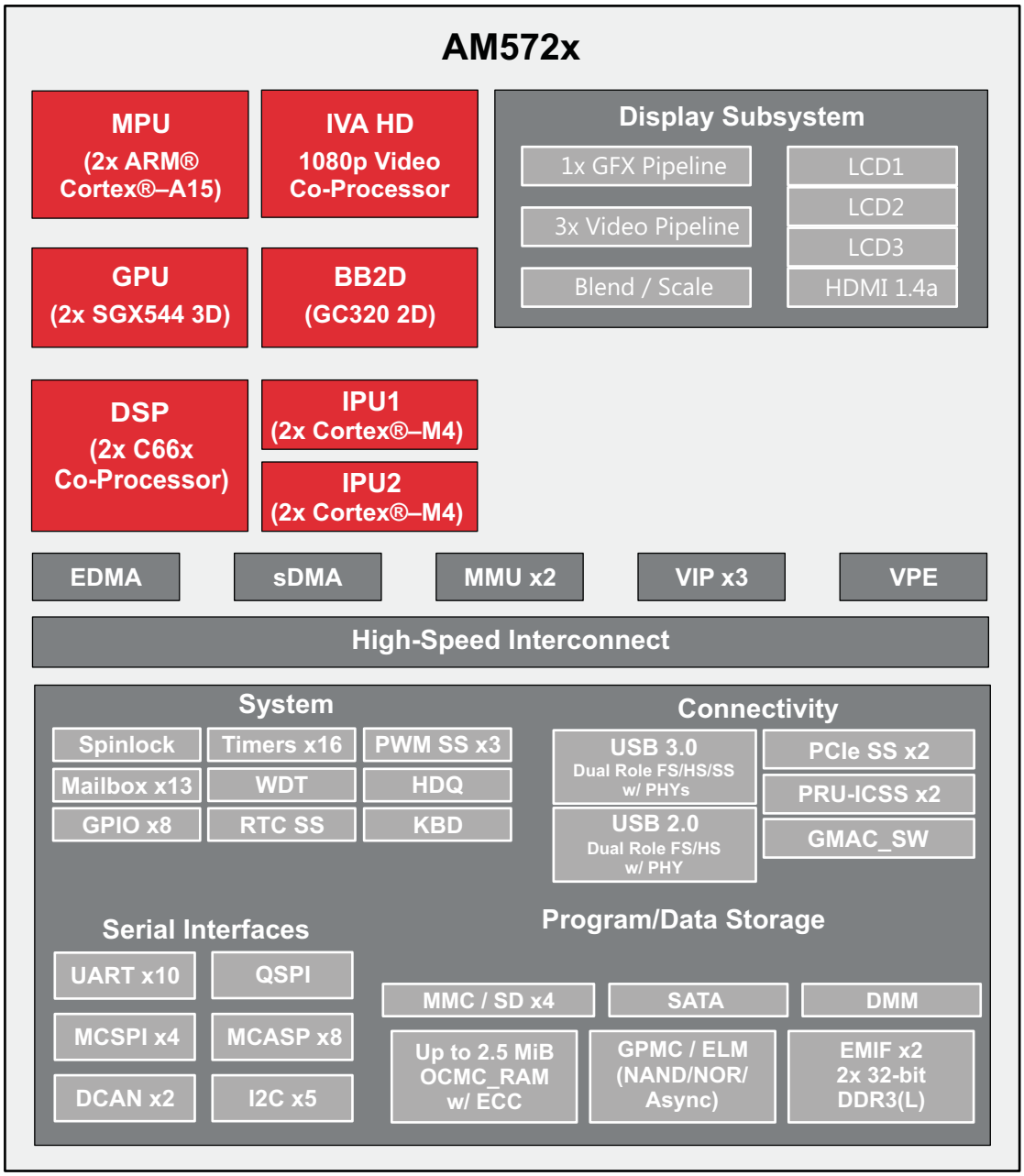


1.3 AM572x Description

The AM572x device is offered in a 760-ball, 23×23-mm, 0.8-mm ball pitch, ball grid array (BGA) package.

Figure 1-2 is the block diagram of the AM572x device.

Figure 1-2. AM572x Block Diagram



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NOTE: The supported set of features and peripherals is device part number dependent. Refer to device Data Manual, for more information.

1.3.1 MPU Subsystem

The Dual Cortex-A15 MPU subsystem integrates the following submodules:

- ARM Cortex-A15 MPCore
  - Two central processing units (CPUs)
  - ARM Version 7 ISA: Standard ARM instruction set plus Thumb®-2, Jazelle® RCT Java™ accelerator, hardware virtualization support, and large physical address extensions (LPAE)
  - Neon™ SIMD coprocessor and VFPv4 per CPU
  - Interrupt controller with up to 160 interrupt requests
  - One general-purpose timer and one watchdog timer per CPU
  - Debug and trace features
  - 32-KiB instruction and 32-KiB data level 1 (L1) cache per CPU
- Shared 2-MiB level 2 (L2) cache
- 48-KiB bootable ROM
- Local power, reset, and clock management (PRCM) module
- Emulation features
- Digital phase-locked loop (DPLL)

1.3.2 DSP Subsystems

There are two DSP subsystems in the device. Each DSP subsystem contains the following submodules:

- TMS320C66x™ VLIW DSP core for audio processing, and general-purpose imaging and video processing. It extends the performance of existing C64x+™ and C647x™ DSPs through enhancements and new features.
  - 32-KiB L1D and 32-KiB L1P cache or addressable SRAM
  - 288-KiB L2 cache
    - 256-KiB configurable as cache or SRAM
    - 32-KiB SRAM
- Enhanced direct memory access (EDMA) engine for video and audio data transfer
- Memory management units (MMU) for address management.
- Interrupt controller (INTC)
- Emulation capabilities

1.3.3 PRU-ICSS

There are two Programmable Real-time Unit and Industrial Communication Subsystems (PRU-ICSS) in the device. Each PRU-ICSS consists of dual 32-bit RISC cores (Programmable Real-Time Units, or PRUs), shared data and instruction memories, internal peripheral modules, and an interrupt controller (INTC).

Among the interfaces supported by the PRU-ICSS are real-time industrial protocols used in master and slave mode, such as:

- EtherCAT®
- PROFINET
- EtherNet/IP™
- PROFIBUS
- Ethernet Powerlink
- SERCOS

1.3.4 IPU Subsystems

There are two Dual Cortex-M4 IPU subsystems in the device:

- IPU1 subsystem is available for general purpose usage
- IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing

Each IPU subsystem includes the following components:

- Two Cortex-M4 CPUs
- ARMv7E-M and Thumb-2 instruction set architectures
- Hardware division and single-cycle multiplication acceleration
- Dedicated INTC with up to 63 physical interrupt events with 16-level priority
- Two-level memory subsystem hierarchy
  - L1 (32-KiB shared cache memory)
  - L2 ROM + RAM
    - 64-KiB RAM
    - 16-KiB bootable ROM
- MMU for address translation
- Integrated power management
- Emulation feature embedded in the Cortex-M4

1.3.5 IVA-HD Subsystem

The IVA-HD subsystem is a set of video encoder and decoder hardware accelerators. The list of supported codecs can be found in the software development kit (SDK) documentation.

1.3.6 Display Subsystem

The display subsystem provides the control signals required to interface the device system memory frame buffer (SDRAM) directly to the displays. It supports hardware cursor, independent gamma curve on all interfaces, multiple-buffer, and programmable color phase rotation. The display subsystem allows low-power display refresh and arbitration between normal and low-priority pipelines.

The display subsystem consists of the following components:

- Display controller: Reads and displays the encoded pixel data stored in memory and writes the output of one of the overlays or one of the pipelines into the system memory. The display controller supports the following components:
  - Three video pipelines, one graphic pipeline, and one write-back pipeline. The graphic pipeline supports pixel formats such as: ARGB16-4444, RGB16-565, ARGB16-1555, ARGB32-8888, RGBA32-8888, RGB24-888. It allows selection of the color-depth expansion.
  - Write-back pipeline: Uses poly-phase filtering for independent horizontal and vertical resampling (upsampling and downsampling). It allows programmable color space conversion of RGB24 into YUV4:2:2-UYVY, YUV4:2:2-YUV2, or YUV4:2:0-NV12 or NV21, and selection of color-depth reduction from RGB24 to RGB16.
  - Three LCD outputs, each one with dedicated overlay manager, for support of active matrix color displays (up to 24-bit interface). Maximum listed resolutions are not supported concurrently on all outputs.
    - First main LCD output delivered on MIPI® DPI 1.0 LCD pixel interface, supporting up to WUXGA (1920 x 1200) with reduced blanking periods.
    - Second and third LCD outputs delivered on MIPI DPI 2.0 LCD pixel interfaces, supporting up to WUXGA (1920 x 1200) with reduced blanking periods.
  - One TV output with dedicated overlay manager to support HDMI v1.4a interface (1080p @ 60 fps video and multichannel audio)
  - Own direct memory access (DMA) engine
- High-definition multimedia interface (HDMI) encoder with the following main features:
  - HDMI 1.4a and DVI 1.0 compliant

1.3.7 Video Processing Subsystem

The video processing engine (VPE) module provides support for the following memory-to-memory operations:

- Reads of raster or tiled YUV420 coplanar, YUV422 coplanar, or YUV422 interleaved video
- Deinterlacing up to two 1080i @60fps video streams
- Scaling up to 1080p (1920x1080 resolution) of the input video
- Chroma up- and downsampling
- VC-1 Range Mapping and Range Reduction
- Color space conversion
- Writes of the resulting video in YUV420 coplanar (raster or tiled), YUV422 coplanar (raster or tiled), YUV422 interleaved (raster or tiled), YUV444 single plane (raster only), or RGB888 (raster only).

1.3.8 Video Capture

There are three Video Input Port (VIP) modules in the device, providing video capture functions.

VIP1 and VIP2 modules support each up to:

- Two separate 24-bit video ports for parallel RGB/YUV/RAW (or BT656/1120) data, up to 165 MHz
- Two separate 8-bit video ports for YUV/RAW (or BT656) data, up to 165 MHz

VIP3 module supports up to two separate 16-bit video ports for parallel RGB/YUV/RAW (or BT656/1120) data, up to 165 MHz.

Each VIP module also supports:

- Embedded Sync (multiplexed sources) and Discrete Sync (single source) data interface modes
- Color space conversion and scaling:
  - Up to 2047 pixels wide input with scaling
  - Up to 3840 pixels wide input - when chroma up/down sampling without scaling
  - Up to 4095 pixels wide input - without scaling and chroma up/down sampling
  - Maximum supported input resolution is further limited by:
    - Pixel clock and feature-dependent constraints
    - For RGB24-bit format (RAW data), the maximum frame width is limited to 2730 pixels
- Embedded DMA engine, supporting tiled (2D) and raster addressing

1.3.9 3D GPU Subsystem

The 3D graphics processing unit (GPU) subsystem is based on POWERVR® SGX544 subsystem from Imagination Technologies. It supports general embedded applications. The GPU can process different data types simultaneously, such as: pixel data, vertex data, video data, and general-purpose data.

The GPU subsystem has the following features:

- Multicore GPU architecture: two SGX544 cores. Shared system level cache of 128 KiB
- Tile-based deferred rendering architecture
- Second-generation universal scalable shader engines (USSE2), multithreaded engines incorporating pixel and vertex shader functionality
- Present and texture load accelerators
  - Enables to move, rotate, twiddle, and scale texture surfaces.
  - Supports RGB, ARGB, YUV422, and YUV420 surface formats.
  - Supports bilinear upscale.
  - Supports source colorkey.
- Industry-standard API supports OpenGL®-ES 1.1 and 2.0
- Fine-grained task switching, load balancing, and power management

- Programmable high-quality image antialiasing
- Bilinear, trilinear, anisotropic texture filtering
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture (MMU)

1.3.10 BB2D Subsystem

The 2D BitBlt (BB2D) graphics accelerator subsystem is based on the GC320 core from Vivante Corporation and has the following features:

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw
- BB2D architecture:
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Clipping rectangle support
  - Alpha blending includes Java 2 Porter-Duff compositing rules
  - 90-, 180-, 270-degree rotation on every primitive
  - YUV-to-RGB color space conversion
  - Programmable display format conversion with 14 source and 7 destination formats
  - High-quality, 9-tap, 32-phase filter for image and video scaling at 1080p
  - Monochrome expansion for text rendering
  - 32K × 32K coordinate system

1.3.11 On-Chip Debug Support

The on-chip debug support has the following features:

- Multiprocessor debugging lets users control multiple CPU cores embedded in the device, such as:
  - Global starting and stopping of individual or multiple processors
  - Each processor can generate triggers that can be used to alter the execution flow of other processors
  - System clocking and power down
  - Interconnection of multiple devices
  - Channel triggering
- Target debugging, using IEEE1149.1 (JTAG®)
- Reduction of power consumption in normal operating mode

The debug subsystem includes:

- Generic TAP for emulation and test control (ICEPick-D™)
- Debug access port (DAP)
- Embedded Trace Macro (ETM)
- Trace Port Interface Unit (TPIU)
- Embedded Trace Buffer (ETM)
- Emulation Pin Manager (EPM)
- Cross triggering (XTRIG)

The debug subsystem provides also:

- ICEMelter, for controlling the wake-up and power-down of the emulation power domain
- L3_INSTR CORE instrumentation interconnect

- OCP watch-point (OCP-WP), for monitoring L3 interconnect transaction when target transaction attributes match the user-defined attributes or trigger on external debug event
- Power-management events profiler (PM instrumentation)
- Clock-management events profiler (CM instrumentation)
- Statistics collector (performance probes)

1.3.12 Power, Reset, and Clock Management

The PRCM module allows efficient control of clocks and power according to the required performance, and reduction of power consumption. The PRCM module is divided into:

- Power and reset management (PRM) with the following features:
  - Dynamic clock gating
  - Dynamic voltage and frequency scaling (DVFS)
  - Dynamic power switching (DPS)
  - Static leakage management (SLM)
- Clock management (CM) for clock generation and distribution, allowing reduction of dynamic consumption.

1.3.13 On-Chip Memory

- The device includes up to three instantiations of an On-Chip Memory Controller (OCMC) with associated RAM with ECC, with total size up to 2.5 MiB.
- Circular buffer feature for OCMC RAM (8-MiB virtual address space required)
- Save and Restore Memory / Scratch Pad in the wake-up domain

1.3.14 Memory Management

The memory management is performed from:

- System DMA controller with up to 128 hardware requests, 32 prioritizable logical channels, and 256 × 64-bit FIFO dynamically allocable between active channels.
- Enhanced DMA controller supporting two simultaneous read and two simultaneous write physical channels, and up to 64 programmable logical channels.
- Dynamic memory management (DMM) module, which performs global address translation, address rotation (tiling), and access interleaving between the two EMIF channels.
- Two memory management units (MMU), with 4KiB, 64KiB, 1MiB, 16MiB programmable page sizes, and 32 entries TLB.
  - MMU1 dedicated to EDMA
  - MMU2 dedicated to PCIe

1.3.15 External Memory Interfaces

- Two 32-bit DDR controllers (EMIF1 and EMIF2), each supporting the following features:
  - Dual-port controller for efficient memory sharing between applications
  - 32-bit data path, one chip-select per memory controller
  - Memory density up to 2 GiB supported over one chip-select providing a total SDRAM space of 4 GiB addressable by the MPU extended address range.
- General-purpose memory controller (GPMC) supporting connection with:
  - Asynchronous SRAM memories
  - Asynchronous and synchronous NOR flash memories
  - NAND flash memories, with up to 16-bit ECC via the Error Location Module (ELM)
  - Pseudo-SRAM devices
- Quad SPI module, supporting 1 to 4 address bytes for SPI NOR flash, and up to 66-MHz single data

rate

1.3.16 System and Connectivity Peripherals

The AM572x device supports a comprehensive set of peripherals to provide flexible and high-speed interfacing and on-chip programming resources.

1.3.16.1 System Peripherals

- Sixteen general-purpose timers (two timer modules supporting 1-ms tick generation)
- One watchdog timer (WDT)
- One 32-kHz synchronization timer
- System control module, which contains registers for the following functions:
  - Static device configuration
  - Debug and observability
  - Status
  - Pad configuration
  - I/O configuration
  - eFuse logic
  - Analog function control
  - System boot decoding logic
- Thirteen system Mailboxes for communication between MPU, IPU, DSP, and PRU-ICSS.
- SpinLock module for hardware semaphore between the MPU, DSP, and IPU subsystems
- Inter-processor Communication Register
- Three Pulse Width Modulation Subsystems (PWMSS), each containing Enhanced High Resolution Pulse Width Modulator (eHRPWM), Enhanced Capture (eCAP), and Enhanced Quadrature Encoded Pulse (eQEP) modules.
- Real-Time-Clock Subsystem (RTCSS), supporting four external wake-up inputs and one power enable output, all of which are 3.3- or 1.8-V multivoltage I/Os.
- Eight general-purpose input/output (GPIO) modules with 32 I/Os each. One GPIO module supporting wake-up request generation.
- HDQ™/1-Wire® – Benchmarq HDQ and Dallas Semiconductor 1-Wire protocols interface
- Keyboard controller, supporting up to 9 × 9 matrix keypads

1.3.16.2 Media Connectivity Peripherals

- Four HS-MMC/SD/SDIO modules:
  - Two modules acting as HS-MMC/SD initiator controllers, supporting JEDEC JESD84 v4.5-A441 and SD3.0 physical layer with SDA3.00 standards
    - One controller with 8-bit interface for JESD84 memories with dual voltage IOs (1.8 or 3.3 V). Another controller with 4-bit interface for external card support with embedded dual voltage I/Os (1.8 or 3 V) and supporting UHS-I rates.
    - Each controller including its DMA controller compliant to ADMA2 (SDA3.00 Part A2 DMA controller)
  - Two modules acting as SDIO interface controllers. One controller supporting 4-bit data bus width. Another controller supporting up to 8-bit data bus width.
- One SuperSpeed Universal Serial Bus (USB) Dual-Role-Device (DRD) subsystem with embedded HS and SS PHYs, compatible with the USB2.0 (up to 480 Mbps) and USB3.0 (5 Gbps) standards
- One High Speed USB subsystem:
  - One HS USB subsystem with embedded HS PHY, supporting up to 480 Mbps.
- One SATA subsystem, providing interface for solid-state drive (SSD) or hard-disk drive (HDD) mass storage. Supports one HBA port with SATA-2 generation speed of 3 Gbps.

1.3.16.3 Connectivity Peripherals

- One 3-port Gigabit Ethernet Switch subsystem (10, 100, or 1000 Mbps). The switch provides two external Ethernet ports and one internal CPPI interface port with AVB/Industrial Ethernet and 802.1ae support. Included support for 3.3-V RMII/MII and 1.8- or 3.3-V RGMII.
- Two DCAN controllers, supporting bitrates up to 1 Mbit/s and compliant to the Controller Area Network (CAN) 2.0B protocol specification.
- Two PCI Express subsystems, one providing Gen2 compliant 2-lane port, and the other providing Gen2 compliant 1-lane port, up to 5 Gbps per lane. Both PCIe subsystems provide support for either Root Complex or Endpoint. The two PCIe subsystems share common 2-lane PCIe PHY, configurable to operate either as 2-lane to one controller (PCIe_SS1) or two separate lanes to two controllers (PCIe_SS1 and PCIe_SS2).

1.3.16.4 Audio Connectivity Peripherals

- Eight multichannel audio serial ports (McASP):
  - Two McASP supporting up to 16 channels each and independent TX/RX clock/sync domains
  - Six McASP supporting up to 4 channels each and unified clock/sync domain
  - Features list of the McASP include:
    - Independent transmit and receive modules, each including programmable clock and frame sync generator, TDM streams from 2 to 32, support for time slot sizes up to 32 bits, data formatter for bit manipulation
    - Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components.
    - Wide variety of I2S and similar bit-stream formats
    - Integrated digital audio interface transmitter (DIT) supporting S/PDIF, IEC60958-1, AES-3 formats, and enhanced channel status/user data RAM
    - 384-slot TDM with external digital audio interface receiver (DIR) device
    - Extensive error checking and recovery

1.3.16.5 Serial Control Peripherals

- Ten universal asynchronous receiver/transmitter (UART) modules as serial-communication interfaces, 16C750 compatible.
  - One UART module with IrDA features
- Four general purpose multichannel serial peripheral interface (McSPI) modules
- Five multimaster HS I^2C, compliant with Philips I2C specification version 2.1.
  - I2C1 and I2C2 controllers suppot Fast-mode, with rates up to 400 Kbps
  - I2C3, I2C4 and I2C5 controllers support High-speed mode, with rates up to 3.4 Mbps

1.4 AM572x Family

The AM572x family is composed of several device variants (that is AM5728, AM5726, etc.).The supported set of features and peripherals is device part number dependent. Refer to device Data Manual, for more information.

1.5 AM572x Device Identification

Table 1-1 describes the identification registers.

The identification registers include the data registers listed in Table 1-2 and Table 1-4. These registers are read-only accessed ports that are programmed into eFuses FARM FROM.

Table 1-1. Device Identification Register Fields

Register Field	Alias Name	Physical Address	Address Offset
CTRL_CORE_STATUS[8:6] DEVICE_TYPE	DEVICE_TYPE	0x4A00 2134	0x134
CTRL_WKUP_STD_FUSE_DIE_ID_0[31:0] STD_FUSE_DIE_ID_0	DIE_ID[31:0]	0x4AE0 C200	0x200
CTRL_WKUP_ID_CODE[31:0] STD_FUSE_IDCODE	ID_CODE	0x4AE0 C204	0x204
CTRL_WKUP_STD_FUSE_DIE_ID_1[31:0] STD_FUSE_DIE_ID_1	DIE_ID[63:32]	0x4AE0 C208	0x208
CTRL_WKUP_STD_FUSE_DIE_ID_2[31:0] STD_FUSE_DIE_ID_2	DIE_ID[95:64]	0x4AE0 C20C	0x20C
CTRL_WKUP_STD_FUSE_DIE_ID_3[31:0] STD_FUSE_DIE_ID_3	DIE_ID[127:96]	0x4AE0 C210	0x210
CTRL_WKUP_STD_FUSE_PROD_ID_0[31:0] STD_FUSE_PROD_ID	PROD_ID	0x4AE0 C214	0x214

Table 1-2. DIE_ID

Register Field	Alias Name	Value
CTRL_WKUP_STD_FUSE_DIE_ID_0[31:0] STD_FUSE_DIE_ID_0	DIE_ID[31:0]	This register is for internal-use only.
CTRL_WKUP_STD_FUSE_DIE_ID_1[31:0] STD_FUSE_DIE_ID_1	DIE_ID[63:32]	This register is for internal-use only.
CTRL_WKUP_STD_FUSE_DIE_ID_2[31:0] STD_FUSE_DIE_ID_2	DIE_ID[95:64]	Part number identifier. See Table 1-3 for more information.
CTRL_WKUP_STD_FUSE_DIE_ID_3[31:0] STD_FUSE_DIE_ID_3	DIE_ID[127:96]	Reserved

The part number identification data can be read in the [31:0] STD_FUSE_DIE_ID_2 bit-field of the CTRL_WKUP_STD_FUSE_DIE_ID_2 register. See Table 1-3 for more information.

Table 1-3. AM572x Part Number Identifier

CTRL_WKUP_STD_FUSE_DIE_ID_2 [31:0] STD_FUSE_DIE_ID_2	Value and Description	Comment
[31:24] Base PN	57 (0x39) = AM5726 58 (0x3A) = AM5726-E (Ethercat slave enabled) 59 (0x3B) = AM5728 60 (0x3C) = AM5728-E (Ethercat slave enabled) Others = Reserved	Refer to device DM for details on the supported features for a given part number.
[23:19] Speed	23 (0x17) = X speed designator Others = Reserved	Refer to device DM for supported speed grades for a given device, and the definition for supported speed grades.
	For SR1.1:	Junction temperature.

Table 1-3. AM572x Part Number Identifier (continued)

CTRL_WKUP_STD_FUSE_DIE_ID_2 [31:0] STD_FUSE_DIE_ID_2	Value and Description	Comment
[18] Temperature	0 = Commercial, 0°C to 90°C 1 = Industrial, -40°C to 105°C For SR2.0: 0 = Automotive Q100, -40°C to 125°C 1 = Commercial, 0°C to 90°C Industrial, -40°C to 105°C	
[17:16] Package	2 = ABC 23×23 Solder Flip Chip Others = Reserved	Refer to device DM for details on packaging.
[15:0] Reserved	Reserved	Reserved

The product type can be read in the value of the RAMP_SYSTEM bit field of the ID_CODE register (see Table 1-4). The silicon revision can be read in the value of the VERSION bit field of the ID_CODE register (see Table 1-4).

Table 1-4. ID_CODE

Register Field	Value	Comment
CTRL_WKUP_ID_CODE[31:28] VERSION	See Table 1-5	Revision number
CTRL_WKUP_ID_CODE[27:12] RAMP_SYSTEM	See Table 1-5	Ramp system number
CTRL_WKUP_ID_CODE[11:1] TI_IDM	0x17	Manufacturer identity (TI)
CTRL_WKUP_ID_CODE[0] ONE	0x1	Always set to 1

Table 1-5 lists the ramp system and revision number values.

Table 1-5. AM572x ID_CODE Values

Silicon Type	VERSION	RAMP_SYSTEM	ID_CODE
AM572x SR1.0	0x0	0xB990	0x0B99002F
AM572x SR1.1	0x1	0xB990	0x1B99002F
AM572x SR2.0	0x2	0xB990	0x2B99002F

1.6 AM572x Package Characteristics Overview

The AM572x die will be offered with the following characteristics:

- Body: 23 × 23mm
- Technology: Ball Grid Array (BGA) package
- Ball pitch: 0.8-mm ball pitch
- Pattern: partial grid
- Pins: 760 total device pins

For more information refer to device Data Manual.