Interrupt Controllers

This chapter describes the interrupt controllers (INTCs) in the device.

Topic **Page**

17.1 Interrupt Controllers Overview

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. The MPU, DSP (x2), IPU (x2), EVE (x4), and PRU-ICSS (x2) subsystems are capable of servicing these interrupts via their integrated interrupt controllers. In addition, each processor's interrupt controller is preceded by an Interrupt Controller Crossbar (IRQ_CROSSBAR) that provides flexibility in mapping the device interrupts to processor interrupt inputs. For more information about IRQ crossbar, see Chapter 18, *Control Module*.

Dual Cortex®-A15 MPU Subsystem Interrupt Controller (MPU_INTC)

The MPU_INTC module (also called Generalized Interrupt Controller [GIC]) is a single functional unit that is integrated in the ARM® Cortex-A15 multiprocessor core (MPCore) alongside Cortex-A15 processors. It provides:

- 160 hardware interrupt inputs
- Generation of interrupts by software
- Prioritization of interrupts
- Masking of any interrupts
- Distribution of the interrupts to the target Cortex-A15 processor(s)
- Tracking the status of interrupts

Each Cortex-A15 processor supports three main groups of interrupt sources, with each interrupt source having a unique ID:

- *Software Generated Interrupts (SGIs):* SGIs are generated by writing to the Cortex-A15 Software Generated Interrupt Register (GICD_SGIR). A maximum of 16 SGIs (ID0–ID15) can be generated for each CPU interface. An SGI has edge-triggered properties. The software triggering of the interrupt is equivalent to the edge transition of the interrupt signal on a peripheral input.
- *Private Peripheral Interrupts (PPIs):* A PPI is an interrupt generated by a peripheral that is specific to a single processor. Although interrupts ID16–ID31 are dedicated to PPIs in general, only seven PPIs are actually used for each CPU interface (ID25–ID31). Interrupts ID16–ID24 are reserved (not used).
- *Shared Peripheral Interrupts (SPIs):* SPIs are triggered by events generated on associated interrupt input lines. In this device, the GIC is configured to support 160 SPIs corresponding to its external IRQS[159:0] signals. SPIs start at ID32 and their mapping is presented in Section 17.3.1.

For detailed information about this module and description of SGIs and PPIs, see the ARM *Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

C66x DSP Subsystem Interrupt Controller (DSPx_INTC, where x = 1, 2)

There are two Digital Signal Processing (DSP) subsystems in the device - DSP1, and DSP2. Each DSP subsystem integrates an interrupt controller - DSPx_INTC, which interfaces the system events to the C66x core interrupt and exceptions inputs. It combines up to 128 interrupts into 12 prioritized interrupts presented to the C66x CPU.

For detailed information about this module, see Chapter 5, *DSP Subsystem*.

Dual Cortex-M4 IPU Subsystem Interrupt Controller (IPUx_Cx_INTC, where x = 1, 2)

There are two Image Processing Unit (IPU) subsystems in the device - IPU1, and IPU2. Each IPU subsystem integrates two ARM Cortex-M4 cores.

A Nested Vectored Interrupt Controller (NVIC) is integrated within each Cortex-M4. The interrupt mapping is the same (per IPU) for the two cores to facilitate parallel processing. The NVIC supports:

- 64 external interrupts (in addition to 16 Cortex-M4 internal interrupts), which are dynamically prioritized with 16 levels of priority defined for each core
- Low-latency exception and interrupt handling
- Prioritization and handling of exceptions
- Control of the local power management
- Debug accesses to the processor core

For detailed information about this module, refer to ARM *Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

NOTE: IPUx_Cx_INTC is a unified name for the following interrupt controllers:
- IPU1_C0_INTC - NVIC in first Cortex-M4 core of IPU1
- IPU1_C1_INTC - NVIC in second Cortex-M4 core of IPU1
- IPU2_C0_INTC - NVIC in first Cortex-M4 core of IPU2
- IPU2_C1_INTC - NVIC in second Cortex-M4 core of IPU2

EVE Subsystem Interrupt Controller (EVEx_INTC, where x = 1 to 4)

NOTE: EVE is not supported in this family of devices.

There are four Embedded Video Engine (EVE) subsystems in the device - EVE1, EVE2, EVE3, and EVE4. Each EVE subsystem integrates an interrupt controller - EVEx_INTC, which handles incoming interrupts, merging them with internal interrupt sources to drive ARP32's interrupt inputs. It also allows ARP32 to generate outgoing interrupts or events to synchronize with other system processors and EDMA.

The EVEx_INTC supports up to 32 active-high level interrupt inputs. Its architecture allows both hardware and software prioritization.

For detailed information about this module, see Chapter 8, *Embedded Vision Engine*.

PRU-ICSS Interrupt Controller (PRUSSx_INTC, where x = 1 to 2)

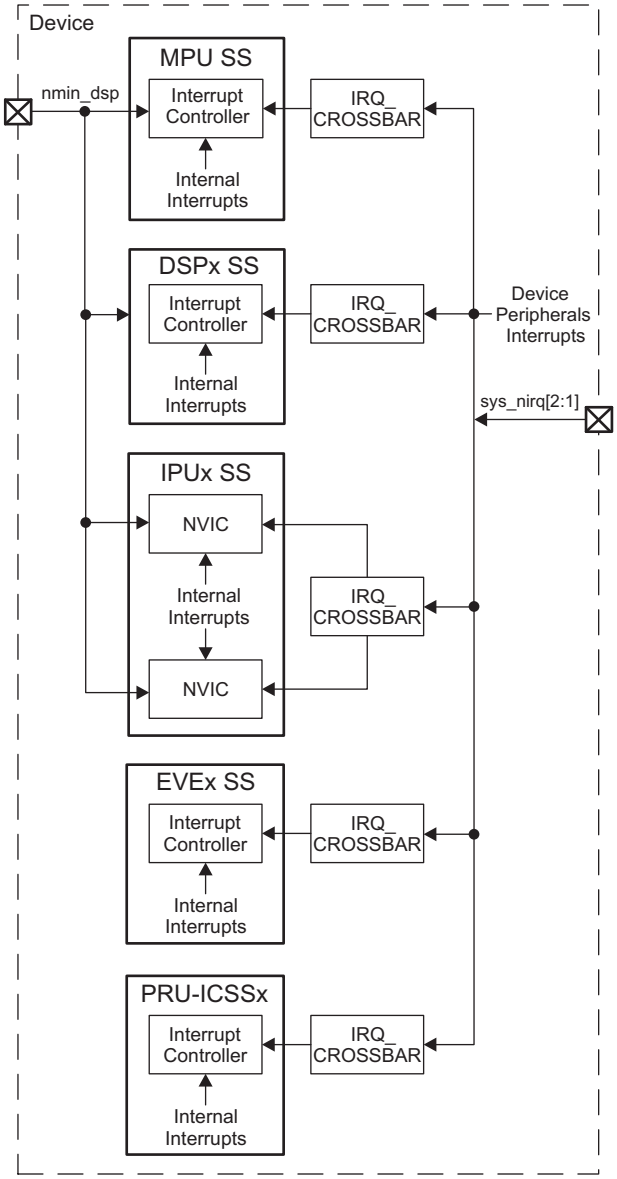
The PRUSSx_INTC is an interface between interrupts coming from different parts of the system (referred to as system events) and the PRU-ICSS interrupt interface.

The PRUSSx_INTC has the following features:
- Capturing up to 64 System Events
- Supports up to 10 interrupt channels
- Generation of 10 Host Interrupts:
  - 2 Host Interrupts for the PRUs
  - 8 Host Interrupts exported from the PRU-ICSS for signaling the ARM interrupt controllers
- Each system event can be enabled and disabled
- Each host event can be enabled and disabled
- Hardware prioritization of events

For detailed information about this module, see Chapter 30, *Programmable Real-Time Unit and Industrial Communication Subsystems*.

Figure 17-1 shows the top-level block diagram of the interrupt controllers in this device.

Figure 17-1. Interrupt Controllers in the Device



17.2 Interrupt Controllers Environment

Figure 17-2 shows the relationship between the device INTCs and external interrupts.

Figure 17-2. Interrupts From External Devices

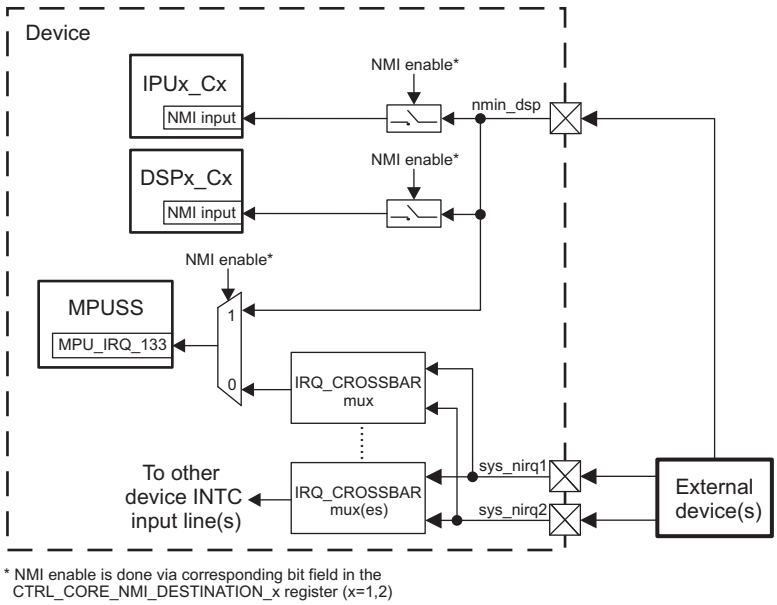


Table 17-1 describes the signals that can be used by external devices to generate interrupts to the device INTCs.

Table 17-1. Interrupts From External Devices

Device Pin	I/O[1]	Description
sys_nirq1	I	External devices can use these pins to generate a system wake-up interrupt event to any device INTC. The user must take care to configure the corresponding IRQ_CROSSBAR properly (via Control Module).
sys_nirq2	I	

(1) I = Input, O = Output

Table 17-1. Interrupts From External Devices (continued)

Device Pin	I/O[1]	Description
nmin_dsp	I	External device can use this pin to generate a non-maskable interrupt (NMI) event to the following device processors: - IPU1_C0, IPU1_C1. Upon enable (via Control Module), the NMI is routed directly to the NMI input of Cortex M4 core. Note that NMI can be enabled separately for IPU1_C0 and IPU1_C1. - IPU2_C0, IPU2_C1. Upon enable (via Control Module), the NMI is routed directly to the NMI input of Cortex M4 core. Note that NMI can be enabled separately for IPU2_C0 and IPU2_C1. - DSP1, DSP2. Upon enable (via Control Module), the NMI is routed directly to the NMI input of C66x CPU. The signal from the **nmin_dsp** pin can also be mapped to the MPU_INTC (MPU_IRQ_133 input) but it would be treated by Cortex-A15 as a general interrupt and not as a non-maskable interrupt. The Cortex-A15 processor does not provide NMI input. The Control Module registers CTRL_CORE_NMI_DESTINATION_1 and CTRL_CORE_NMI_DESTINATION_2 are used to route the **NMI** signal to the corresponding device processor subsystems as follows: • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_1 [23:16] IPU2_C1 enables NMI mapping to IPU2_C1; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_1 [15:8] IPU2_C0 enables NMI mapping to IPU2_C0; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_1 [7:0] IPU1_C1 enables NMI mapping to IPU1_C1; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_2 [31:24] IPU1_C0 enables NMI mapping to IPU1_C0; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_2 [23:16] DSP2 enables NMI mapping to DSP2; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_2 [15:8] DSP1 enables NMI mapping to DSP1; • Writing 0x1 to CTRL_CORE_NMI_DESTINATION_2 [7:0] MPU enables NMI mapping to MPU_IRQ_133 interrupt line of MPU_INTC; writing 0x0 to this bit field disables the NMI mapping and IRQ_CROSSBAR mux is mapped to MPU_IRQ_133 instead. For more information about CTRL_CORE_NMI_DESTINATION_1 and CTRL_CORE_NMI_DESTINATION_2 registers, see Chapter 18, *Control Module*.

NOTE: External devices can also use the GPIO modules to generate an interrupt to the device INTCs. For more information, see Chapter 27, *General-Purpose Interface*.

17.3 Interrupt Controllers Integration

Table 17-2 through Table 17-8 present the default interrupt mapping of the device INTCs. The mapping of device interrupts to IRQ_CROSSBAR inputs is presented in Table 17-13.

NOTE: All device interrupts (external to the MPU, DSP [x2], IPU [x2], EVE [x4], and PRU-ICSS [x2] subsystems) are active-high, level-sensitive.

CAUTION

A single interrupt source can be physically mapped to multiple INTCs. With multiple-mapped interrupts, it is strongly recommended to unmask each interrupt source in only one INTC at a time.

17.3.1 Interrupt Requests to MPU_INTC

Table 17-2 lists the default interrupt sources for the MPU_INTC. In addition, interrupts MPU_IRQ_4, MPU_IRQ_[130:7], MPU_IRQ_[138:133], and MPU_IRQ_[159:141] can alternatively be sourced through the MPU's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_MPU_IRQ_y_z registers (where *y* and *z* are indexes of INTC input lines) in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

NOTE: The interrupts listed in Table 17-2 are also called Shared Peripheral Interrupts (SPIs) in ARM Cortex-A15 terminology. That is, the MPU_IRQ_[159:0] interrupt inputs correspond to the **IRQS[N:0]** GIC signals (N = 159 for this device), described in the ARM *Cortex-A15 MPCore Processor Technical Reference Manual*.

The association between the Shared Peripheral Interrupts (MPU_IRQ_0 – MPU_IRQ_159) and the GIC inputs (ID32 – ID191) is shown in the first column of this table.

Table 17-2. MPU_INTC Default Interrupt Mapping

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_0 (ID32)	N/A	N/A	N/A	MPU_CLUSTER_IRQ_INTERR	Illegal writes to interrupt controller memory map region
MPU_IRQ_1 (ID33)	N/A	N/A	N/A	CS_CTI_MPU_C0_IRQ	TRIGOUT[6] of Cross Trigger Interface 0 (CTI0)
MPU_IRQ_2 (ID34)	N/A	N/A	N/A	CS_CTI_MPU_C1_IRQ	TRIGOUT[6] of Cross Trigger Interface 1 (CTI1)
MPU_IRQ_3 (ID35)	N/A	N/A	N/A	MPU_CLUSTER_IRQ_AXIERR	Error indication for AXI write transactions with a BRESP error condition
MPU_IRQ_4 (ID36)	1	CTRL_CORE_MPU_IRQ_4_7[8:0]	1	ELM_IRQ	Error location process completion interrupt
MPU_IRQ_5 (ID37)	N/A	N/A	N/A	WD_TIMER_MPU_C0_IRQ_WARN	MPU_WD_TIMER channel 0 warning interrupt
MPU_IRQ_6 (ID38)	N/A	N/A	N/A	WD_TIMER_MPU_C1_IRQ_WARN	MPU_WD_TIMER channel 1 warning interrupt
MPU_IRQ_7 (ID39)	2	CTRL_CORE_MPU_IRQ_4_7[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
MPU_IRQ_8 (ID40)	3	CTRL_CORE_MPU_IRQ_8_9[8:0]	3	CTRL_MODULE_CORE_IRQ_SEC _EVTS	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3.
MPU_IRQ_9 (ID41)	4	CTRL_CORE_MPU_IRQ_8_9[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
MPU_IRQ_10 (ID42)	5	CTRL_CORE_MPU_IRQ_10_11[8:0] (not functional)	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error[2]
MPU_IRQ_11 (ID43)	6	CTRL_CORE_MPU_IRQ_10_11[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
MPU_IRQ_12 (ID44)	7	CTRL_CORE_MPU_IRQ_12_13[8:0]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
MPU_IRQ_13 (ID45)	8	CTRL_CORE_MPU_IRQ_12_13[24:16]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
MPU_IRQ_14 (ID46)	9	CTRL_CORE_MPU_IRQ_14_15[8:0]	9	DMA_SYSTEM_IRQ_2	System DMA interrupt 2
MPU_IRQ_15 (ID47)	10	CTRL_CORE_MPU_IRQ_14_15[24:16]	10	DMA_SYSTEM_IRQ_3	System DMA interrupt 3
MPU_IRQ_16 (ID48)	11	CTRL_CORE_MPU_IRQ_16_17[8:0]	11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN statistic collector alarm interrupt
MPU_IRQ_17 (ID49)	12	CTRL_CORE_MPU_IRQ_16_17[24:16]	12	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_18 (ID50)	13	CTRL_CORE_MPU_IRQ_18_19[8:0]	13	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_19 (ID51)	14	CTRL_CORE_MPU_IRQ_18_19[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_20 (ID52)	15	CTRL_CORE_MPU_IRQ_20_21[8:0]	15	GPMC_IRQ	GPMC interrupt
MPU_IRQ_21 (ID53)	16	CTRL_CORE_MPU_IRQ_20_21[24:16]	16	GPU_IRQ	GPU interrupt
MPU_IRQ_22 (ID54)	17	CTRL_CORE_MPU_IRQ_22_23[8:0]	17	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_23 (ID55)	18	CTRL_CORE_MPU_IRQ_22_23[24:16]	18	Reserved	Reserved by default but can be remapped to a valid interrupt source

(1) This column shows the association between the Shared Peripheral Interrupts (MPU_IRQ_0 – MPU_IRQ_159) and the GIC inputs (ID32 – ID191).

(2) The L3_MAIN_IRQ_APP_ERR interrupt is directly mapped to the MPU_IRQ_10 line, bypassing the crossbar instance dedicated to this line. No other interrupt source can be mapped to MPU_IRQ_10.

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_24 (ID56)	19	CTRL_CORE_MPU_IRQ_24_25[8:0]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_25 (ID57)	20	CTRL_CORE_MPU_IRQ_24_25[24:16]	20	DISPC_IRQ	Display controller interrupt
MPU_IRQ_26 (ID58)	21	CTRL_CORE_MPU_IRQ_26_27[8:0]	21	MAILBOX1_IRQ_USER0	Mailbox 1 user 0 interrupt
MPU_IRQ_27 (ID59)	22	CTRL_CORE_MPU_IRQ_26_27[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_28 (ID60)	23	CTRL_CORE_MPU_IRQ_28_29[8:0]	23	DSP1_IRQ_MMU0	DSP1 MMU0 interrupt
MPU_IRQ_29 (ID61)	24	CTRL_CORE_MPU_IRQ_28_29[24:16]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
MPU_IRQ_30 (ID62)	25	CTRL_CORE_MPU_IRQ_30_31[8:0]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
MPU_IRQ_31 (ID63)	26	CTRL_CORE_MPU_IRQ_30_31[24:16]	26	GPIO3_IRQ_1	GPIO3 interrupt 1
MPU_IRQ_32 (ID64)	27	CTRL_CORE_MPU_IRQ_32_33[8:0]	27	GPIO4_IRQ_1	GPIO4 interrupt 1
MPU_IRQ_33 (ID65)	28	CTRL_CORE_MPU_IRQ_32_33[24:16]	28	GPIO5_IRQ_1	GPIO5 interrupt 1
MPU_IRQ_34 (ID66)	29	CTRL_CORE_MPU_IRQ_34_35[8:0]	29	GPIO6_IRQ_1	GPIO6 interrupt 1
MPU_IRQ_35 (ID67)	30	CTRL_CORE_MPU_IRQ_34_35[24:16]	30	GPIO7_IRQ_1	GPIO7 interrupt 1
MPU_IRQ_36 (ID68)	31	CTRL_CORE_MPU_IRQ_36_37[8:0]	31	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_37 (ID69)	32	CTRL_CORE_MPU_IRQ_36_37[24:16]	32	TIMER1_IRQ	TIMER1 interrupt
MPU_IRQ_38 (ID70)	33	CTRL_CORE_MPU_IRQ_38_39[8:0]	33	TIMER2_IRQ	TIMER2 interrupt
MPU_IRQ_39 (ID71)	34	CTRL_CORE_MPU_IRQ_38_39[24:16]	34	TIMER3_IRQ	TIMER3 interrupt
MPU_IRQ_40 (ID72)	35	CTRL_CORE_MPU_IRQ_40_41[8:0]	35	TIMER4_IRQ	TIMER4 interrupt
MPU_IRQ_41 (ID73)	36	CTRL_CORE_MPU_IRQ_40_41[24:16]	36	TIMER5_IRQ	TIMER5 interrupt
MPU_IRQ_42 (ID74)	37	CTRL_CORE_MPU_IRQ_42_43[8:0]	37	TIMER6_IRQ	TIMER6 interrupt
MPU_IRQ_43 (ID75)	38	CTRL_CORE_MPU_IRQ_42_43[24:16]	38	TIMER7_IRQ	TIMER7 interrupt
MPU_IRQ_44 (ID76)	39	CTRL_CORE_MPU_IRQ_44_45[8:0]	39	TIMER8_IRQ	TIMER8 interrupt
MPU_IRQ_45 (ID77)	40	CTRL_CORE_MPU_IRQ_44_45[24:16]	40	TIMER9_IRQ	TIMER9 interrupt
MPU_IRQ_46 (ID78)	41	CTRL_CORE_MPU_IRQ_46_47[8:0]	41	TIMER10_IRQ	TIMER10 interrupt
MPU_IRQ_47 (ID79)	42	CTRL_CORE_MPU_IRQ_46_47[24:16]	42	TIMER11_IRQ	TIMER11 interrupt
MPU_IRQ_48 (ID80)	43	CTRL_CORE_MPU_IRQ_48_49[8:0]	43	MCSPI4_IRQ	McSPI4 interrupt
MPU_IRQ_49 (ID81)	44	CTRL_CORE_MPU_IRQ_48_49[24:16]	44	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_50 (ID82)	45	CTRL_CORE_MPU_IRQ_50_51[8:0]	45	Reserved	Reserved by default but can be remapped to a valid interrupt source

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_51 (ID83)	46	CTRL_CORE_MPU_IRQ_50_51[24:16]	46	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_52 (ID84)	47	CTRL_CORE_MPU_IRQ_52_53[8:0]	47	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_53 (ID85)	48	CTRL_CORE_MPU_IRQ_52_53[24:16]	48	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_54 (ID86)	49	CTRL_CORE_MPU_IRQ_54_55[8:0]	49	SATA_IRQ	SATA interrupt
MPU_IRQ_55 (ID87)	50	CTRL_CORE_MPU_IRQ_54_55[24:16]	50	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_56 (ID88)	51	CTRL_CORE_MPU_IRQ_56_57[8:0]	51	I2C1_IRQ	I2C1 interrupt
MPU_IRQ_57 (ID89)	52	CTRL_CORE_MPU_IRQ_56_57[24:16]	52	I2C2_IRQ	I2C2 interrupt
MPU_IRQ_58 (ID90)	53	CTRL_CORE_MPU_IRQ_58_59[8:0]	53	HDQ1W_IRQ	HDQ1W interrupt
MPU_IRQ_59 (ID91)	54	CTRL_CORE_MPU_IRQ_58_59[24:16]	54	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_60 (ID92)	55	CTRL_CORE_MPU_IRQ_60_61[8:0]	55	I2C5_IRQ	I2C5 interrupt
MPU_IRQ_61 (ID93)	56	CTRL_CORE_MPU_IRQ_60_61[24:16]	56	I2C3_IRQ	I2C3 interrupt
MPU_IRQ_62 (ID94)	57	CTRL_CORE_MPU_IRQ_62_63[8:0]	57	I2C4_IRQ	I2C4 interrupt
MPU_IRQ_63 (ID95)	58	CTRL_CORE_MPU_IRQ_62_63[24:16]	58	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_64 (ID96)	59	CTRL_CORE_MPU_IRQ_64_65[8:0]	59	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_65 (ID97)	60	CTRL_CORE_MPU_IRQ_64_65[24:16]	60	MCSPI1_IRQ	McSPI1 interrupt
MPU_IRQ_66 (ID98)	61	CTRL_CORE_MPU_IRQ_66_67[8:0]	61	MCSPI2_IRQ	McSPI2 interrupt
MPU_IRQ_67 (ID99)	62	CTRL_CORE_MPU_IRQ_66_67[24:16]	62	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_68 (ID100)	63	CTRL_CORE_MPU_IRQ_68_69[8:0]	63	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_69 (ID101)	64	CTRL_CORE_MPU_IRQ_68_69[24:16]	64	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_70 (ID102)	65	CTRL_CORE_MPU_IRQ_70_71[8:0]	65	UART4_IRQ	UART4 interrupt
MPU_IRQ_71 (ID103)	66	CTRL_CORE_MPU_IRQ_70_71[24:16]	66	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_72 (ID104)	67	CTRL_CORE_MPU_IRQ_72_73[8:0]	67	UART1_IRQ	UART1 interrupt
MPU_IRQ_73 (ID105)	68	CTRL_CORE_MPU_IRQ_72_73[24:16]	68	UART2_IRQ	UART2 interrupt
MPU_IRQ_74 (ID106)	69	CTRL_CORE_MPU_IRQ_74_75[8:0]	69	UART3_IRQ	UART3 interrupt

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_75 (ID107)	70	CTRL_CORE_MPU_IRQ_74_75[24:16]	70	PBIAS_IRQ	MMC1 PBIAS interrupt (controlled via device Control Module)
MPU_IRQ_76 (ID108)	71	CTRL_CORE_MPU_IRQ_76_77[8:0]	71	USB1_IRQ_INTR0	USB1 interrupt 0
MPU_IRQ_77 (ID109)	72	CTRL_CORE_MPU_IRQ_76_77[24:16]	72	USB1_IRQ_INTR1	USB1 interrupt 1
MPU_IRQ_78 (ID110)	73	CTRL_CORE_MPU_IRQ_78_79[8:0]	73	USB2_IRQ_INTR0	USB2 interrupt 0
MPU_IRQ_79 (ID111)	74	CTRL_CORE_MPU_IRQ_78_79[24:16]	74	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_80 (ID112)	75	CTRL_CORE_MPU_IRQ_80_81[8:0]	75	WD_TIMER2_IRQ	WD_TIMER2 interrupt
MPU_IRQ_81 (ID113)	76	CTRL_CORE_MPU_IRQ_80_81[24:16]	76	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_82 (ID114)	77	CTRL_CORE_MPU_IRQ_82_83[8:0]	77	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_83 (ID115)	78	CTRL_CORE_MPU_IRQ_82_83[24:16]	78	MMC1_IRQ	MMC1 interrupt
MPU_IRQ_84 (ID116)	79	CTRL_CORE_MPU_IRQ_84_85[8:0]	79	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_85 (ID117)	80	CTRL_CORE_MPU_IRQ_84_85[24:16]	80	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_86 (ID118)	81	CTRL_CORE_MPU_IRQ_86_87[8:0]	81	MMC2_IRQ	MMC2 interrupt
MPU_IRQ_87 (ID119)	82	CTRL_CORE_MPU_IRQ_86_87[24:16]	82	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_88 (ID120)	83	CTRL_CORE_MPU_IRQ_88_89[8:0]	83	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_89 (ID121)	84	CTRL_CORE_MPU_IRQ_88_89[24:16]	84	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_90 (ID122)	85	CTRL_CORE_MPU_IRQ_90_91[8:0]	85	DEBUGSS_IRQ_CT_UART	CT_UART interrupt generated when data ready on RX or when TX empty
MPU_IRQ_91 (ID123)	86	CTRL_CORE_MPU_IRQ_90_91[24:16]	86	MCSPI3_IRQ	McSPI3 interrupt
MPU_IRQ_92 (ID124)	87	CTRL_CORE_MPU_IRQ_92_93[8:0]	87	USB2_IRQ_INTR1	USB2 interrupt 1
MPU_IRQ_93 (ID125)	88	CTRL_CORE_MPU_IRQ_92_93[24:16]	88	USB3_IRQ_INTR0[3]	USB3 interrupt 0
MPU_IRQ_94 (ID126)	89	CTRL_CORE_MPU_IRQ_94_95[8:0]	89	MMC3_IRQ	MMC3 interrupt
MPU_IRQ_95 (ID127)	90	CTRL_CORE_MPU_IRQ_94_95[24:16]	90	TIMER12_IRQ	TIMER12 interrupt
MPU_IRQ_96 (ID128)	91	CTRL_CORE_MPU_IRQ_96_97[8:0]	91	MMC4_IRQ	MMC4 interrupt
MPU_IRQ_97 (ID129)	92	CTRL_CORE_MPU_IRQ_96_97[24:16]	92	Reserved	Reserved by default but can be remapped to a valid interrupt source

(3) USB3 is not supported in this family of devices.

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_98 (ID130)	93	CTRL_CORE_MPU_IRQ_98_99[8:0]	93	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_99 (ID131)	94	CTRL_CORE_MPU_IRQ_98_99[24:16]	94	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_100 (ID132)	95	CTRL_CORE_MPU_IRQ_100_101[8:0]	395	IPU1_IRQ_MMU	IPU1 MMU interrupt
MPU_IRQ_101 (ID133)	96	CTRL_CORE_MPU_IRQ_100_101[24:16]	96	HDMI_IRQ	HDMI interrupt
MPU_IRQ_102 (ID134)	97	CTRL_CORE_MPU_IRQ_102_103[8:0]	97	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_103 (ID135)	98	CTRL_CORE_MPU_IRQ_102_103[24:16]	98	IVA_IRQ_SYNC_1	IVA ICONT2 sync interrupt
MPU_IRQ_104 (ID136)	99	CTRL_CORE_MPU_IRQ_104_105[8:0]	99	IVA_IRQ_SYNC_0	IVA ICONT1 sync interrupt
MPU_IRQ_105 (ID137)	100	CTRL_CORE_MPU_IRQ_104_105[24:16]	100	UART5_IRQ	UART5 interrupt
MPU_IRQ_106 (ID138)	101	CTRL_CORE_MPU_IRQ_106_107[8:0]	101	UART6_IRQ	UART6 interrupt
MPU_IRQ_107 (ID139)	102	CTRL_CORE_MPU_IRQ_106_107[24:16]	102	IVA_IRQ_MAILBOX_0	IVA mailbox user 0 interrupt
MPU_IRQ_108 (ID140)	103	CTRL_CORE_MPU_IRQ_108_109[8:0]	103	McASP1_IRQ_AREVT	McASP1 receive interrupt
MPU_IRQ_109 (ID141)	104	CTRL_CORE_MPU_IRQ_108_109[24:16]	104	McASP1_IRQ_AXEVT	McASP1 transmit interrupt
MPU_IRQ_110 (ID142)	105	CTRL_CORE_MPU_IRQ_110_111[8:0]	105	EMIF1_IRQ	EMIF1 interrupt
MPU_IRQ_111 (ID143)	106	CTRL_CORE_MPU_IRQ_110_111[24:16]	106	EMIF2_IRQ	EMIF2 interrupt
MPU_IRQ_112 (ID144)	107	CTRL_CORE_MPU_IRQ_112_113[8:0]	107	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_113 (ID145)	108	CTRL_CORE_MPU_IRQ_112_113[24:16]	108	DMM_IRQ	DMM interrupt
MPU_IRQ_114 (ID146)	109	CTRL_CORE_MPU_IRQ_114_115[8:0]	109	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_115 (ID147)	110	CTRL_CORE_MPU_IRQ_114_115[24:16]	110	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_116 (ID148)	111	CTRL_CORE_MPU_IRQ_116_117[8:0]	111	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_117 (ID149)	112	CTRL_CORE_MPU_IRQ_116_117[24:16]	112	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_118 (ID150)	113	CTRL_CORE_MPU_IRQ_118_119[8:0]	113	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_119 (ID151)	114	CTRL_CORE_MPU_IRQ_118_119[24:16]	114	EXT_SYS_IRQ_2	External interrupt (active low) via sys_nirq2 pin
MPU_IRQ_120 (ID152)	115	CTRL_CORE_MPU_IRQ_120_121[8:0]	115	KBD_IRQ	Keyboard controller interrupt
MPU_IRQ_121 (ID153)	116	CTRL_CORE_MPU_IRQ_120_121[24:16]	116	GPIO8_IRQ_1	GPIO8 interrupt 1
MPU_IRQ_122 (ID154)	117	CTRL_CORE_MPU_IRQ_122_123[8:0]	117	Reserved	Reserved by default but can be remapped to a valid interrupt source

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_123 (ID155)	118	CTRL_CORE_MPU_IRQ_122_123[24:16]	118	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_124 (ID156)	119	CTRL_CORE_MPU_IRQ_124_125[8:0]	119	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_125 (ID157)	120	CTRL_CORE_MPU_IRQ_124_125[24:16]	120	BB2D_IRQ	BB2D interrupt
MPU_IRQ_126 (ID158)	121	CTRL_CORE_MPU_IRQ_126_127[8:0]	121	CTRL_MODULE_CORE_IRQ_THERMAL_ALERT	CTRL_MODULE thermal alert interrupt
MPU_IRQ_127 (ID159)	122	CTRL_CORE_MPU_IRQ_126_127[24:16]	122	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_128 (ID160)	123	CTRL_CORE_MPU_IRQ_128_129[8:0]	123	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_129 (ID161)	124	CTRL_CORE_MPU_IRQ_128_129[24:16]	124	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_130 (ID162)	125	CTRL_CORE_MPU_IRQ_130_133[8:0]	125	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_131 (ID163)	N/A	N/A	N/A	MPU_CLUSTER_IRQ_PMU_C0	MPU core 0 PMU interrupt
MPU_IRQ_132 (ID164)	N/A	N/A	N/A	MPU_CLUSTER_IRQ_PMU_C1	MPU core 1 PMU interrupt
MPU_IRQ_133 (ID165)	126	CTRL_CORE_MPU_IRQ_130_133[24:16]	0	Reserved	Reserved by default but can be remapped to: • a valid interrupt source (through CTRL_CORE_MPU_IRQ_130_13[24:16]) • the nmin_dsp pin (through CTRL_CORE_NMI_DESTINATION_2[7:0] MPU). See Section 17.2, *Interrupt Controllers Environment* for details.
MPU_IRQ_134 (ID166)	127	CTRL_CORE_MPU_IRQ_134_135[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_135 (ID167)	128	CTRL_CORE_MPU_IRQ_134_135[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_136 (ID168)	129	CTRL_CORE_MPU_IRQ_136_137[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_137 (ID169)	130	CTRL_CORE_MPU_IRQ_136_137[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_138 (ID170)	131	CTRL_CORE_MPU_IRQ_138_139[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_139 (ID171)	N/A	N/A	N/A	WD_TIMER_MPU_C0_IRQ	MPU_WD_TIMER channel 0 timeout interrupt (watchdog reset)

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_140 (ID172)	N/A	N/A	N/A	WD_TIMER_MPU_C1_IRQ	MPU_WD_TIMER channel 1 timeout interrupt (watchdog reset)
MPU_IRQ_141 (ID173)	134	CTRL_CORE_MPU_IRQ_140_141[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_142 (ID174)	135	CTRL_CORE_MPU_IRQ_142_143[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_143 (ID175)	136	CTRL_CORE_MPU_IRQ_142_143[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_144 (ID176)	137	CTRL_CORE_MPU_IRQ_144_145[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_145 (ID177)	138	CTRL_CORE_MPU_IRQ_144_145[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_146 (ID178)	139	CTRL_CORE_MPU_IRQ_146_147[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_147 (ID179)	140	CTRL_CORE_MPU_IRQ_146_147[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_148 (ID180)	141	CTRL_CORE_MPU_IRQ_148_149[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_149 (ID181)	142	CTRL_CORE_MPU_IRQ_148_149[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_150 (ID182)	143	CTRL_CORE_MPU_IRQ_150_151[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_151 (ID183)	144	CTRL_CORE_MPU_IRQ_150_151[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_152 (ID184)	145	CTRL_CORE_MPU_IRQ_152_153[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_153 (ID185)	146	CTRL_CORE_MPU_IRQ_152_153[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_154 (ID186)	147	CTRL_CORE_MPU_IRQ_154_155[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_155 (ID187)	148	CTRL_CORE_MPU_IRQ_154_155[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_156 (ID188)	149	CTRL_CORE_MPU_IRQ_156_157[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_157 (ID189)	150	CTRL_CORE_MPU_IRQ_156_157[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
MPU_IRQ_158 (ID190)	151	CTRL_CORE_MPU_IRQ_158_159[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source

Table 17-2. MPU_INTC Default Interrupt Mapping (continued)

IRQ Input Line (GIC ID Number)[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
MPU_IRQ_159 (ID191)	152	CTRL_CORE_MPU_IRQ_158_159[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-2 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding MPU_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_MPU_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to MPU_INTC inputs. For example, the MPU_IRQ_4_7[8:0] bit field is used to configure which device interrupt would be mapped to the MPU_IRQ_4 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to MPU_IRQ_4 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the MPU subsystem. There is no IRQ_CROSSBAR dedicated to the associated MPU_INTC input line and therefore, the user cannot change its default mapping.

17.3.2 Interrupt Requests to DSP1_INTC

Table 17-3 lists the default interrupt sources for the DSP1_INTC. In addition, interrupts DSP1_IRQ_32 through DSP1_IRQ_95 can alternatively be sourced through the DSP's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_DSP1_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-3. DSP1_INTC Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_0	N/A	N/A	N/A	CGEM_IRQ_0	CGEM Internal Interrupt
DSP1_IRQ_1	N/A	N/A	N/A	CGEM_IRQ_1	CGEM Internal Interrupt
DSP1_IRQ_2	N/A	N/A	N/A	CGEM_IRQ_2	CGEM Internal Interrupt
DSP1_IRQ_3	N/A	N/A	N/A	CGEM_IRQ_3	CGEM Internal Interrupt
DSP1_IRQ_4	N/A	N/A	N/A	CGEM_IRQ_4	CGEM Internal Interrupt
DSP1_IRQ_5	N/A	N/A	N/A	CGEM_IRQ_5	CGEM Internal Interrupt
DSP1_IRQ_6	N/A	N/A	N/A	CGEM_IRQ_6	CGEM Internal Interrupt
DSP1_IRQ_7	N/A	N/A	N/A	CGEM_IRQ_7	CGEM Internal Interrupt
DSP1_IRQ_8	N/A	N/A	N/A	CGEM_IRQ_8	CGEM Internal Interrupt
DSP1_IRQ_9	N/A	N/A	N/A	CGEM_IRQ_9	CGEM Internal Interrupt
DSP1_IRQ_10	N/A	N/A	N/A	CGEM_IRQ_10	CGEM Internal Interrupt

Table 17-3. DSP1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_11	N/A	N/A	N/A	CGEM_IRQ_11	CGEM Internal Interrupt
DSP1_IRQ_12	N/A	N/A	N/A	CGEM_IRQ_12	CGEM Internal Interrupt
DSP1_IRQ_13	N/A	N/A	N/A	CGEM_IRQ_13	CGEM Internal Interrupt
DSP1_IRQ_14	N/A	N/A	N/A	CGEM_IRQ_14	CGEM Internal Interrupt
DSP1_IRQ_15	N/A	N/A	N/A	CGEM_IRQ_15	CGEM Internal Interrupt
DSP1_IRQ_16	N/A	N/A	N/A	TPCC_INTG	EDMA CC global interrupt
DSP1_IRQ_17	N/A	N/A	N/A	TPCC_INT0	EDMA CC region0 interrupt
DSP1_IRQ_18	N/A	N/A	N/A	TPCC_INT1	EDMA CC region1 interrupt
DSP1_IRQ_19	N/A	N/A	N/A	TPCC_INT2	EDMA CC region2 interrupt
DSP1_IRQ_20	N/A	N/A	N/A	TPCC_INT3	EDMA CC region3 interrupt
DSP1_IRQ_21	N/A	N/A	N/A	FW0_FUNC_ERROR	Firewall0 func access error
DSP1_IRQ_22	N/A	N/A	N/A	FW0_DEBUG_ERROR	Firewall0 debug access error
DSP1_IRQ_23	N/A	N/A	N/A	FW1_FUNC_ERROR	Firewall1 func access error
DSP1_IRQ_24	N/A	N/A	N/A	FW1_DEBUG_ERROR	Firewall1 debug access error
DSP1_IRQ_25	N/A	N/A	N/A	MMU0_INT	DSP MMU0 Interrupt
DSP1_IRQ_26	N/A	N/A	N/A	MMU1_INT	DSP MMU1 Interrupt
DSP1_IRQ_27	N/A	N/A	N/A	TPCC_ERRINT	EDMA CC error interrupt
DSP1_IRQ_28	N/A	N/A	N/A	TPTC_ERRINT0	EDMA TC0 error interrupt
DSP1_IRQ_29	N/A	N/A	N/A	TPTC_ERRINT1	EDMA TC1 error interrupt
DSP1_IRQ_30	N/A	N/A	N/A	NOC_ERRINT	Interconnect error interrupt
DSP1_IRQ_31	NA	N/A	N/A	EDMA_WAKE_INT	EDMA wakeup interrupt
DSP1_IRQ_32	1	CTRL_CORE_DSP1_IRQ_32_33[8:0]	1	ELM_IRQ	Error location process completion interrupt
DSP1_IRQ_33	2	CTRL_CORE_DSP1_IRQ_32_33[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
DSP1_IRQ_34	3	CTRL_CORE_DSP1_IRQ_34_35[8:0]	3	CTRL_MODULE_CORE_IRQ_SEC_EVTS	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3.
DSP1_IRQ_35	4	CTRL_CORE_DSP1_IRQ_34_35[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
DSP1_IRQ_36	5	CTRL_CORE_DSP1_IRQ_36_37[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
DSP1_IRQ_37	6	CTRL_CORE_DSP1_IRQ_36_37[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
DSP1_IRQ_38	7	CTRL_CORE_DSP1_IRQ_38_39[8:0]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
DSP1_IRQ_39	8	CTRL_CORE_DSP1_IRQ_38_39[24:16]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
DSP1_IRQ_40	9	CTRL_CORE_DSP1_IRQ_40_41[8:0]	9	DMA_SYSTEM_IRQ_2	System DMA interrupt 2
DSP1_IRQ_41	10	CTRL_CORE_DSP1_IRQ_40_41[24:16]	10	DMA_SYSTEM_IRQ_3	System DMA interrupt 3

Table 17-3. DSP1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_42	11	CTRL_CORE_DSP1_IRQ_42_43[8:0]	11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN statistic collector alarm interrupt
DSP1_IRQ_43	12	CTRL_CORE_DSP1_IRQ_42_43[24:16]	12	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_44	13	CTRL_CORE_DSP1_IRQ_44_45[8:0]	13	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_45	14	CTRL_CORE_DSP1_IRQ_44_45[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_46	15	CTRL_CORE_DSP1_IRQ_46_47[8:0]	15	GPMC_IRQ	GPMC interrupt
DSP1_IRQ_47	16	CTRL_CORE_DSP1_IRQ_46_47[24:16]	16	GPU_IRQ	GPU interrupt
DSP1_IRQ_48	17	CTRL_CORE_DSP1_IRQ_48_49[8:0]	17	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_49	18	CTRL_CORE_DSP1_IRQ_48_49[24:16]	18	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_50	19	CTRL_CORE_DSP1_IRQ_50_51[8:0]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_51	20	CTRL_CORE_DSP1_IRQ_50_51[24:16]	20	DISPC_IRQ	Display controller interrupt
DSP1_IRQ_52	21	CTRL_CORE_DSP1_IRQ_52_53[8:0]	21	MAILBOX1_IRQ_USER0	Mailbox 1 user 0 interrupt
DSP1_IRQ_53	22	CTRL_CORE_DSP1_IRQ_52_53[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_54	23	CTRL_CORE_DSP1_IRQ_54_55[8:0]	23	DSP1_IRQ_MMU0	DSP1 MMU0 interrupt
DSP1_IRQ_55	24	CTRL_CORE_DSP1_IRQ_54_55[24:16]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
DSP1_IRQ_56	25	CTRL_CORE_DSP1_IRQ_56_57[8:0]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
DSP1_IRQ_57	26	CTRL_CORE_DSP1_IRQ_56_57[24:16]	26	GPIO3_IRQ_1	GPIO3 interrupt 1
DSP1_IRQ_58	27	CTRL_CORE_DSP1_IRQ_58_59[8:0]	27	GPIO4_IRQ_1	GPIO4 interrupt 1
DSP1_IRQ_59	28	CTRL_CORE_DSP1_IRQ_58_59[24:16]	28	GPIO5_IRQ_1	GPIO5 interrupt 1
DSP1_IRQ_60	29	CTRL_CORE_DSP1_IRQ_60_61[8:0]	29	GPIO6_IRQ_1	GPIO6 interrupt 1
DSP1_IRQ_61	30	CTRL_CORE_DSP1_IRQ_60_61[24:16]	30	GPIO7_IRQ_1	GPIO7 interrupt 1
DSP1_IRQ_62	31	CTRL_CORE_DSP1_IRQ_62_63[8:0]	31	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_63	32	CTRL_CORE_DSP1_IRQ_62_63[24:16]	32	TIMER1_IRQ	TIMER1 interrupt
DSP1_IRQ_64	33	CTRL_CORE_DSP1_IRQ_64_65[8:0]	33	TIMER2_IRQ	TIMER2 interrupt
DSP1_IRQ_65	34	CTRL_CORE_DSP1_IRQ_64_65[24:16]	34	TIMER3_IRQ	TIMER3 interrupt
DSP1_IRQ_66	35	CTRL_CORE_DSP1_IRQ_66_67[8:0]	35	TIMER4_IRQ	TIMER4 interrupt
DSP1_IRQ_67	36	CTRL_CORE_DSP1_IRQ_66_67[24:16]	36	TIMER5_IRQ	TIMER5 interrupt

Table 17-3. DSP1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_68	37	CTRL_CORE_DSP1_IRQ_68_69[8:0]	37	TIMER6_IRQ	TIMER6 interrupt
DSP1_IRQ_69	38	CTRL_CORE_DSP1_IRQ_68_69[24:16]	38	TIMER7_IRQ	TIMER7 interrupt
DSP1_IRQ_70	39	CTRL_CORE_DSP1_IRQ_70_71[8:0]	39	TIMER8_IRQ	TIMER8 interrupt
DSP1_IRQ_71	40	CTRL_CORE_DSP1_IRQ_70_71[24:16]	40	TIMER9_IRQ	TIMER9 interrupt
DSP1_IRQ_72	41	CTRL_CORE_DSP1_IRQ_72_73[8:0]	41	TIMER10_IRQ	TIMER10 interrupt
DSP1_IRQ_73	42	CTRL_CORE_DSP1_IRQ_72_73[24:16]	42	TIMER11_IRQ	TIMER11 interrupt
DSP1_IRQ_74	43	CTRL_CORE_DSP1_IRQ_74_75[8:0]	43	MCSPI4_IRQ	McSPI4 interrupt
DSP1_IRQ_75	44	CTRL_CORE_DSP1_IRQ_74_75[24:16]	44	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_76	45	CTRL_CORE_DSP1_IRQ_76_77[8:0]	45	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_77	46	CTRL_CORE_DSP1_IRQ_76_77[24:16]	46	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_78	47	CTRL_CORE_DSP1_IRQ_78_79[8:0]	47	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_79	48	CTRL_CORE_DSP1_IRQ_78_79[24:16]	48	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_80	49	CTRL_CORE_DSP1_IRQ_80_81[8:0]	49	SATA_IRQ	SATA interrupt
DSP1_IRQ_81	50	CTRL_CORE_DSP1_IRQ_80_81[24:16]	50	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_82	51	CTRL_CORE_DSP1_IRQ_82_83[8:0]	51	I2C1_IRQ	I2C1 interrupt
DSP1_IRQ_83	52	CTRL_CORE_DSP1_IRQ_82_83[24:16]	52	I2C2_IRQ	I2C2 interrupt
DSP1_IRQ_84	53	CTRL_CORE_DSP1_IRQ_84_85[8:0]	53	HDQ1W_IRQ	HDQ1W interrupt
DSP1_IRQ_85	54	CTRL_CORE_DSP1_IRQ_84_85[24:16]	54	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_86	55	CTRL_CORE_DSP1_IRQ_86_87[8:0]	55	I2C5_IRQ	I2C5 interrupt
DSP1_IRQ_87	56	CTRL_CORE_DSP1_IRQ_86_87[24:16]	56	I2C3_IRQ	I2C3 interrupt
DSP1_IRQ_88	57	CTRL_CORE_DSP1_IRQ_88_89[8:0]	57	I2C4_IRQ	I2C4 interrupt
DSP1_IRQ_89	58	CTRL_CORE_DSP1_IRQ_88_89[24:16]	58	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_90	59	CTRL_CORE_DSP1_IRQ_90_91[8:0]	59	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_91	60	CTRL_CORE_DSP1_IRQ_90_91[24:16]	60	MCSPI1_IRQ	McSPI1 interrupt
DSP1_IRQ_92	61	CTRL_CORE_DSP1_IRQ_92_93[8:0]	61	MCSPI2_IRQ	McSPI2 interrupt

Table 17-3. DSP1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_93	62	CTRL_CORE_DSP1_IRQ_92_93[24:16]	62	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_94	63	CTRL_CORE_DSP1_IRQ_94_95[8:0]	63	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_95	64	CTRL_CORE_DSP1_IRQ_94_95[24:16]	64	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP1_IRQ_96	N/A	N/A	N/A	CGEM_IRQ_16	CGEM Internal Interrupt
DSP1_IRQ_97	N/A	N/A	N/A	CGEM_IRQ_17	CGEM Internal Interrupt
DSP1_IRQ_98	N/A	N/A	N/A	CGEM_IRQ_18	CGEM Internal Interrupt
DSP1_IRQ_99	NA	N/A	N/A	CGEM_IRQ_19	CGEM Internal Interrupt
DSP1_IRQ_100	N/A	N/A	N/A	CGEM_IRQ_20	CGEM Internal Interrupt
DSP1_IRQ_101	N/A	N/A	N/A	CGEM_IRQ_21	CGEM Internal Interrupt
DSP1_IRQ_102	N/A	N/A	N/A	CGEM_IRQ_22	CGEM Internal Interrupt
DSP1_IRQ_103	N/A	N/A	N/A	CGEM_IRQ_23	CGEM Internal Interrupt
DSP1_IRQ_104	N/A	N/A	N/A	CGEM_IRQ_24	CGEM Internal Interrupt
DSP1_IRQ_105	NA	N/A	N/A	CGEM_IRQ_25	CGEM Internal Interrupt
DSP1_IRQ_106	N/A	N/A	N/A	CGEM_IRQ_26	CGEM Internal Interrupt
DSP1_IRQ_107	N/A	N/A	N/A	CGEM_IRQ_27	CGEM Internal Interrupt
DSP1_IRQ_108	N/A	N/A	N/A	CGEM_IRQ_28	CGEM Internal Interrupt
DSP1_IRQ_109	N/A	N/A	N/A	CGEM_IRQ_29	CGEM Internal Interrupt
DSP1_IRQ_110	N/A	N/A	N/A	CGEM_IRQ_30	CGEM Internal Interrupt
DSP1_IRQ_111	N/A	N/A	N/A	CGEM_IRQ_31	CGEM Internal Interrupt
DSP1_IRQ_112	N/A	N/A	N/A	CGEM_IRQ_32	CGEM Internal Interrupt
DSP1_IRQ_113	N/A	N/A	N/A	CGEM_IRQ_33	CGEM Internal Interrupt
DSP1_IRQ_114	N/A	N/A	N/A	CGEM_IRQ_34	CGEM Internal Interrupt
DSP1_IRQ_115	N/A	N/A	N/A	CGEM_IRQ_35	CGEM Internal Interrupt
DSP1_IRQ_116	N/A	N/A	N/A	CGEM_IRQ_36	CGEM Internal Interrupt
DSP1_IRQ_117	N/A	N/A	N/A	CGEM_IRQ_37	CGEM Internal Interrupt
DSP1_IRQ_118	N/A	N/A	N/A	CGEM_IRQ_38	CGEM Internal Interrupt
DSP1_IRQ_119	NA	N/A	N/A	CGEM_IRQ_39	CGEM Internal Interrupt
DSP1_IRQ_120	N/A	N/A	N/A	CGEM_IRQ_40	CGEM Internal Interrupt
DSP1_IRQ_121	N/A	N/A	N/A	CGEM_IRQ_41	CGEM Internal Interrupt
DSP1_IRQ_122	N/A	N/A	N/A	CGEM_IRQ_42	CGEM Internal Interrupt

Table 17-3. DSP1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP1_IRQ_123	N/A	N/A	N/A	CGEM_IRQ_43	CGEM Internal Interrupt
DSP1_IRQ_124	N/A	N/A	N/A	CGEM_IRQ_44	CGEM Internal Interrupt
DSP1_IRQ_125	N/A	N/A	N/A	CGEM_IRQ_45	CGEM Internal Interrupt
DSP1_IRQ_126	N/A	N/A	N/A	CGEM_IRQ_46	CGEM Internal Interrupt
DSP1_IRQ_127	N/A	N/A	N/A	CGEM_IRQ_47	CGEM Internal Interrupt

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-3 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding DSP1_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_DSP1_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to DSP1_INTC inputs. For example, the DSP1_IRQ_32_33[8:0] bit field is used to configure which device interrupt would be mapped to the DSP1_IRQ_32 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to DSP1_IRQ_32 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the DSP1 subsystem. There is no IRQ_CROSSBAR dedicated to the associated DSP1_INTC input line and therefore, the user cannot change its default mapping.

17.3.3 Interrupt Requests to DSP2_INTC

Table 17-4 lists the default interrupt sources for the DSP2_INTC. In addition, interrupts DSP2_IRQ_32 through DSP2_IRQ_95 can alternatively be sourced through the DSP's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_DSP2_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-4. DSP2_INTC Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_0	N/A	N/A	N/A	CGEM_IRQ_0	CGEM Internal Interrupt
DSP2_IRQ_1	N/A	N/A	N/A	CGEM_IRQ_1	CGEM Internal Interrupt
DSP2_IRQ_2	N/A	N/A	N/A	CGEM_IRQ_2	CGEM Internal Interrupt
DSP2_IRQ_3	N/A	N/A	N/A	CGEM_IRQ_3	CGEM Internal Interrupt
DSP2_IRQ_4	N/A	N/A	N/A	CGEM_IRQ_4	CGEM Internal Interrupt
DSP2_IRQ_5	N/A	N/A	N/A	CGEM_IRQ_5	CGEM Internal Interrupt
DSP2_IRQ_6	N/A	N/A	N/A	CGEM_IRQ_6	CGEM Internal Interrupt

Table 17-4. DSP2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_7	N/A	N/A	N/A	CGEM_IRQ_7	CGEM Internal Interrupt
DSP2_IRQ_8	N/A	N/A	N/A	CGEM_IRQ_8	CGEM Internal Interrupt
DSP2_IRQ_9	N/A	N/A	N/A	CGEM_IRQ_9	CGEM Internal Interrupt
DSP2_IRQ_10	N/A	N/A	N/A	CGEM_IRQ_10	CGEM Internal Interrupt
DSP2_IRQ_11	N/A	N/A	N/A	CGEM_IRQ_11	CGEM Internal Interrupt
DSP2_IRQ_12	N/A	N/A	N/A	CGEM_IRQ_12	CGEM Internal Interrupt
DSP2_IRQ_13	N/A	N/A	N/A	CGEM_IRQ_13	CGEM Internal Interrupt
DSP2_IRQ_14	N/A	N/A	N/A	CGEM_IRQ_14	CGEM Internal Interrupt
DSP2_IRQ_15	N/A	N/A	N/A	CGEM_IRQ_15	CGEM Internal Interrupt
DSP2_IRQ_16	N/A	N/A	N/A	TPCC_INTG	EDMA CC global interrupt
DSP2_IRQ_17	N/A	N/A	N/A	TPCC_INT0	EDMA CC region0 interrupt
DSP2_IRQ_18	N/A	N/A	N/A	TPCC_INT1	EDMA CC region1 interrupt
DSP2_IRQ_19	N/A	N/A	N/A	TPCC_INT2	EDMA CC region2 interrupt
DSP2_IRQ_20	N/A	N/A	N/A	TPCC_INT3	EDMA CC region3 interrupt
DSP2_IRQ_21	N/A	N/A	N/A	FW0_FUNC_ERROR	Firewall0 func access error
DSP2_IRQ_22	N/A	N/A	N/A	FW0_DEBUG_ERROR	Firewall0 debug access error
DSP2_IRQ_23	N/A	N/A	N/A	FW1_FUNC_ERROR	Firewall1 func access error
DSP2_IRQ_24	N/A	N/A	N/A	FW1_DEBUG_ERROR	Firewall1 debug access error
DSP2_IRQ_25	N/A	N/A	N/A	MMU0_INT	DSP MMU0 Interrupt
DSP2_IRQ_26	N/A	N/A	N/A	MMU1_INT	DSP MMU1 Interrupt
DSP2_IRQ_27	N/A	N/A	N/A	TPCC_ERRINT	EDMA CC error interrupt
DSP2_IRQ_28	N/A	N/A	N/A	TPTC_ERRINT0	EDMA TC0 error interrupt
DSP2_IRQ_29	N/A	N/A	N/A	TPTC_ERRINT1	EDMA TC1 error interrupt
DSP2_IRQ_30	N/A	N/A	N/A	NOC_ERRINT	Interconnect error interrupt
DSP2_IRQ_31	NA	N/A	N/A	EDMA_WAKE_INT	EDMA wakeup interrupt
DSP2_IRQ_32	1	CTRL_CORE_DSP2_IRQ_32_33[8:0]	1	ELM_IRQ	Error location process completion interrupt
DSP2_IRQ_33	2	CTRL_CORE_DSP2_IRQ_32_33[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
DSP2_IRQ_34	3	CTRL_CORE_DSP2_IRQ_34_35[8:0]	3	CTRL_MODULE_CORE_IRQ_SEC_EVTS	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3.
DSP2_IRQ_35	4	CTRL_CORE_DSP2_IRQ_34_35[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
DSP2_IRQ_36	5	CTRL_CORE_DSP2_IRQ_36_37[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
DSP2_IRQ_37	6	CTRL_CORE_DSP2_IRQ_36_37[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU

Table 17-4. DSP2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_38	7	CTRL_CORE_DSP2_IRQ_38_39[8:0]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
DSP2_IRQ_39	8	CTRL_CORE_DSP2_IRQ_38_39[24:16]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
DSP2_IRQ_40	9	CTRL_CORE_DSP2_IRQ_40_41[8:0]	9	DMA_SYSTEM_IRQ_2	System DMA interrupt 2
DSP2_IRQ_41	10	CTRL_CORE_DSP2_IRQ_40_41[24:16]	10	DMA_SYSTEM_IRQ_3	System DMA interrupt 3
DSP2_IRQ_42	11	CTRL_CORE_DSP2_IRQ_42_43[8:0]	11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN statistic collector alarm interrupt
DSP2_IRQ_43	12	CTRL_CORE_DSP2_IRQ_42_43[24:16]	12	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_44	13	CTRL_CORE_DSP2_IRQ_44_45[8:0]	13	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_45	14	CTRL_CORE_DSP2_IRQ_44_45[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_46	15	CTRL_CORE_DSP2_IRQ_46_47[8:0]	15	GPMC_IRQ	GPMC interrupt
DSP2_IRQ_47	16	CTRL_CORE_DSP2_IRQ_46_47[24:16]	16	GPU_IRQ	GPU interrupt
DSP2_IRQ_48	17	CTRL_CORE_DSP2_IRQ_48_49[8:0]	17	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_49	18	CTRL_CORE_DSP2_IRQ_48_49[24:16]	18	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_50	19	CTRL_CORE_DSP2_IRQ_50_51[8:0]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_51	20	CTRL_CORE_DSP2_IRQ_50_51[24:16]	20	DISPC_IRQ	Display controller interrupt
DSP2_IRQ_52	21	CTRL_CORE_DSP2_IRQ_52_53[8:0]	21	MAILBOX1_IRQ_USER0	Mailbox 1 user 0 interrupt
DSP2_IRQ_53	22	CTRL_CORE_DSP2_IRQ_52_53[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_54	23	CTRL_CORE_DSP2_IRQ_54_55[8:0]	23	DSP2_IRQ_MMU0	DSP2 MMU0 interrupt
DSP2_IRQ_55	24	CTRL_CORE_DSP2_IRQ_54_55[24:16]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
DSP2_IRQ_56	25	CTRL_CORE_DSP2_IRQ_56_57[8:0]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
DSP2_IRQ_57	26	CTRL_CORE_DSP2_IRQ_56_57[24:16]	26	GPIO3_IRQ_1	GPIO3 interrupt 1
DSP2_IRQ_58	27	CTRL_CORE_DSP2_IRQ_58_59[8:0]	27	GPIO4_IRQ_1	GPIO4 interrupt 1
DSP2_IRQ_59	28	CTRL_CORE_DSP2_IRQ_58_59[24:16]	28	GPIO5_IRQ_1	GPIO5 interrupt 1
DSP2_IRQ_60	29	CTRL_CORE_DSP2_IRQ_60_61[8:0]	29	GPIO6_IRQ_1	GPIO6 interrupt 1
DSP2_IRQ_61	30	CTRL_CORE_DSP2_IRQ_60_61[24:16]	30	GPIO7_IRQ_1	GPIO7 interrupt 1
DSP2_IRQ_62	31	CTRL_CORE_DSP2_IRQ_62_63[8:0]	31	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_63	32	CTRL_CORE_DSP2_IRQ_62_63[24:16]	32	TIMER1_IRQ	TIMER1 interrupt

Table 17-4. DSP2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_64	33	CTRL_CORE_DSP2_IRQ_64_65[8:0]	33	TIMER2_IRQ	TIMER2 interrupt
DSP2_IRQ_65	34	CTRL_CORE_DSP2_IRQ_64_65[24:16]	34	TIMER3_IRQ	TIMER3 interrupt
DSP2_IRQ_66	35	CTRL_CORE_DSP2_IRQ_66_67[8:0]	35	TIMER4_IRQ	TIMER4 interrupt
DSP2_IRQ_67	36	CTRL_CORE_DSP2_IRQ_66_67[24:16]	36	TIMER5_IRQ	TIMER5 interrupt
DSP2_IRQ_68	37	CTRL_CORE_DSP2_IRQ_68_69[8:0]	37	TIMER6_IRQ	TIMER6 interrupt
DSP2_IRQ_69	38	CTRL_CORE_DSP2_IRQ_68_69[24:16]	38	TIMER7_IRQ	TIMER7 interrupt
DSP2_IRQ_70	39	CTRL_CORE_DSP2_IRQ_70_71[8:0]	39	TIMER8_IRQ	TIMER8 interrupt
DSP2_IRQ_71	40	CTRL_CORE_DSP2_IRQ_70_71[24:16]	40	TIMER9_IRQ	TIMER9 interrupt
DSP2_IRQ_72	41	CTRL_CORE_DSP2_IRQ_72_73[8:0]	41	TIMER10_IRQ	TIMER10 interrupt
DSP2_IRQ_73	42	CTRL_CORE_DSP2_IRQ_72_73[24:16]	42	TIMER11_IRQ	TIMER11 interrupt
DSP2_IRQ_74	43	CTRL_CORE_DSP2_IRQ_74_75[8:0]	43	MCSPI4_IRQ	McSPI4 interrupt
DSP2_IRQ_75	44	CTRL_CORE_DSP2_IRQ_74_75[24:16]	44	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_76	45	CTRL_CORE_DSP2_IRQ_76_77[8:0]	45	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_77	46	CTRL_CORE_DSP2_IRQ_76_77[24:16]	46	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_78	47	CTRL_CORE_DSP2_IRQ_78_79[8:0]	47	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_79	48	CTRL_CORE_DSP2_IRQ_78_79[24:16]	48	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_80	49	CTRL_CORE_DSP2_IRQ_80_81[8:0]	49	SATA_IRQ	SATA interrupt
DSP2_IRQ_81	50	CTRL_CORE_DSP2_IRQ_80_81[24:16]	50	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_82	51	CTRL_CORE_DSP2_IRQ_82_83[8:0]	51	I2C1_IRQ	I2C1 interrupt
DSP2_IRQ_83	52	CTRL_CORE_DSP2_IRQ_82_83[24:16]	52	I2C2_IRQ	I2C2 interrupt
DSP2_IRQ_84	53	CTRL_CORE_DSP2_IRQ_84_85[8:0]	53	HDQ1W_IRQ	HDQ1W interrupt
DSP2_IRQ_85	54	CTRL_CORE_DSP2_IRQ_84_85[24:16]	54	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_86	55	CTRL_CORE_DSP2_IRQ_86_87[8:0]	55	I2C5_IRQ	I2C5 interrupt
DSP2_IRQ_87	56	CTRL_CORE_DSP2_IRQ_86_87[24:16]	56	I2C3_IRQ	I2C3 interrupt
DSP2_IRQ_88	57	CTRL_CORE_DSP2_IRQ_88_89[8:0]	57	I2C4_IRQ	I2C4 interrupt
DSP2_IRQ_89	58	CTRL_CORE_DSP2_IRQ_88_89[24:16]	58	Reserved	Reserved by default but can be remapped to a valid interrupt source

Table 17-4. DSP2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_90	59	CTRL_CORE_DSP2_IRQ_90_91[8:0]	59	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_91	60	CTRL_CORE_DSP2_IRQ_90_91[24:16]	60	MCSPI1_IRQ	McSPI1 interrupt
DSP2_IRQ_92	61	CTRL_CORE_DSP2_IRQ_92_93[8:0]	61	MCSPI2_IRQ	McSPI2 interrupt
DSP2_IRQ_93	62	CTRL_CORE_DSP2_IRQ_92_93[24:16]	62	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_94	63	CTRL_CORE_DSP2_IRQ_94_95[8:0]	63	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_95	64	CTRL_CORE_DSP2_IRQ_94_95[24:16]	64	Reserved	Reserved by default but can be remapped to a valid interrupt source
DSP2_IRQ_96	N/A	N/A	N/A	CGEM_IRQ_16	CGEM Internal Interrupt
DSP2_IRQ_97	N/A	N/A	N/A	CGEM_IRQ_17	CGEM Internal Interrupt
DSP2_IRQ_98	N/A	N/A	N/A	CGEM_IRQ_18	CGEM Internal Interrupt
DSP2_IRQ_99	NA	N/A	N/A	CGEM_IRQ_19	CGEM Internal Interrupt
DSP2_IRQ_100	N/A	N/A	N/A	CGEM_IRQ_20	CGEM Internal Interrupt
DSP2_IRQ_101	N/A	N/A	N/A	CGEM_IRQ_21	CGEM Internal Interrupt
DSP2_IRQ_102	N/A	N/A	N/A	CGEM_IRQ_22	CGEM Internal Interrupt
DSP2_IRQ_103	N/A	N/A	N/A	CGEM_IRQ_23	CGEM Internal Interrupt
DSP2_IRQ_104	N/A	N/A	N/A	CGEM_IRQ_24	CGEM Internal Interrupt
DSP2_IRQ_105	NA	N/A	N/A	CGEM_IRQ_25	CGEM Internal Interrupt
DSP2_IRQ_106	N/A	N/A	N/A	CGEM_IRQ_26	CGEM Internal Interrupt
DSP2_IRQ_107	N/A	N/A	N/A	CGEM_IRQ_27	CGEM Internal Interrupt
DSP2_IRQ_108	N/A	N/A	N/A	CGEM_IRQ_28	CGEM Internal Interrupt
DSP2_IRQ_109	N/A	N/A	N/A	CGEM_IRQ_29	CGEM Internal Interrupt
DSP2_IRQ_110	N/A	N/A	N/A	CGEM_IRQ_30	CGEM Internal Interrupt
DSP2_IRQ_111	N/A	N/A	N/A	CGEM_IRQ_31	CGEM Internal Interrupt
DSP2_IRQ_112	N/A	N/A	N/A	CGEM_IRQ_32	CGEM Internal Interrupt
DSP2_IRQ_113	N/A	N/A	N/A	CGEM_IRQ_33	CGEM Internal Interrupt
DSP2_IRQ_114	N/A	N/A	N/A	CGEM_IRQ_34	CGEM Internal Interrupt
DSP2_IRQ_115	N/A	N/A	N/A	CGEM_IRQ_35	CGEM Internal Interrupt
DSP2_IRQ_116	N/A	N/A	N/A	CGEM_IRQ_36	CGEM Internal Interrupt
DSP2_IRQ_117	N/A	N/A	N/A	CGEM_IRQ_37	CGEM Internal Interrupt
DSP2_IRQ_118	N/A	N/A	N/A	CGEM_IRQ_38	CGEM Internal Interrupt

Table 17-4. DSP2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
DSP2_IRQ_119	NA	N/A	N/A	CGEM_IRQ_39	CGEM Internal Interrupt
DSP2_IRQ_120	N/A	N/A	N/A	CGEM_IRQ_40	CGEM Internal Interrupt
DSP2_IRQ_121	N/A	N/A	N/A	CGEM_IRQ_41	CGEM Internal Interrupt
DSP2_IRQ_122	N/A	N/A	N/A	CGEM_IRQ_42	CGEM Internal Interrupt
DSP2_IRQ_123	N/A	N/A	N/A	CGEM_IRQ_43	CGEM Internal Interrupt
DSP2_IRQ_124	N/A	N/A	N/A	CGEM_IRQ_44	CGEM Internal Interrupt
DSP2_IRQ_125	N/A	N/A	N/A	CGEM_IRQ_45	CGEM Internal Interrupt
DSP2_IRQ_126	N/A	N/A	N/A	CGEM_IRQ_46	CGEM Internal Interrupt
DSP2_IRQ_127	N/A	N/A	N/A	CGEM_IRQ_47	CGEM Internal Interrupt

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-4 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding DSP2_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_DSP2_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to DSP2_INTC inputs. For example, the DSP2_IRQ_32_33[8:0] bit field is used to configure which device interrupt would be mapped to the DSP2_IRQ_32 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to DSP2_IRQ_32 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the DSP2 subsystem. There is no IRQ_CROSSBAR dedicated to the associated DSP2_INTC input line and therefore, the user cannot change its default mapping.

17.3.4 Interrupt Requests to IPU1_Cx_INTC

Table 17-5 lists the default interrupt sources for the IPU1_Cx_INTC. In addition, device interrupts IPU1_IRQ_23 through IPU1_IRQ_79 can alternatively be sourced through the IPU1's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_IPU1_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-5. IPU1_Cx_INTC Default Interrupt Mapping

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU1_IRQ_0	N/A	N/A	N/A	Reserved	MSP initial value in exception vector table
IPU1_IRQ_1	N/A	N/A	N/A	RESET_IRQ	Reset

(1) This column shows the number of the corresponding exception type.

Table 17-5. IPU1_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU1_IRQ_2	N/A	N/A	N/A	NMI_IRQ	External NMI input (interrupt from nmin_dsp device pad)
IPU1_IRQ_3	N/A	N/A	N/A	HARD_FAULT_IRQ	All fault conditions, if the fault handle is not enabled
IPU1_IRQ_4	N/A	N/A	N/A	MEM_MANAGE_FAULT_IRQ	Memory management fault; access to illegal locations
IPU1_IRQ_5	N/A	N/A	N/A	BUS_FAULT_IRQ	Bus error (on AHB intf)
IPU1_IRQ_6	N/A	N/A	N/A	USAGE_FAULT_IRQ	Program error
IPU1_IRQ_7	N/A	N/A	N/A	Reserved	Reserved
IPU1_IRQ_8	N/A	N/A	N/A	Reserved	Reserved
IPU1_IRQ_9	NA	N/A	N/A	Reserved	Reserved
IPU1_IRQ_10	N/A	N/A	N/A	Reserved	Reserved
IPU1_IRQ_11	N/A	N/A	N/A	SV_CALL_IRQ	Service system Call
IPU1_IRQ_12	N/A	N/A	N/A	DEBUG_MON_IRQ	BP, WP or external debug req.
IPU1_IRQ_13	N/A	N/A	N/A	Reserved	Reserved
IPU1_IRQ_14	N/A	N/A	N/A	PEND_SV_IRQ	Pendable request for system device
IPU1_IRQ_15	N/A	N/A	N/A	SYS_TICK_TIMER_IRQ	System Tick Timer
IPU1_IRQ_16	N/A	N/A	N/A	XLATE_MMU_FAULT_IRQ	xlate_mmu_fault (from L2 MMU)
IPU1_IRQ_17	N/A	N/A	N/A	UNICACHE_MMU_IRQ	Unicache or MMU maintenance complete
IPU1_IRQ_18	N/A	N/A	N/A	CTM_TIM_EVENT1_IRQ	CTM timer event (timer #1)
IPU1_IRQ_19	N/A	N/A	N/A	HWSEM_M4_IRQ	Semaphore interrupt (1 to each core)
IPU1_IRQ_20	N/A	N/A	N/A	ICE_NEMU_IRQ	ICECrusher (1 to each core)
IPU1_IRQ_21	N/A	N/A	N/A	IPU_IMP_FAULT_IRQ	Ducati imprecise fault (from interconnect)
IPU1_IRQ_22	N/A	N/A	N/A	CTM_TIM_EVENT2_IRQ	CTM timer event (timer #2)
IPU1_IRQ_23	1	CTRL_CORE_IPU1_IRQ_23_24[8:0]	20	DISPC_IRQ	Display controller interrupt
IPU1_IRQ_24	2	CTRL_CORE_IPU1_IRQ_23_24[24:16]	48	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_25	3	CTRL_CORE_IPU1_IRQ_25_26[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_26	4	CTRL_CORE_IPU1_IRQ_25_26[24:16]	96	HDMI_IRQ	HDMI interrupt
IPU1_IRQ_27	5	CTRL_CORE_IPU1_IRQ_27_28[8:0]	126	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_28	6	CTRL_CORE_IPU1_IRQ_27_28[24:16]	127	Reserved	Reserved by default but can be remapped to a valid interrupt source

Table 17-5. IPU1_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU1_IRQ_29	7	CTRL_CORE_IPU1_IRQ_29_30[8:0]	128	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_30	8	CTRL_CORE_IPU1_IRQ_29_30[24:16]	129	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_31	9	CTRL_CORE_IPU1_IRQ_31_32[8:0]	130	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_32	10	CTRL_CORE_IPU1_IRQ_31_32[24:16]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_33	11	CTRL_CORE_IPU1_IRQ_33_34[8:0]	131	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_34	12	CTRL_CORE_IPU1_IRQ_33_34[24:16]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
IPU1_IRQ_35	13	CTRL_CORE_IPU1_IRQ_35_36[8:0]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
IPU1_IRQ_36	14	CTRL_CORE_IPU1_IRQ_35_36[24:16]	9	DMA_SYSTEM_IRQ_2	System DMA interrupt 2
IPU1_IRQ_37	15	CTRL_CORE_IPU1_IRQ_37_38[8:0]	10	DMA_SYSTEM_IRQ_3	System DMA interrupt 3
IPU1_IRQ_38	16	CTRL_CORE_IPU1_IRQ_37_38[24:16]	132	IVA_IRQ_MAILBOX_2	IVA mailbox user 2 interrupt
IPU1_IRQ_39	17	CTRL_CORE_IPU1_IRQ_39_40[8:0]	98	IVA_IRQ_SYNC_1	IVA ICONT2 sync interrupt
IPU1_IRQ_40	18	CTRL_CORE_IPU1_IRQ_39_40[24:16]	99	IVA_IRQ_SYNC_0	IVA ICONT1 sync interrupt
IPU1_IRQ_41	19	CTRL_CORE_IPU1_IRQ_41_42[8:0]	51	I2C1_IRQ	I2C1 interrupt
IPU1_IRQ_42	20	CTRL_CORE_IPU1_IRQ_41_42[24:16]	52	I2C2_IRQ	I2C2 interrupt
IPU1_IRQ_43	21	CTRL_CORE_IPU1_IRQ_43_44[8:0]	56	I2C3_IRQ	I2C3 interrupt
IPU1_IRQ_44	22	CTRL_CORE_IPU1_IRQ_43_44[24:16]	57	I2C4_IRQ	I2C4 interrupt
IPU1_IRQ_45	23	CTRL_CORE_IPU1_IRQ_45_46[8:0]	69	UART3_IRQ	UART3 interrupt
IPU1_IRQ_46	24	CTRL_CORE_IPU1_IRQ_45_46[24:16]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
IPU1_IRQ_47	25	CTRL_CORE_IPU1_IRQ_47_48[8:0]	133	PRM_IRQ_IPU1	PRCM interrupt to IPU1
IPU1_IRQ_48	26	CTRL_CORE_IPU1_IRQ_47_48[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_49	27	CTRL_CORE_IPU1_IRQ_49_50[8:0]	66	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_50	28	CTRL_CORE_IPU1_IRQ_49_50[24:16]	134	MAILBOX1_IRQ_USER2	Mailbox 1 user 2 interrupt
IPU1_IRQ_51	29	CTRL_CORE_IPU1_IRQ_51_52[8:0]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
IPU1_IRQ_52	30	CTRL_CORE_IPU1_IRQ_51_52[24:16]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
IPU1_IRQ_53	31	CTRL_CORE_IPU1_IRQ_53_54[8:0]	34	TIMER3_IRQ	TIMER3 interrupt
IPU1_IRQ_54	32	CTRL_CORE_IPU1_IRQ_53_54[24:16]	35	TIMER4_IRQ	TIMER4 interrupt
IPU1_IRQ_55	33	CTRL_CORE_IPU1_IRQ_55_56[8:0]	40	TIMER9_IRQ	TIMER9 interrupt

Table 17-5. IPU1_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU1_IRQ_56	34	CTRL_CORE_IPU1_IRQ_55_56[24:16]	42	TIMER11_IRQ	TIMER11 interrupt
IPU1_IRQ_57	35	CTRL_CORE_IPU1_IRQ_57_58[8:0]	60	MCSPI1_IRQ	McSPI1 interrupt
IPU1_IRQ_58	36	CTRL_CORE_IPU1_IRQ_57_58[24:16]	61	MCSPI2_IRQ	McSPI2 interrupt
IPU1_IRQ_59	37	CTRL_CORE_IPU1_IRQ_59_60[8:0]	50	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_60	38	CTRL_CORE_IPU1_IRQ_59_60[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_61	39	CTRL_CORE_IPU1_IRQ_61_62[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_62	40	CTRL_CORE_IPU1_IRQ_61_62[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_63	41	CTRL_CORE_IPU1_IRQ_63_64[8:0]	83	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_64	42	CTRL_CORE_IPU1_IRQ_63_64[24:16]	108	DMM_IRQ	DMM interrupt
IPU1_IRQ_65	43	CTRL_CORE_IPU1_IRQ_65_66[8:0]	120	BB2D_IRQ	BB2D interrupt
IPU1_IRQ_66	44	CTRL_CORE_IPU1_IRQ_65_66[24:16]	78	MMC1_IRQ	MMC1 interrupt
IPU1_IRQ_67	45	CTRL_CORE_IPU1_IRQ_67_68[8:0]	81	MMC2_IRQ	MMC2 interrupt
IPU1_IRQ_68	46	CTRL_CORE_IPU1_IRQ_67_68[24:16]	89	MMC3_IRQ	MMC3 interrupt
IPU1_IRQ_69	47	CTRL_CORE_IPU1_IRQ_69_70[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_70	48	CTRL_CORE_IPU1_IRQ_69_70[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_71	49	CTRL_CORE_IPU1_IRQ_71_72[8:0]	119	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_72	50	CTRL_CORE_IPU1_IRQ_71_72[24:16]	118	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_73	51	CTRL_CORE_IPU1_IRQ_73_74[8:0]	72	USB1_IRQ_INTR1	USB1 interrupt 1
IPU1_IRQ_74	52	CTRL_CORE_IPU1_IRQ_73_74[24:16]	73	USB2_IRQ_INTR0	USB2 interrupt 0
IPU1_IRQ_75	53	CTRL_CORE_IPU1_IRQ_75_76[8:0]	117	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU1_IRQ_76	54	CTRL_CORE_IPU1_IRQ_75_76[24:16]	87	USB2_IRQ_INTR1	USB2 interrupt 1
IPU1_IRQ_77	55	CTRL_CORE_IPU1_IRQ_77_78[8:0]	88	USB3_IRQ_INTR0[2]	USB3 interrupt 0
IPU1_IRQ_78	56	CTRL_CORE_IPU1_IRQ_77_78[24:16]	62	Reserved	Reserved by default but can be remapped to a valid interrupt source

(2) USB3 is not supported in this family of devices.

Table 17-5. IPU1_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU1_IRQ_79	57	CTRL_CORE_IPU1_IRQ_79_80[8:0]	63	Reserved	Reserved by default but can be remapped to a valid interrupt source

NOTE: Exceptions/interrupts IPU1_IRQ_[15:0] are all internal to the Cortex-M4 core. Exceptions/interrupts IPU1_IRQ_[79:16] are all external to the Cortex-M4 core – that is, the first Cortex-M4 external interrupt is mapped to IPU1_IRQ_16 (exception #16), and the last (sixty-fourth) Cortex-M4 external interrupt is mapped to IPU1_IRQ_79 (exception #79).

For more information about Cortex-M4 exception types, refer to ARM Cortex®-M4 Devices Generic User Guide (available at http://infocenter.arm.com/help/index.jsp).

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-5 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding IPU1_Cx_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_IPU1_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to IPU1_Cx_INTC inputs. For example, the IPU1_IRQ_23_24[8:0] bit field is used to configure which device interrupt would be mapped to the IPU1_IRQ_23 line. The reset value of this bit field is 0x14, meaning that DISPC_IRQ would be mapped to IPU1_IRQ_23 by default because it is connected to the IRQ_CROSSBAR_20 input.

'N/A' in this column means that the corresponding interrupt is internal to the IPU1 subsystem. There is no IRQ_CROSSBAR dedicated to the associated IPU1_Cx_INTC input line and therefore, the user cannot change its default mapping.

The CTRL_CORE_IPU1_IRQ_y_z registers control the IRQ_CROSSBAR settings for both NVICs in the IPU1 subsystem. That is, it is not possible to map different interrupts to the same interrupt input of the NVICs in IPU1.

17.3.5 Interrupt Requests to IPU2_Cx_INTC

NOTE: IPU2 subsystem is dedicated to IVA-HD support and is not available for other processing.

Table 17-6 lists the default interrupt sources for the IPU2_Cx_INTC. In addition, device interrupts IPU2_IRQ_23 through IPU2_IRQ_79 can alternatively be sourced through the IPU2's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_IPU2_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-6. IPU2_Cx_INTC Default Interrupt Mapping

IRQ Input Line[1]	IRQ_CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU2_IRQ_0	N/A	N/A	N/A	Reserved	MSP initial value in exception vector table
IPU2_IRQ_1	N/A	N/A	N/A	RESET_IRQ	Reset
IPU2_IRQ_2	N/A	N/A	N/A	NMI_IRQ	External NMI input (interrupt from nmin_dsp device pad)
IPU2_IRQ_3	N/A	N/A	N/A	HARD_FAULT_IRQ	All fault conditions, if the fault handle is not enabled
IPU2_IRQ_4	N/A	N/A	N/A	MEM_MANAGE_FAULT_IRQ	Memory management fault; access to illegal locations
IPU2_IRQ_5	N/A	N/A	N/A	BUS_FAULT_IRQ	Bus error (on AHB intf)
IPU2_IRQ_6	N/A	N/A	N/A	USAGE_FAULT_IRQ	Program error
IPU2_IRQ_7	N/A	N/A	N/A	Reserved	Reserved
IPU2_IRQ_8	N/A	N/A	N/A	Reserved	Reserved
IPU2_IRQ_9	NA	N/A	N/A	Reserved	Reserved
IPU2_IRQ_10	N/A	N/A	N/A	Reserved	Reserved
IPU2_IRQ_11	N/A	N/A	N/A	SV_CALL_IRQ	Service system Call
IPU2_IRQ_12	N/A	N/A	N/A	DEBUG_MON_IRQ	BP, WP or external debug req.
IPU2_IRQ_13	N/A	N/A	N/A	Reserved	Reserved
IPU2_IRQ_14	N/A	N/A	N/A	PEND_SV_IRQ	Pendable request for system device
IPU2_IRQ_15	N/A	N/A	N/A	SYS_TICK_TIMER_IRQ	System Tick Timer
IPU2_IRQ_16	N/A	N/A	N/A	XLATE_MMU_FAULT_IRQ	xlate_mmu_fault (from L2 MMU)
IPU2_IRQ_17	N/A	N/A	N/A	UNICACHE_MMU_IRQ	Unicache or MMU maintenance complete
IPU2_IRQ_18	N/A	N/A	N/A	CTM_TIM_EVENT1_IRQ	CTM timer event (timer #1)
IPU2_IRQ_19	N/A	N/A	N/A	HWSEM_M4_IRQ	Semaphore interrupt (1 to each core)
IPU2_IRQ_20	N/A	N/A	N/A	ICE_NEMU_IRQ	ICECrusher (1 to each core)
IPU2_IRQ_21	N/A	N/A	N/A	IPU_IMP_FAULT_IRQ	Ducati imprecise fault (from interconnect)
IPU2_IRQ_22	N/A	N/A	N/A	CTM_TIM_EVENT2_IRQ	CTM timer event (timer #2)
IPU2_IRQ_23	1	CTRL_CORE_IPU2_IRQ_23_24[8:0]	20	DISPC_IRQ	Display controller interrupt
IPU2_IRQ_24	2	CTRL_CORE_IPU2_IRQ_23_24[24:16]	48	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_25	3	CTRL_CORE_IPU2_IRQ_25_26[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_26	4	CTRL_CORE_IPU2_IRQ_25_26[24:16]	96	HDMI_IRQ	HDMI interrupt

(1) This column shows the number of the corresponding exception type.

Table 17-6. IPU2_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU2_IRQ_27	5	CTRL_CORE_IPU2_IRQ_27_28[8:0]	126	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_28	6	CTRL_CORE_IPU2_IRQ_27_28[24:16]	127	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_29	7	CTRL_CORE_IPU2_IRQ_29_30[8:0]	128	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_30	8	CTRL_CORE_IPU2_IRQ_29_30[24:16]	129	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_31	9	CTRL_CORE_IPU2_IRQ_31_32[8:0]	130	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_32	10	CTRL_CORE_IPU2_IRQ_31_32[24:16]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_33	11	CTRL_CORE_IPU2_IRQ_33_34[8:0]	131	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_34	12	CTRL_CORE_IPU2_IRQ_33_34[24:16]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
IPU2_IRQ_35	13	CTRL_CORE_IPU2_IRQ_35_36[8:0]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
IPU2_IRQ_36	14	CTRL_CORE_IPU2_IRQ_35_36[24:16]	9	DMA_SYSTEM_IRQ_2	System DMA interrupt 2
IPU2_IRQ_37	15	CTRL_CORE_IPU2_IRQ_37_38[8:0]	10	DMA_SYSTEM_IRQ_3	System DMA interrupt 3
IPU2_IRQ_38	16	CTRL_CORE_IPU2_IRQ_37_38[24:16]	132	IVA_IRQ_MAILBOX_2	IVA mailbox user 2 interrupt
IPU2_IRQ_39	17	CTRL_CORE_IPU2_IRQ_39_40[8:0]	98	IVA_IRQ_SYNC_1	IVA ICONT2 sync interrupt
IPU2_IRQ_40	18	CTRL_CORE_IPU2_IRQ_39_40[24:16]	99	IVA_IRQ_SYNC_0	IVA ICONT1 sync interrupt
IPU2_IRQ_41	19	CTRL_CORE_IPU2_IRQ_41_42[8:0]	51	I2C1_IRQ	I2C1 interrupt
IPU2_IRQ_42	20	CTRL_CORE_IPU2_IRQ_41_42[24:16]	52	I2C2_IRQ	I2C2 interrupt
IPU2_IRQ_43	21	CTRL_CORE_IPU2_IRQ_43_44[8:0]	56	I2C3_IRQ	I2C3 interrupt
IPU2_IRQ_44	22	CTRL_CORE_IPU2_IRQ_43_44[24:16]	57	I2C4_IRQ	I2C4 interrupt
IPU2_IRQ_45	23	CTRL_CORE_IPU2_IRQ_45_46[8:0]	69	UART3_IRQ	UART3 interrupt
IPU2_IRQ_46	24	CTRL_CORE_IPU2_IRQ_45_46[24:16]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
IPU2_IRQ_47	25	CTRL_CORE_IPU2_IRQ_47_48[8:0]	133	PRM_IRQ_IPU2	PRCM interrupt to IPU1
IPU2_IRQ_48	26	CTRL_CORE_IPU2_IRQ_47_48[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_49	27	CTRL_CORE_IPU2_IRQ_49_50[8:0]	66	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_50	28	CTRL_CORE_IPU2_IRQ_49_50[24:16]	134	MAILBOX1_IRQ_USER2	Mailbox 1 user 2 interrupt
IPU2_IRQ_51	29	CTRL_CORE_IPU2_IRQ_51_52[8:0]	24	GPIO1_IRQ_1	GPIO1 interrupt 1

Table 17-6. IPU2_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[(1)]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU2_IRQ_52	30	CTRL_CORE_IPU2_IRQ_51_52[24:16]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
IPU2_IRQ_53	31	CTRL_CORE_IPU2_IRQ_53_54[8:0]	34	TIMER3_IRQ	TIMER3 interrupt
IPU2_IRQ_54	32	CTRL_CORE_IPU2_IRQ_53_54[24:16]	35	TIMER4_IRQ	TIMER4 interrupt
IPU2_IRQ_55	33	CTRL_CORE_IPU2_IRQ_55_56[8:0]	40	TIMER9_IRQ	TIMER9 interrupt
IPU2_IRQ_56	34	CTRL_CORE_IPU2_IRQ_55_56[24:16]	42	TIMER11_IRQ	TIMER11 interrupt
IPU2_IRQ_57	35	CTRL_CORE_IPU2_IRQ_57_58[8:0]	60	MCSPI1_IRQ	McSPI1 interrupt
IPU2_IRQ_58	36	CTRL_CORE_IPU2_IRQ_57_58[24:16]	61	MCSPI2_IRQ	McSPI2 interrupt
IPU2_IRQ_59	37	CTRL_CORE_IPU2_IRQ_59_60[8:0]	50	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_60	38	CTRL_CORE_IPU2_IRQ_59_60[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_61	39	CTRL_CORE_IPU2_IRQ_61_62[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_62	40	CTRL_CORE_IPU2_IRQ_61_62[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_63	41	CTRL_CORE_IPU2_IRQ_63_64[8:0]	83	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_64	42	CTRL_CORE_IPU2_IRQ_63_64[24:16]	108	DMM_IRQ	DMM interrupt
IPU2_IRQ_65	43	CTRL_CORE_IPU2_IRQ_65_66[8:0]	120	BB2D_IRQ	BB2D interrupt
IPU2_IRQ_66	44	CTRL_CORE_IPU2_IRQ_65_66[24:16]	78	MMC1_IRQ	MMC1 interrupt
IPU2_IRQ_67	45	CTRL_CORE_IPU2_IRQ_67_68[8:0]	81	MMC2_IRQ	MMC2 interrupt
IPU2_IRQ_68	46	CTRL_CORE_IPU2_IRQ_67_68[24:16]	89	MMC3_IRQ	MMC3 interrupt
IPU2_IRQ_69	47	CTRL_CORE_IPU2_IRQ_69_70[8:0]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_70	48	CTRL_CORE_IPU2_IRQ_69_70[24:16]	0	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_71	49	CTRL_CORE_IPU2_IRQ_71_72[8:0]	119	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_72	50	CTRL_CORE_IPU2_IRQ_71_72[24:16]	118	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_73	51	CTRL_CORE_IPU2_IRQ_73_74[8:0]	72	USB1_IRQ_INTR1	USB1 interrupt 1
IPU2_IRQ_74	52	CTRL_CORE_IPU2_IRQ_73_74[24:16]	73	USB2_IRQ_INTR0	USB2 interrupt 0
IPU2_IRQ_75	53	CTRL_CORE_IPU2_IRQ_75_76[8:0]	117	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_76	54	CTRL_CORE_IPU2_IRQ_75_76[24:16]	87	USB2_IRQ_INTR1	USB2 interrupt 1

Table 17-6. IPU2_Cx_INTC Default Interrupt Mapping (continued)

IRQ Input Line[1]	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
IPU2_IRQ_77	55	CTRL_CORE_IPU2_IRQ_77_78[8:0]	88	USB3_IRQ_INTR0[2]	USB3 interrupt 0
IPU2_IRQ_78	56	CTRL_CORE_IPU2_IRQ_77_78[24:16]	62	Reserved	Reserved by default but can be remapped to a valid interrupt source
IPU2_IRQ_79	57	CTRL_CORE_IPU2_IRQ_79_80[8:0]	63	Reserved	Reserved by default but can be remapped to a valid interrupt source

(2) USB3 is not supported in this family of devices.

NOTE: Exceptions/interrupts IPU2_IRQ_[15:0] are all internal to the Cortex-M4 core. Exceptions/interrupts IPU2_IRQ_[79:16] are all external to the Cortex-M4 core – that is, the first Cortex-M4 external interrupt is mapped to IPU2_IRQ_16 (exception #16), and the last (sixty-fourth) Cortex-M4 external interrupt is mapped to IPU2_IRQ_79 (exception #79).

For more information about Cortex-M4 exception types, refer to ARM Cortex®-M4 Devices Generic User Guide (available at http://infocenter.arm.com/help/index.jsp).

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-6 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding IPU2_Cx_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_IPU2_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to IPU2_Cx_INTC inputs. For example, the IPU2_IRQ_23_24[8:0] bit field is used to configure which device interrupt would be mapped to the IPU2_IRQ_23 line. The reset value of this bit field is 0x14, meaning that DISPC_IRQ would be mapped to IPU2_IRQ_23 by default because it is connected to the IRQ_CROSSBAR_20 input.

'N/A' in this column means that the corresponding interrupt is internal to the IPU2 subsystem. There is no IRQ_CROSSBAR dedicated to the associated IPU2_Cx_INTC input line and therefore, the user cannot change its default mapping.

The CTRL_CORE_IPU2_IRQ_y_z registers control the IRQ_CROSSBAR settings for both NVICs in the IPU2 subsystem. That is, it is not possible to map different interrupts to the same interrupt input of the NVICs in IPU2.

17.3.6 Interrupt Requests to EVE1_INTC1

NOTE: EVE is not supported in this family of devices.

Table 17-7 lists the default interrupt sources for the EVE1_INTC1. In addition, device interrupts EVE1_IRQ_0 through EVE1_IRQ_7 can alternatively be sourced through the EVE1's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_EVE1_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-7. EVE1_INTC1 Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE1_IRQ_0	1	CTRL_CORE_EVE1_IRQ_0_1[8:0]	1	ELM_IRQ	Error location process completion interrupt
EVE1_IRQ_1	2	CTRL_CORE_EVE1_IRQ_0_1[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
EVE1_IRQ_2	3	CTRL_CORE_EVE1_IRQ_2_3[8:0]	3	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE1_IRQ_3	4	CTRL_CORE_EVE1_IRQ_2_3[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
EVE1_IRQ_4	5	CTRL_CORE_EVE1_IRQ_4_5[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
EVE1_IRQ_5	6	CTRL_CORE_EVE1_IRQ_4_5[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
EVE1_IRQ_6	7	CTRL_CORE_EVE1_IRQ_6_7[8:0]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
EVE1_IRQ_7	8	CTRL_CORE_EVE1_IRQ_6_7[24:16]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
EVE1_IRQ_8	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_9	N/A	N/A	N/A	EVE2_GP8	EVE2 GP8 interrupt
EVE1_IRQ_10	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_11	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_12	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_13	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_14	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_15	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_16	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_17	N/A	N/A	N/A	EVE2_MBX2_INT1	EVE2 Mailbox 2 Interrupt 1
EVE1_IRQ_18	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_19	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_20	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_21	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_22	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_23	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_24	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_25	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_26	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_27	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_28	N/A	N/A	N/A	EVE1_MBX2_INT0	EVE1 Mailbox 2 Interrupt 0
EVE1_IRQ_29	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_30	N/A	N/A	N/A	Reserved	Reserved
EVE1_IRQ_31	N/A	N/A	N/A	Reserved	Reserved

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-7 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding EVE1_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_EVE1_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to EVE1_INTC inputs. For example, the EVE1_IRQ_0_1[8:0] bit field is used to configure which device interrupt would be mapped to the EVE1_IRQ_0 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to EVE1_IRQ_0 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the EVE1 subsystem. There is no IRQ_CROSSBAR dedicated to the associated EVE1_INTC input line and therefore, the user cannot change its default mapping.

17.3.7 Interrupt Requests to EVE2_INTC1

NOTE: EVE is not supported in this family of devices.

Table 17-8 lists the default interrupt sources for the EVE2_INTC1. In addition, device interrupts EVE2_IRQ_0 through EVE2_IRQ_7 can alternatively be sourced through the EVE2's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_EVE2_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-8. EVE2_INTC1 Default Interrupt Mapping

IRQ Input Line	IRQ_CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE2_IRQ_0	1	CTRL_CORE_EVE2_IRQ_0_1[8:0]	1	ELM_IRQ	Error location process completion interrupt
EVE2_IRQ_1	2	CTRL_CORE_EVE2_IRQ_0_1[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
EVE2_IRQ_2	3	CTRL_CORE_EVE2_IRQ_2_3[8:0]	3	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE2_IRQ_3	4	CTRL_CORE_EVE2_IRQ_2_3[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
EVE2_IRQ_4	5	CTRL_CORE_EVE2_IRQ_4_5[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
EVE2_IRQ_5	6	CTRL_CORE_EVE2_IRQ_4_5[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
EVE2_IRQ_6	7	CTRL_CORE_EVE2_IRQ_6_7[8:0]	7	DMA_SYSTEM_IRQ_0	System DMA interrupt 0
EVE2_IRQ_7	8	CTRL_CORE_EVE2_IRQ_6_7[24:16]	8	DMA_SYSTEM_IRQ_1	System DMA interrupt 1
EVE2_IRQ_8	N/A	N/A	N/A	EVE1_GP1	EVE1 GP1 interrupt
EVE2_IRQ_9	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_10	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_11	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_12	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_13	N/A	N/A	N/A	Reserved	Reserved

Table 17-8. EVE2_INTC1 Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE2_IRQ_14	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_15	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_16	N/A	N/A	N/A	EVE1_MBX2_INT1	EVE1 Mailbox 2 Interrupt 1
EVE2_IRQ_17	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_18	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_19	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_20	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_21	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_22	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_23	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_24	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_25	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_26	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_27	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_28	N/A	N/A	N/A	EVE2_MBX2_INT0	EVE2 Mailbox 2 Interrupt 0
EVE2_IRQ_29	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_30	N/A	N/A	N/A	Reserved	Reserved
EVE2_IRQ_31	N/A	N/A	N/A	Reserved	Reserved

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-8 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding EVE2_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_EVE2_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to EVE2_INTC inputs. For example, the EVE2_IRQ_0_1[8:0] bit field is used to configure which device interrupt would be mapped to the EVE2_IRQ_0 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to EVE2_IRQ_0 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the EVE2 subsystem. There is no IRQ_CROSSBAR dedicated to the associated EVE2_INTC input line and therefore, the user cannot change its default mapping.

17.3.8 Interrupt Requests to EVE3_INTC1

NOTE: EVE is not supported in this family of devices.

Table 17-9 lists the default interrupt sources for the EVE3_INTC1. In addition, device interrupts EVE3_IRQ_0 through EVE3_IRQ_7 can alternatively be sourced through the EVE3's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_EVE3_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-9. EVE3_INTC1 Default Interrupt Mapping

IRQ Input Line	IRQ_CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE3_IRQ_0	1	CTRL_CORE_EVE3_IRQ_0_1[8:0]	1	ELM_IRQ	Error location process completion interrupt
EVE3_IRQ_1	2	CTRL_CORE_EVE3_IRQ_0_1[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
EVE3_IRQ_2	3	CTRL_CORE_EVE3_IRQ_2_3[8:0]	3	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE3_IRQ_3	4	CTRL_CORE_EVE3_IRQ_2_3[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
EVE3_IRQ_4	5	CTRL_CORE_EVE3_IRQ_4_5[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
EVE3_IRQ_5	6	CTRL_CORE_EVE3_IRQ_4_5[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
EVE3_IRQ_6	7	CTRL_CORE_EVE3_IRQ_6_7[8:0]	7	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE3_IRQ_7	8	CTRL_CORE_EVE3_IRQ_6_7[24:16]	8	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE3_IRQ_8	N/A	N/A	N/A	EVE1_GP2	EVE1 GP2 interrupt
EVE3_IRQ_9	N/A	N/A	N/A	EVE2_GP10	EVE2 GP10 interrupt
EVE3_IRQ_10	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_11	N/A	N/A	N/A	EVE4_GP26	EVE4 GP26 interrupt
EVE3_IRQ_12	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_13	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_14	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_15	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_16	N/A	N/A	N/A	EVE1_MBX2_INT2	EVE1 Mailbox 2 Interrupt 2
EVE3_IRQ_17	N/A	N/A	N/A	EVE2_MBX2_INT2	EVE2 Mailbox 2 Interrupt 2
EVE3_IRQ_18	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_19	N/A	N/A	N/A	EVE4_MBX2_INT3	EVE4 Mailbox 2 Interrupt 3
EVE3_IRQ_20	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_21	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_22	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_23	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_24	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_25	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_26	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_27	N/A	N/A	N/A	Reserved	Reserved

Table 17-9. EVE3_INTC1 Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE3_IRQ_28	N/A	N/A	N/A	EVE3_MBX2_INT0	EVE3 Mailbox 2 Interrupt 0
EVE3_IRQ_29	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_30	N/A	N/A	N/A	Reserved	Reserved
EVE3_IRQ_31	N/A	N/A	N/A	Reserved	Reserved

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-9 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding EVE3_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_EVE3_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to EVE3_INTC inputs. For example, the EVE3_IRQ_0_1[8:0] bit field is used to configure which device interrupt would be mapped to the EVE3_IRQ_0 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to EVE3_IRQ_0 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the EVE3 subsystem. There is no IRQ_CROSSBAR dedicated to the associated EVE3_INTC input line and therefore, the user cannot change its default mapping.

17.3.9 Interrupt Requests to EVE4_INTC1

NOTE: EVE is not supported in this family of devices.

Table 17-10 lists the default interrupt sources for the EVE4_INTC1. In addition, device interrupts EVE4_IRQ_0 through EVE4_IRQ_7 can alternatively be sourced through the EVE4's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_EVE4_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-10. EVE4_INTC1 Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE4_IRQ_0	1	CTRL_CORE_EVE4_IRQ_0_1[8:0]	1	ELM_IRQ	Error location process completion interrupt
EVE4_IRQ_1	2	CTRL_CORE_EVE4_IRQ_0_1[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
EVE4_IRQ_2	3	CTRL_CORE_EVE4_IRQ_2_3[8:0]	3	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE4_IRQ_3	4	CTRL_CORE_EVE4_IRQ_2_3[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
EVE4_IRQ_4	5	CTRL_CORE_EVE4_IRQ_4_5[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
EVE4_IRQ_5	6	CTRL_CORE_EVE4_IRQ_4_5[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU

Table 17-10. EVE4_INTC1 Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
EVE4_IRQ_6	7	CTRL_CORE_EVE4_IRQ_6_7[8:0]	7	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE4_IRQ_7	8	CTRL_CORE_EVE4_IRQ_6_7[24:16]	8	Reserved	Reserved by default but can be remapped to a valid interrupt source
EVE4_IRQ_8	N/A	N/A	N/A	EVE1_GP3	EVE1 GP3 interrupt
EVE4_IRQ_9	N/A	N/A	N/A	EVE2_GP11	EVE2 GP11 interrupt
EVE4_IRQ_10	N/A	N/A	N/A	EVE3_GP19	EVE3 GP19 interrupt
EVE4_IRQ_11	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_12	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_13	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_14	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_15	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_16	N/A	N/A	N/A	EVE1_MBX2_INT3	EVE1 Mailbox 3 Interrupt 3
EVE4_IRQ_17	N/A	N/A	N/A	EVE2_MBX2_INT3	EVE2 Mailbox 3 Interrupt 3
EVE4_IRQ_18	N/A	N/A	N/A	EVE3_MBX2_INT3	EVE3 Mailbox 3 Interrupt 3
EVE4_IRQ_19	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_20	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_21	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_22	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_23	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_24	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_25	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_26	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_27	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_28	N/A	N/A	N/A	EVE4_MBX2_INT0	EVE4 Mailbox 2 Interrupt 0
EVE4_IRQ_29	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_30	N/A	N/A	N/A	Reserved	Reserved
EVE4_IRQ_31	N/A	N/A	N/A	Reserved	Reserved

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-10 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding EVE4_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_EVE4_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to EVE4_INTC inputs. For example, the EVE4_IRQ_0_1[8:0] bit field is used to configure which device interrupt would be mapped to the EVE4_IRQ_0 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to EVE4_IRQ_0 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the EVE4 subsystem. There is no IRQ_CROSSBAR dedicated to the associated EVE4_INTC input line and therefore, the user cannot change its default mapping.

17.3.10 Interrupt Requests to PRUSS1_INTC

Table 17-11 lists the default interrupt sources for the PRUSS1_INTC. In addition, device interrupts PRUSS1_IRQ_32 through PRUSS1_IRQ_63 can alternatively be sourced through the PRU-ICSS1 IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_PRUSS1_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-11. PRUSS1_INTC Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS1_IRQ_0	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_0	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_1	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_1	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_2	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_2	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_3	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_3	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_4	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_4	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_5	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_5	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_6	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_6	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_7	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_7	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_8	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_8	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_9	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_9	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_10	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_10	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_11	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_11	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_12	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_12	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_13	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_13	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_14	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_14	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_15	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_15	PRU-ICSS1 Internal Interrupt

Table 17-11. PRUSS1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS1_IRQ_16	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_16	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_17	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_17	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_18	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_18	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_19	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_19	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_20	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_20	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_21	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_21	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_22	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_22	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_23	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_23	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_24	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_24	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_25	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_25	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_26	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_26	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_27	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_27	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_28	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_28	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_29	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_29	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_30	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_30	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_31	N/A	N/A	N/A	PRUSS1_INTERNAL_IRQ_31	PRU-ICSS1 Internal Interrupt
PRUSS1_IRQ_32	1	CTRL_CORE_PRUSS1_IRQ_32_33[8:0]	1	ELM_IRQ	Error location process completion interrupt
PRUSS1_IRQ_33	2	CTRL_CORE_PRUSS1_IRQ_32_33[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
PRUSS1_IRQ_34	3	CTRL_CORE_PRUSS1_IRQ_34_35[8:0]	3	CTRL_MODULE_CORE_IRQ_SEC_EVTS	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3.
PRUSS1_IRQ_35	4	CTRL_CORE_PRUSS1_IRQ_34_35[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
PRUSS1_IRQ_36	5	CTRL_CORE_PRUSS1_IRQ_36_37[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
PRUSS1_IRQ_37	6	CTRL_CORE_PRUSS1_IRQ_36_37[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
PRUSS1_IRQ_38	7	CTRL_CORE_PRUSS1_IRQ_38_39[8:0]	7	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_39	8	CTRL_CORE_PRUSS1_IRQ_38_39[24:16]	8	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_40	9	CTRL_CORE_PRUSS1_IRQ_40_41[8:0]	9	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_41	10	CTRL_CORE_PRUSS1_IRQ_40_41[24:16]	10	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_42	11	CTRL_CORE_PRUSS1_IRQ_42_43[8:0]	11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN statistic collector alarm interrupt

Table 17-11. PRUSS1_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS1_IRQ_43	12	CTRL_CORE_PRUSS1_IRQ_42_43[24:16]	12	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_44	13	CTRL_CORE_PRUSS1_IRQ_44_45[8:0]	13	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_45	14	CTRL_CORE_PRUSS1_IRQ_44_45[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_46	15	CTRL_CORE_PRUSS1_IRQ_46_47[8:0]	15	GPMC_IRQ	GPMC interrupt
PRUSS1_IRQ_47	16	CTRL_CORE_PRUSS1_IRQ_46_47[24:16]	16	GPU_IRQ	GPU interrupt
PRUSS1_IRQ_48	17	CTRL_CORE_PRUSS1_IRQ_48_49[8:0]	17	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_49	18	CTRL_CORE_PRUSS1_IRQ_48_49[24:16]	18	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_50	19	CTRL_CORE_PRUSS1_IRQ_50_51[8:0]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_51	20	CTRL_CORE_PRUSS1_IRQ_50_51[24:16]	20	DISPC_IRQ	Display controller interrupt
PRUSS1_IRQ_52	21	CTRL_CORE_PRUSS1_IRQ_52_53[8:0]	21	MAILBOX1_IRQ_USER0	Mailbox 1 user 0 interrupt
PRUSS1_IRQ_53	22	CTRL_CORE_PRUSS1_IRQ_52_53[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_54	23	CTRL_CORE_PRUSS1_IRQ_54_55[8:0]	23	DSP1_IRQ_MMU0	DSP1 MMU0 interrupt
PRUSS1_IRQ_55	24	CTRL_CORE_PRUSS1_IRQ_54_55[24:16]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
PRUSS1_IRQ_56	25	CTRL_CORE_PRUSS1_IRQ_56_57[8:0]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
PRUSS1_IRQ_57	26	CTRL_CORE_PRUSS1_IRQ_56_57[24:16]	26	GPIO3_IRQ_1	GPIO3 interrupt 1
PRUSS1_IRQ_58	27	CTRL_CORE_PRUSS1_IRQ_58_59[8:0]	27	GPIO4_IRQ_1	GPIO4 interrupt 1
PRUSS1_IRQ_59	28	CTRL_CORE_PRUSS1_IRQ_58_59[24:16]	28	GPIO5_IRQ_1	GPIO5 interrupt 1
PRUSS1_IRQ_60	29	CTRL_CORE_PRUSS1_IRQ_60_61[8:0]	29	GPIO6_IRQ_1	GPIO6 interrupt 1
PRUSS1_IRQ_61	30	CTRL_CORE_PRUSS1_IRQ_60_61[24:16]	30	GPIO7_IRQ_1	GPIO7 interrupt 1
PRUSS1_IRQ_62	31	CTRL_CORE_PRUSS1_IRQ_62_63[8:0]	31	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS1_IRQ_63	32	CTRL_CORE_PRUSS1_IRQ_62_63[24:16]	32	TIMER1_IRQ	TIMER1 interrupt

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-11 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding PRUSS1_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_PRUSS1_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to PRUSS1_INTC inputs. For example, the PRUSS1_IRQ_32_33[8:0] bit field is used to configure which device interrupt would be mapped to the PRUSS1_IRQ_32 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to PRUSS1_IRQ_32 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the PRU-ICSS1 subsystem. There is no IRQ_CROSSBAR dedicated to the associated PRUSS1_INTC input line and therefore, the user cannot change its default mapping.

17.3.11 Interrupt Requests to PRUSS2_INTC

Table 17-12 lists the default interrupt sources for the PRUSS2_INTC. In addition, device interrupts PRUSS2_IRQ_32 through PRUSS2_IRQ_63 can alternatively be sourced through the PRU-ICSS2's IRQ_CROSSBAR from one of the 420 multiplexed device interrupts listed in Table 17-13. The CTRL_CORE_PRUSS2_IRQ_y_z registers in the Control Module are used to select between the default interrupts and the multiplexed interrupts.

Table 17-12. PRUSS2_INTC Default Interrupt Mapping

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS2_IRQ_0	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_0	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_1	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_1	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_2	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_2	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_3	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_3	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_4	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_4	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_5	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_5	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_6	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_6	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_7	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_7	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_8	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_8	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_9	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_9	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_10	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_10	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_11	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_11	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_12	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_12	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_13	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_13	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_14	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_14	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_15	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_15	PRU-ICSS2 Internal Interrupt

Table 17-12. PRUSS2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS2_IRQ_16	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_16	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_17	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_17	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_18	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_18	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_19	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_19	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_20	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_20	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_21	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_21	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_22	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_22	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_23	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_23	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_24	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_24	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_25	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_25	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_26	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_26	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_27	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_27	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_28	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_28	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_29	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_29	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_30	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_30	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_31	N/A	N/A	N/A	PRUSS2_INTERNAL_IRQ_31	PRU-ICSS2 Internal Interrupt
PRUSS2_IRQ_32	1	CTRL_CORE_PRUSS2_IRQ_32_33[8:0]	1	ELM_IRQ	Error location process completion interrupt
PRUSS2_IRQ_33	2	CTRL_CORE_PRUSS2_IRQ_32_33[24:16]	2	EXT_SYS_IRQ_1	External interrupt (active low) via sys_nirq1 pin
PRUSS2_IRQ_34	3	CTRL_CORE_PRUSS2_IRQ_34_35[8:0]	3	CTRL_MODULE_CORE_IRQ_SEC_EVTS	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3.
PRUSS2_IRQ_35	4	CTRL_CORE_PRUSS2_IRQ_34_35[24:16]	4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN debug error
PRUSS2_IRQ_36	5	CTRL_CORE_PRUSS2_IRQ_36_37[8:0]	5	L3_MAIN_IRQ_APP_ERR	L3_MAIN application or non-attributable error
PRUSS2_IRQ_37	6	CTRL_CORE_PRUSS2_IRQ_36_37[24:16]	6	PRM_IRQ_MPU	PRCM interrupt to MPU
PRUSS2_IRQ_38	7	CTRL_CORE_PRUSS2_IRQ_38_39[8:0]	7	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_39	8	CTRL_CORE_PRUSS2_IRQ_38_39[24:16]	8	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_40	9	CTRL_CORE_PRUSS2_IRQ_40_41[8:0]	9	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_41	10	CTRL_CORE_PRUSS2_IRQ_40_41[24:16]	10	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_42	11	CTRL_CORE_PRUSS2_IRQ_42_43[8:0]	11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN statistic collector alarm interrupt

Table 17-12. PRUSS2_INTC Default Interrupt Mapping (continued)

IRQ Input Line	IRQ_ CROSSBAR Instance Number	IRQ_CROSSBAR Configuration Register	IRQ_ CROSSBAR Default Input Index	Default Interrupt Name	Default Interrupt Source Description
PRUSS2_IRQ_43	12	CTRL_CORE_PRUSS2_IRQ_42_43[24:16]	12	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_44	13	CTRL_CORE_PRUSS2_IRQ_44_45[8:0]	13	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_45	14	CTRL_CORE_PRUSS2_IRQ_44_45[24:16]	14	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_46	15	CTRL_CORE_PRUSS2_IRQ_46_47[8:0]	15	GPMC_IRQ	GPMC interrupt
PRUSS2_IRQ_47	16	CTRL_CORE_PRUSS2_IRQ_46_47[24:16]	16	GPU_IRQ	GPU interrupt
PRUSS2_IRQ_48	17	CTRL_CORE_PRUSS2_IRQ_48_49[8:0]	17	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_49	18	CTRL_CORE_PRUSS2_IRQ_48_49[24:16]	18	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_50	19	CTRL_CORE_PRUSS2_IRQ_50_51[8:0]	19	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_51	20	CTRL_CORE_PRUSS2_IRQ_50_51[24:16]	20	DISPC_IRQ	Display controller interrupt
PRUSS2_IRQ_52	21	CTRL_CORE_PRUSS2_IRQ_52_53[8:0]	21	MAILBOX1_IRQ_USER0	Mailbox 1 user 0 interrupt
PRUSS2_IRQ_53	22	CTRL_CORE_PRUSS2_IRQ_52_53[24:16]	22	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_54	23	CTRL_CORE_PRUSS2_IRQ_54_55[8:0]	23	DSP1_IRQ_MMU0	DSP1 MMU0 interrupt
PRUSS2_IRQ_55	24	CTRL_CORE_PRUSS2_IRQ_54_55[24:16]	24	GPIO1_IRQ_1	GPIO1 interrupt 1
PRUSS2_IRQ_56	25	CTRL_CORE_PRUSS2_IRQ_56_57[8:0]	25	GPIO2_IRQ_1	GPIO2 interrupt 1
PRUSS2_IRQ_57	26	CTRL_CORE_PRUSS2_IRQ_56_57[24:16]	26	GPIO3_IRQ_1	GPIO3 interrupt 1
PRUSS2_IRQ_58	27	CTRL_CORE_PRUSS2_IRQ_58_59[8:0]	27	GPIO4_IRQ_1	GPIO4 interrupt 1
PRUSS2_IRQ_59	28	CTRL_CORE_PRUSS2_IRQ_58_59[24:16]	28	GPIO5_IRQ_1	GPIO5 interrupt 1
PRUSS2_IRQ_60	29	CTRL_CORE_PRUSS2_IRQ_60_61[8:0]	29	GPIO6_IRQ_1	GPIO6 interrupt 1
PRUSS2_IRQ_61	30	CTRL_CORE_PRUSS2_IRQ_60_61[24:16]	30	GPIO7_IRQ_1	GPIO7 interrupt 1
PRUSS2_IRQ_62	31	CTRL_CORE_PRUSS2_IRQ_62_63[8:0]	31	Reserved	Reserved by default but can be remapped to a valid interrupt source
PRUSS2_IRQ_63	32	CTRL_CORE_PRUSS2_IRQ_62_63[24:16]	32	TIMER1_IRQ	TIMER1 interrupt

NOTE: The "**IRQ_CROSSBAR Default Input Index**" column of Table 17-12 shows which input of the corresponding IRQ_CROSSBAR instance is mapped to its output (and then routed to the corresponding PRUSS2_INTC input) by default. In other words, this column specifies the default (reset) values (in decimal) of the CTRL_CORE_PRUSS2_IRQ_y_z register bit fields that are used to control the mapping of device interrupts to PRUSS2_INTC inputs. For example, the PRUSS2_IRQ_32_33[8:0] bit field is used to configure which device interrupt would be mapped to the PRUSS2_IRQ_32 line. The reset value of this bit field is 0x1, meaning that ELM_IRQ would be mapped to PRUSS2_IRQ_32 by default because it is connected to the IRQ_CROSSBAR_1 input.

'N/A' in this column means that the corresponding interrupt is internal to the PRU-ICSS2 subsystem. There is no IRQ_CROSSBAR dedicated to the associated PRUSS2_INTC input line and therefore, the user cannot change its default mapping.

17.3.12 Mapping of Device Interrupts to IRQ_CROSSBAR Inputs

Table 17-13 shows the individual connection between all module IRQs and all IRQ_CROSSBAR inputs.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_0	Reserved	Reserved	Reserved
IRQ_CROSSBAR_1	ELM_IRQ	ELM	Error location process completion interrupt
IRQ_CROSSBAR_2	EXT_SYS_IRQ_1	External system	External interrupt (active low) via sys_nirq1 pin
IRQ_CROSSBAR_3	CTRL_MODULE_CORE_IRQ_SEC_EVTS	CTRL_MODULE_CORE	Combined firewall error interrupt. For more information, see Section 18.4.6.14.3
IRQ_CROSSBAR_4	L3_MAIN_IRQ_DBG_ERR	L3_MAIN	L3_MAIN debug error
IRQ_CROSSBAR_5	L3_MAIN_IRQ_APP_ERR	L3_MAIN	L3_MAIN application or non-attributable error
IRQ_CROSSBAR_6	PRM_IRQ_MPU	PRM	PRCM interrupt to MPU
IRQ_CROSSBAR_7	DMA_SYSTEM_IRQ_0	DMA_SYSTEM	System DMA interrupt 0
IRQ_CROSSBAR_8	DMA_SYSTEM_IRQ_1	DMA_SYSTEM	System DMA interrupt 1
IRQ_CROSSBAR_9	DMA_SYSTEM_IRQ_2	DMA_SYSTEM	System DMA interrupt 2
IRQ_CROSSBAR_10	DMA_SYSTEM_IRQ_3	DMA_SYSTEM	System DMA interrupt 3
IRQ_CROSSBAR_11	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN	L3_MAIN statistic collector alarm interrupt
IRQ_CROSSBAR_12	Reserved	Reserved	Reserved
IRQ_CROSSBAR_13	Reserved	Reserved	Reserved
IRQ_CROSSBAR_14	Reserved	Reserved	Reserved
IRQ_CROSSBAR_15	GPMC_IRQ	GPMC	GPMC interrupt
IRQ_CROSSBAR_16	GPU_IRQ	GPU	GPU interrupt
IRQ_CROSSBAR_17	Reserved	Reserved	Reserved
IRQ_CROSSBAR_18	Reserved	Reserved	Reserved
IRQ_CROSSBAR_19	Reserved	Reserved	Reserved
IRQ_CROSSBAR_20	DISPC_IRQ	DISPC	Display controller interrupt
IRQ_CROSSBAR_21	MAILBOX1_IRQ_USER0	MAILBOX1	Mailbox 1 user 0 interrupt
IRQ_CROSSBAR_22	Reserved	Reserved	Reserved
IRQ_CROSSBAR_23	DSP1_IRQ_MMU0	DSP1	DSP1 MMU0 interrupt
IRQ_CROSSBAR_24	GPIO1_IRQ_1	GPIO1	GPIO1 interrupt 1
IRQ_CROSSBAR_25	GPIO2_IRQ_1	GPIO2	GPIO2 interrupt 1
IRQ_CROSSBAR_26	GPIO3_IRQ_1	GPIO3	GPIO3 interrupt 1
IRQ_CROSSBAR_27	GPIO4_IRQ_1	GPIO4	GPIO4 interrupt 1
IRQ_CROSSBAR_28	GPIO5_IRQ_1	GPIO5	GPIO5 interrupt 1
IRQ_CROSSBAR_29	GPIO6_IRQ_1	GPIO6	GPIO6 interrupt 1
IRQ_CROSSBAR_30	GPIO7_IRQ_1	GPIO7	GPIO7 interrupt 1
IRQ_CROSSBAR_31	Reserved	Reserved	Reserved
IRQ_CROSSBAR_32	TIMER1_IRQ	TIMER1	TIMER1 interrupt
IRQ_CROSSBAR_33	TIMER2_IRQ	TIMER2	TIMER2 interrupt
IRQ_CROSSBAR_34	TIMER3_IRQ	TIMER3	TIMER3 interrupt
IRQ_CROSSBAR_35	TIMER4_IRQ	TIMER4	TIMER4 interrupt
IRQ_CROSSBAR_36	TIMER5_IRQ	TIMER5	TIMER5 interrupt
IRQ_CROSSBAR_37	TIMER6_IRQ	TIMER6	TIMER6 interrupt
IRQ_CROSSBAR_38	TIMER7_IRQ	TIMER7	TIMER7 interrupt
IRQ_CROSSBAR_39	TIMER8_IRQ	TIMER8	TIMER8 interrupt
IRQ_CROSSBAR_40	TIMER9_IRQ	TIMER9	TIMER9 interrupt
IRQ_CROSSBAR_41	TIMER10_IRQ	TIMER10	TIMER10 interrupt
IRQ_CROSSBAR_42	TIMER11_IRQ	TIMER11	TIMER11 interrupt
IRQ_CROSSBAR_43	MCSPI4_IRQ	McSPI4	McSPI4 interrupt
IRQ_CROSSBAR_44	Reserved	Reserved	Reserved
IRQ_CROSSBAR_45	Reserved	Reserved	Reserved

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_46	Reserved	Reserved	Reserved
IRQ_CROSSBAR_47	Reserved	Reserved	Reserved
IRQ_CROSSBAR_48	Reserved	Reserved	Reserved
IRQ_CROSSBAR_49	SATA_IRQ	SATA	SATA interrupt
IRQ_CROSSBAR_50	Reserved	Reserved	Reserved
IRQ_CROSSBAR_51	I2C1_IRQ	I2C1	I2C1 interrupt
IRQ_CROSSBAR_52	I2C2_IRQ	I2C2	I2C2 interrupt
IRQ_CROSSBAR_53	HDQ1W_IRQ	HDQ1W	HDQ1W interrupt
IRQ_CROSSBAR_54	Reserved	Reserved	Reserved
IRQ_CROSSBAR_55	I2C5_IRQ	I2C5	I2C5 interrupt
IRQ_CROSSBAR_56	I2C3_IRQ	I2C3	I2C3 interrupt
IRQ_CROSSBAR_57	I2C4_IRQ	I2C4	I2C4 interrupt
IRQ_CROSSBAR_58	Reserved	Reserved	Reserved
IRQ_CROSSBAR_59	Reserved	Reserved	Reserved
IRQ_CROSSBAR_60	MCSPI1_IRQ	McSPI1	McSPI1 interrupt
IRQ_CROSSBAR_61	MCSPI2_IRQ	McSPI2	McSPI2 interrupt
IRQ_CROSSBAR_62	Reserved	Reserved	Reserved
IRQ_CROSSBAR_63	Reserved	Reserved	Reserved
IRQ_CROSSBAR_64	Reserved	Reserved	Reserved
IRQ_CROSSBAR_65	UART4_IRQ	UART4	UART4 interrupt
IRQ_CROSSBAR_66	Reserved	Reserved	Reserved
IRQ_CROSSBAR_67	UART1_IRQ	UART1	UART1 interrupt
IRQ_CROSSBAR_68	UART2_IRQ	UART2	UART2 interrupt
IRQ_CROSSBAR_69	UART3_IRQ	UART3	UART3 interrupt
IRQ_CROSSBAR_70	PBIAS_IRQ	MMC1 PBIAS Cell	MMC1 PBIAS interrupt (controlled via device Control Module)
IRQ_CROSSBAR_71	USB1_IRQ_INTR0	USB1	USB1 interrupt 0
IRQ_CROSSBAR_72	USB1_IRQ_INTR1	USB1	USB1 interrupt 1
IRQ_CROSSBAR_73	USB2_IRQ_INTR0	USB2	USB2 interrupt 0
IRQ_CROSSBAR_74	Reserved	Reserved	Reserved
IRQ_CROSSBAR_75	WD_TIMER2_IRQ	WD_TIMER2	WD_TIMER2 interrupt
IRQ_CROSSBAR_76	Reserved	Reserved	Reserved
IRQ_CROSSBAR_77	Reserved	Reserved	Reserved
IRQ_CROSSBAR_78	MMC1_IRQ	MMC1	MMC1 interrupt
IRQ_CROSSBAR_79	Reserved	Reserved	Reserved
IRQ_CROSSBAR_80	Reserved	Reserved	Reserved
IRQ_CROSSBAR_81	MMC2_IRQ	MMC2	MMC2 interrupt
IRQ_CROSSBAR_82	Reserved	Reserved	Reserved
IRQ_CROSSBAR_83	Reserved	Reserved	Reserved
IRQ_CROSSBAR_84	Reserved	Reserved	Reserved
IRQ_CROSSBAR_85	DEBUGSS_IRQ_CT_UART	DEBUGSS	CT_UART interrupt generated when data ready on RX or when TX empty
IRQ_CROSSBAR_86	MCSPI3_IRQ	McSPI3	McSPI3 interrupt
IRQ_CROSSBAR_87	USB2_IRQ_INTR1	USB2	USB2 interrupt 1
IRQ_CROSSBAR_88	USB3_IRQ_INTR0 (1)	USB3	USB3 interrupt 0
IRQ_CROSSBAR_89	MMC3_IRQ	MMC3	MMC3 interrupt

(1) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_90	TIMER12_IRQ	TIMER12	TIMER12 interrupt
IRQ_CROSSBAR_91	MMC4_IRQ	MMC4	MMC4 interrupt
IRQ_CROSSBAR_92	Reserved	Reserved	Reserved
IRQ_CROSSBAR_93	Reserved	Reserved	Reserved
IRQ_CROSSBAR_94	Reserved	Reserved	Reserved
IRQ_CROSSBAR_95	Reserved	Reserved	Reserved
IRQ_CROSSBAR_96	HDMI_IRQ	HDMI	HDMI interrupt
IRQ_CROSSBAR_97	Reserved	Reserved	Reserved
IRQ_CROSSBAR_98	IVA_IRQ_SYNC_1	IVA	IVA ICONT2 sync interrupt
IRQ_CROSSBAR_99	IVA_IRQ_SYNC_0	IVA	IVA ICONT1 sync interrupt
IRQ_CROSSBAR_100	UART5_IRQ	UART5	UART5 interrupt
IRQ_CROSSBAR_101	UART6_IRQ	UART6	UART6 interrupt
IRQ_CROSSBAR_102	IVA_IRQ_MAILBOX_0	IVA	IVA mailbox user 0 interrupt
IRQ_CROSSBAR_103	McASP1_IRQ_AREVT	McASP1	McASP1 receive interrupt
IRQ_CROSSBAR_104	McASP1_IRQ_AXEVT	McASP1	McASP1 transmit interrupt
IRQ_CROSSBAR_105	EMIF1_IRQ	EMIF1	EMIF1 interrupt
IRQ_CROSSBAR_106	EMIF2_IRQ	EMIF2	EMIF2 interrupt
IRQ_CROSSBAR_107	Reserved	Reserved	Reserved
IRQ_CROSSBAR_108	DMM_IRQ	DMM	DMM interrupt
IRQ_CROSSBAR_109	Reserved	Reserved	Reserved
IRQ_CROSSBAR_110	Reserved	Reserved	Reserved
IRQ_CROSSBAR_111	Reserved	Reserved	Reserved
IRQ_CROSSBAR_112	Reserved	Reserved	Reserved
IRQ_CROSSBAR_113	Reserved	Reserved	Reserved
IRQ_CROSSBAR_114	EXT_SYS_IRQ_2	External system	External interrupt (active low) via sys_nirq2 pin
IRQ_CROSSBAR_115	KBD_IRQ	KBD	Keyboard controller interrupt
IRQ_CROSSBAR_116	GPIO8_IRQ_1	GPIO8	GPIO8 interrupt 1
IRQ_CROSSBAR_117	Reserved	Reserved	Reserved
IRQ_CROSSBAR_118	Reserved	Reserved	Reserved
IRQ_CROSSBAR_119	Reserved	Reserved	Reserved
IRQ_CROSSBAR_120	BB2D_IRQ	BB2D	BB2D interrupt
IRQ_CROSSBAR_121	CTRL_MODULE_CORE_IRQ_THERMAL_ALERT	CTRL_MODULE	CTRL_MODULE thermal alert interrupt
IRQ_CROSSBAR_[122:131]	Reserved	Reserved	Reserved
IRQ_CROSSBAR_132	IVA_IRQ_MAILBOX_2	IVA	IVA mailbox user 2 interrupt
IRQ_CROSSBAR_133	PRM_IRQ_IPU1	PRM	PRCM interrupt to IPU1
IRQ_CROSSBAR_134	MAILBOX1_IRQ_USER2	MAILBOX1	Mailbox 1 user 2 interrupt
IRQ_CROSSBAR_135	MAILBOX1_IRQ_USER1	MAILBOX1	Mailbox 1 user 1 interrupt
IRQ_CROSSBAR_136	IVA_IRQ_MAILBOX_1	IVA	IVA mailbox user 1 interrupt
IRQ_CROSSBAR_137	PRM_IRQ_DSP1	PRM	PRCM interrupt to DSP1
IRQ_CROSSBAR_138	GPIO1_IRQ_2	GPIO1	GPIO1 interrupt 2
IRQ_CROSSBAR_139	GPIO2_IRQ_2	GPIO2	GPIO2 interrupt 2
IRQ_CROSSBAR_140	GPIO3_IRQ_2	GPIO3	GPIO3 interrupt 2
IRQ_CROSSBAR_141	GPIO4_IRQ_2	GPIO4	GPIO4 interrupt 2
IRQ_CROSSBAR_142	GPIO5_IRQ_2	GPIO5	GPIO5 interrupt 2
IRQ_CROSSBAR_143	GPIO6_IRQ_2	GPIO6	GPIO6 interrupt 2

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_144	Reserved	Reserved	Reserved
IRQ_CROSSBAR_145	DSP1_IRQ_MMU1	DSP1	DSP1 MMU1 interrupt
IRQ_CROSSBAR_146	DSP2_IRQ_MMU0	DSP2	DSP2 MMU0 interrupt
IRQ_CROSSBAR_147	DSP2_IRQ_MMU1	DSP2	DSP2 MMU1 interrupt
IRQ_CROSSBAR_148	McASP2_IRQ_AREVT	McASP2	McASP2 receive interrupt
IRQ_CROSSBAR_149	McASP2_IRQ_AXEVT	McASP2	McASP2 transmit interrupt
IRQ_CROSSBAR_150	McASP3_IRQ_AREVT	McASP3	McASP3 receive interrupt
IRQ_CROSSBAR_151	McASP3_IRQ_AXEVT	McASP3	McASP3 transmit interrupt
IRQ_CROSSBAR_152	McASP4_IRQ_AREVT	McASP4	McASP4 receive interrupt
IRQ_CROSSBAR_153	McASP4_IRQ_AXEVT	McASP4	McASP4 transmit interrupt
IRQ_CROSSBAR_154	McASP5_IRQ_AREVT	McASP5	McASP5 receive interrupt
IRQ_CROSSBAR_155	McASP5_IRQ_AXEVT	McASP5	McASP5 transmit interrupt
IRQ_CROSSBAR_156	McASP6_IRQ_AREVT	McASP6	McASP6 receive interrupt
IRQ_CROSSBAR_157	McASP6_IRQ_AXEVT	McASP6	McASP6 transmit interrupt
IRQ_CROSSBAR_158	McASP7_IRQ_AREVT	McASP7	McASP7 receive interrupt
IRQ_CROSSBAR_159	McASP7_IRQ_AXEVT	McASP7	McASP7 transmit interrupt
IRQ_CROSSBAR_160	McASP8_IRQ_AREVT	McASP8	McASP8 receive interrupt
IRQ_CROSSBAR_161	McASP8_IRQ_AXEVT	McASP8	McASP8 transmit interrupt
IRQ_CROSSBAR_162	Reserved	Reserved	Reserved
IRQ_CROSSBAR_163	Reserved	Reserved	Reserved
IRQ_CROSSBAR_164	OCMC_RAM1_IRQ	OCMC_RAM1	OCMC_RAM1 interrupt
IRQ_CROSSBAR_165	OCMC_RAM2_IRQ	OCMC_RAM2	OCMC_RAM2 interrupt
IRQ_CROSSBAR_166	OCMC_RAM3_IRQ	OCMC_RAM3	OCMC_RAM3 interrupt
IRQ_CROSSBAR_167	Reserved	Reserved	Reserved
IRQ_CROSSBAR_168	EVE1_IRQ_OUT0[(2)]	EVE1	EVE1 output interrupt 0
IRQ_CROSSBAR_169	EVE1_IRQ_OUT1[(2)]	EVE1	EVE1 output interrupt 1
IRQ_CROSSBAR_170	EVE1_IRQ_OUT2[(2)]	EVE1	EVE1 output interrupt 2
IRQ_CROSSBAR_171	EVE1_IRQ_OUT3[(2)]	EVE1	EVE1 output interrupt 3
IRQ_CROSSBAR_172	EVE2_IRQ_OUT0[(2)]	EVE2	EVE2 output interrupt 0
IRQ_CROSSBAR_173	EVE2_IRQ_OUT1[(2)]	EVE2	EVE2 output interrupt 1
IRQ_CROSSBAR_174	EVE2_IRQ_OUT2[(2)]	EVE2	EVE2 output interrupt 2
IRQ_CROSSBAR_175	EVE2_IRQ_OUT3[(2)]	EVE2	EVE2 output interrupt 3
IRQ_CROSSBAR_176	EVE3_IRQ_OUT0[(2)]	EVE3	EVE3 output interrupt 0
IRQ_CROSSBAR_177	EVE3_IRQ_OUT1[(2)]	EVE3	EVE3 output interrupt 1
IRQ_CROSSBAR_178	EVE3_IRQ_OUT2[(2)]	EVE3	EVE3 output interrupt 2
IRQ_CROSSBAR_179	EVE3_IRQ_OUT3[(2)]	EVE3	EVE3 output interrupt 3
IRQ_CROSSBAR_180	EVE4_IRQ_OUT0[(2)]	EVE4	EVE4 output interrupt 0
IRQ_CROSSBAR_181	EVE4_IRQ_OUT1[(2)]	EVE4	EVE4 output interrupt 1
IRQ_CROSSBAR_182	EVE4_IRQ_OUT2[(2)]	EVE4	EVE4 output interrupt 2
IRQ_CROSSBAR_183	EVE4_IRQ_OUT3[(2)]	EVE4	EVE4 output interrupt 3
IRQ_CROSSBAR_184	Reserved	Reserved	Reserved
IRQ_CROSSBAR_185	Reserved	Reserved	Reserved
IRQ_CROSSBAR_186	PRUSS1_IRQ_HOST2	PRU-ICSS1	PRU-ICSS1 host interrupt 2
IRQ_CROSSBAR_187	PRUSS1_IRQ_HOST3	PRU-ICSS1	PRU-ICSS1 host interrupt 3
IRQ_CROSSBAR_188	PRUSS1_IRQ_HOST4	PRU-ICSS1	PRU-ICSS1 host interrupt 4
IRQ_CROSSBAR_189	PRUSS1_IRQ_HOST5	PRU-ICSS1	PRU-ICSS1 host interrupt 5

(2) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_190	PRUSS1_IRQ_HOST6	PRU-ICSS1	PRU-ICSS1 host interrupt 6
IRQ_CROSSBAR_191	PRUSS1_IRQ_HOST7	PRU-ICSS1	PRU-ICSS1 host interrupt 7
IRQ_CROSSBAR_192	PRUSS1_IRQ_HOST8	PRU-ICSS1	PRU-ICSS1 host interrupt 8
IRQ_CROSSBAR_193	PRUSS1_IRQ_HOST9	PRU-ICSS1	PRU-ICSS1 host interrupt 9
IRQ_CROSSBAR_194	Reserved	Reserved	Reserved
IRQ_CROSSBAR_195	Reserved	Reserved	Reserved
IRQ_CROSSBAR_196	PRUSS2_IRQ_HOST2	PRU-ICSS2	PRU-ICSS2 host interrupt 2
IRQ_CROSSBAR_197	PRUSS2_IRQ_HOST3	PRU-ICSS2	PRU-ICSS2 host interrupt 3
IRQ_CROSSBAR_198	PRUSS2_IRQ_HOST4	PRU-ICSS2	PRU-ICSS2 host interrupt 4
IRQ_CROSSBAR_199	PRUSS2_IRQ_HOST5	PRU-ICSS2	PRU-ICSS2 host interrupt 5
IRQ_CROSSBAR_200	PRUSS2_IRQ_HOST6	PRU-ICSS2	PRU-ICSS2 host interrupt 6
IRQ_CROSSBAR_201	PRUSS2_IRQ_HOST7	PRU-ICSS2	PRU-ICSS2 host interrupt 7
IRQ_CROSSBAR_202	PRUSS2_IRQ_HOST8	PRU-ICSS2	PRU-ICSS2 host interrupt 8
IRQ_CROSSBAR_203	PRUSS2_IRQ_HOST9	PRU-ICSS2	PRU-ICSS2 host interrupt 9
IRQ_CROSSBAR_204	PWMSS1_IRQ_ePWM0_TZINT	PWMSS1	eHRPWM0 TZ interrupt
IRQ_CROSSBAR_205	PWMSS2_IRQ_ePWM1_TZINT	PWMSS2	eHRPWM1 TZ interrupt
IRQ_CROSSBAR_206	PWMSS3_IRQ_ePWM2_TZINT	PWMSS3	eHRPWM2 TZ interrupt
IRQ_CROSSBAR_207	PWMSS1_IRQ_ePWM0INT	PWMSS1	eHRPWM0 event/interrupt
IRQ_CROSSBAR_208	PWMSS2_IRQ_ePWM1INT	PWMSS2	eHRPWM1 event/interrupt
IRQ_CROSSBAR_209	PWMSS3_IRQ_ePWM2INT	PWMSS3	eHRPWM2 event/interrupt
IRQ_CROSSBAR_210	PWMSS1_IRQ_eQEP0INT	PWMSS1	eQEP0 event/interrupt
IRQ_CROSSBAR_211	PWMSS2_IRQ_eQEP1INT	PWMSS2	eQEP1 event/interrupt
IRQ_CROSSBAR_212	PWMSS3_IRQ_eQEP2INT	PWMSS3	eQEP2 event/interrupt
IRQ_CROSSBAR_213	PWMSS1_IRQ_eCAP0INT	PWMSS1	eCAP0 event/interrupt
IRQ_CROSSBAR_214	PWMSS2_IRQ_eCAP1INT	PWMSS2	eCAP1 event/interrupt
IRQ_CROSSBAR_215	PWMSS3_IRQ_eCAP2INT	PWMSS3	eCAP2 event/interrupt
IRQ_CROSSBAR_216	Reserved	Reserved	Reserved
IRQ_CROSSBAR_217	RTC_SS_IRQ_ALARM	RTC_SS	RTC_SS alarm interrupt
IRQ_CROSSBAR_218	UART7_IRQ	UART7	UART7 interrupt
IRQ_CROSSBAR_219	UART8_IRQ	UART8	UART8 interrupt
IRQ_CROSSBAR_220	UART9_IRQ	UART9	UART9 interrupt
IRQ_CROSSBAR_221	UART10_IRQ	UART10	UART10 interrupt
IRQ_CROSSBAR_222	DCAN1_IRQ_INT0	DCAN1	DCAN1 interrupt 0
IRQ_CROSSBAR_223	DCAN1_IRQ_INT1	DCAN1	DCAN1 interrupt 1
IRQ_CROSSBAR_224	DCAN1_IRQ_PARITY	DCAN1	DCAN1 parity interrupt
IRQ_CROSSBAR_225	DCAN2_IRQ_INT0	DCAN2	DCAN2 interrupt 0
IRQ_CROSSBAR_226	DCAN2_IRQ_INT1	DCAN2	DCAN2 interrupt 1
IRQ_CROSSBAR_227	DCAN2_IRQ_PARITY	DCAN2	DCAN2 parity interrupt
IRQ_CROSSBAR_228	MLB_IRQ_SYS_INT0 (3)	MLB	MLB system interrupt 0
IRQ_CROSSBAR_229	MLB_IRQ_SYS_INT1 (3)	MLB	MLB system interrupt 1
IRQ_CROSSBAR_230	VCP1_IRQ_INT (3)	VCP1	VCP1 interrupt
IRQ_CROSSBAR_231	VCP2_IRQ_INT (3)	VCP2	VCP2 interrupt
IRQ_CROSSBAR_232	PCIe_SS1_IRQ_INT0	PCIe_SS1	PCIe_SS1 interrupt 0
IRQ_CROSSBAR_233	PCIe_SS1_IRQ_INT1	PCIe_SS1	PCIe_SS1 interrupt 1
IRQ_CROSSBAR_234	Reserved	Reserved	Reserved
IRQ_CROSSBAR_235	Reserved	Reserved	Reserved

(3) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_236	Reserved	Reserved	Reserved
IRQ_CROSSBAR_237	MAILBOX2_IRQ_USER0	MAILBOX2	Mailbox 2 user 0 interrupt
IRQ_CROSSBAR_238	MAILBOX2_IRQ_USER1	MAILBOX2	Mailbox 2 user 1 interrupt
IRQ_CROSSBAR_239	MAILBOX2_IRQ_USER2	MAILBOX2	Mailbox 2 user 2 interrupt
IRQ_CROSSBAR_240	MAILBOX2_IRQ_USER3	MAILBOX2	Mailbox 2 user 3 interrupt
IRQ_CROSSBAR_241	MAILBOX3_IRQ_USER0	MAILBOX3	Mailbox 3 user 0 interrupt
IRQ_CROSSBAR_242	MAILBOX3_IRQ_USER1	MAILBOX3	Mailbox 3 user 1 interrupt
IRQ_CROSSBAR_243	MAILBOX3_IRQ_USER2	MAILBOX3	Mailbox 3 user 2 interrupt
IRQ_CROSSBAR_244	MAILBOX3_IRQ_USER3	MAILBOX3	Mailbox 3 user 3 interrupt
IRQ_CROSSBAR_245	MAILBOX4_IRQ_USER0	MAILBOX4	Mailbox 4 user 0 interrupt
IRQ_CROSSBAR_246	MAILBOX4_IRQ_USER1	MAILBOX4	Mailbox 4 user 1 interrupt
IRQ_CROSSBAR_247	MAILBOX4_IRQ_USER2	MAILBOX4	Mailbox 4 user 2 interrupt
IRQ_CROSSBAR_248	MAILBOX4_IRQ_USER3	MAILBOX4	Mailbox 4 user 3 interrupt
IRQ_CROSSBAR_249	MAILBOX5_IRQ_USER0	MAILBOX5	Mailbox 5 user 0 interrupt
IRQ_CROSSBAR_250	MAILBOX5_IRQ_USER1	MAILBOX5	Mailbox 5 user 1 interrupt
IRQ_CROSSBAR_251	MAILBOX5_IRQ_USER2	MAILBOX5	Mailbox 5 user 2 interrupt
IRQ_CROSSBAR_252	MAILBOX5_IRQ_USER3	MAILBOX5	Mailbox 5 user 3 interrupt
IRQ_CROSSBAR_253	MAILBOX6_IRQ_USER0	MAILBOX6	Mailbox 6 user 0 interrupt
IRQ_CROSSBAR_254	MAILBOX6_IRQ_USER1	MAILBOX6	Mailbox 6 user 1 interrupt
IRQ_CROSSBAR_255	MAILBOX6_IRQ_USER2	MAILBOX6	Mailbox 6 user 2 interrupt
IRQ_CROSSBAR_256	MAILBOX6_IRQ_USER3	MAILBOX6	Mailbox 6 user 3 interrupt
IRQ_CROSSBAR_257	MAILBOX7_IRQ_USER0	MAILBOX7	Mailbox 7 user 0 interrupt
IRQ_CROSSBAR_258	MAILBOX7_IRQ_USER1	MAILBOX7	Mailbox 7 user 1 interrupt
IRQ_CROSSBAR_259	MAILBOX7_IRQ_USER2	MAILBOX7	Mailbox 7 user 2 interrupt
IRQ_CROSSBAR_260	MAILBOX7_IRQ_USER3	MAILBOX7	Mailbox 7 user 3 interrupt
IRQ_CROSSBAR_261	MAILBOX8_IRQ_USER0	MAILBOX8	Mailbox 8 user 0 interrupt
IRQ_CROSSBAR_262	MAILBOX8_IRQ_USER1	MAILBOX8	Mailbox 8 user 1 interrupt
IRQ_CROSSBAR_263	MAILBOX8_IRQ_USER2	MAILBOX8	Mailbox 8 user 2 interrupt
IRQ_CROSSBAR_264	MAILBOX8_IRQ_USER3	MAILBOX8	Mailbox 8 user 3 interrupt
IRQ_CROSSBAR_265	MAILBOX9_IRQ_USER0	MAILBOX9	Mailbox 9 user 0 interrupt
IRQ_CROSSBAR_266	MAILBOX9_IRQ_USER1	MAILBOX9	Mailbox 9 user 1 interrupt
IRQ_CROSSBAR_267	MAILBOX9_IRQ_USER2	MAILBOX9	Mailbox 9 user 2 interrupt
IRQ_CROSSBAR_268	MAILBOX9_IRQ_USER3	MAILBOX9	Mailbox 9 user 3 interrupt
IRQ_CROSSBAR_269	MAILBOX10_IRQ_USER0	MAILBOX10	Mailbox 10 user 0 interrupt
IRQ_CROSSBAR_270	MAILBOX10_IRQ_USER1	MAILBOX10	Mailbox 10 user 1 interrupt
IRQ_CROSSBAR_271	MAILBOX10_IRQ_USER2	MAILBOX10	Mailbox 10 user 2 interrupt
IRQ_CROSSBAR_272	MAILBOX10_IRQ_USER3	MAILBOX10	Mailbox 10 user 3 interrupt
IRQ_CROSSBAR_273	MAILBOX11_IRQ_USER0	MAILBOX11	Mailbox 11 user 0 interrupt
IRQ_CROSSBAR_274	MAILBOX11_IRQ_USER1	MAILBOX11	Mailbox 11 user 1 interrupt
IRQ_CROSSBAR_275	MAILBOX11_IRQ_USER2	MAILBOX11	Mailbox 11 user 2 interrupt
IRQ_CROSSBAR_276	MAILBOX11_IRQ_USER3	MAILBOX11	Mailbox 11 user 3 interrupt
IRQ_CROSSBAR_277	MAILBOX12_IRQ_USER0	MAILBOX12	Mailbox 12 user 0 interrupt
IRQ_CROSSBAR_278	MAILBOX12_IRQ_USER1	MAILBOX12	Mailbox 12 user 1 interrupt
IRQ_CROSSBAR_279	MAILBOX12_IRQ_USER2	MAILBOX12	Mailbox 12 user 2 interrupt
IRQ_CROSSBAR_280	MAILBOX12_IRQ_USER3	MAILBOX12	Mailbox 12 user 3 interrupt
IRQ_CROSSBAR_281	EVE1_IRQ_TPCC_REGION1[4]	EVE1	EVE1 TPCC region 1 interrupt

[4] ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_282	EVE1_IRQ_TPCC_REGION2[4]	EVE1	EVE1 TPCC region 2 interrupt
IRQ_CROSSBAR_283	EVE1_IRQ_TPCC_REGION3[4]	EVE1	EVE1 TPCC region 3 interrupt
IRQ_CROSSBAR_284	EVE1_IRQ_MBX0_USER1[4]	EVE1	EVE1 mailbox 0 user 1 interrupt
IRQ_CROSSBAR_285	EVE1_IRQ_MBX0_USER2[4]	EVE1	EVE1 mailbox 0 user 2 interrupt
IRQ_CROSSBAR_286	EVE1_IRQ_MBX0_USER3[4]	EVE1	EVE1 mailbox 0 user 3 interrupt
IRQ_CROSSBAR_287	EVE1_IRQ_MBX1_USER1[4]	EVE1	EVE1 mailbox 1 user 1 interrupt
IRQ_CROSSBAR_288	EVE1_IRQ_MBX1_USER2[4]	EVE1	EVE1 mailbox 1 user 2 interrupt
IRQ_CROSSBAR_289	EVE1_IRQ_MBX1_USER3[4]	EVE1	EVE1 mailbox 1 user 3 interrupt
IRQ_CROSSBAR_290	EVE2_IRQ_TPCC_REGION1[4]	EVE2	EVE2 TPCC region 1 interrupt
IRQ_CROSSBAR_291	EVE2_IRQ_TPCC_REGION2[4]	EVE2	EVE2 TPCC region 2 interrupt
IRQ_CROSSBAR_292	EVE2_IRQ_TPCC_REGION3[4]	EVE2	EVE2 TPCC region 3 interrupt
IRQ_CROSSBAR_293	EVE2_IRQ_MBX0_USER1[4]	EVE2	EVE2 mailbox 0 user 1 interrupt
IRQ_CROSSBAR_294	EVE2_IRQ_MBX0_USER2[4]	EVE2	EVE2 mailbox 0 user 2 interrupt
IRQ_CROSSBAR_295	EVE2_IRQ_MBX0_USER3[4]	EVE2	EVE2 mailbox 0 user 3 interrupt
IRQ_CROSSBAR_296	EVE2_IRQ_MBX1_USER1[4]	EVE2	EVE2 mailbox 1 user 1 interrupt
IRQ_CROSSBAR_297	EVE2_IRQ_MBX1_USER2[4]	EVE2	EVE2 mailbox 1 user 2 interrupt
IRQ_CROSSBAR_298	EVE2_IRQ_MBX1_USER3[4]	EVE2	EVE2 mailbox 1 user 3 interrupt
IRQ_CROSSBAR_299	EVE3_IRQ_TPCC_REGION1[4]	EVE3	EVE3 TPCC region 1 interrupt
IRQ_CROSSBAR_300	EVE3_IRQ_TPCC_REGION2[4]	EVE3	EVE3 TPCC region 2 interrupt
IRQ_CROSSBAR_301	EVE3_IRQ_TPCC_REGION3[4]	EVE3	EVE3 TPCC region 3 interrupt
IRQ_CROSSBAR_302	EVE3_IRQ_MBX0_USER1[4]	EVE3	EVE3 mailbox 0 user 1 interrupt
IRQ_CROSSBAR_303	EVE3_IRQ_MBX0_USER2[4]	EVE3	EVE3 mailbox 0 user 2 interrupt
IRQ_CROSSBAR_304	EVE3_IRQ_MBX0_USER3[4]	EVE3	EVE3 mailbox 0 user 3 interrupt
IRQ_CROSSBAR_305	EVE3_IRQ_MBX1_USER1[4]	EVE3	EVE3 mailbox 1 user 1 interrupt
IRQ_CROSSBAR_306	EVE3_IRQ_MBX1_USER2[5]	EVE3	EVE3 mailbox 1 user 2 interrupt
IRQ_CROSSBAR_307	EVE3_IRQ_MBX1_USER3[5]	EVE3	EVE3 mailbox 1 user 3 interrupt
IRQ_CROSSBAR_308	EVE4_IRQ_TPCC_REGION1[5]	EVE4	EVE4 TPCC region 1 interrupt
IRQ_CROSSBAR_309	EVE4_IRQ_TPCC_REGION2[5]	EVE4	EVE4 TPCC region 2 interrupt
IRQ_CROSSBAR_310	EVE4_IRQ_TPCC_REGION3[5]	EVE4	EVE4 TPCC region 3 interrupt
IRQ_CROSSBAR_311	EVE4_IRQ_MBX0_USER1[5]	EVE4	EVE4 mailbox 0 user 1 interrupt
IRQ_CROSSBAR_312	EVE4_IRQ_MBX0_USER2[5]	EVE4	EVE4 mailbox 0 user 2 interrupt
IRQ_CROSSBAR_313	EVE4_IRQ_MBX0_USER3[5]	EVE4	EVE4 mailbox 0 user 3 interrupt
IRQ_CROSSBAR_314	EVE4_IRQ_MBX1_USER1[5]	EVE4	EVE4 mailbox 1 user 1 interrupt
IRQ_CROSSBAR_315	EVE4_IRQ_MBX1_USER2[5]	EVE4	EVE4 mailbox 1 user 2 interrupt
IRQ_CROSSBAR_316	EVE4_IRQ_MBX1_USER3[5]	EVE4	EVE4 mailbox 1 user 3 interrupt
IRQ_CROSSBAR_317	DSP1_IRQ_TPCC_ERR	DSP1	DSP1 TPCC error interrupt
IRQ_CROSSBAR_318	DSP1_IRQ_TPCC_GLOBAL	DSP1	DSP1 TPCC global interrupt
IRQ_CROSSBAR_319	DSP1_IRQ_TPCC_REGION0	DSP1	DSP1 TPCC region 0 interrupt
IRQ_CROSSBAR_320	DSP1_IRQ_TPCC_REGION1	DSP1	DSP1 TPCC region 1 interrupt
IRQ_CROSSBAR_321	DSP1_IRQ_TPCC_REGION2	DSP1	DSP1 TPCC region 2 interrupt
IRQ_CROSSBAR_322	DSP1_IRQ_TPCC_REGION3	DSP1	DSP1 TPCC region 3 interrupt
IRQ_CROSSBAR_323	DSP1_IRQ_TPCC_REGION4	DSP1	DSP1 TPCC region 4 interrupt
IRQ_CROSSBAR_324	DSP1_IRQ_TPCC_REGION5	DSP1	DSP1 TPCC region 5 interrupt
IRQ_CROSSBAR_325	DSP2_IRQ_TPCC_ERR	DSP2	DSP2 TPCC error interrupt
IRQ_CROSSBAR_326	DSP2_IRQ_TPCC_GLOBAL	DSP2	DSP2 TPCC global interrupt
IRQ_CROSSBAR_327	DSP2_IRQ_TPCC_REGION0	DSP2	DSP2 TPCC region 0 interrupt

(5) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_328	DSP2_IRQ_TPCC_REGION1	DSP2	DSP2 TPCC region 1 interrupt
IRQ_CROSSBAR_329	DSP2_IRQ_TPCC_REGION2	DSP2	DSP2 TPCC region 2 interrupt
IRQ_CROSSBAR_330	DSP2_IRQ_TPCC_REGION3	DSP2	DSP2 TPCC region 3 interrupt
IRQ_CROSSBAR_331	DSP2_IRQ_TPCC_REGION4	DSP2	DSP2 TPCC region 4 interrupt
IRQ_CROSSBAR_332	DSP2_IRQ_TPCC_REGION5	DSP2	DSP2 TPCC region 5 interrupt
IRQ_CROSSBAR_333	MMU1_IRQ	MMU1	Top level MMU1 interrupt
IRQ_CROSSBAR_334	GMAC_SW_IRQ_RX_THRESH_PULSE	GMAC_SW	GMAC_SW receive threshold interrupt
IRQ_CROSSBAR_335	GMAC_SW_IRQ_RX_PULSE	GMAC_SW	GMAC_SW receive interrupt
IRQ_CROSSBAR_336	GMAC_SW_IRQ_TX_PULSE	GMAC_SW	GMAC_SW transmit interrupt
IRQ_CROSSBAR_337	GMAC_SW_IRQ_MISC_PULSE	GMAC_SW	GMAC_SW miscellaneous interrupt
IRQ_CROSSBAR_338	Reserved	Reserved	Reserved
IRQ_CROSSBAR_339	TIMER13_IRQ	TIMER13	TIMER13 interrupt
IRQ_CROSSBAR_340	TIMER14_IRQ	TIMER14	TIMER14 interrupt
IRQ_CROSSBAR_341	TIMER15_IRQ	TIMER15	TIMER15 interrupt
IRQ_CROSSBAR_342	TIMER16_IRQ	TIMER16	TIMER16 interrupt
IRQ_CROSSBAR_343	QSPI_IRQ	QSPI	QSPI interrupt
IRQ_CROSSBAR_344	USB3_IRQ_INTR1 (5)	USB3	USB3 interrupt 1
IRQ_CROSSBAR_345	USB4_IRQ_INTR0 (5)	USB4	USB4 interrupt 0
IRQ_CROSSBAR_346	USB4_IRQ_INTR1 (5)	USB4	USB4 interrupt 1
IRQ_CROSSBAR_347	GPIO7_IRQ_2	GPIO7	GPIO7 interrupt 2
IRQ_CROSSBAR_348	GPIO8_IRQ_2	GPIO8	GPIO8 interrupt 2
IRQ_CROSSBAR_349	Reserved	Reserved	Reserved
IRQ_CROSSBAR_350	Reserved	Reserved	Reserved
IRQ_CROSSBAR_351	VIP1_IRQ_1	VIP1	VIP1 interrupt 1
IRQ_CROSSBAR_352	VIP2_IRQ_1	VIP2	VIP2 interrupt 1
IRQ_CROSSBAR_354	VPE_IRQ	VPE	VPE interrupt
IRQ_CROSSBAR_355	PCIe_SS2_IRQ_INT0	PCIe_SS2	PCIe_SS2 interrupt 0
IRQ_CROSSBAR_356	PCIe_SS2_IRQ_INT1	PCIe_SS2	PCIe_SS2 interrupt 1
IRQ_CROSSBAR_357	Reserved	Reserved	Reserved
IRQ_CROSSBAR_358	Reserved	Reserved	Reserved
IRQ_CROSSBAR_359	EDMA_TPCC_IRQ_ERR	EDMA TPCC	EDMA TPCC error interrupt
IRQ_CROSSBAR_360	EDMA_TPCC_IRQ_MP	EDMA TPCC	EDMA TPCC memory protection interrupt
IRQ_CROSSBAR_361	EDMA_TPCC_IRQ_REGION0	EDMA TPCC	EDMA TPCC region 0 interrupt
IRQ_CROSSBAR_362	EDMA_TPCC_IRQ_REGION1	EDMA TPCC	EDMA TPCC region 1 interrupt
IRQ_CROSSBAR_363	EDMA_TPCC_IRQ_REGION2	EDMA TPCC	EDMA TPCC region 2 interrupt
IRQ_CROSSBAR_364	EDMA_TPCC_IRQ_REGION3	EDMA TPCC	EDMA TPCC region 3 interrupt
IRQ_CROSSBAR_365	EDMA_TPCC_IRQ_REGION4	EDMA TPCC	EDMA TPCC region 4 interrupt
IRQ_CROSSBAR_366	EDMA_TPCC_IRQ_REGION5	EDMA TPCC	EDMA TPCC region 5 interrupt
IRQ_CROSSBAR_367	EDMA_TPCC_IRQ_REGION6	EDMA TPCC	EDMA TPCC region 6 interrupt
IRQ_CROSSBAR_368	EDMA_TPCC_IRQ_REGION7	EDMA TPCC	EDMA TPCC region 7 interrupt
IRQ_CROSSBAR_369	MMU2_IRQ	MMU2	Top level MMU2 interrupt
IRQ_CROSSBAR_370	EDMA_TC0_IRQ_ERR	EDMA TC0	EDMA TPTC0 error interrupt
IRQ_CROSSBAR_371	EDMA_TC1_IRQ_ERR	EDMA TC1	EDMA TPTC1 error interrupt
IRQ_CROSSBAR_372	OCMC_RAM1_IRQ_CBUF	OCMC_RAM1	OCMC_RAM1 CBUF interrupt
IRQ_CROSSBAR_373	OCMC_RAM2_IRQ_CBUF	OCMC_RAM2	OCMC_RAM2 CBUF interrupt
IRQ_CROSSBAR_374	OCMC_RAM3_IRQ_CBUF	OCMC_RAM3	OCMC_RAM3 CBUF interrupt

Table 17-13. Connection of Device IRQs to IRQ_CROSSBAR Inputs (continued)

IRQ_CROSSBAR Input	Interrupt Name	Interrupt Source	Description
IRQ_CROSSBAR_375	DSP1_IRQ_TPCC_REGION6	DSP1	DSP1 TPCC region 6 interrupt
IRQ_CROSSBAR_376	DSP1_IRQ_TPCC_REGION7	DSP1	DSP1 TPCC region 7 interrupt
IRQ_CROSSBAR_377	DSP2_IRQ_TPCC_REGION6	DSP2	DSP2 TPCC region 6 interrupt
IRQ_CROSSBAR_378	DSP2_IRQ_TPCC_REGION7	DSP2	DSP2 TPCC region 7 interrupt
IRQ_CROSSBAR_379	MAILBOX13_IRQ_USER0	MAILBOX13	Mailbox 13 user 0 interrupt
IRQ_CROSSBAR_380	MAILBOX13_IRQ_USER1	MAILBOX13	Mailbox 13 user 1 interrupt
IRQ_CROSSBAR_381	MAILBOX13_IRQ_USER2	MAILBOX13	Mailbox 13 user 2 interrupt
IRQ_CROSSBAR_382	MAILBOX13_IRQ_USER3	MAILBOX13	Mailbox 13 user 3 interrupt
IRQ_CROSSBAR_383	Reserved	Reserved	Reserved
IRQ_CROSSBAR_384	Reserved	Reserved	Reserved
IRQ_CROSSBAR_385	Reserved	Reserved	Reserved
IRQ_CROSSBAR_386	PRM_IRQ_IPU2	PRM	PRCM interrupt to IPU2
IRQ_CROSSBAR_387	PRM_IRQ_DSP2	PRM	PRCM interrupt to DSP2
IRQ_CROSSBAR_388	PRM_IRQ_EVE1	PRM	PRCM interrupt to EVE1
IRQ_CROSSBAR_389	PRM_IRQ_EVE2	PRM	PRCM interrupt to EVE2
IRQ_CROSSBAR_390	Reserved	Reserved	Reserved
IRQ_CROSSBAR_391	Reserved	Reserved	Reserved
IRQ_CROSSBAR_392	VIP1_IRQ_2	VIP1	VIP1 interrupt 2
IRQ_CROSSBAR_393	VIP2_IRQ_2	VIP2	VIP2 interrupt 2
IRQ_CROSSBAR_395	IPU1_IRQ_MMU	IPU1	IPU1 MMU interrupt
IRQ_CROSSBAR_396	IPU2_IRQ_MMU	IPU2	IPU2 MMU interrupt
IRQ_CROSSBAR_397	MLB_IRQ(6)	MLB	MLB interrupt
IRQ_CROSSBAR_398	EVE1_IRQ_TPCC_REGION4(6)	EVE1	EVE1 TPCC region 4 interrupt
IRQ_CROSSBAR_399	EVE2_IRQ_TPCC_REGION4(6)	EVE2	EVE2 TPCC region 4 interrupt
IRQ_CROSSBAR_400	EVE3_IRQ_TPCC_REGION4(7)	EVE3	EVE3 TPCC region 4 interrupt
IRQ_CROSSBAR_401	EVE4_IRQ_TPCC_REGION4(7)	EVE4	EVE4 TPCC region 4 interrupt
IRQ_CROSSBAR_[402:419]	Reserved	Reserved	Reserved

(6) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.
(7) ATL, VCP, EVE, MLB, USB3 (ULPI), and USB4 (ULPI) are not supported in this family of devices.

17.4 Interrupt Controllers Functional Description

For detailed information about each device INTC (including functional description and registers descriptions), see the TRM chapters and ARM documents referenced in Section 17.1, *Interrupt Controllers Overview*.