Xilinx Zynq FPGA, TI DSP,MCU
프로그래밍 및 회로 설계 전문가 과정

김현, 최준호 PWM
문서화

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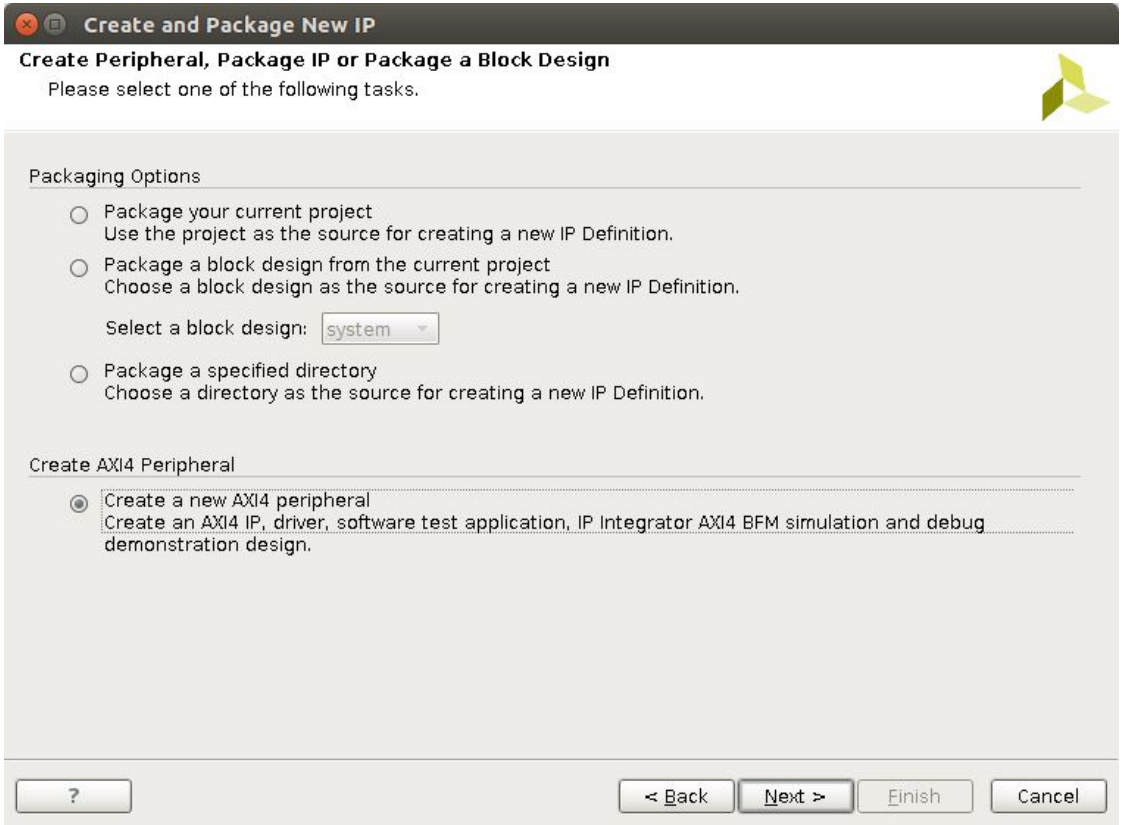
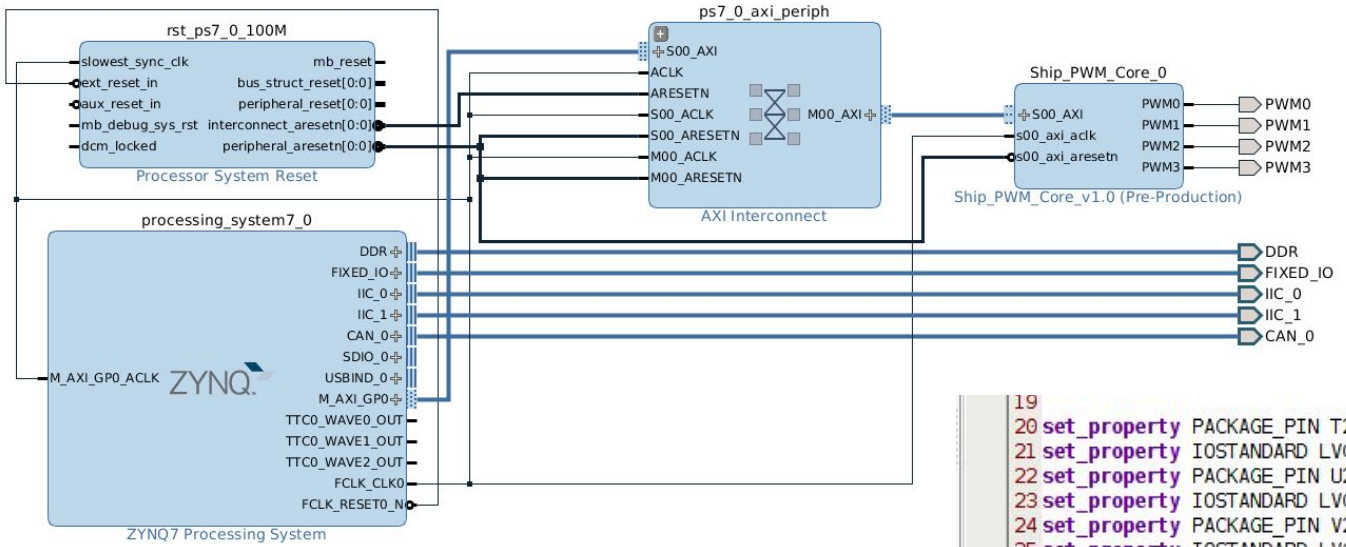
LiDAR App

PWM Custom IP 만들기



Zynq에는 PWM IP가 따로 하드코어로존재하지 않기 때문에 PL을 활용하여 새로 Custom IP를 만들어야 한다.

PWM Custom IP 만들기




```
19
20 set_property PACKAGE_PIN T20 [get_ports PWM0]
21 set_property IOSTANDARD LVCMOS33 [get_ports PWM0]
22 set_property PACKAGE_PIN U20 [get_ports PWM1]
23 set_property IOSTANDARD LVCMOS33 [get_ports PWM1]
24 set_property PACKAGE_PIN V20 [get_ports PWM2]
25 set_property IOSTANDARD LVCMOS33 [get_ports PWM2]
26 set_property PACKAGE_PIN W20 [get_ports PWM3]
27 set_property IOSTANDARD LVCMOS33 [get_ports PWM3]
```

생성한 Custom IP를 추가하고 .xdc에서 핀 제약을 설정한다.

PWM Custom IP 만들기

Peripheral Drivers

Drivers present in the Board Support Package.

Ship_PWM_Core_0	Ship_PWM_Core		
ps7_afi_0	generic	Documentation	
ps7_afi_1	generic	Documentation	
ps7_afi_2	generic	Documentation	
ps7_afi_3	generic	Documentation	
ps7_can_0	canps	Documentation	Import Examples
ps7_coresight_comp_0	coresightps_dcc	Documentation	
ps7_ddr_0	ddrps	Documentation	
ps7_ddrc_0	generic	Documentation	
ps7_dev_cfg_0	devcfg	Documentation	Import Examples
ps7_dma_ns	dmaps	Documentation	Import Examples
ps7_dma_s	dmaps	Documentation	Import Examples
ps7_ethernet_0	emacps	Documentation	Import Examples
ps7_globaltimer_0	generic	Documentation	
ps7_gpio_0	gpiops	Documentation	Import Examples

ps7_can_0	0xe0008000	0xe0008fff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER
ps7_dma_s	0xf8003000	0xf8003fff		REGISTER
ps7_iop_bus_config_0	0xe0200000	0xe0200fff		REGISTER
ps7_xadc_0	0xf8007100	0xf8007120		REGISTER
ps7_ddr_0	0x00100000	0x1fffffff		MEMORY
ps7_ddrc_0	0xf8006000	0xf8006fff		REGISTER
ps7_ocmc_0	0xf800c000	0xf800cfff		REGISTER
ps7_pl310_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_uart_1	0xe0001000	0xe0001fff		REGISTER
ps7_coresight_comp_0	0xf8800000	0xf88fffff		REGISTER
ps7_i2c_0	0xe0004000	0xe0004fff		REGISTER
ps7_ttc_0	0xf8001000	0xf8001fff		REGISTER
ps7_i2c_1	0xe0005000	0xe0005fff		REGISTER
ps7_scugic_0	0xf8f00100	0xf8f001ff		REGISTER
ps7_ethernet_0	0xe000b000	0xe000bfff		REGISTER
Ship_PWM_Core_0	0x43c00000	0x43c0ffff	S00_AXI	REGISTER
ps7_dev_cfg_0	0xf8007000	0xf80070ff		REGISTER

XSDK를 활용해 새로 추가한 PWM IP가 HDF 잘 기술 돼 있는지 확인한다.

페타리눅스로 설계 내용을 이미지로 빌드

pl.dtsi | pwm_test_f.c | test_i2c_app.c | pcw.dtsi | skeleton.dtsi

```
/*
 * CAUTION: This file is automatically generated by Xilinx.
 * Version: HSI 2015.4
 * Today is: Tue Jul  4 14:35:42 2017
*/


/ {
    amba_pl: amba_pl {
        #address-cells = <1>;
        #size-cells = <1>;
        compatible = "simple-bus";
        ranges ;
        Ship_PWM_Core_0: Ship_PWM_Core@43c00000 {
            compatible = "xlnx,Ship-PWM-Core-1.0";
            reg = <0x43c00000 0x10000>;
            xlnx,s00-axi-addr-width = <0x4>;
            xlnx,s00-axi-data-width = <0x20>;
        };
    };
};

```

페타리눅스에서 새로 생성된 IP의 정보를 잘 가져왔는지 확인하고 빌드한다.

앱 테스트

pl.dtsi | pwm_test_f.c | test_i2c_app.c | pcw.dtsi | skeleton.dtsi

```
/*
 * CAUTION: This file is automatically generated by Xilinx.
 * Version: HSI 2015.4
 * Today is: Tue Jul  4 14:35:42 2017
*/


/ {
    amba_pl: amba_pl {
        #address-cells = <1>;
        #size-cells = <1>;
        compatible = "simple-bus";
        ranges ;
        Ship_PWM_Core_0: Ship_PWM_Core@43c00000 {
            compatible = "xlnx,Ship-PWM-Core-1.0";
            reg = <0x43c00000 0x10000>;
            xlnx,s00-axi-addr-width = <0x4>;
            xlnx,s00-axi-data-width = <0x20>;
        };
    };
};

```

동영상 들어갈 부분

gpio-dev-mem 테스트 코드로 pwm이 잘 작동하는지 확인한다.
(with oscilloscope)