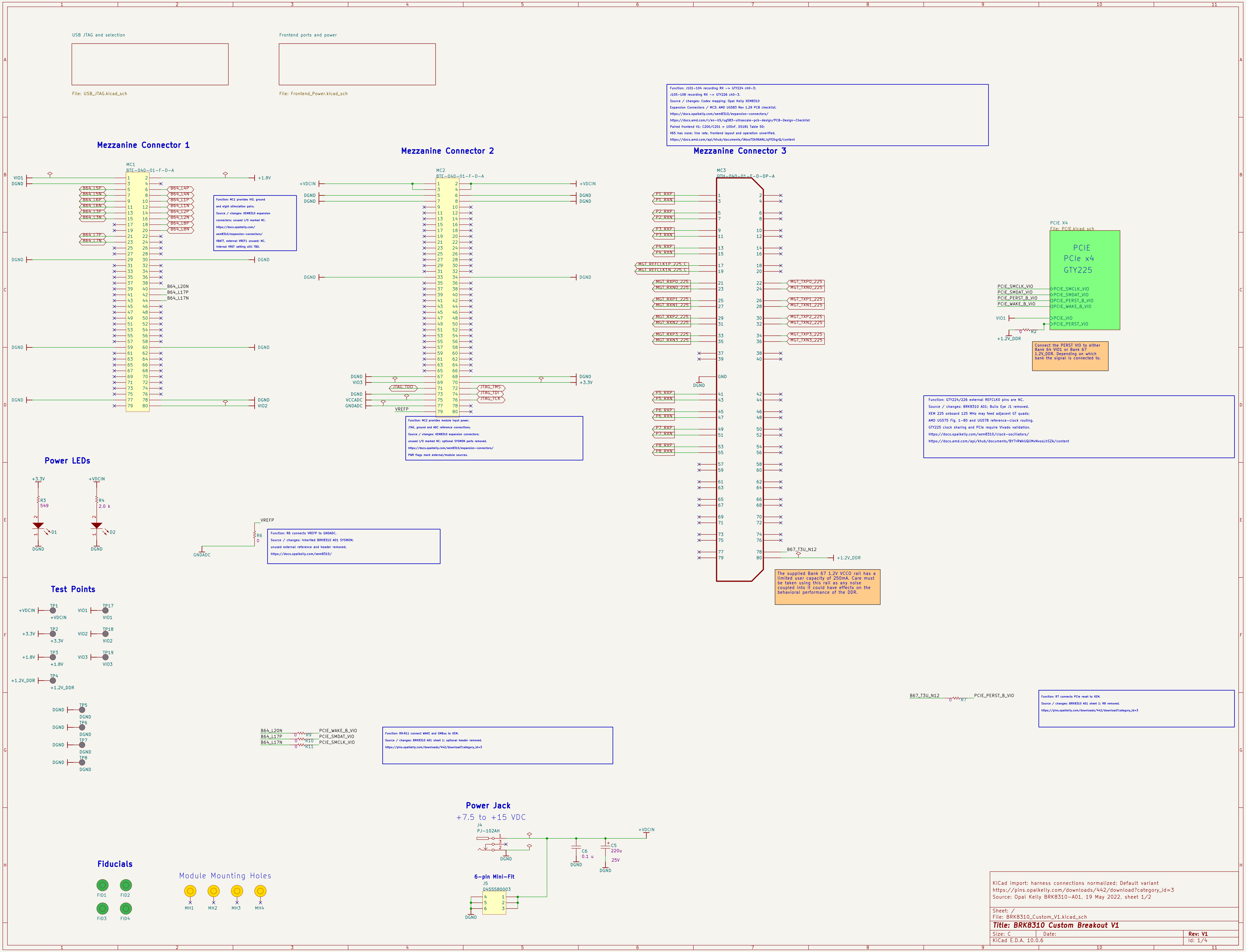


Function: J101-104 recording RX -> GTY224 ch0-3;
J105-108 recording RX -> GTY226 ch0-3.
Source / changes: Codex mapping; Opal Kelly XEM8310
Expansion Connectors / MC3; AMD UG583 Rev 1.29 PCB checklist.
https://docs.opalkelly.com/xem8310/expansion-connectors/
https://docs.amd.com/r/en-US/ug583-ultrascale-pcb-design/PCB-Design-Checklist
Paired frontend V1: C200/C201 = 100nF, DS181 Table 50;
V65 has none; line rate, frontend layout and operation unverified.
https://docs.amd.com/api/khub/documents/iAkxxTOk96ANLJqYf2hgrQ/content

Function: MC1 provides VIO, ground
and eight stimulation pairs.
Source / changes: XEM8310 expansion
connectors; unused I/O marked NC.
https://docs.opalkelly.com/
xem8310/expansion-connectors/
VBATT, external VREF1 unused; NC.
Internal VREF setting still TBD.

Function: MC2 provides module input power,
JTAG, ground and ADC reference connections.
Source / changes: XEM8310 expansion connectors;
unused I/O marked NC; optional SYSMON parts removed.
https://docs.opalkelly.com/xem8310/expansion-connectors/
PWR flags mark external/module sources.

Connect the PERST VIO to either Bank 64 VIO1 or Bank 67 1.2V_DDR. Depending on which bank the signal is connected to.

Function: GTY224/226 external REFCLK0 pins are NC.
Source / changes: BRK8310 A01; Bulls Eye J1 removed.
XEM 225 onboard 125 MHz may feed adjacent GT quads;
AMD UG575 Fig. 1-80 and UG578 reference-clock routing.
GTY225 clock sharing and PCIe require Vivado validation.
https://docs.opalkelly.com/xem8310/clock-oscillators/
https://docs.amd.com/api/khub/documents/BY7rRWkUQliMvNvosLhSZA/content

Function: R6 connects VREFP to GNDADC.
Source / changes: inherited BRK8310 A01 SYSMON;
unused external reference and header removed.
https://docs.opalkelly.com/xem8310/

The supplied Bank 67 1.2V VCCO rail has a limited user capacity of 250mA. Care must be taken using this rail as any noise coupled into it could have effects on the behavioral performance of the DDR.

Function: R7 connects PCIe reset to XEM.
Source / changes: BRK8310 A01 sheet 1; R8 removed.
https://pins.opalkelly.com/downloads/442/download?category_id=3

Function: R9-R11 connect WAKE and SMBus to XEM.
Source / changes: BRK8310 A01 sheet 1; optional header removed.
https://pins.opalkelly.com/downloads/442/download?category_id=3

KiCad import: harness connections normalized; Default variant
https://pins.opalkelly.com/downloads/442/download?category_id=3
Source: Opal Kelly BRK8310-A01, 19 May 2022, sheet 1/2

Sheet: /
File: BRK8310_Custom_V1.kicad_sch

Title: BRK8310 Custom Breakout V1

Size: C
Date:
Rev: V1
KiCad E.D.A. 10.0.6
Id: 1/4

Function: J6 provides PCIe x4 on GTY225.

Source / changes: BRK8310 A01 PCIE sheet;

lanes 4–7 and C21–C26, C29–C30 removed;

R28=0R selects the x4 PRSNT connection.

TI PCA9306 Rev O Fig 8–1: https://www.ti.com/lit/ds/symlink/pca9306.pdf

https://docs.opalkelly.com/xem8310/

brk8310–breakout–board/

REFCLK1/225 and PCIe boot need Vivado check.

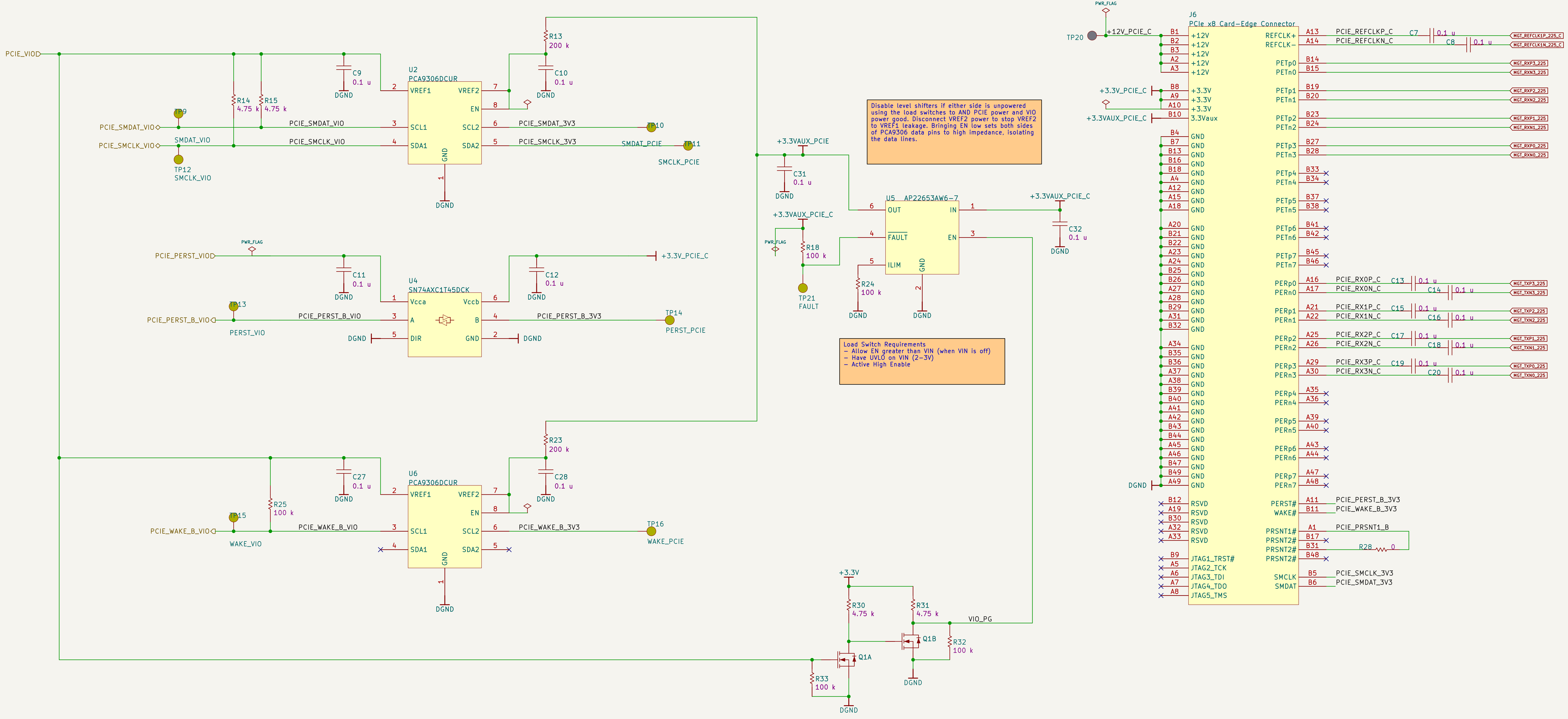
Removed DNP R12/R16/R17/R20/R21/R22/R26;

R27/R29 removed; flags mark host / R2 / bias sources.

U2/U6: 200k bias only; not a supply rail; conditional AUX.

U5 OUT pin type: Diodes DS41186 Rev4–2 p2; https://www.diodes.com/datasheet/download/AP22652_AP22653_AP22652A_AP22653A.pdf
C10/C28 0.1uF + 200k: ~20ms nominal; startup TBD.

PCIe x8 physical edge, x4 electrical



Disable level shifters if either side is unpowered using the load switches to AND PCIE power and VIO power good. Disconnect VREF2 power to stop VREF2 to VREF1 leakage. Bringing EN low sets both sides of PCA9306 data pins to high impedance, isolating the data lines.

Load Switch Requirements
- Allow EN greater than VIN (when VIN is off)
- Have UVLO on VIN (2–3V)
- Active High Enable

KiCad import: harness connections normalized; Default variant
https://pins.opalkelly.com/downloads/442/download?category_id=3
Source: Opal Kelly BRK8310–A01, 19 May 2022, sheet 2/2

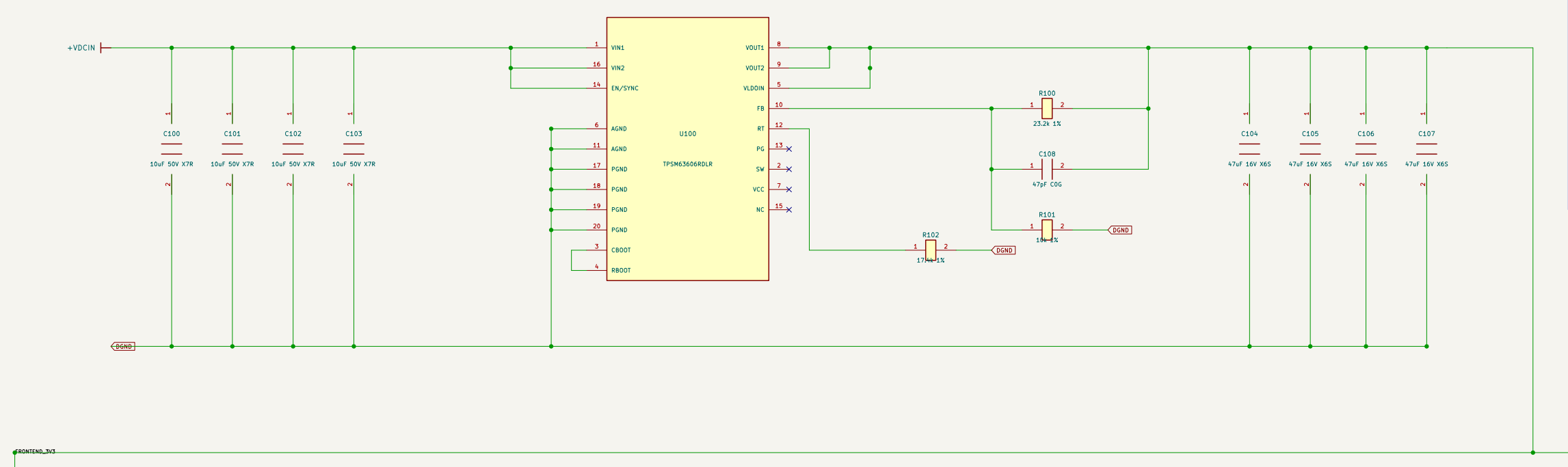
Sheet: /PCIE X4/
File: PCIE.kicad_sch

Title: BRK8310 Custom V1 – PCIe

Size: C
Date:
Rev: V1
KiCad E.D.A. 10.0.6
Id: 2/4

12 V TO 3.3 V FRONTEND SUPPLY — PROVISIONAL V1

U100 includes inductor. New rail is separate from XEM 3.3 V. Layout, inrush, filtering and thermal checks remain open.



Function: Convert BRK +VDCIN into a separate 3.3 V rail for eight frontend boards.

Source / changes: TI TPSM63606 Rev B Fig 8-1 / Table 8-1; 3.3 V feedback,

750 kHz and capacitor quantities adapted from TI EVM SLVUC93 Fig 6-1 / Table 6-1.

https://www.ti.com/lit/ds/symlink/tpsm63606.pdf

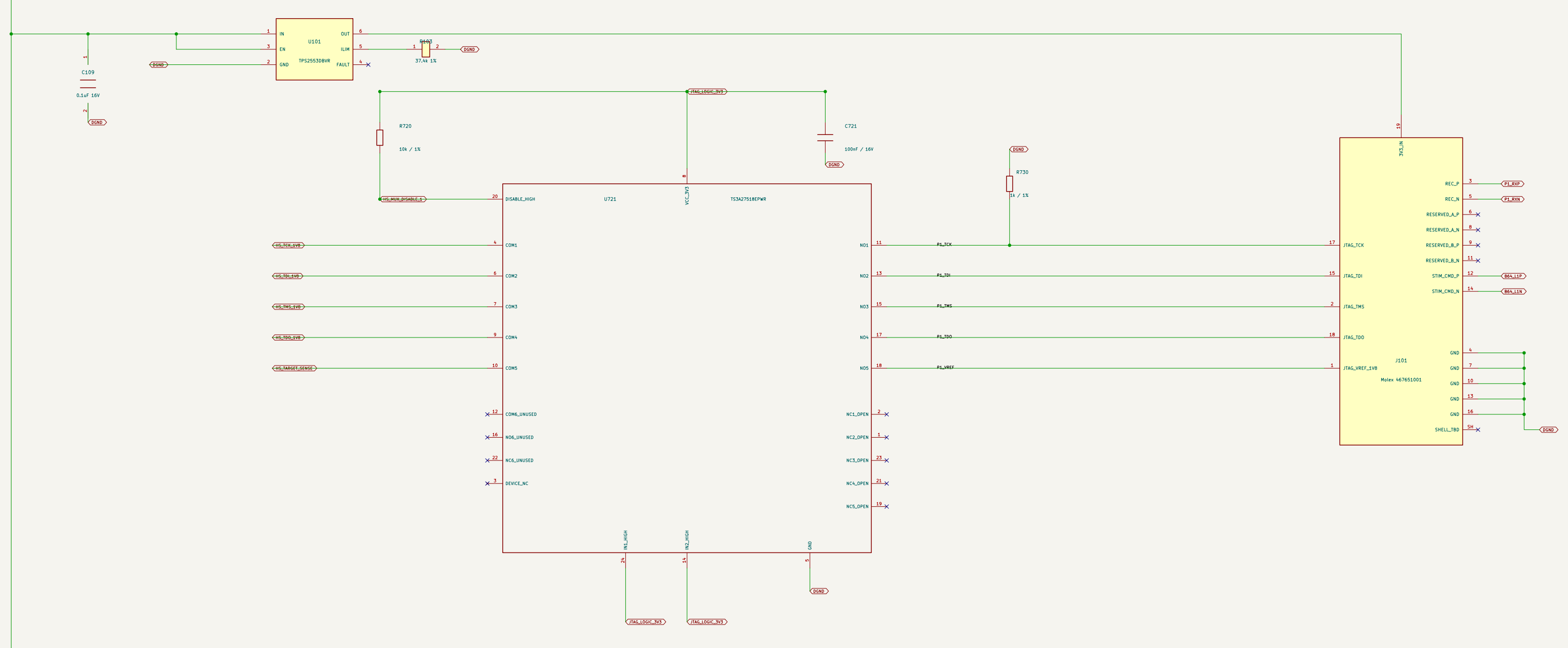
https://www.ti.com/lit/ug/slvuc93/slvuc93.pdf

Validate >=50uF effective COUT, input filtering, startup and layout/thermal performance.

U100 TI EVM footprint; PG/SW/VCC/NC open; EN auto-on; BOOT shorted; thermal vias TBD.

FRONTEND_3V3

FRONTEND 1 — J101 / U721



Function: Port 1 power and switched JTAG to J101;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

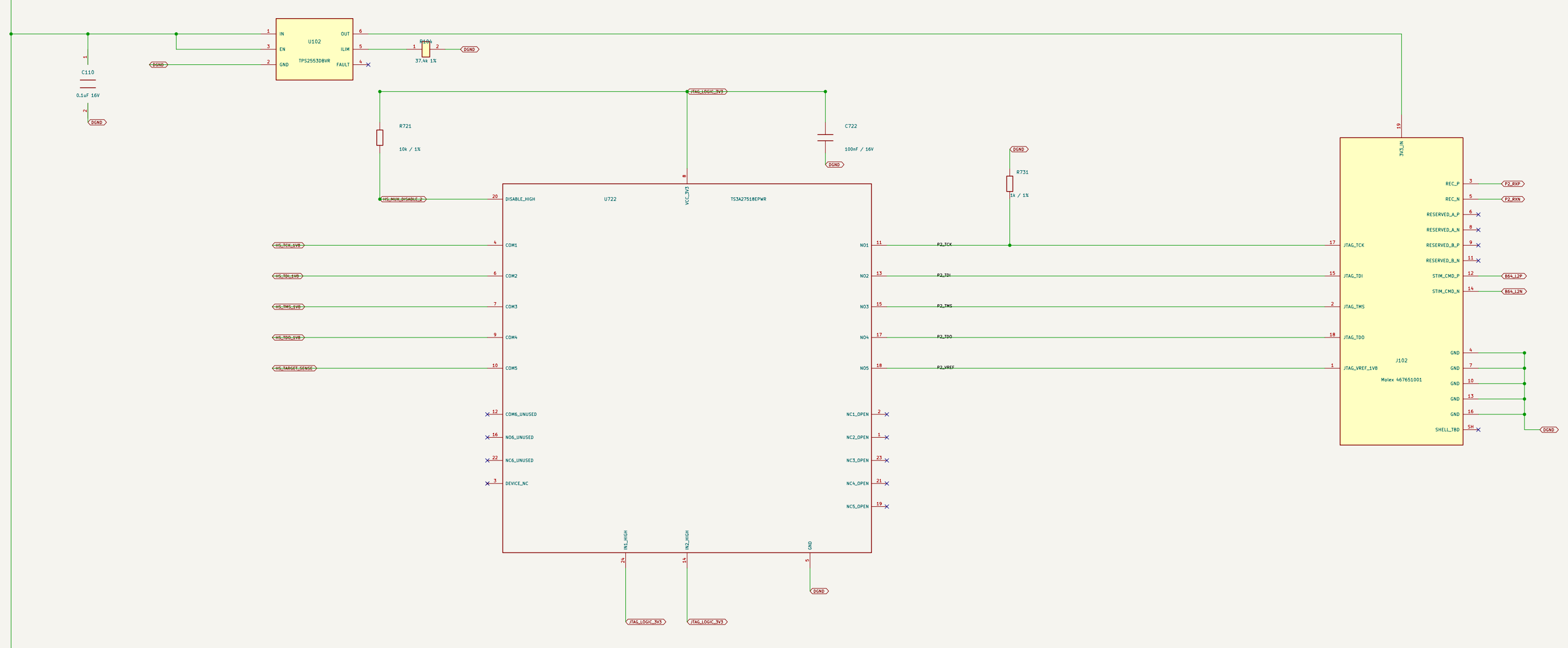
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 2 — J102 / U722



Function: Port 2 power and switched JTAG to J102;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

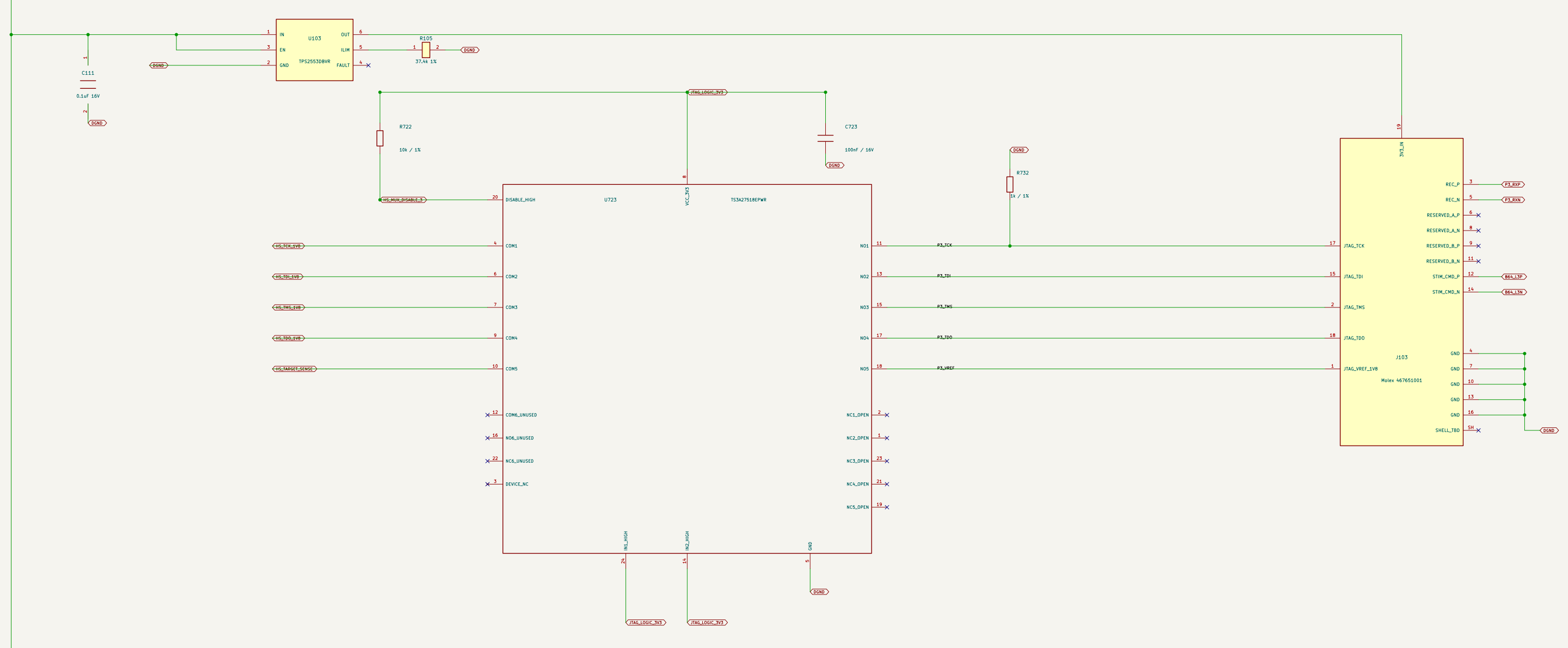
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 3 — J103 / U723



Function: Port 3 power and switched JTAG to J103;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

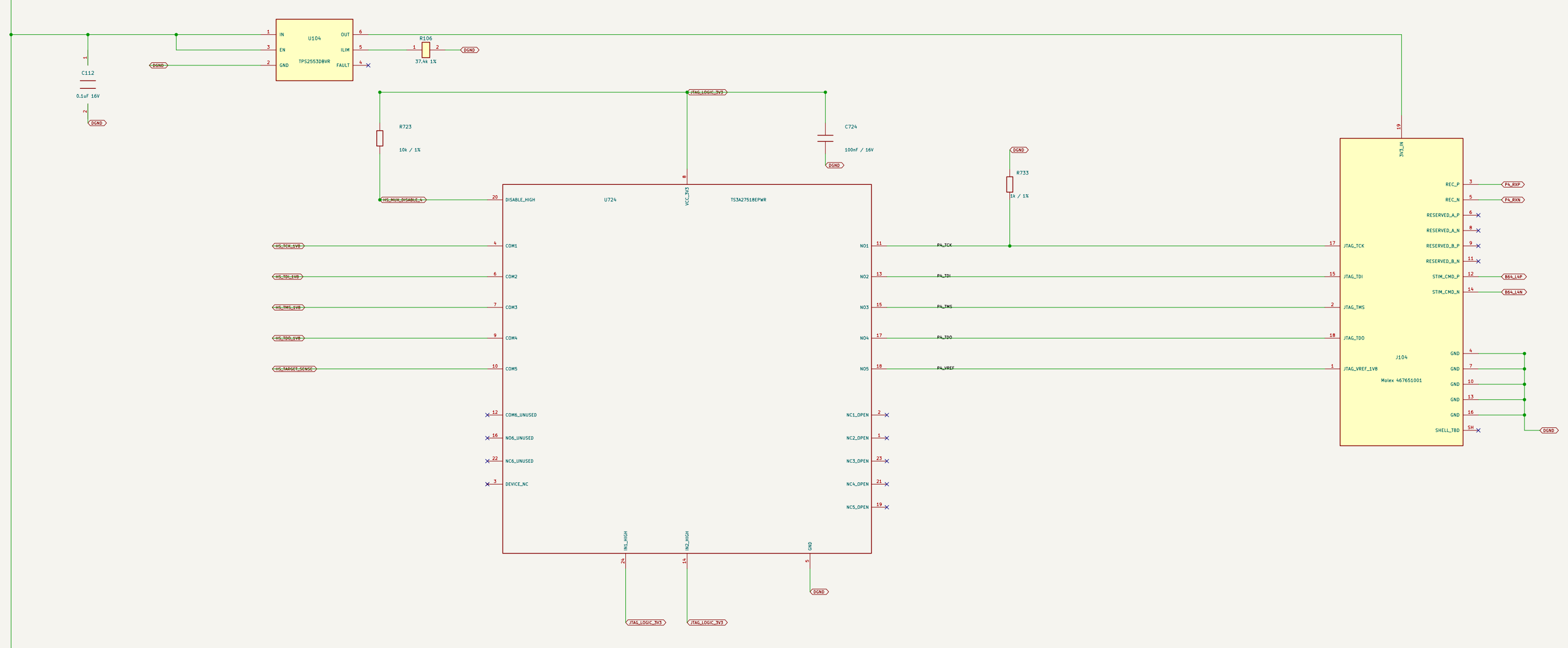
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 4 — J104 / U724



Function: Port 4 power and switched JTAG to J104;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

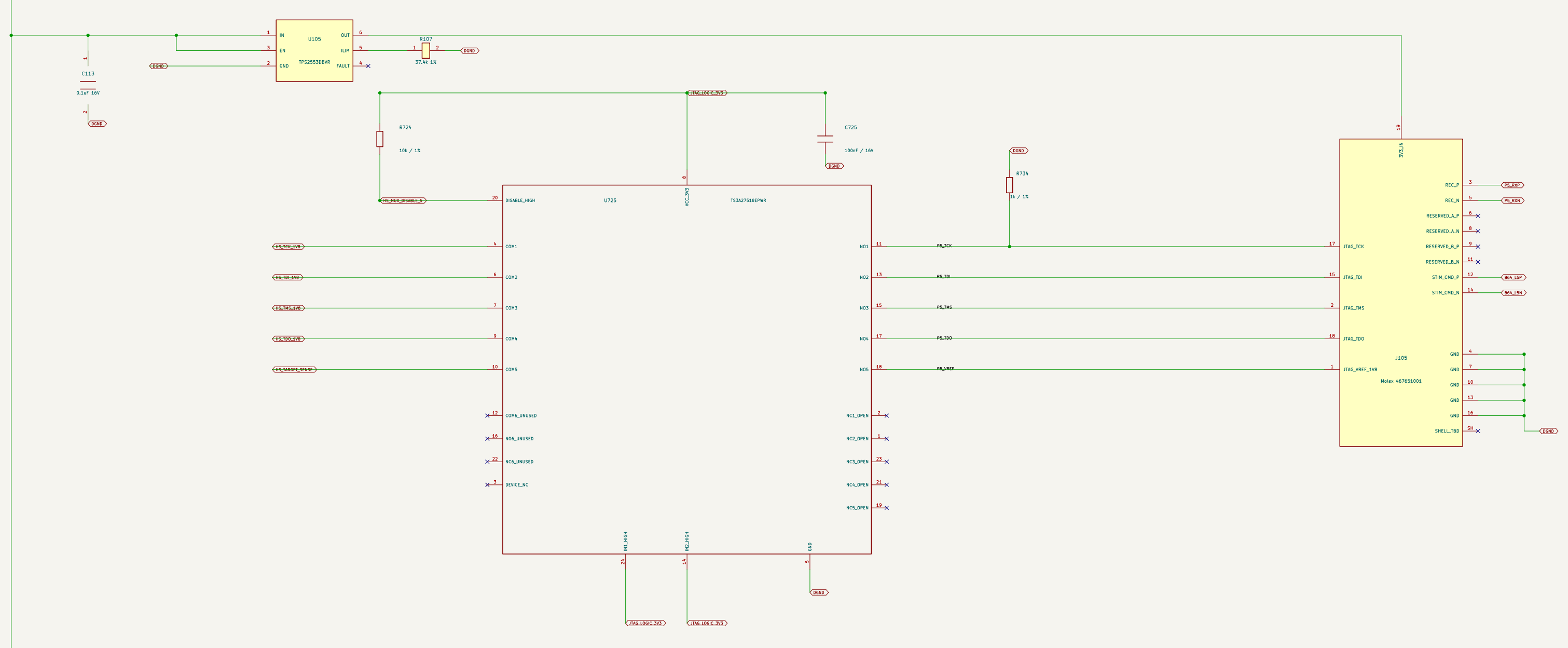
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 5 — J105 / U725



Function: Port 5 power and switched JTAG to J105;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

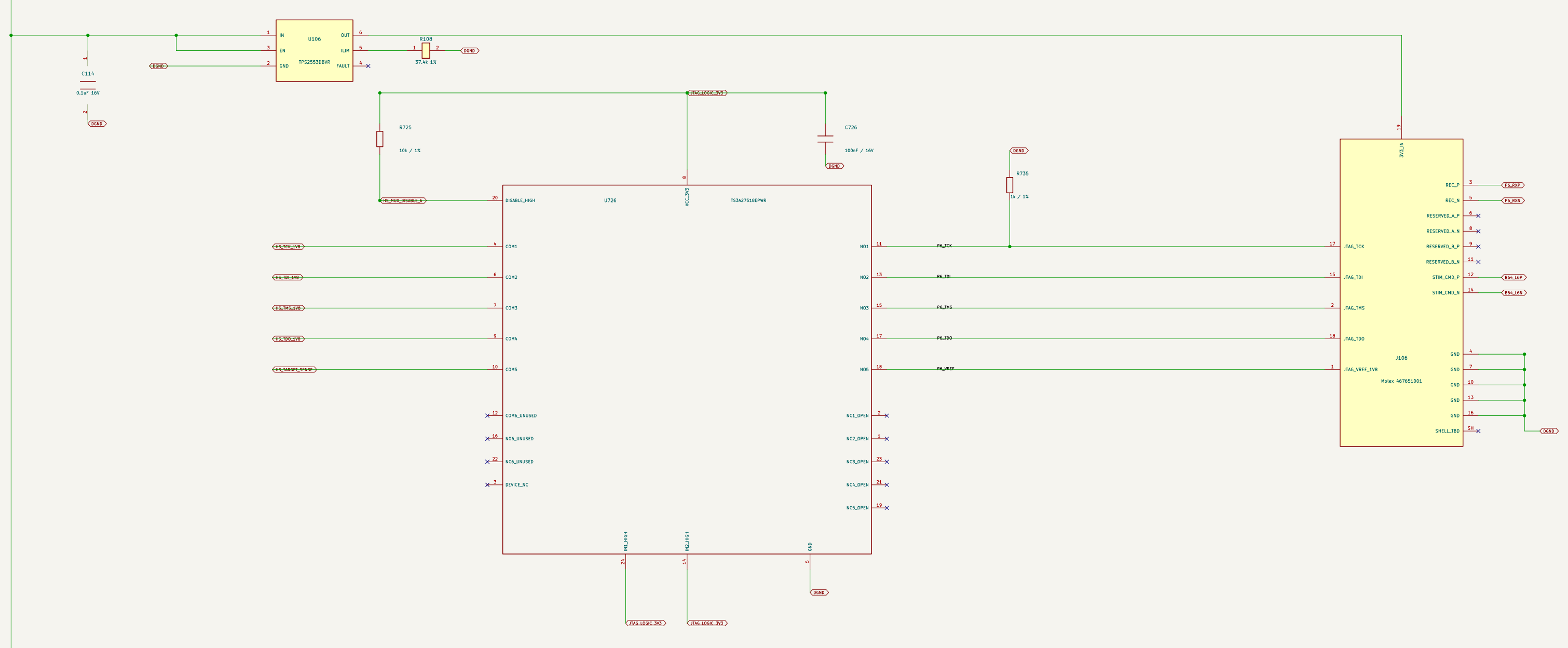
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 6 — J106 / U726



Function: Port 6 power and switched JTAG to J106;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

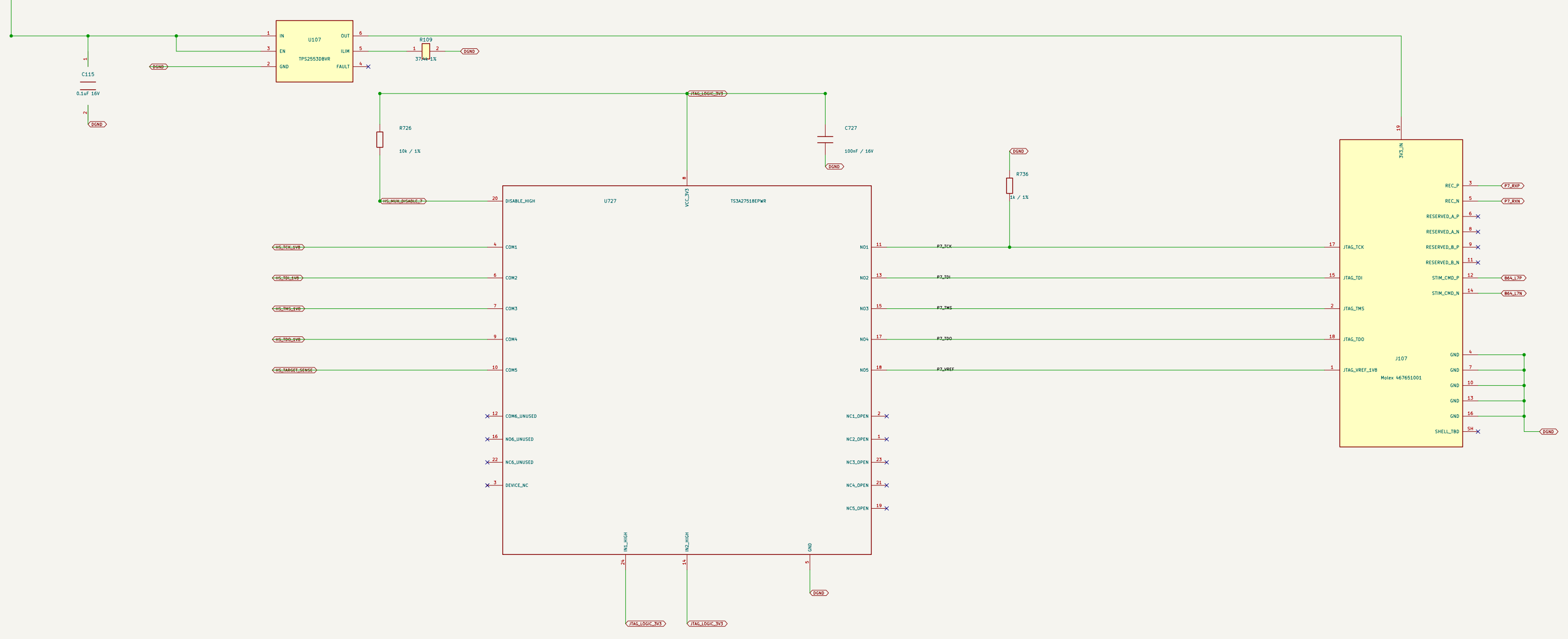
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 7 — J107 / U727



Function: Port 7 power and switched JTAG to J107;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

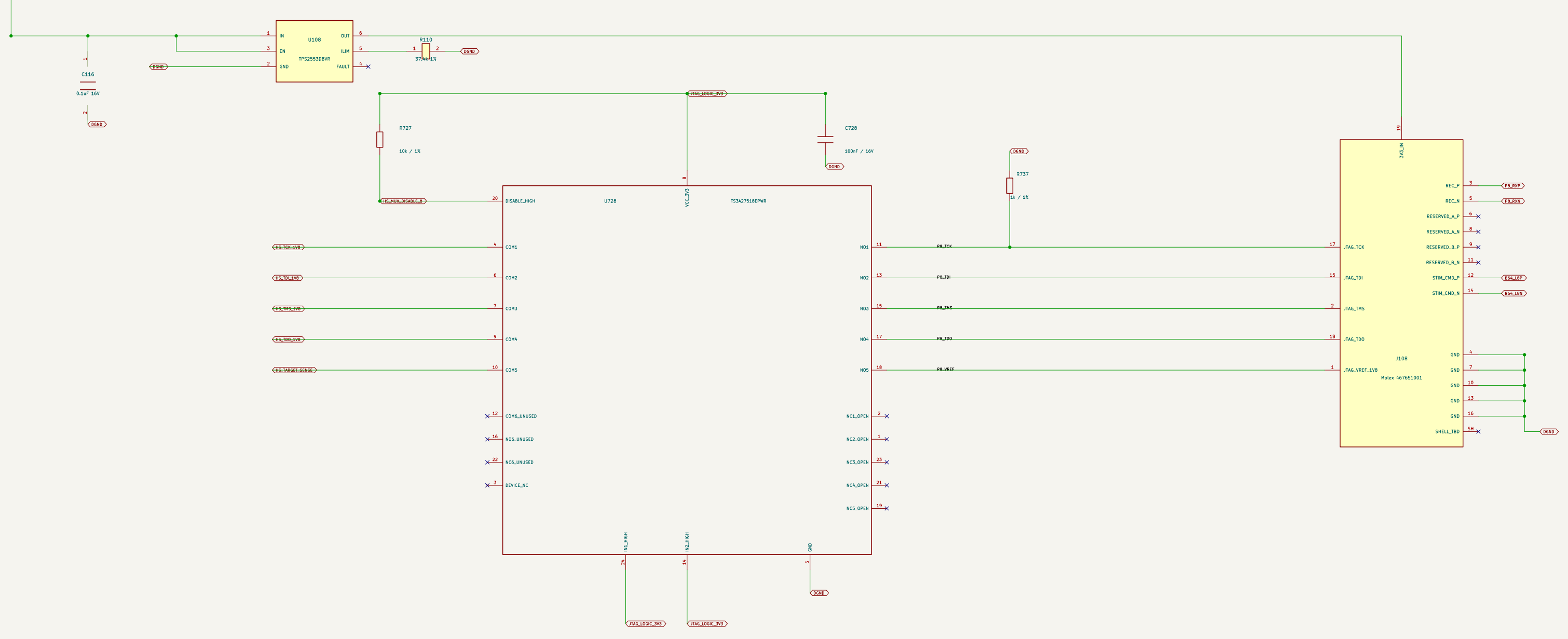
https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

FRONTEND 8 — J108 / U728



Function: Port 8 power and switched JTAG to J108;

recording RX and stimulation lines use labels to XEM.

Source / changes: Codex combined existing port + selector;

TI TPS2553 Rev F Table 2; TS3A27518E Rev F Table 8-1.

https://www.ti.com/lit/ds/symlink/tps2553.pdf

https://www.ti.com/lit/ds/symlink/ts3a27518e.pdf

AMD UG471 v1.10 Table 1-7 and Fig 1-59:

https://docs.amd.com/v/u/en-US/ug471_7Series_SelectIO

1.5 V STIM / cable / JTAG behavior remain to validate.

Added converter and 8 ports; not qualified for fabrication

Sheet: /Frontend ports and power/
File: Frontend_Power.kicad_sch

Title: BRK8310 Custom V1 — frontend power

Size: User
Date:
Rev: V1
KiCad E.D.A. 10.0.6
Id: 3/4

USB TO JTAG PROGRAMMER

Function: U501 is the USB2-to-JTAG MPSSE host. HOST_TCK/TDI/TMS
are3.3V outputs; HOST_TDO is an input. U505 stores programmer
configuration; Y500 is12MHz. USB and selector return share DGND.

Source / changes: Codex V11 adaptation from BRK8305 A03,
25Oct2023,JTAG sheet8/PDFp4:
https://pins.opalkelly.com/downloads/583/download?category_id=3
Inherited FT232HQ core values retained; all21 former USB GND
symbols now join carrier DGND. GNDADC remains unchanged.
The external BRK8310 J3 header is removed; XEM and eight
headstages use the supervised TXU0304 branches below.
R50810k retains high ADBUS4; ADBUS5-7 remain NC.
R50910k retains HOST_TDO idle bias. VCK190 UG908 wiring
requires ADBUS0-7; compatibility is unverified.
FTDI DS_FT232H v2.2,6Sep2024,sections3.3,4.1,6:
https://ftdichip.com/wp-content/uploads/2024/09/DS_FT232H.pdf
Standard93LC56B-E/MS is unprovisioned. AMD UG908,
Programming FTDI Devices for Vivado Hardware Manager Support:
https://docs.amd.com/r/en-US/ug908-vivado-programming-debugging/
Programming-FTDI-Devices-for-Vivado-Hardware-Manager-Support
program_ftdi is a provisioning path, not proof of a working cable.
No CFG001 image is supplied. Verify EEPROM programming/readback,
Vivado discovery and powered operation on the assembled board.

Function: J500 is the USB2 device input. CC1/CC2
use 5.1k pulldowns; shield uses 100nF and a
220ohm@100MHz ferrite to DGND. USB5V feeds
the FTDI core through the source filter. D500 protects data and VBUS.

Source / changes: Codex extraction from the
BRK8305 A03-derived Carrier_V1 J4 USB-C
adaptation. Original BRK J500/R500/R501/
FB503/C522; JTAG sheet8/PDFp4,25Oct2023:
https://pins.opalkelly.com/downloads/583/
download?category_id=3
GCT USB4110-GF-A revB4,22May2024,sheets1-2:
https://gct.co/files/drawings/usb4110.pdf
D500 ST USBLC6-2SC6 DS4260 Rev7 Dec2021 p1, pp3-6:
https://www.st.com/resource/en/datasheet/usblc6-2.pdf
V11 D500 moved beside J500; pins 1/6 and 3/4 exchange sides.
USB4110 SMT shell pin mapping retained;
source optional LED/probes omitted. D500 adds data/VBUS ESD protection in the
same local circuit. V11 joins USB return to carrier DGND.
USB qualification pending.

Function: U506 supplies JTAG_LOGIC_3V3 from USB5V for the selector
and branch logic. It stays separate from the FTDI3V3 internal rail.

Source / changes: Codex adapts TI TLV755P typical application,
SBVS320D,RevD,Sep2024,p1,p3Table4-1,sec6.3.2 andsec7.2.
https://www.ti.com/lit/ds/symlink/tlv755p.pdf
TLV75533PDBVR,DBV:SOT-23-5;1IN,2GND,3EN,4NC,5OUT.
EN tied to IN; C520/C521=2.2uF ceramic,chosen by Codex to allow
DC-bias margin above TI1uF effective minimum. USB current,
effective capacitance, reverse current and dissipation need review.

USB HOST TCK / TDI / TMS / TDO

18 SHARED HEADSTAGE JTAG / SEPARATE XEM + EIGHT SWITCHED PORTS

USB JTAG: SHARED EIGHT-HEADSTAGE INTERFACE + SEPARATE XEM — V1

Function: Generate the local 1.8 V translator rail from USB programmer 3.3 V. The selected target sense qualifies JTAG; this local
rail does not supply a headstage.

Source / changes: Inherited V5 Codex selector topology; TI TLV755P SBVS320D RevD Sep2024, Fig7-4 / pp3,19-21.
https://www.ti.com/lit/ds/symlink/tlv755p.pdf C600/C601 changed to2.2uF10V X7R; verify effective C>0.47uF. Local rail is not the
target supply; target qualification separately controls OE.

USB JTAG ENABLE / OFF

Function: SW700 enables or disables USB JTAG. ENABLE connects pin2 to JTAG_LOGIC_3V3; OFF connects pin2 to DGND. USB_SELECT_ENABLE_3V3 feeds the rotary common and U621 /MR. OFF disables both translator branches and all headstage switches. Stop host TCK, set OFF, select XEM or P1-P8, then ENABLE and wait at least50ms. USB remains powered.

Source / changes: Codex Adapted USB-only selector,26Oct2026. BRK8305 A03,25Oct2023,JTAG sheet8/PDFp4 supplies the USB-core precedent: https://pins.opalkelly.com/downloads/583/download?category_id=3 . BRK8310 A01,19May2022,sheet1 C4 retained, J3 removed: https://pins.opalkelly.com/downloads/442/download?category_id=3 .
U700/C700/R701/R700 from the inherited selector removed; U610 connects directly to MC2. R60010k remains the common pulldown. C&K/Littelfuse JS series,revVL01/14/26,JS202011JCQN DPDT circuit/SMT drawing: https://www.littelfuse.com/assetdocs/littelfuse-c-k-slide-js-series-datasheet?assetguid=aba42b08-0d2c-423b-813d-a2faa5a3bb14 . Only terminals1/2/3 used;5/6/7 NC.
Physical part/pads unqualified; switch symbol names describe ENABLE/OFF. Hot switching and power sequencing remain unqualified.

POS1 — XEM8310 / 1.8 V JTAG

Function: Select XEM8310 or one of eight Artix-7 cable targets. Switch positions1-9=XEM/P1-P8;10-12=OFF. SW700 OFF
drives rotary common LOW; all nine branches disable.

Source / changes: Codex adaptation retains the V9 one-hot selector; SW700 now means ENABLE/OFF. Grayhill Series56 Rev2024/10 pp1-2,4: exact56P30-01-1-12N-F
nonshorting12-position PC-mount fixed-stop switch. https://www.grayhill.com/wp-content/uploads/media/56-datasheet.pdf .
Positions1=XEM,2-9=HS1-HS8,10-12=NC(all-off). Wiper USB_SELECT_ENABLE_3V3 is unchanged. XEM MR follows SEL_0; SEL_1-8 control U710
and switch EN. One shared headstage supervisor uses USB master gating and selected sense. Hardware selection is independent of
FPGA configuration. Stop TCK; set SW700 OFF before turning, then ENABLE and wait50ms. Hot switching remains unqualified.

Function: Connect selected, powered XEM8310 directly to the USB translator. R614/R615/R616 feed MC2.76 TCK / .74 TDI / .72 TMS;
MC2.71 returns TDO to U610.10. MR LOW disables; valid target plus stable selection delays enable20ms typical(12-28ms).

Source / changes: Codex Adapted USB-only selector of BRK8310 A01,19May2022,sheet1 JTAG contact contract:
https://pins.opalkelly.com/downloads/442/download?category_id=3 . J3 removed; C4 moved beside U620 sense; U700/C700/R700/R701 from the earlier selector were removed;
U610 output labels now join existing MC2 JTAG nets. All33R resistors and supervisor/OE support remain.
The USB host derives from BRK8305 A03,25Oct2023,JTAG sheet8/PDFp4:
https://pins.opalkelly.com/downloads/583/download?category_id=3 . This is a Codex adaptation, not an unchanged BRK circuit.
TI TXU0304 SCES935A RevA Nov2021 pp4,7-8,20-25: https://www.ti.com/lit/ds/symlink/txu0304.pdf
TPS3808 SBVS050N RevN Aug2026 pp3-7,10-12: https://www.ti.com/lit/ds/symlink/tps3808.pdf
SN74LVC1G17 SCES351Y RevY Oct2025 pp3,5-7: https://www.ti.com/lit/ds/symlink/sn74lvc1g17.pdf
C4 100nF and R6121M connect to U620 1.8V SENSE; it does not join local JTAG1.8V. CT open;10k MR PD/RESET PU;100k OE PD.
Stop TCK, SW700 OFF, select XEM, then ENABLE and wait50ms. Start TCK1MHz; edge quality and powered operation unqualified.
TXU0304 replaces BRK8305 four discrete SN74AXC1T45 translators; OE gates three forward signals and one return.

SHARED EIGHT-HEADSTAGE JTAG — V1 / ONE HOT, TARGET SENSE, LOCAL 1.8V

Function: Enable the shared headstage translator only after selected target VTREF is valid.
SW700 OFF resets the enable delay; remote pin1 never supplies the translator.

Source / changes: Codex shared adaptation of TI TPS3808 SBVS050N RevN Aug2026 pp3-7,10-12
https://www.ti.com/lit/ds/symlink/tps3808.pdf and 1G17 SCES351Y pp3,5-7.
https://www.ti.com/lit/ds/symlink/sn74lvc1g17.pdf
U621 changedG18 toG01;CT open. R738140k/R73949.9k0.1% divider per Fig7-1.
R62010k RESET PU,R62268k common discharge,R623100k OE PD.
Common-bus cutoff~1.54Vnominal: target-presence gate, not qualified power-good.
Remote1.71..1.89V,R27=1k assumptions; staticDC corners screened.
Cable loss, actual regulator tolerance, rail-collapse latency and powered behavior remain unqualified.

Function: Translate shared USB JTAG3.3V to fixed local1.8V for one headstage.
All four outputs, including HOST_TDO return, are high-Z while OE is LOW.

Source / changes: Codex sharing of inherited interface; TI TXU0304 SCES935A RevA Nov2021 pp4,7-8,20-25.
https://www.ti.com/lit/ds/symlink/txu0304.pdf
U611 retained; seven duplicate translators removed. C622/C623100nF local bypass;
R624/R625/R62633R now one common output set. No local positive pullups on cable pins.
TCK starts1MHz; cable loading and edge quality need measurement.
Change targets: stop host TCK, SW700 OFF, rotate SW600, then ENABLE;
wait at least50ms before JTAG. Hot target switching is not qualified.
TXU0304 replaces BRK8305 four discrete SN74AXC1T45 translators; common OE gates three forward signals and one return.

Function: Convert active-HIGH SEL1..8 to active-HIGH switch disable.
Exactly one powered switch connects; all other COM pins are OFF.

Source / changes: Codex onehot star; TI SN74LVC540A SCAS297O RevO Jun2026 p3 and Sec7.4.
https://www.ti.com/lit/gpn/sn74lvc540a
Both OE pins grounded. C710100nF; existing SEL pulldowns10k retained.
Per-port EN pullup10k ensures default isolation.
SW600/common and XEM branch are retained in the parent schematic.
SW600 positions1=XEM,2..9=HS1..8;10..12=OFF.
SW700 OFF drives the common LOW, disabling USB paths.
Shared and XEM translator outputs must never enable together.
Eight switches plus one inverter replace eight repeated interface chains;
shared U611/U621/U631 service all headstages.

Candidate: unpowered targets, USB enumeration and wiring not qualified

Sheet: /USB JTAG and selection/
File: USB_JTAG.kicad_sch

Title: USB JTAG programmer and target selector — V1

Size: User
Date:
Rev: V1
KiCad E.D.A. 10.0.6
Id: 4/4