」EE2401 微算機系統 Fall 2019

HW#7 (ARM) (11/30/2019)

Due date: 12/12/2019. Severe penalty will be given to late homework.

Note:

(a) The homework will be graded based on your **answer**. Please read class handouts (ARM-1, ARM-2, ARM-3, and ARM-4)

(b) You are required to **type** your homework (first the problem then your solution) by using a **word processor** and submit in .docx (or .pdf) format under a filename **EE2401f19-hw7-student_no-vn.docx(or .pdf)**, where **student_no** is your student number, e.g., **107061xxx** and **vn** is your version number, e.g., **v3**. You should upload your .doc file in **iLMS** by the specified deadline whenever you have a newer version. Follow the iLMS upload homework process to upload your file.

(c) The homework will be graded based on your **latest version**. Old version(s) will be discarded.

(d) Each homework assignment will have full score of 100 points. 5 points will be deducted if you do not comply with the naming convention. Severe grade penalty will be given to late homework. 20 points will be taken off per day after deadline till zero point. ***Copying is violating the regulations and is definitely not allowed!***

(e) Please treat the above requirements as a kind of training in writing a decent homework report. If you have any problem regarding this homework, **please feel free to consult with TA or teacher**. If you think the time is too short to accomplish this homework, please let me know in class.

A. Quizzes (40%)

1. Which statement(s) is(are) **incorrect**?

(a) The computer architecture describes the user invisible implementation of the computer while the computer organization describes the user's view of the computer;

(b) The state of the computer system is defined by the sizes of the memory and the values in the registers;

(c) A processor can be divided into two basic components: datapath and control. The ALU and PC are part of the datapath;

(d) When designing a *new processor* all the issues regarding ISA must be resolved, such as instruction set, data types, storage organizations, addressing modes, and ALU.

ANS: ABD

A is incorrect

Computer architecture describes the user's view of the computer. The instruction set, visible registers, memory management table structures and exception handling model are all part of the architecture, and computer organization describes the user-invisible implementation of the architecture. The pipeline structure,

transparent cache, table-walking hardware and translation look-aside buffer are all aspects of the organization

B is incorrect

The state of the system is defined by the values held in the memory locations together with the values held in certain registers within the processor itself.

D is incorrect

ALU is not included in the ISA

2. From the simple MU0 design example, to make CPU faster, one can:
(a) increase the CPI of each instruction;
(b) increase the number of registers;
(c) increase the capacity of external memory;
(d) reduce the clock frequency.

ANS: B

A is incorrect

Reduce CPI

C is incorrect

Does not affect the performance

D is incorrect

Increase the clock frequency

3. Regarding RISC and CISC CPU, which statement(s) is(are) **incorrect**?
(a) CISC instruction decoding can be hard-wired;
(b) Both CISC and RISC are equally suitable for pipelining;
(c) CISC usually can have a more compact code than RISC for the same tasks;
(d) CISC emphasizes compiler complexity. RISC emphasizes hardware complexity.

ANS: ABD

A is incorrect

RISC instruction decoding can be hard-wired.

B is incorrect

Only CISC is suitable

D is incorrect

RISC emphasizes compiler complexity and CISC emphasizes hardware complexity.

4. In a certain RISC processor's 3-operand instruction set, there are 63 instructions, and 64 registers in the register file. What will be the minimum length (in bits) of encoded instruction?
(a) 16;
(b) 20;
(c) 24;
(d) 32.

ANS:C

6*4 = 24

5. Which of the following is(are) **not included** in ISA (Instruction Set Architecture)?
(a) RTL design of datapath
(b) the design of ALU
(c) memory organization and addressing modes
(d) the instruction set

ANS: AB

6. Which statement(s) is(are) **correct** regarding of CPU power consumption and power saving?
(a) Major power consumption of a CMOS CPU comes from switching.
(b) Decreasing power supply voltage reduces power consumption
(c) Clock gating, signal gating and power gating are commonly adopted techniques for saving power
(d) Increasing parallelism of the CPU circuit will increase gate counts, thus is not a good tactic for low power design

ANS: ABC

D is incorrect

Duplicating a circuit allows the two circuits to sustain the same performance at half the clock frequency of the original circuit, which allows the required performance to be delivered with a lower supply voltage.

7. The address system supported by ARM systems is/are:
(a) Little Endian;
(b) Big Endian;
(c) X-little Endian;
(d) both (a) and (b).

ANS: D

8. Which of the following RISC features is(are) **included** in the original ARM CPU?
(a) A large uniform register file with full independent register bank (i.e., r0~r14) for each CPU mode
(b) A delayed branch mechanism for ameliorate the pipeline stall problem
(c) A Harvard architecture to facilitate single cycle execution of instructions
(d) A inline barrel shifter to improve core performance and code density

ANS: D

9. Which of the following statements is(are) **correct**?
(a) The contemporary ARM architecture profiles include three profiles, i.e., Cortex-A, Cortex-R, and Cortex-M
(b) In an ARM embedded system hardware, the APB bus is used to connect the ARM processor and other controllers such as counter/timer, UARTs, …, etc.
(c) Four typical software components are required to control an ARM embedded device. The initialization code is the first code executed on the board and is specific to a particular target or group of targets.
(d) ARM adopts I/O mapped I/O technique for peripherals

The ARM handles I/O peripherals (such as disk controllers, network interfaces, and so on) as memory-mapped devices with interrupt support.

ANS: ABC

10. ARM is a RISC processor that doesn't take the RISC concept too far. What non-RISC features does the ARM support?
(a) Arithmetic instructions;
(b) Logical instructions;
(c) Branch instructions;
(d) Load-store-multiple instructions.

ANS: D

D is inherited from the Berkeley RISC

11. FIQs are faster to handle than IRQs because:
(a) The processor always uses the barrel shifter in FIQ mode;
(b) Memory accesses are not permitted in FIQ mode;
(c) FIQ mode has more banked registers;
(d) The FIQ interrupt handler is conveniently stored at 0x0.

ANS: C

The ARM fast interrupt (FIQ) architecture includes more banked registers than the other exception modes in order to minimize the register save and restore overhead associated with handling one of these interrupts.

12. Which of the following statements is(are) **correct**?
(a) Each privileged mode of ARM is equipped with its own saved program status register SPSR and SP, LR
(b) The I, F bits in CPSR of ARM are used as flag to indicate the occurrence of an IRQ or FIQ status.
(c) To switch to other modes from user mode, ARM provides MRS instruction for that purpose
(d) **Exceptions** are generated by **internal** and **external sources** to cause the processor to handle an event, such as an externally generated interrupt or an attempt to execute an undefined instruction.

ANS: B, D

A is incorrect

A does not have a SPSR

C is incorrect

Under user mode, CPSR is not allowed to modify.

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ANS: B, D

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A does not have a SPSR
C is incorrect
Under user mode, CPSR is not allowed to modify.

15. Which of the following instructions modifies **both** the lr and the pc?
(a) MOVS pc, lr;
(b) BL <label>;
(c) LDR pc, [pc, #offset];
(d) SWI 0x123456.

ANS: B,D

When a subroutine call is performed by a BL or BLX instruction, the link register is set to the subroutine return address.

16. Which of the following instructions will change the contents of the cpsr, given that cpsr = nzcvqift USER to start with?
(a) MOVS r1, #0x08;
(b) ADD r1, r1, LSL #2;
(c) BX r3 ;where the value of r3 is 0x100F
(d) LDMIA r0!, {r1-r3}.

ANS: C

Condition code flags may be change

17. If r6=0x8000, what address is held in r6 after executing the following instruction?
LDMIA r6!,{r0,r1,r2,r3,r4,r5}
(a) 0x8000;
(b) 0x8010;
(c) 0x8014;
(d) 0x8018;

ANS: D

R6 will be incremented by 18H times

18. In a ARM processor, which exception vector is located at the highest memory address of the exception vector table?
a) Undefined Instruction
b) Data Abort
c) IRQ
d) FIQ

ANS: D

FIQ is stored in 0x0000001C

19. What are the values of the I and F bits in the Program Status Register on reset?
(a) I=0, F=0
(b) I=1, F=0
(c) I=0, F=1
(d) I=1, F=1

ANS: D

20. Register R1 has the value 0x80008001, which statement(s) is(are) **incorrect** regarding the value of R1 after the following operations are performed independently?
(a) MOV R1, R1, LSR #3 → R1 = 0x10001000
(b) MOV R1, R1, LSL #4 → R1 = 0x00080010
(c) MOV R1, R1, ASR #1 → R1 = 0xC0004000
(d) MOV R1, R1, ASL #3 → R1 = 0x00040008

All of them are correct

B. (8%) The addressing modes commonly seen in ARM and other microprocessors could contain the followings. Please fill in the following five blanks to explain how to get the operand in memory (denoted by mem) or register (denoted by reg) via the effective address EA.

Addressing mode	**Effective address EA**
Immediate addressing:	#value
Absolute addressing:	EA = mem
____1_____ addressing:	EA = (mem)

Register addressing:	EA = reg
Register indirect addressing:	EA = ____2___
Base plus offset addressing:	EA = base + offset_value
Base plus index addressing:	EA = _____3_____
_____4____addressing:	EA = base+val*reg
Stack addressing:	EA = sp

1. **Indirect addressing**
2. **(reg)**
3. **base + reg**
4. **Base plus scaled index**

C. (12%) ARM is a RISC type processor and accesses memory through load (LDR, LDM) and store (STR, STM) instructions. Assume that before executing the LDR instruction, the initial values are

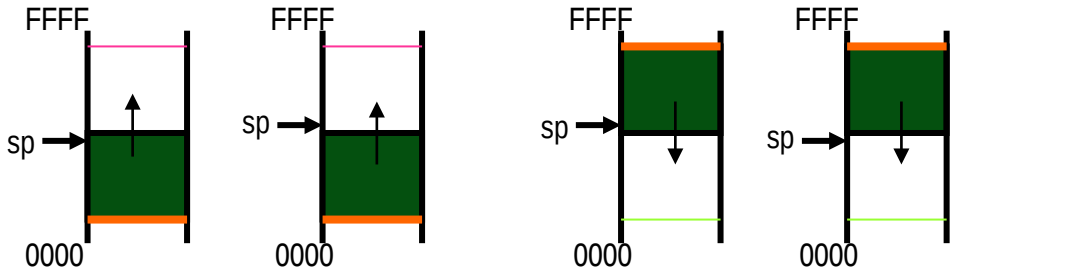
r0 = 0x00000000,
r1 = 0x00009000,
mem32[0x00009000] = 0x01010101 (i.e., the memory contents at 0x00009000 is 0x01010101), and
mem32[0x00009004] = 0x02020202

What are **the contents of r0 and r1 after** executing the LDR instruction for the following three cases?

(1) LDR r0,[r1,#4]!
(2) LDR r0,[r1,#4]
(3) LDR r0,[r1],#4

1. **r0 = 0x02020202, r1 = 0x00009004**
2. **r0 = 0x02020202, r1 = 0x00009000**
3. **r0 = 0x01010101, r1 = 0x00009004**

D. (24%) The following figure shows four types of stack from (A) ~ (D). Please write down their names and the corresponding LDM, STM instructions for popping and pushing data items for each type of stack.



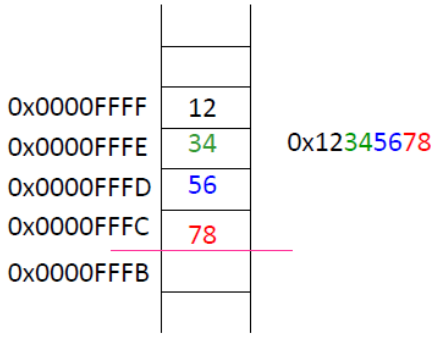
(A) _____ (B) _____ (C) _____ (D) _____

(A) Full ascending stack, STMFA/LDMFA
(B) Empty ascending stack STMEA/LDMEA
(C) Full descending stack STMFD/LDMFD
(D) Empty descending stack STMED/LDMED

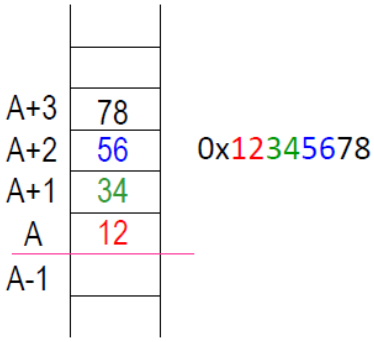
E. (8%)A word: 0x12345678 is to be stored at memory location with address A where A = 0x0000FFFC and "0x12" is the MSB (byte) of the word. Please draw two

figures clearly indicating the address and the contents of the memory for storing the word 0x12345678 with little endian and big endian convention, respectively.

Little Endian:



A=0x0000FFC
Big Endian:



F. (8%) When exception occurs, some operations are performed as below. Please fill in the following 4 blanks.

(1) R14_<exception_mode> = _____1_____
(2) SPSR_<exception_mode> = ___2___
(3) CPSR[4:0] = exception mode number
(4) CPSR[5] = 0 /* Execute in ARM state */
(5) if <exception_mode> == Reset or FIQ then CPSR[6] = 1 /* Disable___3___ interrupts else CPSR[6] is unchanged */
(6) CPSR[7] = 1 /* Disable normal interrupts */
(7) PC = _____4_____

1. **Return link**
2. **CPSR**
3. **Fast**
4. **Exception vector address**