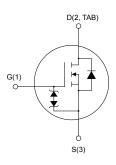


N-channel 650 V, 132 m Ω typ., 20 A MDmesh M9 Power MOSFET in a DPAK package

Features





Order code	V _{DS}	R _{DS(on)} max.	I _D	
STD65N160M9	650 V	160 mΩ	20 A	
Worldwide heat FOM D *Og emeng cilican besed devices				

- Worldwide best FOM R_{DS(on)}*Qg among silicon-based devices
- Higher V_{DSS} rating
- · Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- · Zener-protected

Applications

· High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.





Product status link STD65N160M9

Product summary			
Order code	STD65N160M9		
Marking	65N160M9		
Package	DPAK		
Packing	Tape and reel		



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V_{GS}	Gate-source voltage	±30	V	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C			
ID(·)	Drain current (continuous) at T _C = 100 °C	12.5	_ A	
I _{DM} ⁽²⁾	Drain current (pulsed)	60	Α	
P _{TOT}	Total power dissipation at T _C = 25 °C	106	W	
dv/dt ⁽³⁾	Peak diode recovery voltage slope	50	V/ns	
di/dt ⁽³⁾	Peak diode recovery current slope	900	A/µs	
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	120	V/ns	
T _{stg}	Storage temperature range	55 to 150	°C	
TJ	Operating junction temperature range	-55 to 150	°C	

- 1. Referred to TO-220 package.
- 2. Pulse width is limited by safe operating area.
- 3. $I_{SD} \le 10 \text{ A}$, V_{DS} (peak) $< V_{(BR)DSS}$, $V_{DD} \le 400 \text{ V}$.
- 4. V_{DS} (peak) $< V_{(BR)DSS}$, $V_{DD} \le 400 \text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	1.18	°C/W
R _{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max)	4	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	200	mJ

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2 Electrical characteristics

 T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
lass	Zoro goto voltogo droin ourrent	V _{GS} = 0 V, V _{DS} = 650 V			1	
I _{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V, T_{C} = 125 °C ⁽¹⁾			200	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±5	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	3.2	3.7	4.2	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 10 A		132	160	mΩ

^{1.} Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 400 V, f = 1 MHz, V _{GS} = 0 V	-	1240	-	pF
C _{oss}	Output capacitance	V _{DS} = 400 V, 1 = 1 MH12, V _{GS} = 0 V	-	25	-	pF
Coss eq. (1)	Equivalent output capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0 V	-	290	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	2	-	Ω
Qg	Total gate charge	V _{DD} = 400 V, I _D = 10 A, V _{GS} = 0 to 10 V	-	32	-	nC
Q _{gs}	Gate-source charge	(see Figure 15. Test circuit for gate	-	7	-	nC
Q _{gd}	Gate-drain charge	charge behavior)	-	15	-	nC

^{1.} $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(v)}	Voltage delay time	V _{DD} = 400 V, I _D = 10 A,	-	8	-	ns
t _{r(v)}	Voltage rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	5	_	ns
t _{f(i)}	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times	-	7	-	ns
t _{c(off)}	Crossing time off	and Figure 17. Turn-off switching time waveform on inductive load)		40	-	ns
t _{d(i)}	Current delay time	$V_{DD} = 400 \text{ V}, I_D = 10 \text{ A},$	-	14	-	ns
t _{r(i)}	Current rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	4	-	ns
t _{f(v)}	Voltage fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times	-	10	-	ns
t _{c(on)}	Crossing time on	and Figure 18. Turn-on switching time waveform on inductive load)	-	12	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾	Source-drain current		-		20	Α
I _{SDM} ⁽²⁾	Source-drain current (pulsed)		-		60	Α
V _{SD} ⁽³⁾	Forward on voltage	I _{SD} = 20 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 20 A, di/dt = 100 A/μs,	-	192		ns
Qrr	Reverse recovery charge	V _{DD} = 100 V	-	1.8		μC
I _{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	17.5		Α
t _{rr}	Reverse recovery time	$I_{SD} = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	280		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 100 V, T _J = 150 °C	-	3.6		μC
I _{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	20.5		Α

- 1. Referred to TO-220 package.
- 2. Pulse width is limited by safe operating area.
- 3. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

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2.1 Electrical characteristics (curves)

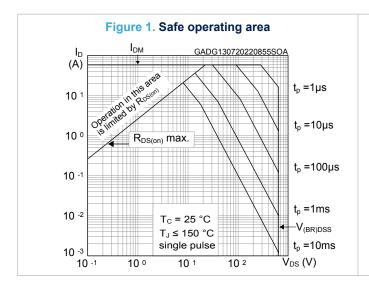
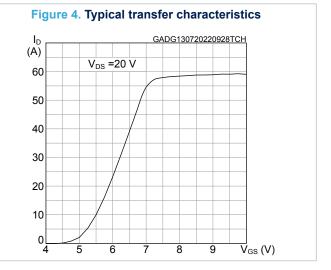
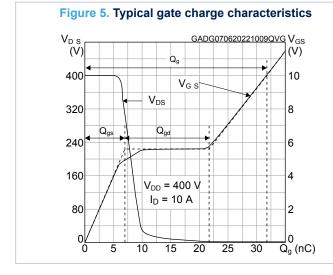
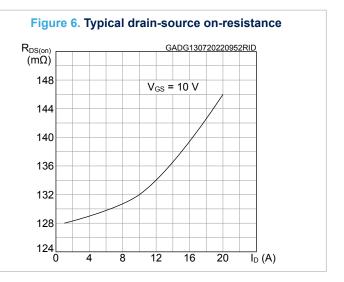


Figure 3. Typical output characteristics Ι_D (A) GADG130720220928OCH 60 V_{GS} =8, 9, 10V 50 V_{GS} =7V 40 30 V_{GS} =6V 20 10 V_{GS} =5V 16 12 8 $\overline{V}_{DS}(V)$







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Figure 7. Typical capacitance characteristics

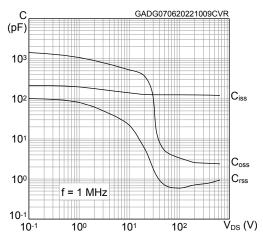


Figure 8. Typical output capacitance stored energy

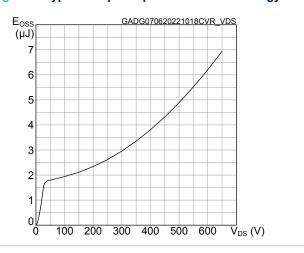


Figure 9. Normalized gate threshold vs temperature

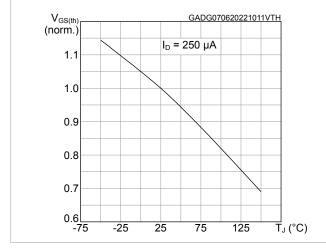


Figure 10. Normalized on-resistance vs temperature

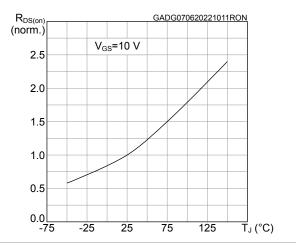


Figure 11. Normalized breakdown voltage vs temperature

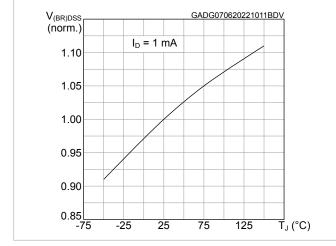
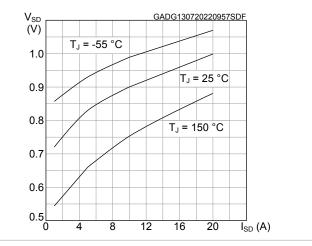


Figure 12. Typical reverse diode forward characteristics



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3 Test circuits

Figure 13. Unclamped inductive load test circuit

Figure 14. Unclamped inductive waveform

V_{(BR)DSS}

V_{DD}

V_{DD}

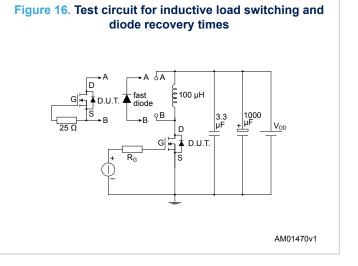
AM01472v1

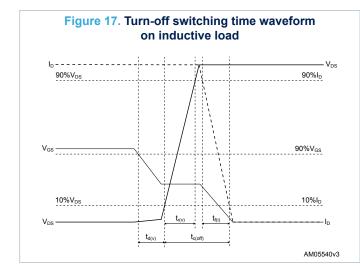
Figure 15. Test circuit for gate charge behavior

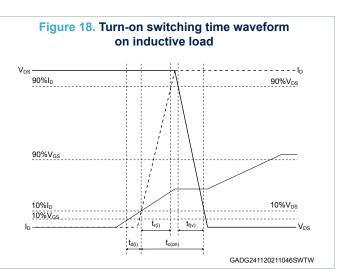
Vosting 100 \(\Omega \)

Vosting 100 \(\Omega \)

AM01469v10







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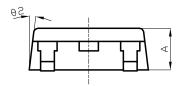


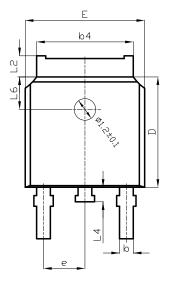
4 Package information

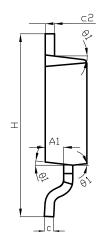
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

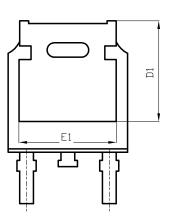
4.1 DPAK (TO-252) type C2 package information

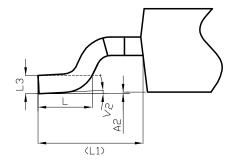
Figure 19. DPAK (TO-252) type C2 package outline











0068772_type-C2_rev31

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Table 8. DPAK (TO-252) type C2 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
С	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10	5.35	5.60
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
е	2.186	2.286	2.386
Н	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60 0.80		1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

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Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)

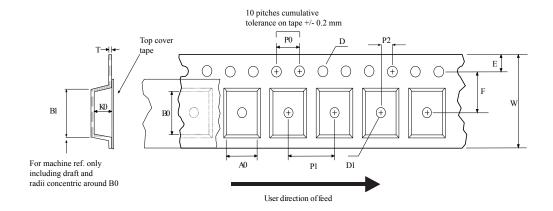
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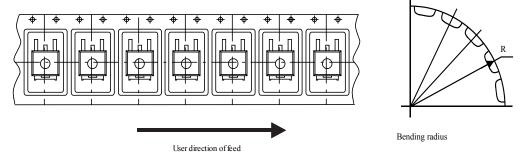
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4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



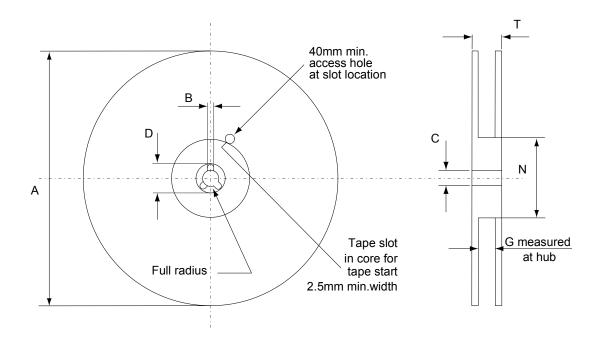


AM08852v1

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Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

	Таре			Reel		
Dim	mm		D:	mm		
Dim.	Min.	Max.	Dim.	Min.	Max.	
A0	6.8	7	А		330	
В0	10.4	10.6	В	1.5		
B1		12.1	С	12.8	13.2	
D	1.5	1.6	D	20.2		
D1	1.5		G	16.4	18.4	
E	1.65	1.85	N	50		
F	7.4	7.6	Т		22.4	
K0	2.55	2.75				
P0	3.9	4.1	Base	e qty.	2500	
P1	7.9	8.1	Bulk	c qty.	2500	
P2	1.9	2.1				
R	40					
Т	0.25	0.35				
W	15.7	16.3				

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Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Jul-2022	1	First release.
		Updated title in cover page.
	2	Updated Features in cover page.
01-Dec-2022		Updated Table 1. Absolute maximum ratings.
01-Dec-2022		Updated Table 5. Dynamic.
		Updated Table 7. Source-drain diode.
		Updated Figure 3. Typical output characteristics.

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