Comments on Exercise 1 in TIHSC - Xilinx

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1 Introduction

This document describes all problems encountered in the execution of the TIHSC1_Exercise1_Xilinx.pdf exercise. The document is devided into chapters and sections according to the exercise descriptions.

The source code for the full solution can be found on GitHUb: `https://github.com/HrNilsson/Xilinx`.

Note, that the first part of the exercise is not present here. Only the finished Lab1, Lab3/4, and the Multyplier project is present.

The folder structure is as shown in Figure 1.1. The folders Lab1, Lab3, project_multiply includes all Vivado files. The corresponding folders ending with _SDK includes the corresponding SDK projects.

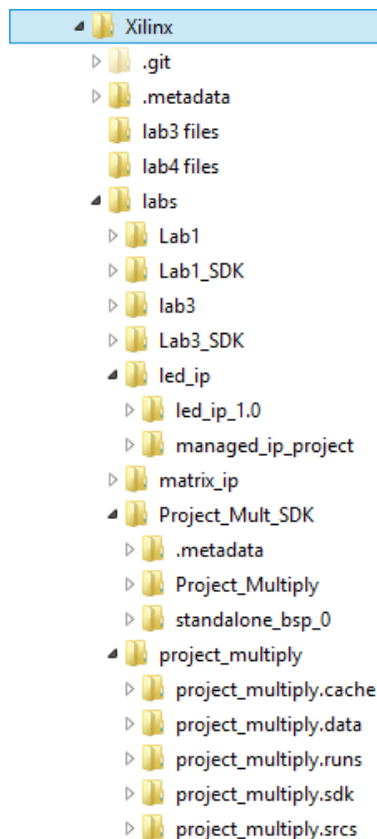The folders led_ip and matrix_ip includes the custom IP packages.

Figure 1.1: Directory structure

2 Installation

I am running Windows 8, 64 bit, and using Xilinx software version 2013.4, which is the newest at the moment. The following experiments are defined in: Setting Up a Development Platform for Zynq 2013_3_02.pdf

2.1 Experiment 1

- Install 7-zip - No comments.

2.2 Experiment 2

- Register account on Xilinx.com

- Download Vivado design suite - appr. 7 Gb

- Check it with FastSum, to make sure the MD5 checksum is correct.

- Insall Vivado system edition + sdk. Note, the license installion fails, because Windows 8 is not supported. This does not matter.

2.3 Experiment 3

2.3.1 Install license

Xilinx license manager does not work in 64 bit mode. Use 32 bit instead!
    It is located C:/Xilinx/Vivado/2013.4/ids_lite/ISE/bin/nt/xlcm.exe

2.3.2 Running the Vivado suite

Vivado GUI is not supported in windows 8! Instead, run the Vivado in Windows 7 compatible mode:

- Open C:/Xilinx/Vivado/2013.4/bin/vivado.bat and insert:

- set __COMPAT_LAYER=WIN7RTM, so the last 3 lines are:

```
set  RDI_PATASK=yes
set  _COMPAT_LAYER=WIN7RTM
call  "%RDI_BINROOT%/loader.bat"  −exec %RDI_PROG% %∗
```

Aparrently, this is not enough. Java throws an exception.
Instead create a new shortcut to the 32 bit program:

- Open the folder:
  C:/Xilinx/Vivado/2013.4/bin/unwrapped/win32.o

- Create a shortcut for vivado.exe.

- Open the properties for the shortcut.

- Change the following:
  Target: = "C:/Xilinx/Vivado/2013.4/bin/unwrapped/win32.o/vvgl.exe C:/Xilinx/Vivado/2013.4/./bin/vivado.bat"
  Start in: = "%APPDATA%/Xilinx/Vivado"

2.4 Experiment 4

Install USB-UART serial driver

2.5 Experiment 5

Install Tera Term

2.6 Experiment 7

Configure Tera Term - Note, the virtual com port lost connection: solution = restart PC.

2.7 Experiment 8

Windows firewall

2.8 Summary

Full installation took a couple of hours!
This would not be the case on a windows 7 machine.

3 Vivado

The following steps are defined in: lab1(2)_EmbeddedSystem.

3.1   Hardware Generation

Step 2-6-4:
The GPIO_0 has disappered. - run step 2-2 and 2-3 again.
If it complains about wrong license, with no bitstream generation, just add the right license, WITH bitstream generation.

Step 3-1-1:
lab1.xdc, added in step 2.8 does not work correctly.
It seems it is case-sensitive. Correct the lines to:

```
set_property PACKAGE_PIN R18 [get_ports btnr_tri_io]
set_property IOSTANDARD LVCMOS25 [get_ports btnr_tri_io]
```

4 Xilinx SDK

4.1 Software Platform

Step 5.1:
Building the software platform throws an include error.
Reason:

- There must be NO parentheses or spaces in project path.

- The PATH environment variable should be set up properly, by running setting32. This did not work. Instead write the following in the top of the makefile (in one line):
  PATH=C:/Xilinx/SDK/2013.4/bin/nt;
  C:/Xilinx/SDK/2013.4/bin;
  C:/Xilinx/SDK/2013.4/gnu/microblaze/nt/bin;
  C:/Xilinx/SDK/2013.4/gnu/powerpc-eabi/nt/bin;
  C:/Xilinx/SDK/2013.4/gnuwin/bin;
  C:/Xilinx/SDK/2013.4/gnu/arm/nt/bin;
  C:/Xilinx/SDK/2013.4/gnu/microblaze/linux_toolchain/nt_be/bin;
  C:/Xilinx/SDK/2013.4/gnu/microblaze/linux_toolchain/nt_le/bin;%PATH%

4.2 C application

Step 5.2:
Building the C application:
Building error:
"make: Interrupt/Exception caught (code = 0xc00000fd, addr = 0x4227d3)"

This error is caused because of my PATH environment settings. It turns out that the ARM gcc compiler uses a file called sh.exe, which is also used/part of the program Github. A possible solution is to remove Github from your PATH environment. Or renaming the sh.exe file in github (Then Github might not work!!):
C:/Program Files (x86)/Git/bin/sh.exe
You might need to restart your PC after changing your PATH variable.

5 Configure Peripherals

The following exercises and steps are defined in: lab3_ZynqHW.pdf.

5.1 Clocks

Experiment 2, Step 8: Do not turn of FCLK_CLK0! It is already in use by the ZYng processor!

6 Create Custom IP

The following steps are defined in: lab3_EmbeddedSystem.pdf.

6.1 Block design

Step 4-1-7:
Note, the diagrams are not alike, since I did not make Lab2, which is used in the toturial. There is no BTNR and no leds_8bits, instead there is btns_5bits in lab3. In my design, there is both leds_8bits and LED[7:0]! The leds_8bits and BTNR should be removed, and the btns_5bits should be added!! Otherwise the following lab exercises cannot be completed!
This is done by:

- Double clicking leds_8bits and change the board interface to btns_5bits. Additional the block and external connection should be renamed.

- Open the ZYNQ, under MIO Configurations, remove EMIO GPIO.

- Delete the BTNR connection from the block design.

- Remove the lab1 constraint (and the System_wrapper constraint), since we deleted BTNR.

7 Writing basic software application

The following steps are defined in: lab4_EmbeddedSystem.pdf.
Note I did not rename my Vivado project, since there is no need to do that!

Step 2-2: The hw_platform and bsp will not rebuild automaticly, since the Vivado project has been renamed to lab3, instead of lab1. Therefore the new hw_platform must be imported, and the bsp created.

Step 2-2-15: Note that the LEDs will not light up yet!

Step 2-4-5: In my case, the correct name is:

LED_IP_mWriteReg(XPAR_LED_IP_S_AXI_BASEADDR, 0, dip_check);

Step 4-2-2: I do not get any error, because the text area already is in the DDR, and not the BRAM.

8 Console application

The following steps are defined in: TIHSC1_Exercise1_Xilinx.pdf part 3.
In the source code given, the defined value for one second should be changed to:

$\#define\ ONE\_SECOND\ 1333000$

9 Hardware IP Acceleration

9.1 Creating matrix_ip

Step 1-2-27 in lab3_EmbeddedSystem: There is no guide help, thus no "Merge changes....." - I try without...

Note, that the drivers for matrix_ip will be located in labs/matrix_ip/matrix_ip_1.0/drivers/matrix_ip_v1_00_a/src. For some reason it is not part of the exported hardware platform.