Assignment 2

Name : Hriday Jain

Batch : S13

Roll no : 56

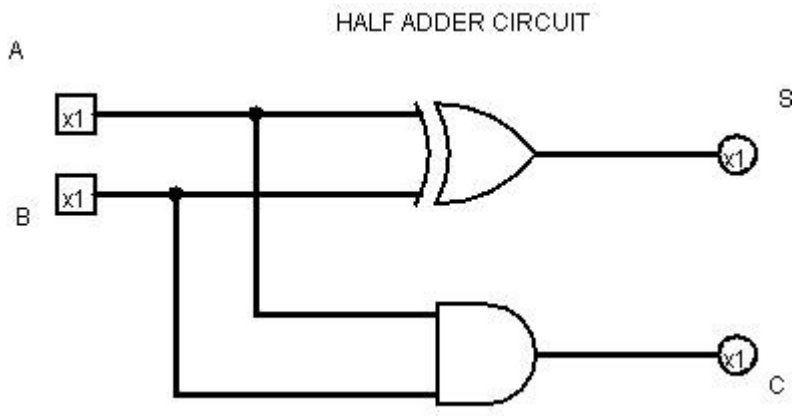
Subject : MPL

Software : Logisim

AIM : To study adder and subtractor circuits.

1. **HALF ADDER CIRCUIT :**

   CIRCUIT DIAGRAM :

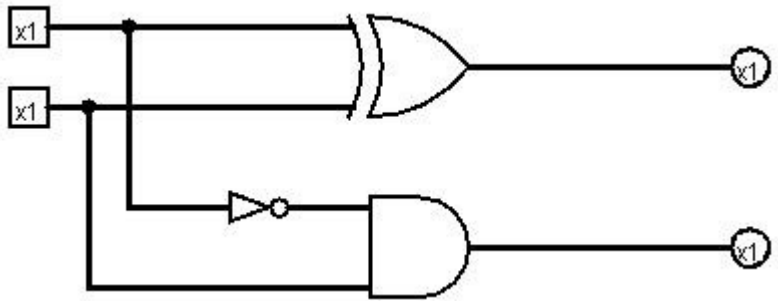


   TRUTH TABLE :

a	b	x	y
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2. **HALF SUBTRACTOR CIRCUIT :**

   CIRCUIT DIAGRAM :

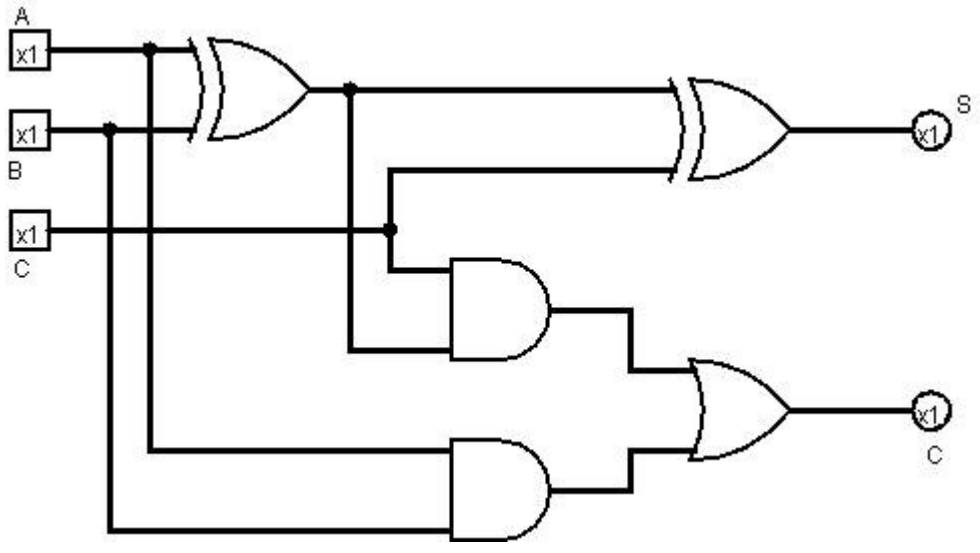


TRUTH TABLE :

a	b	x	y
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

3. FULL ADDER CIRCUIT :

CIRCUIT DIAGRAM :

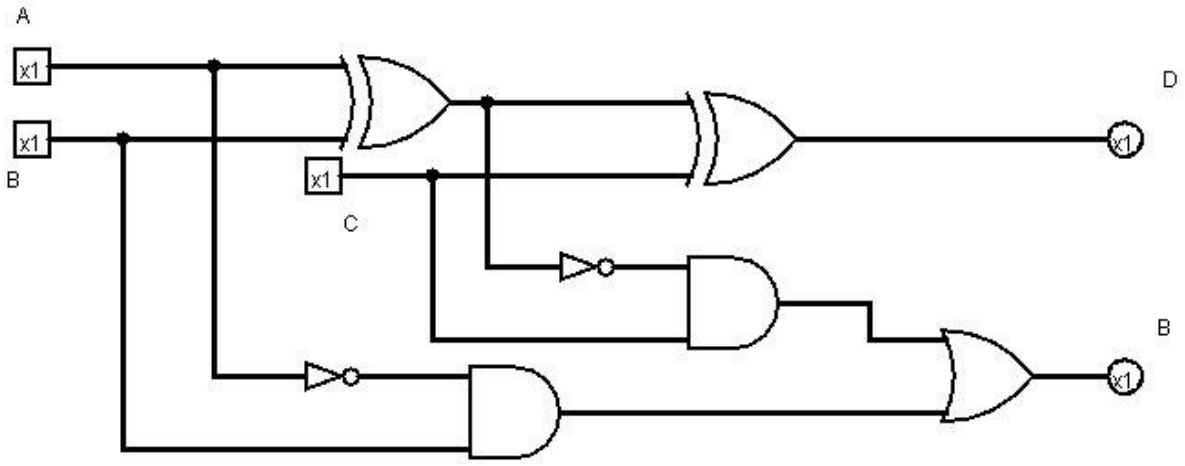


TRUTH TABLE :

a	b	c	x	y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. FULL SUBTRACTOR CIRCUIT :

CIRCUIT DIAGRAM :



TRUTH TABLE :

a	b	c	x	y
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1