Harsh Nangia

Delhi, India
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Education

Indraprastha Institute of Information Technology Delhi, India **CGPA: 8.08**
Bachelor of Technology in Electronics and VLSI Engineering *Nov. 2022 – Present*

Bharatiya Vidya Bhavan's Mehta Vidyalaya Delhi, India **Percentage: 89.60**
All India Senior School Certificate Examination *Apr. 2020 – Jun. 2021*

Bharatiya Vidya Bhavan's Mehta Vidyalaya Delhi, India **Percentage: 90.00**
All India Secondary School Examination *Apr. 2018 – Mar. 2019*

Relevant Coursework

- Embedded Systems
- Operating Systems
- Digital VLSI Design
- VLSI Design Flow
- Algorithms
- Signals & Systems
- NLP
- Machine Learning

Projects

Gendered Abuse Detection In Indic Languages | Github | *Natural Language Processing* **Jan 2025 – Apr 2025**
- Developed a multilingual text classification model to detect gendered abuse in Hindi, English, and Tamil tweets using advanced NLP techniques.
- Fine-tuned the XLM-RoBERTa transformer model and integrated BiLSTM and CNN layers for enhanced contextual and local feature extraction.
- Achieved a **77% macro-averaged F1 score**, significantly outperforming baseline models.

IEEE 802.11a Transceiver on Zedboard | *Xilinx Vivado — HLS — Zynq SoC* **Jan 2025 – Apr 2025**
- Designed and implemented an IEEE 802.11a OFDM transceiver on ZedBoard using Xilinx Vivado and High-Level Synthesis (HLS).
- Reduced running time by **86%** by creating custom hardware IPs and offloading computation to FPGA.
- Optimized software algorithms and evaluated BER and EVM under varying SNR conditions to validate performance.

Matrix Multiplication Custom IP Design | *Xilinx Vivado — HLS — Zynq SoC* **Mar 2025 – Apr 2025**
- Designed and implemented 4 custom IPs for 8x8 matrix multiplication with progressive HLS optimizations: baseline, pipelining, array partitioning, and memory-mapped interface.
- Achieved **4× speedup**, reducing running time from **26.07µs to 6.41µs** using memory-mapped interface.
- Verified functionality and performance of all IPs using Xilinx Vivado and SDK integration.

Timing Analysis and Scan Design Flow | *Digital Design — Static Timing Analysis* **Sep 2024 – Dec 2024**
- Performed **Timing Analysis** by designing and constraining Verilog netlists with SDC files, including clock and I/O constraints, to achieve positive setup slack.
- Conducted **Static Timing Analysis (STA)** to identify **worst-case setup and hold slacks**, and analyzed timing paths under varying clock latencies, uncertainties, and input/output delay constraints.
- Implemented **Scan Insertion** manually in Verilog netlists to understand its effect on timing, developing functional and shift mode SDC files with case analysis for mode-specific constraints.
- Analyzed **worst-case slacks** (late and early paths) pre and post-scan insertion for both **functional and shift modes**, comparing timing trade-offs.

OAI33 Standard Cell Design and Optimizations | *Cadence Virtuoso — Layout Design* **Sep 2024 – Dec 2024**
- Designed complex and non-complex designs using Cadence Virtuoso with LVS and DRC clean layouts.
- Reduced area by over **2.3** times and power by **up to 20%** in complex design compared to non-complex counterpart.
- Validated timings and power across PVT corners.

Technical Skills

Languages: C, C++, Verilog, Python, Java, TCL
Tools: Xilinx Vivado, Vivado HLS, Cadence Virtuoso, Eldo, Git, VS Code, OpenSTA, YOSYS
Technologies/Frameworks: PyTorch, AXI Interface, HLS Pragmas, MATLAB, Linux, GitHub

Achievements

- **Solved 500+ algorithm problems** on various coding platforms: LeetCode | Codeforces | CodeChef.
- Achieved **97.67 percentile** in JEE Main 2022, placing in the **top 2.33%** among nearly 1 million students nationwide.