Experiment : 4
PARALLEL ADDER

Aim: To design and set up the 4 bit binary adder and Subtractor.

Learning objective:

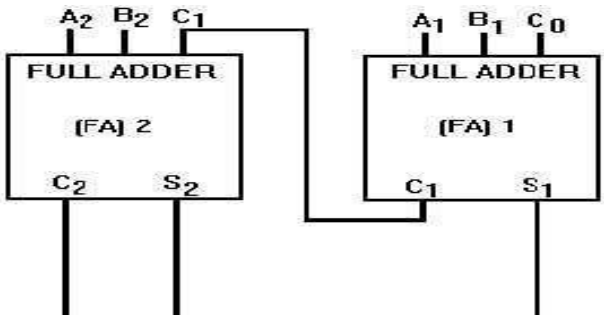
- To learn about IC 7483 and its internal structure.
- To realize a Subtractor using adder IC 7483.

Components required: IC 7483, IC 7486 trainer kit, patch cords.

Theory:

The Full adder can add single-digit binary numbers and carries. The largest sum that can be obtained using a full adder is 11_2. Parallel adders can add multiple-digit numbers. If full adders are placed in parallel, we can add two- or four-digit numbers or any other size desired. Figure below uses standard symbols to show a parallel adder capable of adding two; two-digit binary numbers. The addend would be on A inputs, and the augend on the B inputs. For this explanation

we will assume there is no input to C_0 (carry from a previous circuit)



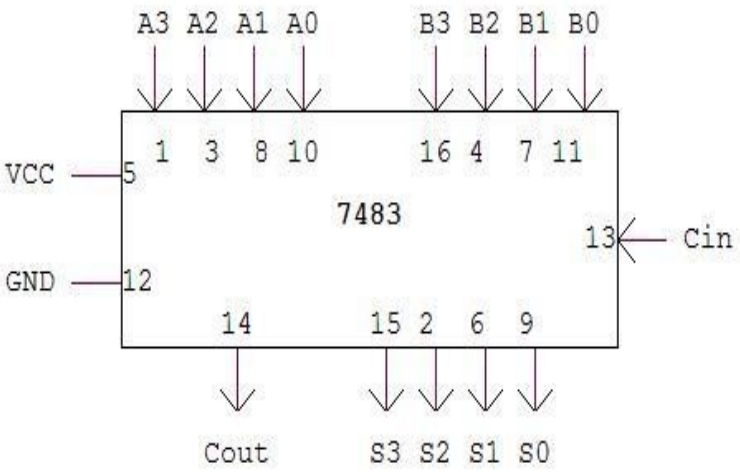
To add 10_2 (addend) and 01_2 (augend), the addend inputs will be 1 on A2 and 0 on A1. The augend inputs will be 0 on B2 and 1 on B1. Working from right to left, as we do in normal addition, let's calculate the outputs of each full adder. With A1 at 0 and B1 at 1, the output of adder1 will be a sum (S_1) of 1 with no carry (C_1). Since A2 is 1 and B2 is 0, we have a sum (S_2) of 1 with no carry (C_2) from adder 1. To determine the sum, read the outputs (C2, S2, and S1) from left to right. In this case, C2 = 0, S2 = 1, and S1 = 1. The sum, then, of 10_2 and 01_2 is 011_2.

Circuit implementation:

4 Bit Binary Adder:

An Example: 7+2=9 (1001)

7 is realized at $A_3\ A_2\ A_1\ A_0 = 0111$
2 is realized at $B_3\ B_2\ B_1\ B_0 = 0010$
Sum = 1001



Truth table:

Inputs A					Inputs B					Sum			
A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0		S3	S2	S1	S0
0	1	1	1		0	0	1	0		1	0	0	1

Procedure:

- Check the components for their working.
- Insert the appropriate IC into the IC base.
- Rig up the circuit as shown in the logic circuit diagram.
- Apply various input data to the logic circuit via the input logic switches.
- Note down the corresponding output and verify the truth table.

Result: Hence parallel adder designed and implemented successfully.