Aim = To verify Full adder using simulation tool CircuitVerse

Component Require = A system , CircuitVerse

Theory = In our system ,we use simulation tool that is CircuitVerse to construct basic circuit of Full Adder .

Full Adder carry bit from its previous stage is called carry-in-bit a combinational logic circuit that adds two data bits , A and B and a carry-in-bit , C_{in} is called a full-adder . The Boolean functions describing the full adder are :-

$$Sum = A \oplus B \oplus C_{in}$$

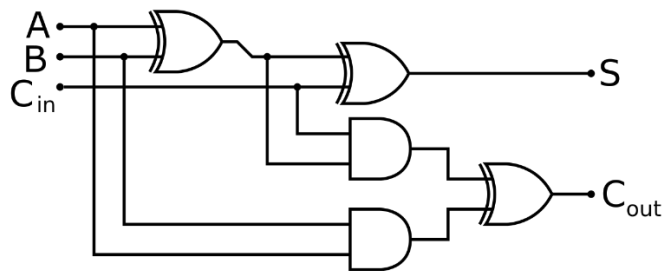$$Carry = A.B + B. C_{in} + A. C_{in}$$

DIAGRAM OF FULL BIT ADDER

Procedure =

1. In Simulation , we construct circuit as shown in diagram .
2. We use XOR gates and AND gates for making this circuit .
3. Make sure in simulation all connection should be connected.
4. Verify the Truth Table and observe the output .

Truth table

Input			Output	
A	B	C_{in}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Result = Hence full adder is verified by simulation .