4.8 FET OPERATION

If a p-n junction is reverse biased, the majority carriers will move away from the junction. That is holes on the p-side will move away from the junction leaving negative charge or negative ions on the p-side (because each atom is deprived of a hole or an electron fills the hole. So it becomes negative by charge). Similarly, electrons on the n-side will move away from the junction leaving positive ions near the junction. Thus, there exists space charge on both sides of the junction in a reverse biased p-n junction diode. So, the electric field intensity, the lines of force originate from the positive charge region to the negative charge region. This is the source of voltage drop across the junction. As the reverse bias across the junction increases, the space charge region also increases, or the region of immobile uncovered charges increases (i.e., negative region on p-side and positive region on n-side increases as shown in Fig. 4.31). The conductivity of this region is usually zero or very small. Now in a FET, between gate and source, a reverse bias is applied. Therefore the channel width is controlled by the reverse bias applied between gate and source. Space charge region exists near the gate region on both sides. The space between them is the channel. If the reverse bias is increased, the channel width decreases. Therefore, for a fixed drain to source voltage the drain current will be a function of the reverse biasing voltage across the junction. Drain is at positive potential (for n-type FET). Therefore, electrons tend to move towards drain from the source (1) Because, source is at negative potential, they tend to move towards the drain. But because of the reverse bias applied to the gate, there is depletion region or negative charge region near the gate which restricts the number of electrons reaching the drain. Therefore the drain current also depends upon the reverse bias voltage across the gate junction. The term field effect is used to describe this device because the mechanism of current control is the effect of the extensions, with increase reverse bias of the field associated with region of uncovered charges.

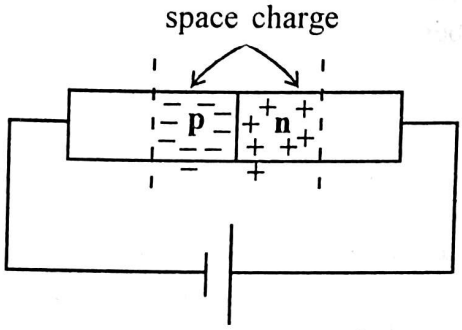

Fig 4.31 Space charge in p-n junction.

The characteristics of n-channel FET between I_D, the drain current and V_{DS} the drain source voltage are as shown in Fig. 4.32, for different values of V_{GS}.

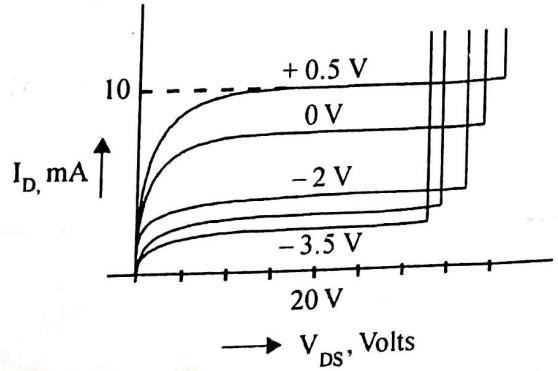

Fig 4.32 Drain charecteristics

To explain these characteristics, suppose $V_{GS} = 0$. When $V_{DS} = 0$, $I_D = 0$, because the channel is entirely open. When a small V_{DS} is applied (source is forward biased or negative

voltage is applied to n-type source), the n-type bar acts as a simple semiconductor resistor and so I_D increases linearly with V_{DS}. With increasing current, the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting portion of the channel begins to constrict. Because, the source gets reverse biased or the negative potential at the n-type source reduces. Because of the ohmic drop, along the length of the channel it self, the constrictions is not uniform, but is more ***pronounced*** at distances farther from the source. i.e., the channel width is narrow at the ***drain*** and wide at the source. Finally, the current will remain constant at a particular value and the corresponding voltage at which the current begins to level off is called as the ***pinch off voltage***. But the channel cannot be closedown completely and there by reducing the value of I_D to zero, because the required reverse bias will not be there.

Now if a gate voltage V_{GS} is applied in a direction to reverse bias the gate source junction, pinch off will occur for smaller values of (V_{DS}), and the maximum drain current will be smaller compared to when $V_{GS} = 0$. If V_{GS} is made + 0.5V, the gate source junction is forward biased. But at this voltage, the gate current will be very small because for Si FET, 0.5V is just equal to or less than the cut in voltage. Therefore, the characteristic for $V_{GS} = +0.5V$, I_D value will be comparatively larger, (compared to $V_{GS} = 0V$ or $-0.5V$). Pinch off will occur early.

FET characteristics are similar to that of a pentode, in vacuum tubes.

The maximum voltage that can be applied between any two terminals of the FET is the lowest voltage that will cause avalanche breakdown, across the gate junction. From the FET characteristics it can be observed that, as the reverse bias voltage for the gate source junction is increased, avalanche breakdown occurs early or for a lower value of V_{DS}. This is because, the reverse bias gate source voltage adds to the drain voltage because drain though n -type (for n-channel FET), a positive voltage is applied to it. Therefore, the effective voltage across the gate junction is increased.

For n-channel FET, the gate is p-type, source and drain are n-type. The source should be forward-biased, so negative voltage is applied. Positive voltage is applied to the drain. ***Gate source junction should be reverse biased,*** and gate is p-type. Therefore,voltage or negative voltage is applied to the gate. Therefore, n-channel FET is exactly similar to a Vacuum Tube (Triode). Drain is similar to anode (at positive potential), source to cathode and gate to grid, (But the characteristics are similar to pentode).

For p-channel FET, gate is n-type, and positive voltage is applied, drain is at negative potential with respect to source.

Consider n-channel FET. The source and drain are n-type and p-type gate is diffused from both sides of the bar (See Fig. 4.33 below).

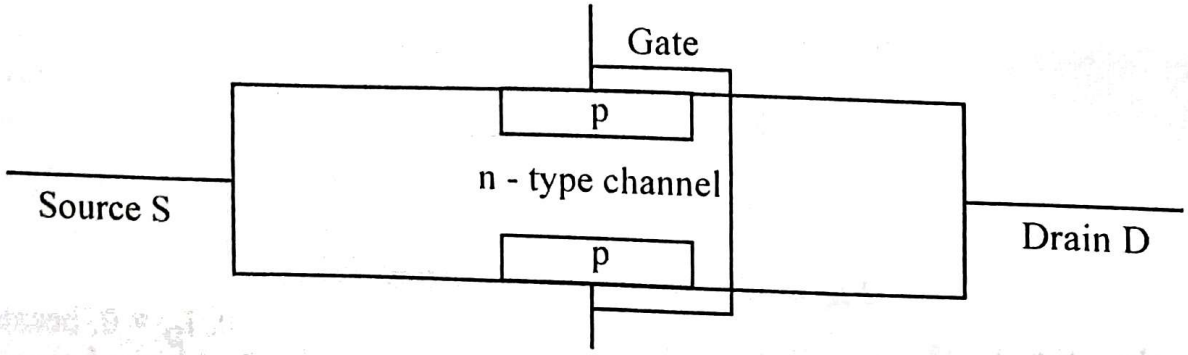

Fig 4.33 Structure of n-channel J FET.

Suppose source and gate are at ground potential and small positive voltage is applied to the drain. Source is n-type. So it is Forward biased. Because drain is at positive potential, electrons from the source will move towards the drain. Negligible current flows between source and gate or gate and drain, since these p-n junctions are reverse biased and so the current is due to minority carriers only. Because gate is heavily doped, the current between S and G or G and D can be neglected. The current flowing from source to drain I_D depends on the potential between source and drain, V_{DS}, resistance of the n-material in the channel between drain to source. This resistance is a function of the doping of the n-material and the channel width; length and thickness.

If V_{DS} is increased, the reverse bias voltage for the gate drain junction is increased, since, drain is n-type and positive voltage at drain is increased. This problem is similar to that of a reverse biased p-n junction diode.

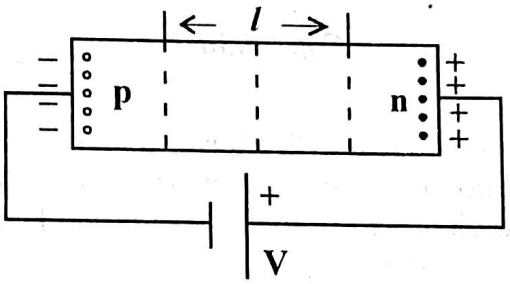

Fig 4.34 Reverse biased G - D junctions

Consider a p-n junction which is reverse biased. The holes on the p-side remain near the negative terminal and electrons on the n-side reach near the positive terminal as shown in Fig.4.34. There are no mobile charges near the junction. So we call this as the depletion region since it is depleted of mobile carriers or charges. As the reverse voltage is increased, the depletion region width '*l*' increases.

This result is directly applicable for JFET. The depletion region extends more towards drain because points close to the drain are at higher positive voltage compared to points close to source. So the depletion region is not uniform $V_{DS} < V_{PO}$. But extends more towards drain than source. V_{P0} is the pinch off voltage.

As V_{DS} is increased, depletion region is increased (shaded portion). So channel width decreases and channel resistance increases. Therefore, the rate at which I_D increases reduces, eventhough there is positive potential for the electrons at the drain and hence they tend to move towards the drain and conventional current flows as shown by the arrow mark, in the Fig.4.35.

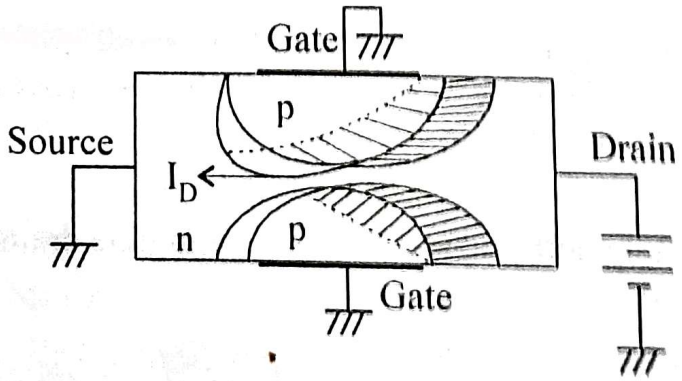

Fig 4.35

When $V_{DS} = V_{PO}$

When V_{DS} is further increased, the depletion region on each side of the channel join together as shown in Fig.4.36. ***The corresponding V_{DS} is called as V_{PD}, the pinch off voltage,*** because it pinches off the channel connection between drain and source.

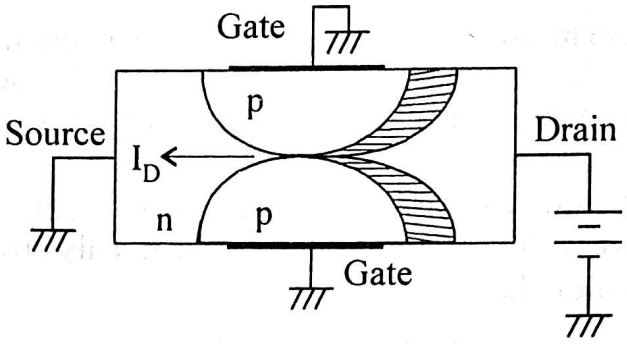

Fig. 4.36

When $V_{DS} > V_{PO}$

If V_{DS} is further increased, the depletion region thickens. So the resistivity of the channel increases. Because drain is at more positive potential, more electrons tend to move towards the drain. Hence I_D should increase. But, because channel resistance increases, I_D decreases. Therefore, the net result is I_D levels off, for any V_{DS} above V_{PO}.

$$I_D = \frac{V_{DS}}{r_{DS}}$$

In the linear region, r_{DS} is almost constant. So as V_{DS} is increased, I_D increases. When the two channels meet, as V_{DS} increases r_{DS} also increases. So I_D remains constant.(See Fig.4.37)

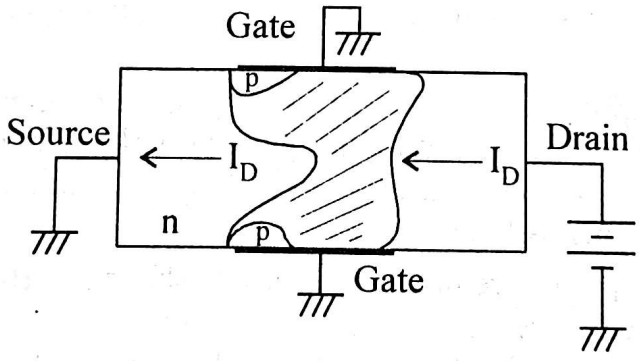

Fig 4.37 Depletion region width variation in JFET.

4.9 JFET VOLT-AMPERE CHARACTERISTICS

Suppose the applied voltage V_{DS} is small. The resulting small drain current I_D will not have appreciable effect on the channel profile. Therefore, the channel cross-section A can be assumed to be constant throughout, its length.

$$\therefore \quad A = 2b.w,$$

Where 2b is the channel width corresponding to negligible drain current and w is channel dimension perpendicular to the 'b' direction.

$$\therefore \quad I_D = Ae \; . \; N_D \; \mu_n \in$$

$$A = 2b \; . \; w$$

$$\epsilon = \frac{V_{DS}}{L}$$

$$= 2bwe \cdot N_D \mu_n \cdot \frac{V_{DS}}{L} \quad \text{.....(1)}$$

Where L is the length of the channel. Eliminating 'b' which is unknown,

$$V_{GS} = \left(1-\frac{b}{a}\right)^2 \cdot V_P$$

$$\left(1-\frac{b}{a}\right) = \left(\frac{V_{GS}}{V_P}\right)^{1/2}$$

$$\frac{b}{a} = 1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}$$

$$b = a\left[1-\left(\frac{V_{GS}}{V_P}\right)^{1/2}\right]$$

Substituting, this value in equation (1),

$$\boxed{I_D = \frac{2awe N_D \mu_n}{L}\left[1-\left(\frac{V_{GS}}{V_P}\right)^{1/2}\right] V_{DS}}$$

This is the expression for I_D in terms of V_{GS}, V_P and V_{DS} because the value of b is not directly known.

$$V_P = \frac{e.N_D}{2\varepsilon} \cdot w^2$$

But, $w = a - b\ (x)$

$b = 0$, at pinch off,

$\therefore$ $w = a$ = The spacing between the two gate dopings.

$\therefore$ $$\boxed{|V_P| = \frac{e.N_D}{2\epsilon} \cdot a^2}$$

V_{DS} controls the width of the depletion region (a – b) because for a given V_{GS}, as V_{DS} increases, the reverse potential between drain and gate increase. Therefore, depletion region width increases.

Expression for V_{GS}

$$V = \frac{e.N_D x^2}{2\epsilon}$$

We can get the expression for V_{GS} if we replace x by (a - b) and V by V_{GS}.

$\therefore$ $$V_{GS} = \frac{e.N_D(a-b)^2}{2\epsilon}$$

$$\therefore \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

This V_p is $V_{GS(off)}$ and not V_{DS} because when $V_p = V_{GS(off)}$, $I_D = 0$.

I_{DSS} = The saturation value of drain current when gate is shorted to source or $V_{GS} = 0$.

The transfer characteristics can be derived from the drain characteristics.

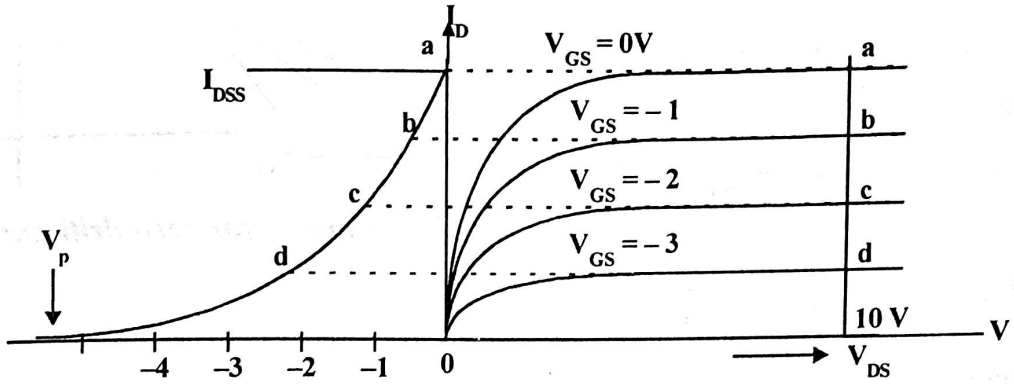

Fig 4.39 Drain and Gate characteristics of JFET.

To construct transfer characteristics, a constant value of V_{DS} is selected. Normally this is chosen in the saturation region, because the characteristics are flat. The intersection of the vertical line abcd gives a particular value of I_D for different values of V_{GS}. So the transfer characteristics between I_D and V_{GS} can be drawn.

If the end points V_P and I_{DSS} are known, a transfer characteristics for the device can be constructed.

Here V_p is again called the ***pinch off voltage*** or $V_{GS(off)}$ voltage. This is the voltage between gate and source for which I_D becomes zero. As the reverse potential between G and S increases, depletion region width increases. So channel width decreases. For some value of V_{GS} channel pinches off or I_D practically becomes zero (It cannot be exactly zero but few nano - amps). So this gate source voltage at which I_D becomes zero is also called as pinch off voltage or $V_{GS(off)}$ voltage. This pinch off voltage is different from V_{DS} voltage at which I_D levels off. Since in the latter case I_D is not zero, but channel width becomes zero and channel pinches off. This channel width is made zero either by controlling V_{DS} or V_{GS}. Hence there are two types of pinch of voltages. The specified pinch off voltage V_p for a given FET can be known if it is due to V_{DS} or V_{GS} from the polarity of the voltage V_p. For n-channel FET, V_{GS} is negative (since gate is p-type, G-S junction is reverse biased) V_{DS} is positive. If the specified V_p is –5V, (say) that it is due to $V_{GS(off)}$ because V_P is negative. If V_P is positive, it is due to V_{DS} at which I_{DSS} levels off.

4.10.1 FET Biasing for Zero Drift Current

As Temperature (T) increases, Mobility (μ) decreases at constant Electric Field (ε), therefore I_D increases. As T increases depletion region width decreases. So conductivity σ of the channel increases, I_D also increases.

I_D decreases by 0.7 % per degree centigrade.