Experiment - 8

REALIZATION OF CLOCKED SR &JK FLIP FLOP

AIM:

1. To verify the Truth Table of clocked SR Flip Flop
2. To verify the Truth Table of JK Flip Flop

COMPONENTS REQUIRED:

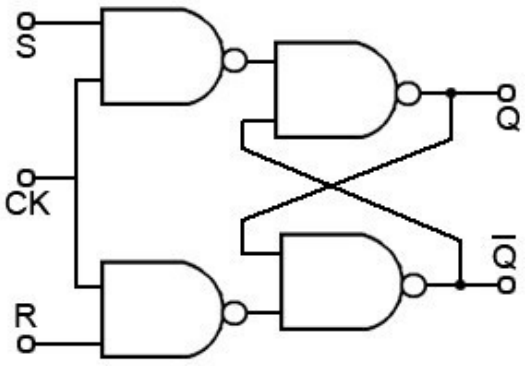
Trainer Kit	01
IC 7400	03
Patch chord	20

THEORY:

clocked SR flip flop

The SR flip-flop can be considered as a 1-bit memory, since it stores the input pulse even after it has passed. Flip-flops (or bi-stables) of different types can be made from logic gates and, as with other combinations of logic gates, the NAND and NOR gates are the most versatile, the NAND being most widely used. This is because, as well as being universal, i.e. it can be made to mimic any of the other standard logic functions, it is also cheaper to construct.

LOGIC DIAGRAM:



TRUTH TABLE FOR CLOCKED SR FLIP-FLOP:

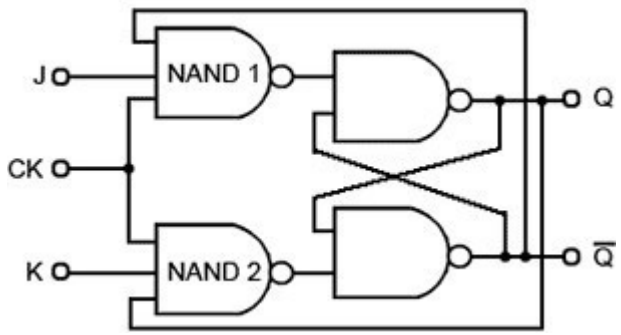
Inputs			Output Q_{n+1}	Operation
CLK	S	R		
0	X	X	Q_n	No change
⊓↓	0	0	Q_n	No change
⊓↓	0	1	0	Reset
⊓↓	1	0	1	Set
⊓↓	1	1	-	Indeterminate

JK FLIP FLOP:

Theory:

A JK flip-flop is a refinement of the SR flip-flop in that the indeterminate state of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip-flop (note that in a JK flip-flop, the letter J is for set and the letter K is for clear). When logic 1 inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, ie., if Q=1, it switches to Q=0 and vice versa.

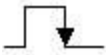
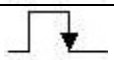
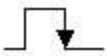
Logic Diagram:



PROCEDURE:

1. Connections are made as shown in the Logic diagrams, using the pin details of different IC's used.
2. Switch on the power supply of the Trainer Kit.
3. Verify the Truth Tables of JK FF.

TRUTH TABLE FOR JK - FF:

Inputs			Output Q_{n+1}	Operation
CLK	J	K		
0	X	X	Q_n	No change
	0	0	Q_n	No change
	0	1	0	Reset
	1	0	1	Set
	1	1	Q_n'	Toggles

RESULT:

Thus the truth table for clocked SR FF & JK FF were verified.