CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI (C.G.)

M. TECH – Microelectronics and VLSI

Eligibility Criteria:

B.E./B.Tech. in ELX/ECE/ETC &EEE/E&I or M.Sc. Physics/Electronics with GATE qualifying marks in the Electronics / Electronics & Telecommunication Engineering.

SEMESTER I

S. No.	Board of Study	Subject Code	Subject	Periods per Week			Scheme of Examination Theory / Practical			Total Marks	Credit
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	588111(28)	MICROELECTRONICS TECHNOLOGY & IC FABRICATION	3	1	-	100	20	20	140	4
2.	ET&T Engg.	588112(28)	Basics of Micro-electronics & VLSI	3	1	-	100	20	20	140	4
3.	ET&T Engg.	572112(28)	Hardware Descriptive Languages	3	1	-	100	20	20	140	4
4.	ET&T Engg.	588113(28)	CMOS ANALOG INTEGRATED CIRCUITS	3	1	-	100	20	20	140	4
5.		**Elective – I**		3	1	-	100	20	20	140	4
6.	ET&T Engg.	588121(28)	Hardware Descriptive Languages Lab I	-	-	3	75	-	75	150	2
7.	ET&T Engg.	588122(28)	CMOS Integrated Circuits Lab II	-	-	3	75	-	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L- Lecture T- Tutorial

P- Practical, ESE- End Semester Exam

CT- Class Test, TA- Teacher's Assessment

Table-I

ELECTIVE – I

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588131(28)	Introduction to MEMS
2.	ET&T	588132(28)	MEMORY DESIGN AND TESTING
3.	ET&T	588133(28)	Optoelectronics
4.	ET&T	588134(28)	Microwave Integrated Circuits
5.	ET&T	588135(28)	Neural Networks for VLSI

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **MICROELECTRONICS TECHNOLOGY & IC FABRICATION** **Code: 588111(28)**
Total Theory Periods: **40 Codes**:
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I: Material properties:
crystal structure, lattice, basis, planes, directions, angle between different planes, characterization of material based on band diagram and bonding, conductivity, resistivity, sheet resistance, phase diagram and solid solubility, Crystal growth techniques, wafer cleaning, Epitaxy, Clean room and safety requirements.

Unit II Oxidation:
Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, thickness characterization methods, multi dimension oxidation modeling. Diffusion and Ion Implantation: Diffusion process, Solid state diffusion modeling, various doping techniques, Ion implantation, modeling of Ion implantation, statistics of ion implantation, damage annealing, thermal budget, rapid thermal annealing, spike anneal, advanced annealing methods Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating .

Unit III: Etch and Cleaning:
materials used in cleaning, various cleaning methods, Wet etch, Dry etch, Plasma etching, RIE etching, etch selectivity/selective etch. Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, Resolution, Depth of Focus, Numerical Aperture (NA), sensitivity, contrast, need for different light sources, masks, Contact, proximity and projection lithography, step and scan, optical proximity correction, develop(development of resist).

Unit IV :
Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL. Planarization Techniques: Need for planarization, Chemical Mechanical Polishing

Unit V :
Copper damascene process, Metal interconnects; Multi-level metallization schemes, Process integration: NMOS, CMOS and Bipolar process.

References:
1. James Plummer, M. Deal and P.Griffin, Silicon VLSI Technology, Prentice Hall Electronics
2. Stephen Campbell, The Science and Engineering of Microelectronics, Oxford University Press, 1996
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988
4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
5. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Basics of Microelectronics & VLSI**
Total Theory Periods: **40** Code: **588112(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Introduction

MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitic, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Unit II: CMOS inverter:

static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Unit III: Static CMOS design:

Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

Unit IV: Circuit design considerations of Arithmetic circuits

Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behavior -Delay and power consumption in BiCMOS Logic

Unit V : VLSI Circuits and Systems

Introduction to VLSI systems; Timing circuit; Clock generators; Direct and PLL frequency synthesizer; Data converters; SAR, oversampled A/D and high speed converters; advanced A/D converters; filter design; Memory (volatile and non-volatile); DSP chip; CPU architecture; advanced low-power circuits.

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, , MGH, Third Ed., 2003
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005
3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004
4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007
5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill Professional, 2001

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – I Branch: ET&T Engg.
Subject: **Hardware Descriptive Languages**
Total Theory Periods: 40 Codes: **572112(28)**
Total Marks in End Semester Examination: 100 TotalTutorial Periods: 12
Minimum No. of Class Tests to be Conducted: 02

UNIT- I Introduction to VHDL:-

Basic concepts of hardware description languages. Hierarchy, Concurrency, Logic and Delay modeling. Structural, Data-flow and Behavioral styles of hardware description.

UNIT- II Architecture of event driven simulators.

Syntax and Semantics of VHDL. Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations. Component instantiation .Concurrent and sequential constructs.Use of Procedures and functions, Examples of design using VHDL.

UNIT- III Model simulation:-

Simulation, Writing test bench, converting real and integer to time, Dumpingresult into text file, Reading vector from a text file, Test bench examples, Variable file names.

UNIT-IV Hardware modeling examples:-

Modeling entity interfaces, Modeling simple elements, Different types of modeling, Modeling regular structures, Modeling delays, Modeling conditional operations, Modeling synchronous logic, State machine Modeling, Interacting state machine, Modeling a Moore FSM, Modeling Mealy FSM, Generic priority encoder, Clock divider, Generic binary multiplier, Hierarchy in design.

UNIT- V Verilog:

Syntax and Semantics of Verilog.Variable types, arrays and tables. Operators, expressions and signal assignments. Modules, nets and registers, Concurrent and sequential constructs Tasks and functions, Examples of design using Verilog. Synthesis of logic from hardware description.

Texts:

1. J. Bhaskar, "VHDL Primer", Pearson Education Asia 2001.
2. J.Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing,(Allentown, PA) 1998.
3. Douglas Perry, " VHDL programming by example" TMH 2004

References:

1. Z. Navabi, "VHDL", McGraw Hill International Ed. 1998.
2. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA), 1996.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **ANALOG INTEGRATED CIRCUITS**
Total Theory Periods: **40** Code: **588114(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT I: SINGLE STAGE AMPLIFIERS

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT II: FREQUENCY RESPONSE AND NOISE ANALYSIS

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascade stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers. 7

UNIT III OPERATIONAL AMPLIFIERS

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION

General considerations, Multiple systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BIASING CIRCUITS

Basic current mirrors, cascade current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002

ELECTIVE: I

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Introduction to MEMS**
Total Theory Periods: **40** Code: **588131(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I : Historical Background:
Silicon Pressure sensors, Micro-machining, Micro-Electro Mechanical Systems. Micro-fabrication and Micro-machining: Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA).

Unit II: Physical Micro-sensors :
Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.

Unit III: **Micro-actuators** :
Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors-Micro-actuator systems

Unit IV:
Ink-Jet printer heads, Micro-mirror TV Projector. Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Poly-silicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials**.**

Unit V: Surface Micro-machined Systems :
Success Stories, Micro-motors, Gear trains, Mechanisms.; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

Text/References

1. Stephen D. Senturia, "Micro-system Design" by, Kluwer Academic Publishers, 2001.
2. Marc Madou,
3. Fundamentals of Microfabrication by, CRC Press, 1997.Gregory Kovacs, Micromachined Transducers Sourcebook WCB McGraw-Hill, Boston, 1998.
4. M.-H. Bao, Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes by Elsevier, New York, 2000.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **MEMORY DESIGN AND TESTING**
Total Theory Periods: **40** Code: **588132(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I:

Random Access Memory Technologies Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Unit II:

Nonvolatile Memories Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-Erasable (UV) Programmable Road-Only Memories (EPROMs)-Floating Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Unit III:

Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Unit IV:

Semiconductor Memory Reliability And Radiation Effects General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

Unit V:

Advanced Memory Technologies and High-Density Memory Packaging Technologies Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories Magneto resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Text/References:

1. A.K Sharma, " Semiconductor Memories Technology, Testing and Reliability", IEEE Press.
2. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill.
3. Belty Prince, " Semiconductor Memory Design Handbook" • Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S)

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Opto Electronics**
Total Theory Periods: **40** Code: **588133(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I:
Nature of light, light sources, units of light, radio metric and photometric units, basic semi conductors, PN junction, carrier recombination and diffusion, injection efficiency, hetreo-junction, internal quantum efficiency, External quantum efficiency, double hetero junction, fabrication of heterojunction, quantum wells and super lattices.

Unit II:
Opto electronic devices, Optical modulators, modulation methods and modulators, transmitters, optical transmitter circuits, LED and laser drive circuits, LED-Power and efficiency, double hereostructure LED, LED structures, LED characteristics.

Unit III:
Laser modes, strip geometry, gain guided lasers, index guided lasers. Modulation of light, birefringence, electro optic effect, EO materials, Kerr modulators, scanning and switching, self electro optic devices, MO devices, AO devices, AO modulators.

Unit IV:
Display devices, Photoluminescence, cathode luminescence, EL display, LED display, drive circuitry, plasma panel display, liquid crystals, properties, LCD displays, numeric displays.

Unit V:
Photo detectors, thermal detectors, photoconductors, detectors, photon devices, PMT, photodiodes, photo transistors, noise characteristics of photo-detectors, PIN diode, APD characteristics, APD Design of detector arrays, CCD, Solar cells.

Text/References:

1. Opto electronics - An introduction - J Wilson and J F B J iS Hawkers. (Prentics-Hall India, 1996)
2. Optical fibre communication - J M Senior (Prentice Hall India (1985)
3. Optical fibre communication systems - J Gowar (Prentice Hall 1995).
4. Introduction to optical electronics - J Palais (Prentice Hall, 1988)
5. Semiconductor opto electronics - Jasprit Singh (McGraw-Hill, Inc, 1995)
6. Semiconductor optoelectronic devices - P Bhattacharya (Prentice Hall of India, 1995)
7. Fibre Optics and Opto-electronics, R P Khare (Oxford University Press, 2004)

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: Microwave Integrated Circuits
Total Theory Periods: **40** Code: **588134(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I:
Introduction to microwave integrated circuits: Active and passive components.
Unit II:
Analysis of micro strip lines: variational method, conformal transformation, numerical analysis; losses inmicrostrip lines; Slot line and Coupled lines;
Unit III:
Design of power dividers and combiners, directional couplers, hybrid couplers, filters.
Unit IV:
Microstrip lines on ferrite and garnet substrates; Isolators and circulators;
Unit V:
Lumped elements in MICs. Technology of MICs: Monolithic and hybrid substrates; thin and thick filmtechnologies, computer aided design.

Textbooks/References:

1. Leo Young and H. Sobol, Ed. Advances in Microwaves, Vol.2, Academic Press Inc., 1974.
2. B.Bhat and S. Koul, Stripline-like transmission lines for MICs, John Wiley, 1989.
3. T.K. Ishii, Handbook of Microwave Technology

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Neural Networks for VLSI**
Total Theory Periods: **40** Code: 588232(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I

Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons

UNIT II

ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

UNIT III

Supervised Learning and Neuro-dynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

UNIT IV

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ARTnetworks, LVQ

UNIT V

Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:

1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999
2. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.

Reference:

1. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques",Addison-Wesley, Reading, Mass, (1992).
2. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge,MA, 1996.
3. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York,1998.

LABS

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Hardware Descriptive Language Lab I**
Total Lab Periods: 40 Code: 588121(28)
Total Marks in End Semester Examination: **75**

Lab Experiments

1. Write a VHDL & Verilog Program to implement a 3:8 decoder,16:1 MUX
2. Write a VHDL & Verilog Program to implement 4 bit addition/subtraction
3. Write a VHDL& Verilog Program to implement a.4 bit comparator
4. Write a VHDL & Verilog Program to implement a Mod- 10 up counter
5. Write a VHDL & Verilog Program to perform serial to parallel transfer of 4 bit binary number
6. Write a VHDL & Verilog Program to design a 2 bit ALU containing 4 arithmetic & 4 Logic operations
7. Write a VHDL & Verilog Program to generate the 1010 sequence detector. The overlapping patterns are allowed.
8. Write a VHDL & Verilog Program to generate the 1010 sequence detector. The overlapping patterns are notallowed
9. Experiment on VHDL& Verilog program to design 4 bit shift register.
10. Experiment on VHDL& Verilog program to design Tflip flop & JK FlipFlop(toggle).
11. Experiment on VHDL& Verilog program to design JK flip flop.
12. Experiment on VHDL & Verilog program to design asynchronous binary up counter.
13. Experiment on VHDL & Verilog program to design BCD up - down counter.
14. Design Melay machine using VHDL.& Verilog
15. Design Moore machine using VHDL.& Verilog

BHILAI (C.G.)

Semester: M. Tech. – I **Branch: ET&T Engg.**

Subject: CMOS Integrated Circuits Lab II

Total Lab Periods: 40 **Code: 588122(28)**

Total Marks in End Semester Examination: 75

Lab Experiments

Schematic capture, circuit simulation, layout design, DRC, layout extraction and post-layout simulation, parasitic extraction and GDS II of following circuits

1. CMOS Inverter.
2. CMOS NAND gate
3. CMOS NOR gate
4. Resistance for a specific value.
5. Capacitor for a specific value.
6. JK Flip Flop
7. Differential amplifier
8. Current Mirror
9. 4:1 MUX
10. Op-Amp

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI (C.G.)
M. TECH – Microelectronics and VLSI
SEMESTER II

S. N	Board of Study	Subject Code	Subject	Periods per Week		Scheme of Examination			Total Marks		Credit
						Theory / Practical					
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	572211(28)	Mixed Signal and RF Circuit Design	3	1	-	100	20	20	140	4
2.	ET&T Engg.	588212(28)	SYSTEM ON CHIP	3	1	-	100	20	20	140	4
3.	ET&T Engg.	588213(28)	DIGITAL SIGNAL PROCESSING & IMPLEMENTATION WITH VLSI	3	1	-	100	20	20	140	4
4.	ET&T Engg.	588214(28)	Testing and Verification of VLSI Circuits	3	1	-	100	20	20	140	4
5.		**Elective – II**		3	1	-	100	20	20	140	4
6.	ET&T Engg.	588221(28)	RF Circuit Lab I	-	-	3	75	-	75	150	2
7.	ET&T Engg.	588222(28)	SYSTEM ON CHIP Lab II	-	-	3	75	-	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table-II
ELECTIVE – II

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588231(28)	Physics of Nano Electronic Devices
2.	ET&T E.	588232(28)	ASIC
3.	ET&T E	588233(28)	Nano-sensors
4.	ET&T E	572231(28)	ULSI Technology
5.	ET&T E	588234(28)	Process and Device Characterization & Measurements

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Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Mixed Signal and RF circuit Design**
Total Theory Periods: **40** Code: 572211(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Basic Concepts in RF design:
Nonlinearity and Time Variance, Inter symbol Interference, Random Processes & Noise , Sensitivity & Dynamic Range, Passive Impedance Transformation, Passive RLC Networks ,Characteristics of Passive IC Components.

Unit II: Distributed Systems:-
Link between Lumped and Distributed Regimes, Driving Point Impedance, Finite Length Transmission Lines, Smith Chart, S parameter, Bandwidth Estimation Techniques:-Method of Open-Circuit & Short –Circuit Time Constants.

Unit III: Low Noise Amplifier:-
General Consideration Input Matching, CMOS LNAs, CMOS Mixers, Noise in Mixers, Basic LC Oscillator Topologies, VCO, Phase Noise, CMOS LC Oscillator, Quadrature Signal Generation, Single Sideband Generation.

Unit IV: Data Converters:-
Specification of Converters, Flash Converter, Dual Slope A/D Converter, Pipelined & Sigma Delta Converter. D/A Converters, R-2R, Binary weighted, Weighted Capacitor Converter System, Self Calibrating D/A Converter System.

Unit V: Frequency Synthesizers,
Linearized PLL Models, Noise Properties of PLLs, Phase Detectors, Loop Filters, Charge Pumps, RF Synthesizer Architecture, Frequency Divider.

Text Book:
1) T. H. Lee, Design of CMOS Radio Frequency Integrated Circuits, Second Edition, CUP, 2004.
2) R. J. van de Plassche Integrated A-D and D-A Converters, Second Edition, Springer/Kluwer, 2003. (Cheap Edition)
3) B. Razavi, RF Microelectronics, IEEE Press.
Reference:
1B. Razavi, Monolithic Phase-locked Loops and Clock Recovery Circuits: Theory and Design, IEEE Press, 1996.
2. Baker, CMOS mixed signal circuit design. Wiley eastern, ISBN 978-0-470-29026-2

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **SYSTEM ON CHIP**
Total Theory Periods: **40** Code: 588212(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I LOGIC GATES

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives

UNIT II: COMBINATIONAL LOGIC NETWORKS

Introduction. Standard Cell-Based Layout .Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT III: SEQUENTIAL MACHINES

Introduction, Latches and Flip-Flops, Sequential Systems and Clocking Disciplines, Sequential System Design, Power Optimization, Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN

Introduction, Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers, High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays, References, Problems.

UNIT V FLOOR-PLANNING

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, the I/O Architecture, PAD Design.

REFERENCES

1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
2. Wayne Wolf , "Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition, 2008.
CP7023 RECONFIGURABLE COMPUTING L

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **DIGITAL SIGNAL PROCESSING & IMPLEMENTATION WITH VLSI**
Total Theory Periods: **40** Code: 588213(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I : INTRODUCTION

Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation. Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance

UNIT II: METHODS OF CRITICAL PATH REDUCTION

Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) Pipelining and parallel processing – retiming – unfolding – systolic architecture design.DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multi-computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT III: ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN

Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design. DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, discrete cosine transforms.

UNIT IV: DESIGN OF PIPELINED DIGITAL FILTERS

Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

UNIT V: SYNCHRONOUS ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP

Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

REFERENCES:

1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems,
2. Design and Implementation", John Wiley, Indian Reprint, 2007
3. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.
4. S.Y.Kuang, H.J. White house, T. Kailath, ""VLSI and Modern Signal Processing", Prentice Hall, 1995.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Testing and Verification of VLSI Circuits**
Total Theory Periods: **40** Code: 588214(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I Special purpose Subsystems: Packaging, power distribution, I/O, Clock, Trans-conductance amplifier, follower integrated circuits, etc. Design Economics: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example

UNIT II TESTING OF COMBINATIONAL CIRCUITS: Faults in digital circuits – Failures and faults –Modeling of faults – Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues.

UNIT III TESTING OF SEQUENTIAL CIRCUITS: Test generation for sequential circuits – Design of testable sequential CK5- Built in self test – Testable memory design.

UNIT IV VERIFICATION AND TESTING: Verification – Timing verification – Testing concepts – Fault coverage – ATPG – Types of tests – Testing FPGAs – Design for testability.

UNIT V VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan. VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.

Textbook:
1. Neil H.E. Weste, Davir Harris, "CMOS VLSI Design: A Circuits and system perspectives" Pearson Education 3rd Edition.
2. Wayne, Walf, "Modern VLSI design: System on Silicon" Pearson Education, Second Edition

References:
1. Pucknull, "Basic VLSI Design" PHI 3rd Edition

ELECTIVE - II

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Physics of Nano Electronic Devices**
Total Theory Periods: **40** **Codes**: 588231(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Pre-requisites Physics of Nano electronic Devices or equivalent, Atomic structure: crystal structure, defects in Solids. Electronic structure: energy bands in solids, electron-electron interactions, band structure calculations, band structure engineering,

Unit II: Mechanical properties: Phonon engineering, elasticity and strain engineering, Semi-classical transport properties: dynamics of Bloch electrons, Zener tunneling and its device applications, the Boltzmann Transport Equation and its moments, drift-diffusion, hydrodynamic equations and Monte-Carlo simulation of semiconductor devices, thermoelectric and magneto electric phenomena.

Unit III: Nano scale transport properties: scattering formalism, ballistic nano-transistors, Greens functions, Feynman paths, quantum-interference devices.;

Unit IV: Optical properties: Maxwell's equations in dielectric media, polarization in insulators, ferroelectrics, polarons and polarities, direct and indirect transitions in semiconductors, excitations, optoelectronic and photovoltaic devices.

Unit V: Frequency response of metals skin-depth, plasma frequency, plasmatic Devices. Magnetic properties: Diamagnetism and para-magnetism of ions and electrons, magnetic interactions and ferromagnetic ordering, mean field theory, symmetry-breaking and phase transitions, spintronic devices.

Text/References

1. J. P. McKelvey, introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill, 1966.
2. E. H. Nicollian and J. R. Brews, MOS Physics and Technology, John Wiley, 1982.
3. K. K. Ng, Complete Guide to Semiconductor Devices, McGraw Hill, 1995.
4. D.K. Schroder, Seminconductor Material and Device Characterization, John Wiley, 1990.
5. S. M. Sze, Physics of Semiconductor Devices, 2nd edition John Wiley, 1981.
6. C. T. Sah, Fundamentals of Solid-State Electronic Devices, Allied Publishers and World Scientific, 1991.
7. E. F. Y. Waug, Introduction to Solid State Electronics North Holland, 1980.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: M. Tech. – II | Branch: ET&T Engg.
Subject: **ASIC**
Total Theory Periods: 40 | Code: 572214(28)
Total Marks in End Semester Examination: 100 | Total Tutorial Periods: 12
Minimum No. of Class Tests to be Conducted: 02

UNIT –I

Introduction to ASIC, Modeling combinational and sequential circuits, Design entry by verilog / VHDL/FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different Verilog /VHDL constructs, and Logic
Synthesis.

UNIT – II

ASIC construction, Simulation ,Verification of complex logic design model, Verification issues like verification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models,

UNIT – III

verification Automation, physical verification, Layout planning and verifications ,ASIC design flow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction ,

UNIT – IV

Analysis: static timing analysis , current analysis , clock tree synthesis , power grid analysis , clockskew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using CMOS for various combination Ckt and Different timing parameters for ASICs.

UNIT V

Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , Automatic Test pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

Text books:

1. Wayne Wolf, "Modern VLSI Design "by Pearson Education Asia
2. Michael Smith, "Application Specific Integrated Circuits –"by Pearson Education Asia

References:

1. Geiger, Allen Strader, " VLSI Design Techniques for Analog and Digital circuits" McGraw HILL
2. Neil Waste," Principles of CMOS VLSI Design "by Pearson Education Asia

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Nano sensors**
Total Theory Periods: **40** Code: 588233(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I:
Introduction to sensors, static Characteristics and dynamic characteristics, Physical effects Photoelectric Effect, Photoluminescence Effect, Electroluminescence Effect, Chemi-luminescence Effect, Doppler Effect, Hall Effect, thermoelectric effect, magneto-optical phenomena, Quantum and classical regimes of electron transport, microscopic transport.

Unit II:
Diffusive transport: Boltzmann transport equation, electron mobility and diffusion coefficient, Drift-diffusion model. Quantum electron transport; Double barrier Resonant-Tunneling structures: Coherent tunneling and sequential tunneling, Negative differential resistance, single electron tunneling, Coulomb blockade.

Unit III:
Types of sensors-Mechanical, optical, spintronic, bioelectronics and bio-magnetic sensors-surface modification-surface materials and interactions and its examples .MEMS and NEMS definitions,

Unit IV: Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Biomimetics, Biological analogies, and design– Biomimetics Fundamentals, Biomimetics for NEMS and MEMS, Nano-ICs and Nano-computer architectures.

Unjit V: Nano-sensors: Temperature Sensors, Smoke Sensors, Sensors for aerospace and defense: Accelerometer, Pressure Sensor, Night Vision System, Nano tweezers, nano-cutting tools, Integration of sensor with actuators and electronic circuitry Biosensors. Nano machines, nano robots, electronics based on CNT, molecular Electronics. Quantum Computation: Future of Meso/Nano-electronics? -Interfacing with the Brain, towards molecular medicine, Lab-on-Bio Chips- Guided evolution for challenges and the solutions in Nano Manufacturing technology.

Text/References

1. Sergey Edward Lyshevski, Lyshevski Edward Lyshevski, Micro-Electro Mechanical and Nano-Electro Mechanical Systems, Fundamental of Nano-and Micro-Engineering – 2nd Ed., CRC Press, (2005).
2. A. S. Edelstein and Cammarata, Nanomaterials: Synthesis, Properties and Applications Institute of Physics, Bristol, Philadelphia: Institute of Physics, (2002).
3. N. P. Mahalik, Micro manufacturing and Nanotech.,Springer B Heidelberg Newyork (2006).
4. Mark J. Jackson, Micro and Nanomanufacturing, (2007).
5. Zheng Cui, Nanofabrication, Principles, Capabilities and Limits, (2008).
6. Kalantar–Zadeh K, Nanotechnology Enabled Sensors, Springer, (2008).
7. Serge Luryi, Jimmy Xu, Alex Zaslavsky, Future trends in MicroElectronics, John Wiley Sons, Inc. Hoboken, New Jersey (2007).

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **ULSI**
Total Theory Periods: **40** Code: 572231(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Clean room Technology: Classification, Design concepts, Installation, Operation and Automation. Wafer- Cleaning Technology: Basic concepts, Wet-Cleaning and Dry-Cleaning Technology. Epitaxy: Fundamental Aspects, Conventional Si Epitaxial, Low temperature Epitaxial of Si, Selective Epitaxial Growth of Si.

Unit II: conventional and Rapid thermal process: Requirement of thermal process, Rapid thermal processing, Dielectric and poly-silicon film deposition: Deposition process, APCVD & LPCVD silicon oxides, LPCVD silicon nitride, LPCVD Poly-silicon film, Plasma assisted Deposition, Applications of deposited poly-silicon, silicon oxide.

UNIT III : Lithography and Etching: Optical, Electron, X-ray , Ion lithography, Low pressure gas discharge, Etching mechanism, selectivity and profile control, Reactive plasma etching techniques and equipments, Plasma processing, Wet chemical etching. Metallization: Metal deposition technique, silicide process, CVD Tungsten plug and other plug process, Multilevel Metallization, Metallization Reliability,

UNIT IV: Process integration: Basic process module and devices consideration for ULSI, CMOS Technology, Bipolar technology, Bi-CMOS technology, MOS memory technology, Process integration consideration in ULSI Fabrication Technology. Assembly & Packaging: Package type, ULSI assembly technology, Package fabrication technology, package design consideration, Special package consideration.

UNIT V: Wafer Fab Manufacturing technology: Wafer Fab manufacturing consideration, manufacturing start-up technology, Volume ramp up Consideration, Continuous improvement. Reliability: Hot carrier injection, electromagnetism, stress migration, oxide breakdown, Effect of scaling on device reliability, Relation between DC and AC lifetime, Some recent ULSI Reliability concern, Mathematics of Failure distribution.

TEXT BOOK:

1. C.Y. Chang and S. M. Sze "ULSI Technology" McGraw-Hill publications.
2. Chen, "VLSI Technology" Wiley, March 2003.

REFERENCE BOOKS:

1. B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.
2. Sze, "Modern Semiconductor Device Physics", John Wiley & Sons, 2000

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – II Branch: ET&T Engg.

Subject: **Process and Device Characterization & Measurements**

Total Theory Periods: 40 Code: 588235(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12

Minimum No. of Class Tests to be conducted: 02

Unit I: Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometer, FTIR

Unit II: Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope

Unit III: Material and Impurity Characterization: SIMS, XRD, And EDAX

Unit IV: Electrical Characterization: • Our-probe technique, Hall Effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements

Unit V: Process and SPICE model parameter Extraction.

Textbooks /References

1. W.R. Reunyan, " Semiconductor Measurements And Instrumentation", Mc-Graw Hill.

2. Schroder, "Semiconductor Material And Device Characterization"

3. Philips F. Kare and Greydon B. Lauabee, " Characterization of semiconductor Materials", Mc-GrawHill.

4. K.V. Ravi, "Imperfections And Impurities In Semiconductor Silicon", John Wiley And Sons.

LABs:

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **RF Circuit Lab I**
Total Lab Periods: 40 Code: 588221(28)
Total Marks in End Semester Examination: **75**

Lab Experiments
Schematic capture, circuit simulation, layout design, DRC, layout extraction and post-layout simulation , Parasitic extraction and GDS II of following circuits

1. CMOSLNA
2. CMOS DAC
3. CMOS ADC
4 . CMOS VCO
5. CMOS PLL

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: M. Tech. – II Branch: ET&T Engg.
Subject: **System on Chip Lab II**
Total Lab Periods: 40 Code: 588222(28)
Total Marks in End Semester Examination: 75

1 Verilog Coding and Test Bench Verification

2 Encounter RTL Compilers: Logic Synthesis

3 Encounter Physical Design Implementation: Floor-planning, Power planning,

4 Placement, CTS, Routing, Static Timing Analysis

5 ASIC views - .lib, .lef, .gds, .sdf

6 Std. cells- Design, layout, characterization

7 PAD Design & Logical Equivalence checking

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY,
BHILAI (C.G.)
M. TECH – Microelectronics and VLSI

SEMESTER III

S. No.	Board of Study	Subject Code	Subject	Periods per Week			Scheme of Examination Theory / Practical			Total Marks	Credit
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	588311(28)	Digital Systems Engineering	3	1	-	100	20	20	140	4
2.		**Elective-III**		3	1	-	100	20	20	140	4
3.	ET&T Engg.	588321(28)	Project Work	-	-	28	100	-	100	200	14
4.	ET&T Engg.	588322(28)	Seminar on Industrial Training and Dissertation	-	-	3	-	-	20	20	2
Total				**6**	**2**	**31**	**300**	**40**	**160**	**500**	**24**

Table-III
ELECTIVE – III

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588331(28)	DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS
2.	ET&T.	588332(28)	HARDWARE SOFTWARE CO-DESIGN
3.	ET&T	588333(28)	LOW POWER VLSI CIRCUIT AND SYSTEM
4.	ET&T	588334(28)	SENSORS

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.

Subject: **Digital Systems Engineering**

Total Theory Periods: 40 Code: 588311(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12

Minimum No. of Class Tests to be conducted: 02

UNIT-I

Introduction: Engineering view of a digital system, Technology Trends and Digital Systems Engineering, Packaging of Digital Systems: A typical digital system, on chip wiring, Integrated Circuit Packages, Printed Circuit Boards, Chassis and Cabinets, Backplanes and Mother Boards, Wireand Cable, Connectors, Modeling and Analysis of Wires: Geometry and Electrical Properties ,Electrical Models of Wires, Simple Transmission Lines, Special Transmission Lines, Wire Cost Models

UNIT-II

Power Distribution: The Power Supply Network, Local Regulation, Logic Loads and on chip supply distribution, Power Supply Isolation, Bypass capacitors, Example power distribution system. Noise in Digital Systems: Noise Sources in a digital system, Power supply noise, Crosstalk, Inter symbol Interference, Managing Noise.

UNIT-III

Signaling Conventions: A Comparison of two transmission systems, considerations in a transmission system design, Signaling modes for transmission lines, signaling over lumped transmission media, Signal Encoding. Advanced Signaling Conventions: Signaling over RC Interconnect, Driving lossy LC lines, Simultaneous bidirectional signaling, AC and N of M Balanced Signaling,

UNIT-IV

Timing Conventions: A comparison of two timing conventions, considerations in timing design, Timing fundamentals, encoding timing: Signals and Events, Open Loop Synchronous timing, Closed loop timing, clock distribution. Synchronization: A Comparison of two synchronization strategies, synchronization fundamentals, synchronizer design, asynchronous design,

UNIT-V

Signaling Circuits: Terminations, transmitter circuits, receiver circuits, ESD Protection, An example signaling system. Timing Circuits: Delay line circuits, Voltage controller oscillators, Phase comparators, loop filters, Clock aligners.

Text Books:

1. William J. Dally and John Poulton, Digital Systems Engineering, Cambridge University Press,

Reference Books:

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2003.

2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits. 3rd Ed. TMH publication, 2005.

3. Jan M Rabaey, Digital Integrated Circuits, Second Edition, Prentice Hall Publications.
4. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2001.

ELECTIVE – III

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – III** Branch: ET&T Engg.
Subject: **DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS**
Total Theory Periods: **40** Code: 588331(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I FILTER TOPOLOGIES
The Bilinear Transfer Function - Active RC Implementation, Trans-conductor-C implementation, Switched Capacitor Implementation, Bi-quadratic Transfer Function, Active RC implementation Switched capacitor implementation, High Q, Q peaking and instability, Trans-conductor-C Implementation, Bi-quad.

UNIT II INTEGRATOR REALIZATION
Low pass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active-RCSNR, gm-C Integrators, Discrete Time Integrators.

UNIT III SWITCHED CAPACITOR FILTER REALIZATION
Switched capacitor Technique, Bi-quadratic SC Filters, SC N-path filters, Finite gain and band width effects, Layout consideration, Noise in SC Filters.

UNIT IV SIGNAL CONDITIONING TECHNIQUES
Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners forcapacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V SIGNAL CONDITIONING CIRCUITS
Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Trans-impedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

REFERENCES:
1. Schauman, Xiao and Van Valkenburg, “Design of Analog Filters”, Oxford University Press, 2009.
2. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning”, A wiley Interscience
Publication, John Wiley & Sons INC, 2001.
3. R.Jacob Baker, “CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008.
AP8071 ADVANCED MICROPROCESSORS AND MICROCONTROLL

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – III** Branch: ET&T Engg.
Subject: **HARDWARE SOFTWARE CO-DESIGN**
Total Theory Periods: **40** Code: 588332(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I SYSTEM SPECIFICATION AND MODELLING
Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION
Introduction, Prototyping and Emulation Techniques Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

REFERENCES:
1. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems",
Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.

3. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design " KaufmannPublishers,2001.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.
Subject: **LOW POWER VLSI CIRCUIT AND SYSTEM**

Total Theory Periods: 40 Code: 588333(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12
Minimum No. of Class Tests to be conducted: 02

Unit I: Dynamic Power Reduction:
Introduction: Why Low Power? Definition of dynamic power, Transition probability, Signal probability, Transition probability of basic gates, Glitch power, source of switching capacitance

Unit II: Dynamic Power reduction with V_{dd}, Delay vs. Power Trade-off, Dual Vdd, Dynamic Voltage Scaling (DVS), Dynamic Power Management, Capacitance Scaling, Transistor sizing, Transition probability reduction by clock gating, Logic restructuring, Input Reordering, Glitch reduction

Unit III: Standby Power Reduction: Leakage power definition, Gate Leakage, Channel Leakage, Junction Leakage. Channel leakage issue with Threshold Scaling, Leakage vs. Dynamic power

Unit IV : Technology Solution of Gate Leakage reduction: High-K, Fin-FET, Channel leakage reduction techniques: Multiple Threshold Voltage, Long Channel Transistor, Device Downsizing, Stacking, Power Gating, Dual Vdd, Dynamic Body-Biasing, Technology Solution: Fin-FET

Unit V: Short Circuit Power Reduction: Definition, Dependency on Load Capacitance, Various reduction techniques: Power Reduction at Various Design Phase System level, Algorithm level, Architecture Level (Parallel vs. Pipeline), Gate level, transistor level, Power Analysis Tool, Low Power Memory Circuit Example on DRAM, SRAM, ROM and Power issue with Dynamic Gates: Floating node and Keeper Solution.

Text Book:
1. Practical Low Power Digital VLSI Design, Author: Gary Yeap, KLUWER ACADEMIC PUBLISHERS, 2010
Reference Book:
2. Low Power CMOS VLSI Circuit Design, Author: Kuashik Roy and Sharat Prasad, John Wiley & Sons, Inc. 2009

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.
Subject: **SENSORS**
Total Theory Periods: 40 Code: 588334(28)
Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12
Minimum No. of Class Tests to be conducted: 02
Course Name: Course Code: VLSI 5242

Unit I:
Principles of Physical and Chemical Sensors: Sensor classification, sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.
Sensor Characterization and Calibration: Study of Static and Dynamic Characteristics, Sensor Reliability, aging test, failure mechanisms and their evaluation and stability study.

Unit II
Sensor Modeling: Numerical modeling techniques, Model equations, Different effects on modeling (Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological) and examples of modeling. Sensor Design and Packaging: Partitioning, Layout, technology constraints, scaling.

Unit III: Sensor Technology: Thick and thin films fabrication process, Micro machining,

Unit IV: IOC (Integrated Optical circuit) fabrication process, Ceramic material fabrication process, Wire bonding, and Packaging. Sensor Interfaces: Signal processing, Multi sensor signal processing, Smart Sensors, Interface Systems.

Unit V: Sensor Applications: Process Engineering, Medical Diagnostic and Patient monitoring,

Text Book:
1. AN INTRODUCTION TO MICROELECTROMECHANICAL SYSTEMS ENGG. BY NADIM MALUF & K WILLIAMS, ARTECH HOUSE

Reference Book:
2. RF MEMS THEORY DESIGN AND TECHNOLOGY BY G.M.REBEIZ, WILEY

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)
M. TECH – Microelectronics and VLSI

SEMESTER IV

S. No.	Board of Study	Subject Code	Subject	Periods per Week			Scheme of Examination			Total Marks	Credit
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	588421(28)	Major project + Seminar	6	-	34	300	-	200	500	23
Total				**6**	**-**	**34**	**300**	**-**	**200**	**500**	**23**