CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI (C.G.)
M. TECH – Microelectronics and VLSI
SEMESTER II

S. N	Board of Study	Subject Code	Subject	Periods per Week		Scheme of Examination			Total Marks	Credit
						Theory / Practical				
				L	T	P	ESE	CT	TA	
1.	ET&T Engg.	572211(28)	Mixed Signal and RF Circuit Design	3	1	-	100	20	20	140	4
2.	ET&T Engg.	588212(28)	SYSTEM ON CHIP	3	1	-	100	20	20	140	4
3.	ET&T Engg.	588213(28)	DIGITAL SIGNAL PROCESSING & IMPLEMENTATION WITH VLSI	3	1	-	100	20	20	140	4
4.	ET&T Engg.	588214(28)	Testing and Verification of VLSI Circuits	3	1	-	100	20	20	140	4
5.		**Elective – II**		3	1	-	100	20	20	140	4
6.	ET&T Engg.	588221(28)	RF Circuit Lab I	-	-	3	75	-	75	150	2
7.	ET&T Engg.	588222(28)	SYSTEM ON CHIP Lab II	-	-	3	75	-	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table-II
ELECTIVE – II

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588231(28)	Physics of Nano Electronic Devices
2.	ET&T E.	588232(28)	ASIC
3.	ET&T E	588233(28)	Nano-sensors
4.	ET&T E	572231(28)	ULSI Technology
5.	ET&T E	588234(28)	Process and Device Characterization & Measurements

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Mixed Signal and RF circuit Design**
Total Theory Periods: **40** Code: 572211(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Basic Concepts in RF design:
Nonlinearity and Time Variance, Inter symbol Interference, Random Processes & Noise , Sensitivity & Dynamic Range, Passive Impedance Transformation, Passive RLC Networks ,Characteristics of Passive IC Components.

Unit II: Distributed Systems:-
Link between Lumped and Distributed Regimes, Driving Point Impedance, Finite Length Transmission Lines, Smith Chart, S parameter, Bandwidth Estimation Techniques:-Method of Open-Circuit & Short –Circuit Time Constants.

Unit III: Low Noise Amplifier:-
General Consideration Input Matching, CMOS LNAs, CMOS Mixers, Noise in Mixers, Basic LC Oscillator Topologies, VCO, Phase Noise, CMOS LC Oscillator, Quadrature Signal Generation, Single Sideband Generation.

Unit IV: Data Converters:-
Specification of Converters, Flash Converter, Dual Slope A/D Converter, Pipelined & Sigma Delta Converter. D/A Converters, R-2R, Binary weighted, Weighted Capacitor Converter System, Self Calibrating D/A Converter System.

Unit V: Frequency Synthesizers,
Linearized PLL Models, Noise Properties of PLLs, Phase Detectors, Loop Filters, Charge Pumps, RF Synthesizer Architecture, Frequency Divider.

Text Book:
1) T. H. Lee, Design of CMOS Radio Frequency Integrated Circuits, Second Edition, CUP, 2004.
2) R. J. van de Plassche Integrated A-D and D-A Converters, Second Edition, Springer/Kluwer, 2003. (Cheap Edition)
3) B. Razavi, RF Microelectronics, IEEE Press.
Reference:
1B. Razavi, Monolithic Phase-locked Loops and Clock Recovery Circuits: Theory and Design, IEEE Press, 1996.
2. Baker, CMOS mixed signal circuit design. Wiley eastern, ISBN 978-0-470-29026-2

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **SYSTEM ON CHIP**
Total Theory Periods: **40** Code: 588212(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I LOGIC GATES

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives

UNIT II: COMBINATIONAL LOGIC NETWORKS

Introduction. Standard Cell-Based Layout .Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT III: SEQUENTIAL MACHINES

Introduction, Latches and Flip-Flops, Sequential Systems and Clocking Disciplines, Sequential System Design, Power Optimization, Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN

Introduction, Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers, High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays, References, Problems.

UNIT V FLOOR-PLANNING

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, the I/O Architecture, PAD Design.

REFERENCES

1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
2. Wayne Wolf , "Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition, 2008.
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CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **DIGITAL SIGNAL PROCESSING & IMPLEMENTATION WITH VLSI**
Total Theory Periods: **40** Code: 588213(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I : INTRODUCTION

Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation. Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance

UNIT II: METHODS OF CRITICAL PATH REDUCTION

Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) Pipelining and parallel processing – retiming – unfolding – systolic architecture design.DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multi-computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT III: ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN

Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design. DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, discrete cosine transforms.

UNIT IV: DESIGN OF PIPELINED DIGITAL FILTERS

Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

UNIT V: SYNCHRONOUS ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP

Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

REFERENCES:

1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems,
2. Design and Implementation", John Wiley, Indian Reprint, 2007
3. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.
4. S.Y.Kuang, H.J. White house, T. Kailath, ""VLSI and Modern Signal Processing", Prentice Hall, 1995.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Testing and Verification of VLSI Circuits**
Total Theory Periods: **40** Code: 588214(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I Special purpose Subsystems: Packaging, power distribution, I/O, Clock, Trans-conductance amplifier, follower integrated circuits, etc. Design Economics: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example

UNIT II TESTING OF COMBINATIONAL CIRCUITS: Faults in digital circuits – Failures and faults –Modeling of faults – Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues.

UNIT III TESTING OF SEQUENTIAL CIRCUITS: Test generation for sequential circuits – Design of testable sequential CK5- Built in self test – Testable memory design.

UNIT IV VERIFICATION AND TESTING: Verification – Timing verification – Testing concepts – Fault coverage – ATPG – Types of tests – Testing FPGAs – Design for testability.

UNIT V VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan. VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.

Textbook:
1. Neil H.E. Weste, Davir Harris, "CMOS VLSI Design: A Circuits and system perspectives" Pearson Education 3rd Edition.
2. Wayne, Walf, "Modern VLSI design: System on Silicon" Pearson Education, Second Edition

References:
1. Pucknull, "Basic VLSI Design" PHI 3rd Edition

ELECTIVE - II

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Physics of Nano Electronic Devices**
Total Theory Periods: **40** **Codes**: 588231(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Pre-requisites Physics of Nano electronic Devices or equivalent, Atomic structure: crystal structure, defects in Solids. Electronic structure: energy bands in solids, electron-electron interactions, band structure calculations, band structure engineering,

Unit II: Mechanical properties: Phonon engineering, elasticity and strain engineering, Semi-classical transport properties: dynamics of Bloch electrons, Zener tunneling and its device applications, the Boltzmann Transport Equation and its moments, drift-diffusion, hydrodynamic equations and Monte-Carlo simulation of semiconductor devices, thermoelectric and magneto electric phenomena.

Unit III: Nano scale transport properties: scattering formalism, ballistic nano-transistors, Greens functions, Feynman paths, quantum-interference devices.;

Unit IV: Optical properties: Maxwell's equations in dielectric media, polarization in insulators, ferroelectrics, polarons and polarities, direct and indirect transitions in semiconductors, excitations, optoelectronic and photovoltaic devices.

Unit V: Frequency response of metals skin-depth, plasma frequency, plasmatic Devices. Magnetic properties: Diamagnetism and para-magnetism of ions and electrons, magnetic interactions and ferromagnetic ordering, mean field theory, symmetry-breaking and phase transitions, spintronic devices.

Text/References

1. J. P. McKelvey, introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill, 1966.
2. E. H. Nicollian and J. R. Brews, MOS Physics and Technology, John Wiley, 1982.
3. K. K. Ng, Complete Guide to Semiconductor Devices, McGraw Hill, 1995.
4. D.K. Schroder, Seminconductor Material and Device Characterization, John Wiley, 1990.
5. S. M. Sze, Physics of Semiconductor Devices, 2nd edition John Wiley, 1981.
6. C. T. Sah, Fundamentals of Solid-State Electronic Devices, Allied Publishers and World Scientific, 1991.
7. E. F. Y. Waug, Introduction to Solid State Electronics North Holland, 1980.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: M. Tech. – II | Branch: ET&T Engg.
Subject: **ASIC**
Total Theory Periods: 40 | Code: 572214(28)
Total Marks in End Semester Examination: 100 | Total Tutorial Periods: 12
Minimum No. of Class Tests to be Conducted: 02

UNIT –I

Introduction to ASIC, Modeling combinational and sequential circuits, Design entry by verilog / VHDL/FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different Verilog /VHDL constructs, and Logic
Synthesis.

UNIT – II

ASIC construction, Simulation ,Verification of complex logic design model, Verification issues like verification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models,

UNIT – III

verification Automation, physical verification, Layout planning and verifications ,ASIC design flow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction ,

UNIT – IV

Analysis: static timing analysis , current analysis , clock tree synthesis , power grid analysis , clockskew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using CMOS for various combination Ckt and Different timing parameters for ASICs.

UNIT V

Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , Automatic Test pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

Text books:

1. Wayne Wolf, "Modern VLSI Design "by Pearson Education Asia
2. Michael Smith, "Application Specific Integrated Circuits –"by Pearson Education Asia

References:

1. Geiger, Allen Strader, " VLSI Design Techniques for Analog and Digital circuits" McGraw HILL
2. Neil Waste," Principles of CMOS VLSI Design "by Pearson Education Asia

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **Nano sensors**
Total Theory Periods: **40** Code: 588233(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I:
Introduction to sensors, static Characteristics and dynamic characteristics, Physical effects Photoelectric Effect, Photoluminescence Effect, Electroluminescence Effect, Chemi-luminescence Effect, Doppler Effect, Hall Effect, thermoelectric effect, magneto-optical phenomena, Quantum and classical regimes of electron transport, microscopic transport.

Unit II:
Diffusive transport: Boltzmann transport equation, electron mobility and diffusion coefficient, Drift-diffusion model. Quantum electron transport; Double barrier Resonant-Tunneling structures: Coherent tunneling and sequential tunneling, Negative differential resistance, single electron tunneling, Coulomb blockade.

Unit III:
Types of sensors-Mechanical, optical, spintronic, bioelectronics and bio-magnetic sensors-surface modification-surface materials and interactions and its examples .MEMS and NEMS definitions,

Unit IV: Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Biomimetics, Biological analogies, and design– Biomimetics Fundamentals, Biomimetics for NEMS and MEMS, Nano-ICs and Nano-computer architectures.

Unjit V: Nano-sensors: Temperature Sensors, Smoke Sensors, Sensors for aerospace and defense: Accelerometer, Pressure Sensor, Night Vision System, Nano tweezers, nano-cutting tools, Integration of sensor with actuators and electronic circuitry Biosensors. Nano machines, nano robots, electronics based on CNT, molecular Electronics. Quantum Computation: Future of Meso/Nano-electronics? -Interfacing with the Brain, towards molecular medicine, Lab-on-Bio Chips- Guided evolution for challenges and the solutions in Nano Manufacturing technology.

Text/References

1. Sergey Edward Lyshevski, Lyshevski Edward Lyshevski, Micro-Electro Mechanical and Nano-Electro Mechanical Systems, Fundamental of Nano-and Micro-Engineering – 2nd Ed., CRC Press, (2005).
2. A. S. Edelstein and Cammarata, Nanomaterials: Synthesis, Properties and Applications Institute of Physics, Bristol, Philadelphia: Institute of Physics, (2002).
3. N. P. Mahalik, Micro manufacturing and Nanotech.,Springer B Heidelberg Newyork (2006).
4. Mark J. Jackson, Micro and Nanomanufacturing, (2007).
5. Zheng Cui, Nanofabrication, Principles, Capabilities and Limits, (2008).
6. Kalantar–Zadeh K, Nanotechnology Enabled Sensors, Springer, (2008).
7. Serge Luryi, Jimmy Xu, Alex Zaslavsky, Future trends in MicroElectronics, John Wiley Sons, Inc. Hoboken, New Jersey (2007).

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **ULSI**
Total Theory Periods: **40** Code: 572231(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Clean room Technology: Classification, Design concepts, Installation, Operation and Automation. Wafer- Cleaning Technology: Basic concepts, Wet-Cleaning and Dry-Cleaning Technology. Epitaxy: Fundamental Aspects, Conventional Si Epitaxial, Low temperature Epitaxial of Si, Selective Epitaxial Growth of Si.

Unit II: conventional and Rapid thermal process: Requirement of thermal process, Rapid thermal processing, Dielectric and poly-silicon film deposition: Deposition process, APCVD & LPCVD silicon oxides, LPCVD silicon nitride, LPCVD Poly-silicon film, Plasma assisted Deposition, Applications of deposited poly-silicon, silicon oxide.

UNIT III : Lithography and Etching: Optical, Electron, X-ray , Ion lithography, Low pressure gas discharge, Etching mechanism, selectivity and profile control, Reactive plasma etching techniques and equipments, Plasma processing, Wet chemical etching. Metallization: Metal deposition technique, silicide process, CVD Tungsten plug and other plug process, Multilevel Metallization, Metallization Reliability,

UNIT IV: Process integration: Basic process module and devices consideration for ULSI, CMOS Technology, Bipolar technology, Bi-CMOS technology, MOS memory technology, Process integration consideration in ULSI Fabrication Technology. Assembly & Packaging: Package type, ULSI assembly technology, Package fabrication technology, package design consideration, Special package consideration.

UNIT V: Wafer Fab Manufacturing technology: Wafer Fab manufacturing consideration, manufacturing start-up technology, Volume ramp up Consideration, Continuous improvement. Reliability: Hot carrier injection, electromagnetism, stress migration, oxide breakdown, Effect of scaling on device reliability, Relation between DC and AC lifetime, Some recent ULSI Reliability concern, Mathematics of Failure distribution.

TEXT BOOK:

1. C.Y. Chang and S. M. Sze "ULSI Technology" McGraw-Hill publications.
2. Chen, "VLSI Technology" Wiley, March 2003.

REFERENCE BOOKS:

1. B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.
2. Sze, "Modern Semiconductor Device Physics", John Wiley & Sons, 2000

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – II Branch: ET&T Engg.

Subject: **Process and Device Characterization & Measurements**

Total Theory Periods: 40 Code: 588235(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12

Minimum No. of Class Tests to be conducted: 02

Unit I: Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometer, FTIR

Unit II: Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope

Unit III: Material and Impurity Characterization: SIMS, XRD, And EDAX

Unit IV: Electrical Characterization: • Our-probe technique, Hall Effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements

Unit V: Process and SPICE model parameter Extraction.

Textbooks /References

1. W.R. Reunyan, " Semiconductor Measurements And Instrumentation", Mc-Graw Hill.

2. Schroder, "Semiconductor Material And Device Characterization"

3. Philips F. Kare and Greydon B. Lauabee, " Characterization of semiconductor Materials", Mc-GrawHill.

4. K.V. Ravi, "Imperfections And Impurities In Semiconductor Silicon", John Wiley And Sons.

LABs:

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – II** Branch: ET&T Engg.
Subject: **RF Circuit Lab I**
Total Lab Periods: 40 Code: 588221(28)
Total Marks in End Semester Examination: **75**

Lab Experiments
Schematic capture, circuit simulation, layout design, DRC, layout extraction and post-layout simulation , Parasitic extraction and GDS II of following circuits

1. CMOSLNA
2. CMOS DAC
3. CMOS ADC
4 . CMOS VCO
5. CMOS PLL

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
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Semester: M. Tech. – II Branch: ET&T Engg.
Subject: **System on Chip Lab II**
Total Lab Periods: 40 Code: 588222(28)
Total Marks in End Semester Examination: 75

1 Verilog Coding and Test Bench Verification

2 Encounter RTL Compilers: Logic Synthesis

3 Encounter Physical Design Implementation: Floor-planning, Power planning,

4 Placement, CTS, Routing, Static Timing Analysis

5 ASIC views - .lib, .lef, .gds, .sdf

6 Std. cells- Design, layout, characterization

7 PAD Design & Logical Equivalence checking