CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI (C.G.)
M. TECH – Microelectronics and VLSI

SEMESTER III

S. No.	Board of Study	Subject Code	Subject	Periods per Week			Scheme of Examination Theory / Practical			Total Marks	Credit
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	588311(28)	Digital Systems Engineering	3	1	-	100	20	20	140	4
2.		**Elective-III**		3	1	-	100	20	20	140	4
3.	ET&T Engg.	588321(28)	Project Work	-	-	28	100	-	100	200	14
4.	ET&T Engg.	588322(28)	Seminar on Industrial Training and Dissertation	-	-	3	-	-	20	20	2
Total				**6**	**2**	**31**	**300**	**40**	**160**	**500**	**24**

Table-III
ELECTIVE – III

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588331(28)	DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS
2.	ET&T.	588332(28)	HARDWARE SOFTWARE CO-DESIGN
3.	ET&T	588333(28)	LOW POWER VLSI CIRCUIT AND SYSTEM
4.	ET&T	588334(28)	SENSORS

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.

Subject: **Digital Systems Engineering**

Total Theory Periods: 40 Code: 588311(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12

Minimum No. of Class Tests to be conducted: 02

UNIT-I

Introduction: Engineering view of a digital system, Technology Trends and Digital Systems Engineering, Packaging of Digital Systems: A typical digital system, on chip wiring, Integrated Circuit Packages, Printed Circuit Boards, Chassis and Cabinets, Backplanes and Mother Boards, Wireand Cable, Connectors, Modeling and Analysis of Wires: Geometry and Electrical Properties ,Electrical Models of Wires, Simple Transmission Lines, Special Transmission Lines, Wire Cost Models

UNIT-II

Power Distribution: The Power Supply Network, Local Regulation, Logic Loads and on chip supply distribution, Power Supply Isolation, Bypass capacitors, Example power distribution system. Noise in Digital Systems: Noise Sources in a digital system, Power supply noise, Crosstalk, Inter symbol Interference, Managing Noise.

UNIT-III

Signaling Conventions: A Comparison of two transmission systems, considerations in a transmission system design, Signaling modes for transmission lines, signaling over lumped transmission media, Signal Encoding. Advanced Signaling Conventions: Signaling over RC Interconnect, Driving lossy LC lines, Simultaneous bidirectional signaling, AC and N of M Balanced Signaling,

UNIT-IV

Timing Conventions: A comparison of two timing conventions, considerations in timing design, Timing fundamentals, encoding timing: Signals and Events, Open Loop Synchronous timing, Closed loop timing, clock distribution. Synchronization: A Comparison of two synchronization strategies, synchronization fundamentals, synchronizer design, asynchronous design,

UNIT-V

Signaling Circuits: Terminations, transmitter circuits, receiver circuits, ESD Protection, An example signaling system. Timing Circuits: Delay line circuits, Voltage controller oscillators, Phase comparators, loop filters, Clock aligners.

Text Books:

1. William J. Dally and John Poulton, Digital Systems Engineering, Cambridge University Press,

Reference Books:

1. S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, Third Edition, McGraw Hill, 2003.

2. Jackson & Hodges, Analysis and Design of Digital Integrated circuits. 3rd Ed. TMH publication, 2005.

3. Jan M Rabaey, Digital Integrated Circuits, Second Edition, Prentice Hall Publications.
4. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2001.

ELECTIVE – III

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – III** Branch: ET&T Engg.
Subject: **DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS**
Total Theory Periods: **40** Code: 588331(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I FILTER TOPOLOGIES
The Bilinear Transfer Function - Active RC Implementation, Trans-conductor-C implementation, Switched Capacitor Implementation, Bi-quadratic Transfer Function, Active RC implementation Switched capacitor implementation, High Q, Q peaking and instability, Trans-conductor-C Implementation, Bi-quad.

UNIT II INTEGRATOR REALIZATION
Low pass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active-RCSNR, gm-C Integrators, Discrete Time Integrators.

UNIT III SWITCHED CAPACITOR FILTER REALIZATION
Switched capacitor Technique, Bi-quadratic SC Filters, SC N-path filters, Finite gain and band width effects, Layout consideration, Noise in SC Filters.

UNIT IV SIGNAL CONDITIONING TECHNIQUES
Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners forcapacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V SIGNAL CONDITIONING CIRCUITS
Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Trans-impedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

REFERENCES:
1. Schauman, Xiao and Van Valkenburg, “Design of Analog Filters”, Oxford University Press, 2009.
2. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning”, A wiley Interscience
Publication, John Wiley & Sons INC, 2001.
3. R.Jacob Baker, “CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008.
AP8071 ADVANCED MICROPROCESSORS AND MICROCONTROLL

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – III** Branch: ET&T Engg.
Subject: **HARDWARE SOFTWARE CO-DESIGN**
Total Theory Periods: **40** Code: 588332(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I SYSTEM SPECIFICATION AND MODELLING
Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION
Introduction, Prototyping and Emulation Techniques Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

REFERENCES:
1. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems",
Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.

3. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design " KaufmannPublishers,2001.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.
Subject: **LOW POWER VLSI CIRCUIT AND SYSTEM**

Total Theory Periods: 40 Code: 588333(28)

Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12
Minimum No. of Class Tests to be conducted: 02

Unit I: Dynamic Power Reduction:
Introduction: Why Low Power? Definition of dynamic power, Transition probability, Signal probability, Transition probability of basic gates, Glitch power, source of switching capacitance

Unit II: Dynamic Power reduction with V_{dd}, Delay vs. Power Trade-off, Dual Vdd, Dynamic Voltage Scaling (DVS), Dynamic Power Management, Capacitance Scaling, Transistor sizing, Transition probability reduction by clock gating, Logic restructuring, Input Reordering, Glitch reduction

Unit III: Standby Power Reduction: Leakage power definition, Gate Leakage, Channel Leakage, Junction Leakage. Channel leakage issue with Threshold Scaling, Leakage vs. Dynamic power

Unit IV : Technology Solution of Gate Leakage reduction: High-K, Fin-FET, Channel leakage reduction techniques: Multiple Threshold Voltage, Long Channel Transistor, Device Downsizing, Stacking, Power Gating, Dual Vdd, Dynamic Body-Biasing, Technology Solution: Fin-FET

Unit V: Short Circuit Power Reduction: Definition, Dependency on Load Capacitance, Various reduction techniques: Power Reduction at Various Design Phase System level, Algorithm level, Architecture Level (Parallel vs. Pipeline), Gate level, transistor level, Power Analysis Tool, Low Power Memory Circuit Example on DRAM, SRAM, ROM and Power issue with Dynamic Gates: Floating node and Keeper Solution.

Text Book:
1. Practical Low Power Digital VLSI Design, Author: Gary Yeap, KLUWER ACADEMIC PUBLISHERS, 2010
Reference Book:
2. Low Power CMOS VLSI Circuit Design, Author: Kuashik Roy and Sharat Prasad, John Wiley & Sons, Inc. 2009

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: M. Tech. – III Branch: ET&T Engg.
Subject: **SENSORS**
Total Theory Periods: 40 Code: 588334(28)
Total Marks in End Semester Examination: 100 Total Tutorial Periods: 12
Minimum No. of Class Tests to be conducted: 02
Course Name: Course Code: VLSI 5242

Unit I:
Principles of Physical and Chemical Sensors: Sensor classification, sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.
Sensor Characterization and Calibration: Study of Static and Dynamic Characteristics, Sensor Reliability, aging test, failure mechanisms and their evaluation and stability study.

Unit II
Sensor Modeling: Numerical modeling techniques, Model equations, Different effects on modeling (Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological) and examples of modeling. Sensor Design and Packaging: Partitioning, Layout, technology constraints, scaling.

Unit III: Sensor Technology: Thick and thin films fabrication process, Micro machining,

Unit IV: IOC (Integrated Optical circuit) fabrication process, Ceramic material fabrication process, Wire bonding, and Packaging. Sensor Interfaces: Signal processing, Multi sensor signal processing, Smart Sensors, Interface Systems.

Unit V: Sensor Applications: Process Engineering, Medical Diagnostic and Patient monitoring,

Text Book:
1. AN INTRODUCTION TO MICROELECTROMECHANICAL SYSTEMS ENGG. BY NADIM MALUF & K WILLIAMS, ARTECH HOUSE

Reference Book:
2. RF MEMS THEORY DESIGN AND TECHNOLOGY BY G.M.REBEIZ, WILEY