Design of a Low Power High Resolution High Speed 9 bit DAC using 0.18µm CMOS Technology

Project Report

Submitted in partial fulfilment of the requirements for the summer internship in

By

Hrit Mukherjee

and

Upali Ghosh

DECLARATION

We, **Upali Ghosh** and **Hrit Mukherjee**, hereby declare that this report entitled **"Design of a Low Power High Resolution High Speed 9 bit DAC using 0.18µm CMOS Technology"** submitted by us to **Variable Energy Cyclotron Centre(VECC)**, **Kolkata** as a part of our summer internship project**,** is a record of bonafide work carried out by us under the guidance of **Mr. Tanushyam Bhattacharya, Head of the Department of Application Specific Integrated Circuits, Computer Division, VECC, Kolkata.**

Hrit Mukherjee

Upali Ghosh

Date:

CERTIFICATE

This is to certify that the report entitled **“Design of a Low Power High Resolution High Speed 9 bit DAC using 0.18µm CMOS Technology”** submitted by **Upali Ghosh** and **Hrit Mukherjee,** students of second year of **Department of Electronics and Telecommunications Engineering**, **Jadavpur University, Kolkata**, is a record of bonafide work carried out by them under my supervision as a part of their summer internship project.

Mr. Tanushyam Bhattacharya,

HoD,

Application Specific Integrated Circuits,

Computer Division,

Variable Energy Cyclotron Centre,

Kolkata.

Date:

ACKNOWLEDGEMENT

We wish to take this opportunity to express our deepest appreciation and sincere gratitude to our project mentor **Mr. Tanushyam Bhattacharya** for his spontaneous guidance and continuous encouragement during the course of our project. We would like to convey special thanks to **Piyush Bahre** and **Manish Jha,** who worked on strengthening our Analog circuit background and provided a lot of support and valuable inputs to the problems that we faced while designing this circuit thus, cooperating with us and creating a joyful and happy atmosphere to work on.

ABSTRACT

With the advent of high performance (in terms of speed, power and area) digital circuits, the need for data converters with high accuracy and speed for various kinds of applications, has attracted the attention of scientists and technologists all over the world. Constant efforts are being put in to miniaturize the data converters from the point of low power and less area. Constant Fraction Discriminator (CFD) is a special type of time pick-off circuit which determines the time of positron-annihilation experiments. As such, it requires a threshold voltage at the input of one of its comparators whose value is set using a DAC. In view of this, an attempt has been made to develop a high speed, high resolution and low power digital to analog converter (DAC) using CMOS technology.

Literature survey on DACs has indicated various DAC architectures based on implementation modes. The current steering DAC architecture helps in keeping the load current (i.e. current drawn by the DAC) constant, and in achieving a higher speed of operation. The power drawn can be minimized by choosing a low value of current for LSB. Keeping these considerations in view, a 9-bit current steering DAC has been attempted. The entire DAC architecture has been divided into two separate blocks: one being a 6 bit DAC with a resolution of 1mV, and the other being a 3 bit DAC with a resolution of 64mV. Since, the fine DAC has a full scale voltage of 63mV and the coarse DAC has 1 LSB = 64mV, the overall combination of the two corresponds to a 9 bit DAC having a resolution of 1mV and full scale voltage range of 512mV. The advantage of this combined architecture is that, while in a conventional 9 bit current steering DAC, $(2^9 - 1) = 511$ current sources are required, this architecture requires only $[(2^6 - 1) + (2^3 - 1)] = 70$ current sources. This results in a reduced chip area and low power consumption. The technology used in the design of this DAC is TSMC 0.18 µm CMOS. In this, it has been possible to achieve a reasonable accuracy with a LSB current of 2 µA, which has resulted in a further low power operation of the DAC. With these considerations, a design for current steering DAC has been arrived at and simulated using LT-Spice. It has been found that this DAC needs a power supply of 1.8 V with a stability of ±2 mV to result in a change of less than 1 µA (less than 0.5 LSB) at the output of the DAC. Further, the current that is to be supplied is about 880 µA.

An operational amplifier acting as a non-inverting summer has been used to add up the coarse and fine responses of the DAC. The INL, DNL of the fine and coarse DACs separately are found to be within ±0.5 LSB and though the combined architecture has very high non-linearity error at a handful of discrete points, most of the data points have these errors well within ±0.5 LSB with a power consumption of about 1.584mW.

This project indicates the effort put in to realize the proposed 9-bit DAC, organized into 8 chapters.

CONTENTS

CHAPTER 1

INTRODUCTION

In most of the electronic systems the input and output signals are analog in nature. Hence there are analog processing devices like amplifiers as input and output devices. However most of the modifications to be carried out on the input signals before obtaining the outputs are carried out in digital domain. Therefore, there is a need to convert the analog input signals into digital signals at the input end, and after processing them in the digital domain, they have to be converted back into analog signals. The circuits that convert analog signals to digital signals are known as Analog to Digital Converters(ADCs) and the circuits that convert digital signals to analog signals are called Digital to Analog Converters (DACs).

CHAPTER 2

LITERATURE SURVEY

DAC PERFORMANCE MEASURES

There are many performance measures for a DAC. They can be divided into static measures, dynamic measures, and frequency-domain measures.

STATIC PERFORMANCE MEASURES

The static performance measures include integral nonlinearity error, differential nonlinearity error, zero-scale error and gain error.

Zero Scale Error

For an input value that is equal to zero, the output value of a DAC should also be zero, but practically it is not so. The deviation from zero is called zero-scale error, E_{ZS}.

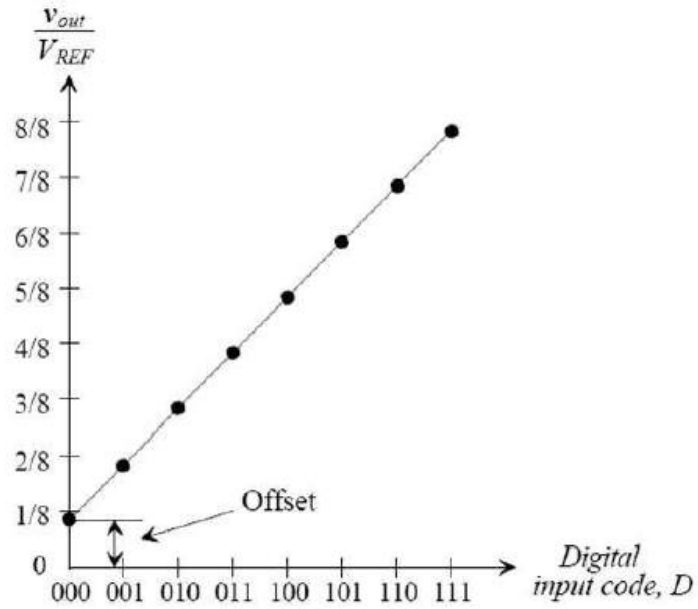


FIG 2.1 Example of Zero Scale Error

Gain Error

Gain error, E_G is defined as the difference in slope between the ideal curve and the actual curve. Before the gain error is calculated the offset error is subtracted. The gain error can be calculated according to the formula,

Egain = IdealSlope - ActualSlope

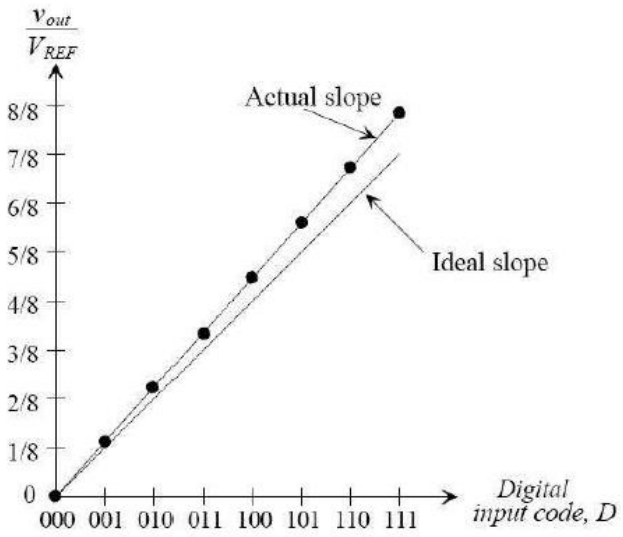


FIG 2.2 Example of Gain Error

Differential Non-Linearity

The DNL specification is a way to characterise the difference between two successive voltage levels that a DAC produces. DNL (Differential Non-Linearity) shows how much two adjacent code analog values deviate from the ideal 1 LSB step.

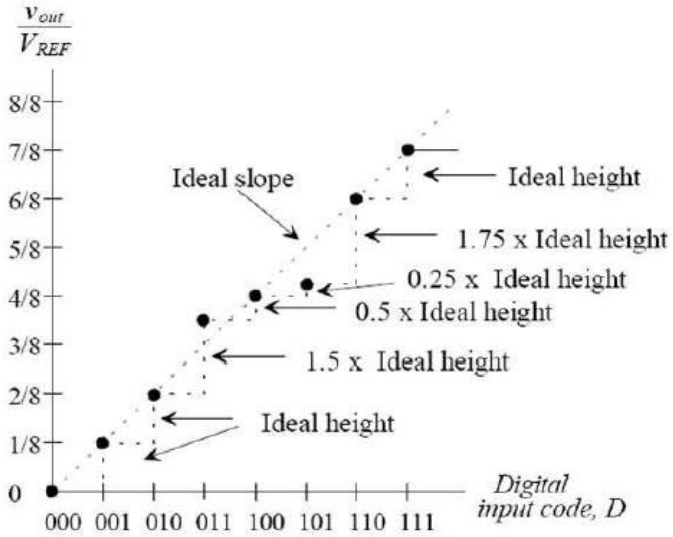


FIG 2.3 Example showing DNL

The actual increment heights are labeled with respect to the ideal increment height, which is 1 LSB. The increment height corresponding to 001 is equal to the corresponding height of the ideal case, therefore DNL1 = 0. In case of 011, increment is not equal to the ideal curve but is 1.5 times the ideal height. Therefore, DNL3 = 1.5 LSB - 1 LSB = 0.5 LSB.

Integral Non-Linearity

INL (Integrated Non-Linearity) shows how much the DAC transfer characteristic deviates from an ideal one. The ideal characteristic is usually a straight line. INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1 LSB steps).

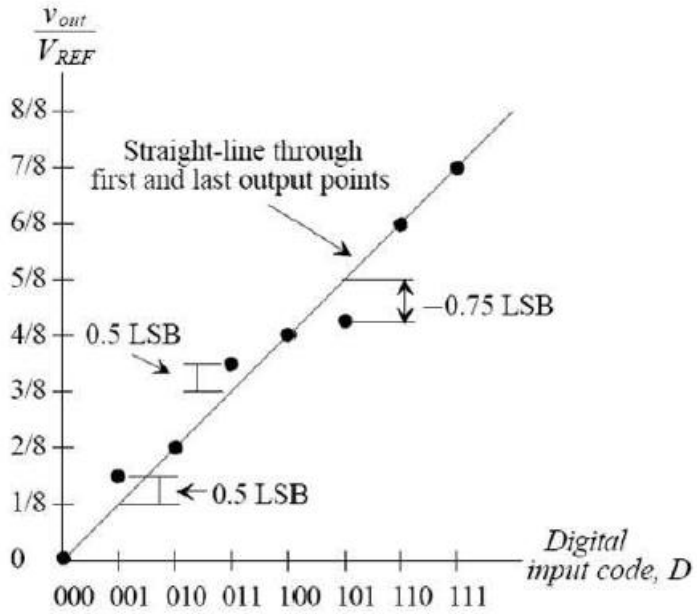


FIG 2.4 Example illustrating INL

Outputs corresponding to 001 and 011 are 1/2 LSB higher than the ideal values, therefore, INL1 = INL3 = 0.5 LSB.

Monotonicity

If a DAC is monotonic, then the output always increases as the input increases. It is normally not necessary to state such a condition for a DAC explicitly to have this behavior. If the maximum DNL error is less than 1 LSB it is said that the DAC is guaranteed to be monotonic. Monotonicity can also be guaranteed if the maximum INL error is less than 0.5 LSB.

DYNAMIC PERFORMANCE MEASURES

The dynamic performance describes the behavior of the DAC when the digital input makes transitions. The major dynamic measures of a DAC are its settling time and slew rate which decides the speed of the DAC.

Settling Time

In DACs settling time gives information about the time required by the converter to meet the right output value after a change in the input code. The settling time has many components as shown in FIG 2.5. The delay time is very small and during this interval there is no output change. During slew time, instead, the output amplifier moves at its highest possible speed towards the final value or the output capacitance gets charged. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band.

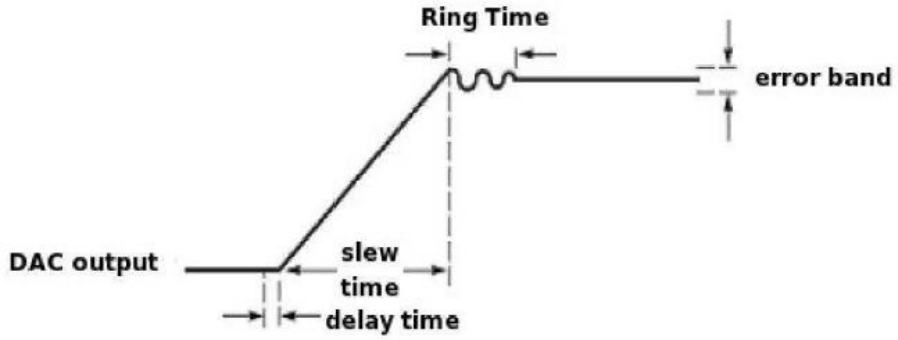


FIG 2.5 Settling Time

Slew Rate

Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

Total Harmonic Distortion

THD which represents the amount of signal distortion can be defined as the square root of the ratio of total harmonic energy and fundamental energy, as is indicated below:

$$THD = \sqrt{\frac{P - P_1}{P_1}} = \sqrt{\frac{\sum_{n=2}^{\infty} P_n}{P_1}}$$

where P is the total energy; P_1 is the fundamental energy; P_n is the n-th order harmonic energy .

Also THD can be defined as the ratio of the root-mean-square value of total harmonic voltage (current) and fundamental voltage (current) when the

load is pure resistance, as indicated below:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} U_n^2}}{U_1} \times 100\%$$

where U1 is the root-mean-square value of the fundamental voltage; U_n is the root-mean-square value of the n-th order harmonic voltage.

A chief criterion to appraise the accuracy of synthesized digital sinusoidal waves is THD, which depends on three factors:

(1) the number M of discrete points in a sinusoidal function period

(2) the resolution N of DAC, also the bit number of DAC

(3) the converting frequency F of DAC with the value of M×f (where f is the frequency of the synthesized sinusoidal wave)

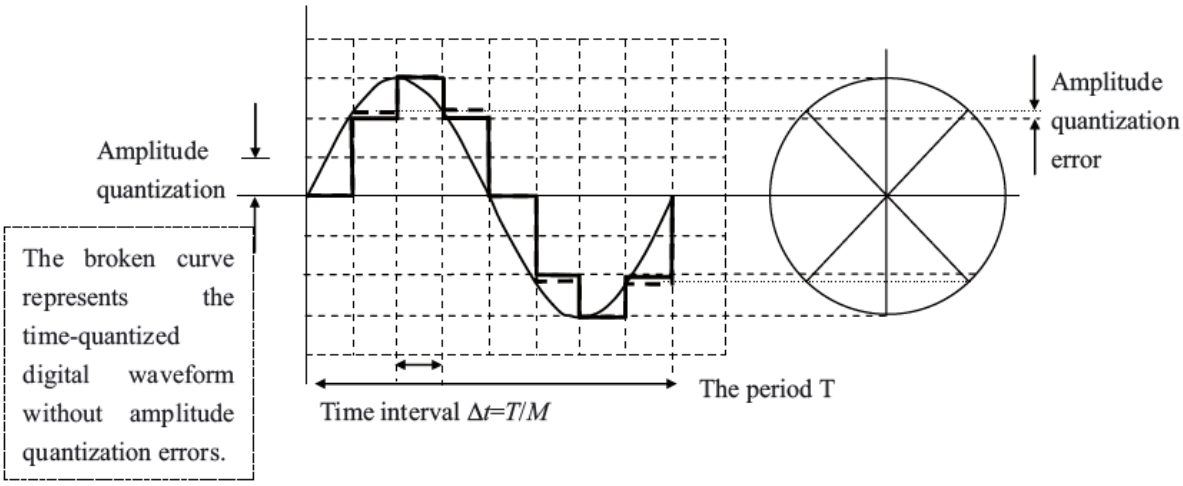


FIG 2.6 Sinusoidal Wave Fitted by Rectangular Steps at the Output-end of DAC

Power Supply Rejection Ratio

1. Power supply rejection ratio at zero scale is measured by varying VDD and is given by: PSRR = 20log[E_{ZS}(VDD_{max} - VDD_{min})/VDD_{max}]
2. Power supply rejection ratio at full scale is measured by varying VDD and is given by: PSRR = 20log[E_G(VDD_{max} - VDD_{min})/ VDD_{max}]

DAC ARCHITECTURES

DAC architectures can be broadly classified into:

1. Thermometer Coded DAC architecture, and

2. Binary Weighted DAC architecture

The thermometer coded DAC contains number of reference elements equal to the maximum value of the digital word. For example, a 10-bit thermometer DAC would have 1023 segments, i.e. 2^{N-1} thermometer bits, corresponding to N binary bits.

Binary-weighted, binary-encoded, or binary-scaled, uses binary scaled elements e.g., current sources, resistors, or capacitors. This means that every element is weighted with 2^1, 2^2, 2^3 ... 2^N where N is the number of bits.

The main advantage of binary weighted DAC architecture over thermometer coded DAC is that it requires less number of reference sources (voltage/current) and switches. Hence, it saves a lot of chip area, thus being cost effective. But at the same time, it exhibits random glitches during output transition. Though this problem doesn't exist in thermometer coded DAC as it goes through only a single bit change per output transition, it is highly expensive. Since in this project, the motive is to build a DAC for low power applications, binary weighted DAC architecture has been adopted.

DAC ARCHITECTURES BASED ON IMPLEMENTATION MODES

There are three different implementation modes for DACs: voltage-mode, current-mode, and charge- redistribution mode. In voltage mode DACs, the element values are given by voltage levels. With current-mode DAC, the elements are given by currents as for example switched current sources or resistors dividing a major current into weighted sub-currents. In case of charge redistribution DAC, elements are given by capacitor values and the operation of the DAC is given by a switched-capacitor techniques.

Weighted Resistor DAC

In the weighted resistor type DAC, each digital level is converted into an equivalent analog voltage or current. The following figure shows the circuit diagram of the binary weighted resistor type DAC.

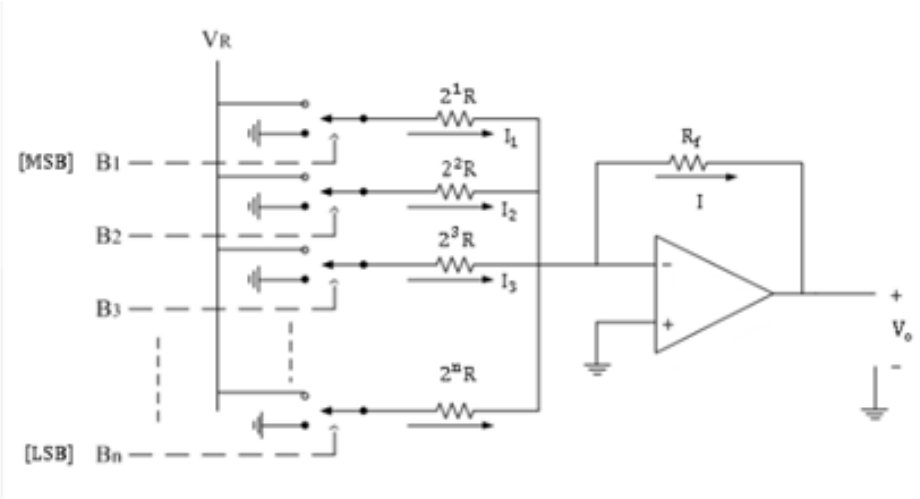


FIG 2.7 Weighted resistor DAC

It consists of parallel binary weighted resistor bank and a feedback resistor R_f.

The switch positions decide the binary word (i.e. B_1, B_2, B_3,…,B_n). In the circuit op-amp is used as current to voltage converter. When the switches are closed the respective currents are flowing through resistors as shown in the circuit diagram above.

Since input current to the op-amp is zero, the addition current flows through feedback resistor.

$\therefore I = I_1 + I_2 + I_3 + \ldots\ldots\ldots\ldots + I_n$

The inverting terminal of op-amp is virtually at ground potential.

Therfore, $V_o = - IR_f$

$= - [I_1 + I_2 + I_3 + \ldots + I_n]R_f$

$= - \frac{Rf}{R} V_R[B_1 2^{-1} + B_2 2^{-2} + B_3 2^{-3} + \ldots + B_n 2^{-n}]$

If $R_f = R$, $V_o = - V_R[B_1 2^{-1} + B_2 2^{-2} + B_3 2^{-3} + \ldots + B_n 2^{-n}]$

Current Steering DAC

This architecture consists of weighted currents produced by current mirrors, switches to steer the current and an adder. The reference elements are current sources and sum elements are only wire connections. The switches are normally MOS transistors. The switches are controlled by the input bits. In the figure, binary-weighted current sources are produced by the use of current mirrors. This means that every element is weighted with 2^1, 2^2, 2^3 ... 2^N where N is the number of bits. The output current is given by

$$I_{out} = b_0 I_{unit} + b_1 2^{-1} I_{unit} + \ldots + b_N 2^{-N} I_{unit}$$

In FIG 2.8, an N-bit current-steering DAC is shown. The current-steering DAC in the figure is binary-weighted, as can be seen from the weighting of the current sources. The switches are controlled by the input word. Depending on the input word, the current source is switched to the load or to the ground which improves the speed of the DAC.

The advantage of current steering architecture is the ease of implementing the elements on the chip. The current sources are current mirrors implemented using FETs. The weightage in the current values can be obtained by simply varying the widths of the transistors. All the switches can also be realized by using FETs. Thus, all the elements in current steering DAC can be realized using MOSFETs. The power efficiency is also very high since most of the power is dissipated in the small load resistor at the output. This architecture is thus suitable for high speed design and cost effective to implement. The major difficulty is to realize current sources with ideal characteristics because of device mismatches, and to avoid the switching related glitches.

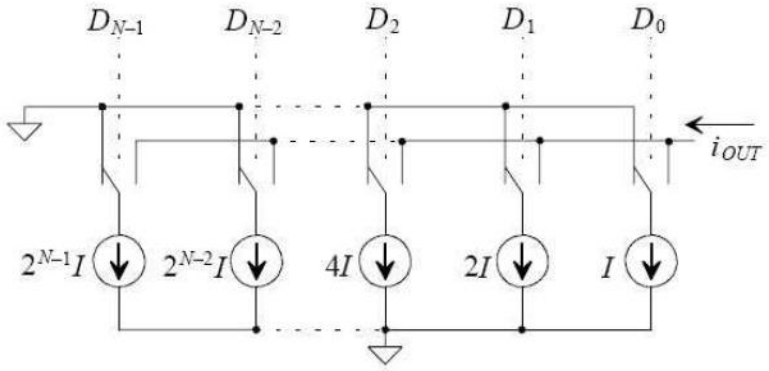


FIG 2.8 Current Steering DAC using Binary-weighted Current Sources

Charge Redistribution DAC

The charge-redistribution DAC is a switched-capacitor (SC) DAC, where the charge stored on a number of scaled capacitors is used to perform the conversion. The MSB capacitor is 2^{N-1} times larger than the LSB capacitor. In FIG 2.9 an N-bit charge distribution DAC is shown. This is a type of switched-capacitor DAC with an amplifier at the output.

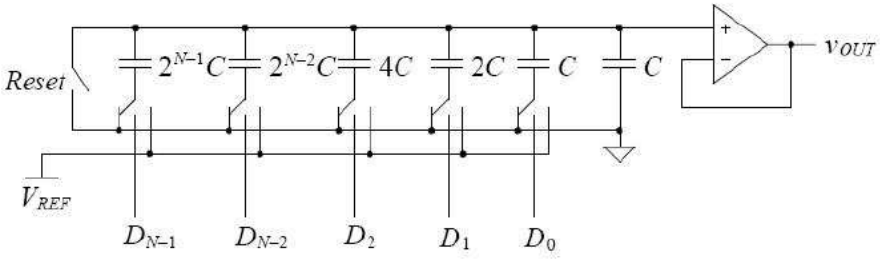


FIG 2.9 Charge Redistribution DAC

The limitation of the converter is due to a number of factors such as the matching of the capacitors, the switch on-resistance, and the finite bandwidth of the amplifier. The matching error of the capacitors affects the monotonicity of the DAC. Another significant problem is that a substantial amount of chip area is occupied due to the use of capacitors in CMOS technology.

Resistor String DAC

This DAC consists of a resistor string which acts as voltage divider. It provides taps for the different voltage levels with the use of equally values resistors. An example of a 3 bit-DAC is shown in FIG 2.10.

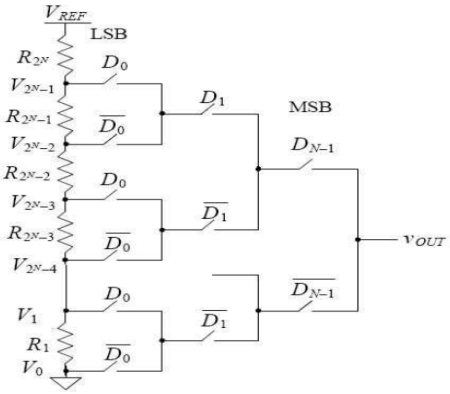


FIG 2.10 A Resistor String DAC

This is one of the most common DAC architecture used in ICs due to its simple implementation. It is also fast and inherently monotonic. This architecture is however not suitable for higher resolution DACs because it requires large number of resistors and switches as resolution increases over 10 bits. Moreover, to avoid mismatching of resistors and maintain accuracy, there is a need for trimming a large unary array of resistors.

R-2R Ladder DAC

The R-2R DAC is a binary weighted DAC that uses a repeating cascaded structure of resistor values R and 2R as shown in FIG 2.11. The advantage is that this type of implementation uses a small number of components, and only two different sizes of resistors. This improves the precision due to the relative ease of producing equal valued matched resistors. The disadvantages are that if the number of bits is high there is a time delay between the LSB and the MSB, and the resistors values must have high linearity.

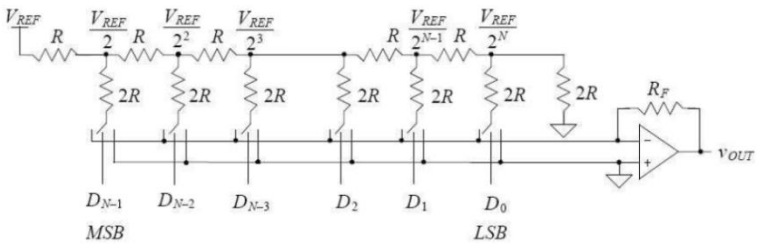


FIG 2.11 R-2R DAC Architecture

CHAPTER 3

CURRENT MIRROR

In this section, we turn our attention towards design and simulation of current mirrors, which will serve as the weighted current sources in our current-steering DAC architecture.

BASIC CURRENT MIRROR

A current mirror is a circuit that sources or sinks a constant current. NMOS transistors are employed for sinking current and PMOS transistors for sourcing current.

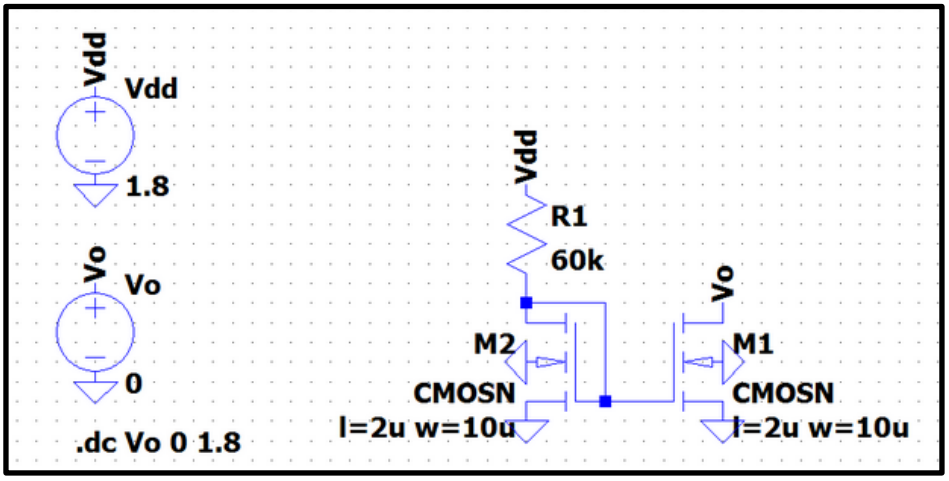


FIG 3.1 Basic Current Mirror

The basic NMOS current sink shown above has been designed to sink a current of 20µA. The MOSFET M2 is diode connected to always keep it in saturation. Equal gate to source voltages VGS1=VGS2 ensure that the current in M2 is mirrored in M1, provided that M1 is in saturation. Output has been shown below for a dc sweep of the reference voltage Vo from 0 to 1.8V. The transistors have the same aspect ratio(W/L ratio),VGS and Id so that their drain to source voltages are equal. Results have been derived neglecting channel length modulation for which we see in the output below that an ideal constant current has not been obtained.

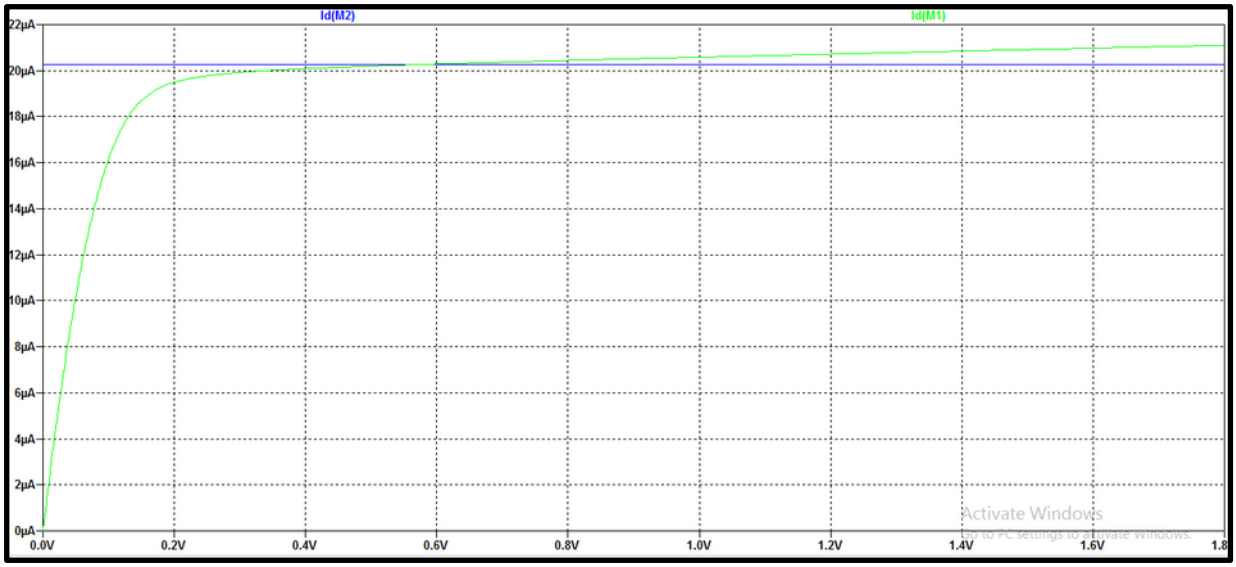


FIG 3.2 Operation of NMOS current mirror

BIASING THE CURRENT MIRROR

Setting the bias current using a resistor is not feasible as the currents become dependent on voltage supply and temperature. The reference current I_{REF}(of M2) linearly varies with supply(VDD). The mirrored current Io(of M1) is in turn dependent on both λV_{DS}(of M1) and I_{REF}. Therefore, the design of the bias circuit should be such that it is independent of power supply variations.

SUPPLY INDEPENDENT BIASING

Instead of connecting the resistance in the drain of mosfet M2, it is tied to the source of M1(in which current is mirrored) so that reference current I_{REF}(of M2) becomes independent of supply VDD.

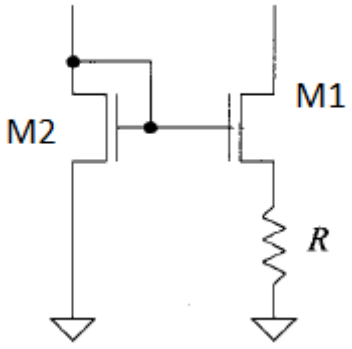


FIG 3.2 Basic Current Mirror with Resistance in Source

However, in this approach the value of mirrored current in M1 is not known as the gate to source voltages of the mosfets are not equal due to the voltage drop across resistance R. It is apparent that VGS2>VGS1 and they are related by the equation, VGS2 = VGS1 + I_D(M1)R. In order to force the same current I_{REF} in M1, a PMOS current mirror is added as shown below.

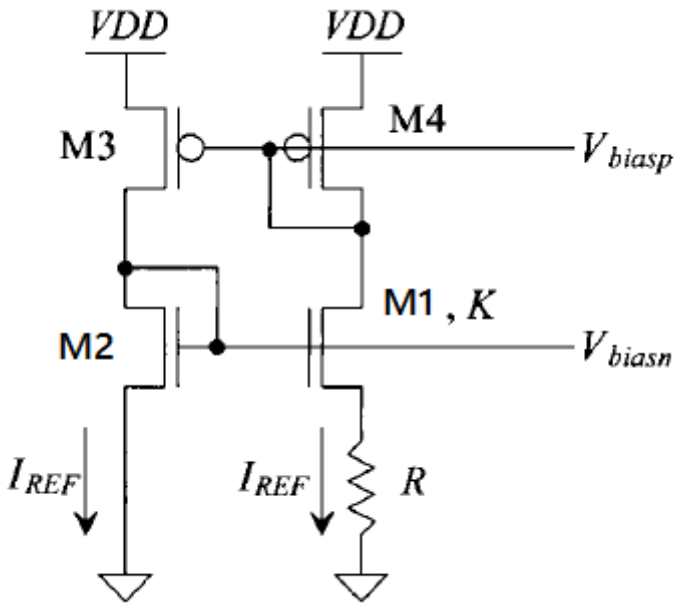


FIG 3.3 PMOS added device

For the above figure, when M1 has the same size as M2, it is not powerful enough to sink the current I_{REF} (supplied by M3), because of a smaller VGS. For M2 to sink current I_{REF} with a smaller VGS, the W/L ratio has to be enhanced.
For I_D(M1) to be equal to I_{REF}, β1 is made equal to $k\beta_2$(by increasing the width of M1).
Thus the resulting circuit is called a beta multiplier reference circuit.

VGS2 = VGS1 + I_{REF}R

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN}$$

$$I_{REF} = \frac{2}{R^2 KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \text{ or } V_{DS,sat} = V_{GS} - V_{THN} = \frac{2}{R \cdot KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right)$$

Taking k=4, we get

$$g_m = \sqrt{2KP_n \frac{W}{L} \cdot I_{REF}} = \frac{1}{R}$$

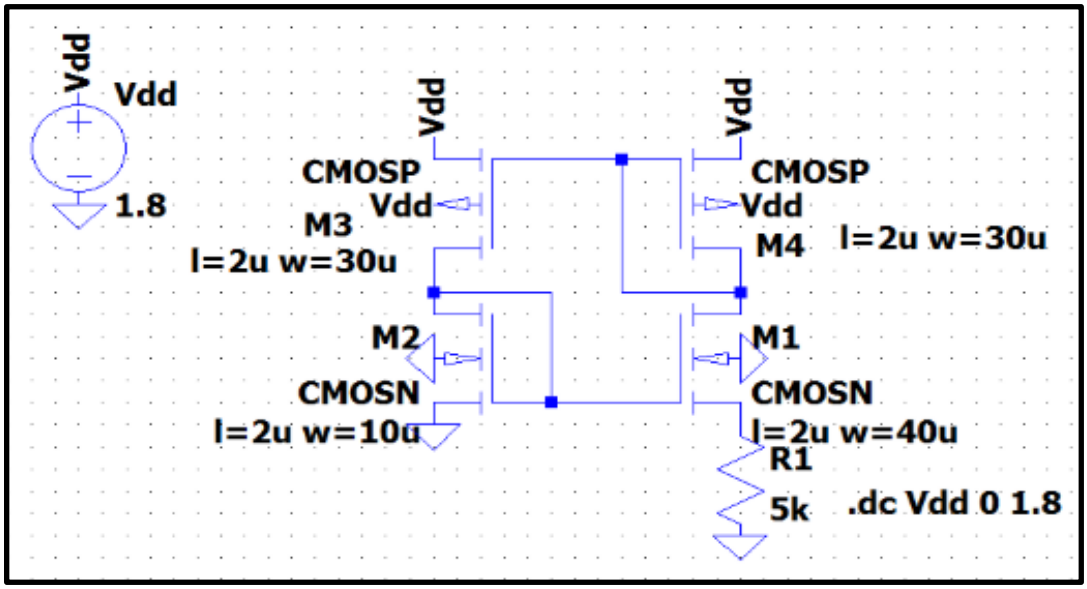


FIG 3.4 Long Channel Design

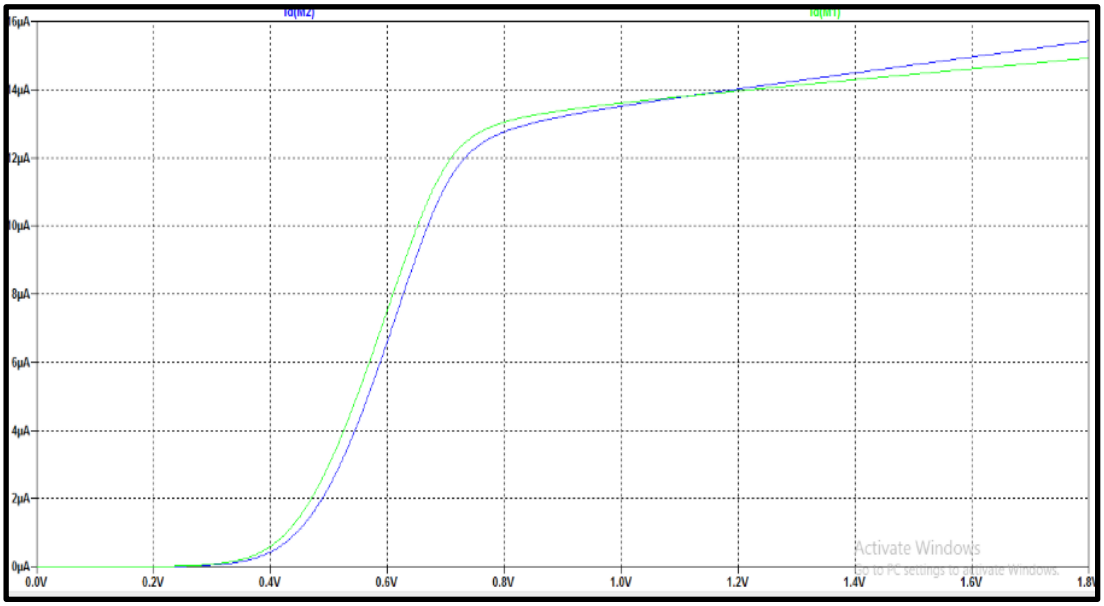


FIG 3.5 output for Long Channel Design

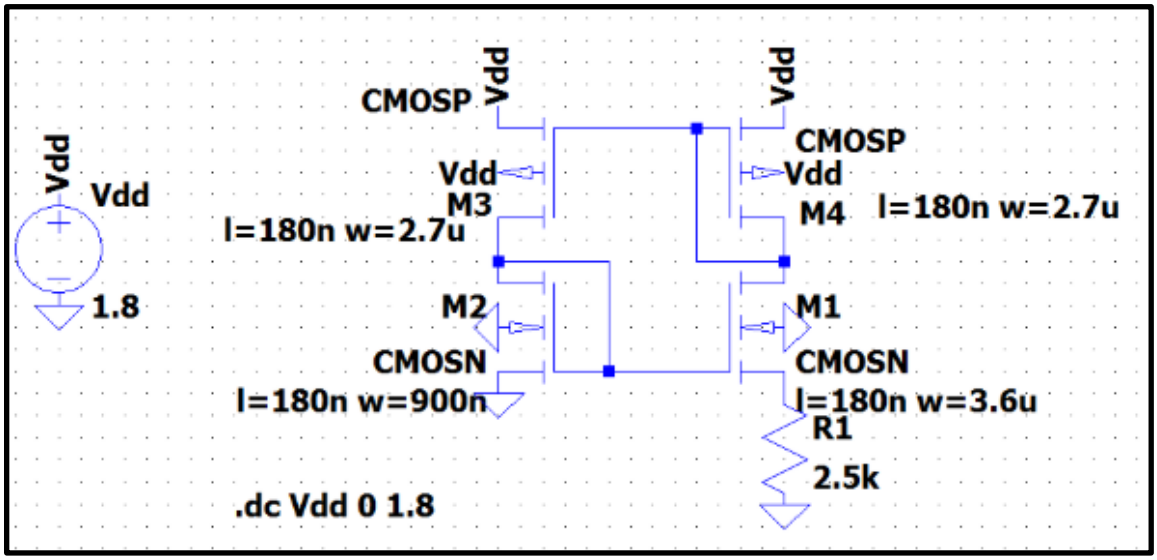


FIG 3.6 Short Channel Design

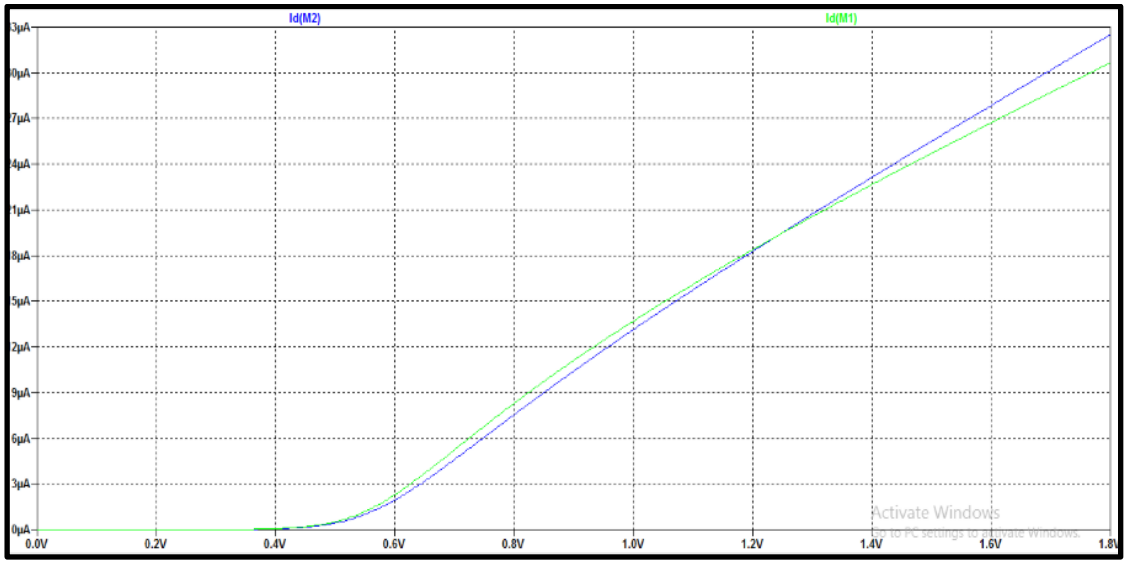


FIG 3.7 Output for Short Channel Design

For the short channel design above, it is observed that the output current varies significantly with the drain to source voltage, even when it is in saturation. This is because of the low output resistance associated with short channel devices. This output resistance can be increased by using a voltage controlled voltage source(VCVS) which thereby reduces the variations in VDS of NMOS devices with supply VDD as shown in the next section.

IMPROVED CURRENT REFERENCE FOR SHORT CHANNEL DEVICES

Fig shows a VCVS, with one of the inputs tied to the drain of M4 and output tied to the gate of M4, thus no longer keeping it diode connected.

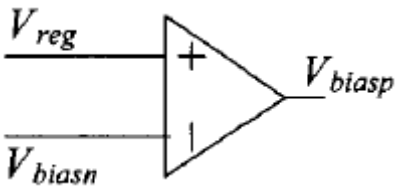


FIG 3.8

Input Vreg is tied to the drain of M4 and input Vbiasn is tied to the drain of M3. Output Vbiasp is tied to the gate of M4. The idea behind this approach is to compare the drain voltages of M1 and M2, and regulate them to make them equal. Since M2 is already diode connected and the gates of M1 and M2 are at the same potential, hence the drain potential of M1(Vreg) follows the drain potential of M2(Vbiasn) thus making it independent of supply voltage variations thereby increasing M1's effective output resistance.

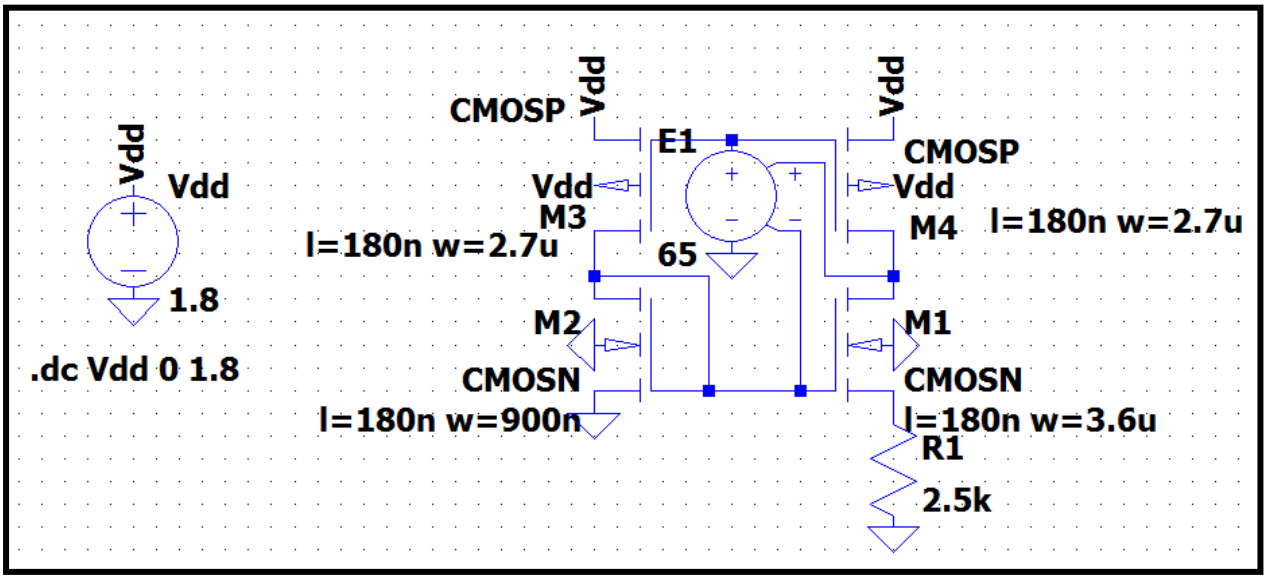


FIG 3.9 Improved Current reference using ideal VCVS

Suppose Vreg becomes greater than Vbiasn, resulting in an increased output Vbiasp. Therefore the gate potential of M4 increases, as a result of which current through M4 decreases and Vreg drops. Again, gate potential of M3 increases causing it to source less current and Vbiasn decreases. Due to symmetry, the reverse action takes place when Vbiasn rises over Vreg.

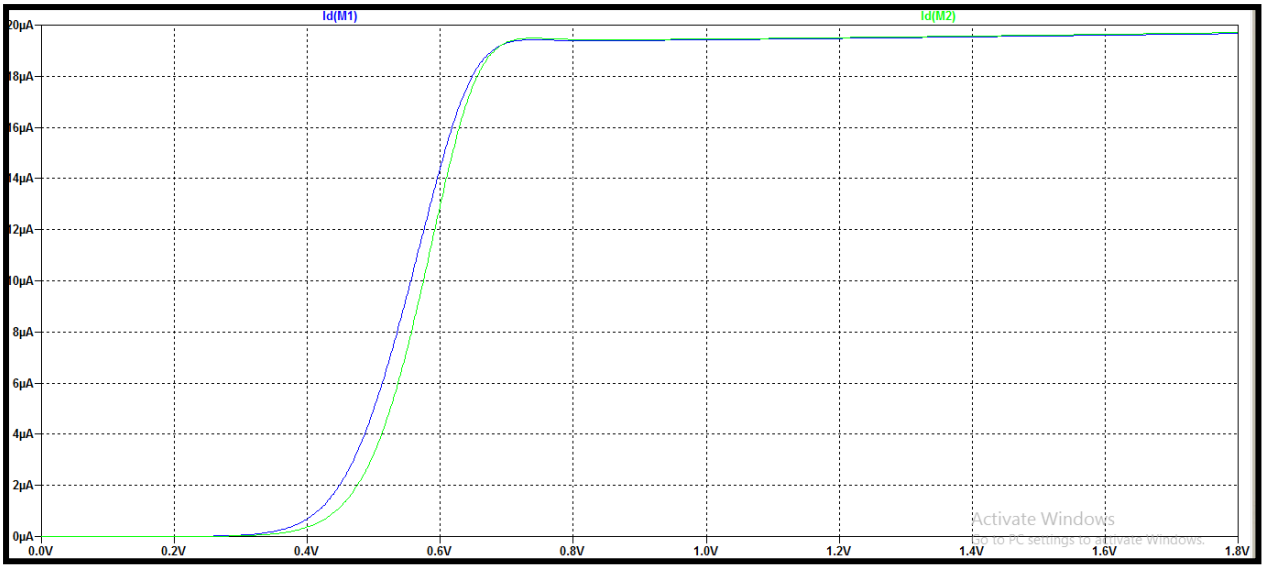


FIG 3.10 Improved BMR output (short channel) using ideal VCVS

An implementation of the VCVS using a differential amplifier is shown below. When Vbiasn = Vreg, the basic current mirror action takes place whereas, when Vbiasn ≠ Vreg, then the imbalance causes the amplifier output to swing up and down thus performing the desired action.

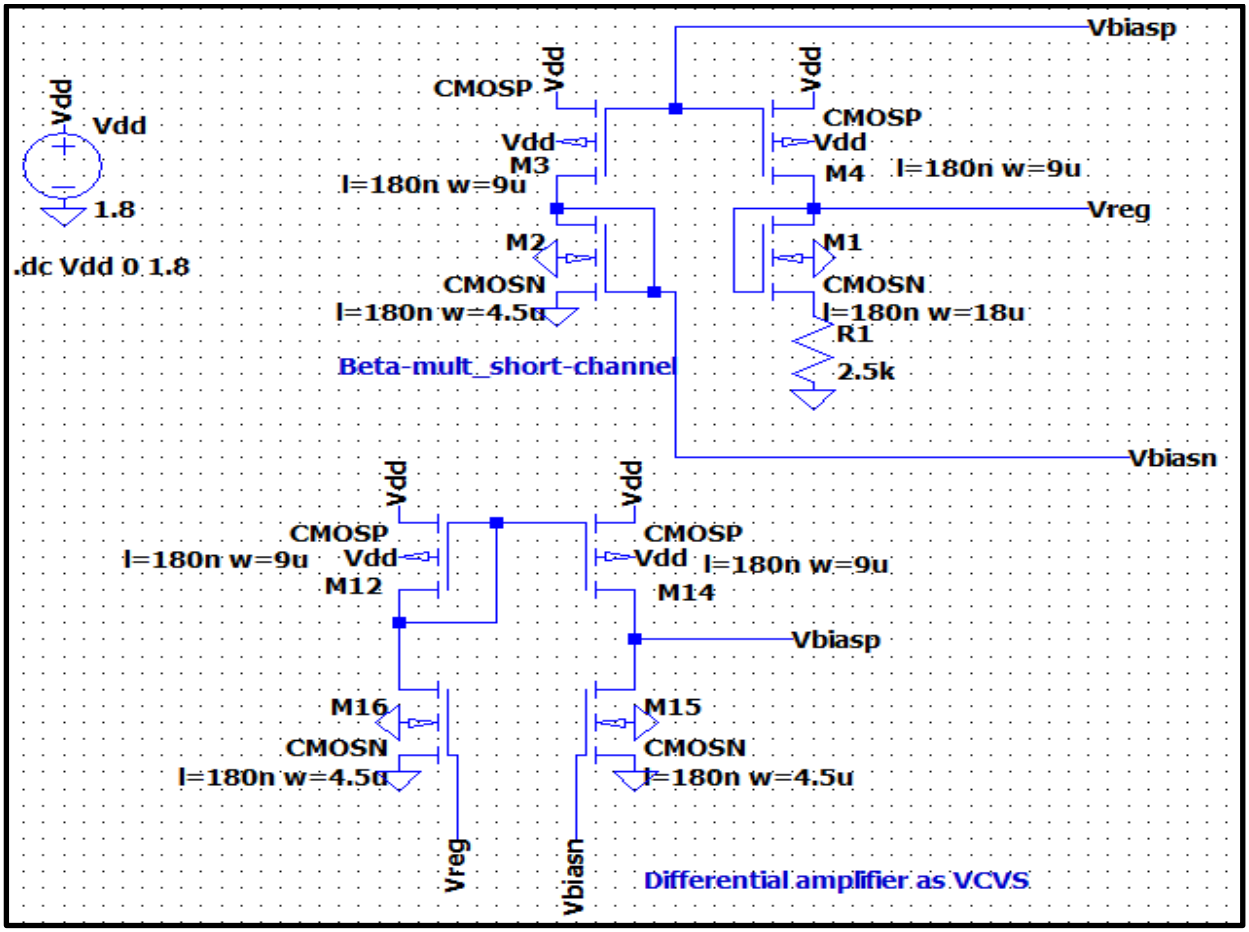


FIG 3.11 Implementing VCVS using differential amplifier

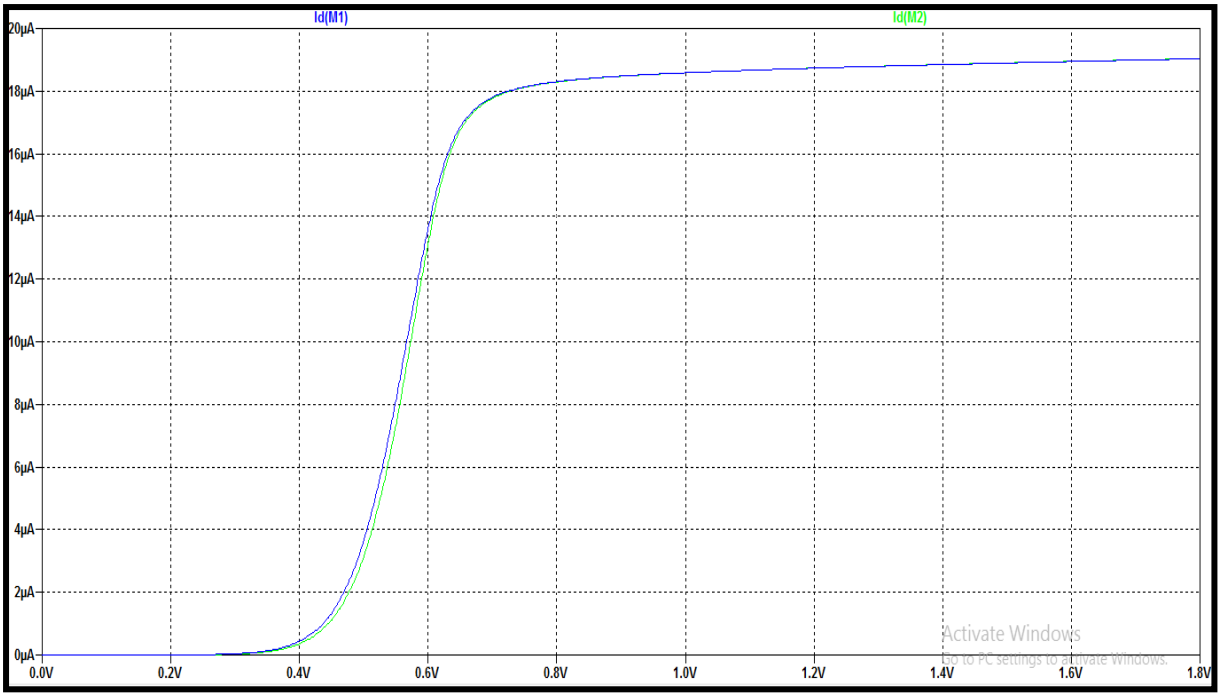


FIG 3.12 Improved BMR output (short channel) using diff-amp VCVS

CASCODING THE CURRENT MIRROR

In this section, the main objective is to increase the output resistance of current mirror so that it behaves more or less like an ideal current source. This is done by holding the drain to source voltages of the MOSFETs relatively constant. The basic cascode design of a current mirror is shown below.

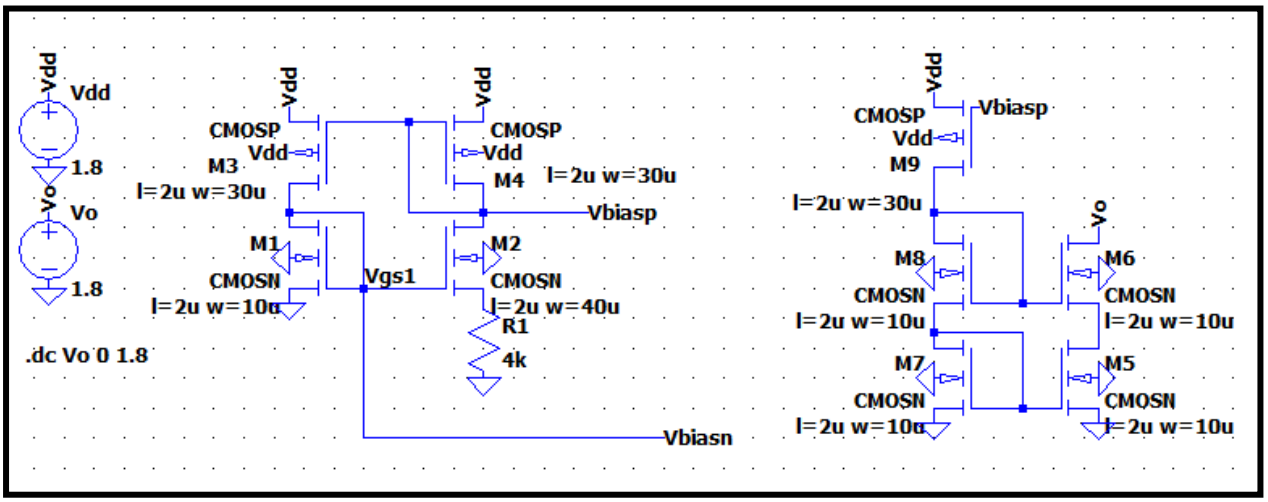


FIG 3.13 Basic Cascode Design

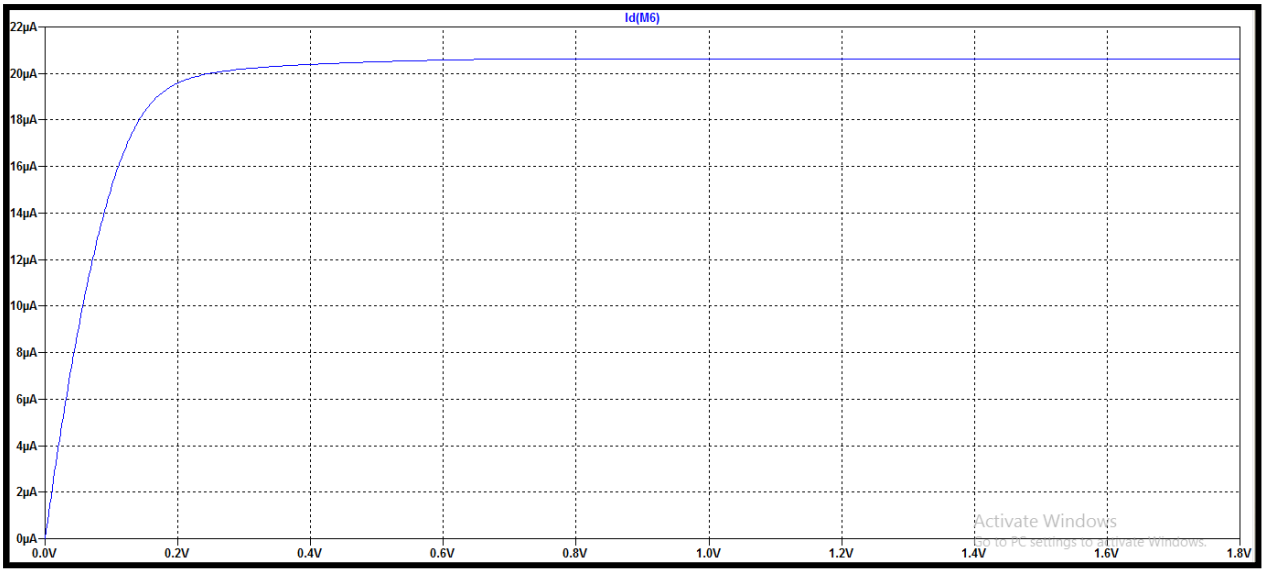


FIG 3.14 Output of the Basic Cascode Design

DC Operation:

Let VGS7 = VGS8 = VGS. Therefore, VGS5 = VGS6 = VGS.

Since, M7 and M8 are diode connected,

VD8 = VG8 = VGS + VDS7 = VGS + VGS7 = 2VGS.

This implies that VG6 is also at 2VGS as gates of M6 and M8 are connected together.

Therefore, VDS5 = VG6 – VGS6 = 2VGS – VGS = VGS.

Hence, it has been established that both VDS7 and VDS5 are at the same potential (VGS).

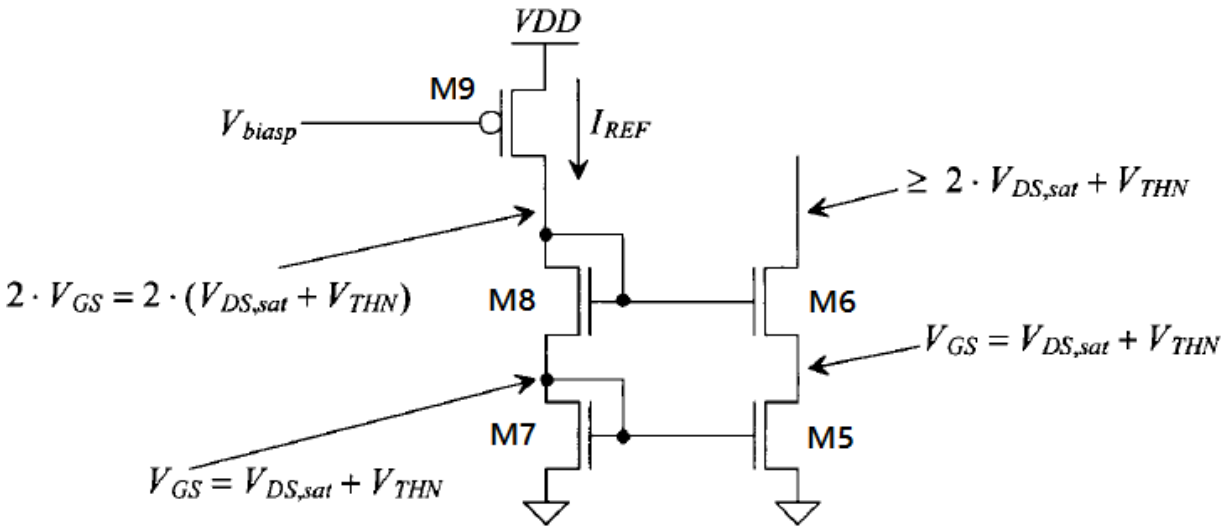


FIG 3.15 Regular Cascode Structure

To keep M6 in saturation, the minimum voltage drop required across M6 is VDSsat. Therefore, the minimum drain potential of M6 has to be (VDSsat + VGS) i.e. (2VDSsat + V_{THN}).

However, in order to keep M5 in saturation, only a drop of VDSsat will suffice. This will lower the minimum M6 drain potential to 2VDSsat. This design is called wide-swing or low-voltage cascode current mirror as discussed in the next section.

Cascode Output Resistance:

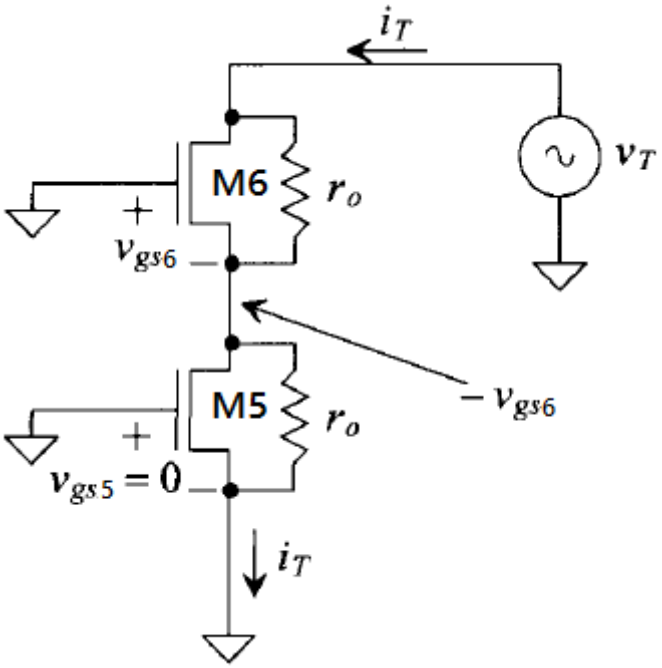


FIG 3.16 Small Signal AC Model of Basic Cascode

FIG 3.16 shows the small signal AC model for calculating the output resistance of the cascode structure.

$$-v_{gs6} = i_T \cdot r_o$$

Current through M6 is then

$$i_T = g_m v_{gs6} + [v_T - (-v_{gs6})]/r_o$$

Substituting the value of vgs6 we get,

$$i_T = g_m(-i_T \cdot r_o) + v_T/r_o - i_T$$

Solving for the output resistance,

$$R_o = (2 + g_m r_o) r_o = g_m r_o^2.$$

Thus, it can be concluded that output resistance of a cascode is significantly higher.

WIDE SWING CASCODE

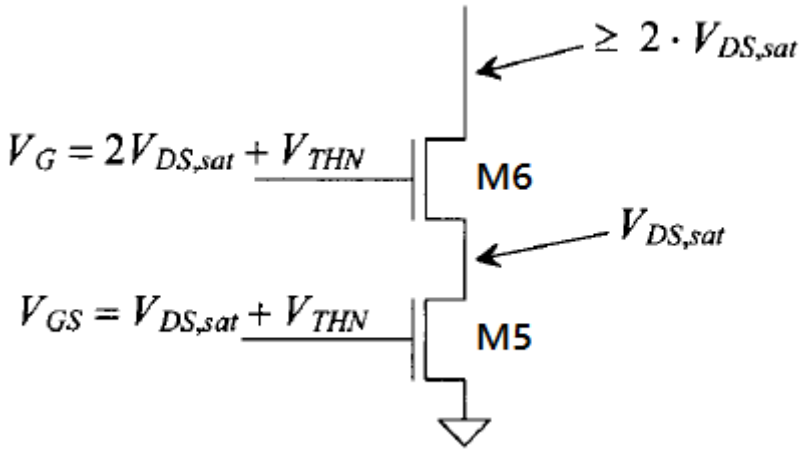


FIG 3.17 Low-Voltage (aka wide-swing) structure

For a drop of VDSsat across M5, the gate voltages of M5 and M6 are generated using two separate diode connected MOSFETs biased by the same voltage reference.

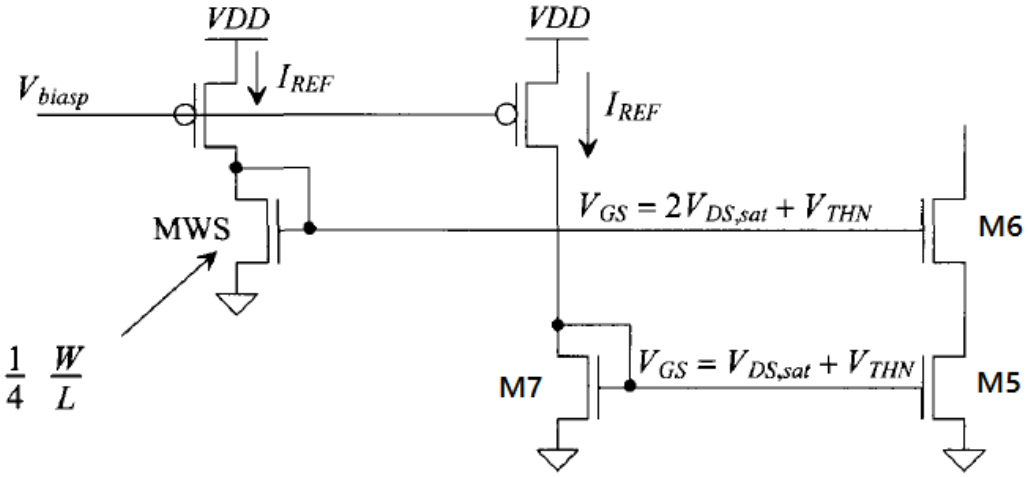


FIG 3.18 Generating bias voltages for M5 and M6

For M7,

IREF = k/2 W/L $(VGS - VTHN)^2$ ....neglecting channel length modulation -(1)

For MWS,

IREF = k/2 W_{ws}/L_{ws} $(VGS_{ws} - VTHN)^2$ ....neglecting channel length modulation

or, IREF = k/2 W_{ws}/L_{ws} $(2VDSsat + VTHN - VTHN)^2$

or, IREF = k/2 W_{ws}/L_{ws} $[2(VGS - VTHN) + VTHN - VTHN]^2$

or, IREF = k/2 W_{ws}/L_{ws} $4(VGS - VTHN)^2$ -(2)

From (1) and (2),

W/L = 4 W_{ws}/L_{ws}

WIDE SWING SHORT CHANNEL DESIGN

In short channel devices,

$$VDSsat \neq VGS - VTHN = Vovn$$

The output resistance of a short channel MOSFET depends on its drain to source voltage. To increase the output resistance, M7(FIG 3.19) is biased deeper into the saturation region by increasing the gate voltage of M8(FIG 3.19). This is done by using a smaller ratio(say 5 times) than that used for long channel devices.

Therefore, W_{ws}/L_{ws} = 1/25 W/L

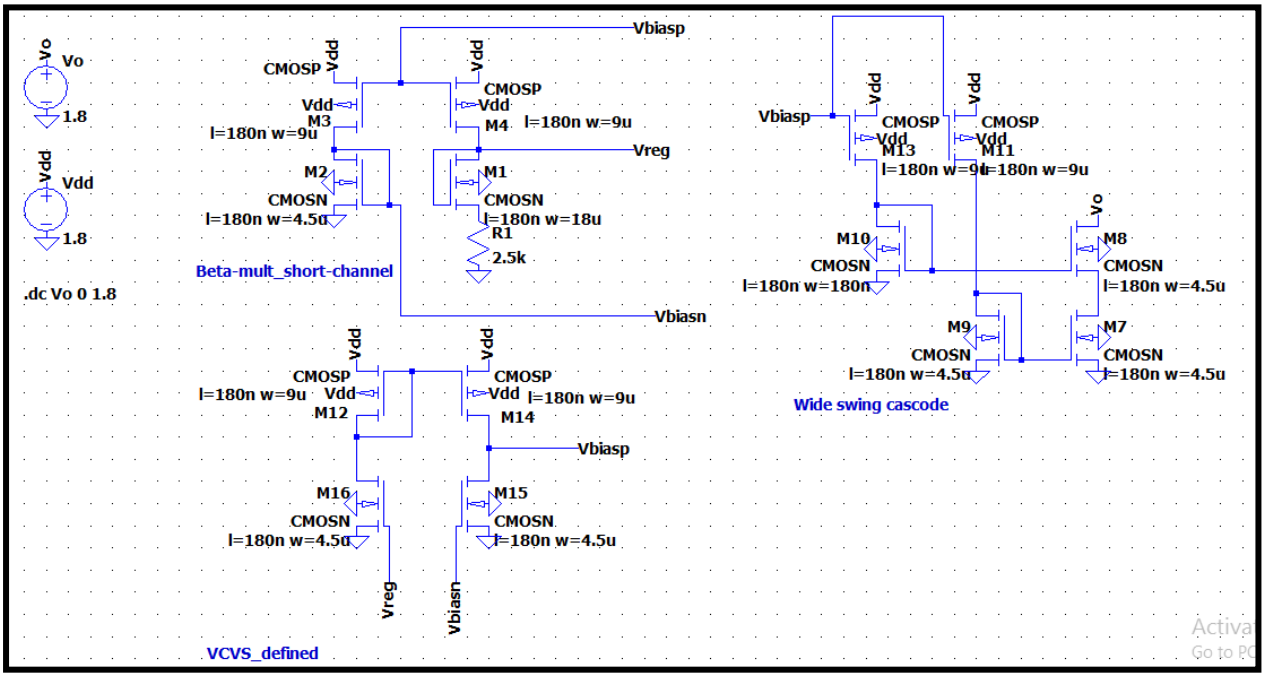


FIG 3.19 Wide Swing Cascode Short Channel Design

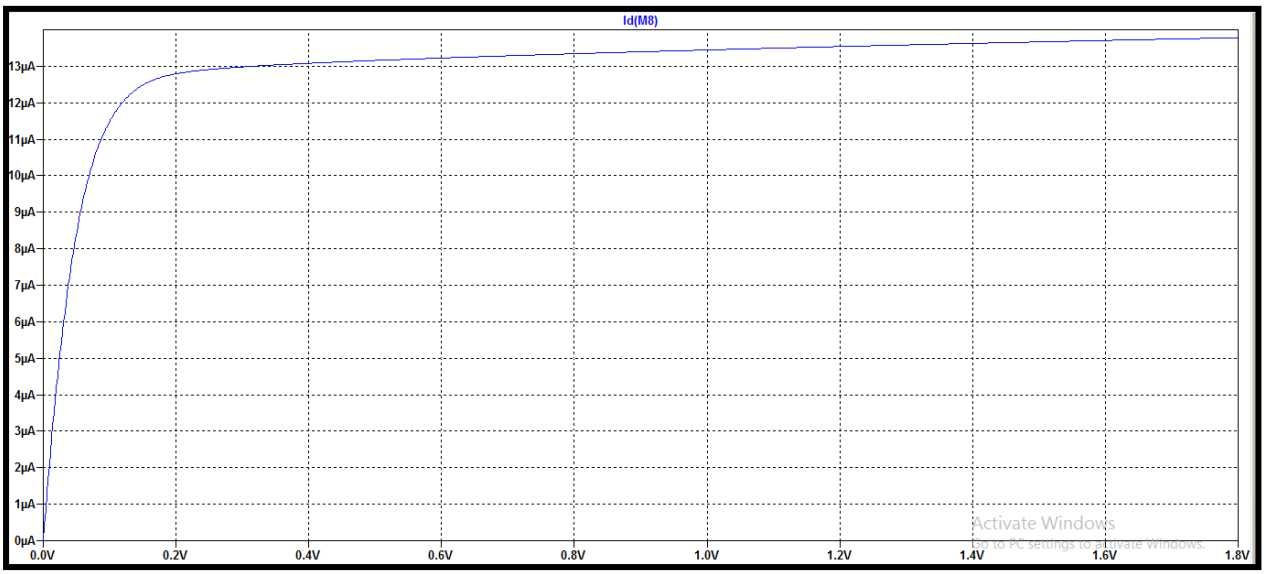


FIG 3.20 Wide Swing Cascode Current Mirror Output

However, in the above design, due to mismatch in the drain to source voltages of M7 and M9, the 20µA current could not be mirrored accurately. To rectify this, an added device, M17(FIG 3.21) is used to lower the VDS of M9 and appropriately match it to the VDS of M7.

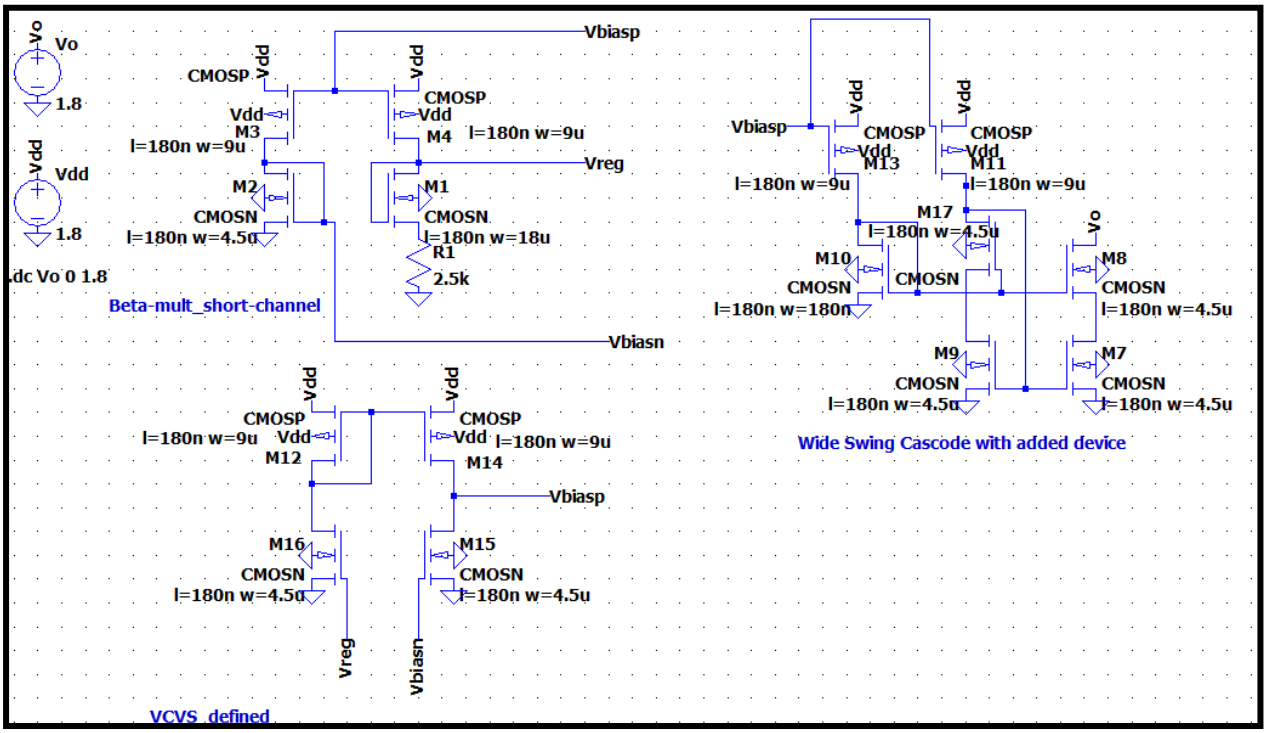


FIG 3.21 Wide Swing Cascode Short Channel Design with Added Device

For the above figure, gate of M9 is connected to drain of M17. Therefore, V_D(M17) = V_{GS}. Since, drop across M9 is V_{DSsat}, therefore, V_{DS}(M17) = V_{GS} - V_{Dssat} = V_{THN}.

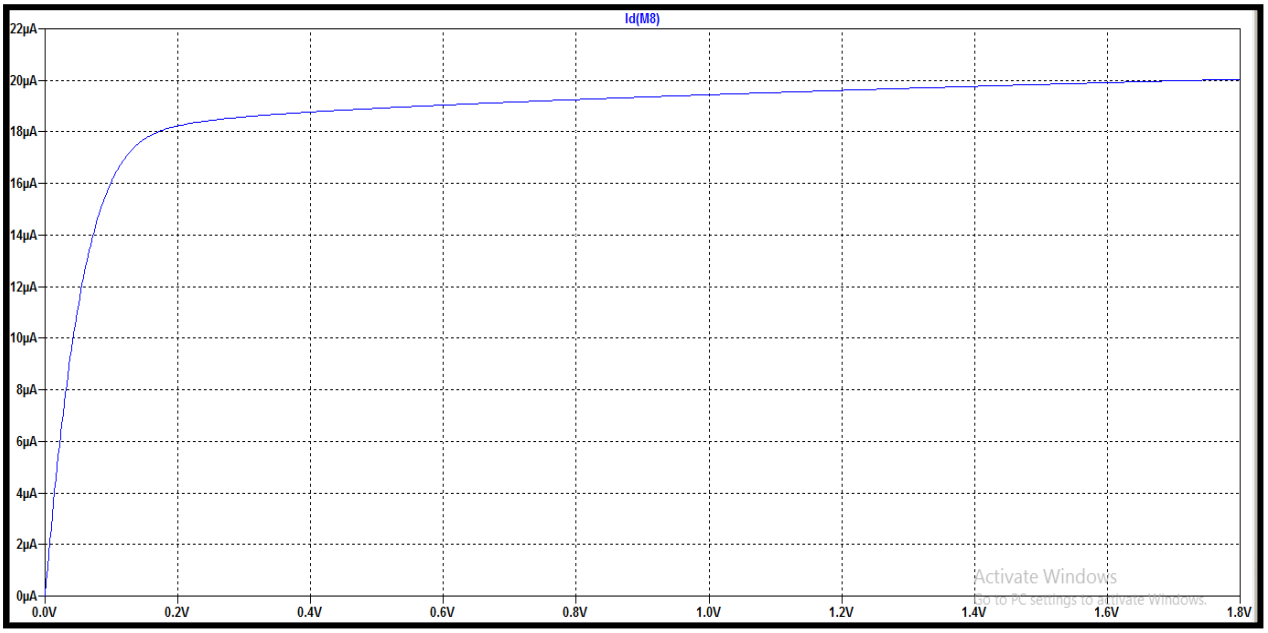


FIG 3.22 Wide Swing Cascode Current Mirror Output with Added Device

START-UP CIRCUIT

In any self-biased circuit, there are two possible operating points: One is the stable desired operating point and the other is the unwanted operating point where zero current flows through the circuit. If current through the beta-multiplier reference, I_{REF} is 0, then V_D(of M2) = 0 and V_D(of M4) = VDD. But in reality, some leakage current flows through M2, thereby pulling up the drain voltage of M2 slightly above 0. When this current gets mirrored in M1 and flows through M4, it lowers the drain voltage of M4 a little bit below VDD. Since, V_G(of M4) = V_D(of M4), this again causes some additional current to flow through M3 and M2 thus, rising V_D(of M2) futher above 0. This process goes on and on till it reaches the stable wanted operating state.

So, the BMR circuit consumes a lot of unnecessary power, problem addressed by use of 'Start-Up Circuit' shown below in FIG 3.23.

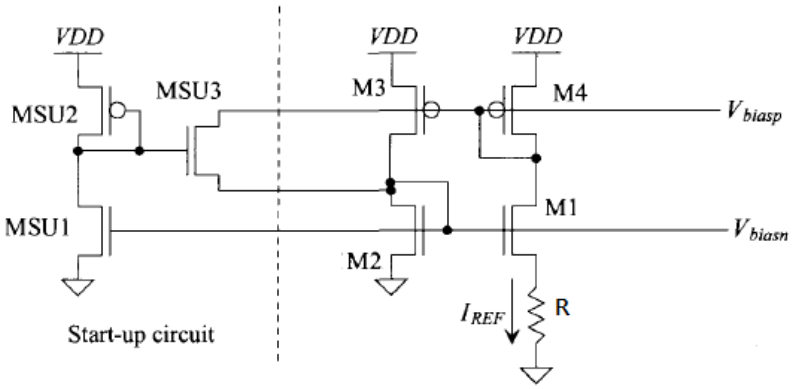


FIG 3.23 BMR with Start-Up Circuit

When BMR is in the undesired state, the gate of MSU1 is at ground and it is OFF. Therefore, the gates of MSU2 and MSU3, somewhere between VDD and VDD - |VTHP| drives the NMOS MSU3 into saturation, thereby injecting current into the gate of M2 which in turn again gets mirrored in M1, thereby snapping the BMR into its desired operating state again.

REGULATED DRAIN CURRENT MIRROR

The output resistance of wide swing cascode current mirror can be increased further by adding an amplifier to hold the drain of M7(FIG 3.23) at a more fixed potential.

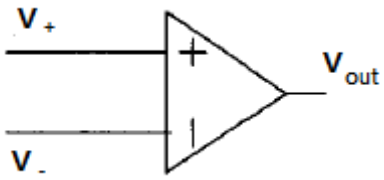


FIG 3.24

In FIG 3.24, v_{out} is connected to the gate of the MOSFET M8, with one of the inputs v_- tied to the drain of M7 and the other, v_+ tied to the drain of M9.

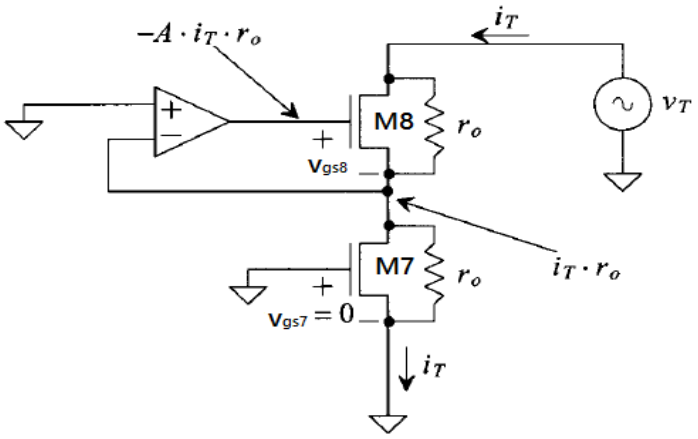


FIG 3.25 Determining Output Resistance of Regulated Drain Current Mirror

From FIG 3.25,

$v_{out} = A\ (v_+ - v_-)$ .....where A is the gain of the amplifier

$vgs8 = -iT.ro\ (A + 1)$

and,

$$iT = gm(-iT.ro\ (A + 1)) + (vT - iT.ro)/ro$$

and finally,

$$Ro = vT/iT = 2ro + gm.ro^2(A + 1) \approx gm.ro^2.A$$

A practical implementation of the amplifier using MOSFETs has been shown in FIG 3.25. The MOSFETs M17 and M18 hold the drain potentials of M9 and M7 respectively at VGS. If the drain voltage of M7 starts to decrease, the MOSFET M18 starts being driven into cut-off thereby increasing its drain potential and hence, M8's gate potential thus pulling back up the drain potential of M7. Due to symmetry in the design, the same action occurs for the combination of the MOSFETs M9, M10 and M18.

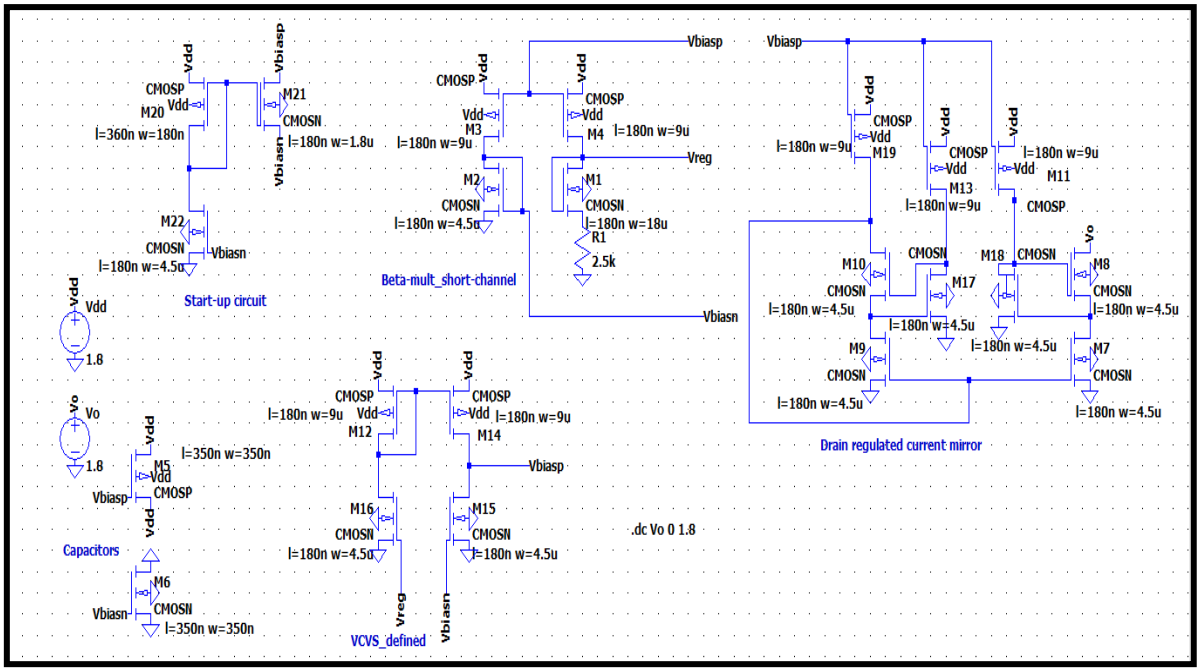


FIG 3.26 Using Amplifier to regulate drain potential

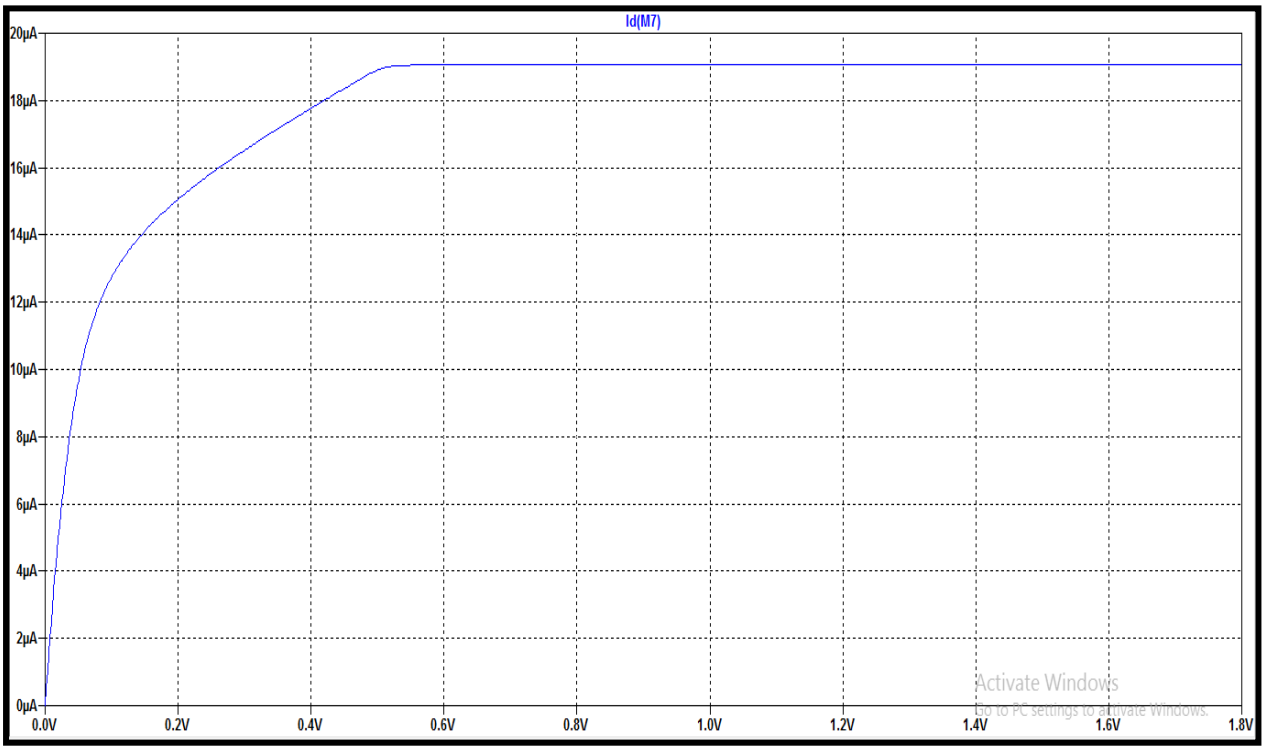


FIG 3.27 Output for Drain Regulated Current Mirror

BIASING CIRCUITS

FIG 3.28 shows the biasing circuit for a current sink where VGS1 and VGS2 are the generated bias voltages used to drive the mirrored current through the NMOS transistors M7 and M8 in FIG 3.29.

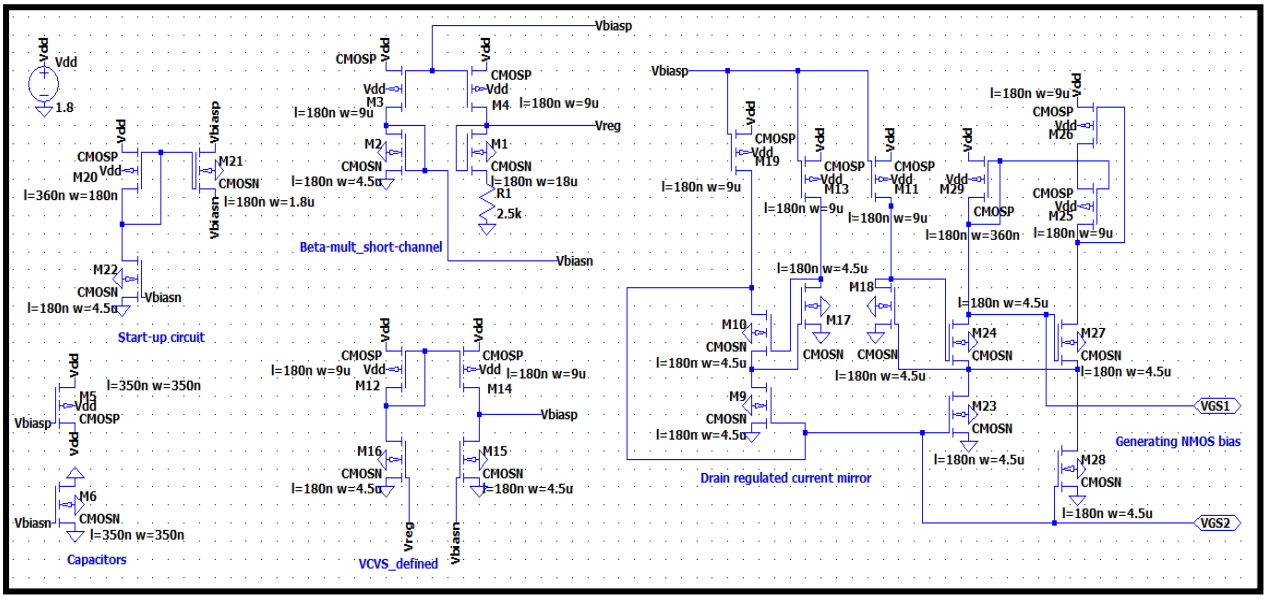


FIG 3.28 Biasing Circuit for Current Sink

- VGS1 = 1.08V
- VGS2 = 0.53V
- I_o = 18.42µA

To keep the current sink in saturation, the minimum reference voltage V_o required is approximately 0.6V as is evident from FIG 3.30.

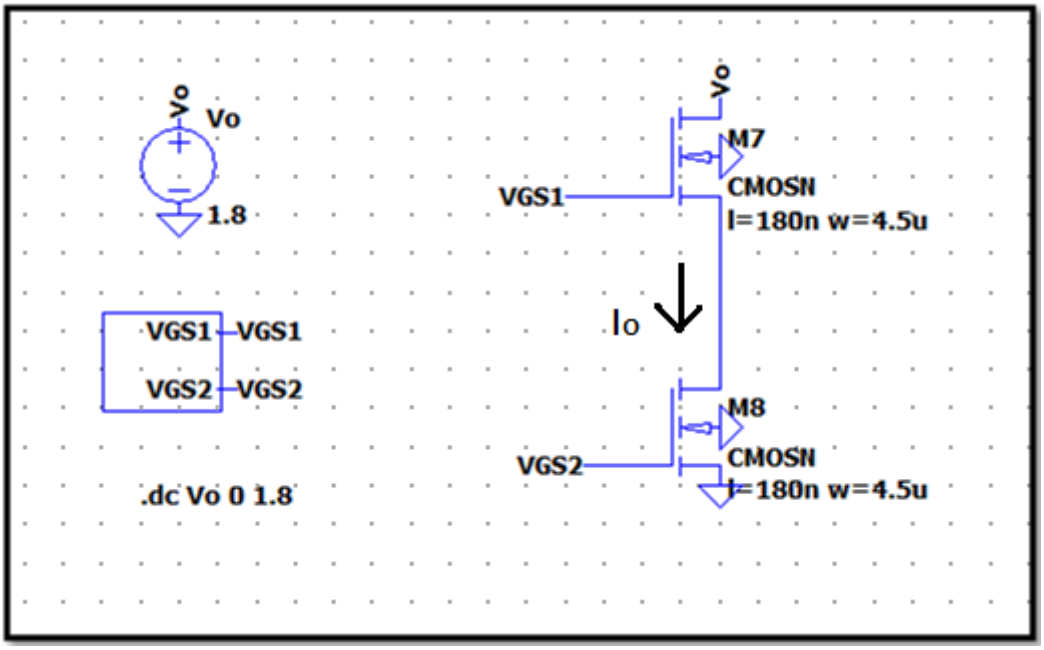


FIG 3.29 Current Sink

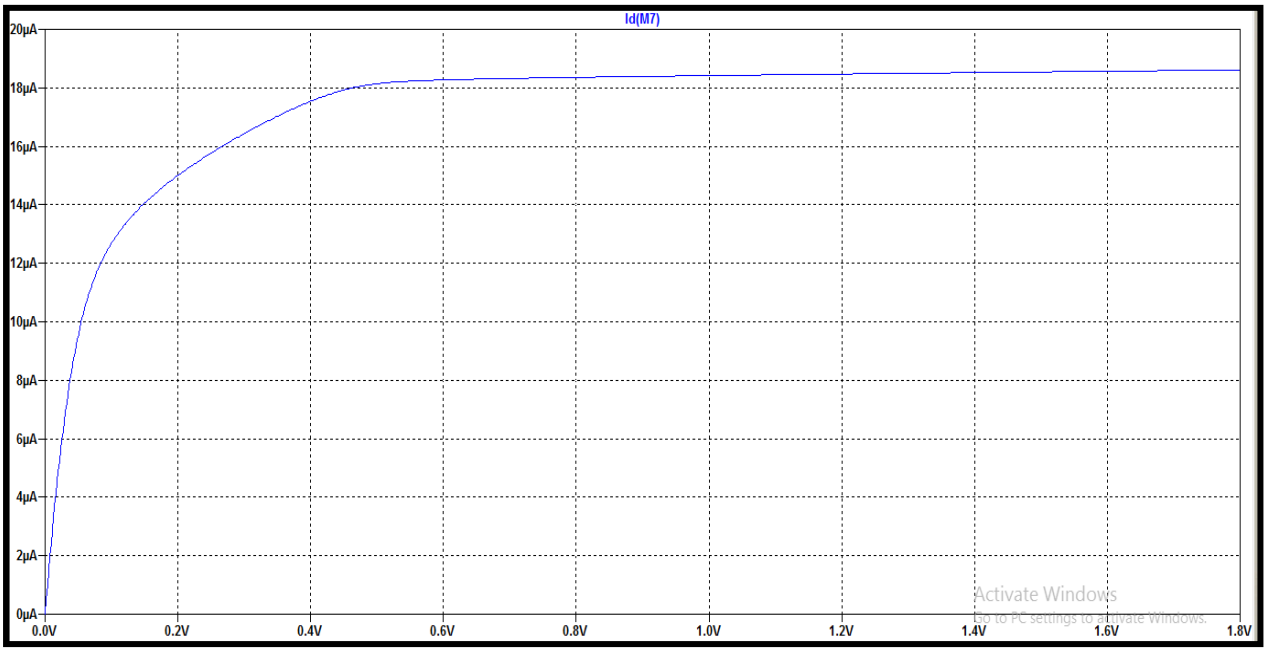


FIG 3.30 Current Sink Output

FIG 3.31 shows the biasing circuit for a current source where VSG1 and VSG2 are the generated bias voltages used to drive the mirrored current through the PMOS transistors M8 and M7 in FIG 3.32.

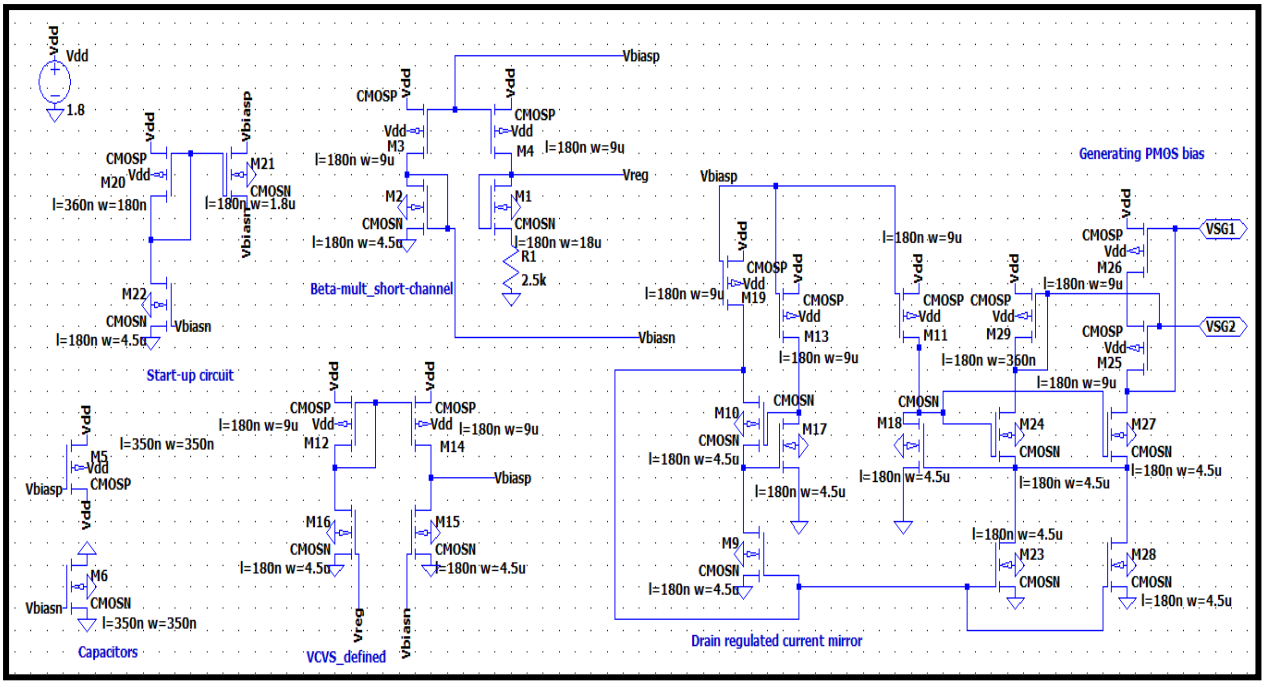


FIG 3.31 Biasing Circuit for Current Source

- VSG1 = 1.23V
- VSG2 = 0.88V
- I_o = 21.58µA

To keep the current source in saturation, the maximum reference voltage V_o possible is approximately 1.4V as is evident from FIG 3.33.

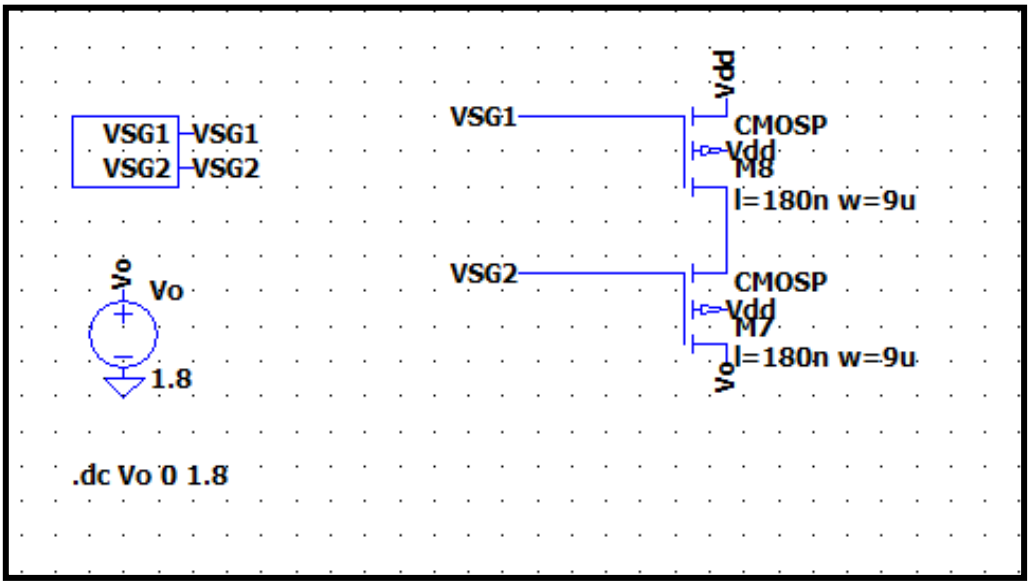


FIG 3.32 Current Source

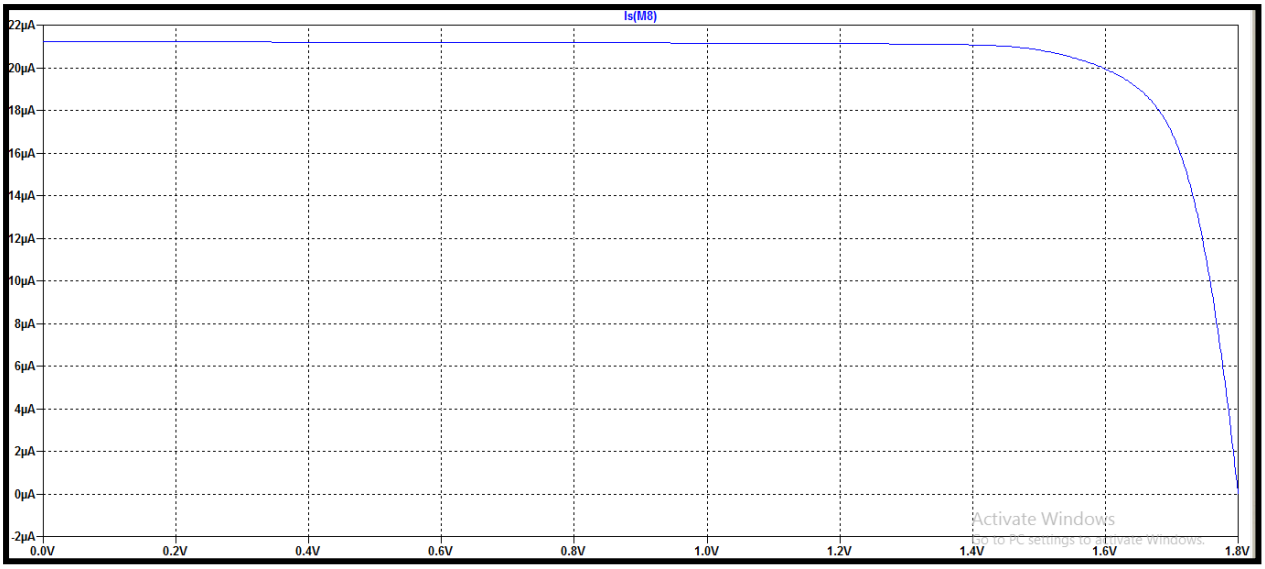


FIG 3.33 Current Source Output

CHAPTER 4

CMOS INVERTER AND SWITCHES

In this section, the design and working of CMOS inverter and switches are discussed in detail.

CMOS INVERTER

FIG 4.1 shows the design of a CMOS inverter, where Vin is the input and Vout is the output. Vdd and DGND represent analog source and ground respectively.

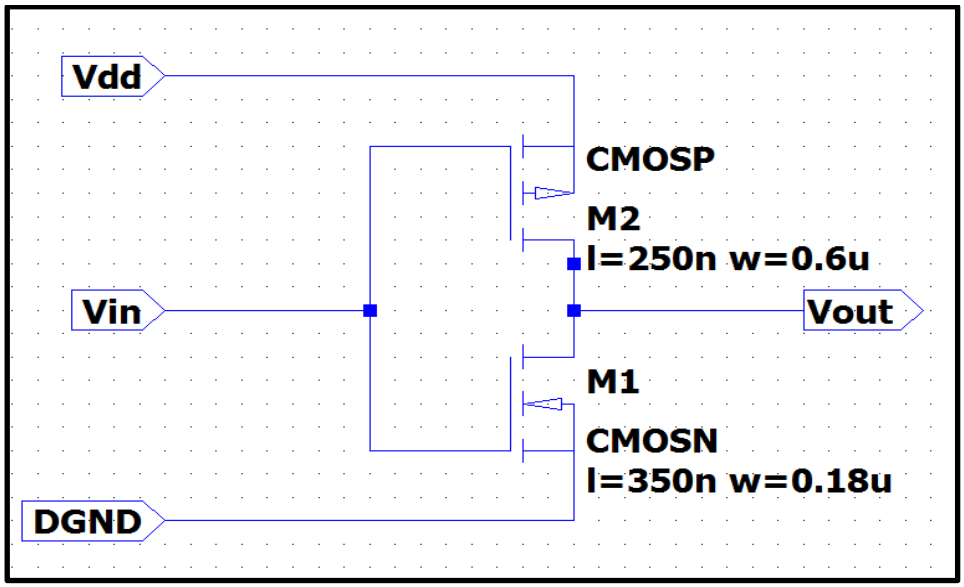


FIG 4.1 CMOS Inverter

When the input Vin is 0, the NMOS transistor M1 is OFF and the PMOS M2 transistor is ON. Thus, the output Vout is pulled up to 1 because it is connected to Vdd but not to DGND. Conversely, when Vin is 1, the NMOS is ON, the PMOS is OFF, and Vout is pulled down to '0.'

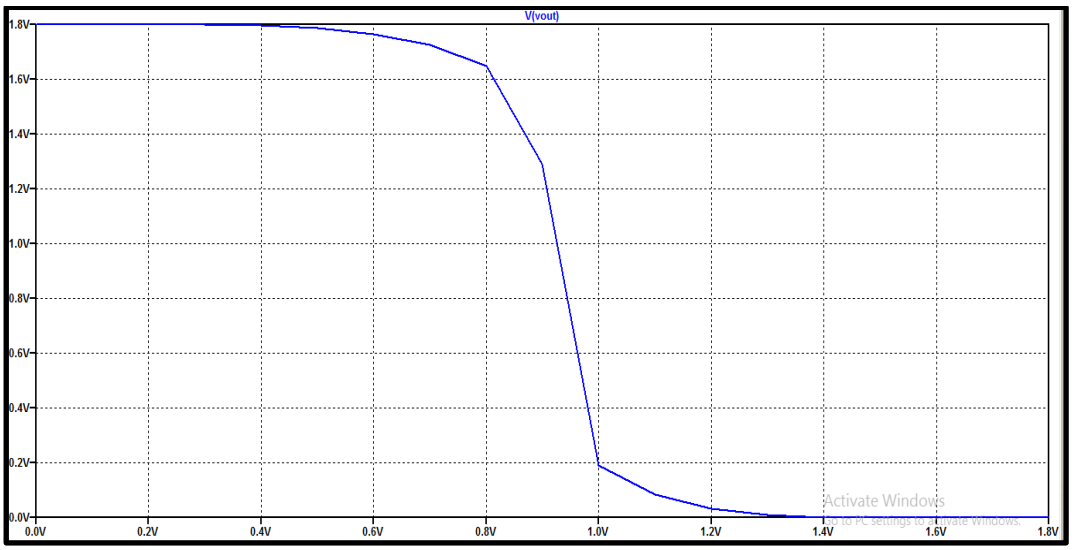


FIG 4.2 Inverter Action

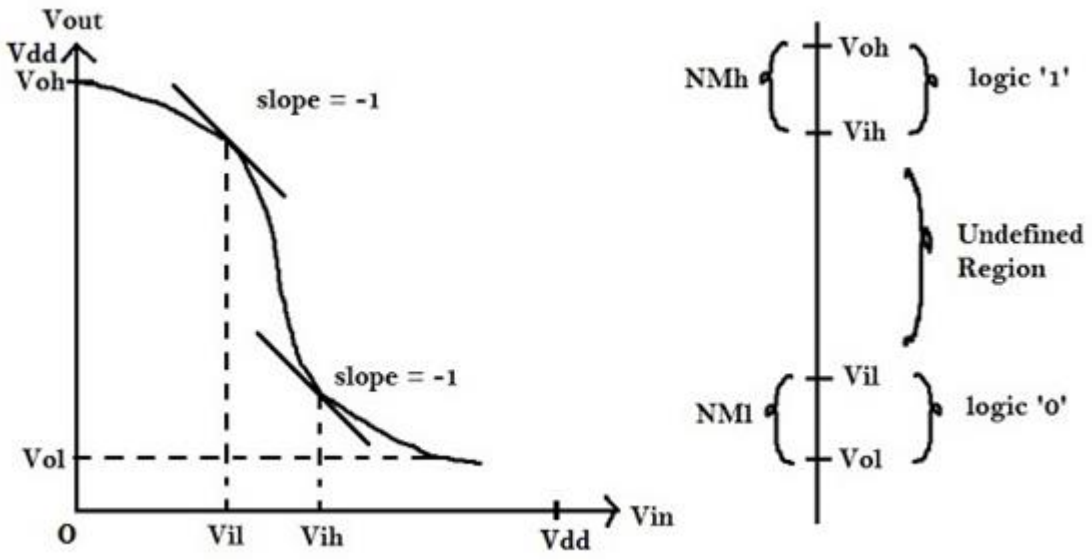


FIG 4.3 Calculating Noise Margins

By definition, Vih and Vil are the operational points of the inverter where slope = -1. These are points where the gain of the amplifier, formed by the inverter, is equal to -1.

Noise margins are defined as follows:

NMl (Noise Margin Low) = Vil – Vol

NMh (Noise margin High) = Voh – Vih

We have seen that for βp = βn, the inverter threshold voltage Vinv is VDD/2. This may be desirable because it maximizes noise margins and allows a capacitive load to charge and discharge in equal times by providing equal current source and sink capabilities. Now, since mobility of NMOS, μ_n is higher than that of PMOS μ_p, the W/L ratio of the PMOS transistor is to be kept higher.

SWITCHES

A switch is a network, consisting of two or more input ports, and one output port. Depending on the input applied at the switch terminal, any one of the inputs is shorted to the output.

VOLTAGE SWITCH

Since the switching action, as mentioned above is analogous to the working of a digital Nx1 multiplexer, a voltage switch has been designed in this section based on digital logic, using CMOS technology.

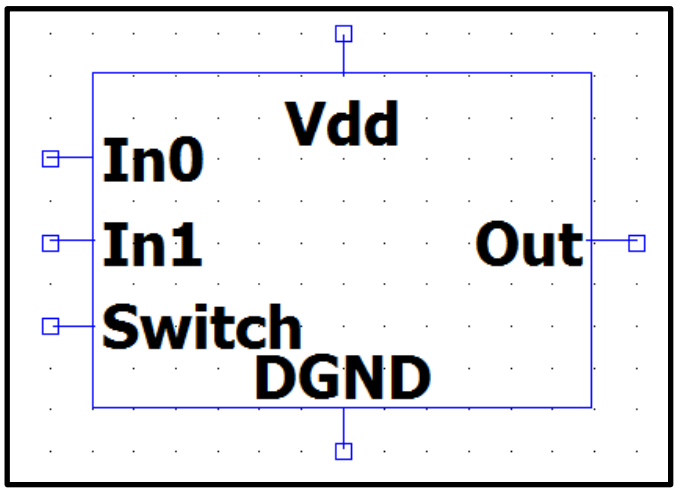


FIG 4.4 Voltage Switch

FIG 4.4 shows a 2x1 voltage switch, where 'In0' and 'In1' are the input lines, 'Out' is the output line, and 'Switch' is the address line. 'Vdd' and 'DGND' represent the analog source and ground respectively. If 'Switch' is high(logic '1'), input at 'In1' is transferred to 'Out' and if 'Switch' is low(logic '0'), input at 'In0' is transferred to 'Out'.

Truth Table:

Switch	Out
0	In0
1	In1

Therefore, Out = (Switch)'.(In0) + (Switch).(In1)

Based on the above equation, it is observed that AND gate, OR gate and Inverter is required to design the switch as shown below.

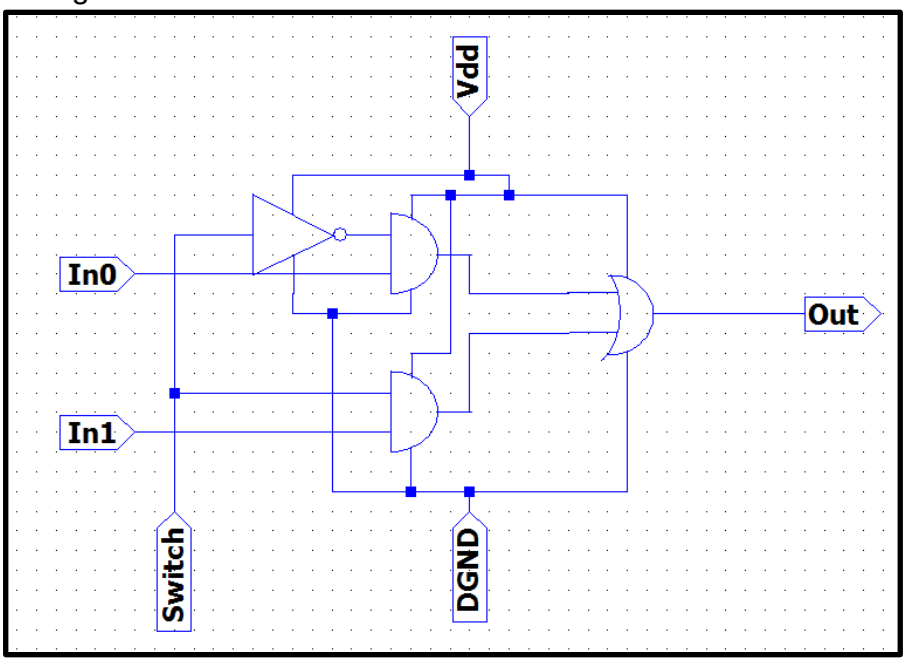


FIG 4.5 Logic Diagram of Voltage Switch

FIG 4.5 shows the logic diagram of the voltage switch. The AND and OR gates in FIG 4.5, have been designed using Inverter and NAND gates.

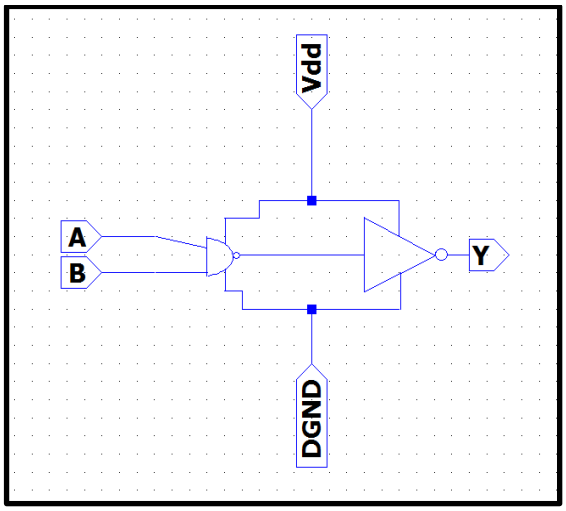


FIG 4.6 AND Gate Logic Diagram

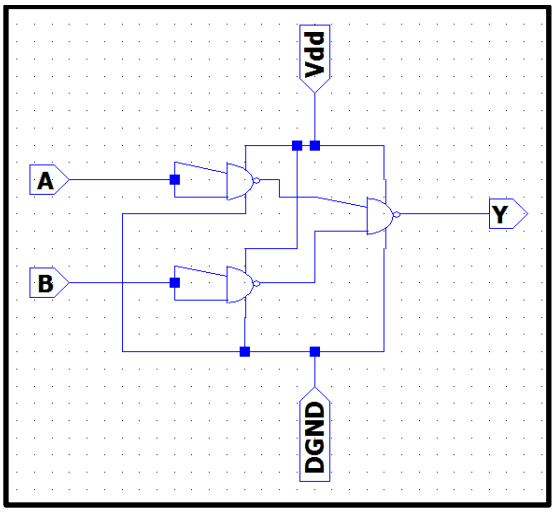


FIG 4.7 OR Gate Logic Diagram

The design of the inverter has already been discussed in this chapter previouly. The design of the NAND gate using CMOS technology is discussed in the following section.

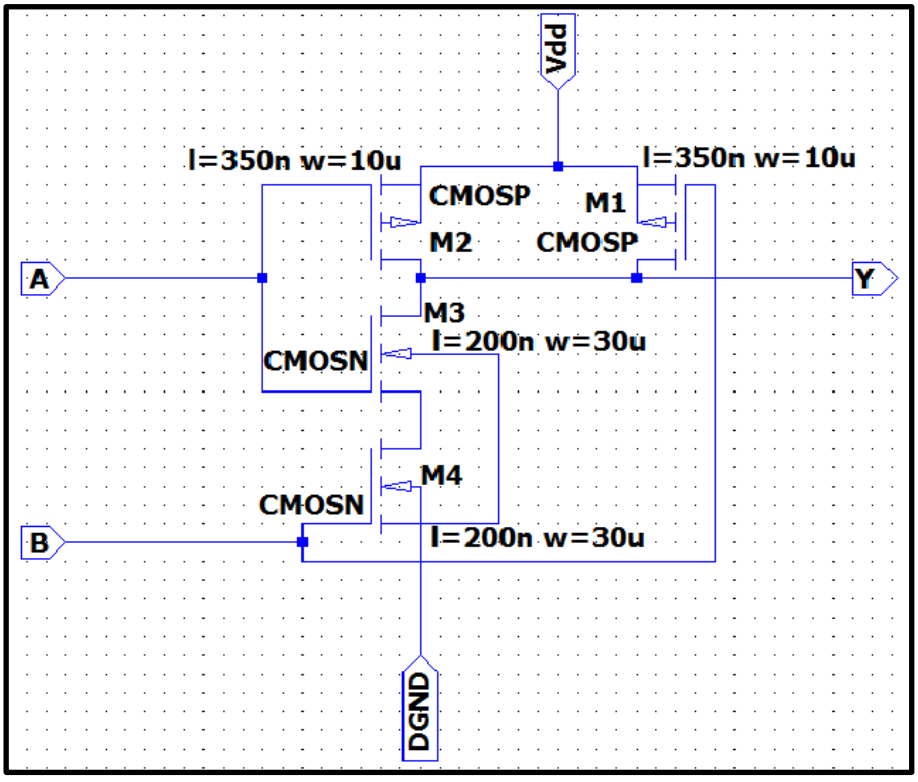


FIG 4.8 NAND Gate using CMOS

FIG 4.8 shows the design of a NAND gate using NMOS and PMOS transistors. When at least one of the inputs, A or B is low(logic '0'), the corresponding PMOS transistor, M2 or M1 turns ON and the output Y gets shorted to Vdd (logic '1'), while the corresponding NMOS transistor, M3 or M4 turns OFF. On the contrary, when

both A and B are high (logic ‘1’), both PMOS transistors turn OFF(open circuit), both NMOS transistors turn ON and output Y gets shorted to ground(logic ‘0’).

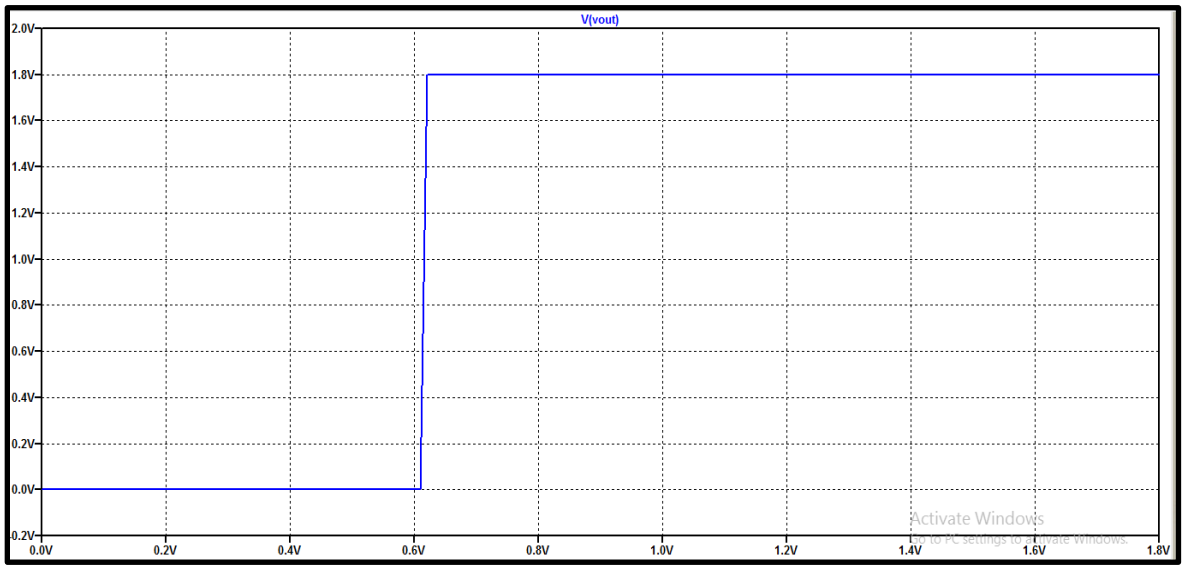


FIG 4.9 Response of the Voltage Switch

FIG 4.9 shows the response of the switch for input voltage ranging from 0 to 1.8V. The W/L ratios have been chosen carefully by simulation in order to improve the switching transient.

CURRENT SWITCHES

In the design of the current steering DAC architecture, current switches can be used to deliver the required amount of current to the load from the current source, depending on its digital input. If the current is to flow into the load, the current source should be connected to the load. When it is not connected to the load, there is a need for diverting this current to some other low resistive path in order to lower power dissipation, thus maintaining constant current supply from the current source.

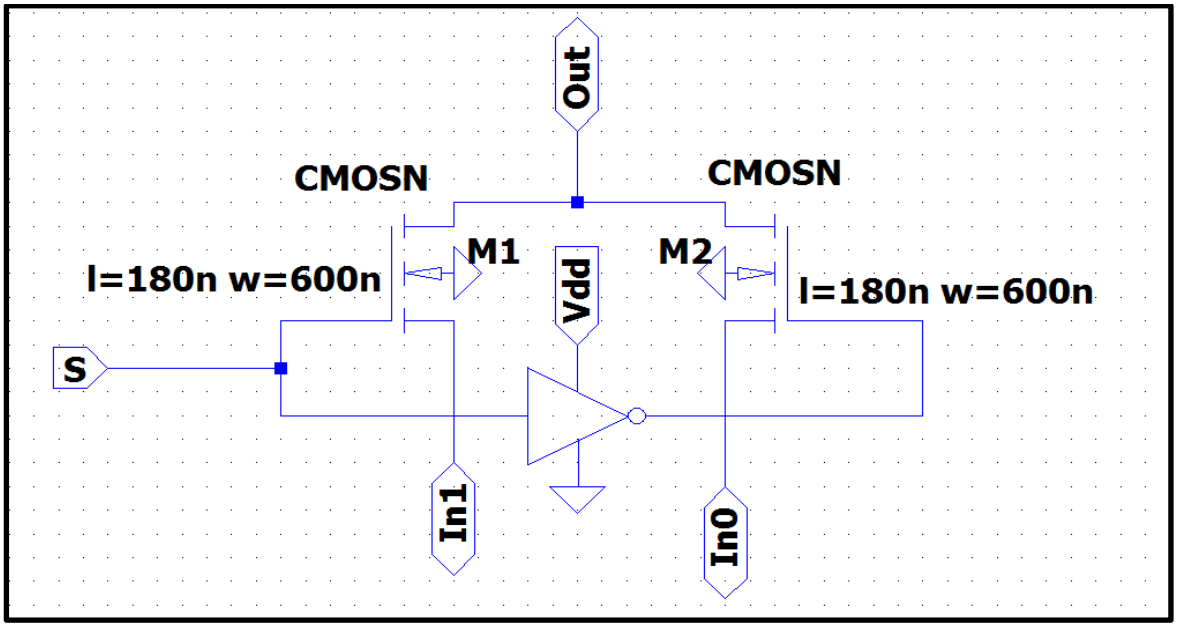


FIG 4.10 Current Switch

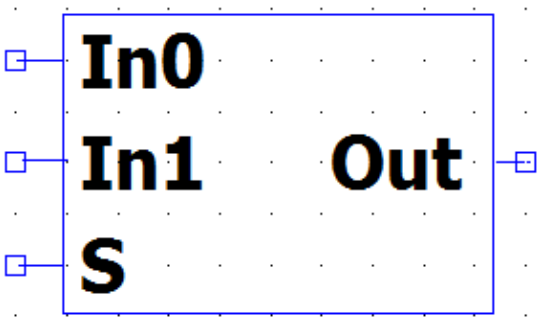


FIG 4.11 Symbol of Current Switch

FIG 4.11 shows a current switch built using 2 NMOS transistors M1 and M2, and a CMOS inverter. M1 connects the current source to the load whereas M2 connects it to ground. Depending on the input, the required amount of current is delivered to the load through M1, while the remaining current is diverted to ground via M2. If the input S is high,(logic '1'), transistor M1 is on and transistor M2 receives the complement of S(logic ‘0’), and is turned off, and vice versa.

The complement of S is derived by using a CMOS inverter as discussed in Section . This mode of switching is known as differential switching.

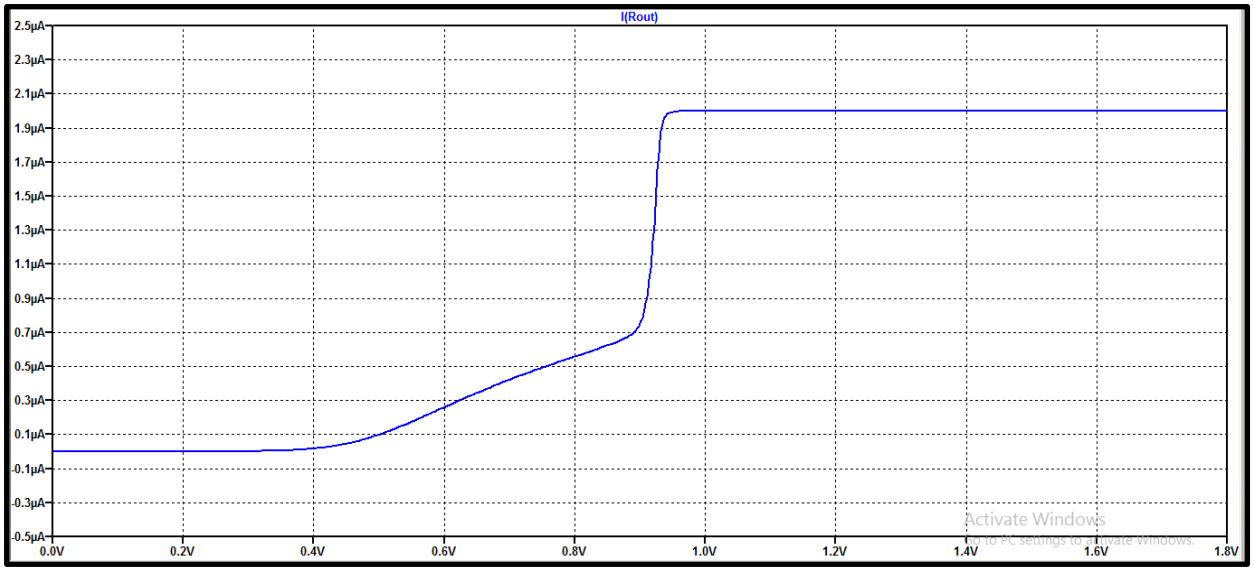


FIG 4.12 Response of the Current Switch

The widths of the transistors are kept to a minimal value so that the speed of switching can be improved. Since the larger width transistor has more gate-drain capacitance, it takes time for the switch to completely steer the current to either of the node. Hence, to decrease the internal capacitance of the transistor and improve the speed of switching, transistors with the width 600 nm are used.

CHAPTER 5

OPERATIONAL AMPLIFIER

NON-INVERTING OPAMP

The non-inverting configuration of an ideal Op-amp is shown below in FIG 5.1 .

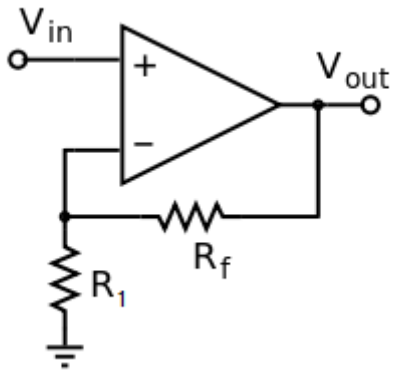


FIG 5.1 Op-amp as a Non-Inverting Amplifier

CALCULATING CLOSED LOOP GAIN

Let the open loop gain of the Op-amp be A_{OL}.

For FIG 5.1,

Voltage at the non-inverting terminal, $v_+ = Vin$

Since, voltage at the output terminal = Vout and input bias current flowing into the inverting terminal of the Op-amp, $i_{B-} = 0$, voltage at the inverting terminal, $v_- = \frac{R1}{(R1+Rf)}Vout$

Now, $Vout = A_{OL}(v_+ - v_-)$

or, $Vout = A_{OL}(Vin - \frac{R1}{(R1+Rf)}Vout)$

or, $(1 + A_{OL}\frac{R1}{(R1+Rf)})Vout = A_{OL}Vin$

or, $\frac{Vout}{Vin} = \frac{AOL}{(1 + AOL\frac{R1}{(R1+Rf)})}$

or, $A_{CL} = \frac{AOL}{(1 + AOL\frac{R1}{(R1+Rf)})}$

Since, A_{OL} of an Op-amp is very high (ideally infinite), $A_{CL} \approx \frac{1}{\frac{R1}{(R1+Rf)}} = 1 + \frac{Rf}{R1}$.

NON-INVERTING OPAMP AS AN ADDER

A non-inverting summer can also be constructed, using the non-inverting operational amplifier configuration. The input voltages are applied to the non-inverting input terminal and a part of the output is fed back to the inverting input terminal, through voltage-divider-bias feedback. Design of non-inverting summing circuit is approached by first designing the non-inverting amplifier to have the required voltage gain.

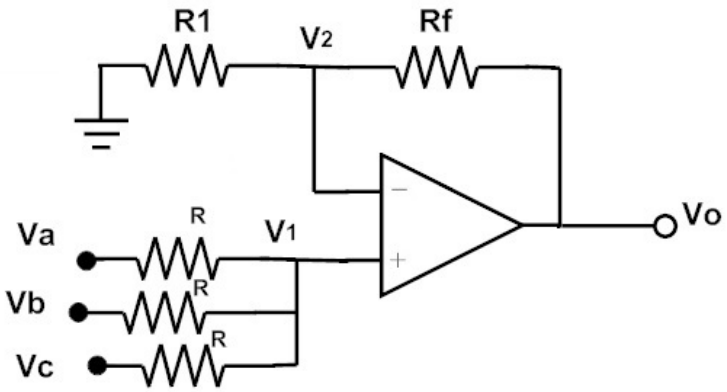
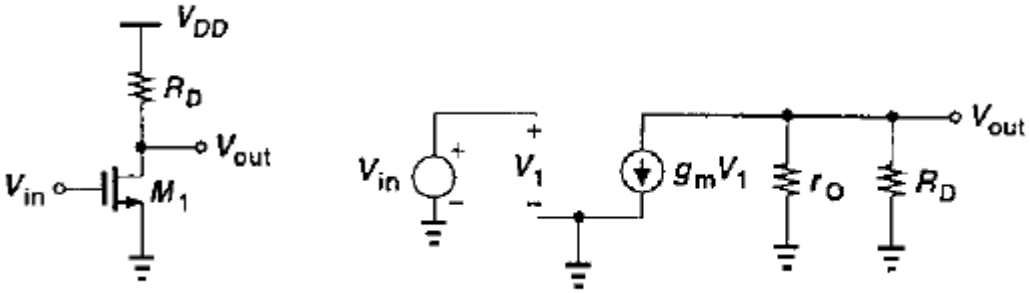


FIG 5.2 Non-inverting Op-amp Adder Configuration

FIG 5.2 shows the non-inverting Op-amp adder configuration. If the input resistances are equal, the output voltage of the above circuit is given by: $V_0 = V_a + V_b + V_c$. The first step taken is to build a common source amplifier with AC gain 1 as designed below.

COMMON SOURCE AMPLIFIER



(a) **(b)**

FIG 5.3 (a) Common Source Stage; (b) Small Signal Model of the CS Stage

FIG 5.3(a) shows the most general common source amplifier configuration. From its corresponding small signal ac model in FIG 5.3(b), the small signal voltage gain is calculated as follows:

Assuming, the MOSFET in saturation,

$V_1 = Vin$ -(1)

And, $Vout = -(r_o||R_D)g_mV_1$ -(2)

From (1) and (2),

$Vout = -(r_o||R_D)g_mVin$

or, $A_v = -(r_o||R_D)g_m$

GAIN ENHANCEMENT

From the expression of the gain derived above, it is evident that gain can be enhanced by increasing one or more of the three parameters: r_o, R_D or g_m. Since, g_m and r_o are internal MOSFET parameters, it is only R_D that can be varied externally to improve the gain.

Again, increasing R_D reduces the drain voltage as $V_D = V_{DD} - I_D R_D$, eventually pushing the MOSFET into triode region. So, an attempt should be made to increase the drain resistance, keeping the MOSFET in saturation. This can be done by placing an ideal current source at the drain of the MOSFET.

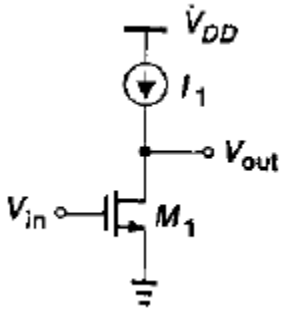


FIG 5.4 CS Stage with Ideal Current Source Load

Since, output resistance of a current source, R_o->∞, the gain becomes $-g_m r_o$ (maximum achievable gain of a Common Source Amplifier).

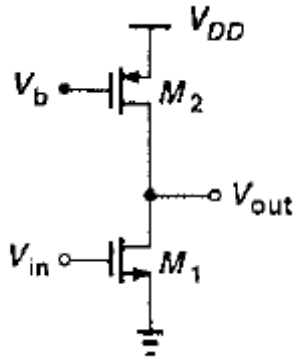


FIG 5.5 CS Stage with MOSFET as Current Source Load

FIG 5.5 shows a CS amplifier with a PMOS acting as Current Source Load. The PMOS will act as a constant current source only if it is in saturation. For the PMOS to be in saturation, it has to be ensured that the gate-to-source voltage is less than the threshold voltage and the drain voltage is at least one threshold below the gate voltage. A simple solution of the above mentioned criteria is to use a gate-drain connected PMOS(FIG 5.6), ensuring that it is always in saturation.

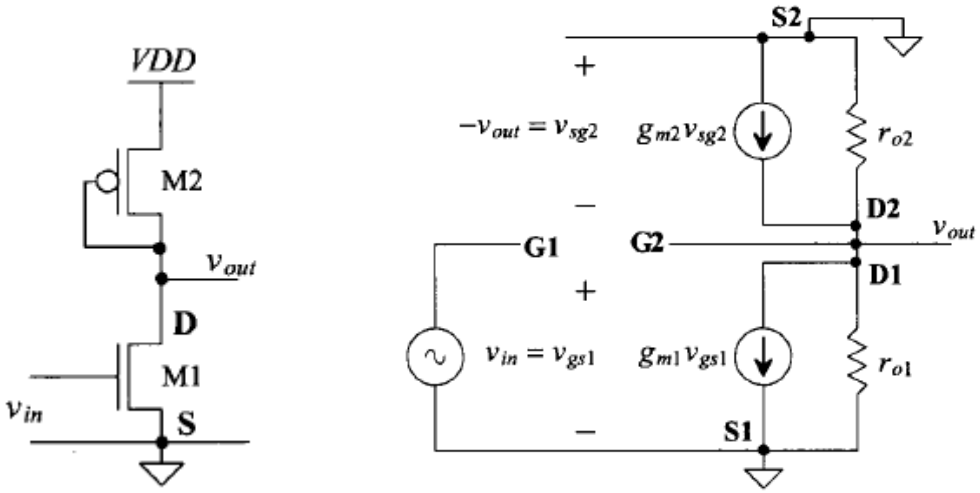


FIG 5.6 (a) CS Stage with Gate-Drain Load; (b) Small Signal Model of (a)

From the Small Signal Model in FIG 5.6(b),

Applying KCL at the output of the amplifier,

$$g_{m1}v_{in} + \frac{Vout}{ro1||ro2} = - g_{m2}v_{out}$$

$$\text{or, } A_v = \frac{Vout}{Vin} = - \frac{gm1}{gm2 + \frac{1}{ro1||ro2}} = - \frac{\frac{1}{gm2}||ro1||ro2}{\frac{1}{gm1}}$$

When $\frac{1}{gm2} \ll ro1||ro2$, $A_v \approx - \frac{gm1}{gm2}$.

DESIGNING A COMMON SOURCE AMPLIFIER WITH UNITY AC GAIN

From the expression derived above for gain, g_{m1} and g_{m2} are brought close and $ro1, ro2$ are made much higher with respect to $\frac{1}{gm2}$ by varying the W/L ratios of the MOSFETS to achieve unity gain.

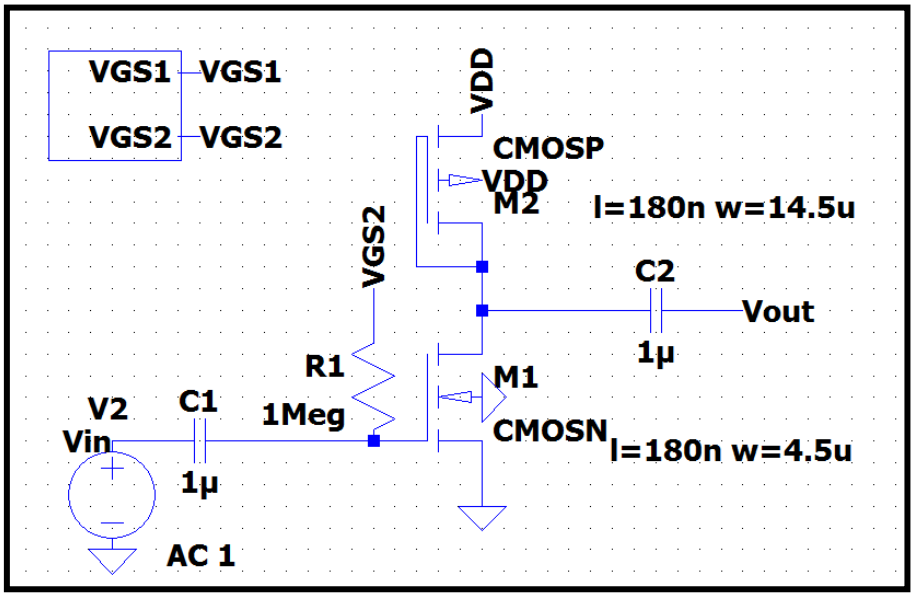


FIG 5.7 Common Source Amplifier having AC Gain 1

In the CS amplifier stage shown above (FIG 5.7), the MOSFET M1 has been kept in saturation region using a DC bias, VGS2 = 530mV (biasing circuit designed in Chapter 3).

SPICE Error Log: F:\DAC\Current source\gain1.log

Name:	m:x1:2	m:x1:1	m2	m1
Model:	x1:cmosn	x1:cmosn	cmosp	cmosn
Id:	1.90e-05	1.90e-05	-2.76e-05	2.76e-05
Vgs:	5.30e-01	4.83e-01	-5.49e-01	5.31e-01
Vds:	5.30e-01	4.83e-01	-5.49e-01	1.25e+00
Vbs:	0.00e+00	-4.76e-02	0.00e+00	0.00e+00
Vth:	4.93e-01	5.12e-01	-4.84e-01	4.88e-01
Vdsat:	6.17e-02	4.57e-02	-8.62e-02	6.38e-02
Gm:	3.69e-04	4.31e-04	4.82e-04	4.98e-04
Gds:	1.13e-05	1.38e-05	6.09e-06	1.19e-05
Gmb	9.04e-05	1.06e-04	1.43e-04	1.21e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.86e-15	1.54e-14	1.13e-14	3.86e-15
Cgdov:	3.86e-15	1.54e-14	1.13e-14	3.86e-15
Cgbov:	1.46e-19	1.46e-19	1.21e-19	1.46e-19
dQgdVgb:	1.16e-14	4.05e-14	3.40e-14	1.17e-14
dQgdVdb:	-3.84e-15	-1.54e-14	-1.13e-14	-3.84e-15
dQgdVsb:	-7.06e-15	-2.09e-14	-2.15e-14	-7.18e-15
dQddVgb:	-5.20e-15	-1.77e-14	-1.55e-14	-5.26e-15
dQddVdb:	3.85e-15	1.54e-14	1.13e-14	3.85e-15
dQddVsb:	1.72e-15	2.93e-15	5.45e-15	1.79e-15
dQbdVgb:	-1.15e-15	-5.02e-15	-2.99e-15	-1.15e-15
dQbdVdb:	8.60e-19	1.52e-18	-1.27e-18	1.38e-18
dQbdVsb:	-2.42e-16	-4.10e-16	-6.85e-16	-2.51e-16

FIG 5.8 Spice Error Log Showing MOSFET Parameters of M1 and M2

From the spice error log(FIG 5.8),

$g_{m1} = 4.98 \times 10^{-4}$ S

$g_{m2} = 4.82 \times 10^{-4}$ S

$r_{o1} = \frac{1}{1.19\ X\ 10^{-5}}\Omega = 84.033k\Omega$

$r_{o2} = \frac{1}{6.09\ X\ 10^{-6}}\Omega = 164.204k\Omega$

Now, $r_{o1} || r_{o2} = 55.6k\Omega$

Therefore, $A_v = -\frac{\frac{1}{gm2}||ro1||ro2}{\frac{1}{gm1}} = -\frac{2.074||55.6}{2.088} = -0.958$(approx.)

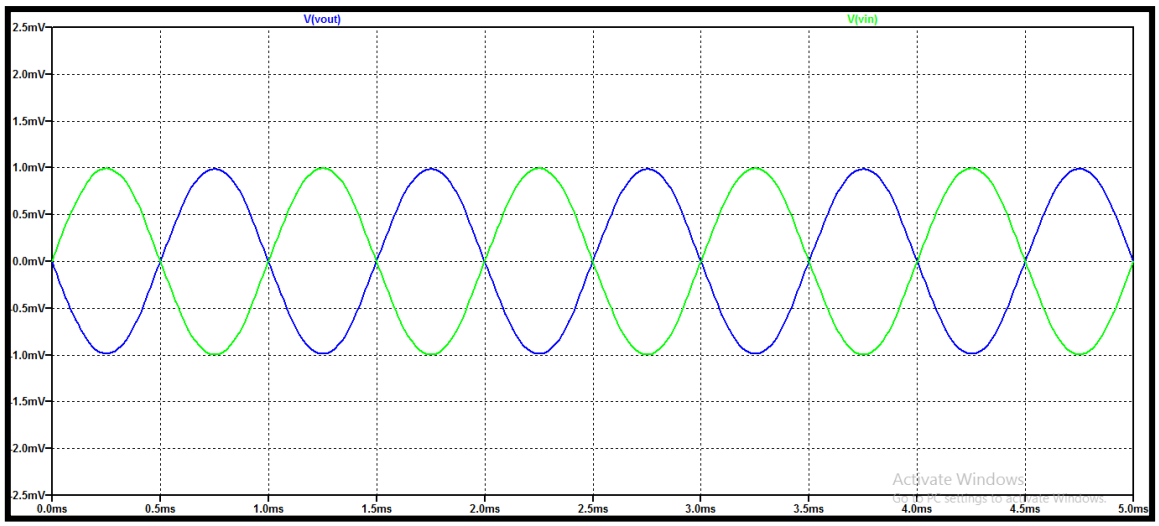


FIG 5.9 Transient Response of Amplifier for a Sinusoidal Input of 1mV

Simulation for the transient response shows an AC gain of $|A_v| = 0.988$ (approximately 1) with a phase shift of 180°.

An attempt has been made to design the required differential amplifier using a Folded Cascode configuration as discussed below.

FOLDED CASCODE AMPLIFIER

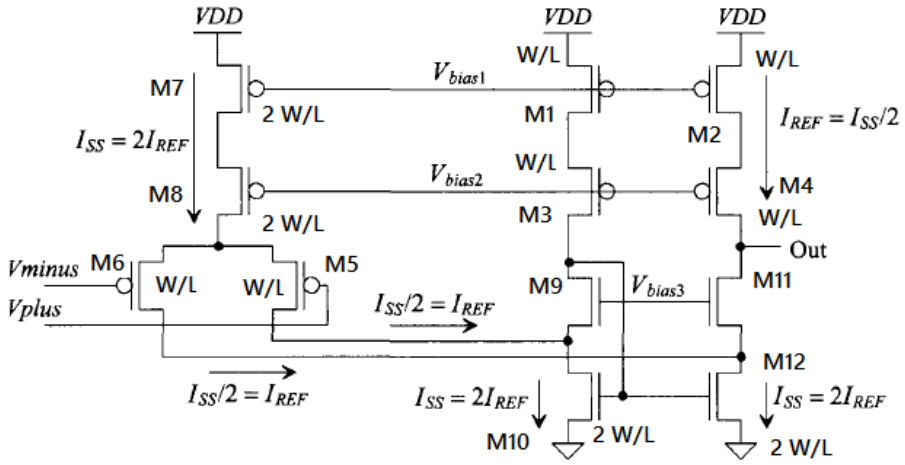


FIG 5.10 Folded Cascode Configuration

The folded cascade amplifier is a special type of differential amplifier where the amplifier functions perfectly even when the input signal swings below the ground level. The differential input voltages are applied at the gates of the PMOS transistors, M5 and M6 and output is taken at drain of M4. Since, for proper functioning of the folded cascade, all the transistors need to remain in saturation, the input voltage can be at most

V_{inmax} = VDD – $2V_{SDsat}$(needed to keep M7 and M8 in saturation) – V_{SG}

Similarly, the minimum input voltage that has to be applied to the gate is obtained by noting the minimum drain voltage of M5 and M6 i.e. V_{DSsat}(needed to keep M10 and

M12 in saturation). Therefore, $V_{inmin} = V_{DSsat} - V_{THP}$. Thus, if $|V_{THP}|$ is greater than V_{DSsat}, then V_{in} can very well go below ground. However, the output voltage is limited to swing between $2V_{DSsat}$ above ground and $2V_{DSsat}$ below VDD.

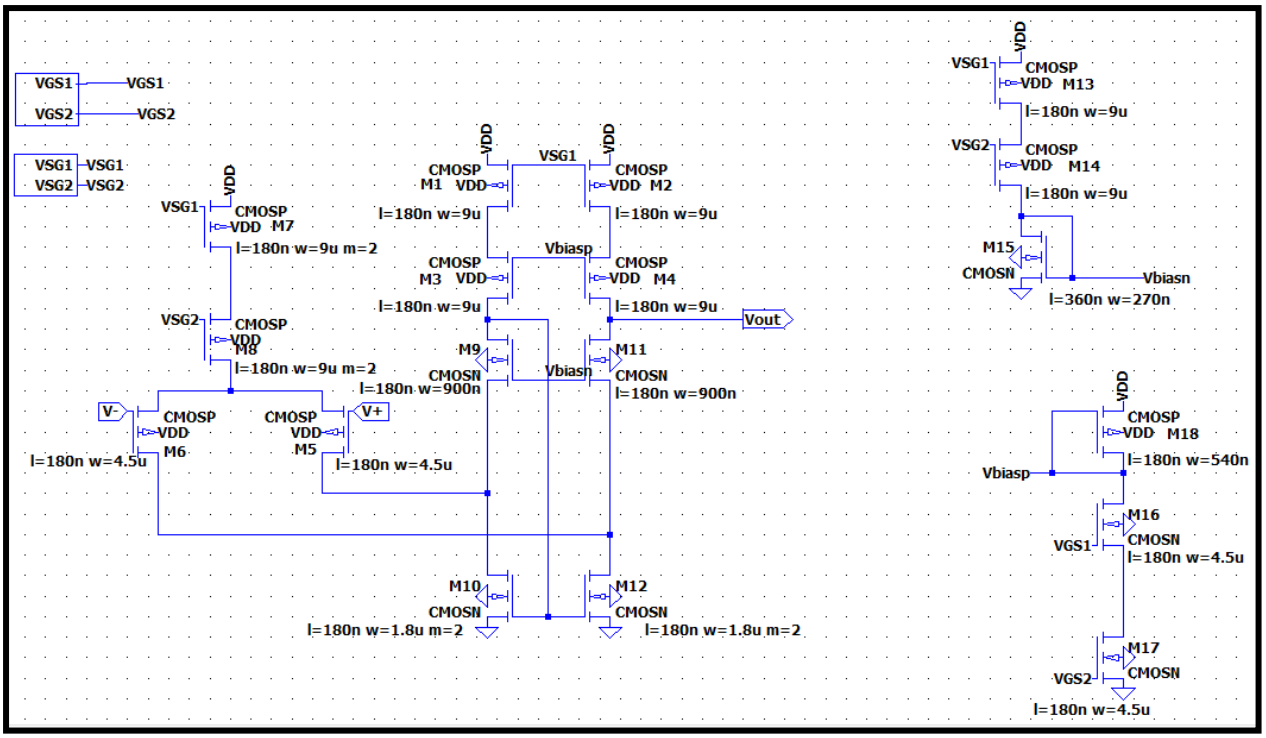


FIG 5.11 Implementation of a Differential Amplifier using Folded Cascode Configuration

SOURCE FOLLOWER

Folded cascade configuration can drive only capacitive loads or very high resistive loads. Hence the AC response of the output becomes unstable. Since a resistive load is present, to overcome the difficulty a source follower is used at the output. For low voltage applications, an NMOS source follower is used and for high voltage applications, a PMOS source follower is preferred.

Since, the source follower (or common drain) configuration provides unity small signal gain, the transfer characteristics of the folded cascode remains unaltered and the extra voltage at lower levels is compensated by the gate-source voltage drop of a NMOS source follower. Similarly, in case of a PMOS source follower, the low voltage at higher voltage levels get enhanced by the source-gate voltage gain.

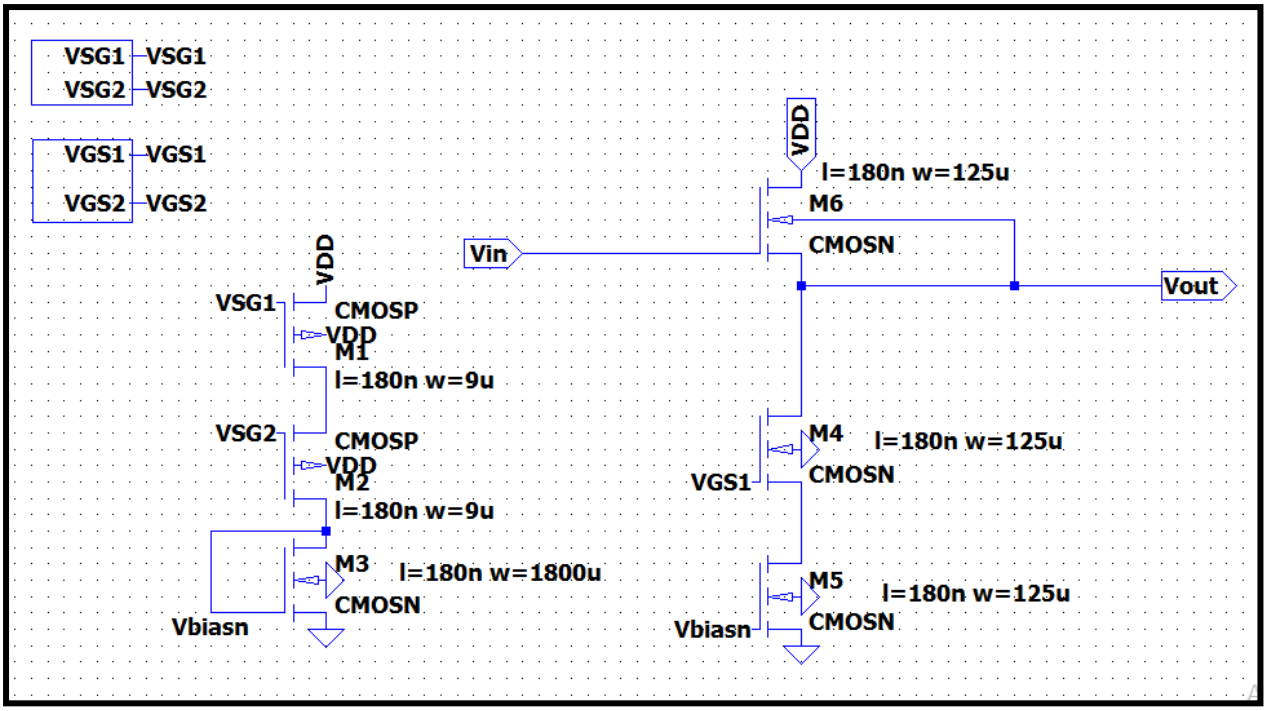


FIG 5.12 Source Follower

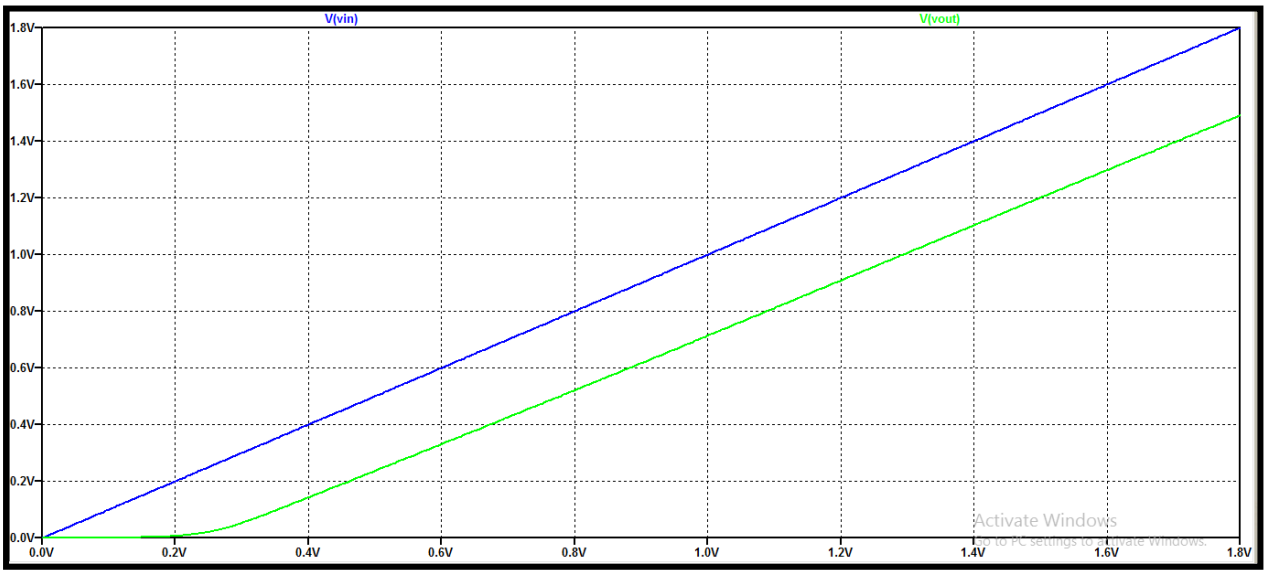


FIG 5.13 Output of Source Follower(of FIG 5.12)

FIG 5.13 shows the output response of an NMOS source follower.

FOLDED CASCODE AMPLIFIER WITH SOURCE FOLLOWER AT OUTPUT

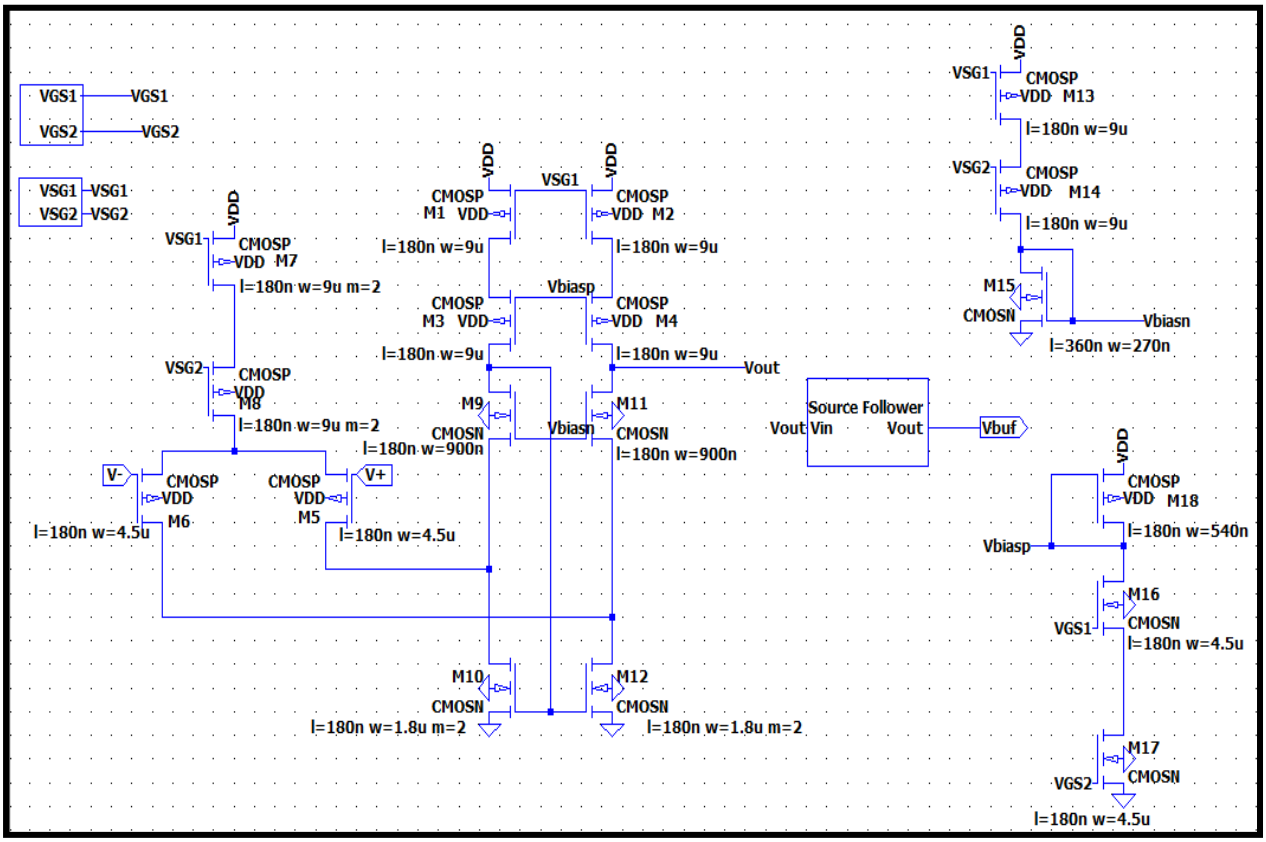


FIG 5.13 Folded Cascode with Source Follower

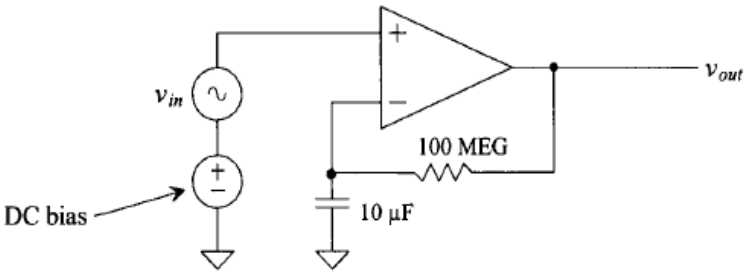


FIG 5.14 Circuit Configuration to Simulate Open Loop Frequency Response

FIG 5.14 shows the circuit configuration of Op-amp to check open loop AC response of the amplifier.

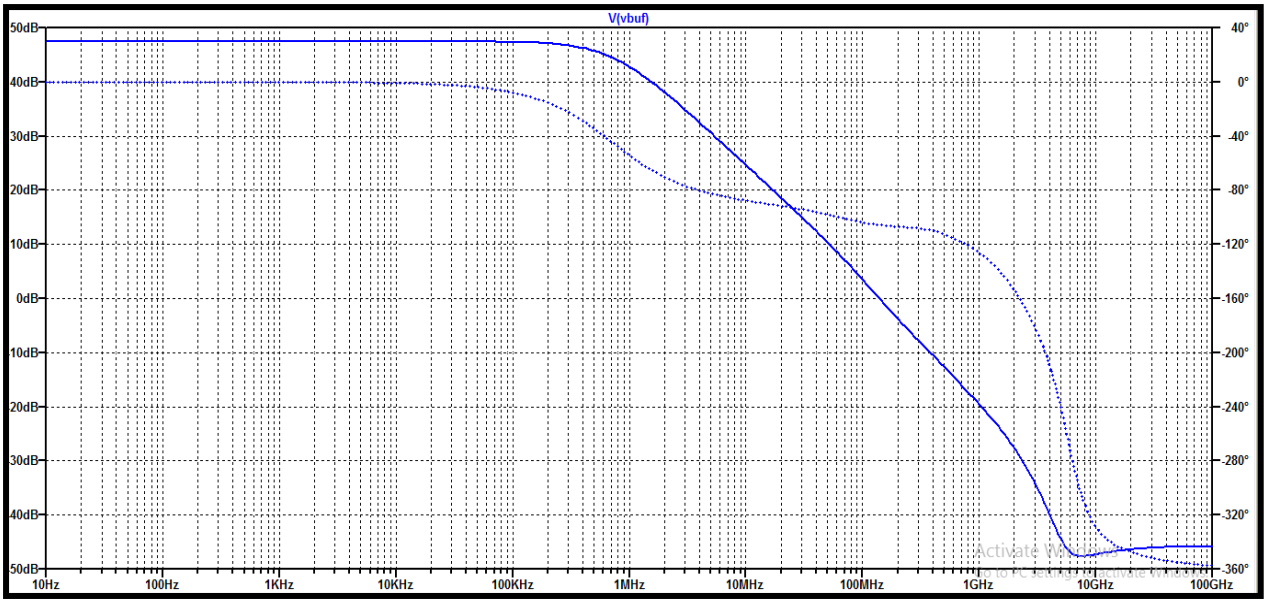


FIG 5.15 Simulation Showing Open Loop Frequency Response

FIG 5.15 shows the open loop frequency response of the buffer amplifier for an input ac signal of 1V. From the response, it is observed

- Open Loop Gain = 237 (47.5dB)
- 3 dB Bandwidth = 1.47MHz
- Phase-Margin = 20°

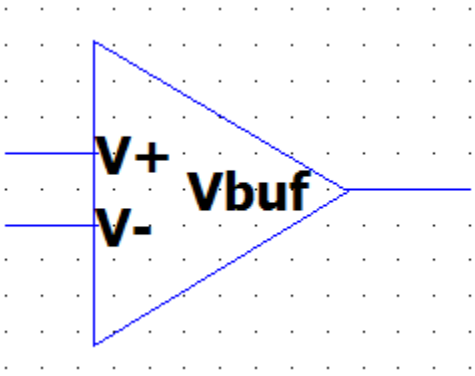


FIG 5.16 Block Diagram of Non-Inverting Op-amp

The final designed non-inverting Op-amp of FIG 5.16 is then used as a summing amplifier in the non-inverting configuration.

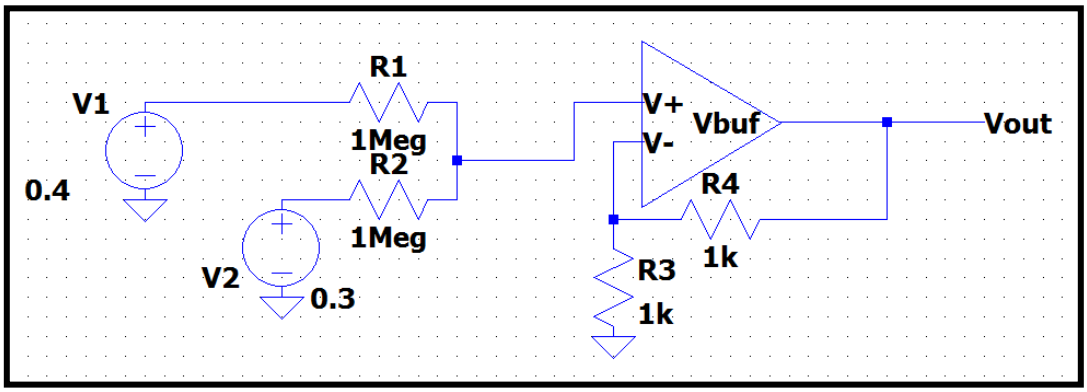


FIG 5.17 Example Illustrating Adder

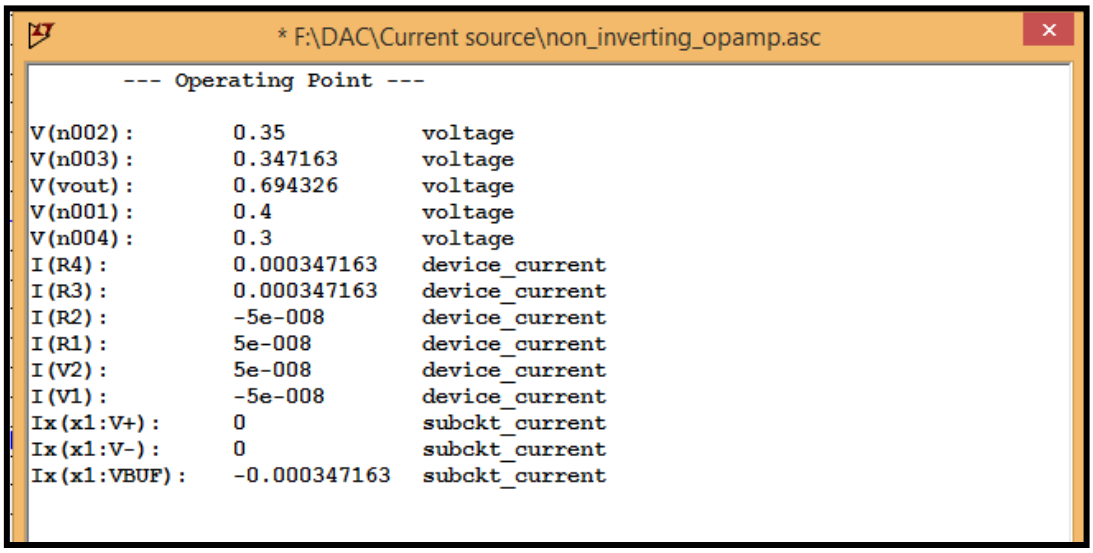


FIG 5.18 Operating Point Output

For equal resistances R1 and R2, the output voltage should be the sum of the voltages V1 and V2(FIG 5.17).
Therefore, Vout = 0.4V + 0.3V = 0.7V
Simulation(FIG 5.18) shows Vout = 0.694V, thus ensuring proper working of the amplifier.

CHAPTER 6

DESIGN OF THE PROPOSED DAC ARCHITECTURE

As discussed in the previous chapters, implementation of a low power, high resolution, high speed current steering DAC architecture has been discussed in this section. It has been implemented using MOS based current sources, current switches and a non-inverting operational amplifier.

DESIGN OF THE 6 BIT FINE DAC WITH 1mV RESOLUTION

The block diagram of the DAC is shown in FIG , and the internal circuit diagram is shown in FIG .

BLOCK DIAGRAM

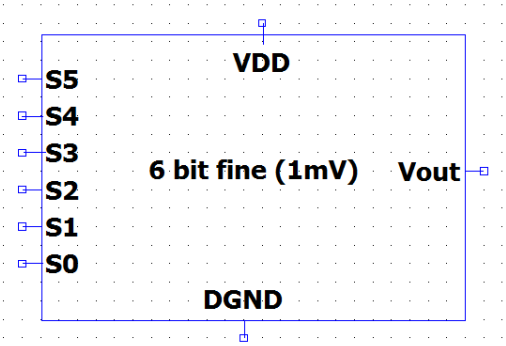


FIG 6.1 Block Diagram of the 6 bit fine DAC Architecture

In FIG 6.1, S0 through S5 represent the digital inputs and Vout is the corresponding analog output of the DAC. VDD represents the analog source and DGND represents the analog ground of the DAC.

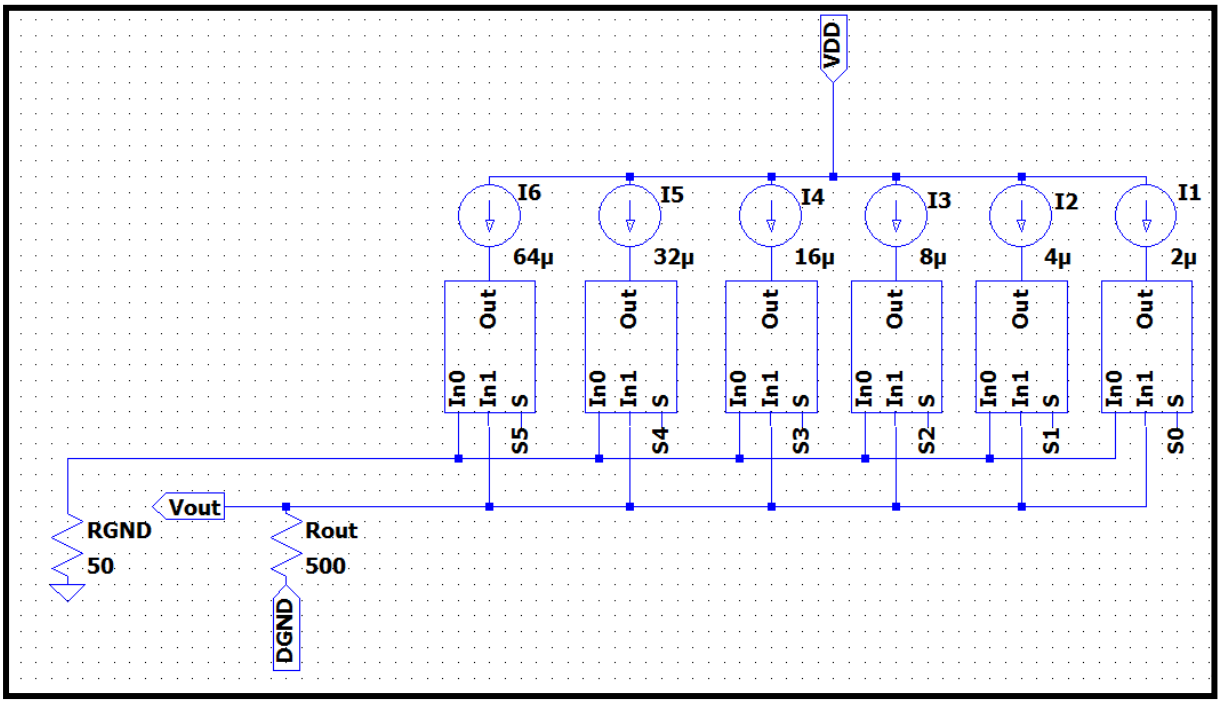


FIG 6.2 Circuit Diagram of the 6 bit fine DAC Architecture

The current sources shown here have been implemented with PMOS transistors having necessary aspect ratios so as to source the desired amount of current. In order to keep power consumption low, an LSB current of 2µA has been chosen. For an N bit current steering DAC, the current sources corresponding to each bit are weighted such that the current for the MSB is 2^{N-1} times I_{LSB} and the total current $I = (2^0 + 2^1 + 2^2 + ... + 2^{N-1}) I_{LSB} = (2^N – 1) I_{LSB}$.

Here, N=6 and I_{LSB} = 2µA. Therefore, I_{MSB} = 64µA and I = 126µA.

INTERNAL CIRCUIT OF CURRENT SOURCE

The current sources of FIG 6.2 have been biased using the same biasing circuit to minimise power consumption. Design of the final biasing circuit for the PMOS current sources have been described in Section .The biasing circuit was originally designed for supplying a current of 20µA. However, since the desired I_{LSB} = 2µA, the W/L ratio was reduced 10 times to get a current of 2µA. However, it was observed that an exact current of 2µA was not obtained with W = 9µm/10 = 900nm and L=180nm. Simulations resulted in I_{LSB} = 2µA when W = 820nm instead of W = 900nm.

Implementing weighted current sources using PMOS requires the width of the PMOS components to be multiplied in the same ratio.

Preliminary simulation experiments, with sizing of widths of the transistors in current sources as discussed above, did not result in the currents proportional to widths of the transistors. This anomaly is perhaps due to the variation of effective width for smaller widths of transistors. This narrowing of widths for smaller widths is known as Narrow Width Effect or Short Channel Effect. To overcome this problem, the number of transistors with the same width, are used in parallel instead of using transistors of different widths. The number of transistors is proportional to the current of the current source. This approach also improves the linearity and reduces the problems arising because of the mismatch of transistors.

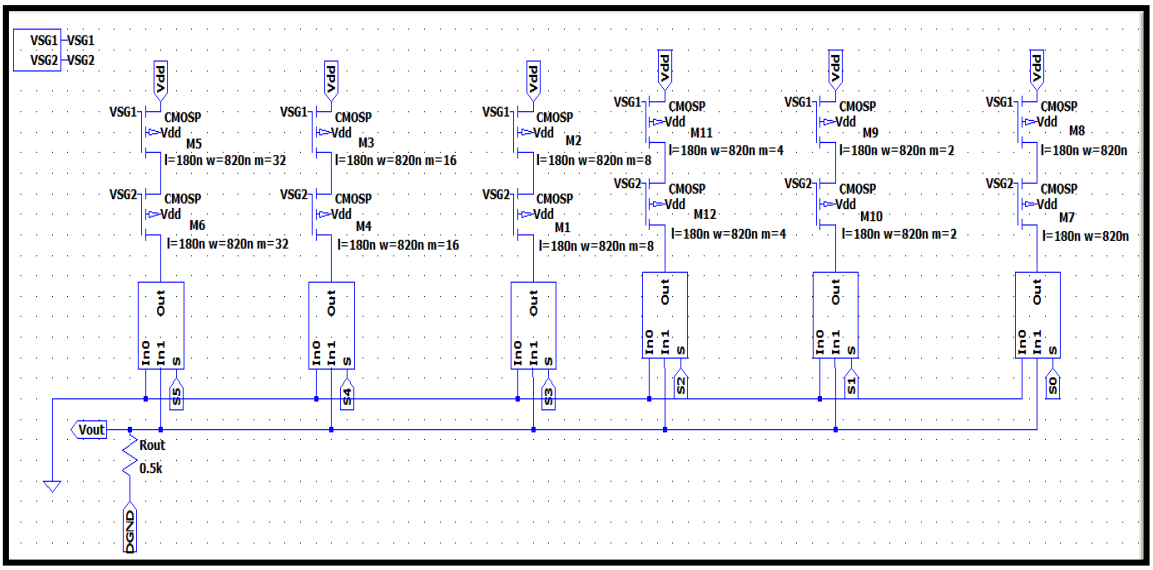


FIG 6.3 PMOS components as the current sources

The bias voltages VSG1 and VSG2 as shown in FIG 6.3, are generated using the designed biasing circuit in Chapter 3.

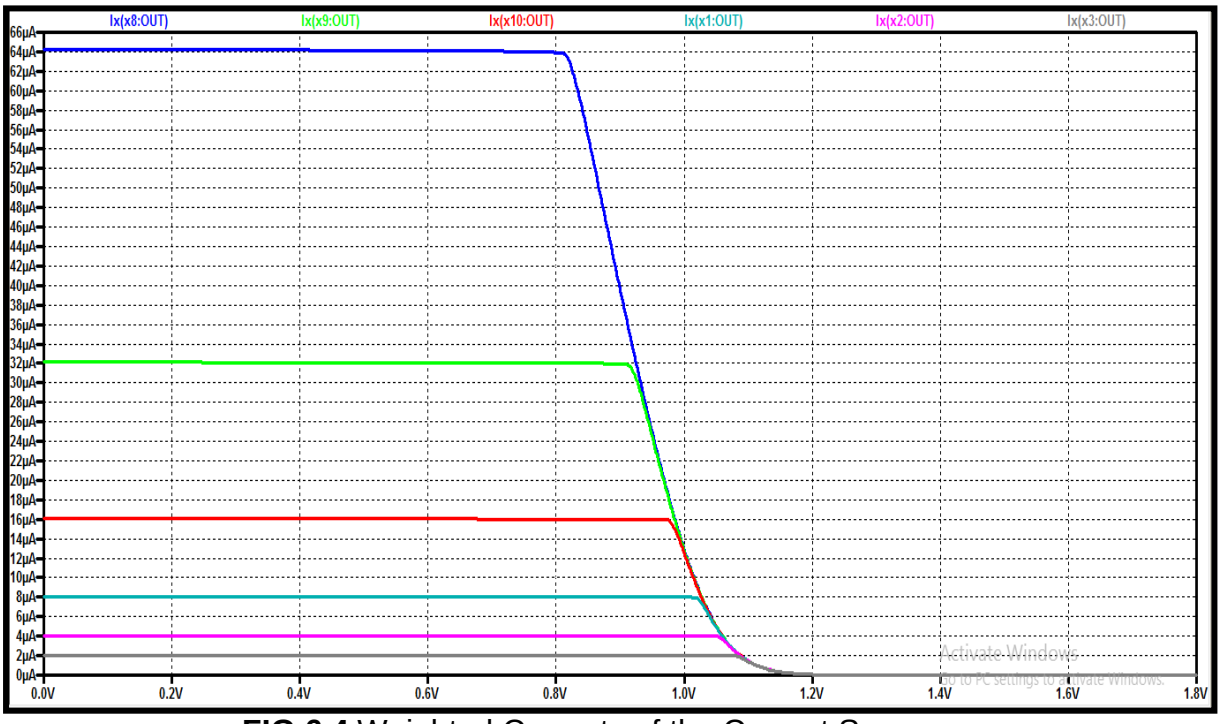


FIG 6.4 Weighted Currents of the Current Sources

As mentioned in the abstract, for a resolution of 1mV, the full scale voltage of a 6 bit DAC has to be equal to 63mV. Again, the current corresponding to full scale voltage is I = 126µA. Therefore, the resistance Rout = 63mV/126µA = 500Ω.

INTERNAL CIRCUIT OF CURRENT SWITCH

The internal circuit diagram of the current switch shown in the block diagram of FIG 6.2, is shown below in FIG 6.5. It sinks the current supplied by the current sources and directs it to one of the two output paths, In1or In0 depending on the switch input, S. The W/L ratio of the NMOS transistors M1 and M2 (FIG 6.5) are chosen such that the switch is powerful enough to sink the current supplied by the current source.

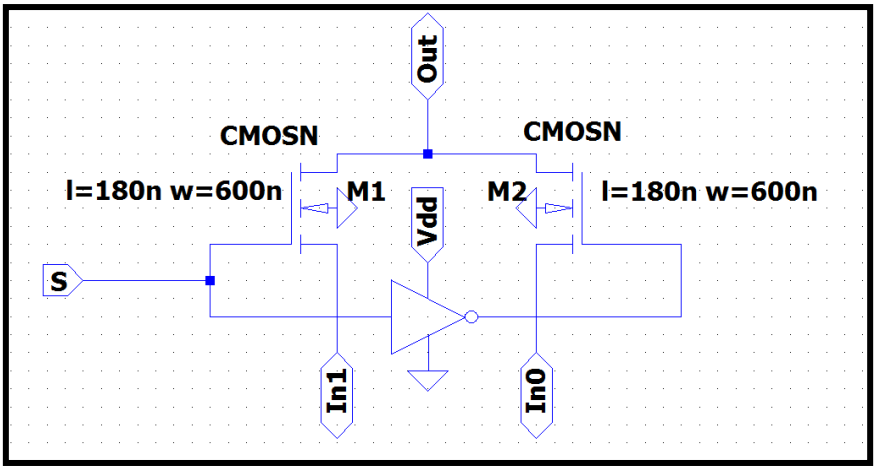


FIG 6.5 Internal Circuit of Current Switch

INTERNAL CIRCUIT OF CMOS INVERTER

The CMOS inverter used in the internal circuit diagram of the current switch has the following schematic (FIG 6.6).

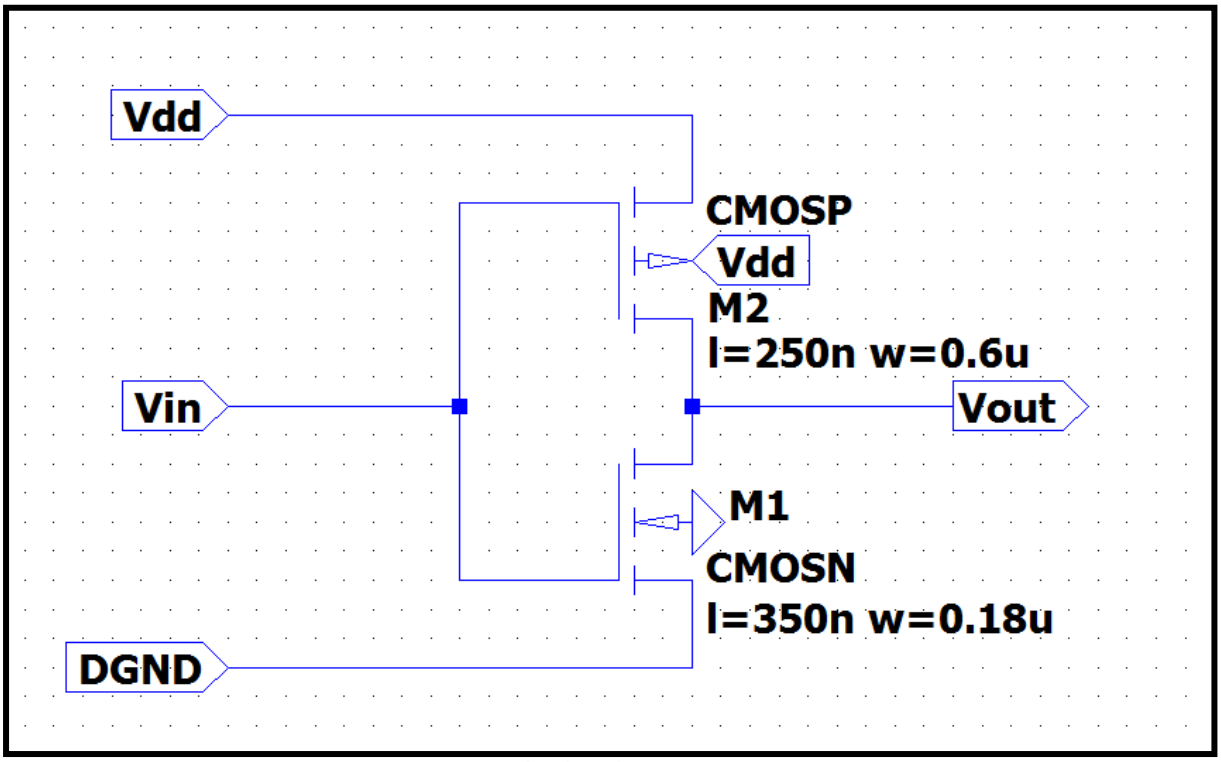


FIG 6.6 Internal Circuit of CMOS Inverter

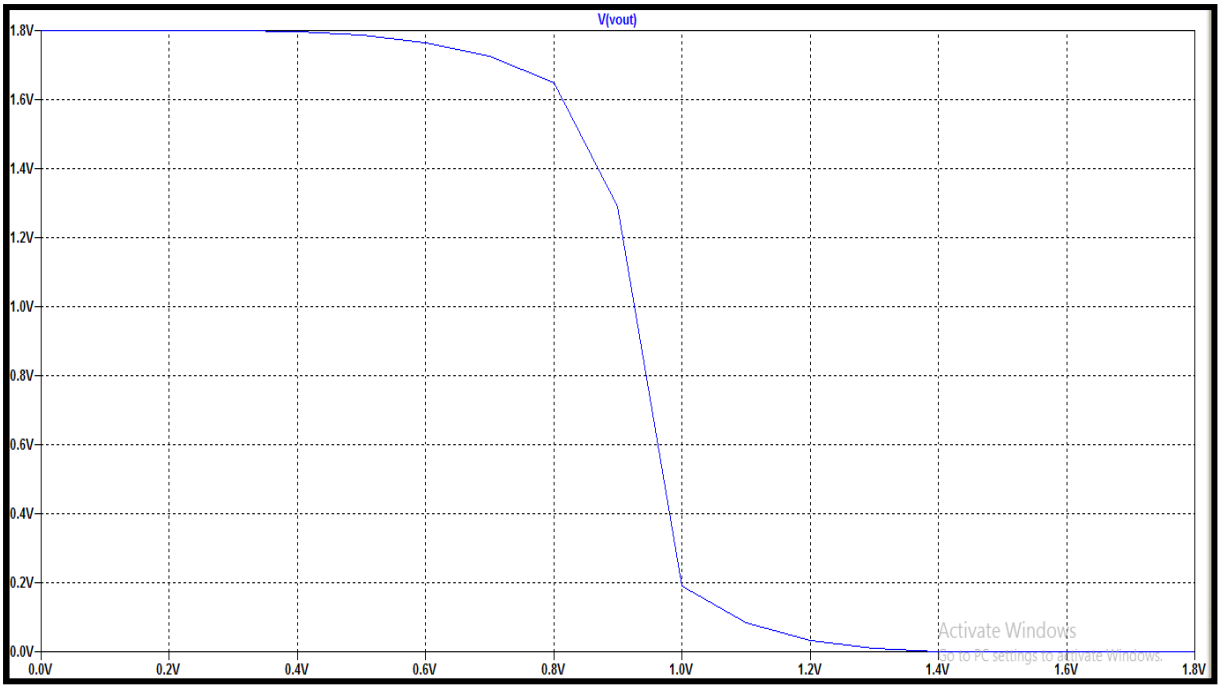


FIG 6.7 Inverter Action

As defined previously,
NMl (Noise Margin Low) = Vil – Vol
NMh (Noise margin High) = Voh – Vih

Now, Vol = 0 and Voh = VDD(1.8V).
Simulation results show : Vil = 0.792V and Vih = 1.092V. Therefore, NMl = 0.792V – 0V = 0.792V and NMh = 1.8V – 1.092V = 0.708V and the undefined region, Vih – Vil = 1.092V – 0.792V = 0.3V. Since, the undefined region is very small, therefore both transistors are simultaneously in saturation for a brief range, thereby resulting in a quick transition.

DESIGN OF THE 3 BIT COARSE DAC WITH 64mV RESOLUTION
The block diagram of the DAC is shown in FIG 6.8, and the internal circuit diagram is shown in FIG 6.9.

BLOCK DIAGRAM

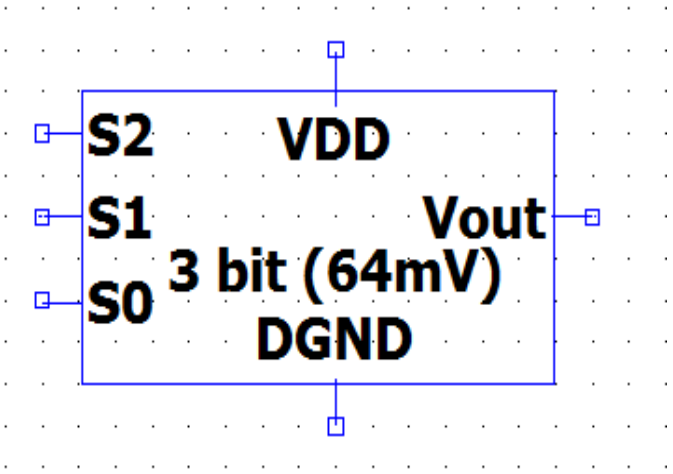


FIG 6.8 Block Diagram of the 3 bit coarse DAC Architecture
In FIG 6.8, S2, S1 and S0 represent the digital inputs and Vout is the corresponding analog output of the DAC. VDD represents the analog source and DGND represents the analog ground of the DAC.

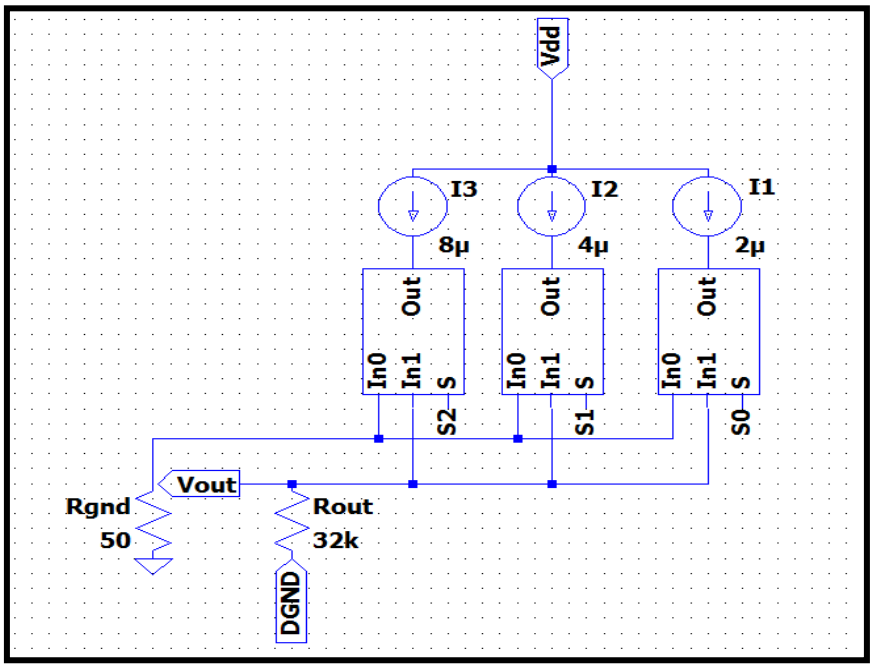


FIG 6.9 Circuit Diagram of the 3 bit coarse DAC Architecture

For the coarse DAC, N=3 and I_{LSB} = 2µA. Therefore, I_{MSB} = 8µA and I = 14µA. As mentioned in the abstract, for a resolution of 64mV, the full scale voltage of a 3 bit DAC has to be equal to (64x7)mV = 448mV. Again, the current corresponding to full scale voltage is I = 14µA. Therefore, the resistance Rout = 448mV/14µA = 32kΩ.

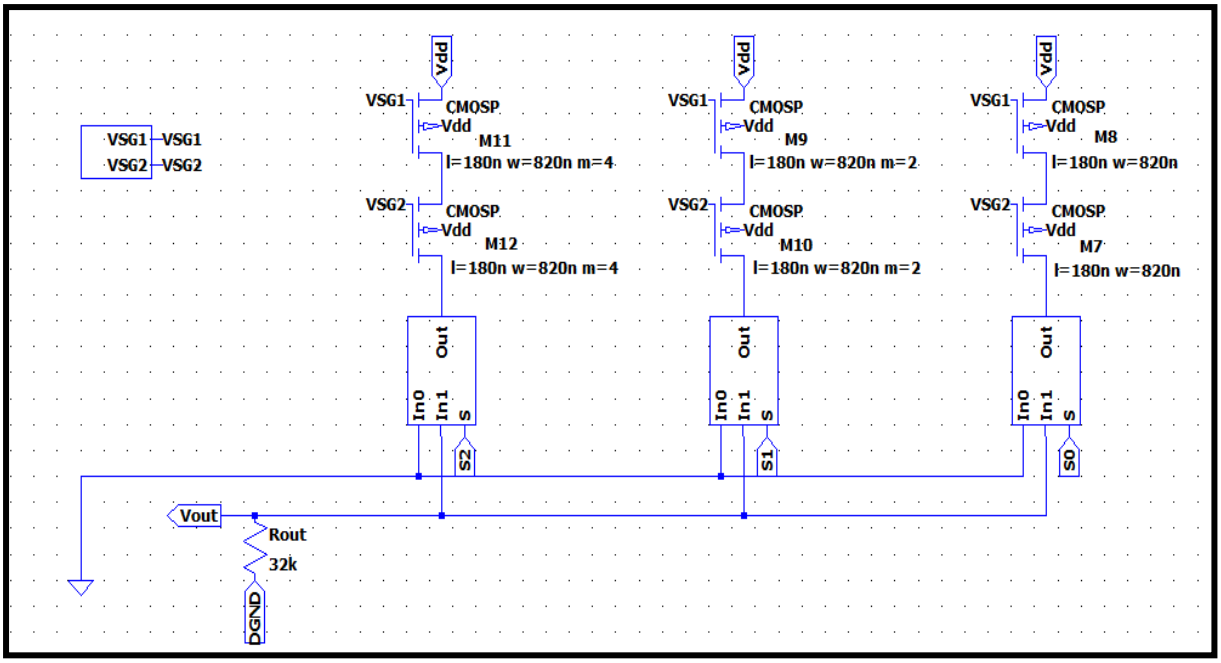


FIG 6.10 PMOS Components as Current Sources

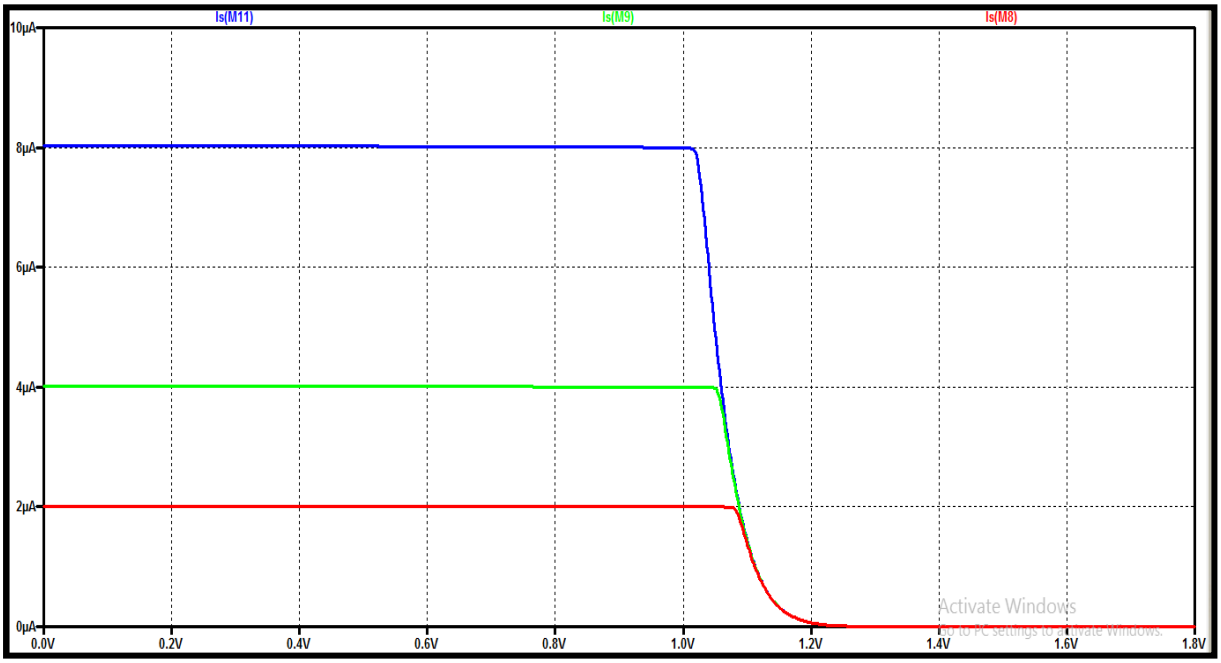


FIG 6.11 Weighted Currents of the Current Sources

DESIGN OF THE COMBINED DAC

As described in the abstract, in the combined DAC, the analog output of the 3 bit coarse DAC is added to the analog output of the 6 bit fine DAC through an operational amplifier in non-inverting configuration. The result will be an effective 9

bit DAC with 1mV resolution, having $2^9 - 1 = 511$ levels. Therefore, full scale voltage = full scale voltage of coarse DAC + full scale voltage of fine DAC = (448 + 63)mV = 511mV.

USE OF OP-AMP AS THE SUMMING AMPLIFIER

The individual DAC structures (coarse and fine) have been designed for open circuit load. Now, if the DAC outputs are directly fed to the inputs of the non-inverting summing Op-amp through some arbitrary resistance, then that resistance comes in parallel with the 32kΩ and 500Ω resistances in the coarse and fine DACs respectively, drastically reducing the output resistance of the individual DACs, thereby changing the DAC outputs.

Therefore, the aim is to make these input resistances as high as possible so that equivalent resistance of the overall parallel combination is very close to the smaller resistance of the combination. In the combined architecture shown below (FIG 6.12), 1MΩ resistors are used.

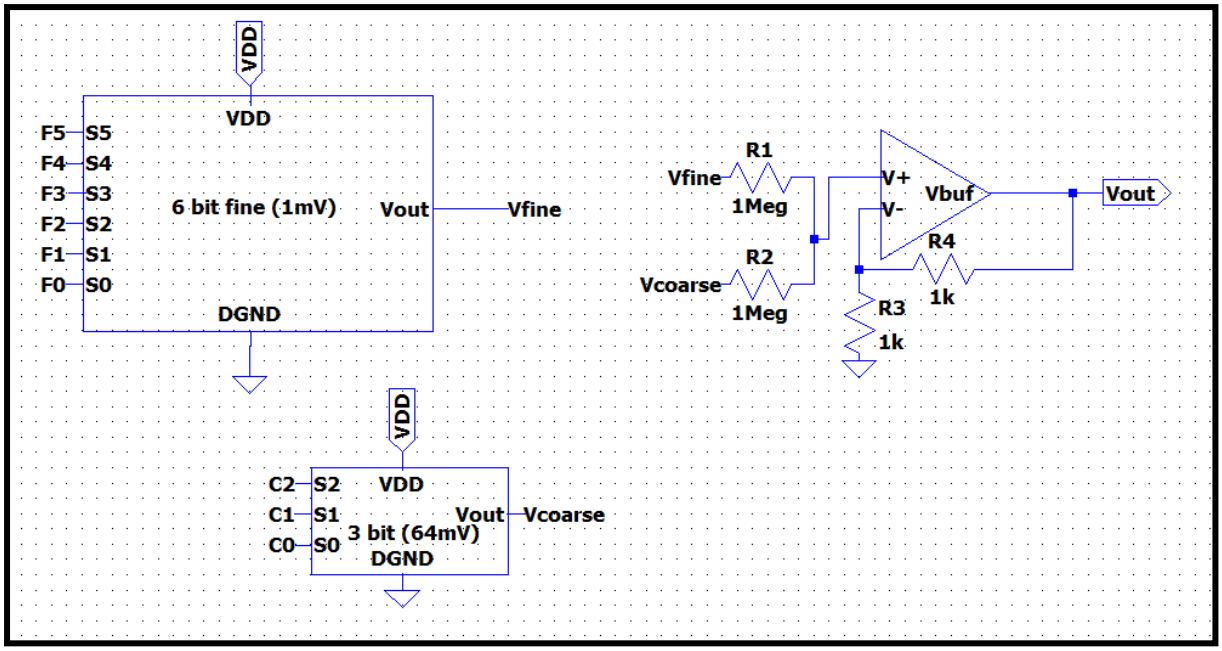


FIG 6.12 Block Diagram of Combined DAC Architecture

CHAPTER 7

ELECTRICAL CHARACTERISTICS OF DAC

The electrical characteristics of the DAC structures are listed below in the following section in tabular form.

TABLE 7.1

OPERATING CONDITIONS	
Supply Voltage, VDD	1.8V
High-level digital input voltage, V_{IH}	1.8V
Low-level digital input voltage, V_{IL}	0V
Operating free-air temperature, T_A	27°C

ELECTRICAL CHARACTERISTICS OF 6 BIT FINE DAC

TABLE 7.2

POWER SUPPLY		
Power supply current, IDD	0.306mA	
Power supply rejection ratio, PSRR	Zero scale	-114dB(±0.2V VDD variation)
	Full scale	-61.5dB(±0.2V VDD variation)
Power consumption	0.5508mW	

TABLE 7.3

STATIC DAC SPECIFICATIONS	
Resolution	1mV
Integral Non-Linearity, INL	0.266LSB
Differential Non-Linearity, DNL	0.005LSB
Zero-scale error(offset error at zero scale)	9.862×10^{-6} LSB
Gain error	0.0042

TABLE 7.4

OUTPUT SPECIFICATIONS			
Parameter	Test Conditions	Rated voltage	Full scale voltage
Output load regulation accuracy	R_L = 10kΩ	5%	4.76%
	R_L = 100kΩ	0.5%	0.476%

TABLE 7.5

ANALOG OUTPUT DYNAMIC PERFORMANCE		
Parameter	Test Conditions	Value
Output settling time(full scale), $t_{s(FS)}$	R_L = 10kΩ, C_L = 100pF	0.31μs
	C_L = 10pF	0.04μs
Output settling time(code to code), $t_{s(CC)}$	R_L = 10kΩ, C_L = 100pF	0.25μs
	C_L = 10pF	0.038μs
Slew rate, SR	R_L = 10kΩ, C_L = 100pF	95V/μs
	C_L = 10pF	950V/μs
Total harmonic distortion, THD	f_{out} = 0.80645kHz R_L = 100kΩ, C_L = 100pF	-38.8dB(1.15%)

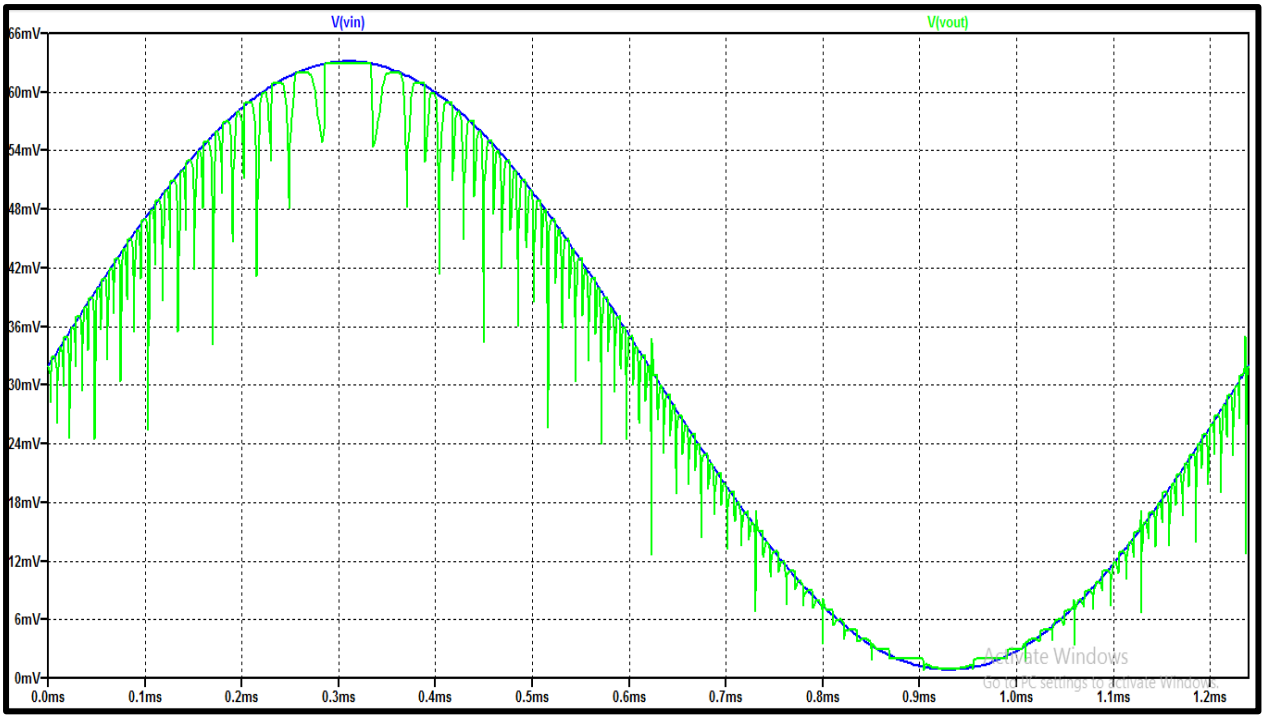


FIG 7.1DAC Output for a Digitally Synthesized Sine Wave Input
(R_L = 100kΩ, C_L = 100pF)

The above graph shows the DAC output corresponding to a digitally synthesized sine wave having frequency, f_{out} = 0.80645kHz and time period, T = 1.24ms.

However, due to use of piece wise linear input(PWL file) in Spice for obtaining sine wave sample points in time domain, transitions from logic '0' to logic '1' (1.8V) and vice versa are linear, not abrupt. Hence, glitches arise in the output. This problem has been addressed in a later chapter.

SPICE Error Log: F:\DAC\Current source\DAC_6bit_PWL.log

```
N-Period=1
Fourier components of V(vout)
DC component:0.0309648

Harmonic     Frequency     Fourier     Normalized    Phase      Normalized
 Number        [Hz]       Component     Component   [degree]    Phase [deg]
    1       8.065e+02    2.993e-02    1.000e+00       0.01°       0.00°
    2       1.613e+03    1.834e-04    6.127e-03     -89.74°     -89.75°
    3       2.419e+03    1.420e-04    4.745e-03    -178.44°    -178.45°
    4       3.226e+03    1.546e-04    5.167e-03      91.73°      91.72°
    5       4.032e+03    1.083e-04    3.619e-03       2.60°       2.59°
    6       4.839e+03    9.892e-05    3.305e-03     -86.38°     -86.38°
    7       5.645e+03    8.240e-05    2.753e-03    -171.45°    -171.46°
    8       6.452e+03    8.604e-05    2.875e-03      98.49°      98.49°
    9       7.258e+03    7.229e-05    2.415e-03      12.12°      12.11°
Total Harmonic Distortion: 1.150853%(9.840835%)
```

FIG 7.2 Calculating Total Harmonic Distortion (THD)
(R_L = 100kΩ, C_L = 100pF)

FIG 7.2 shows the total harmonic distortion (THD) for the DAC output in response to the digitally synthesized sinusoidal input.

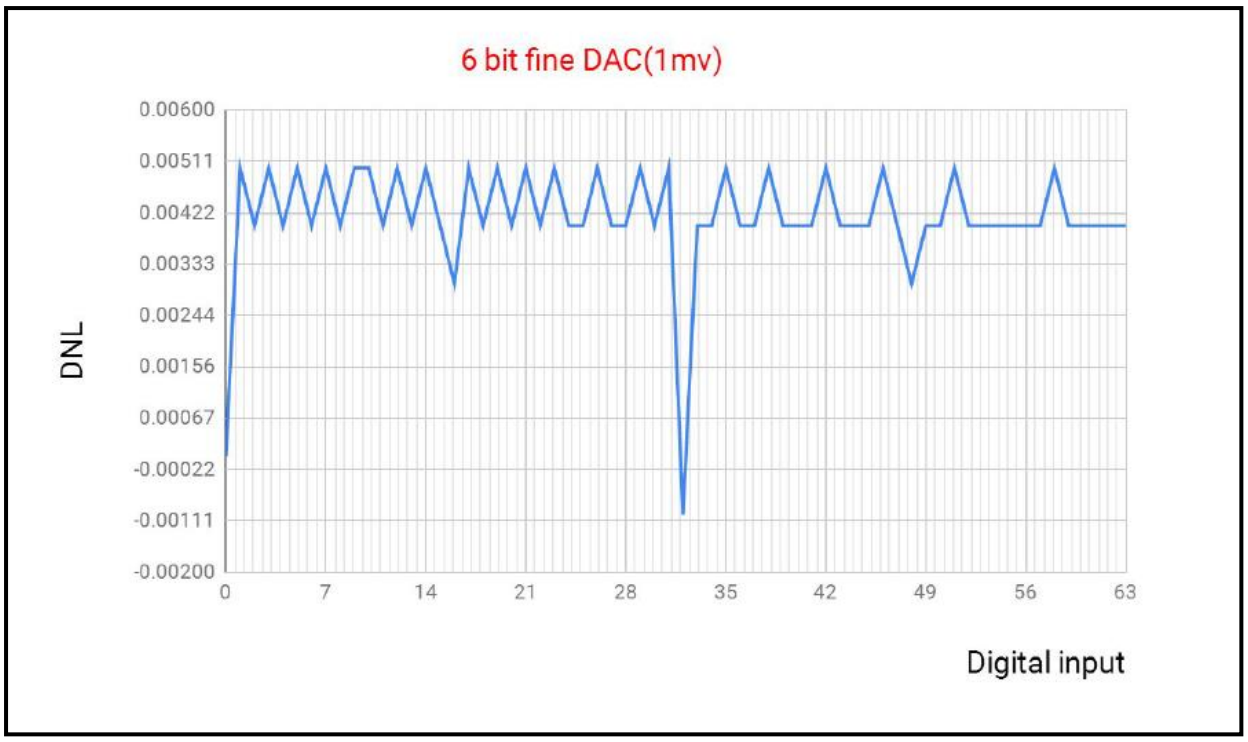


FIG 7.3 Differential Non-Linearity Error

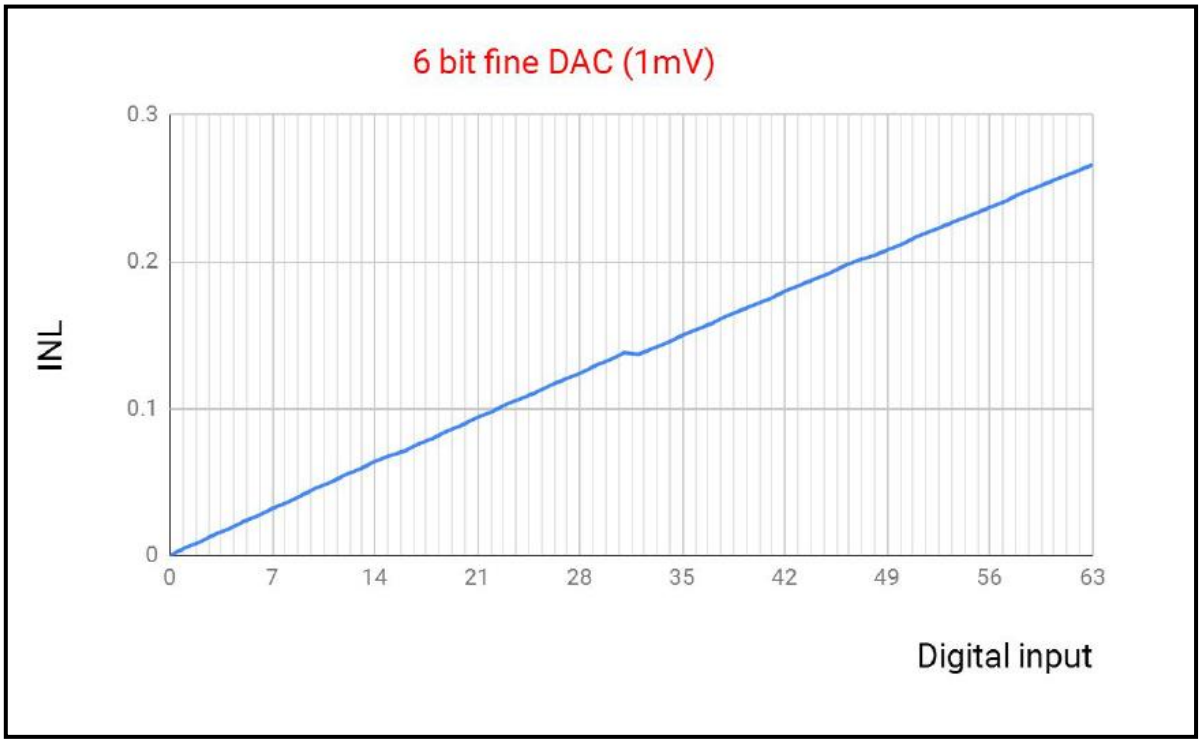


FIG 7.4 Integral Non-Linearity Error

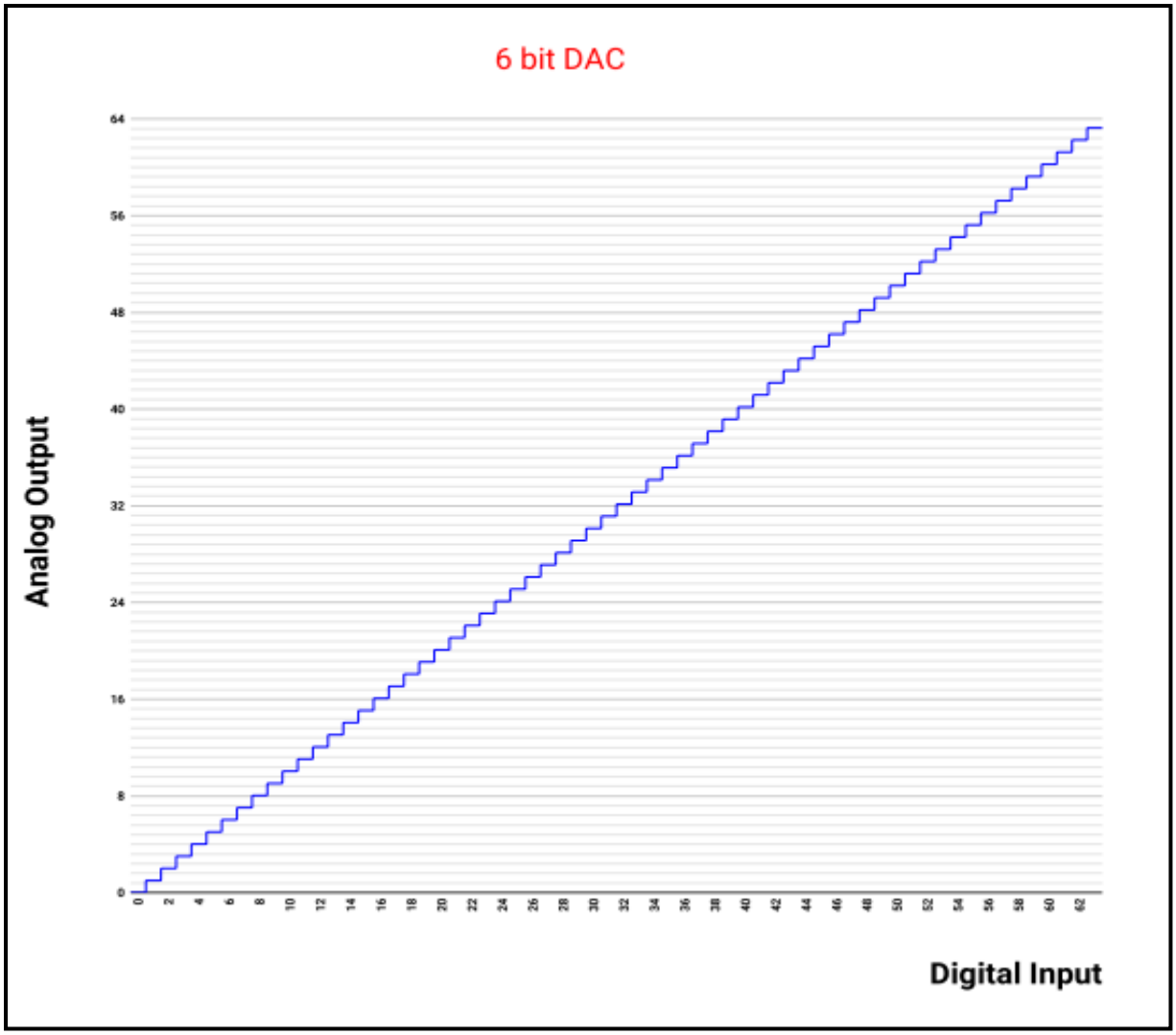


FIG 7.5 Analog Output v/s Digital Input

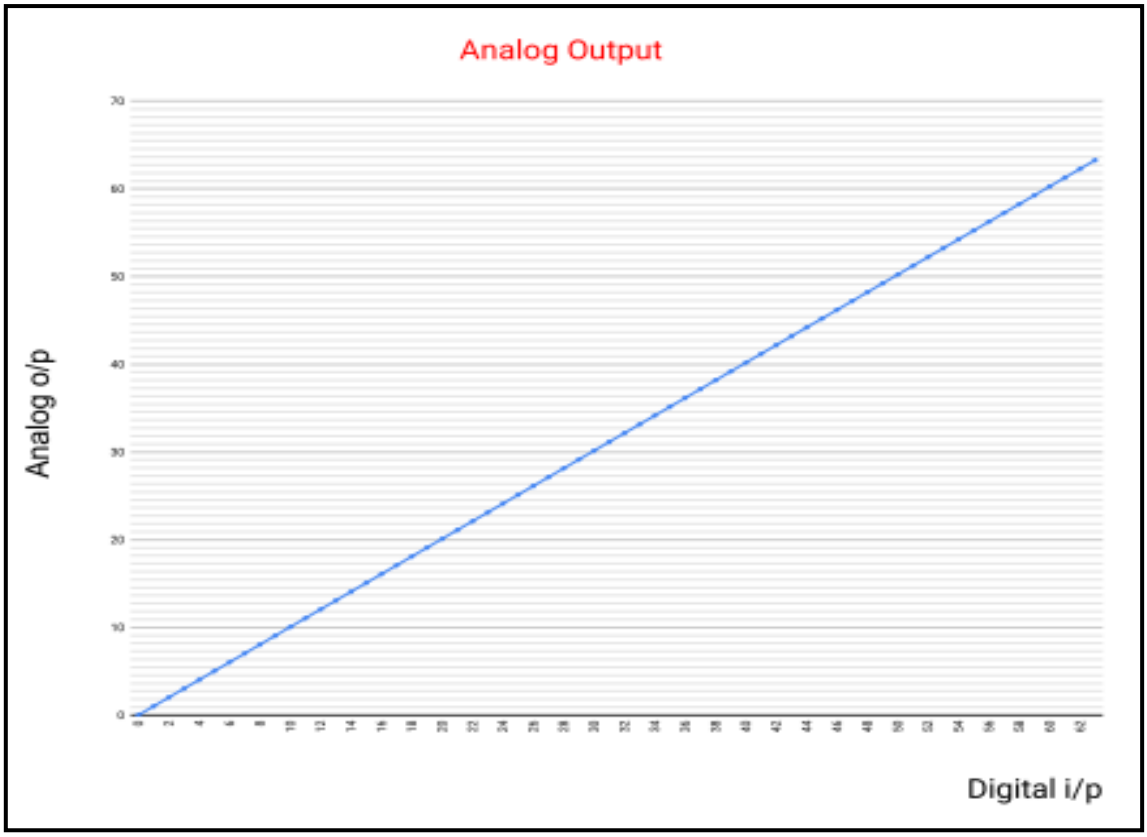


FIG 7.6 Analog Output of DAC

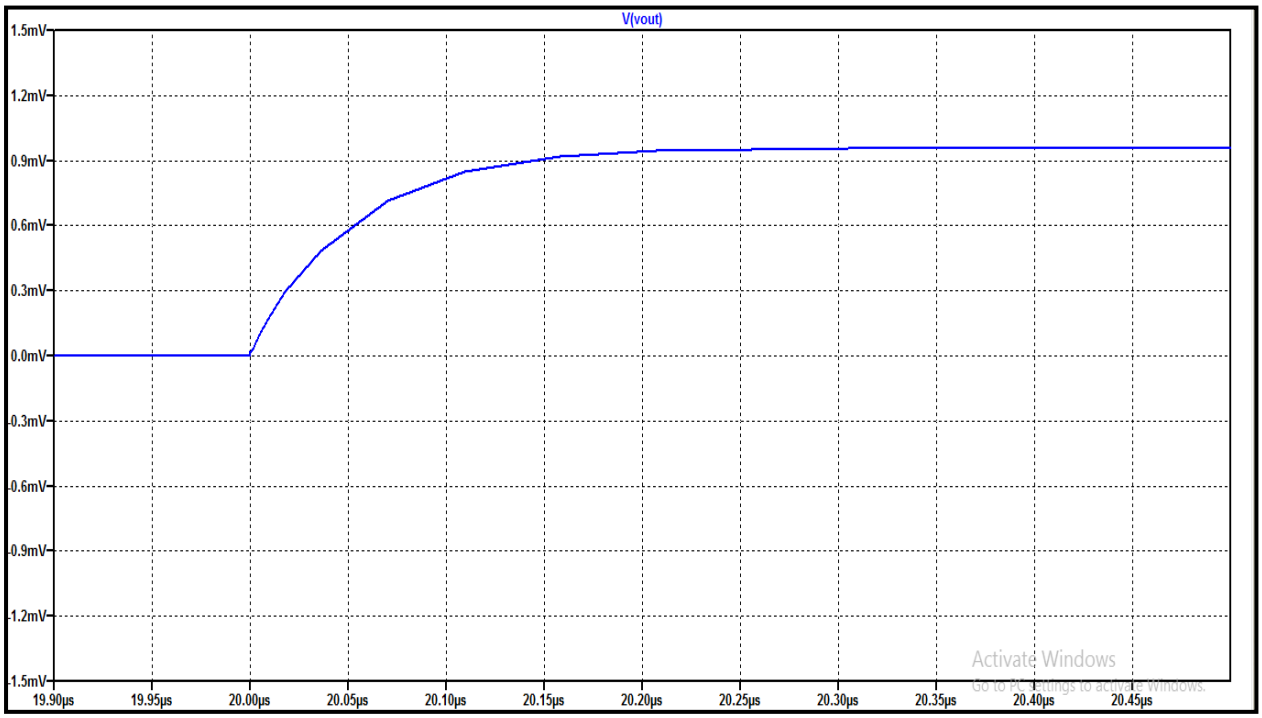


FIG 7.7 Simulation showing Code to Code Output Settling Time
(R_L = 10kΩ, C_L = 100pF)

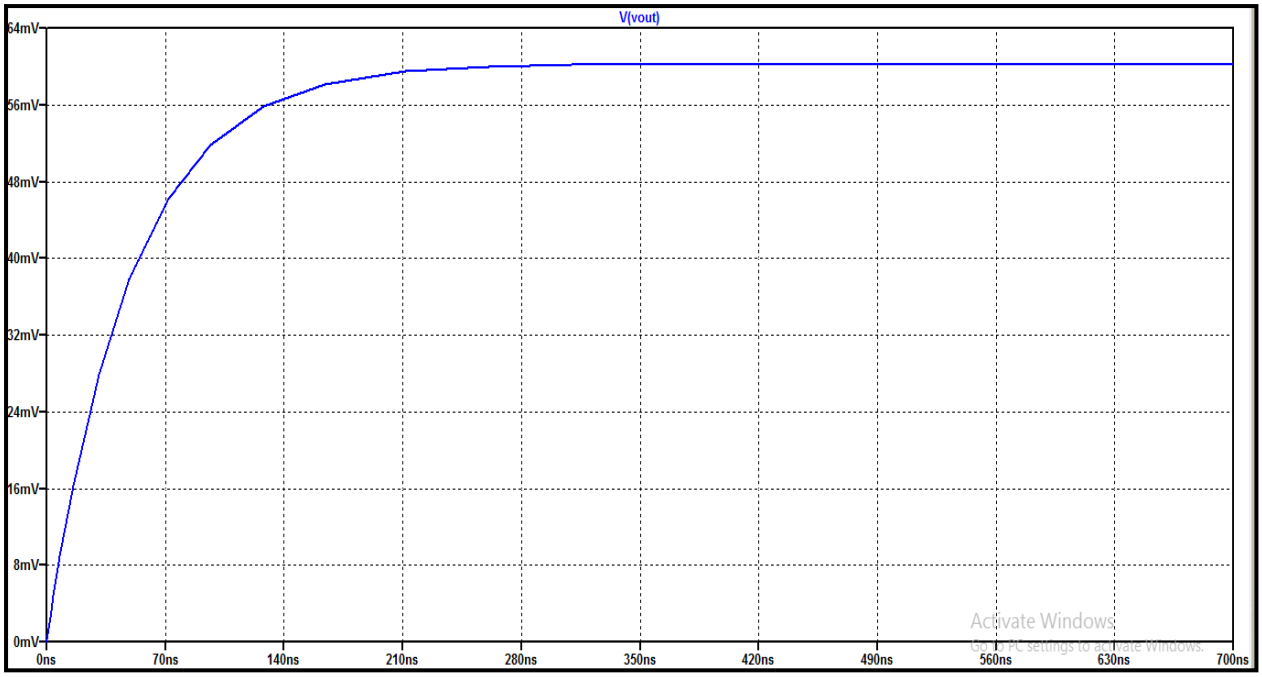


FIG 7.8 Simulation showing Full Scale Output Settling Time
(R_L = 10kΩ, C_L = 100pF)

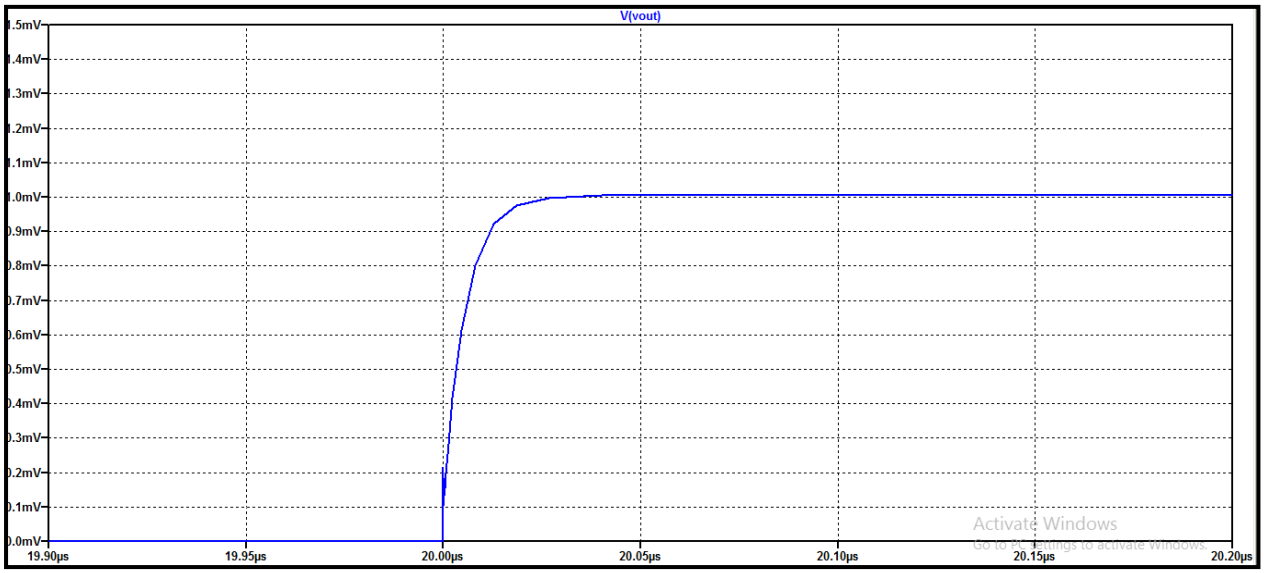


FIG 7.9 Simulation showing Code to Code Output Settling Time
(C_L = 10pF)

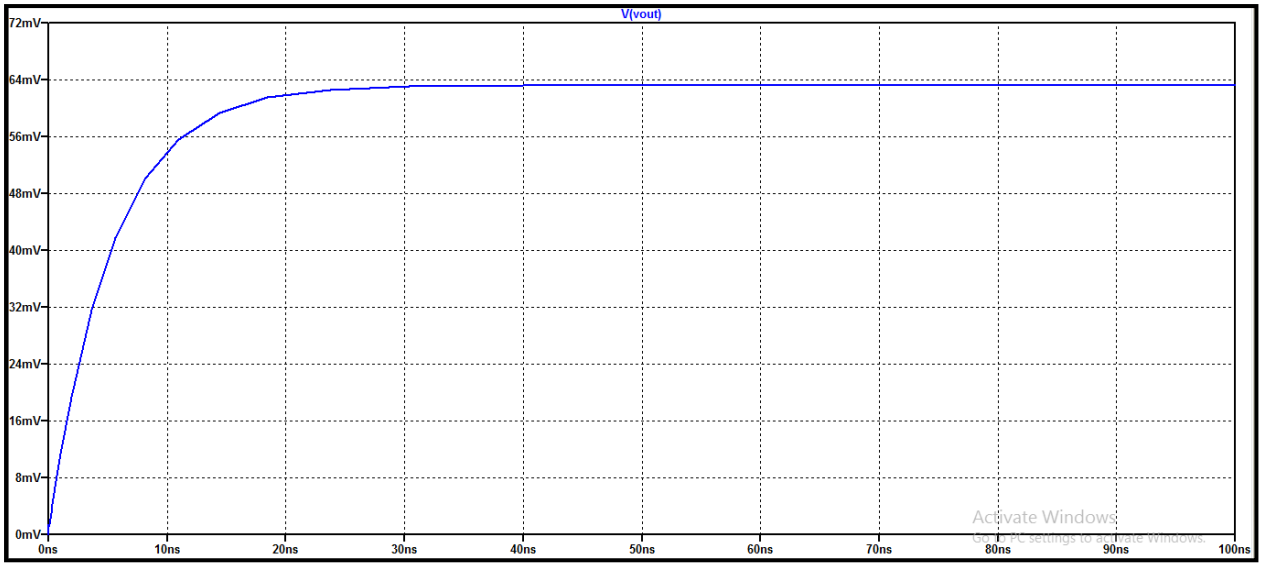


FIG 7.10 Simulation showing Full Scale Output Settling Time (C_L = 10pF)

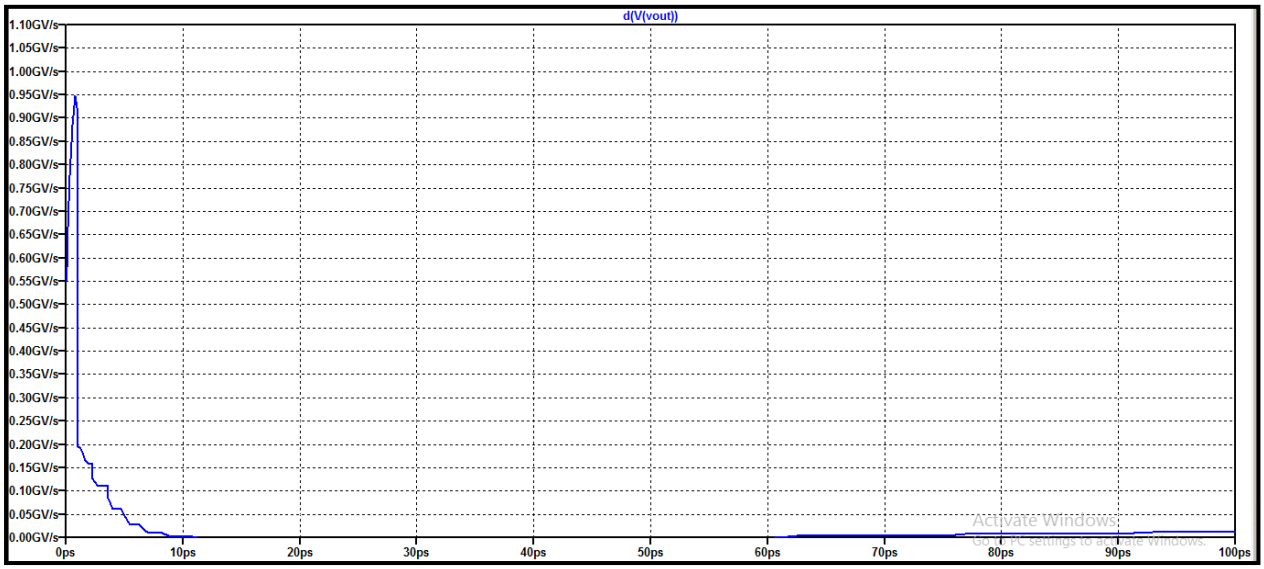


FIG 7.11 Simulation Showing Slew Rate (C_L = 10pF)

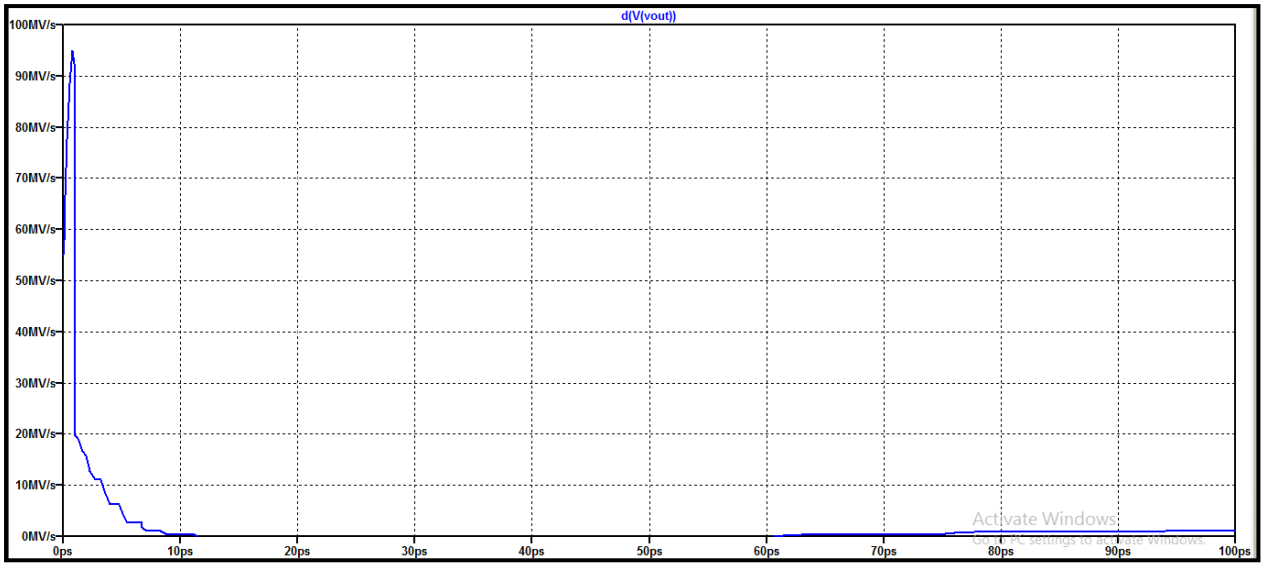


FIG 7.12 Simulation Showing Slew Rate (R_L = 10kΩ, C_L = 100pF)

ELECTRICAL CHARACTERISTICS OF 3 BIT COARSE DAC

TABLE 7.6

POWER SUPPLY		
Power supply current, IDD	0.194mA	
Power supply rejection ratio, PSRR	Zero scale	-153dB(±0.2V VDD variation)
	Full scale	-41.87dB(±0.2V VDD variation)
Power consumption	0.5508mW	

TABLE 7.7

STATIC DAC SPECIFICATIONS	
Resolution	64mV
Integral Non-Linearity, INL	0.284LSB
Differential Non-Linearity, DNL	0.144LSB
Zero-scale error(offset error at zero scale)	1.747×10^{-6} LSB
Gain error	0.0403

TABLE 7.8

OUTPUT SPECIFICATIONS			
Parameter	Test Conditions	Rated voltage	Full scale voltage
Output load regulation accuracy	R_L = 100kΩ	31.94%	24.21%
	R_L = 1MΩ	3.19%	2.42%

TABLE 7.9

ANALOG OUTPUT DYNAMIC PERFORMANCE		
Parameter	Test Conditions	Value
Output settling time(full scale), $t_{s(FS)}$	R_L = 100kΩ, C_L = 1pF	0.19µs
	C_L = 10pF	1.97µs
Output settling time(code to code), $t_{s(CC)}$	R_L = 100kΩ, C_L = 1pF	0.19µs
	C_L = 10pF	1.6µs
Slew rate, SR	R_L = 100kΩ, C_L = 1pF	15,550V/µs
	C_L = 10pF	1560V/µs
Total harmonic distortion, THD	f_{out} = 2.083kHz R_L = 100kΩ, C_L = 100pF	-6.93dB(45.048%)

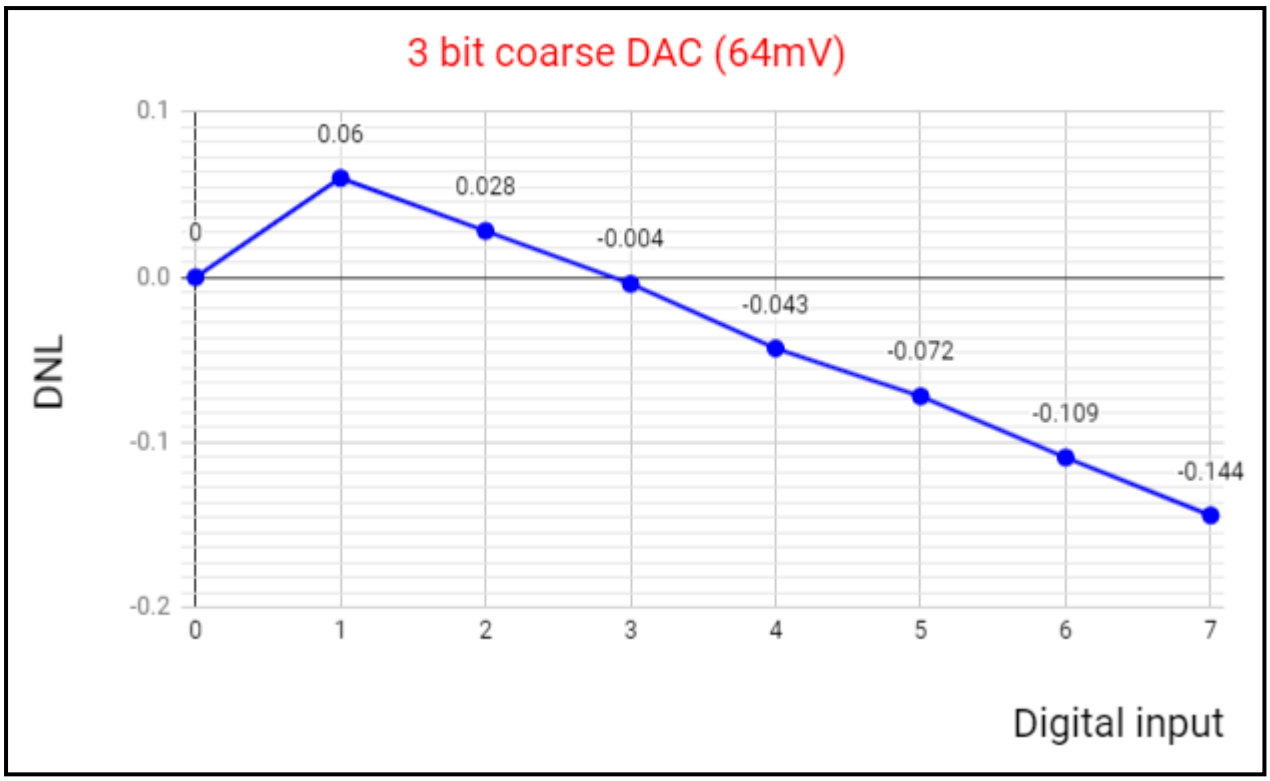


FIG 7.13 Differential Non-Linearity Error

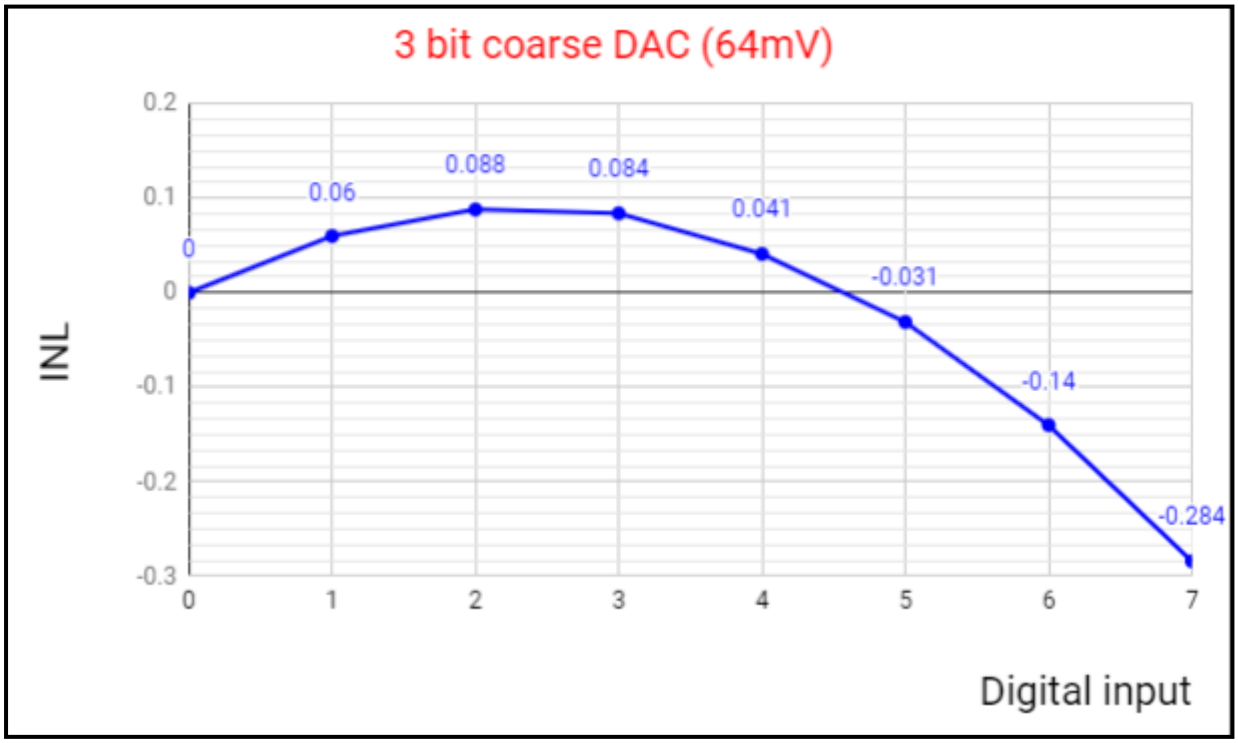


FIG 7.14 Integral Non-Linearity Error

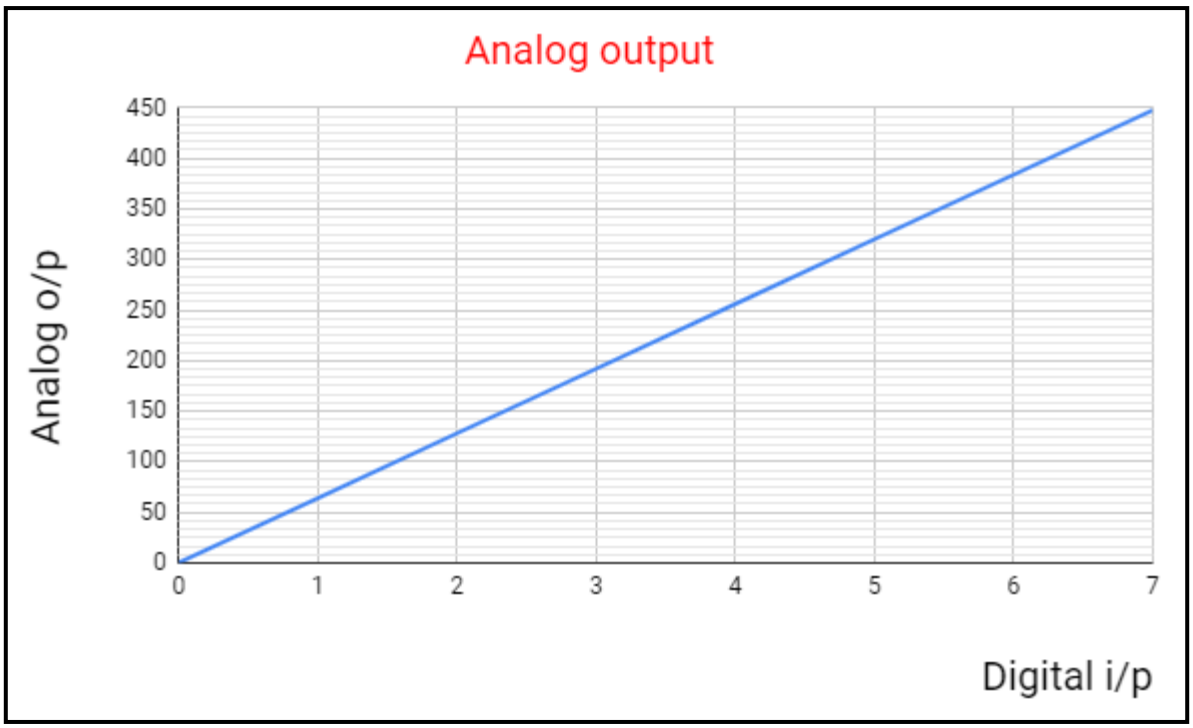


FIG 7.15 Analog Output of DAC

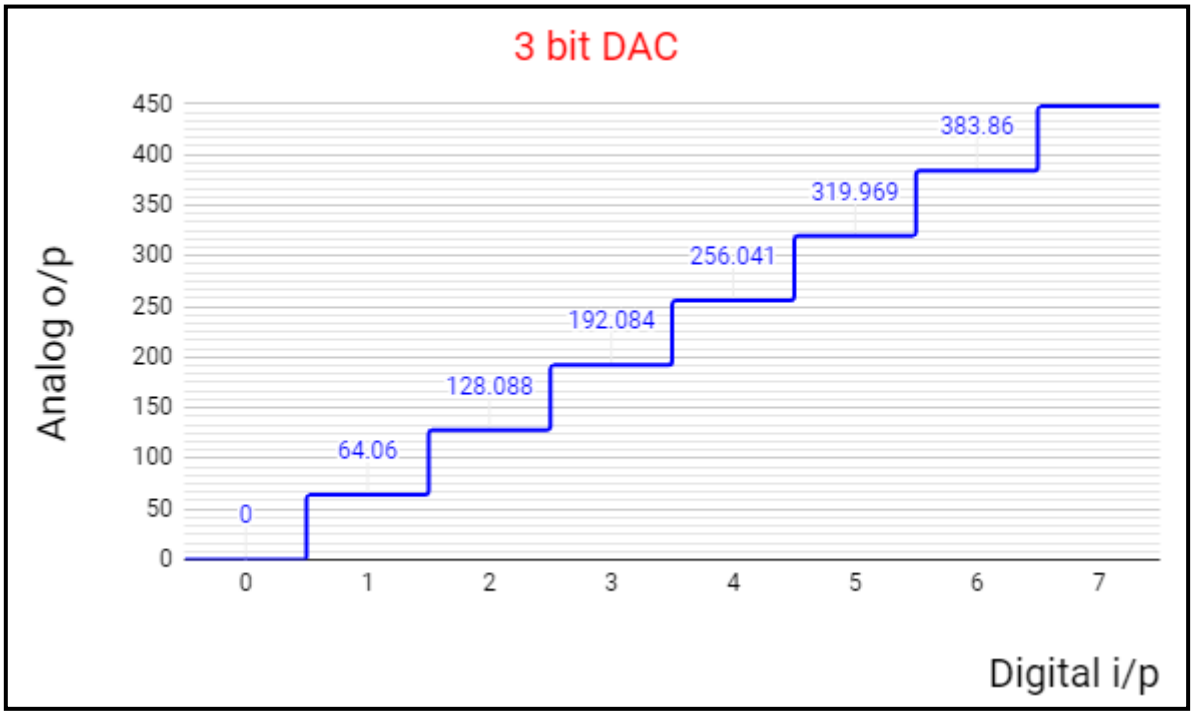


FIG 7.16 Analog Output v/s Digital Input

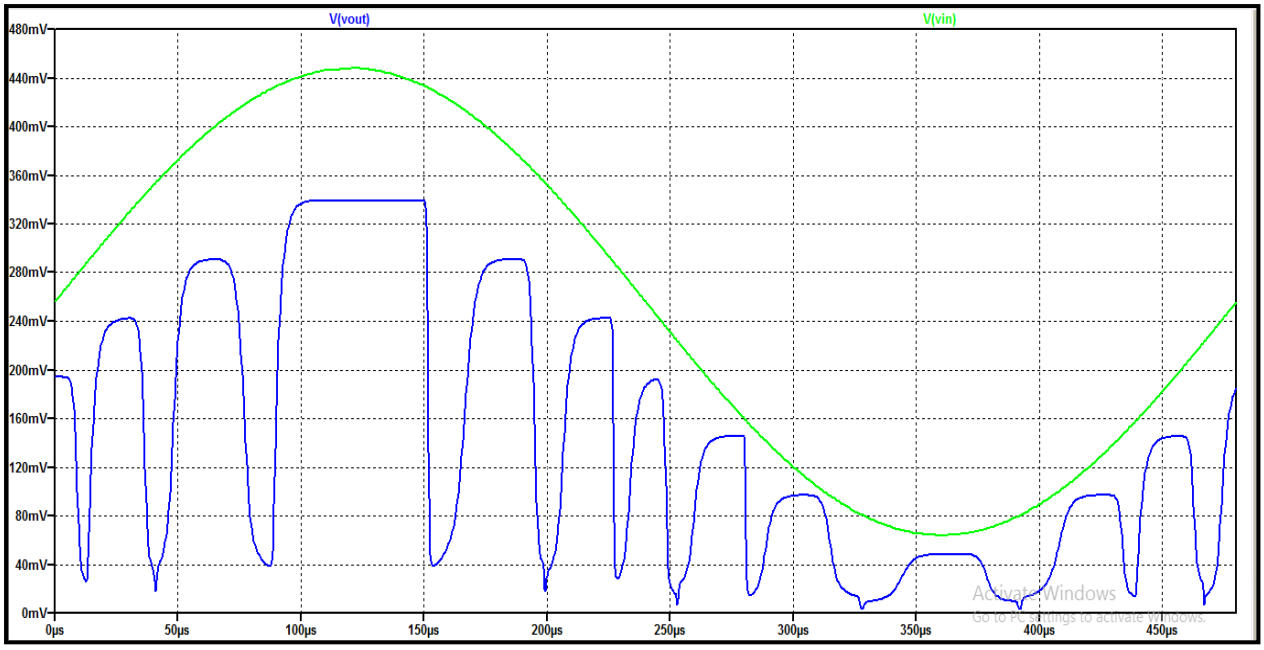


FIG 7.17 DAC Output for a Digitally Synthesized Sine Wave Input
(R_L = 100kΩ, C_L = 100pF)

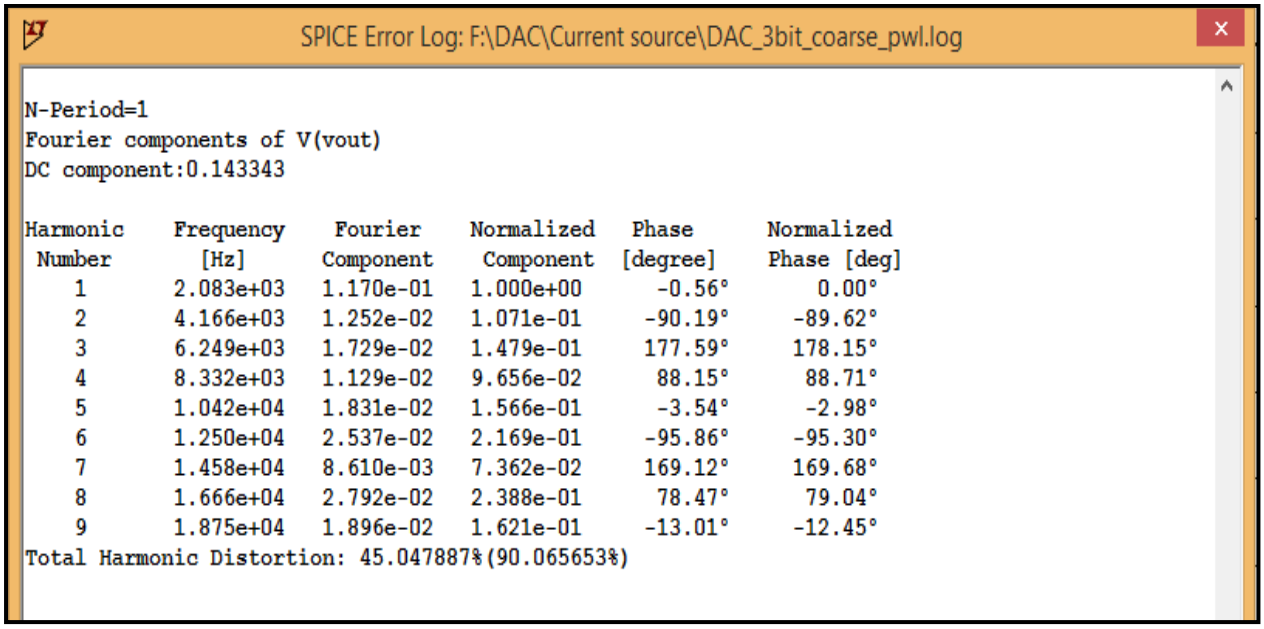


FIG 7.18 Calculating Total Harmonic Distortion (THD)
(R_L = 100kΩ, C_L = 100pF)

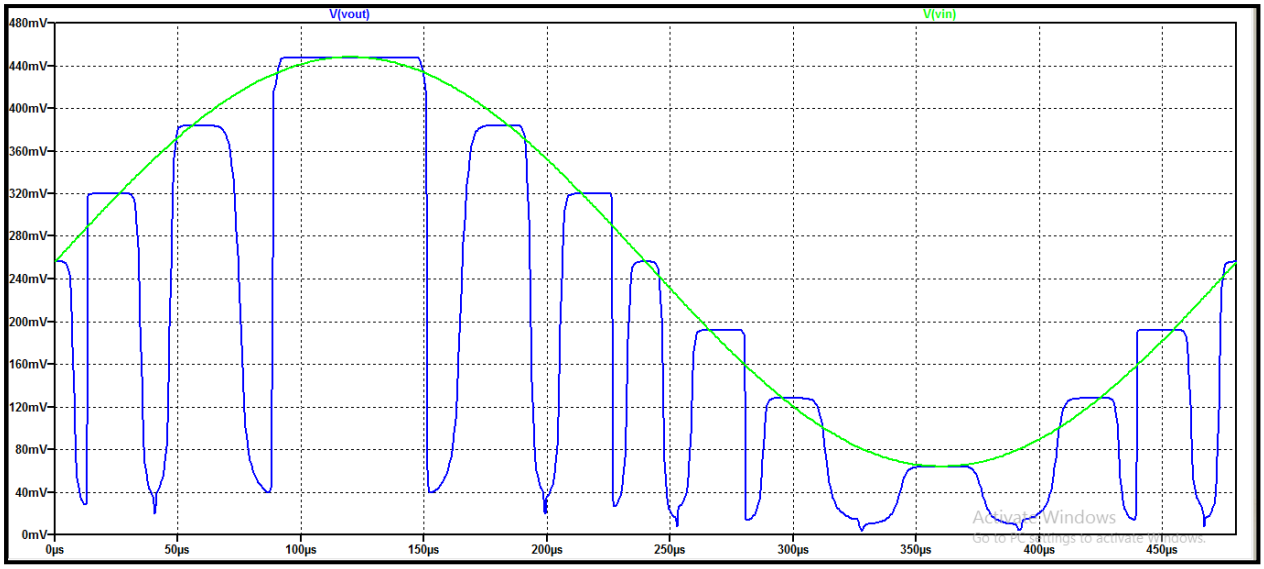


FIG 7.19 DAC Output for a Digitally Synthesized Sine Wave Input (Open Circuit Load)

SPICE Error Log: F:\DAC\Current source\DAC_3bit_coarse_pwl.log

```
N-Period=1
Fourier components of V(vout)
DC component:0.192341

Harmonic     Frequency     Fourier     Normalized    Phase      Normalized
 Number        [Hz]       Component     Component   [degree]    Phase [deg]
    1        2.083e+03    1.567e-01    1.000e+00       0.22°       0.00°
    2        4.166e+03    1.315e-02    8.396e-02     -88.12°     -88.33°
    3        6.249e+03    2.375e-02    1.516e-01    -178.87°    -179.09°
    4        8.332e+03    1.677e-02    1.070e-01      91.90°      91.69°
    5        1.042e+04    2.457e-02    1.568e-01       1.37°       1.15°
    6        1.250e+04    3.336e-02    2.129e-01     -88.90°     -89.11°
    7        1.458e+04    6.901e-03    4.405e-02    -178.29°    -178.50°
    8        1.666e+04    3.627e-02    2.315e-01      89.75°      89.54°
    9        1.875e+04    2.638e-02    1.684e-01      -0.50°      -0.72°
Total Harmonic Distortion: 44.194008%(94.962446%)
```

FIG 7.20 Calculating Total Harmonic Distortion (THD) (Open Circuit Load)

In the above simulation, THD for the 3 bit coarse DAC comes out to be 44.2%(open circuit load) which is large as compared to the THD for the 6 bit fine DAC(1.15%). This is because the number of discrete points, M in the synthesis of the sine wave has much influence on the THD. When M = 63(taken for 6 bit), THD = 1.15% and when M = 7(taken for 3 bit), THD = 44.2%.

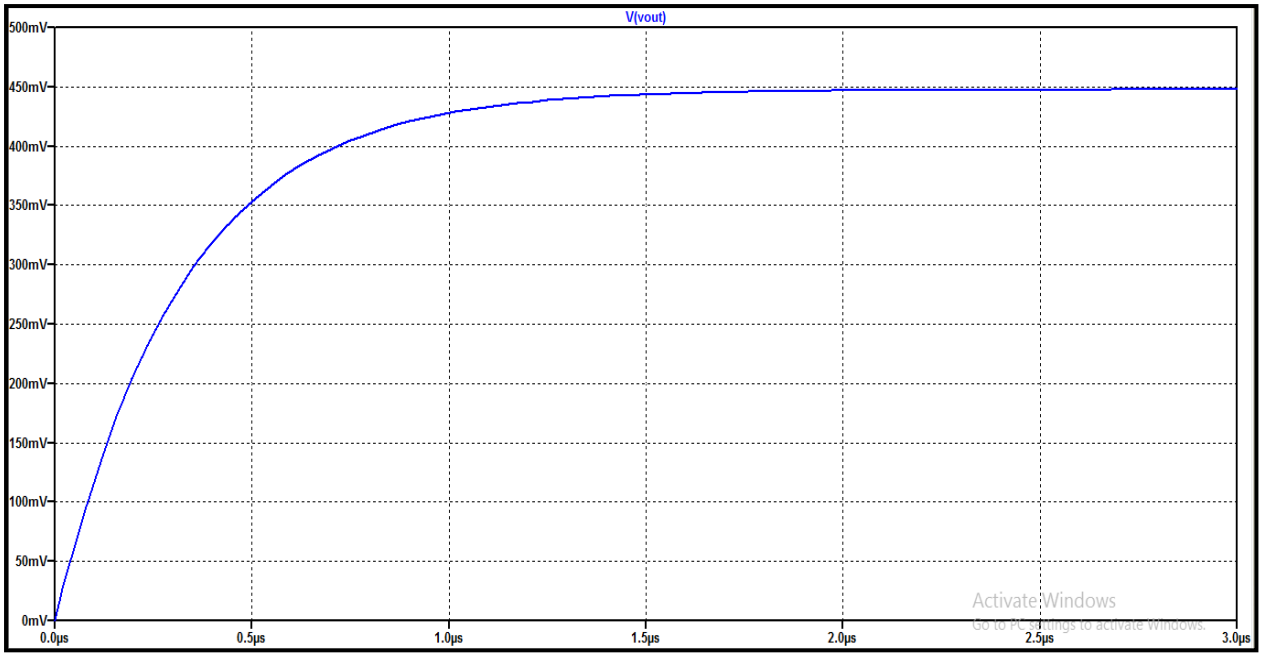


FIG 7.21 Simulation showing Full Scale Output Settling Time (C_L = 10pF)

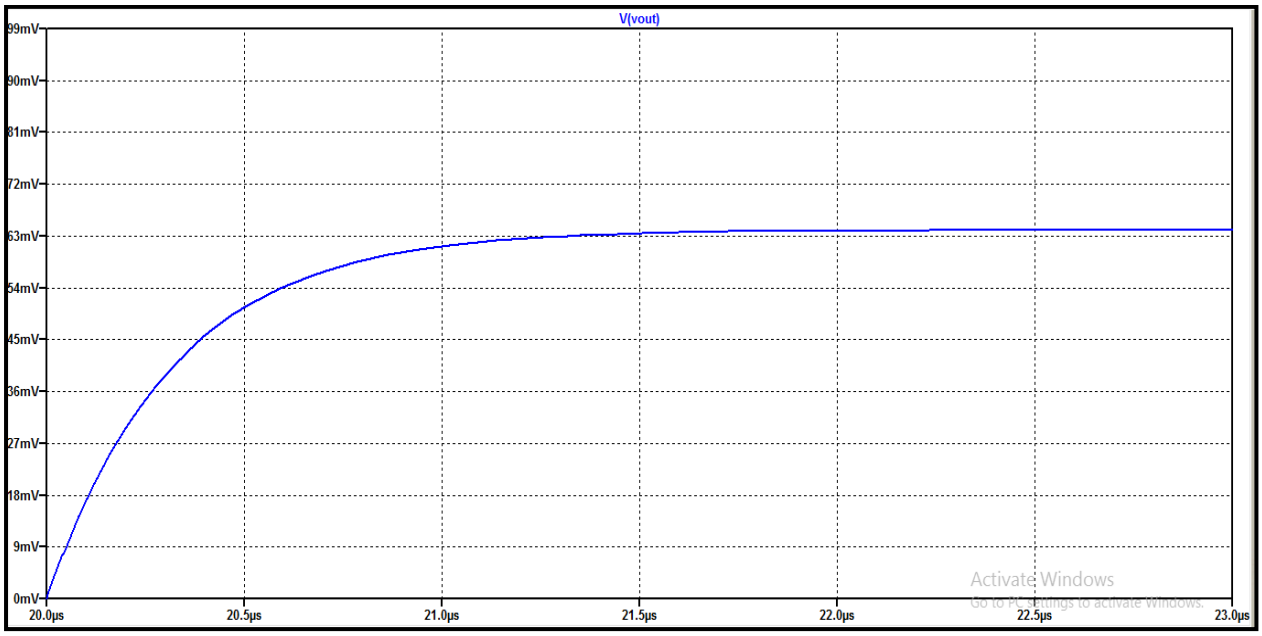


FIG 7.22 Simulation showing Code to Code Output Settling Time (C_L = 10pF)

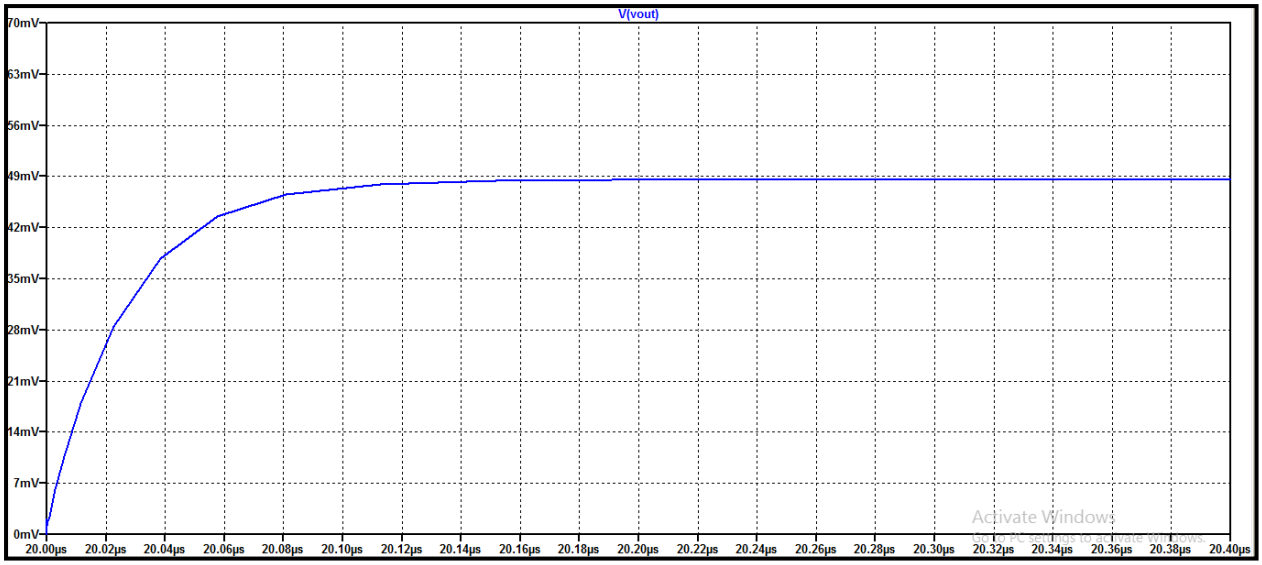


FIG 7.23 Simulation showing Code to Code Output Settling Time
(R_L = 100kΩ, C_L = 1pF)

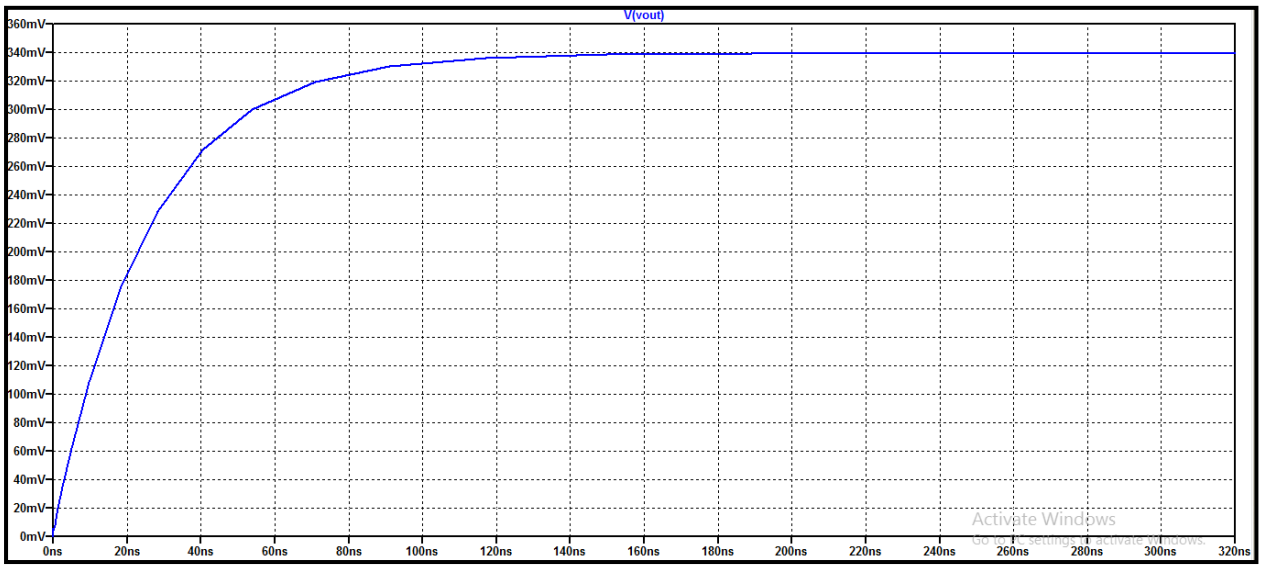


FIG 7.24 Simulation showing Full Scale Output Settling Time
(R_L = 100kΩ, C_L = 1pF)

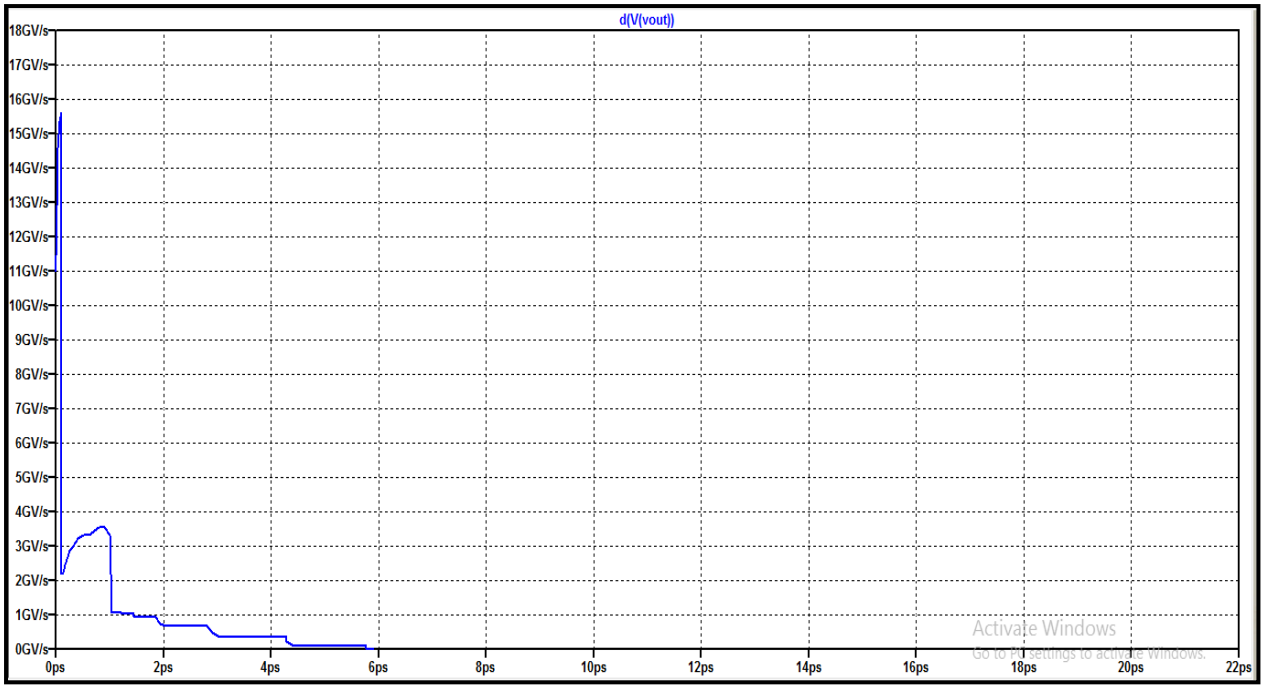


FIG 7.25 Simulation Showing Slew Rate (R_L = 100kΩ, C_L = 1pF)

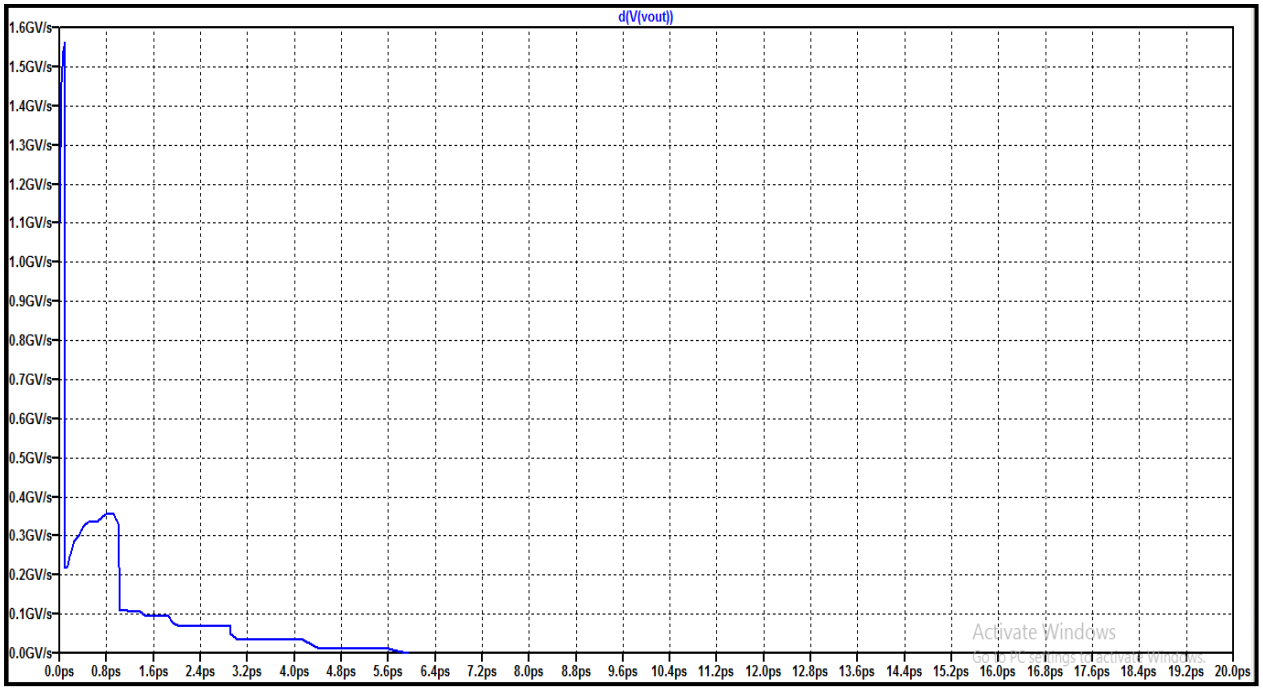


FIG 7.26 Simulation Showing Slew Rate (C_L = 10pF)

ELECTRICAL CHARACTERISTICS OF COMBINED 9 BIT DAC (USING BUFFER)

The characteristics obtained for the 9 bit DAC by combining the 3 bit coarse and the 6 bit fine DACs (as discussed above), isolated by an ideal buffer stage, are listed below in tabular form.

TABLE 7.10

POWER SUPPLY		
Power supply current, IDD	0.32mA	
Power supply rejection ratio, PSRR	Zero scale	-114dB(±0.2V VDD variation)
	Full scale	-79.09dB(±0.2V VDD variation)
Power consumption	0.576mW	

TABLE 7.11

STATIC DAC SPECIFICATIONS	
Resolution	1mV
Integral Non-Linearity, INL	0.354LSB
Differential Non-Linearity, DNL	0.41LSB
Zero-scale error(offset error at zero scale)	9.862×10^{-6} LSB
Gain error	0.000555

TABLE 7.12

OUTPUT SPECIFICATIONS			
Parameter	Test Conditions	Rated voltage	Full scale voltage
Output load regulation accuracy	R_L = 10kΩ	5%	4.76%
	R_L = 100kΩ	0.5%	0.476%

TABLE 7.13

ANALOG OUTPUT DYNAMIC PERFORMANCE		
Parameter	Test Conditions	Value
Output settling time(full scale), $t_{s(FS)}$	R_L = 100kΩ, C_L = 10pF	0.12µs
	C_L = 100pF	0.319µs
Output settling time(code to code), $t_{s(CC)}$	R_L = 100kΩ, C_L = 10pF	0.024µs
	C_L = 100pF	0.254µs
Slew rate, SR	R_L = 100kΩ, C_L = 10pF	18.82V/µs
	C_L = 100pF	4.831V/µs
Total harmonic distortion, THD	f_{out} = 0.9804kHz R_L = 100kΩ, C_L = 100pF	-41.17dB(0.874%)

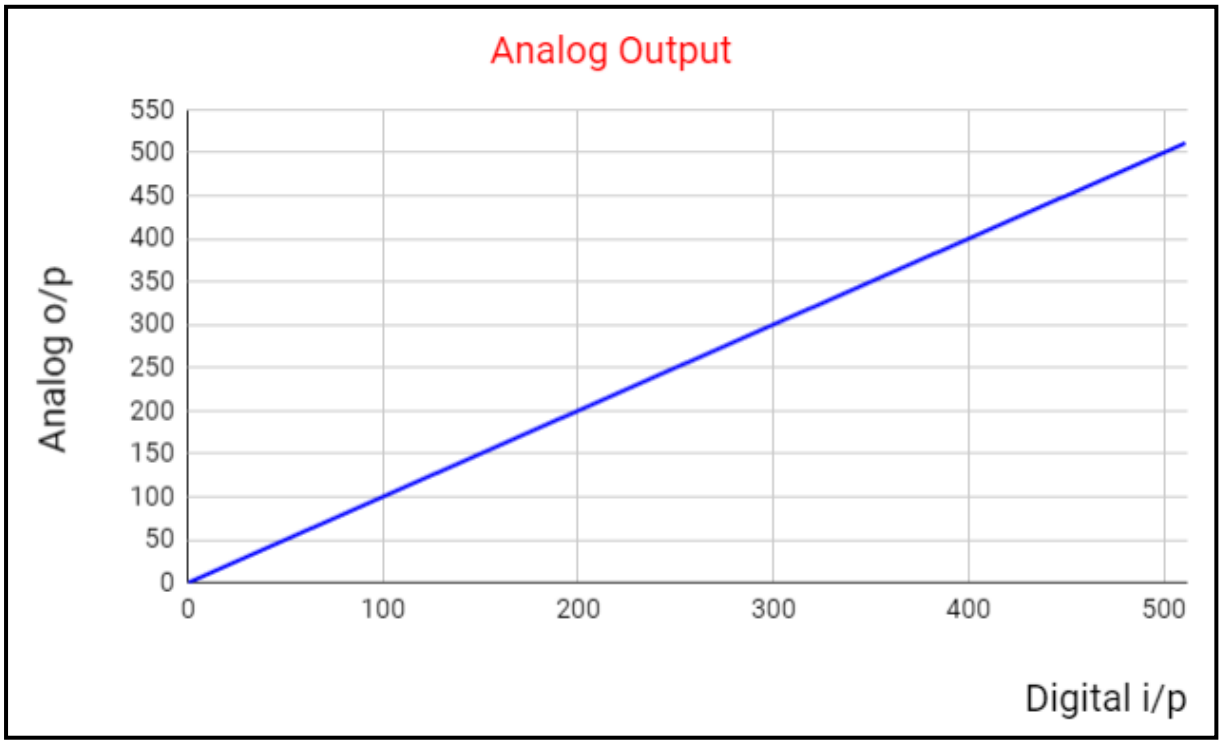


FIG 7.27 Analog Output of DAC

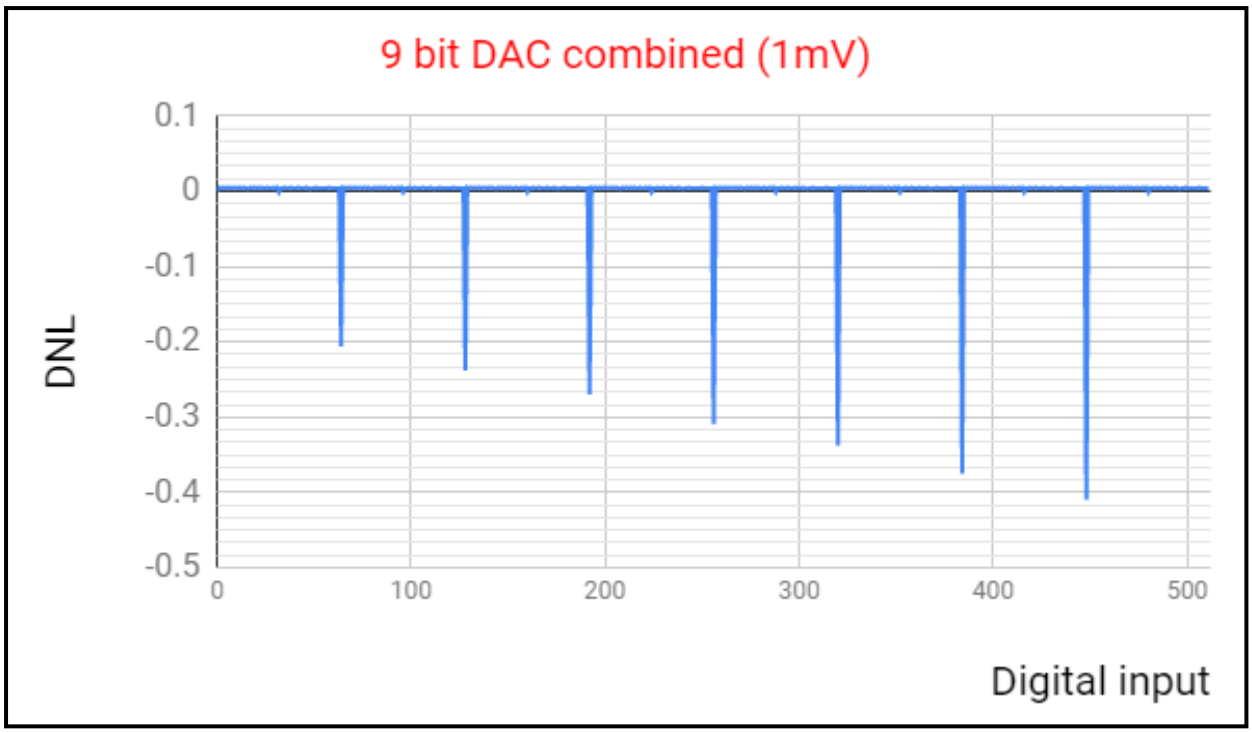


FIG 7.28 Differential Non-Linearity Error

For the combined DAC architecture, it is observed that the maximum DNL error occurs at the points of transition of coarse DAC. As such the DNL obtained is 0.41LSB. FIG 7.29 below shows a zoomed version of the above figure for digital inputs ranging from 0 to 100.

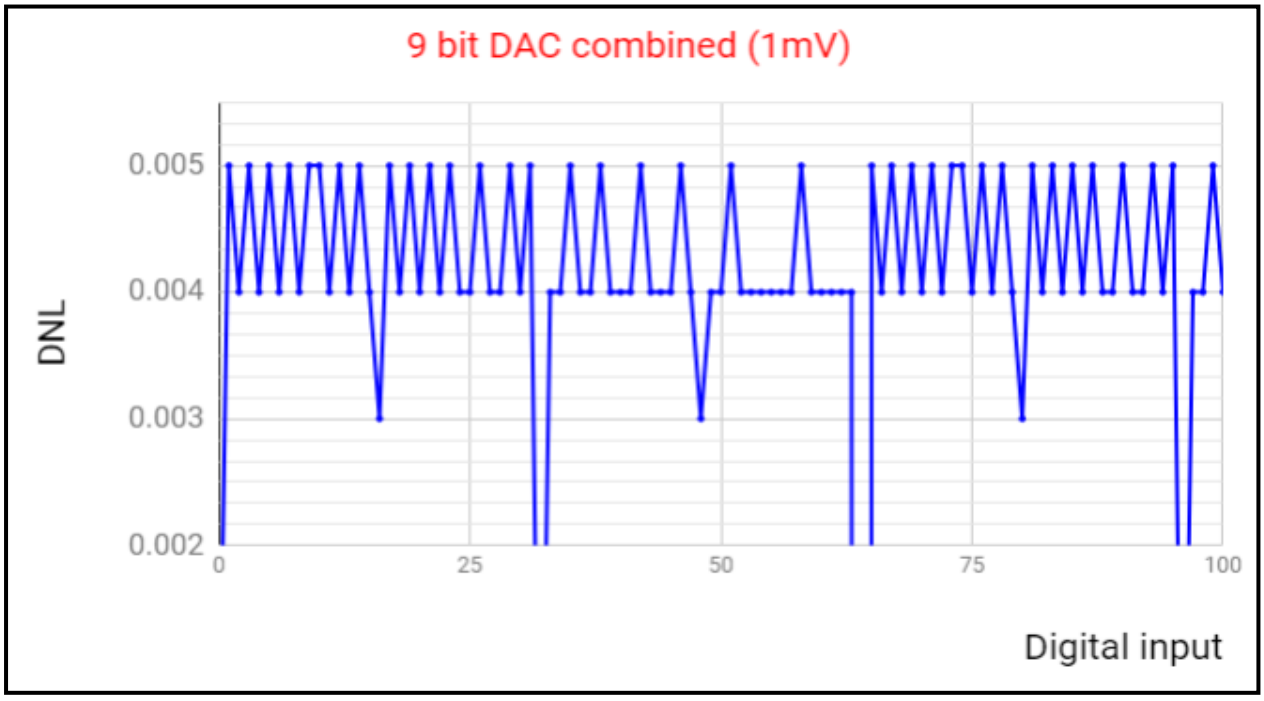


FIG 7.29 Differential Non-Linearity Error
(Zoomed Version)

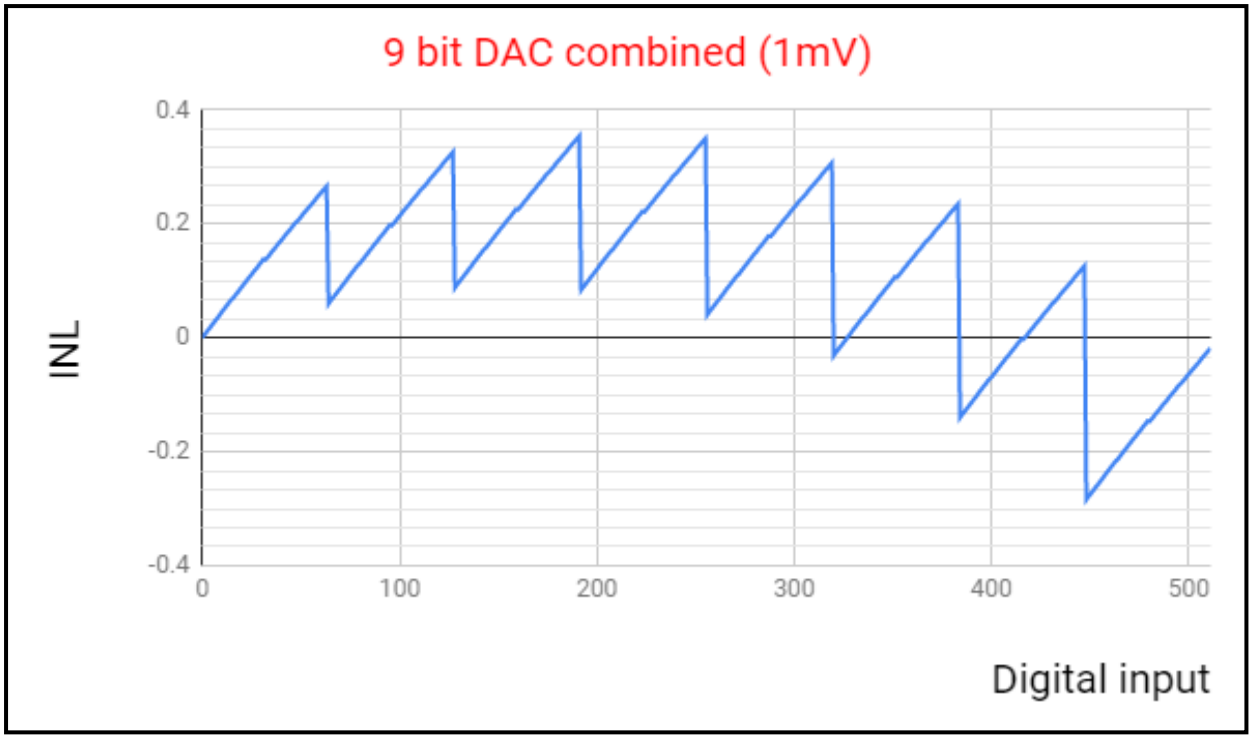


FIG 7.30 Integral Non-Linearity Error

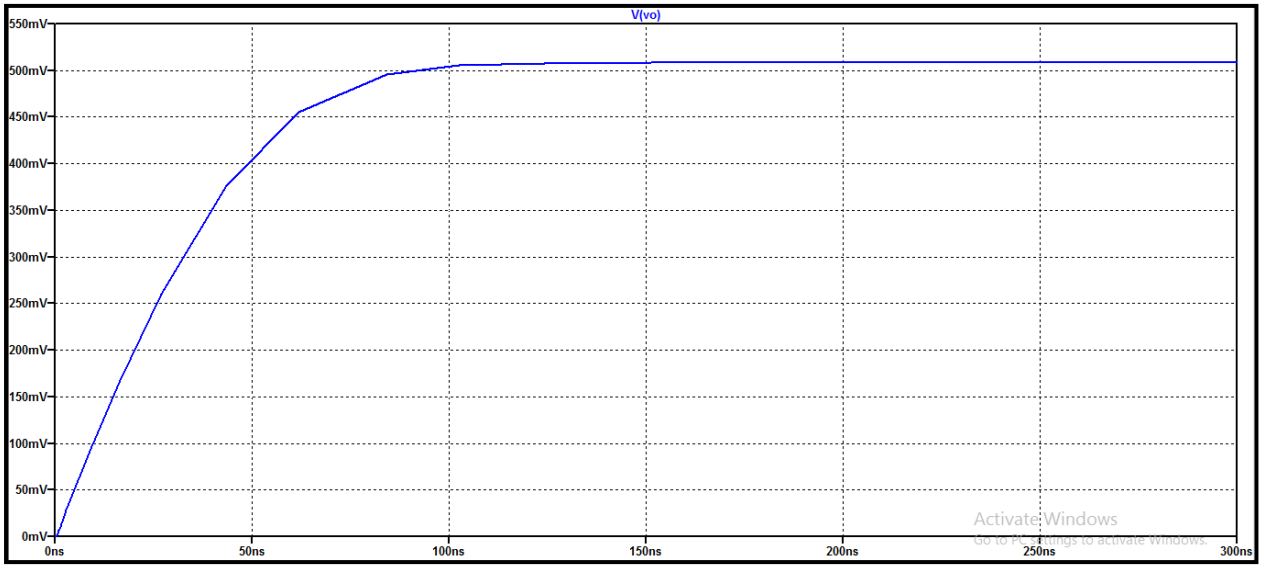


FIG 7.31 Simulation showing Full Scale Output Settling Time
(R_L = 100kΩ, C_L = 10pF)

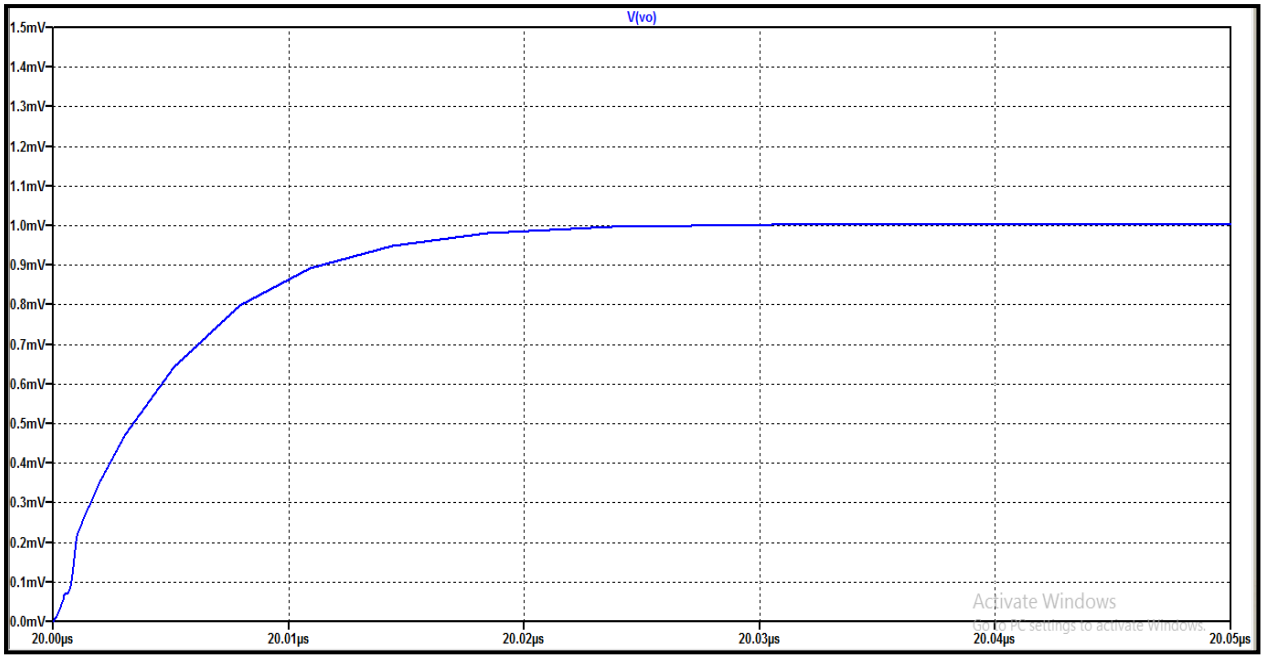


FIG 7.32 Simulation showing Code to Code Output Settling Time (R_L = 100kΩ, C_L = 10pF)

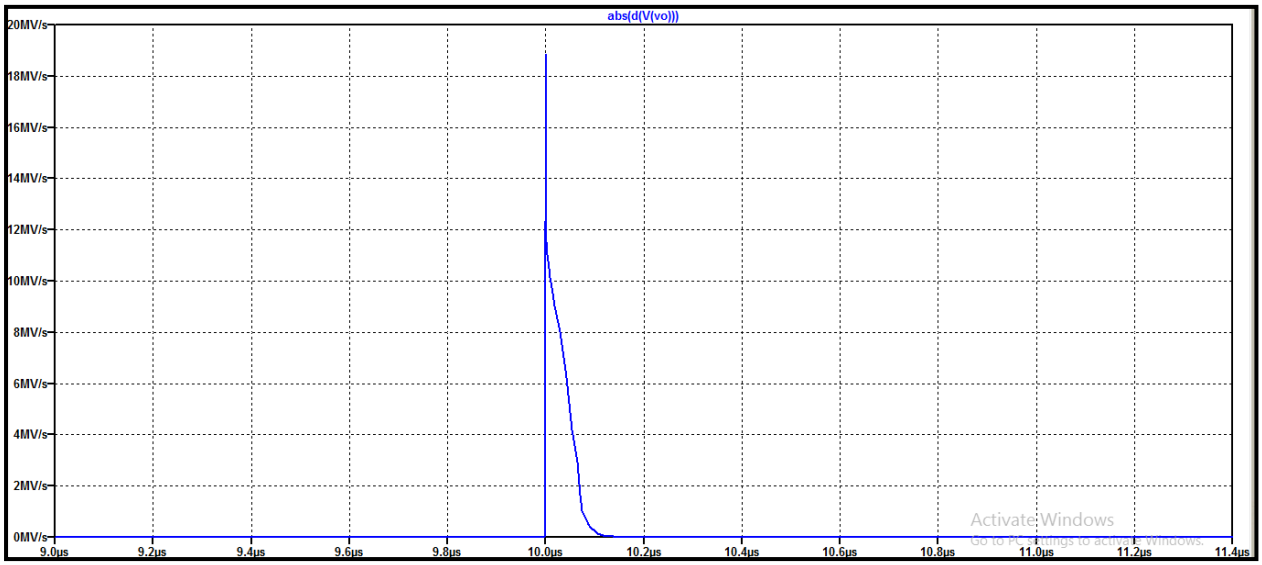


FIG 7.33 Simulation Showing Slew Rate (R_L = 100kΩ, C_L = 10pF)

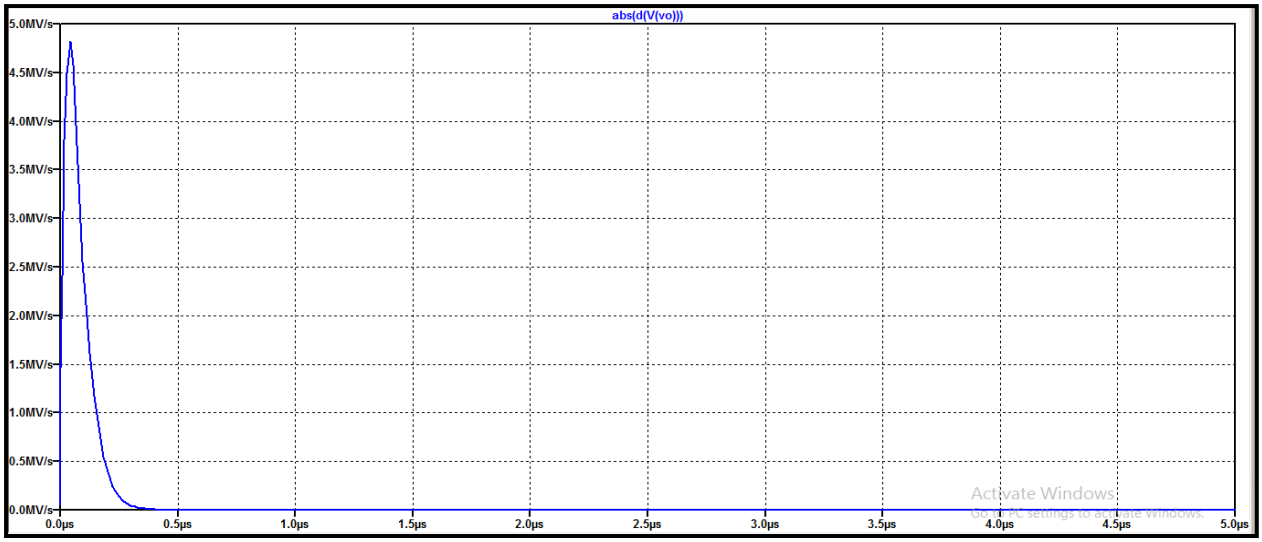


FIG 7.34 Simulation Showing Slew Rate (C_L = 100pF)

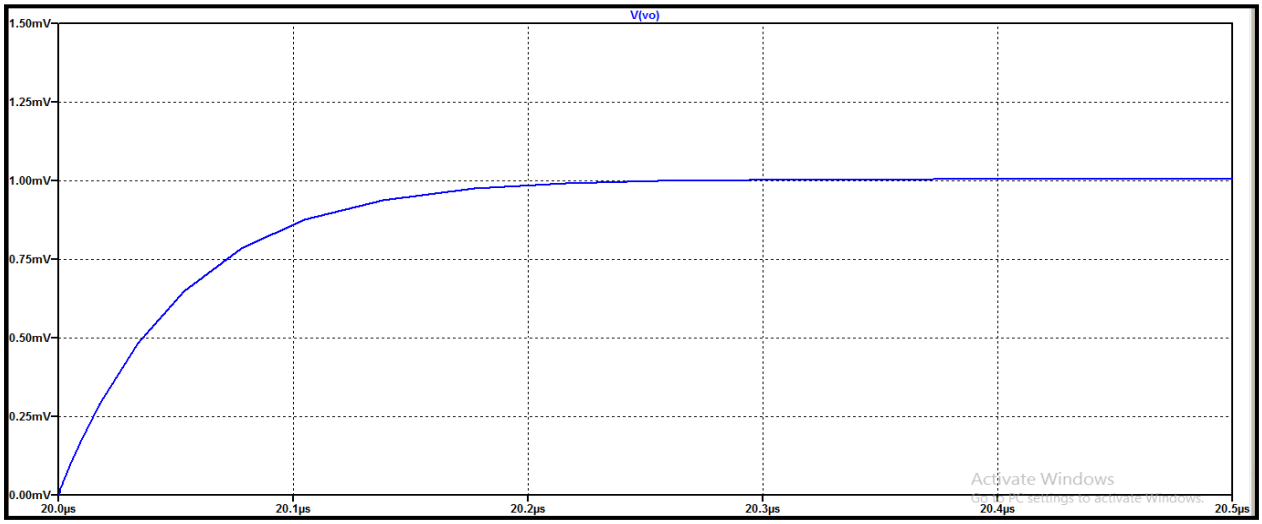


FIG 7.35 Simulation showing Code to Code Output Settling Time (C_L = 100pF)

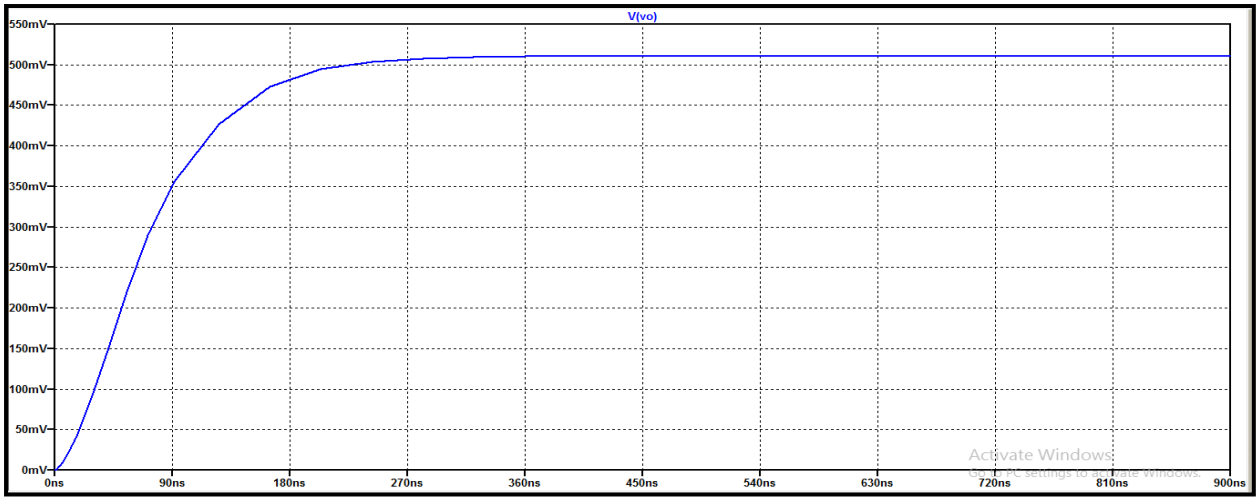


FIG 7.36 Simulation showing Full Scale Output Settling Time (C_L = 100pF)

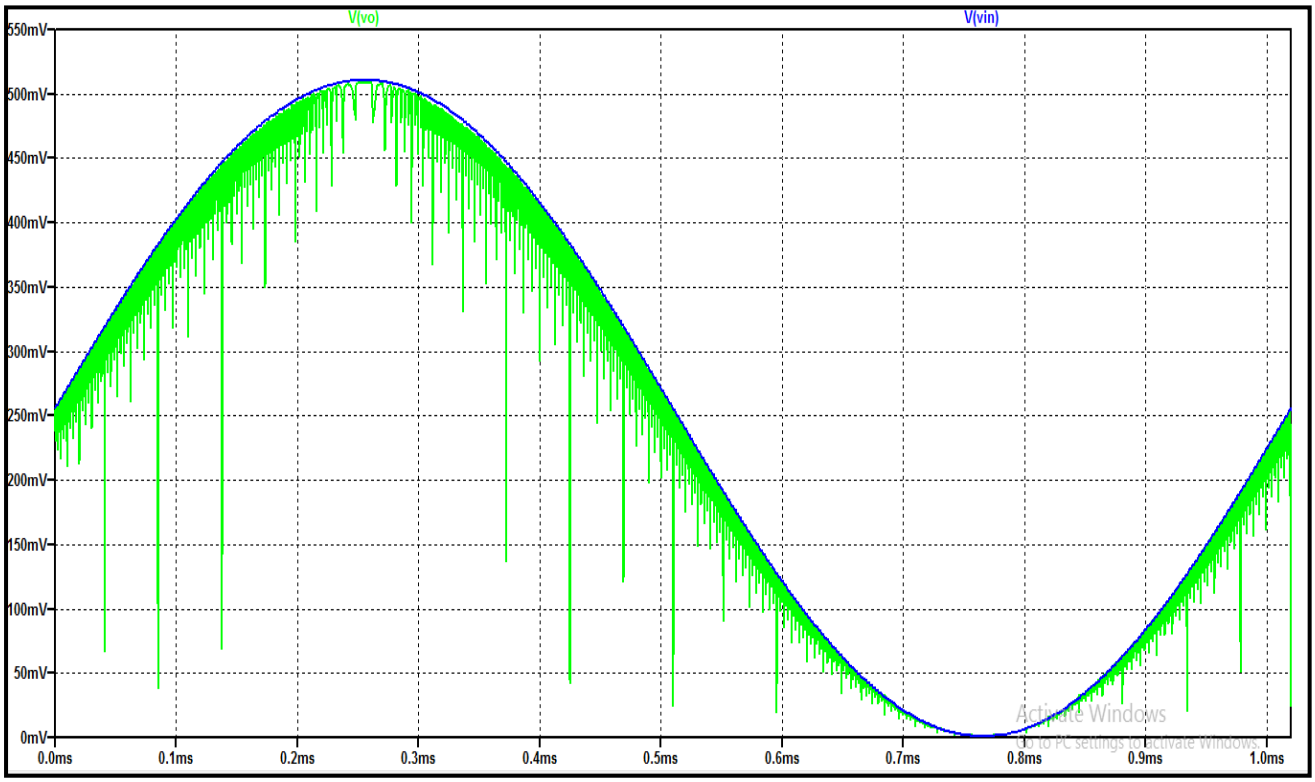


FIG 7.37 Calculating Total Harmonic Distortion (THD)
(R_L = 100kΩ, C_L = 100pF)

SPICE Error Log: F:\DAC\Current source\fine_coarse_comb.log

```
N-Period=1
Fourier components of V(vo)
DC component:0.249148

Harmonic     Frequency     Fourier     Normalized    Phase      Normalized
 Number        [Hz]       Component     Component   [degree]    Phase [deg]
    1       9.800e+02    2.497e-01    1.000e+00       0.03°       0.00°
    2       1.960e+03    2.020e-03    8.089e-03     -95.59°     -95.62°
    3       2.940e+03    5.591e-04    2.239e-03     178.63°     178.60°
    4       3.920e+03    4.763e-04    1.908e-03      99.28°      99.25°
    5       4.900e+03    3.036e-04    1.216e-03       5.36°       5.33°
    6       5.880e+03    1.234e-04    4.942e-04    -112.02°    -112.05°
    7       6.860e+03    1.252e-04    5.013e-04     178.43°     178.40°
    8       7.840e+03    9.988e-05    4.000e-04     106.57°     106.54°
    9       8.820e+03    1.191e-04    4.770e-04       0.44°       0.41°
Total Harmonic Distortion: 0.874303%(7.928515%)
```

FIG 7.38 Calculating Total Harmonic Distortion(THD)

ELECTRICAL CHARACTERISTICS OF COMBINED 9 BIT DAC(USING OP-AMP)

The characteristics obtained for the 9 bit DAC by summing the 3 bit coarse and the 6 bit fine DACs' responses (as discussed above) through a non-inverting operational amplifier, are listed below in tabular form.

TABLE 7.14

POWER SUPPLY		
Power supply current, IDD	0.88mA	
Power supply rejection ratio, PSRR	Zero scale	5.702dB(±0.2V VDD variation)
	Full scale	-43.715dB(±0.2V VDD variation)
Power consumption	1.584mW	

TABLE 7.15

STATIC DAC SPECIFICATIONS	
Resolution	1mV
Integral Non-Linearity, INL	20.21LSB
Differential Non-Linearity, DNL	2.37LSB
Zero-scale error(offset error at zero scale)	9.64LSB
Gain error	0.0326

TABLE 7.16

OUTPUT SPECIFICATIONS			
Parameter	Test Conditions	Rated voltage	Full scale voltage
Output load regulation accuracy	R_L = 10kΩ	0.014%	0.014%
	R_L = 100kΩ	0.0014%	0.0014%

TABLE 7.17

ANALOG OUTPUT DYNAMIC PERFORMANCE		
Parameter	Test Conditions	Value
Output settling time(full scale), $t_{s(FS)}$	R_L = 10kΩ, C_L = 100pF	2µs
	C_L = 10pF	0.089µs
Output settling time(code to code), $t_{s(CC)}$	R_L = 10kΩ, C_L = 100pF	0.132µs
	C_L = 10pF	0.088µs
Slew rate, SR	R_L = 10kΩ, C_L = 100pF	98.92V/µs
	C_L = 10pF	130V/µs
Total harmonic distortion, THD	f_{out} = 0.9804kHz R_L = 100kΩ, C_L = 100pF	-40.74dB(0.918%)

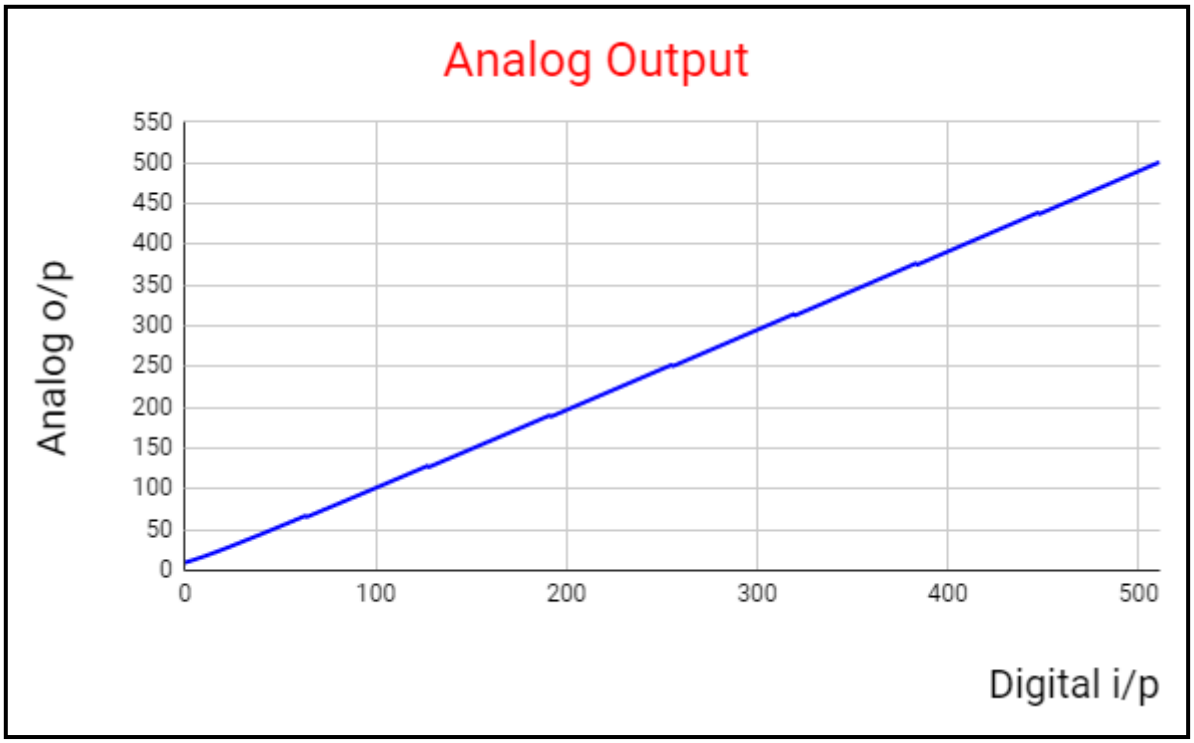


FIG 7.39 Analog Output of DAC

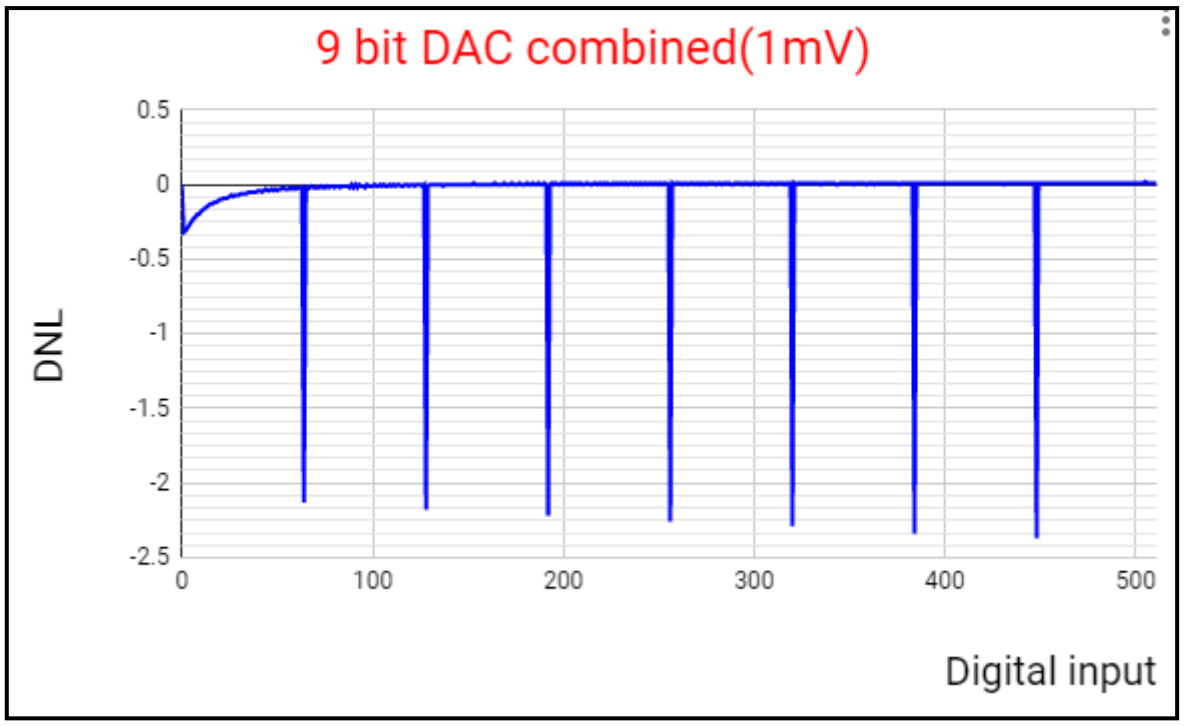


FIG 7.40 Differential Non-Linearity Error

For the combined DAC architecture, it is observed that the maximum DNL error occurs at the points of transition of coarse DAC. As such the DNL obtained is 2.37LSB. But at other points, the DNL remains between 0 and 0.3LSB with almost no differential non-linearity error at a larger number of points. FIG below shows a zoomed version of the above figure for digital inputs ranging from 100 to 200.

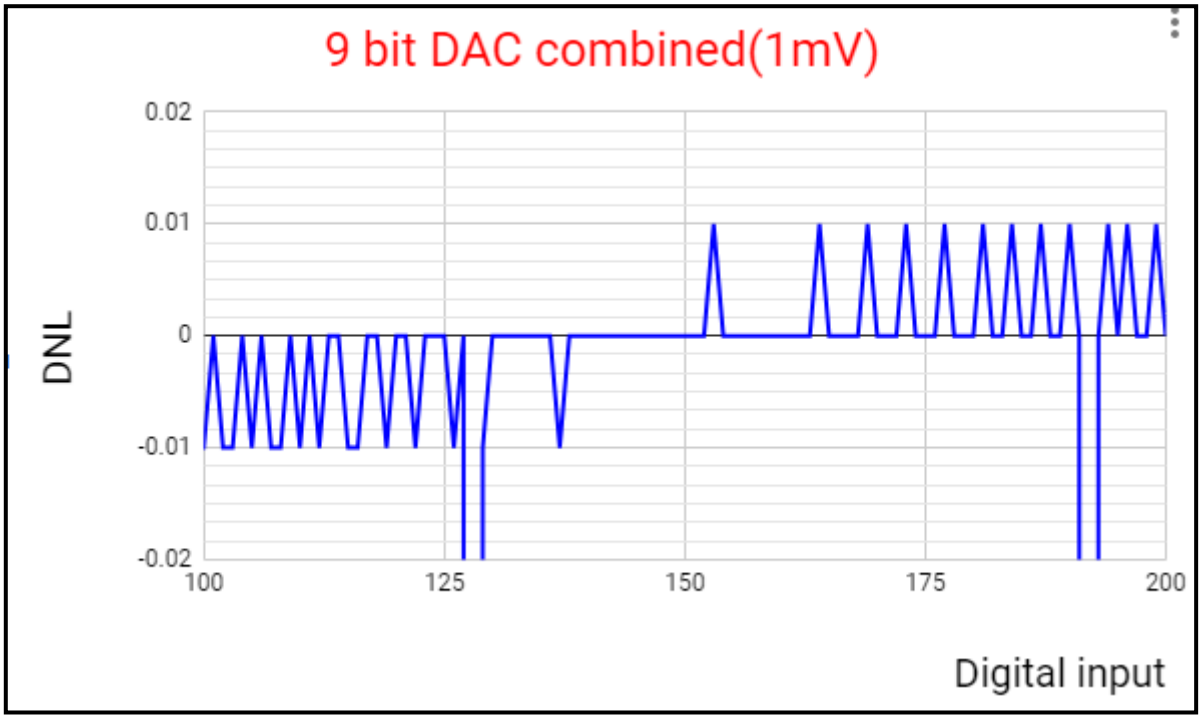


FIG 7.41 Differential Non-Linearity Error
(Zoomed Version)

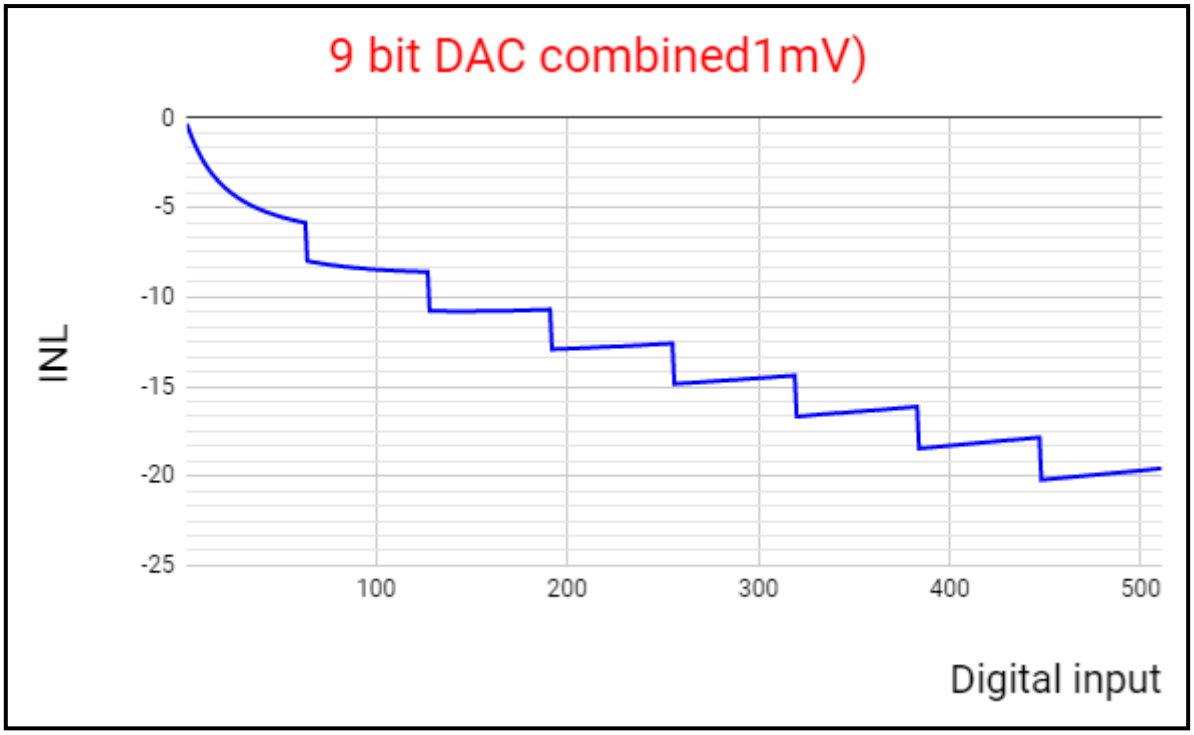


FIG 7.42 Integral Non-Linearity Error

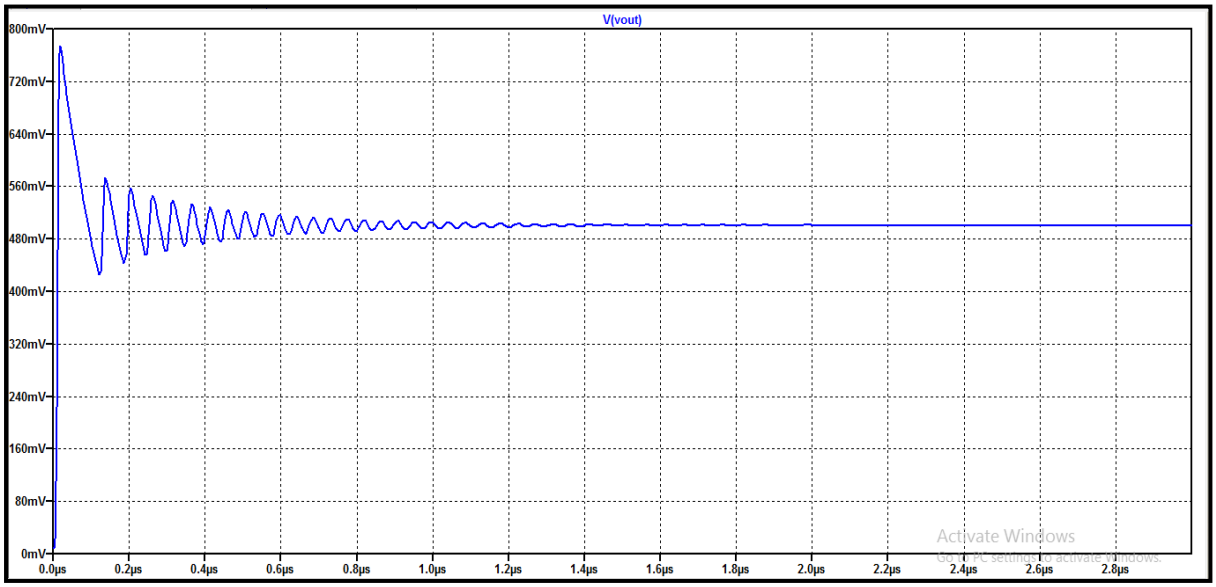


FIG 7.43 Simulation showing Full Scale Output Settling Time
(R_L = 10kΩ, C_L = 100pF)

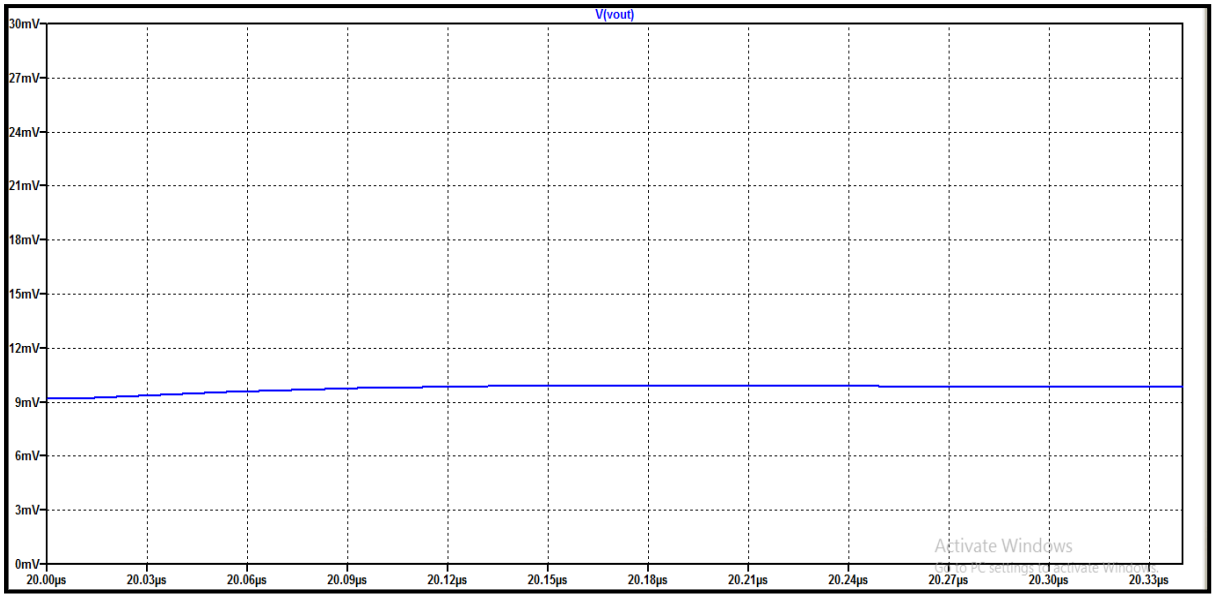


FIG 7.44 Simulation showing Code to Code Output Settling Time (R_L = 10kΩ, C_L = 100pF)

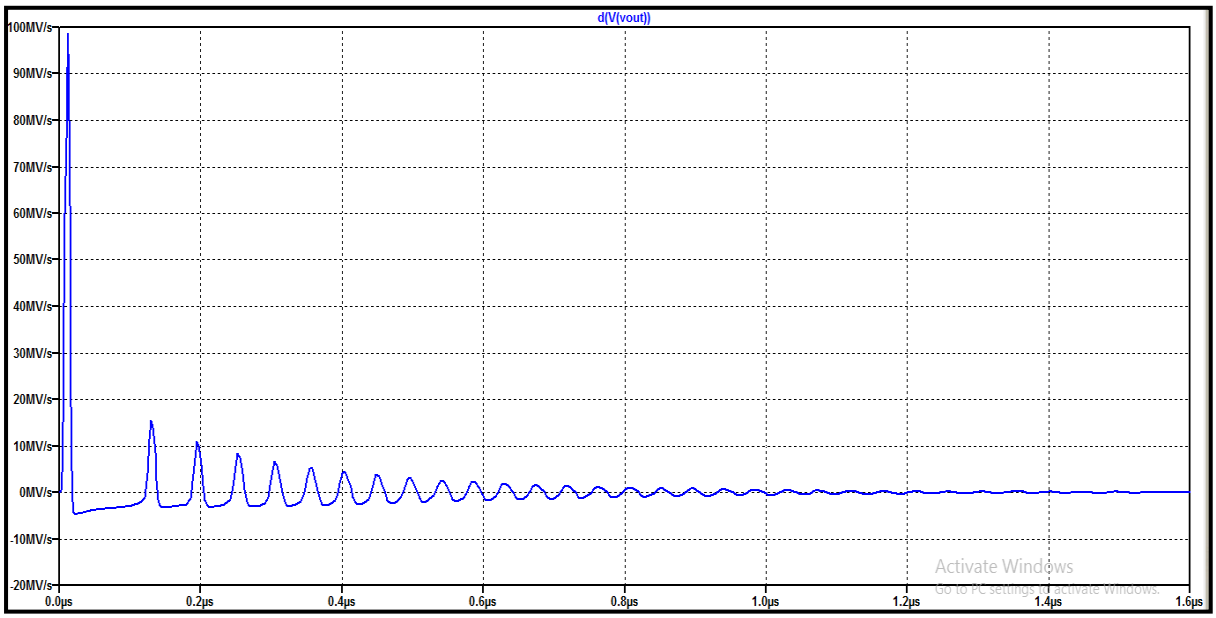


FIG 7.45 Simulation Showing Slew Rate (R_L = 10kΩ, C_L = 100pF)

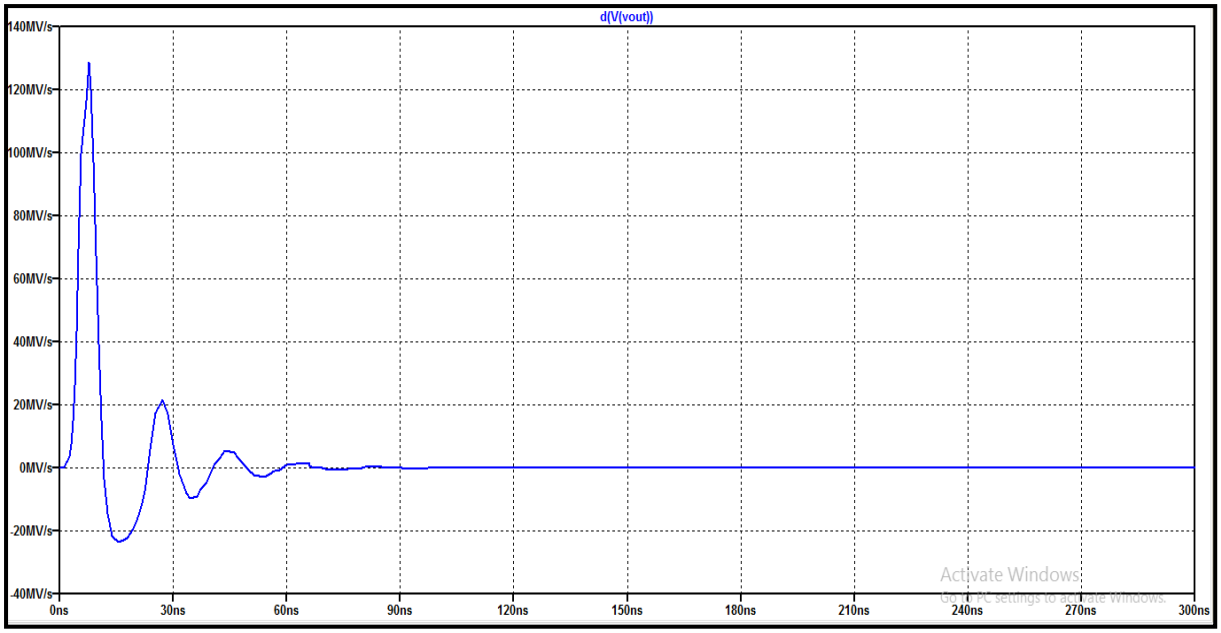


FIG 7.46 Simulation Showing Slew Rate (C_L = 10pF)

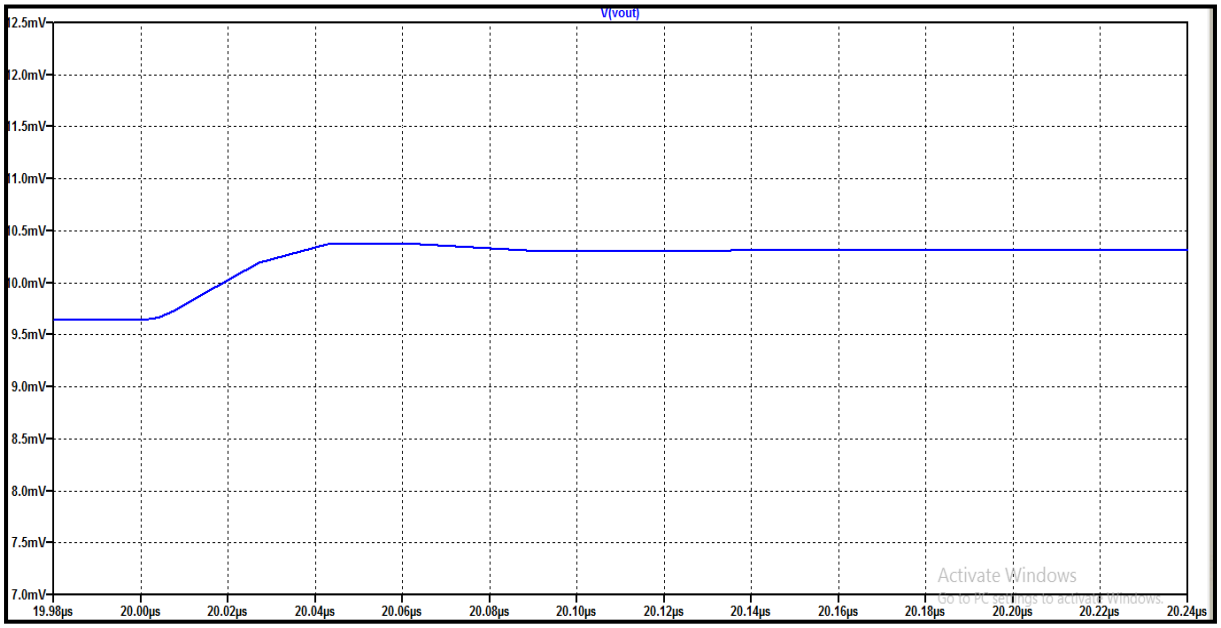


FIG 7.47 Simulation showing Code to Code Output Settling Time (C_L = 10pF)

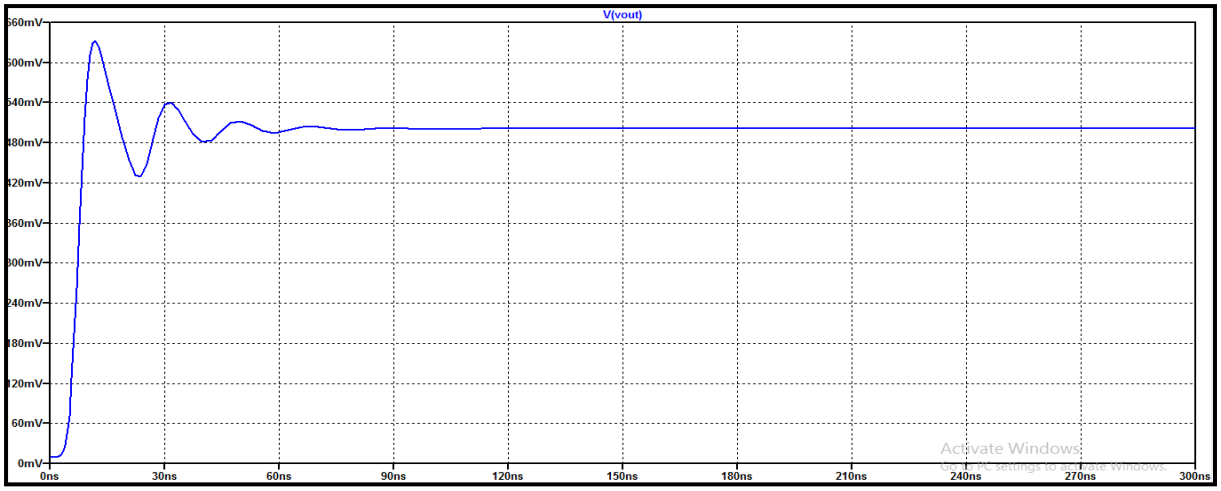


FIG 7.48 Simulation showing Full Scale Output Settling Time (C_L = 10pF)

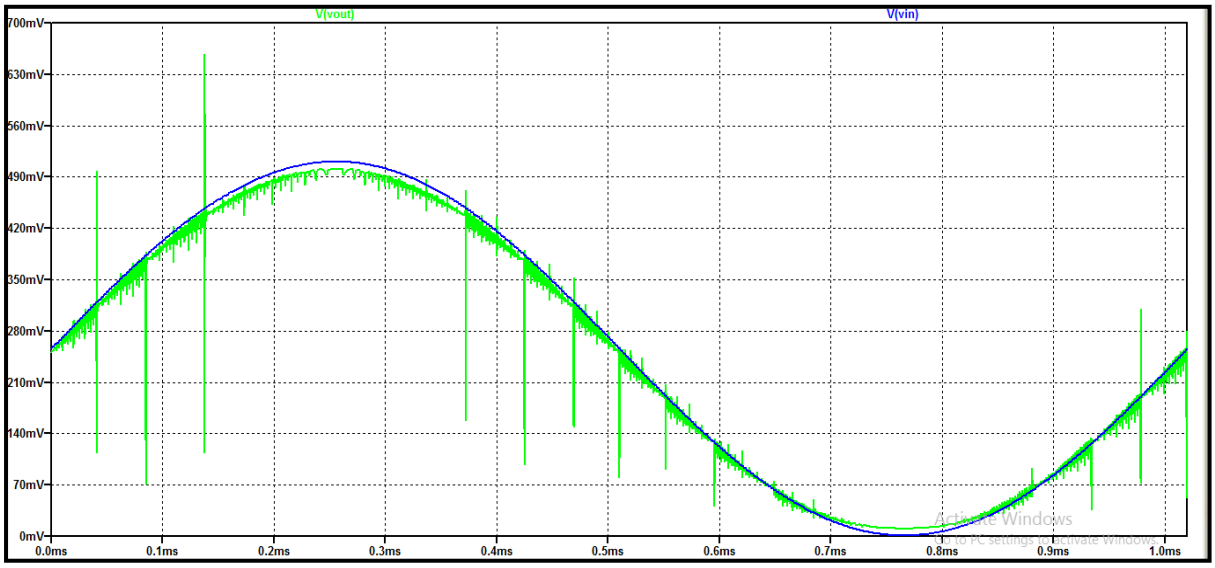


FIG 7.49 Calculating Total Harmonic Distortion (THD) (R_L = 100kΩ, C_L = 100pF)

SPICE Error Log: F:\DAC\Current source\Final\9bit_comb_pwl.log

```
N-Period=1
Fourier components of V(vout)
DC component:0.251671

Harmonic     Frequency     Fourier     Normalized   Phase      Normalized
 Number        [Hz]       Component    Component   [degree]   Phase [deg]
    1       9.800e+02    2.457e-01   1.000e+00      0.06°       0.00°
    2       1.960e+03    1.988e-03   8.094e-03    -94.24°     -94.30°
    3       2.940e+03    5.302e-04   2.158e-03      0.54°       0.48°
    4       3.920e+03    7.954e-04   3.238e-03     95.50°      95.44°
    5       4.900e+03    3.564e-04   1.451e-03    177.18°     177.12°
    6       5.880e+03    1.683e-04   6.850e-04    -97.04°     -97.10°
    7       6.860e+03    2.292e-04   9.330e-04      1.18°       1.12°
    8       7.840e+03    8.827e-05   3.593e-04    104.95°     104.89°
    9       8.820e+03    4.338e-05   1.766e-04   -171.70°    -171.76°
Total Harmonic Distortion: 0.917889%(4.912612%)
```

FIG 7.50 Calculating Total Harmonic Distortion(THD)

CHAPTER 8

CONCLUSION AND FUTURE WORKS

CONCLUSION

This report presents the design and simulation of a high resolution 9 bit DAC using TSMC 180 nm technology. Realising low power, high speed, high resolution and high accuracy DACs is still a problem. In view of this, an attempt has been made to design a high resolution, low power DAC using current steering architecture. It is a 9 bit DAC implemented by integrating a 6 bit DAC with 1 mV resolution and a 3 bit DAC with 64 mV resolution, so that the architecture results in a general 9 bit DAC with 1 mV resolution. The result is a is a significant reduction in the number of MOS current sources required, hence a lower chip area and lower power consumption. A non- inverting summing amplifier using folded cascode configuration of differential amplifier has been designed to add the outputs of the coarse(3 bit) and fine(6 bit) DACs, generating the desired analog output for the corresponding digital input.

Dynamic characteristics of the DAC such as INL, DNL, settling time, slew rate have been measured for different inputs which show satisfactory results, except for a discrepancy in the INL, DNL results which has been discussed in the section for future works.

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both due to which a glitch may appear on the output due to code transition in transient analysis. These glitches can be removed by using:

1. Capacitive filter:The use of capacitor at the output filters the unexpected spikes and glitches get minimized at the output. However, a large capacitor has to be used and this affects the settling time of the DAC as the capacitor takes time to charge. Hence a compromise between speed and accuracy has to be made to suit the requirements of the designer.
2. RLC filter: An RLC filter may also be used at the output of the DAC as this filter effectively minimizes glitches at the output.

Frequency domain characteristic of total harmonic distortion(THD) comes out to be 0.92% for a load of R = 100kΩand C = 100pF. However the graph for THD shows spikes at every transition. This does not pose a cause for concern, as the simulating software LTSpice uses PWL (piecewise linear) files for providing the digital input combinations at different time points. As such, the function being linear doesn't allow for a sudden transition between logic '1' and logic '0', rather provides a linear transition. This problem of spikes can be easily rectified with a filter, as discussed above.

FUTURE WORKS AND SCOPE OF IMPROVEMENT

The final DAC design gives a zero scale error or offset error of 9.64mV and this result could be improved. Further, in the design of biasing circuit for current mirrors, it is seen that the current source works(remains in saturation) for a range of approximately 0 to 1.4V while the working range of the current sink is approximately 0 to 1.8V. This range could be improved further if the gate to source voltage V_{GS} is attempted to be brought closer to threshold voltage V_{TH}, resulting in a reduced V_{DSsat} which in turn increases the range of operation.

A major drawback of the design are the large values of DNL at the transition points, consequently resulting in a large INL. Results show that a change in digital input for the coarse DAC results in a step size of almost 2LSB at the output of the summing amplifier. However the digital inputs between two consecutive transition points of the coarse DAC give very good results of almost 0 DNL error. Efforts can be invested in attempting to design a non-inverting summing amplifier whose output remains unaffected by the change in coarse DAC input.

Finally, apart from the above mentioned criteria future work should also concentrate on further decreasing power consumption, and providing better accuracy.

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[4] “Design of Low Power 8-Bit Digital-to-Analog Converter with Good Voltage-Stability”, Anshul Agarwal, *Master of Science (by Research),In Electronics and Communication Engineering ,*Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India*,* May 2013.

[5] “Analysis of Influence of DAC on Total Harmonic Distortion in Digital Waveform Synthesis”, Li Yalu Liu Min (Beijing Orient Institute of Measurement & Test Chinese Academy of Space Technology Mail-Box 9628, Beijing, China,100086).