A Comparative Analysis of Analog Performances of Underlapped Dual Gate AlGaN/GaN based MOS-HEMT and Schottky-HEMT

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***Abstract* — This paper elucidates a comparative and analytical study on the basis of analog performances of an Underlapped Dual Gate (U-DG) AlGaN/GaN MOS-HEMT with Hafnium based high-k dielectric (HfO_2) as the gate oxide and an U-DG AlGaN/GaN Schottky-HEMT. The study has been conducted based on the effect on the conduction band energy profile and also on the basic Analog Figure of Merits (FoMs) like Drain current (I_D), Transconductance (g_m), Output Resistance (r_o), Intrinsic Gain ($g_m r_0$). It has been observed that though Schottky-HEMTs have higher transconductance and faster switching transients, MOS-HEMTs are advantageous over the former as the latter experiences higher drive current capacity, lower threshold voltage, better I_{on}/I_{off} ratio and greater peak intrinsic gain.**

Index Terms —Analog, AlGaN/GaN Heterojunction, MOS-HEMT, Schottky-HEMT, Symmetric Underlap, Underlapped Dual Gate (U-DG).

I. Introduction

Traditional MOSFETs have been found to deliver slower performances owing to the impurity scattering in short channel devices, which eventually also gives rise to undesirable heating and loss **[1]**. So growth of high-electron-mobility-transistor (HEMT) structures of graded aluminium gallium nitride–gallium nitride (AlGaN/GaN) is now preferred over the former **[2-4]**. Wide and tunable band gap, high electron mobility and average drift velocity, high breakdown voltage as well as good thermal stability makes gallium nitride (GaN) a promising material for high power and high frequency electronic devices **[5-6].** AlGaN/GaN HEMT structures on high quality ammonothermal GaN substrate became recently available **[7],** allowing development of low leakage current electronic devices **[8].**

Although in HEMT devices, ionized impurity scattering is prevented and carrier mobility is also increased by the use of undoped AlGaN/GaN substrate, the gate leakage current and buffer leakage are important factors limiting its performance and reliability **[9].** Therefore, a Schottky contact is made between the gate metal and the channel, and the potential of the channel is varied by applying a voltage at the gate. Schottky-HEMTs undergo only a two step photolithography processing procedure as oxide layer implantation is not required and hence are more economical**.** However, the greatest drawback is that turn-on voltage for Schottky is very low **[10]** and since, the threshold has to be lower than the turn-on voltage, they are not preferred for high voltage applications. However, the use of a gate oxide as an insulator between gate and channel helps to improve gate contact forming a MOS-HEMT, further decreasing the gate leakage current and increasing the drain current **[11-13]**. Nevertheless, it partly reduces the transconductance because of a larger gate-to-channel separation **[14].** MOS-HEMT devices still exhibit a gate leakage reduction of six to ten orders of magnitude compared to a Schottky barrier HEMT of similar design **[15].**

Schottky-HEMTs exhibit higher carrier mobility as compared to MOS-HEMTs **[16].** This is explained from the fact that in MOS-HEMTs, high electric fields required to form the inversion layer pull the carriers closer to the gate oxide interface below the MOS gate. In contrast, the perpendicular electric fields in the Schottky-HEMT are smaller and the carrier confinement is less pronounced. Therefore, fewer charge carriers interact with the rough back interface causing less surface scattering and higher average electron velocity than MOS-HEMTs. Though Schottky-HEMTs showcases higher carrier mobility and faster switching, MOS-HEMTs are preferred more over the former as the latter has higher input impedance, higher gate capacitance, higher drive current capacity, lower leakage current and are much more preferred in high frequency RF applications **[16].**

In this paper, an Underlapped Dual Gate (U-DG) AlGaN/GaN heterostructured MOS-HEMT and a Schottky-HEMT has been analyzed and compared on the basis of their electrical characteristics and analog performance. The use of dual gates helps improve the channel control and reduce the short channel effects (SCEs). They also add to higher on current (I_{on}) by better channel utilization **[17-18]**. Underlap creates a physical separation between Gate and Drain, suppressing DIBL and hence to reduce the off current (I_{off}) **[19].** It also takes care of fringing losses**,** which have now found applications in bio-detection for robust noise handling devices **[20-22].**

II. Device Structure

The two dimensional cross sectional views of an U-DG AlGaN/GaN based heterostructured MOS-HEMT and a Schottky-HEMT with symmetric source and drain overlap on both sides of the two gates are depicted in Fig. 1 and Fig. 2 respectively. While a rectifying contact is formed between the gate and the channel in the Schottky-HEMT, the MOS-HEMT uses Hafnium based high K dielectric gate material with thickness (t_{ox}) 10 nm, to achieve improved device performance **[23].** The device dimensions that are common to both taken into consideration is gate length (L_g), of 200 nm, gate height (gh), of 50 nm, underlap length on both sides of source/drain electrodes (L_s/L_d), of 200 nm, source/drain length (S), of 200 nm according to ITRS 2008 for RF and Mixed Signal applications **[24].** In both the devices, AlGaN/GaN heterojunction has been implemented with a layer of AlGaN of thickness (d1) 18 nm grown over GaN with thickness (d2) 180 nm. As the I_{on}/I_{off} ratio is maximum for the range 140 nm - 180 nm **[25],** therefore, in this paper, device channel thickness is chosen as 180 nm.

III. Simulation Procedure

All the simulations relevant to the analysis have been performed using TCAD device simulator **[26]** and standard experimental data has been used for calibration **[27].** The model specifications have been adjusted and tuned for incorporating the attributes and features of this experimental prototype into the simulator model. Mobility models have been included to handle the effects of carrier mobility degradation owing to the short channel effects (SCEs) like surface scattering and carrier velocity saturation due to the high lateral electric field. The Albrecht Model is added to simulate low field mobility calibration in the device, the Shockley-Reed-Hall (SRH) Recombination Model is incorporated for determining the correct active carrier lifetime and the Fermi-Dirac statistics model for correct device processing. Polarization Model is for GaN based devices and Newton Model is for device computations involving complex equations and quadratic convergence. The mole fraction, x of Al in $Al_xGa_{(1-x)}N$ is considered as 0.3 with Molybdenum as the gate material **[28]** and metallic source and drain having a work function of 4.31 eV on Si_3N_4 substrate. The following section showcases a comparative study of Analog Performances of the above described MOS-HEMT and Schottky-HEMT devices.

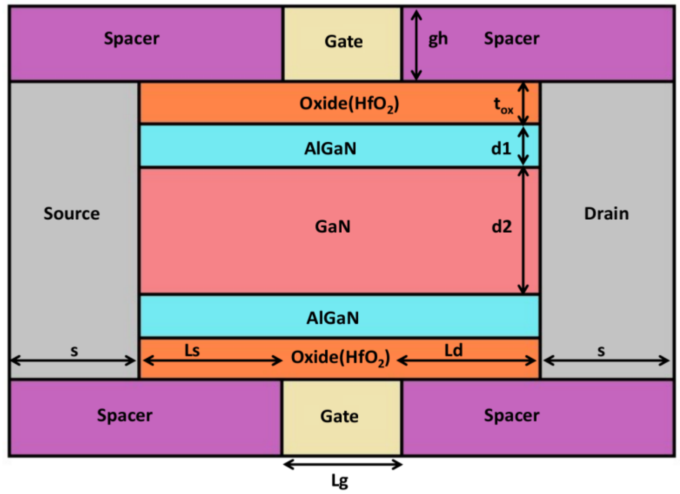

Fig. 1. Cross section of U-DG AlGaN/GaN MOS-HEMT with source and drain underlap.

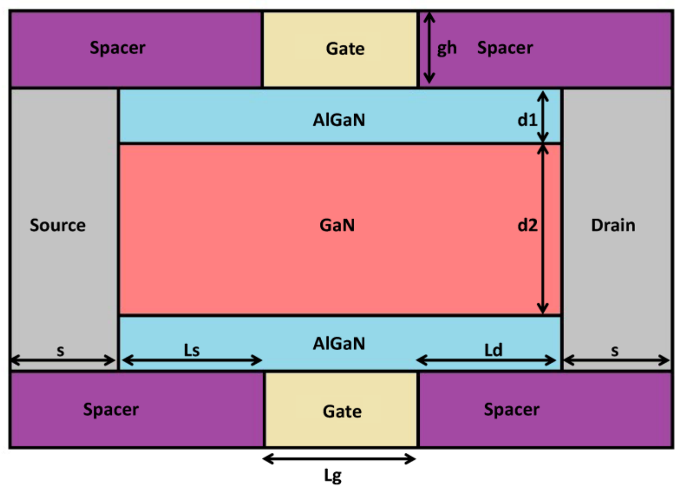

Fig. 2. Cross section of U-DG AlGaN/GaN Schottky-HEMT with source and drain underlap.

IV. Analog Performance

The Analog FOMs that have been compared between a MOS-HEMT and a Schottky-HEMT include the variation of Drain Current (I_D) with respect to both Gate to Source Voltage (V_{GS}) and Drain to Source Voltage (V_{DS}), Transconductance (g_m), Output Resistance (r_o) and Intrinsic Gain (g_mr_o).

Fig. 3 and Fig. 4 show the variation of conduction band energy along the length of the channel for MOS-HEMT and Schottky-HEMT devices in OFF state and ON state respectively. As observed from the Fig. 4, both the devices have almost same conduction energy variation throughout the channel in ON state. In the central part of the channel beneath the gate together with the underlaps on either side, the conduction band energy in MOS-HEMT is lower than that of Schottky-HEMT. This implies more number of carriers can overcome the barrier between source and channel and thus reach the drain, contributing to large drain current for any specific V_{DS}.

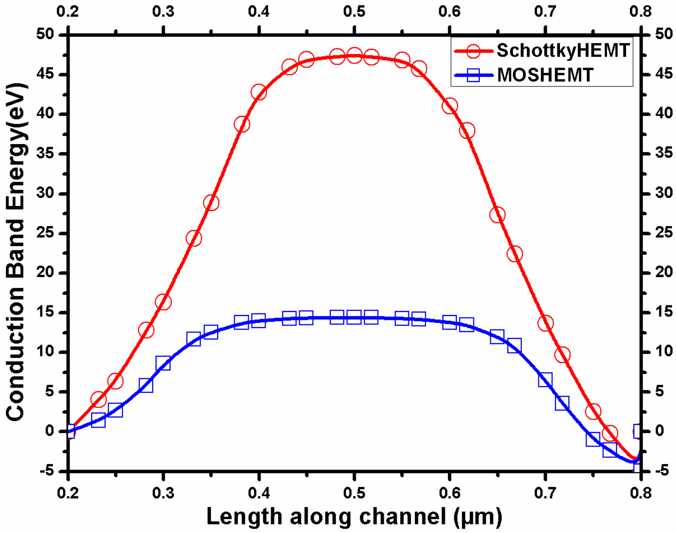

Fig. 3. Conduction band energy variation along the channel of U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT at V_{DS} = 5V both devices are in OFF state.

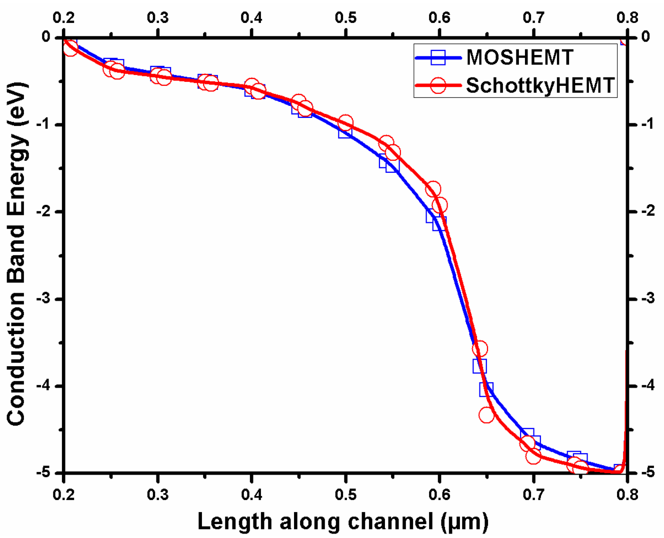

Fig. 4. Conduction band energy variation along the channel of U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT at V_{DS} = 5 V in ON state.

Fig. 5 illustrates the variation of I_D with respect to V_{DS} and as it depicts, I_D is almost same in linear region for both devices, but in saturation region I_D for MOS-HEMT is higher and this difference keeps increasing with increasing V_{DS}. This fact can be justified by the above explanation which shows MOS-HEMT has lower conduction band energy than Schottky-HEMT in the channel, and hence I_D will be higher for MOS device for a particular V_{DS} in saturation region.

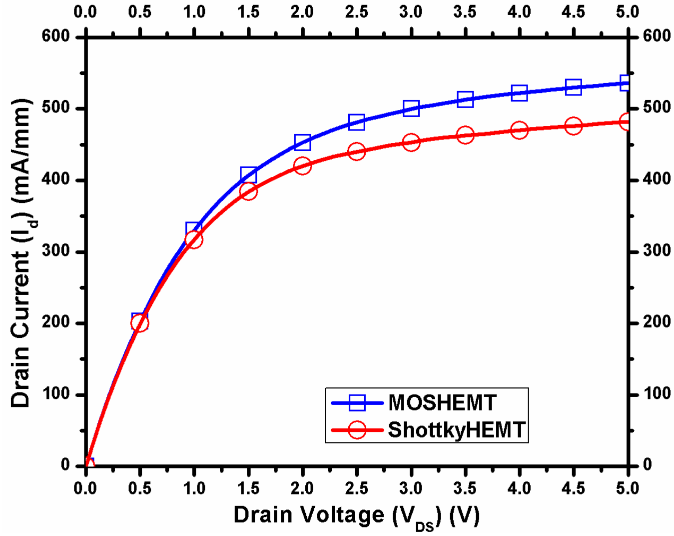

Fig. 5. Variation of I_D in linear scale as a function of V_{DS} at V_{GS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT devices.

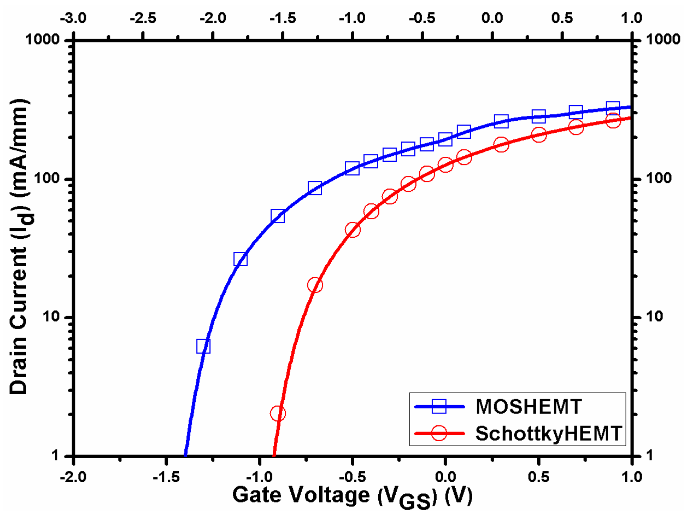

Fig. 6. Variation of I_D in logarithmic scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT

In both the devices, a conduction channel is already present beforehand which enables current flow even at zero gate bias voltage. Increasing the gate bias voltage makes the channel further conducting, whereas, decreasing it drives the channel into cut-off. The negative gate voltage required to completely turn off the device is called threshold voltage, V_{th}. In Schottky-HEMT, V_{th} is the voltage required to fully deplete the doped channel region of the reverse biased Schottky junction, thereby removing the channel band bending at the gate/AlGaN interface. On the other hand, in MOS-

HEMT, both the oxide band bending and the channel band bending have to be removed to turn off the device. Therefore, greater negative gate bias voltage is required for MOS-HEMT. So, absolute value of threshold voltage is greater for MOS-HEMT in comparison to Schottky-HEMT as is evident from Fig. 6.

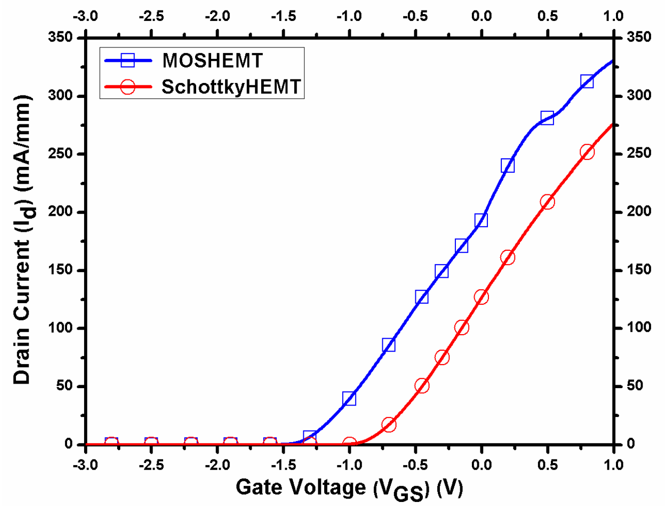

Fig. 7. Variation of I_D in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT devices.

In case of MOS-HEMT, the metallic oxide present between gate and substrate not only serves as an insulator by reducing the gate leakage current, but also increases the gate capacitance giving better gate control over channel thus accounting for improved device performance. As the charge stored per unit channel area, Q_{ch} varies directly with C_{ox}, the oxide capacitance per unit area, the concentration of charge carriers per unit channel width will be more in MOS-HEMT than Schottky-HEMT due to the presence of C_{ox} term. Thus, as evident from Fig. 7, I_D of MOS-HEMT is greater than Schottky-HEMT for any specific V_{GS}.

Fig. 8 illustrates the transconductance curves for both MOS-HEMT and Schottky-HEMT with varying V_{GS}. Mobility degradation due to surface roughness scattering at the oxide channel interface under high vertical effective fields causes the transconductance to exhibit a fall-off at about 0.5V above threshold in conventional MOSFETs **[29]**. However, Schottky experiences higher carrier mobility in the channel as compared to MOS. This is because the carriers located in the inversion layer of the MOS have a wavefunction extending into the oxide which causes their surface mobility to drop than that of the bulk material. On the other hand, as the depletion layer in Schottky separates the carriers from the surface their mobility is close to the bulk material **[10]**. Lower mobility leads to lower transconductance. But since I_D is higher in MOS and the threshold is also more negative, the g_m-V_{GS} curve of MOS-HEMT starts at lower V_{GS}, increases and experiences an early fall off at a higher rate than that of Schottky and therefore a cross-over is observed of both the curves at approximately -0.5V after which the transconductance of Schottky always leads that of MOS.

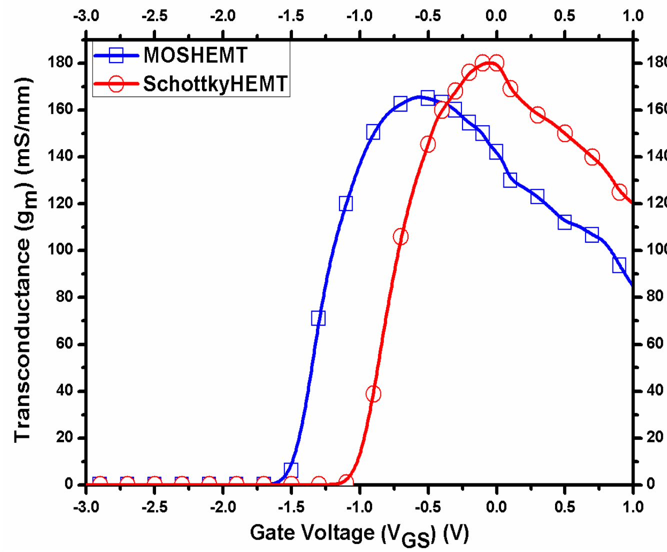

Fig. 8. Variation of g_m in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT

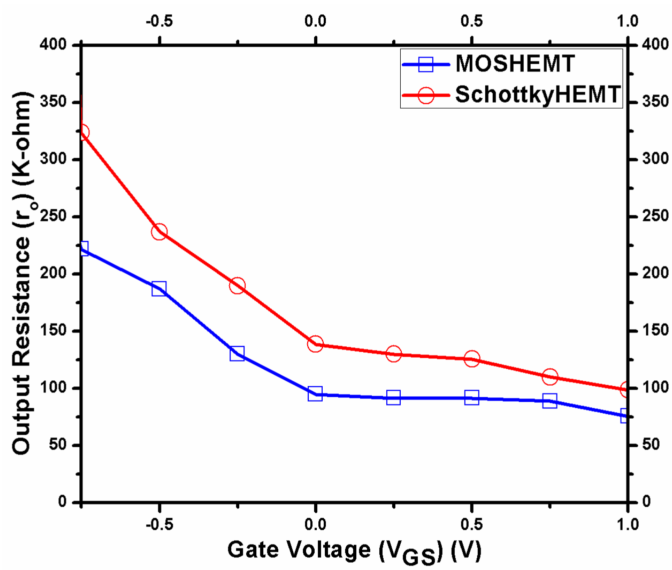

Fig. 9. Variation of r_o in linear scale as a function of V_{GS} for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT

It is observed from Fig. 9, output resistance of Schottky-HEMT is higher than that of MOS-HEMT. This can be justified by the fact that since, the drain current in MOS is higher than that of Schottky because of the presence of the gate oxide layer which provides better control to the channel, change in drain current for same change in drain voltage in saturation is also higher in MOS, yielding lower r_o in MOS-HEMT, compared to Schottky-HEMT.

The g_m and r_o values thus obtained illustrate the plot of intrinsic gain with V_{GS} in Fig. 10. Initially, the MOS-HEMT having lower V_{th} becomes on, while the Schottky-HEMT still remains in cut-off and hence the latter showcases higher intrinsic gain due to very high r_o. Eventually, when both the devices are on, the intrinsic gain of MOS overshoots that of Schottky due to predominance of its higher g_m. However, as stated above, MOS experiences a sharper decay in its transconductance than Schottky from approximately -0.5 V gate voltage onwards. Thus, intrinsic gain of Schottky eventually becomes higher and the trend is maintained for the rest part of the plot.

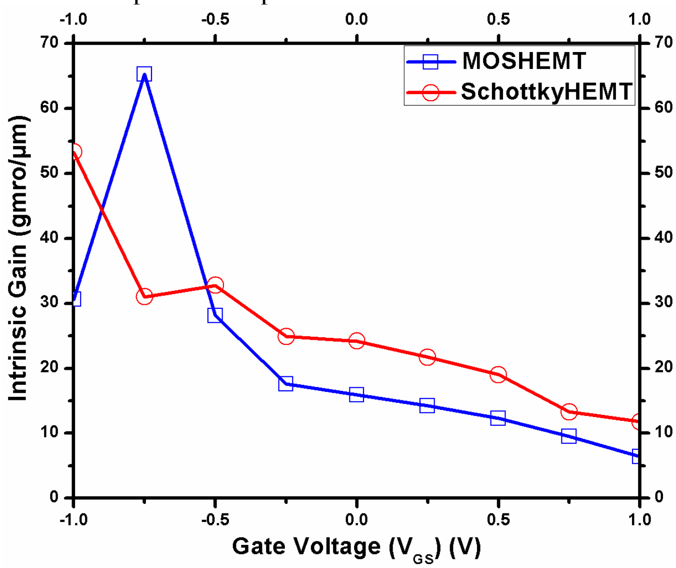

Fig. 10. Variation of $g_m r_o$ in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT

V. CONCLUSION

The simulation results indicate a superior improvement in the output characteristics of MOS-HEMTs with respect to Schottky-HEMTs, with 10% higher saturation drain current values at V_{DS}=5V. Furthermore, MOS-HEMT has threshold voltage lower by 0.5V increasing its ON state operating range and 16.3% higher drain current values at V_{GS}=1V. Though the transconductance peak ($g_{m,max}$) is observed to be 8.4% more for Schottky with respect to MOS, the latter has a peak intrinsic gain ($g_m r_{o,max}$) greater by 18.4%. All these experimental results show that MOS-HEMT is indeed a promising alternative to regular HEMT for high power, high frequency and high temperature applications. However, from a futuristic point of view, these HEMT structures could be proposed as suitable replacements for conventional MOSFETs.

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VII. REFERENCES

[1] V. F. Conwell, E. and Weisskopf,"Theory of Impurity Scattering in Semiconductors," Phys. Rev, vol. 77, no. 3, pp. 388–390, 1949.

[2] F. Schwierz,"The frequency limits of field-effect transistors: MOSFET vs. HEMT," *Int. Conf. Solid-State Integr. Circuits Technol. Proceedings, ICSICT*, pp. 1433–1436, 2008 DOI: 10.1109/ICSICT.2008.4734822.

[3] K. Zhang, M. Y. Cao, Y. H. Chen, L. Y. Yang, C. Wang, X. H. Ma, and Y. Hao,"Fabrication and characterization of V-gate AlGaN/GaN high-electron-mobility transistors," *Chinese Phys. B*, vol. 22, no. 5, 2013 DOI: 10.1088/1674-1056/22/5/057304.

[4] A. Mondal, A. Roy, R. Mitra ,and A. Kundu,"Comparative Study of Variations in Gate Oxide Materials of a Novel Underlap DG MOS-HEMT for Analog/RF and High Power Applications," [In Press] *Silicon-Springer.*

[5] J. Zolper, Advanced device technologies for defense systems, in: Proceedings of Device Research Conference (University Park, TX, 2012) pp. 9–12.

[6] Lithuanian Journal of Physics, SCHOTTKY DIODES AND HIGH ELECTRON MOBILITY TRANSISTORS OF 2DEG AlGaN/GaN STRUCTURES ON SAPPHIRE SUBSTRATE V. Jakštas, I. Kašalynas, I. Šimkienė, V. Strazdienė, P. Prystawko, and M. Leszczynski.

[7] R. Dwiliński et al., Ammonothermal GaN substrates – growth accomplishments and applications, Phys. Status Solidi A 208, 1489 (2011).

[8] P. Kruszewski et al., AlGaN/GaN HEMT structures on Ammono bulk GaN substrate, Semiconduct. Sci. Technol. 29, 075004/7 (2014), http://dx.doi. org/10.1088/0268-1242/29/7/075004

[9] "Enhanced device performance of AlGaN/GaN HEMTs uing HfO_2 high-k dielectric for surface passivation and gate oxide" by Chang Liu, Eng Fong Chor and Leng Seow Tan on SEMICONDUCTOR SCIENCE AND TECHNOLOGY by IOP PUBLISHING DOI: 10.1088/0268-1242/22/5/011

[10] Van Zeghbroeck, B., 2011,"Principles of semiconductor devices", Chapter 3:Metal-Semiconductor Junctions, Boulder, Colorado.

[11] J. McPherson, J. Y. Kim, A. Shanware, and H. Mogul,"Thermochemical description of dielectric breakdown in high dielectric constant materials," *Appl. Phys. Lett.*, vol. 82, no. 13, pp. 2121–2123, 2003 DOI: 10.1063/1.1565180.

[12] A. Z. KHOKHAR, S. TAKING, A. M. DABIRAN, E. WASIGE, and D. MACFARLANE,"DC and RF Performance of AlN/GaN MOS-HEMTs," *IEICE Trans. Electron.*, vol. E94-C, no. 5, pp. 835–841, 2011 DOI: 10.1587/transele.e94.c.835.

[13] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter,"Observation of a twodimensional electron gas in low pressure metalorganic chemical vapor deposited $GaNAl_xGa_{1-x}N$ heterojunctions Qbserwation metalorganic of a two-dimensional electron gas in low pressure chemical vapor deposited GaN-AI , Ga , - , N he," vol. 3027, no. 1992, pp. 58–61, 1995 DOI: 10.1063/1.106798.

[14] E. Tschumak, R. Granzer, J. K. N. Lindner F. Schwierz, K. Lischka, H. Nagasawa, M. Abe, and D. J. As, "*Nonpolar cubic AlxGa1-xN/GaN heterojunction field-effect transistor on Ar+ implanted 3C–SiC (001)*", Appl. Phys. Lett, vol. 96, n°.25, pp. 3501-3503, June 2010.

[15] Pozzovivo G, Kuzmik J, Golka S, et al. Gate insulation and drain current saturation mechanism in InAlN /GaN metal–oxide–semiconductor high-electron-mobility transistors. Appl Phys Lett, 2007, 91: 043509

[16] T.Khan, D.Vasileska. Member, IEEE and T.J. Thornton,"Study of Cutoff Frequency Calculation in the subthreshold regime of operation of the SOI-MESFETs", NSTI-Nanotech 2005, ISBN 0 -9767985-2-2 Vol. 3.

[17] J. Colinge,"Multiple-gate SOI MOSFETs," vol. 48, pp. 897–905, 2004 DOI: 10.1016/j.sse.2003.12.020.

[18] M. Bhattacharya, J. Jogi, R. S. Gupta, M. Gupta, S. Devices, S. Campus, S. Campus, and C. Engineering,"Impact of Doping concentration and Donor- layer thickness on the dc characterization of symmetric Double-gate and Single-gate InAlAs / InGaAs / InP HEMT for nanometer gate dimension-A comparison," pp. 134–139, 2010.

[19] Effect of Underlap and gate length on device performance of an ALInN/GaN underlap MOFET by Hemant Pardeshi, Sudhansu Kumar Pati, Godwin Raj, N Mohankumar and Chandan Kumar arkar on Journal of Semiconductors, December 2012.

[20] Dielectric Modulated Underlap Based AlGaN/AlN/GaN MOS-HEMT for Label Free Bio-Detection by Varghese, Arathy, Periasamy, Chinnamuthan,Bhargava,Lava on Journal of Nanoelectronics and Optoelectronics, Volume 14, Number 8,August 2019, pp. 1064-1071(8) Publisher: American Scientific Publishers.

[21] M.Boˇzani´c and S.Sinha, "Emerging Transistor Technologies Capable of Terahertz Amplification: A Way to Re-Engineer Terahertz Radar Sensors" Sensors,vol. 19,no.11, pp. 2454, 2019.

[22] B.Buvaneswari and N.B.Balamurugan, "2D Analytical Modeling and Simulation of Dual Material DG MOSFET for Biosensing Application" AEU-International Journal of Electronics and Communications,vol. 99, pp. 193-200, 2019.

[23] K.P.Pradhan, S.K.Mohapatra, P.K.Sahu, D.K.Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET", Microelectronics Journal 45 (2014) 144-151.

[24] Internatonal Technology Roadmaps for Semiconductors (ITRS); 2008 edition.

[25] A. Roy, R. Mitra, A. Kundu, "Influence of Channel Thickness on Analog and RF Performance Enhancement of an Underlap DG AlGaN/GaN based MOS-HEMT Device", Devices for Integrated Circuit (DevIC), 23-24 March, 2019, Kalyani, India, pp. 186-190.

[26] A. Kundu, A. Dasgupta, R. Das, S. Chakraborty, A. Dutta, and C. K. Sarkar,"Influence of Underlap on Gate Stack DG-MOSFET for analytical study of Analog/RF performance," *SuperlatticesMicrostruct.*, vol. 94, pp. 60–73, Jun. 2016 DOI: 10.1016/j.spmi.2016.04.013.

[27] Mao Wei, Zhang Jin Cheng, Xue Jun Shuai, Hao Yao et al, 'Fabrication and Characteristics of AlInN/AlN/GaN MOS-HEMTs with Ultra Thin Atomic Layer Deposited Al2O3 Gate Dielectric", 2010, 27,(12), pp.2008-2011.

[28] A. Kundu,Kalyan Kole,Arka Dutta,Chandan K.Sarkar, "Impact of gate metal work function engineering for enhancement of subthrehold analog/RF performance of underlap dual material gate DG-FET", Mioelectronics Reliability 54 (2014), pp.2717-2722.

[29] D. Pearman, "Electrical Characterisation and Modelling of Schottky barrier metal source/drain MOSFETs", Thesis, University of Warwick, September, 2007.