Hrit Mukherjee

Résumé

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Research Work Experience

Summer Research Intern, Variable Energy Cyclotron Centre (VECC), Kolkata, India. May'19-July'19.	**Low Power High Resolution High Speed DAC design:** Worked as a summer intern under the ASIC team and successfully completed the design of a Low Power High Resolution High Speed 9 bit DAC. The proposed DAC was designed following current steering architecture and consists of two separate DACs, a 6 bit fine and a 3 bit coarse, whose individual responses have been added up using a non-inverting opamp. **Design Specifications:** Resolution = 1mV, Power Consumption =1.6mW (Battery used = 1.8V and LSB current = 2µA). Project_Report
IEEE Center for Excellence, Heritage Institute of Technology, Kolkata, India. October'19-Present.	**Design and Analysis of Schottky-HEMT and MOS-HEMT in the light of electrical characteristics:** Completed a project which presents the comparison of electrical characteristics of SchottkyHEMT and MOSHEMT and thereby concluding which is more suitable in case of High Frequency(RF) applications. The structures and layouts are designed according to given specifications. **Design Specifications:** Channel length = 180 nm, Source/Drain/Gate/Underlap Length = 200 nm each, Technology used = AlGaN/GaN HEMT. **Simulators:** TCAD Silvaco, Origin Maker 8. Paper(Published)

Academic Background

2017 - present	**Jadavpur University**, Kolkata, India. Third Year, Bachelor of **Electronics and Telecommunication Engineering** (2017-2021) . **SGPA:- 9.13** (1st year 1st semester) **Class Rank:- 7** **9.12** (1st year 2nd semester) **Class Rank:- 4** **9.31** (2nd year 1st semester) **Class Rank:- 3** **9.47** (2nd year 2nd semester) **Class Rank:- 5**
2017	**Higher Secondary Examination**, West Bengal Council of Higher Secondary Examination. **Nava Nalanda High School**, Kolkata, India. **Percentage: 96.40%** **State Rank: 8**
2015	**Madhyamik Examination**, West Bengal Board of Secondary Examination. **Nava Nalanda High School**, Kolkata, India. **Percentage: 94.00%** **Percentage (Science Group): 99.67%**

Internships and Schools Attended

Summer Research Intern, Variable Energy Cyclotron Centre (VECC), Kolkata, India. May'18-July'18.	Worked under the **ASIC section, Computer and Informatics Group, VECC, Kolkata** under the mentorship of Dr. Tanushyam Bhattacharja. Project: designing a **Low Power High Resolution High Speed Digital to Analog Converter.** Software Simulators used : **LT Spice and Cadence**
Finalist, Arm of Achelous, Kshitij, IIT Kharagpur. December'17-January'18.	Member of **Team Highfliers, ETCE, Jadavpur University** Project: built a basic **hydraulic arm bot**. The locomotive part was electrically powered. The controller is wired and is basically a dpdt (double pole double throw) control.
Trainee, Remote Control Plane Workshop, IIT Kanpur. November'17.	Member of **Team Highfliers, ETCE, Jadavpur University** Project: designing a **high winger aircraft** following the given specifications. **Flight test was conducted successfully** at airstrip, IIT Kanpur. Mentor: Professor Dr. Shantanu Bhattacharya.

Project

Hurry-Cane

- *Industrial project under the guidance of Prof. Sayan Chatterjee(PhD), Dept. of ETCE, Jadavpur University* **(Dec'19-Present)**

A breakthrough in navigation for the visually impaired to significantly increase their self support, mobility and social participation.

Designing a broadband communication system for improved RF performance using a log periodic toothed trapezoidal antenna at the receiver end.

-*Personal Project* **(October '19-Present)**

- Efficient antenna design to improve impedance matching and increase read range for better communication.
- Utilising ASK modulation scheme for modulation and PSK backscattering for demodulation.

Designing a low power high speed high resolution Bipolar DAC with output range normalized from -1 to +1

- *Research project under the guidance of Prof. Mrinal Kanti Naskar(PhD), Dept. of ETCE, Jadavpur University* **(October'19)**

- Design of a low power high speed unipolar n bit DAC using VLSI 180 nm CMOS technology.
- Conversion of unipolar DAC to bipolar DAC using a non-inverting opamp, external voltage source(not required, can be created by potentially dividing the given battery) and some additional passive components(resistors and capacitors) to get normalized output between -1 and +1 voltage range.

Low Complexity Generic VLSI Architecture Design Methodology for Nth Power and Nth Root Computations

- *Research project under the guidance of Prof. Jaydeb Bhaumik(PhD), Dept. of ETCE, Jadavpur University* **(October'19)**

- Nth root and Nth power computations have been performed using binary logarithm binary inverse relation(for a specified range of N and base, R), written in Verilog Language.
- The synthesis performed in SMDP lab, JU, shows that the proposed Nth root and Nth power computation saves 19.38% and 38% on chip area respectively and 15.86% and 35.67% power consumption respectively when compared with the conventional state of the art architecture implementations, without compromising the computational accuracy.

Training a Medical Image Classifier to attain a High Level of Accuracy for proper diagnosis of Brain Cancer

-*Research project under the guidance of Dr. Amitava Mukherjee, Senior Researcher, Dept. of ETCE, Jadavpur University* **(January'19-April'19)**

- Efficient compression of medical images via Compressed Sensing and Compression techniques. (done by me)
- Training a CNN model which will provide the measure of accuracy for any medical result namely MRI etc.

Electronic Alarm

-*Personal project* **(Dec'18)**

An alarm system built using a constant current source and a low input impedance operational amplifier which gets activated depending on the amount of current flowing through its two terminals.

Areas of Interest

Electronic Devices and Circuits, Analog Circuit Designing, Finite State Machine Circuit Design using digital logic, Digital Signal Processing, Microprocessors and Microcontrollers.

Some of relevant course-works done

1. **Physical Electronics and Electron Devices**, Professor Dr. Chayanika Bose, Dept. of ETCE, JU.
2. **Razavi Electronics 1** – by Behzad Razavi.
3. **Engineering Electronics II and Analog IC Design (Spring, 2019)** - by R. Jacob Baker, PhD, PE, University of Nevada, Las Vegas.
4. **Analog Circuits** and **IC Design –** by Dr. Nagendra Krishnapura, ECE, IIT Madras.
5. **Digital logic circuits** and **Digital systems**, Professor Dr. Mrinal Kanti Naskar, Dept. of ETCE, JU.
6. **Hardware Modeling Using Verilog**, Professor Indranil Sengupta, Dept. of ECE, IIT Kharagpur.
7. **Control Theory**, Professor Dr. Amit Konar, Dept. of ETCE, JU.
8. **Microprocessors and Microcontrollers,** Professor Bharat Acharya, University of Mumbai.

Skillset

1. Programming: C, Python, Matlab.
2. Operating Systems: Windows, Linux.
3. Software Simulators: LT Spice, P Spice, Circuit Maker, iVerilog, origin, Xilinx, GKTWAVE, TCAD Silvaco, Cadence(learning).
4. Typesetting tools and version control: Latex, Git & Github.

Some of Honors and Awards

1. Secured 8th position in Higher Secondary Examination, 2017.
2. Ranked 202 in WBJEE (West Bengal Joint Entrance Examination), 2017.
3. Winner (multiple times), DhrisTI online contest (on analog and microcontrollers), organized by Texas Instruments.
4. 2nd Runner-up, Electroniche(a competitive event involving circuit solving and designing and simulating circuits based on given specifications), organized by Srijan'19 (technological fest of Jadavpur University).
5. 2nd Runner-up, **Anveshan 2019-20: Student Research Convocation (East Zone)**, Social Science Category.
6. 1st Runner-up, **Papier**(a competitive event involving practical embedded systems model building and demonstration), organized by Convolution'2k20 (technological fest of Jadavpur University Electrical Engineering Department).

Responsibilities Holding / Held

1. IEEE *Student Member, Kolkata Section*

- Member of the Management team of Jadavpur University Student Branch of IEEE, Kolkata Section.
- Working under an active project, "*tete-a-tete* with IEEE".

2. Jadavpur University Code Club – Co-ordinator.

3. Jadavpur University Science Club – Member.

4. Fantasy for Innovation (Srijan'19) – Executive Committee Member.

5. Electrophoria'18(Departmental Freshers') – Core Member of the backdrop design team and web team.

Languages Known

1. Bengali- Native proficiency
2. English- Full working proficiency.
3. Hindi- Limited working proficiency.

Hobbies

Drawing, especially pencil-sketching
Website designing
Video Editing
Reading story books and comics
Listening to Music and Podcasts
Watching Football

Referees

Dr. Mrinal Kanti Naskar – Professor
Department of Electronics and Telecommunication Engineering, Jadavpur University
Email: mrinaletce@gmail.com

Dr. Tanushyam Bhattacharjee – Scientific Officer
Head, ASIC Design Section, VECC, Kolkata
Email: btanu@vecc.gov.in