Hrit Mukherjee Résumé

(A circuit designing enthusiast particularly interested in the Analog/Mixed Signal implementation of high speed, high precision Electronics devices.

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Address:- Kolkata, West Bengal, India

## **Work Experience**

# Analog Design Engineer, Texas Instruments, Bangalore, India.

Dec'21 - present.

# **Project: Continuous Time Delta Sigma ADC (DISHA) with enhanced linearity** (hpa9 process technology)

Architecture and Modelling: Developed the architecture for a 4th order CTSD based on SQNR and Linearity requirements. Implemented the discrete time model in MATLAB and continuous time model in Simulink and Cadence.

Key Specs: SQNR = 122dB for MSA = 0.8, THD = 123dB for signal frequency ranging from 0 to 1MHz for Fs = 64MHz.

Blocks designed:

1. Summer: A 3-stage differential input differential output Miller compensated OPAMP functioning as a summing amplifier.

Key Specs: DC Gain = 80dB (drops to 60dB at Band edge = 1MHz), UGB = 170MHz, PM = 45 deg, GM = 9dB, settling = 4tau in 12ns

2. Quantizer: A 4 bit SAR ADC acting as a quantizer providing the digital output of the CTSD. Key Specs: Conversion Time = 6ns

3. Compensation DAC: 2 4-bit R-DACs with SAR data as i/p and feeds current o/p to the summer. Key Specs: 95dB THD at SAR i/p, settling = 5 bit in 8ns

**Software:** Cadence, MATLAB and Simulink

Analog Design Engineer, Cirel Systems, Bangalore, India.

July'21 - Nov'21.

Project: KALAMOS Stylus IC (Dongbu process technology)

Blocks designed:

- 1. Charger: Powered by SCAP or Li-ion battery, can deliver a charging current from 21uA to 4.2mA or 1mA to 200mA with 10% accuracy across PVT.
- 2. PROT LDO: Powered by SCAP or Li-ion battery, soft starts upto 1.6V, delivers a load of 0 to 100mA at 1.8V output with input varying from 2.5V to 5.5V across PVT.
- 3. RTC LDO: Powered by SCAP battery, soft starts upto 1.6V, delivers a load of 0 to 4mA at 1.8V output with input varying from 1.9V to 2.05V across PVT.

Software: Cadence

Analog Design Intern, Variable Energy Cyclotron Centre (VECC), Kolkata, India.

May'19-July'19.

Project: Low Power High Resolution High Speed DAC design (TSMC 180nm CMOS technology) Worked as a summer intern in the ASIC team and successfully completed the design of a Low Power High Resolution High Speed Analog/Mixed Signal 9 bit DAC using 180 nm TSMC CMOS technology. The proposed DAC was designed following current steering architecture and consists of two separate DACs, a 6 bit fine and a 3 bit coarse, whose individual responses have been added up using a non-inverting opamp.

Software: LT Spice and Cadence

Project Report (https://hrit-mukherjee.github.io/Project%20Report.pdf)

Undergraduate Researcher, IEEE Center for Excellence, Heritage Institute of Technology, Kolkata, India.

Oct'19-Mar'22.

Design and Analysis of MOS-HEMT in the light of Analog/RF and Power performances:

1. Enhancement in Analog/RF and Power Performance of Underlapped Dual-Gate GaN-Based MOSHEMTs with Quaternary InAlGaN Barrier of Varying Widths: *Paper* (Enhancement in Analog/RF and Power Performance of Underlapped Dual-Gate GaN-Based MOSHEMTs with Quaternary InAlGaN Barrier of Varying Widths | Journal of Electronic Materials (springer.com))

- 2. A Comparative Analysis of Analog Performances of Underlapped Dual Gate AlGaN/GaN Based MOS-HEMT and Schottky-HEMT: <u>Paper</u> (https://ieeexplore.ieee.org/document/9106420)
- 3. Impact of Mole Fraction Variation on the Analog/RF Performance of Quaternary InAlGaN DG MOS-HEMTs: Paper (Impact of Mole Fraction Variation on the Analog/RF Performance of Quaternary InAlGaN DG MOS-HEMTs | Journal of Electronic Materials (springer.com))

Software: TCAD Silvaco.

Undergraduate Researcher, Innovation, TEQIP PHASE-III. Feb'20 -Mar'20.

**Hurry-Cane: "See through my eyes!":** Designed an IoT based electronic stick which is aimed to provide artificial vision to the visually impaired people by facilitating in their safe and independent terrestrial locomotion by virtue of its applications.

Hardware: Arduino UNO, Raspberry Pi3, NodeMCU, sensors and actuators.

Software: Android Studio. IoT server: Thinkspeak.

Project\_Report(https://github.com/Hurry-Cane/Papier\_Submission/blob/master/Hurry-Cane.pdf)

## **Academic Background**

2021	Bachelor of Electronics and Telecommunication Engineering (20 Jadavpur University, Kolkata, India. CGPA:- 9.6	017-2021) Dept. Rank:- 4
2017	Higher Secondary Examination (12th standard)	
	West Bengal Council of Higher Secondary Examination.	
	Nava Nalanda High School, Kolkata, India.	
	Percentage: 96.40%	State Rank: 8
2015	Madhyamik Examination (10th Standard)	
	West Bengal Board of Secondary Examination.	
	Nava Nalanda High School, Kolkata, India.	
	Percentage: 94.00%	Percentage (Science Group): 99.67%

### **Areas of Interest**

Analog and Mixed Signal Circuit Design, Microelectronics and Device physics, Digital Signal Processing, Embedded Systems.

#### Skillset

- 1. Programming: C, C++, Python, Matlab, Simulink.
- 2. Operating Systems: Windows, Linux.
- 3. Simulators: Cadence, LT Spice, P Spice, T Spice, Circuit Maker, Xilinx, Vivado, TCAD Silvaco.
- 4. Embedded System Platforms: Arduino UNO, NodeMCU, RaspberryPi 3.
- 5. Typesetting tools and version control: Latex, Git & Github.

# **Projects**

- 1. Hardware Implementation of Direction of Arrival (DoA) estimation and Node Localization algorithm for Smart Antenna in Wireless Sensor Networks
- Research project under the guidance of Prof. Dr. Mrinal Kanti Naskar, Dept. of ETCE, Jadavpur University (August'20-May'21)
- Final Year Project, Jadavpur University (Final Year Project.pdf (hrit-mukherjee.github.io))
- 2. Analytical Modeling of Surface Potential and Threshold Voltage for small geometry MOSFETs, HEMTs and FinFETs with non-uniformly doped channels
- Research project under the guidance of Prof. Dr. Amitava Dasgupta, Dept. of EE, IIT Madras (April'20-July'20)
- Summer Internship, Microelectronics and MEMS Laboratory Group, IIT Madras.

## Some of relevant course-works done

- 1. Razavi Electronics 1 by Behzad Razavi, University of California, Los Angeles.
- 2. Engineering Electronics II and Analog IC Design (Spring, 2019) by R. Jacob Baker, PhD, PE, University of Nevada, Las Vegas.
- 3. Analog Circuits and IC Design by Dr. Nagendra Krishnapura, ECE, IIT Madras.
- 4. VLSI Data Conversion Circuits by Dr. Shanthi Pavan, EE, IIT Madras.
- 5. Digital logic circuits and systems, Digital Signal Processing, Professor Dr. Mrinal Kanti Naskar, Dept. of ETCE, JU.

## **Awards and Achievements**

- 1. Recipient of 2021 IEEE Electron Device Society Undergraduate Student Scholarship (Region 10).
- 2. 1st Runner-up, **Anveshan 2019-20: Student Research Convention**, Social Science Category, a national level research contest, organized by AIU (Association of Indian Universities).
- 3. 2<sup>nd</sup> Runner-up, **Electroniche**(a competitive event involving circuit solving, designing and simulating circuits based on given specifications), organized by Srijan'19 (technological fest of Jadavpur University).
- 4. Winner (multiple times) of DhrisTI online contest (on analog and microcontrollers), organized by Texas Instruments.
- 5. Ranked 202 in WBJEE (West Bengal Joint Entrance Examination), 2017.
- 6. Secured 8th position in **Higher Secondary Examination** (12th Standard), 2017.

### Responsibilities Holding / Held

- 1. IEEE Student Member, Kolkata Section
  - Member of the Management team of Jadavpur University Student Branch of IEEE, Kolkata Section.
  - Member of IEEE EDS, Region 10.
- 2. Jadavpur University Code Club and Jadavpur University Science Club Co-ordinator.
- 3. Fantasy for Innovation: Srijan-Technological fest of Jadavpur University) Executive Committee Member.

## Referees

> Dr. Mrinal Kanti Naskar – Professor

Department of Electronics and Telecommunication Engineering, Jadavpur University Email: mrinaletce@gmail.com

Rahul Sharma – Analog Design Manager Precision ADC Team, Analog Signal Chain, Texas Instruments Email: <u>A0131586@ti.com</u>