Hrit Mukherjee

Résumé

*(A pre-final year undergraduate and **circuit designing enthusiast** particularly interested in the **Hardware** implementation of our **Electronics industry**)*

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Work Experience

Summer Intern, Variable Energy Cyclotron Centre (VECC), Kolkata, India. May'19-July'19.	**Low Power High Resolution High Speed DAC design:** Worked as a summer intern under the ASIC team and successfully completed the design of a Low Power High Resolution High Speed Analog/Mixed Signal 9 bit DAC. The proposed DAC was designed following current steering architecture and consists of two separate DACs, a 6 bit fine and a 3 bit coarse, whose individual responses have been added up using a non-inverting opamp. **Design Specifications:** Resolution = 1mV, Power Consumption =1.6mW (Battery used = 1.8V and LSB current = 2µA). **Simulators:** LT Spice and Cadence Project_Report
IEEE Center for Excellence, Heritage Institute of Technology, Kolkata, India. October'19-November'19.	**Design and Analysis of Schottky-HEMT and MOS-HEMT in the light of electrical characteristics:** Completed a project which presents the comparison of electrical characteristics of SchottkyHEMT and MOSHEMT and thereby concluding which is more suitable in case of High Frequency(RF) applications. The structures and layouts are designed according to given specifications. **Design Specifications:** Channel length = 180 nm, Source/Drain/Gate/Underlap Length = 200 nm each, Technology used = AlGaN/GaN HEMT. **Simulators:** TCAD Silvaco, Origin Maker 8. Paper (Published)

Academic Background

2017 - present	**Jadavpur University**, Kolkata, India. Third Year, Bachelor of **Electronics and Telecommunication Engineering** (2017-2021) . **SGPA:- 9.13** (1st year 1st semester) **Class Rank:- 7** **9.12** (1st year 2nd semester) **Class Rank:- 4** **9.31** (2nd year 1st semester) **Class Rank:- 3** **9.47** (2nd year 2nd semester) **Class Rank:- 5**
2017	**Higher Secondary Examination**, West Bengal Council of Higher Secondary Examination. **Nava Nalanda High School**, Kolkata, India. **Percentage: 96.40%** **State Rank: 8**
2015	**Madhyamik Examination**, West Bengal Board of Secondary Examination. **Nava Nalanda High School**, Kolkata, India. **Percentage: 94.00%** **Percentage (Science Group): 99.67%**

Internships and Schools Attended

Summer Intern, Variable Energy Cyclotron Centre (VECC), Kolkata, India. May'18-July'18.	Worked under the **ASIC section, Computer and Informatics Group, VECC, Kolkata** under the mentorship of Dr. Tanushyam Bhattacharja. Project: designing a **Low Power High Resolution High Speed Digital to Analog Converter.** Software Simulators used : **LT Spice and Cadence**
Finalist, Arm of Achelous, Kshitij, IIT Kharagpur. December'17-January'18.	Member of **Team Highfliers, ETCE, Jadavpur University** Project: built a basic **hydraulic arm bot**. The locomotive part was electrically powered. The controller is wired and is basically a dpdt (double pole double throw) control.
Trainee, Remote Control Plane Workshop, IIT Kanpur. November'17.	Member of **Team Highfliers, ETCE, Jadavpur University** Project: designing a **high winger aircraft** following the given specifications. **Flight test was conducted successfully** at airstrip, IIT Kanpur. Mentor: Professor Dr. Shantanu Bhattacharya.

Projects

1. Hurry-Cane

- *Industrial project under the guidance of Prof. Sayan Chatterjee(PhD), Dept. of ETCE, Jadavpur University* **(Jan'20-Present)**

- An electronic stick which is aimed to provide artificial vision to the visually impaired people by facilitating in their safe and independent terrestrial locomotion.
- The hardware has been deployed in embedded systems based platform with appropriate sensors and actuators.

2. Designing a low power high speed high resolution Bipolar DAC with output range normalized from -1 to +1

- *Research project under the guidance of Prof. Mrinal Kanti Naskar(PhD), Dept. of ETCE, Jadavpur University* **(October'19)**

Design of a low power high speed unipolar n bit analog/mixed-signal DAC using VLSI 180 nm CMOS technology.

3. Low Complexity Generic VLSI Architecture Design Methodology for Nth Power and Nth Root Computations

- *Research project under the guidance of Prof. Jaydeb Bhaumik(PhD), Dept. of ETCE, Jadavpur University* **(October'19)**

Nth root and Nth power computations have been performed using binary logarithm binary inverse relation(for a specified range of N and base, R), using Verilog Hardware Description Language, yielding much less power consumption and chip area with respect to conventional state of art architecture implementations.

4. Training a Medical Image Classifier to attain a High Level of Accuracy for proper diagnosis of Brain Cancer

-*Research project under the guidance of Dr. Amitava Mukherjee, Senior Researcher, Dept. of ETCE, Jadavpur University* **(January'19-April'19)**

- Efficient compression of medical images via Compressed Sensing and Compression techniques.
- Training a CNN model which will provide the measure of accuracy for any medical result namely MRI etc.

Areas of Interest

Microprocessors, Microcontrollers, Embedded Systems, PCB Design, Analog Circuit Design, Digital Signal Processing and VLSI Design.

Some of relevant course-works done

1. **Microprocessors and Microcontrollers, Embedded Systems,** Professor Bharat Acharya, University of Mumbai.
2. **Physical Electronics and Electron Devices**, Professor Dr. Chayanika Bose, Dept. of ETCE, JU.
3. **Razavi Electronics 1** – by Behzad Razavi.
4. **Engineering Electronics II and Analog IC Design (Spring, 2019)** - by R. Jacob Baker, PhD, PE, University of Nevada, Las Vegas.
5. **Analog Circuits** and **IC Design –** by Dr. Nagendra Krishnapura, ECE, IIT Madras.
6. **Digital logic circuits** and **systems, Digital Signal Processing**, Professor Dr. Mrinal Kanti Naskar, Dept. of ETCE, JU.
7. **Hardware Modeling Using Verilog**, Professor Indranil Sengupta, Dept. of ECE, IIT Kharagpur.
8. **Control Systems**, Professor Dr. Amit Konar, Dept. of ETCE, JU.

Skillset

1. Programming: C, C++, Python, Matlab.
2. Operating Systems: Windows, Linux.
3. Software: LT Spice, P Spice, T Spice, Circuit Maker, Origin, Xilinx, Vivado, Simulink, SEDA tools, TCAD Silvaco, Cadence.
4. Embedded System Platforms: Arduino UNO, NodeMCU, RaspberryPi 3.
5. Typesetting tools and version control: Latex, Git & Github.

Awards and Achievements

1. Secured 8th position in **Higher Secondary Examination**, 2017.
2. Ranked 202 in **WBJEE** (West Bengal Joint Entrance Examination), 2017.
3. Winner (multiple times), **DhrisTI** online contest (on analog and microcontrollers), organized by Texas Instruments.
4. 2nd Runner-up, **Electroniche**(a competitive event involving circuit solving and designing and simulating circuits based on given specifications), organized by Srijan'19 (technological fest of Jadavpur University).
5. 2nd Runner-up, **Anveshan 2019-20: Student Research Convocation (East Zone)**, Social Science Category.
6. 1st Runner-up, **Papier**(a competitive event involving practical embedded systems model building and demonstration), organized by Convolution'2k20 (technological fest of Jadavpur University Electrical Engineering Department).

Responsibilities Holding / Held

1. IEEE *Student Member, Kolkata Section*

- Member of the Management team of Jadavpur University Student Branch of IEEE, Kolkata Section.
- Working under an active project, "*tete-a-tete* with IEEE".

2. Jadavpur University Code Club and **Jadavpur University Science Club –** Co-ordinator.

3. Fantasy for Innovation (Srijan-Technological fest of Jadavpur University) – Executive Committee Member.

Referees

- **Dr. Mrinal Kanti Naskar –** Professor
  Department of Electronics and Telecommunication Engineering, Jadavpur University
  Email: mrinaletce@gmail.com
- **Dr. Tanushyam Bhattacharjee –** Scientific Officer
  Head, ASIC Design Section, VECC, Kolkata
  Email: btanu@vecc.gov.in