A Comparative Analysis of Analog Performances of Underlapped Dual Gate AlGaN/GaN Based MOS-HEMT and Schottky-HEMT

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Abstract—This paper presents a comparative and analytical study on the basis of analog performances of an Underlapped Dual Gate (U-DG) AlGaN/GaN MOS-HEMT with gate oxide and an U-DG AlGaN/GaN Schottky-HEMT. The study has been conducted based on the effect on the conduction band energy profile and also on the basic Analog Figure of Merits (FoMs) like Drain current (I_d) , Transconductance (g_m) , Output Resistance (r_o) , Intrinsic Gain $(g_m r_o)$. It has been observed that though Schottky-HEMTs have higher transconductance and faster switching transients, MOS-HEMTs are advantageous over the former as the latter experiences higher drive current capacity, lower threshold voltage, better I_{on}/I_{off} ratio and greater peak intrinsic gain.

Index Terms—Analog, AlGaN/GaN, Dual Gate (DG), Heterojunction, MOS-HEMT, Schottky-HEMT, Underlap.

I. INTRODUCTION

Traditional MOSFETs have been found to deliver slower performances owing to the impurity scattering in short channel devices, which eventually also give rise to undesirable heating and loss [1]. These challenges are addressed using modern high electron mobility transistors (HEMT) where a straddling based heterojunction is grown at the graded AlGaN/GaN interface [2-4]. GaN is a propitious material providing high breakdown voltage, good thermal stability, high average electron drift velocity along with a wide and tunable band gap and thus are preferred over conventional MOSFETs for high power and high speed electronic devices [5].

Although in HEMT devices, ionized impurity scattering is prevented and carrier mobility is also increased by the use of undoped AlGaN/GaN substrate, the gate leakage and buffer leakage currents are primary factors delimiting its performance and reliability. So, a Schottky contact is made between the gate metal and the channel, and the potential of the channel is varied by applying a voltage at the gate. Schottky-HEMTs undergo only

a two step photolithography processing procedure as oxide layer implantation is not required and are more economical. However, the greatest drawback is that turn-on voltage for Schottky is very low [6] and since, the threshold has to be lower than the turn-on voltage, they are not preferred for high voltage applications. However, the use of a gate oxide as an insulator between gate and channel helps to improve gate control in MOS-HEMT. Nevertheless, the distance between the gate and the channel being large MOSHEMTs undergo a partial degradation in its transconductance [7]. MOS-HEMT devices yet showcase a mitigation of gate leakage current of six to ten orders of magnitude with respect to a Schottky barrier HEMT device of similar architecture [8].

Schottky-HEMTs exhibit higher carrier mobility as compared to MOS-HEMTs [9]. This is explained from the fact that in short channel MOS-HEMTs, vertical electric fields due to gate voltage is much more pronounced. Thus the resultant of horizontal and vertical electric fields drives the carriers more towards the oxide at the channel oxide interface. On the contrary, weaker perpendicular electric fields are involved in Schottky-HEMTs which cause reduced carrier confinement near the MOS gate. This, in turn, results in less surface scattering and higher average electron velocity than MOS-HEMTs. Though Schottky-HEMTs showcases higher carrier mobility and faster switching, MOS-HEMTs are preferred more over the former as the latter has higher input impedance, higher gate capacitance, higher drive current capacity, lower leakage current and are much more preferred in high frequency RF applications [9].

In this study, an U-DG AlGaN/GaN heterostructured MOS-HEMT and a Schottky-HEMT has been analyzed and compared on the basis of their electrical characteristics and analog performance. The use of dual gates helps improve the channel control and reduce the short channel effects (SCEs). They also add to

higher on current (Ion) by better channel utilization [10-11]. Underlap creates a physical separation between Gate and Drain, supressing DIBL and hence reduces the off current (I_{off}) [8] as well as takes care of fringing losses [12-14].

II. DEVICE STRUCTURE

The two dimensional cross sectional views of an U-DG Al-GaN/GaN based heterostructured MOS-HEMT and a Schottky-HEMT with symmetric source and drain overlap on either sides of the two gates are depicted in Fig. 2 and Fig. 3 respectively. While a rectifying contact is formed between the gate and the channel in the Schottky-HEMT, the MOS-HEMT uses a layer of Hafnium based high K dielectric as gate oxide to achieve improved device performance [15]. As the Ion/Ioff ratio is maximum for the range 140 nm - 180 nm [16], therefore, in this paper, device channel thickness is chosen as 180 nm.

Device parameters	Length/Thickness
Source Underlap (L,)	200nm
Drain Underlap (L₄)	200nm
Source/Drain length (S)	200nm
Gate Length (L _z)	200nm
Gate Height (gh)	50nm
Oxide(HfO ₂) thickness (t _{ox})	10nm
AlGaN thickness (d1)	18nm
GaN thickness (d2)	180nm

Fig. 1. Device parameters and dimensions.

III. SIMULATION PROCEDURE

All the simulations relevant to the analysis have been performed using TCAD device simulator [17] and standard experimental data has been used for calibration [18]. The model specifications have been adjusted and tuned for incorporating the attributes and features of this experimental prototype into the simulator model. Mobility models have been included to handle the effects of carrier mobility degradation owing to the short channel effects (SCEs) like surface scattering and carrier velocity saturation due to the high lateral electric field governing device performance. Hence, the Shockley-Reed-Hall (SRH) Recombination Model is included for correctly determining the active carrier lifetime. The Fermi-Dirac statistics model is used for consistent device simulations. Newton Model is used so that simulations provide convergent solutions and Polarization Model is used for GaN based devices. The mole fraction, x of Al in $Al_xGa_{1-x}N$ is considered as 0.3 with Molybdenum as the gate material and metallic source and drain having a work function of 4.31 eV on Si_3N_4 substrate.

IV. ANALOG PERFORMANCE

The Analog FOMs that have been compared between a MOS-HEMT and a Schottky-HEMT include the variation of Drain

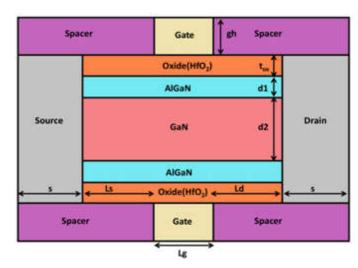


Fig. 2. Cross-sectional view of U-DG AlGaN/GaN MOS-HEMT with source and drain underlap.

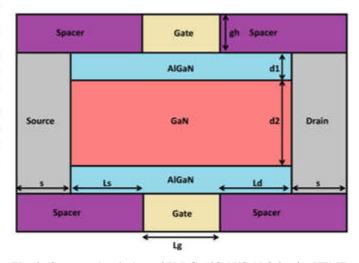


Fig. 3. Cross-sectional view of U-DG AlGaN/GaN Schottky-HEMT with source and drain underlap.

Current (I_D) with respect to both Gate to Source Voltage (V_{GS}) and Drain to Source Voltage (V_{DS}) , Transconductance (g_m) , Output Resistance (r_o) and Intrinsic Gain $(g_m r_o)$.

Fig. 4 and Fig. 5 show that conduction band energy varies continuously along the length of the channel for MOS-HEMT and Schottky-HEMT devices in OFF state and ON state respectively. The higher conduction band energy of the Schottky-HEMT with respect to the MOS-HEMT in OFF state as is evident from Fig. 4, implies that Schottky-HEMT experiences less DIBL than MOS-HEMT. As observed from the Fig. 5, both the devices have almost same conduction band energy variation throughout the length of the channel in ON state. In the central part of the channel beneath the gate together with the underlaps on either side, the conduction band energy in MOS-HEMT is slightly lower than that of Schottky-HEMT. This implies that since more number of carriers can overcome the barrier between source and channel and thus reach the drain, they recombine and contribute to larger drain current in MOS-HEMT for any specific V_{DS} .

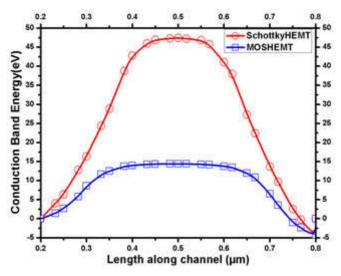


Fig. 4. Conduction band energy variation along the channel of U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT at $V_{DS}=5\mathrm{V}$ both devices are in OFF state.

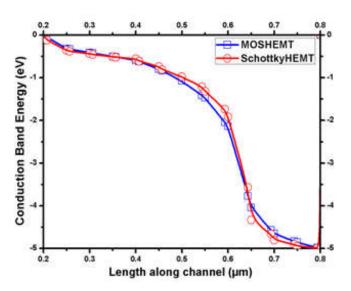


Fig. 5. Conduction band energy variation along the channel of U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT at $V_{DS}=5\,\mathrm{V}$ in ON state.

Fig. 6 illustrates the variation of I_D with respect to V_{DS} and as it depicts, I_D is almost same in linear region for both devices, but in saturation region I_D for MOS-HEMT is higher and this difference keeps increasing with increasing V_{DS} . This fact can be justified by the above explanation which shows MOS-HEMT has lower conduction band energy than Schottky-HEMT in the channel, and hence I_D will be higher for MOS device for a particular V_{DS} in saturation region.

In both the devices, a conduction channel is already present beforehand which enables current flow even at zero gate bias voltage. Increasing the gate bias voltage makes the channel further conducting, whereas, decreasing it drives the channel into cut-off. The negative gate voltage required to completely turn off

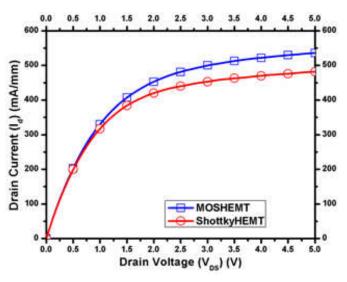


Fig. 6. Variation of I_D in linear scale as a function of V_{DS} at V_{GS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

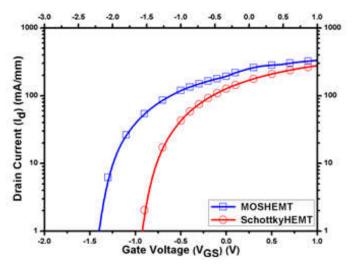


Fig. 7. Variation of I_D in logarithmic scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

the device is called threshold voltage, V_{th} . In Schottky-HEMT, V_{th} is the voltage required to fully deplete the doped channel region of the reverse biased Schottky junction, thereby removing the channel band bending at the gate/AlGaN interface. On the other hand, in MOS-HEMT, both the oxide band bending and the channel band bending have to be removed to turn off the device. Therefore, greater negative gate bias voltage is required for MOS-HEMT. So, absolute value of threshold voltage is greater for MOS-HEMT in comparison to Schottky-HEMT as is evident from Fig. 7.

In case of MOS-HEMT, the metallic oxide present between gate and substrate not only serves as an insulator by reducing the gate leakage current, but also increases the gate capacitance giving better gate control over channel thus accounting for improved device performance. As the charge stored per unit channel area, Q_{ch} varies directly with C_{ox} , the oxide capacitance per unit

area, the concentration of charge carriers per unit channel width will be more in MOS-HEMT than Schottky-HEMT due to the presence of C_{ox} term. Thus, as evident from Fig. 8, I_D of MOS-HEMT is greater than Schottky-HEMT for any specific V_{GS} .

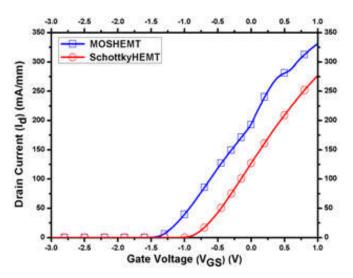


Fig. 8. Variation of I_D in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

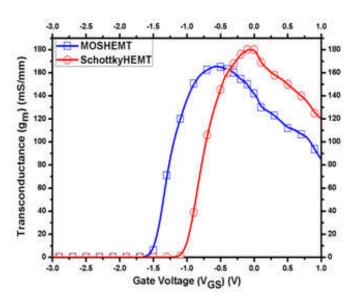


Fig. 9. Variation of g_m in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

Fig. 9 illustrates the transconductance curves for both the devices with varying V_{GS} . Surface roughness and scattering at the oxide-channel interface under strong vertical electric fields results in mobility degradation, causing the transconductance to experience a fall-off at about 0.5V beyond threshold in conventional MOSFETs. However, Schottky experiences higher carrier mobility in the channel as compared to MOS. This is because the carriers located in the inversion layer of the MOS have a wavefunction extending into the oxide which causes their surface mobility to drop than that of the bulk material. On the other hand,

as the depletion layer in Schottky separates the carriers from the surface, their mobility is close to the bulk material. Lower mobility leads to lower transconductance. But since I_D is higher in MOS and the threshold is also more negative, the g_m - V_{GS} curve of MOS-HEMT starts at lower V_{GS} , increases and experiences an early fall off at a higher rate than that of Schottky and therefore a cross-over is observed of both the curves at approximately -0.5V after which the transconductance of Schottky always leads that of MOS.

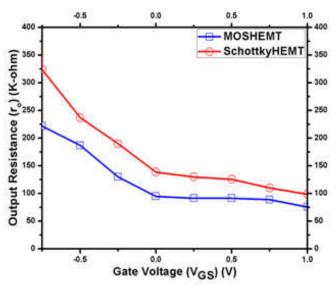


Fig. 10. Variation of r_o in linear scale as a function of V_{GS} for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

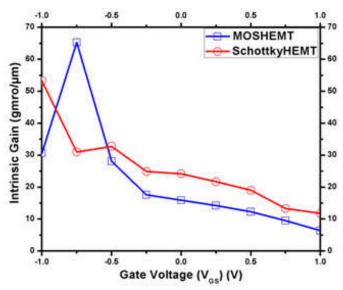


Fig. 11. Variation of $g_m r_o$ in linear scale as a function of V_{GS} at V_{DS} = 1.0 V for U-DG AlGaN/GaN MOS-HEMT and Schottky-HEMT.

It is observed from Fig. 10, output resistance of Schottky-HEMT is higher than that of MOS-HEMT. This can be justified from the fact that since, the drain current in MOS is higher than

that of Schottky because of the gate oxide layer which ensures better control over the channel, change in drain current for same change in drain voltage in saturation is also higher in MOS-HEMT, yielding lower r_o in MOS, compared to Schottky-HEMT.

The g_m and r_o values thus obtained illustrate the plot of intrinsic gain with V_{GS} in Fig. 11. Initially, the MOS-HEMT, having lower V_{th} remains in cut-off while the Schottky-HEMT is turned on. This accounts for the higher r_o and thus, higher intrinsic gain of the MOS-HEMT and hence the spike in the Fig. 11. Had both the devices been shown deeper in their ON states, the spike could have been avoided. However, as stated above, MOS-HEMT showcases a sharper decay in its transconductance than Schottky. Thus, $g_m r_o$ of Schottky-HEMT eventually becomes higher and thereafter this trend is maintained.

V. CONCLUSION

The simulation results indicate a substantial improvement in the output characteristics of MOS-HEMTs with respect to Schottky-HEMTs, with 10% higher saturation drain current values at V_{DS} =5V. Furthermore, MOS-HEMT has threshold voltage lower by 0.5V and 16.3% higher drain current values at V_{GS} =1V. Though the transconductance peak ($g_{m,max}$) is observed to be 8.4% more for Schottky with respect to MOS, the latter has a peak intrinsic gain ($g_m r_{o,max}$) greater by 18.4%. All these results show that MOS-HEMT is indeed a promising alternative to regular HEMT in terms of high power and high frequency applications.

VI. ACKNOWLEDGEMENT

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REFERENCES

- V. F. Conwell, E. and Weisskopf, "Theory of Impurity Scattering in Semiconductors," *Phys. Rev.*, vol. 77, no. 3, pp. 388–390, February 1950. DOI: 10.1103/PhysRev.77.388.
- [2] F. Schwierz, "The frequency limits of field-effect transistors: MOS-FET vs. HEMT," Proceedings, 9th International Conference on Solid-State and Integrated-Circuit Technology, pp. 1433–1436, 2008. DOI: 10.1109/ICSICT.2008.4734822.
- [3] JK. Zhang, M. Y. Cao, Y. H. Chen, L. Y. Yang, C. Wang, X. H. Ma, and Y. Hao, "Fabrication and characterization of V-gate Al-GaN/GaN high-electron-mobility transistors," *Chinese Phys. B*, vol. 22, no. 5, pp. 057304-1 057304-4, May 2013. DOI: 10.1088/1674-1056/22/5/057304.
- [4] A. Mondal, A. Roy, R. Mitra, "Comparative Study of Variations in Gate Oxide Material of a Novel Underlap DG MOS-HEMT for Analog/RF and High Power Applications," *Silicon*, vol. 0, no. 0, pp. 1-7, October 2019. DOI: 10.1007/s12633-019-00316-0
- [5] J. Zolper, Advanced device technologies for defense systems, in: *Proceedings of Device Research Conference* (University Park, TX, 2012) pp. 9–12.
- [6] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter, "Observation of a twodimensional electron gas in low pressure metalorganic chemical vapor deposited GaNAlxGa1xN heterojunctions," *Applied Physics Letters*, vol. 60, no. 24, pp. 3027-3029, March 1992. DOI: 10.1063/1.106798.

- [7] E. Tschumak, R. Granzer, J. K. N. Lindner F. Schwierz, K. Lischka, H. Nagasawa, M. Abe, and D. J. As, "Nonpolar cubic AlxGa1-xN/GaN heterojunction field-effect transistor on Ar+ implanted 3C–SiC (001)", Appl. Phys. Lett., vol. 96, no.25, pp. 3501-3503, June 2010. DOI: 10.1063/1.3455066.
- [8] H. Pardeshi, S. K. Pati, G. Raj, N. Mohankumar, C. K. Sarkar, "Effect of Underlap and gate length on device performance of an ALInN/GaN underlap MOFET," *Journal of Semiconductors*, vol. 33, no. 12, pp. 124001-1 - 124001-7, December 2012. DOI:10.1088/1674-4926/33/12/124001
- [9] T.Khan, D.Vasileska, T.J. Thornton, "Study of Cutoff Frequency Calculation in the subthreshold regime of operation of the SOI-MESFETS", NSTI Nanotech 2005 Technical Proceedings. 150-152, vol. 3, pp. 150-152, January 2005. ISBN 0 -9767985-2-2.
- [10] J. Colinge, "Multiple-gate SOI MOSFETs," Solid State Electronics, vol. 48, no. 6, pp. 897–905, June 2004. DOI: 10.1016/j.sse.2003.12.020.
- [11] M. Bhattacharya, J. Jogi, R. S. Gupta and M. Gupta, "Impact of doping concentration and donor-layer thickness on the dc characterization of symmetric double-gate and single-gate InAlAs/InGaAs/InP HEMT for nanometer gate dimension-A comparison," TENCON 2010 2010 IEEE Region 10 Conference, Fukuoka, pp. 134-139, November 2010.
- [12] Varghese, Arathy, Periasamy, Chinnamuthan, Bhargava,"Dielectric Modulated Underlap Based AlGaN/AlN/GaN MOS-HEMT for Label Free Bio-Detection," Lava on Journal of Nanoelectronics and Optoelectronics, vol. 14, no. 8, pp. 1064-1071, August 2019. Publisher: American Scientific Publishers.
- [13] M.Bo'zani'c and S.Sinha, "Emerging Transistor Technologies Capable of Terahertz Amplification: A Way to Re-Engineer Terahertz Radar Sensors" Sensors, vol. 19, no. 11, pp. 2454(1-32), May 2019. DOI: 10.3390/s19112454.
- [14] B.Buvaneswari and N.B.Balamurugan, "2D Analytical Modeling and Simulation of Dual Material DG MOSFET for Biosensing Application," *AEU-International Journal of Electronics and Communications*, vol. 99, pp. 193-200, 2019. DOI: 10.1016/j.aeue.2018.11.039.
- [15] K.P.Pradhan, S.K.Mohapatra, P.K.Sahu, D.K.Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET", *Microelectronics Journal*, vol. 45, no. 2, pp. 144-151, February 2014.
- [16] A. Roy, R. Mitra and A. Kundu, "Influence of Channel Thickness on Analog and RF Performance Enhancement of an Underlap DG AlGaN/GaN based MOS-HEMT Device," 2019 Devices for Integrated Circuit (DevIC), Kalyani, India, 2019, pp. 186-190.
- [17] A. Kundu, A. Dasgupta, R. Das, S. Chakraborty, A. Dutta, and C. K. Sarkar, "Influence of Underlap on Gate Stack DG-MOSFET for analytical study of Analog/RF performance," *Superlattices and Microstructures*, vol. 94, pp. 60–73, June 2016. DOI: 10.1016/j.spmi.2016.04.013.
- [18] M. Wei, Z. J. Cheng, X. J. Shuai, H. Yao,"Fabrication and Characteristics of AlInN/AlN/GaN MOS-HEMTs with Ultra Thin Atomic Layer Deposited Al2O3 Gate Dielectric," CHIN. PHYS. LETT., vol. 27, no. 12, pp.2008-2011, December 2010. DOI: 10.1088/0256-307X/27/12/128501.