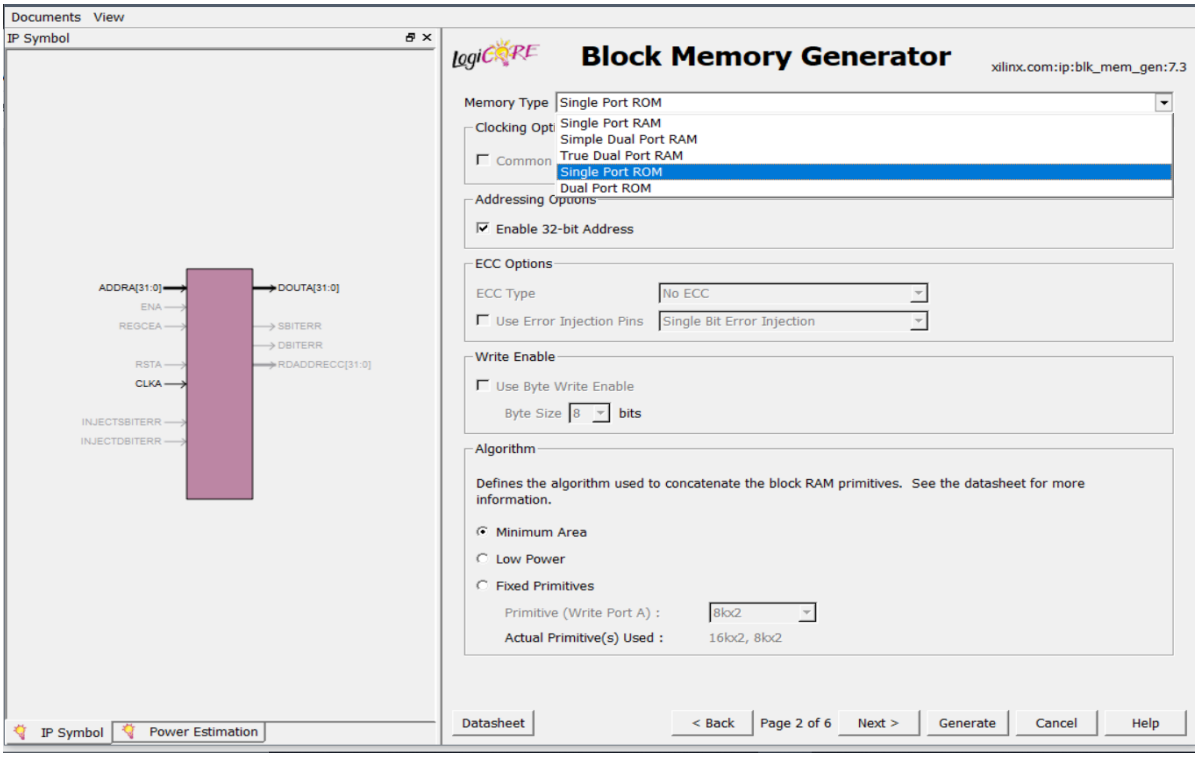
IP-CORE INITIALIZATION

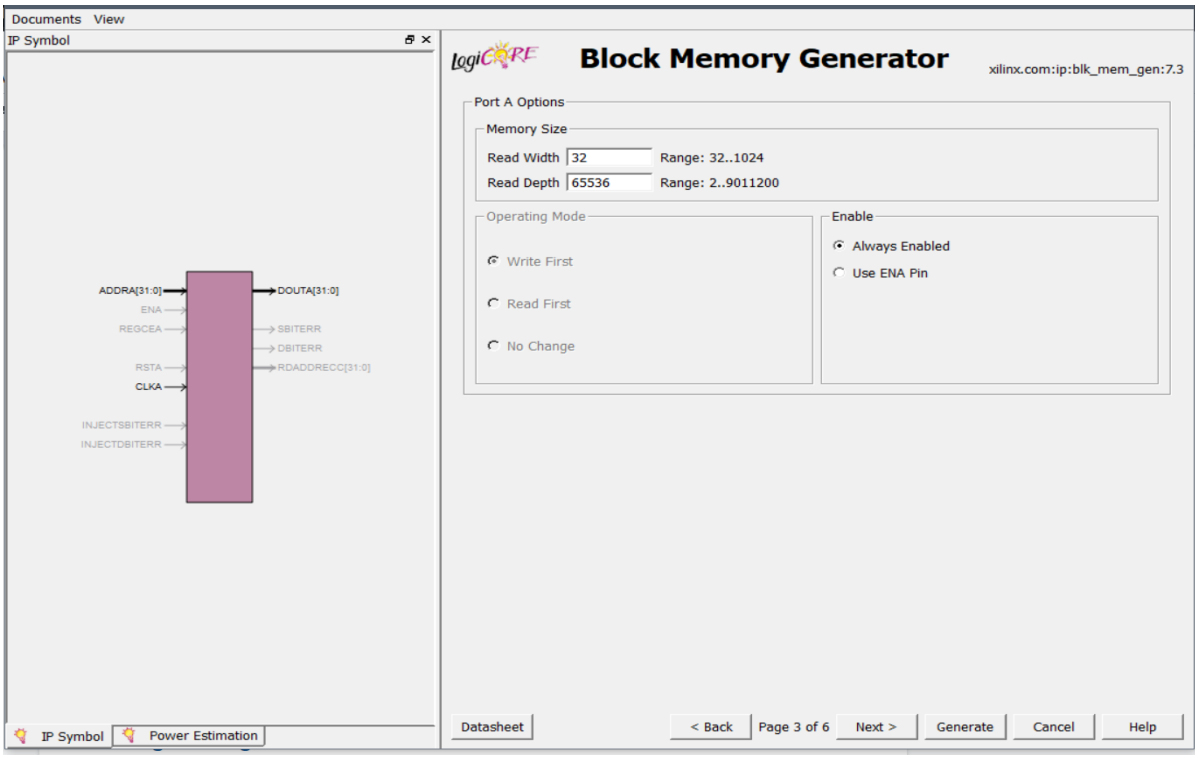
• Instruction Memory

The reader is requested to adhere to the following specifications while generating the Memory Unit for instructions. Please note that this memory module should be generated before synthesizing the top *KGP_RISC* module. The name of the module must be **SINGLE_PORT_ROM**.

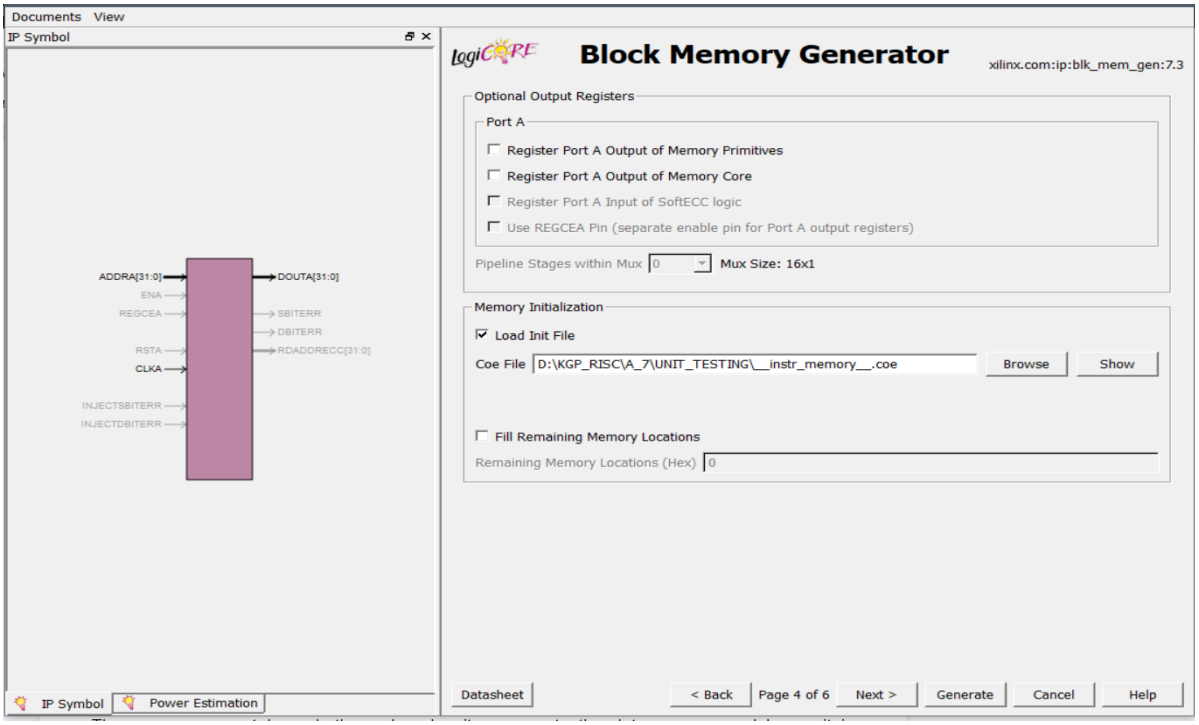
- **Memory Type** must be *Single Port ROM*. **Enable 32-bit Address** must be *checked*.



- Make sure that the **Read Width** is 32. Fill **Read Depth** as 65536.



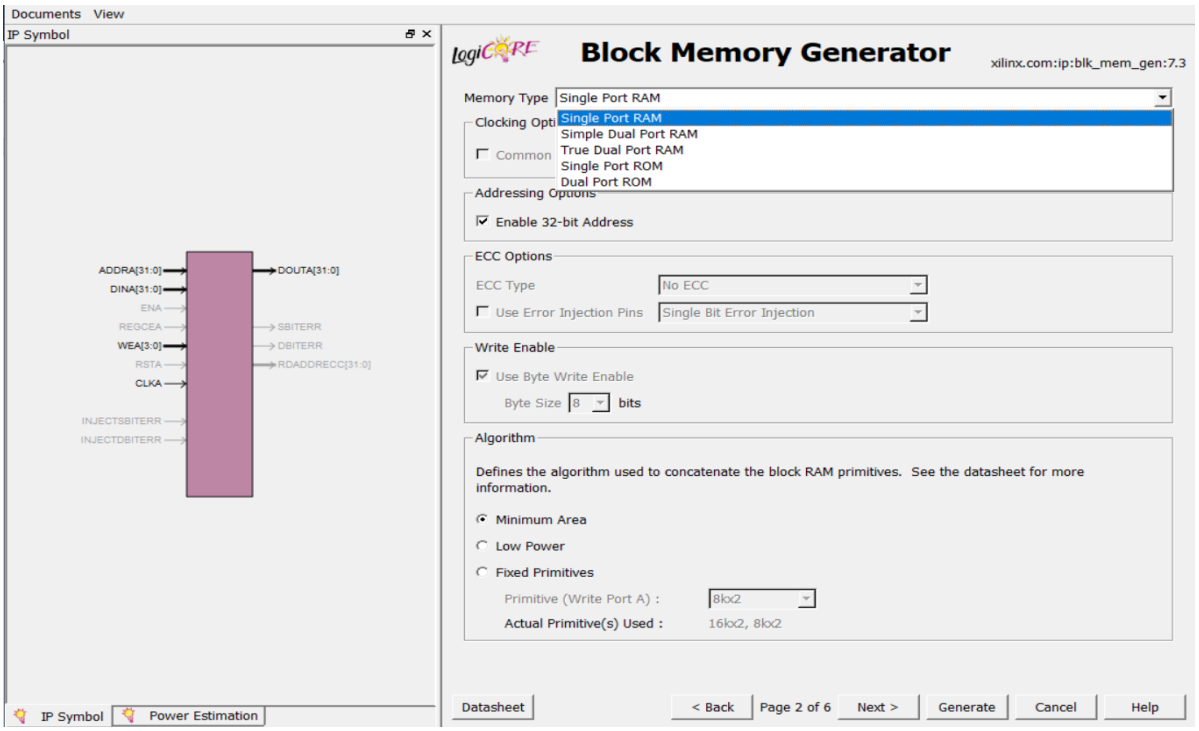
- **Load Init File** should be *checked* and any of the initialized instruction memories can be loaded in the form of a .coe file, depending upon whether you are performing a unit test or the integrated test. Which .coe files have to be loaded for which tests will be clearly specified later. The reader can also load their own .coe files.
Even if you do not load the .coe file at the time of generation, you can always go back to the block memory generator in order to load the file by simply double-clicking on the ip-core in the hierarchy.



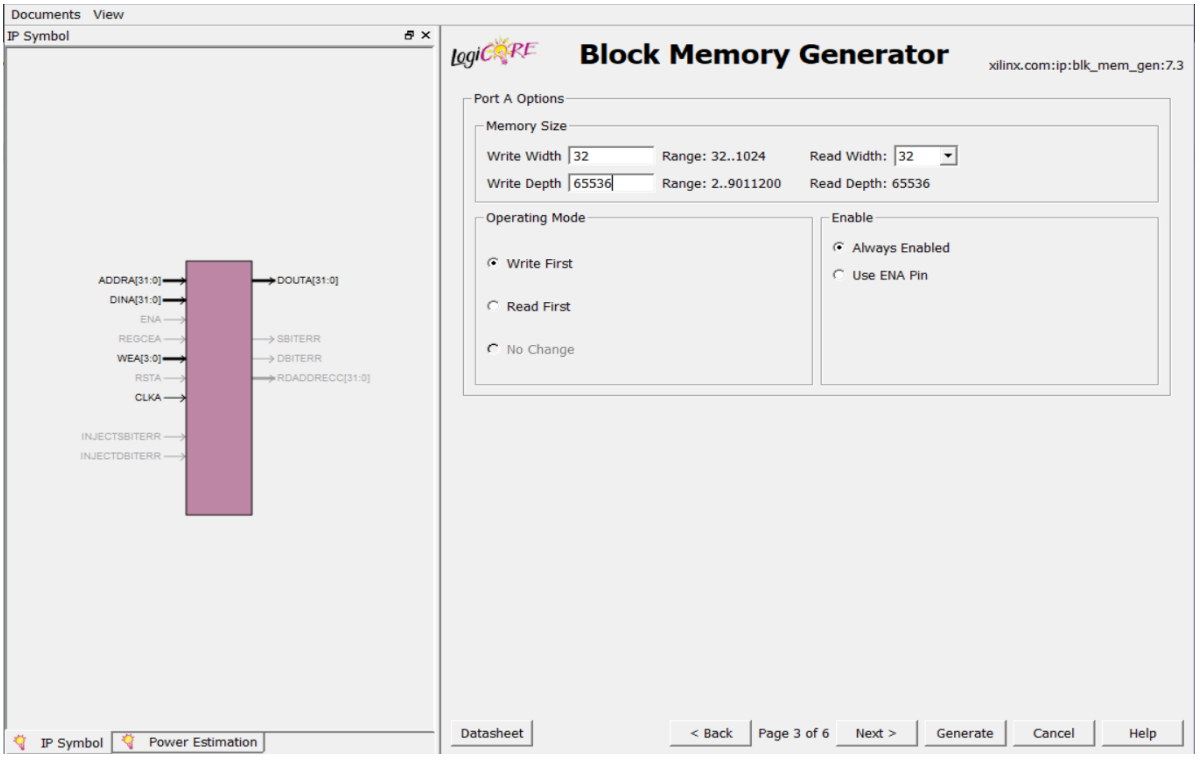
• Data Memory

The reader is requested to adhere to the following specifications while generating the Memory Unit for data or block-RAM. Please note that this memory module should be generated before synthesizing the top *KGP_RISC* module. The name of the module must be **SINGLE_PORT_RAM**.

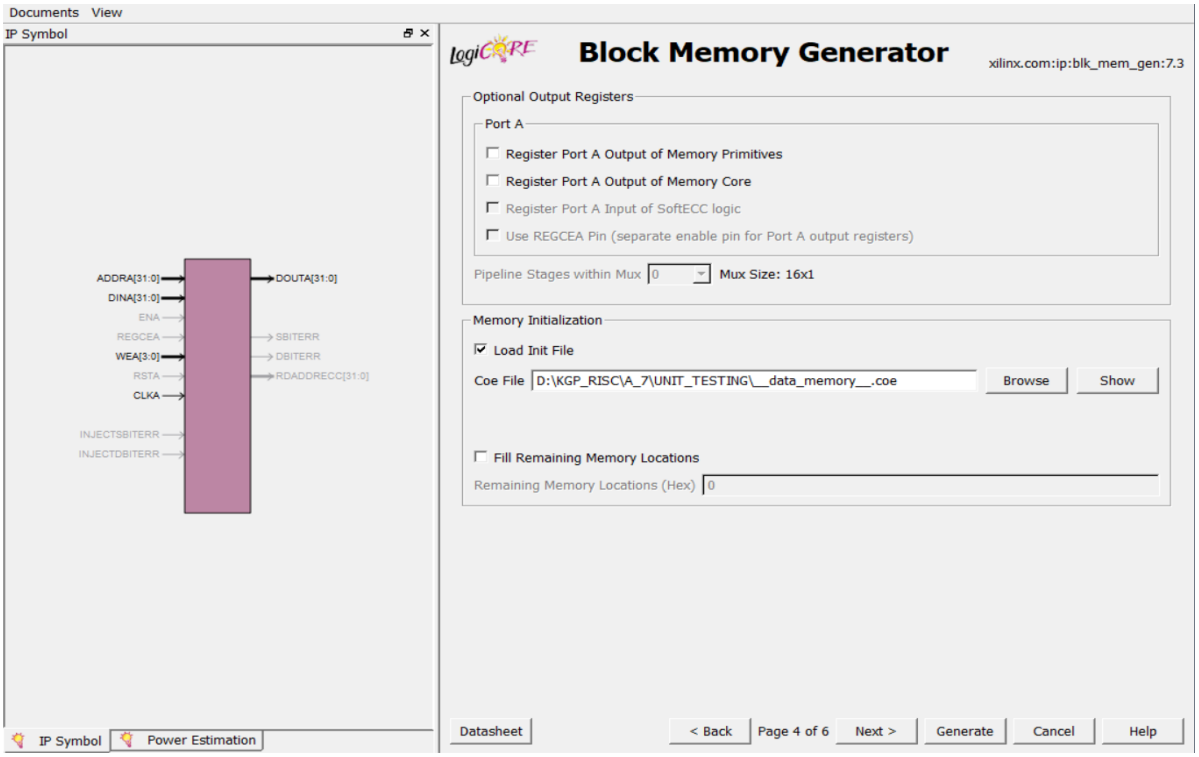
- **Memory Type** must be *Single Port RAM*. **Enable 32-bit Address** must be *checked*.



- Make sure that the **Write Width** and **Read Width** is 32. Fill **Write Depth** as 65536.



- **Load Init File** should be *checked* and any of the initialized data memories can be loaded in the form of a .coe file, depending upon which test you are performing. Which .coe files have to be loaded for which tests will be clearly specified later. The reader can also load their own .coe files.
Even if you do not load the .coe file at the time of generation, you can always go back to the block memory generator in order to load the file by simply double-clicking on the ip-core in the hierarchy.



• Initializing Single Port ROM

The reader will have to load the initial instruction memory into the *Single Port ROM* before simulating the *KGP-RISC* Processor. There are multiple testbenches written for unit testing and for integrated testing that require a suitable .coe file to be first loaded into the ROM before simulation.

Unit Testing

The testbenches that require a .coe file loaded into the ROM before simulating are as follows. Next to every testbench, the corresponding *.coe* file that has to be loaded is also mentioned.

TestBench_Datapath.v (A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/TestBench_Datapath.v)
Location: **A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/__instr_memory__.coe**

TestBench_InstructionMemory.v (A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/TestBench_InstructionMemory.v)
Location: **A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/__instr_memory__.coe**

Integrated Testing

The testbenches that require a .coe file loaded into the ROM before simulating are as follows. Next to every testbench, the corresponding *.coe* file that has to be loaded is also mentioned.

TestBench_BinaryToDecimal.v (A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/TestBench_BinaryToDecimal.v)
Location: **A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/__instr_memory__.coe**

TestBench_ComputeGCD.v (A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/TestBench_ComputeGCD.v)
Location: **A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/__instr_memory__.coe**

• Initializing Single Port RAM

The reader will have to load the initial instruction memory into the *Single Port RAM* before simulating the *KGP-RISC* Processor. There are multiple testbenches written for unit testing and for integrated testing that require a suitable .coe file to be first loaded into the RAM before simulation.

Unit Testing

The testbenches that require a .coe file loaded into the RAM before simulating are as follows. Next to every testbench, the corresponding *.coe* file that has to be loaded is also mentioned.

TestBench_Datapath.v (A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/TestBench_Datapath.coe)
Location: **A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/__data_memory__.coe**

TestBench_DataMemory.v (A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/TestBench_DataMemory.coe)
Location: **A7_19CS10044_19CS30053/KGP_RISC/UNIT_TESTING/__data_memory__.coe**

Integrated Testing

The testbenches that require a .coe file loaded into the ROM before simulating are as follows. Next to every testbench, the corresponding *.coe* file that has to be loaded is also mentioned.

Note that the input arguments for the algorithm implemented in the assembly code are taken from the data memory. So different test cases will correspond to different initializations of the data memory. Hence depending on the test case ID, the suitable *.coe* file should be loaded into the RAM.

TestBench_BinaryToDecimal.v (A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/TestBench_BinaryToDecimal.v)
Location:

A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/__test_case_01__.coe
A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/__test_case_02__.coe
A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/BINTODEC/__test_case_03__.coe

TestBench_ComputeGCD.v (A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/TestBench_ComputeGCD.v)
Location:

A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/__test_case_01__.coe
A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/__test_case_02__.coe
A7_19CS10044_19CS30053/KGP_RISC/INTEGERATED_TESTING/GCD/__test_case_03__.coe