

Introduction to Embedded System Design

Introduction to MSP430, MSP430 Architecture

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Introduction to MSP430

- MSP430 is a microcontroller family from Texas Instruments.
- It is one of the simplest microcontroller families from TI.
- ‘MSP’ stands for Mixed Signal Processor.
- It is a 16-bit processor (AB = 16 bit or 20 bit and DB =16 bit) designed for low power applications.
- It can be used for
 - General purpose sensing and measurement
 - Capacitive touch sensing
 - Ultrasonic sensing

Introduction to MSP430

- MSP430 series was launched in 1993 in Europe and in 1997 worldwide.
- The series has more than 500 different microcontrollers.
- MSP430 series support low power operation, over 5 low power modes are available.

MSP430 FAMILY

MSP430 SERIES	MSP430 FAMILY	FREQUENCY	MEMORY	GPIO
CAPACITIVE SENSING MCUs	FR25x/FR26x	16MHz	FRAM: UP TO 16KB SRAM: UP TO 4KB	15-19
VALUE LINE SENSING MCUs	FR2XX/FR4X	16MHz	FRAM: UP TO 16KB SRAM: UP TO 4 KB	16-64
	G2X/I2X	16MHz	FLASH: UP TO 56KB SRAM: UP TO 4KB	4-32
PERFORMANCE -SENSING MCUs	FR5X/FR6X	16MHz	FRAM: UP TO 256KB SRAM: UP TO 8KB	17-83
	F5X/F6X	25MHz	FLASH: 512KB SRAM: UP TO 67 KB	29-90
OTHER MSP430 MCUs	F2X/F4X	16MHz	FLASH: UP TO 120KB SRAM: UP TO 8KB	14-80
	F1X	16MHz	FLASH: UP TO 120KB SRAM: UP TO 10KB	10-48

MSP430 Nomenclature

MSP430F2618ATZQWT-EP

Processor Family

CC = Embedded RF Radio
MSP = Mixed Signal Processor
XMS = Experimental Silicon

430 MCU Platform

Device Type

Memory Type	Specialized Application
C = ROM	FG = Flash Medical
F = Flash	CG = ROM Medical
FR = FRAM	FE = Flash Energy Meter
G = Flash (Value Line)	FW = Flash Electronic Flow Meters
L = No non-volatile memory	AFE = Analog Front End
	BT = Pre-programmed with Bluetooth
	BQ = Contactless Power

Generation

1 series = up to 8 MHz
2 series = up to 16 MHz
3 series = Legacy OTP
4 series = up to 16 MHz w/ LCD

5 series = up to 25 MHz
6 series = up to 25 MHz w/ LCD
0 = Low Voltage Series

Family

Series and Device Number

Optional: A = revision

Optional: Temperature range

S = 0°C to 50°C
I = -40°C to 85°C
T = -40°C to 105°C

Packaging

www.ti.com/packaging

Optional: Distribution format

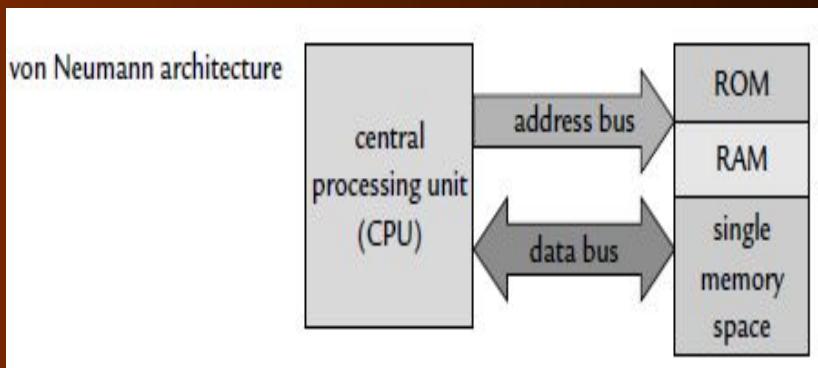
T = Small Reel (7-in)
R = Large Reel (11-in)
No markings = Tube or Tray

Optional: Additional features

*-Q1 = Automotive qualified
*-EP = Enhanced product (-40°C to 125°C)
*-HT = Extreme temp parts (-55°C to 150°C)

MSP430G2x53 Features

- 16-BIT RISC Architecture
- Von Neumann Memory Architecture



MSP430G2x53 Features

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - Active Mode: 230 μ A at 1 MHz, 2.2 V
 - Standby Mode (LPM): 0.5 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power Saving Modes (LPM0 -LPM4)
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μ s

MSP430G2x53 Features

- **62.5ns Instruction Cycle Time (register to register operation)**
- **Basic Clock Module Configurations**
 - Internal Frequencies up to 16 MHz with four calibrated frequencies - 1MHz, 8Mhz, 12Mhz, 16Mhz.
 - Internal Very-Low-Power Low Frequency (LF) Oscillator.
 - 32-kHz Crystal as external clock source
 - External Digital Clock Source

MSP430G2x53 Features

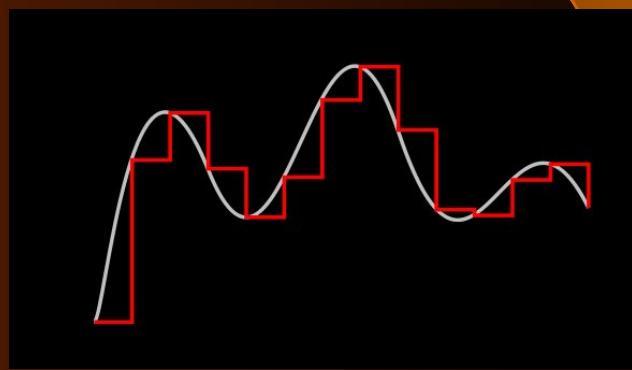
- **Two 16-Bit Timer_A With Three Capture/Compare Registers**
 - A timer is a hardware counter. Since 16 bit it counts from 0 to 65535.
- **Up to 24 Capacitive-Touch Enabled I/O Pins**
 - Inbuilt capacitive touch feature on all GPIO Pins

MSP430G2x53 Features

- **Universal Serial Communication Interface (USCI)**
 - UART
 - IrDA Encoder and Decoder
 - Synchronous SPI (Serial Peripheral Interface)
 - I2C (Inter IC Communication)
- **On-Chip Comparator**
- **Analog-to-Digital Cycle Time (A/D) Conversion**

MSP430G2x53 Features

- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter
 - Internal Reference(1.5 V or 2.5 V)
 - Sample and Hold with programmable sample periods
 - Eight External Input channels



MSP430G2x53 Features

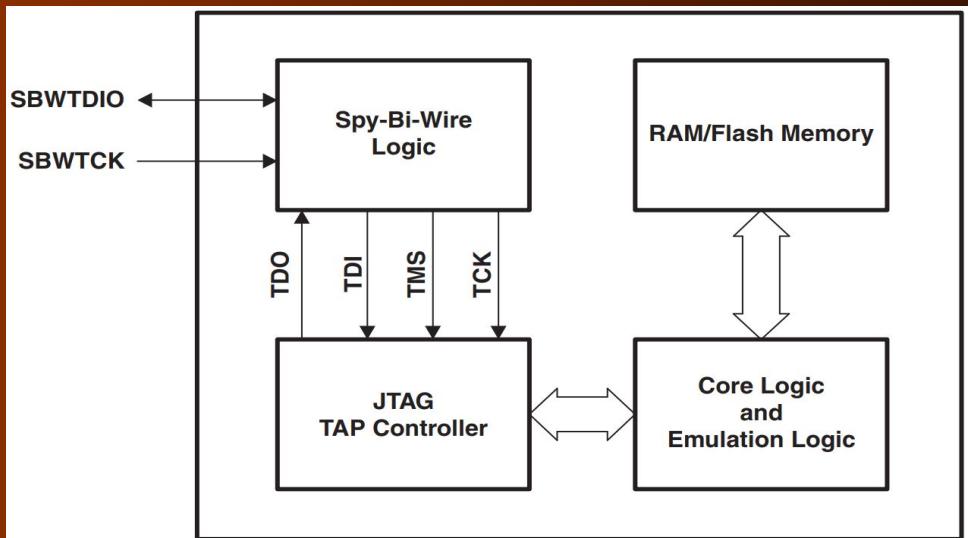
- Brownout Detector
- Serial Onboard Programming
- No External Programming Voltage Needed
- Programmable Code Protection by Security Fuse

MSP430G2x53 Features

- **On-Chip Emulation Logic With Spy-Bi-Wire**

Spy-Bi-Wire is a serialised JTAG protocol.

The two connections are a bidirectional data output (SBWTDO), and a clock (SBWTCK). The clocking signal is split into a period of three clock pulses, for each clock pulse the TDI, TDO and TMS signals are passed on the microcontroller via the bidirectional data output.



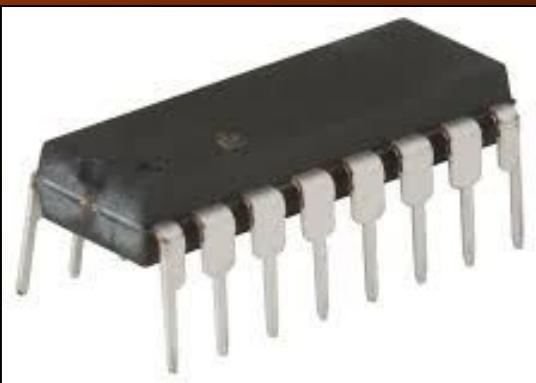
Spy-Bi-Wire Basic
Concept Diagram

MSP430G2x53 Features

- The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device.

MSP430 Package Options

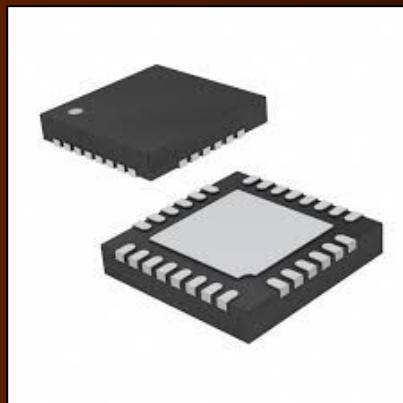
PDIP(PLASTIC DUAL IN-LINE PACKAGE)



TSSOP(THIN SHRINK SMALL OUTLINE PACKAGE)

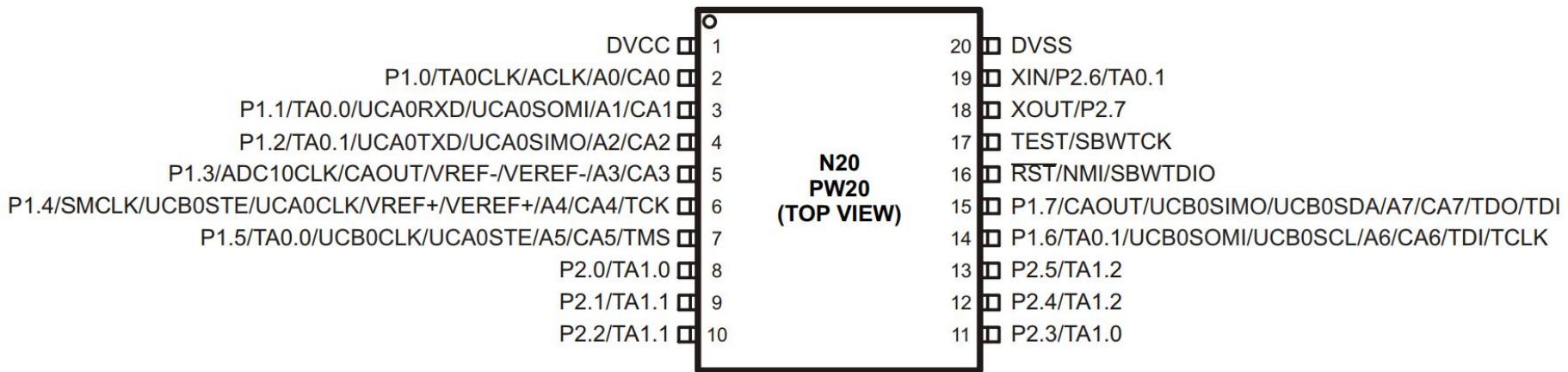


QFN(QUAD FLAT NO-LEAD)



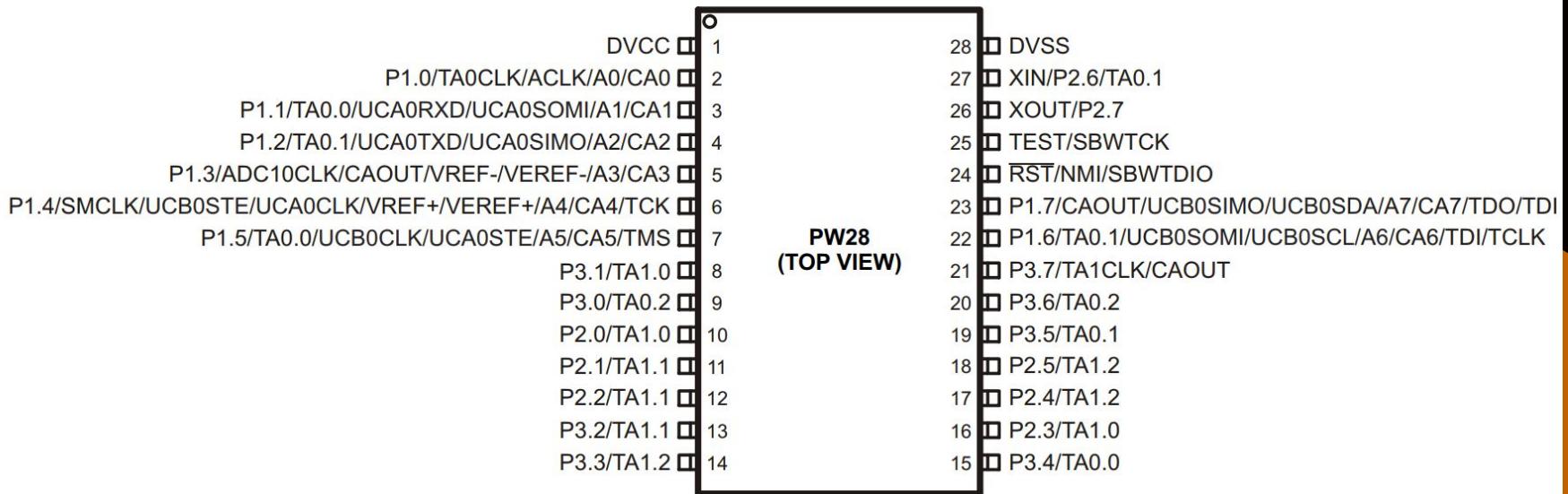
MSP430 PINOUT

Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP



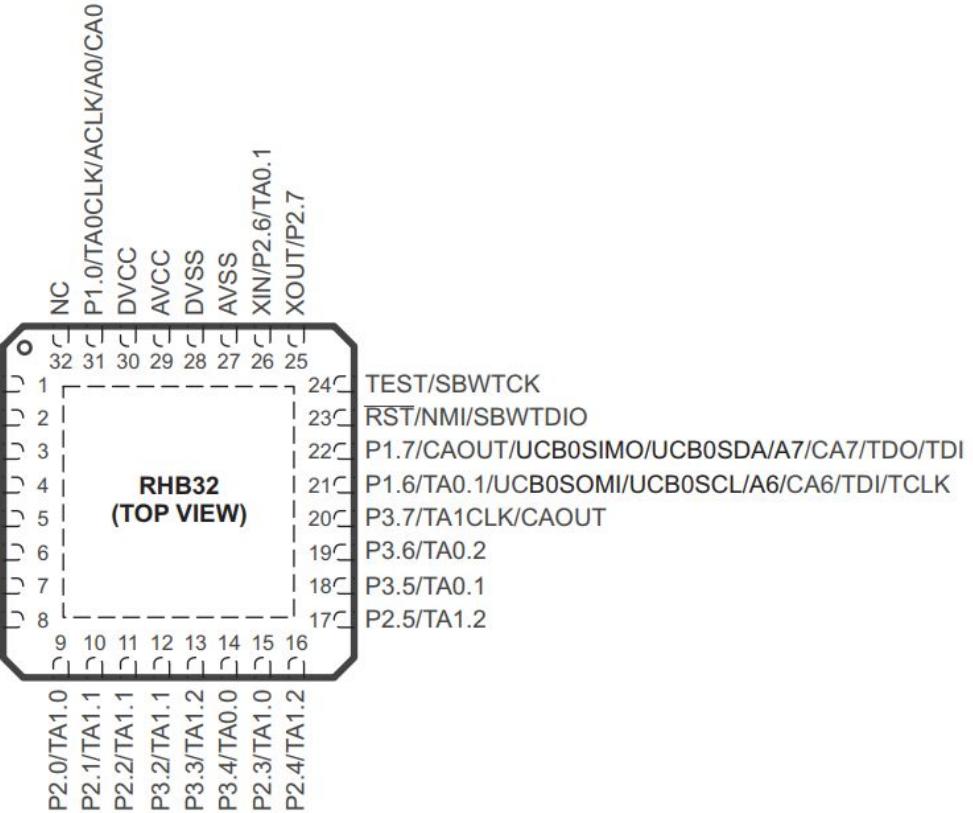
MSP430 PINOUT

Device Pinout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP



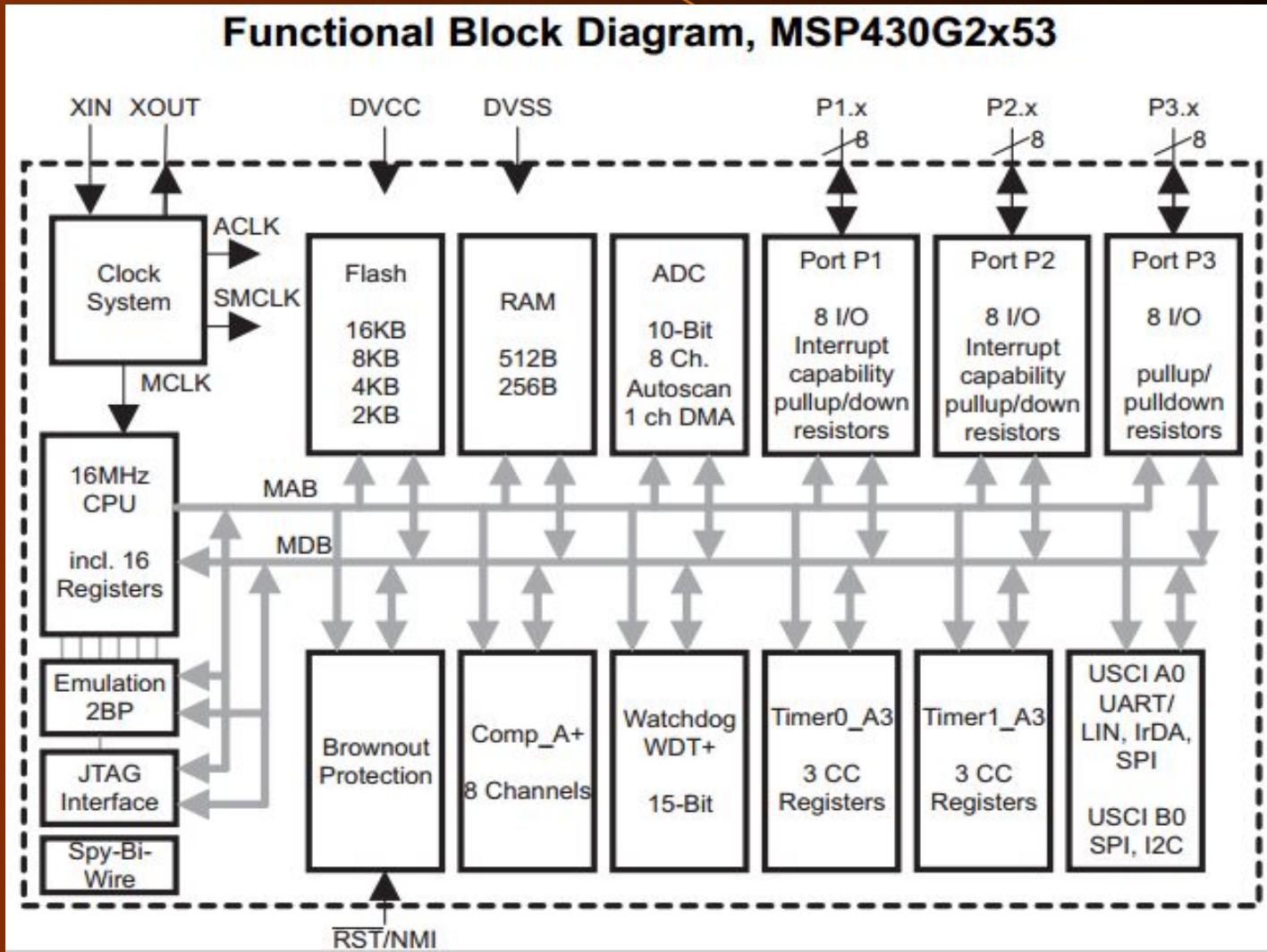
MSP430 PINOUT

Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN



NOTE: ADC10 is available on MSP430G2x53 devices only.

Functional Block Diagram



How to read the datasheet of the microcontroller

MSP430 Architecture

Introduction to the **MSP430 CPU**

- RISC Architecture with 27 core instructions and 7 addressing modes.
- 16-Bit Address Bus and 16-Bit Data Bus
- A set of 16 16-Bit Registers reduces fetches to memory
- Maximum clock frequency:- 16MHz(G-Series)
25MHz(F-Series)
- Constant generator provides six most used immediate values and reduces code size.
- Direct memory-to-memory transfers without intermediate register holding.
- Word and byte addressing and instruction formats.

Memory Architecture

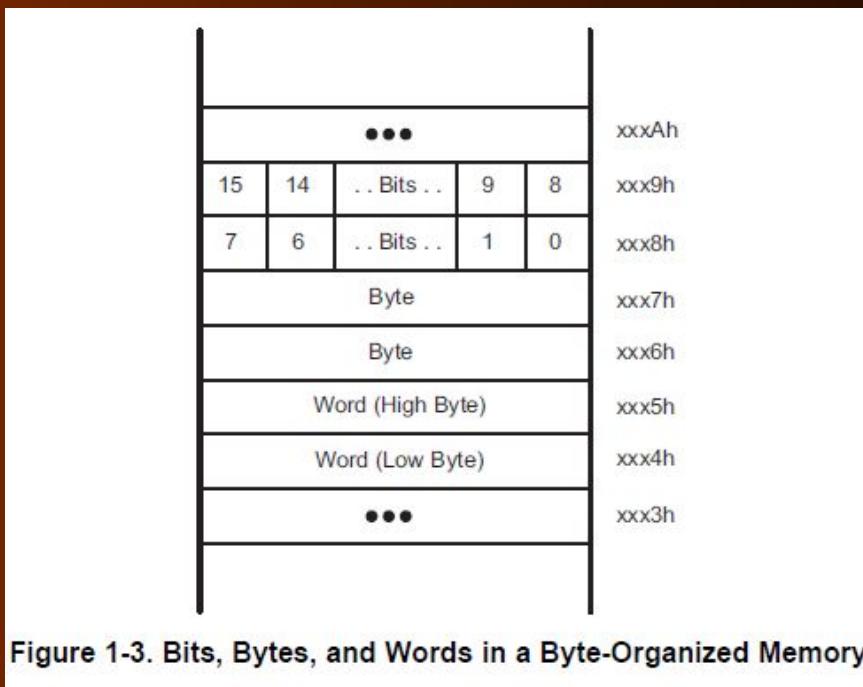
- MSP430 has Von Neumann Memory Architecture.
In von Neumann architecture there is only one set of addresses which cover both volatile and non-volatile memories.
- Address Bus is 16 bits wide, so $2^{16} = 65,536 = 64K$ addresses. So, Address Range is 0x0000 to 0xFFFF.
- MSP430X has an Address Bus of 20 Bits, so $2^{20} = 10,48,576$ addresses are possible.
- The memory data bus is 16 bits wide and can transfer either a word of 16 bits or a byte of 8 bits.

Memory Architecture

- The address of a word is defined to be the address of the byte with the lower address, which must be even. Eg: the two bytes at 0x4000 and 0x4001 can be fetched as a word with address 0x4000 in a single cycle.
- Instructions are composed of words and therefore must lie at even addresses.

Memory Architecture

- Words are stored as two bytes in the memory in the little endian ordering
- In little endian ordering, the lower order byte is stored at the lower address and the higher order byte at higher address.



MSP430 G Series Memory Map

		MSP430G2153	MSP430G2253 MSP430G2213	MSP430G2353 MSP430G2313	MSP430G2453 MSP430G2413	MSP430G2553 MSP430G2513
Memory	Size	1kB	2kB	4kB	8kB	16kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xFC00	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000	0xFFFF to 0xC000
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
RAM	Size	256 Byte	256 Byte	256 Byte	512 Byte	512 Byte
		0x02FF to 0x0200	0x02FF to 0x0200	0x02FF to 0x0200	0x03FF to 0x0200	0x03FF to 0x0200
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

Memory Organization (Flash)

- MSP430 flash memory is partitioned into segments. A segment is the smallest size of flash memory that can be erased.
- The flash memory is partitioned into main and information memory sections.
- The differences between the two sections are the segment size and the physical addresses. The information memory has four 64-byte segments. The main memory has one or more 512-byte segments.

Memory Organization (Flash)

- The start address of Flash/ROM depends on the amount of Flash/ROM present and varies by device.
- The end address for Flash/ROM is 0xFFFF for devices with less than 60KB Flash/ROM.
- Flash can be used for both code and data but is generally used as code memory. The code memory holds the program.
- The interrupt vectors are used to handle the interrupts. The interrupt vector table is mapped into the upper 16 words of Flash/ROM address space, with the highest priority interrupt vector at the highest Flash/ROM word address (0xFFFFE).

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	Flash Code Memory (lower boundary varies)
0xFFB0	
0xF000	
0xEFFF	
0x1100	
0x10FF	
0x1000	Flash Information Memory
0x0FFF	
0x0C00	Bootstrap Loader (BSL)
0x0BFF	
0x0280	
0x027F	RAM (upper boundary varies)
0x0200	
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

8.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to OFFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range ⁽¹⁾	PORIFG RSTIFG WDTIFG KEYV ⁽²⁾	Reset	0FFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG ⁽⁴⁾	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG ⁽²⁾⁽⁴⁾	maskable	0FFF8h	28
Comparator_A+	CAIFG ⁽⁴⁾	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG ⁽⁴⁾	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG ⁽⁵⁾⁽⁴⁾	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I ² C status	UCA0RXIFG, UCB0RXIFG ⁽²⁾⁽⁵⁾	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I ² C receive/transmit	UCA0TXIFG, UCB0TXIFG ⁽²⁾⁽⁶⁾	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG ⁽⁴⁾	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7 ⁽²⁾⁽⁴⁾	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See ⁽⁷⁾			0FFDEh	15
See ⁽⁸⁾			0FFDEh to OFFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) In SPI mode: UCB0RXIFG. In I²C mode: UCALIFG, UCNACKIFG, ICSTTIIFG, UCSTPIFG.

(6) In UART or SPI mode: UCB0TXIFG. In I²C mode: UCB0RXIFG, UCB0TXIFG.

(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.

(8) The interrupt vectors at addresses 0FFDEh to OFFC0h are not used in this device and can be used for regular program code if necessary.

Memory Organization (Information Memory)

- Information memory is a 256B block of flash memory that is intended for storage of nonvolatile data.
- Memory address range is: 0x1000h to 0x10FFh.
- The information memory has 4 segments of 64 bytes each. Segment A contains factory calibration data for the DCO in the MSP430G2553.
- After reset, segment A is protected against programming and erasing.

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	Flash Code Memory (lower boundary varies)
0xF000	
0xEFFF	
0x1100	
0x10FF	Flash Information Memory
0x1000	
0x0FFF	Bootstrap Loader (BSL)
0x0C00	
0x0BFF	
0x0280	
0x027F	RAM (upper boundary varies)
0x0200	
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

Memory Organization (Information Memory)

- Bootstrap Loader memory is a 1023B block of flash memory that is intended for storage of nonvolatile data.
- Memory address range is: 0x0C00h to 0xFFFFh.
- Bootstrap Loader (BSL) memory space contains code which is invoked when the controllers enters into BSL programming mode

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	
0xF000	Flash Code Memory (lower boundary varies)
0xEFFF	
0x1100	
0x10FF	
0x1000	Flash Information Memory
0x0FFF	
0x0C00	Bootstrap Loader (BSL)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

Memory Organization (RAM)

- RAM is used for data/variables.
- RAM starts at 0200h. The end address of RAM depends on the amount of RAM present and varies by device.
- MSP430G2553 has 512 Bytes of RAM.

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	
0xF000	Flash Code Memory (lower boundary varies)
0xEFFF	
0x1100	
0x10FF	
0x1000	Flash Information Memory
0x0FFF	
0x0C00	Bootstrap Loader (BSL)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

Memory Organization (Peripheral Modules)

- Peripheral registers are used by CPU to access and configure peripherals.
- The address space from 0100 to 01FFh is reserved for 16-bit peripheral modules. These modules should be accessed with word instructions. If byte instructions are used, only even addresses are permissible, and the high byte of the result is always 0.
- You can find the details of each peripheral register and its address in the ‘Peripheral File Map’ in the datasheet.

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	
0xF000	Flash Code Memory (lower boundary varies)
0xEFFF	
0x1100	
0x10FF	
0x1000	Flash Information Memory
0x0FFF	
0x0C00	Bootstrap Loader (BSL)
0x0BFF	
0x0280	
0x027F	RAM (upper boundary varies)
0x0200	
0x01FF	peripheral registers (word access)
0x0100	
0x00FF	peripheral registers (byte access)
0x0100	
0x000F	special function registers (byte access)
0x0000	

Table 14. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10 (MSP430G2x53 devices only)	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
Timer1_A3	Capture/compare register	TA1CCR2	0196h
	Capture/compare register	TA1CCR1	0194h
	Capture/compare register	TA1CCR0	0192h
	Timer_A register	TA1R	0190h
	Capture/compare control	TA1CCTL2	0186h
	Capture/compare control	TA1CCTL1	0184h
	Capture/compare control	TA1CCTL0	0182h
	Timer_A control	TA1CTL	0180h
	Timer_A interrupt vector	TA1IV	011Eh
Timer0_A3	Capture/compare register	TA0CCR2	0176h
	Capture/compare register	TA0CCR1	0174h
	Capture/compare register	TA0CCR0	0172h
	Timer_A register	TA0R	0170h
	Capture/compare control	TA0CCTL2	0166h
	Capture/compare control	TA0CCTL1	0164h
	Capture/compare control	TA0CCTL0	0162h
	Timer_A control	TA0CTL	0160h
	Timer_A interrupt vector	TA0IV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Memory Organization (Peripheral Modules)

- The address space from 010h to 0FFh is reserved for 8-bit peripheral modules. These modules should be accessed with byte instructions.
- Read access of byte modules using word instructions results in unpredictable data in the high byte. If word data is written to a byte module only the low byte is written into the peripheral register, ignoring the high byte.

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	
0xF000	Flash Code Memory (lower boundary varies)
0xEFFF	
0x1100	
0x10FF	Flash Information Memory
0x1000	
0x0FFF	Bootstrap Loader (BSL)
0x0C00	
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

Table 15. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI_B0 I2C interrupt enable	UCB0CIE	06Ch
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
	USCI_B0 I2C slave address	UCB0SA	011Ah
	USCI_B0 I2C own address	UCB0OA	0118h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
ADC10 (MSP430G2x53 devices only)	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Comparator_A+	Comparator_A+ port disable	CAPD	05Bh
	Comparator_A+ control 2	CACTL2	05Ah
	Comparator_A+ control 1	CACTL1	059h
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P3 (28-pin PW and 32-pin RHB only)	Port P3 selection 2, pin	P3SEL2	043h
	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection 2	P2SEL2	042h
	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

Table 15. Peripherals With Byte Access (continued)

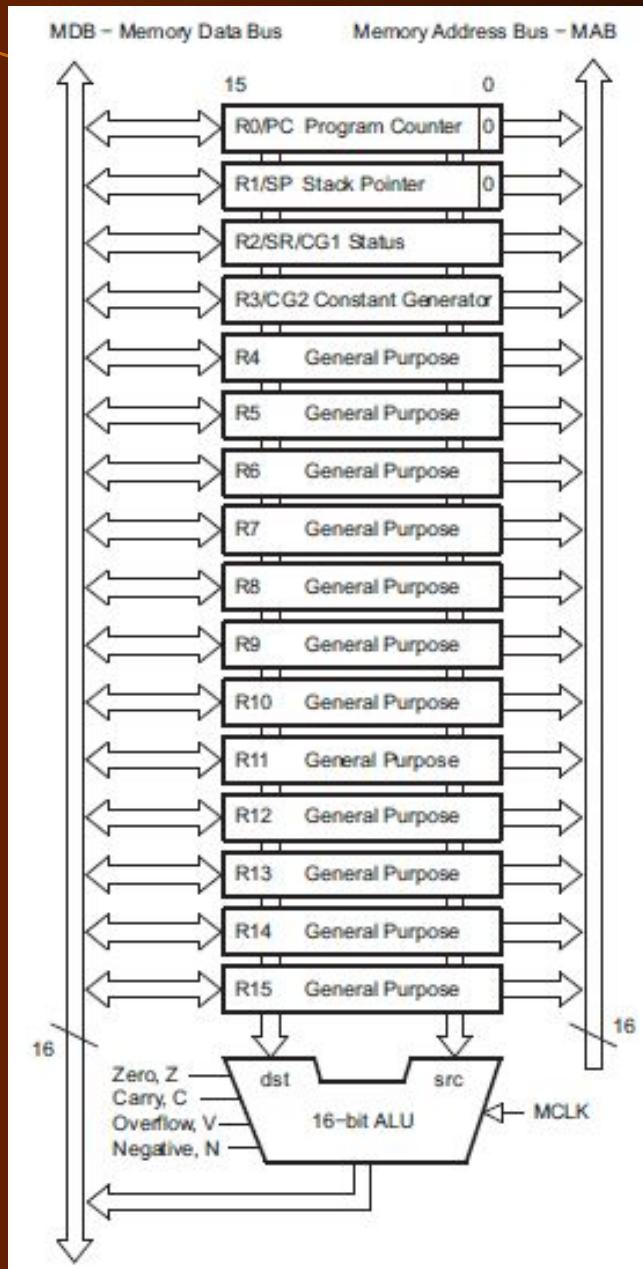
MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
Port P1	Port P1 selection 2	P1SEL2	041h
	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

Memory Organization (Special Function Registers)

- Some peripheral functions are configured in the SFRs. The SFRs are located in the lower 16 bytes of the address space, and are organized by byte. SFRs must be accessed using byte instructions only.
- MSP430G2553 has interrupt enables and interrupt flag registers as SFRs.

0xFFFF	Interrupt and Reset Vector Table
0xFFC0	
0xFFBF	Flash Code Memory (lower boundary varies)
0xF000	
0xEFFF	
0x1100	
0x10FF	Flash Information Memory
0x1000	
0x0FFF	Bootstrap Loader (BSL)
0x0C00	
0x0BFF	
0x0280	
0x027F	RAM (upper boundary varies)
0x0200	
0x01FF	peripheral registers
0x0100	(word access)
0x00FF	peripheral registers
0x0100	(byte access)
0x000F	special function registers
0x0000	(byte access)

MSP430 CPU



MSP430 CPU Block Diagram

CPU Registers

- 16 Registers: The generous set of 16 registers is characteristic of a RISC CPU.
- These Registers provide reduced instruction execution time.
- Register to register operation takes only clock cycle.
- 4 Special Purpose
 - Program Counter(PC)
 - Stack Pointer(SP)
 - Status Register(SR)
 - Constant Generator
- 12 General Purpose

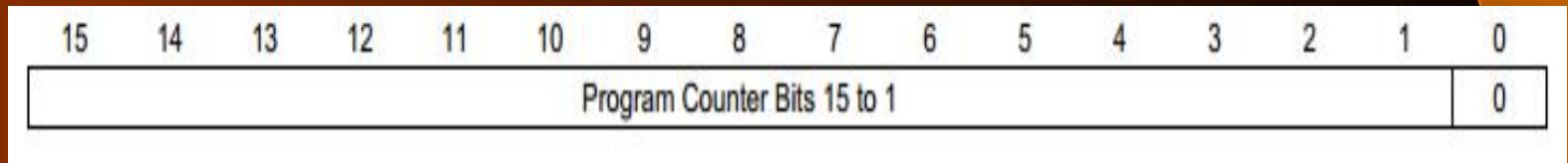
Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

CPU Registers

CPU Registers

Program Counter

- This contains the address of the next instruction to be executed. Instructions are composed of 1–3 words, which must be aligned to even addresses, so the LSB of the PC is hard-wired to 0.



CPU Registers

Stack Pointer

- The stack pointer is used by the CPU to store the return addresses of subroutine calls and interrupts.
- The SP is initialized into RAM by the user, and is aligned to even addresses.
- SP hold the address of the most recently added word in the stack and is automatically adjusted as the stack goes up and down.



CPU Registers

Status Register

- This contains a set of flags (single bits), whose functions fall into three categories.
 - The most commonly used flags are C, Z, N, and V, which give information about the result of the last arithmetic or logical operation. Decisions that affect the flow of control in the program can be made by testing these bits.
 - Setting the GIE bit enables maskable interrupts.
 - The final group of bits is CPUOFF, OSCOFF, SCG0, and SCG1, which control the mode of operation of the MCU.

Status Register

Bit	Description	
V	Overflow bit. This bit is set when the result of an arithmetic operation overflows the signed-variable range.	
	ADD (.B), ADDC (.B)	Set when: Positive + Positive = Negative Negative + Negative = Positive Otherwise reset
	SUB (.B), SUBC (.B), CMP (.B)	Set when: Positive – Negative = Negative Negative – Positive = Positive Otherwise reset
SCG1	System clock generator 1. When set, turns off the SMCLK.	
SCG0	System clock generator 0. When set, turns off the DCO dc generator, if DCOCLK is not used for MCLK or SMCLK.	
OSCOFF	Oscillator Off. When set, turns off the LFXT1 crystal oscillator, when LFXT1CLK is not use for MCLK or SMCLK.	
CPUOFF	CPU off. When set, turns off the CPU.	
GIE	General interrupt enable. When set, enables maskable interrupts. When reset, all maskable interrupts are disabled.	
N	Negative bit. Set when the result of a byte or word operation is negative and cleared when the result is not negative. Word operation: N is set to the value of bit 15 of the result. Byte operation: N is set to the value of bit 7 of the result.	
Z	Zero bit. Set when the result of a byte or word operation is 0 and cleared when the result is not 0.	
C	Carry bit. Set when the result of a byte or word operation produced a carry and cleared when no carry occurred.	

CPU Registers

Constant Generator Registers

- Six commonly-used constants are generated with the constant generator registers R2 and R3, without requiring an additional 16-bit word of program code. The constants are selected with the source-register addressing modes (As).
- The constant generator advantages are:
 - No special instructions required
 - No additional code word for the six constants
 - No code memory access required to fetch the constant

CPU Registers

General Purpose Registers

- The remaining 12 registers R4–R15 have no dedicated purpose and may be used as general working registers.
- They may be used for either data or addresses because both are 16-bit values, which simplifies the operation significantly.

MSP430 Instruction Set Architecture

Instruction Format

There are three formats of instructions in the MSP430:

- **Double operand:** Arithmetic and logical operations with two operands such as ADD R4,R5. Both operands must be specified in the instruction. This contrasts with accumulator-based architectures, where an accumulator or working register is used automatically as the destination and one operand.
- **Single operand:** A mixture of instructions for control or to manipulate a single operand, which is effectively the *source* for the addressing modes.
- **Jumps:** The jump to the destination rather than its absolute address, in other words the offset that must be added to the program counter.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Addressing Modes

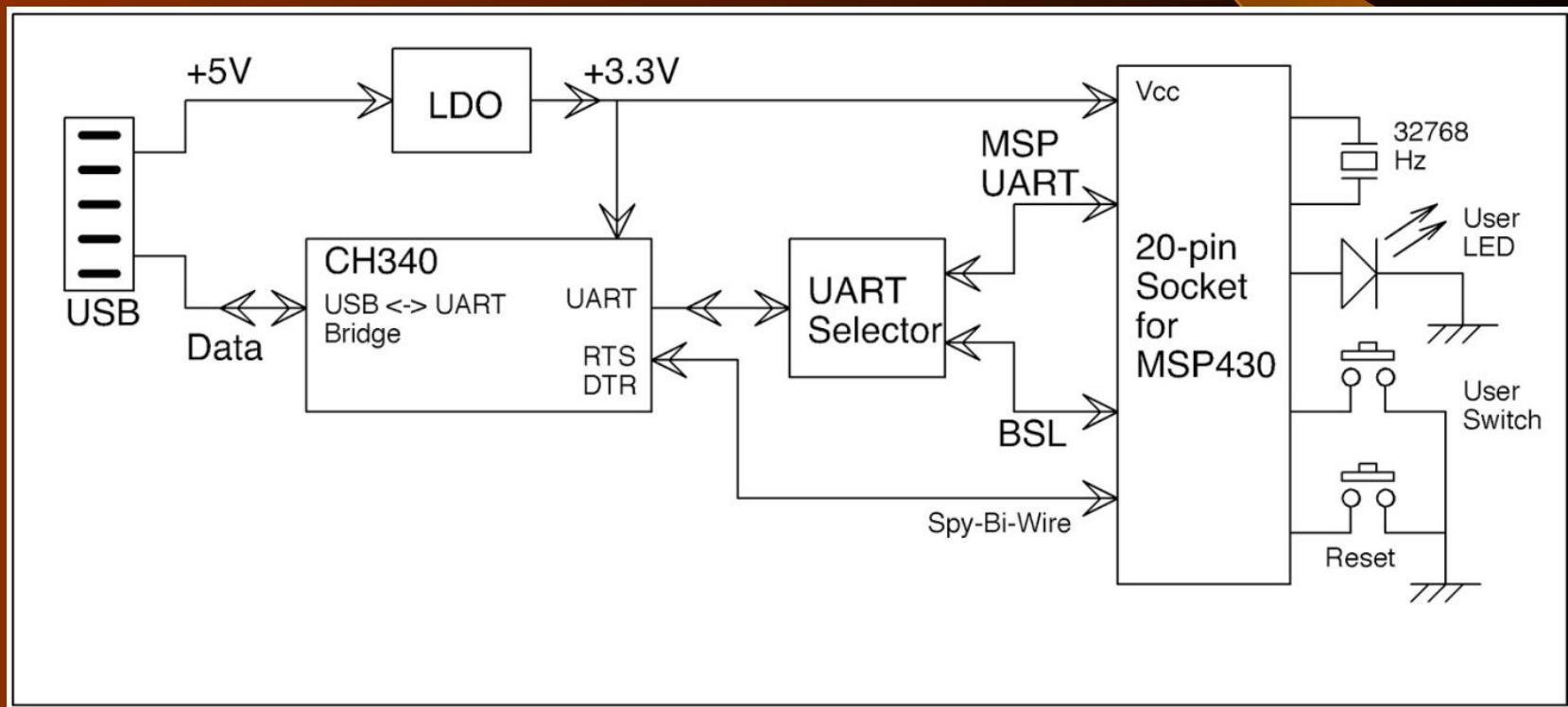
- Addressing modes are the ways in which operands can be specified.
- MSP430 has seven addressing modes. These are:
 1. Register Mode
 2. Indexed Mode
 3. Symbolic Mode
 4. Absolute Mode
 5. Indirect Register Mode
 6. Indirect Autoincrement Mode
 7. Immediate Mode

Source/Destination Operand Addressing Modes

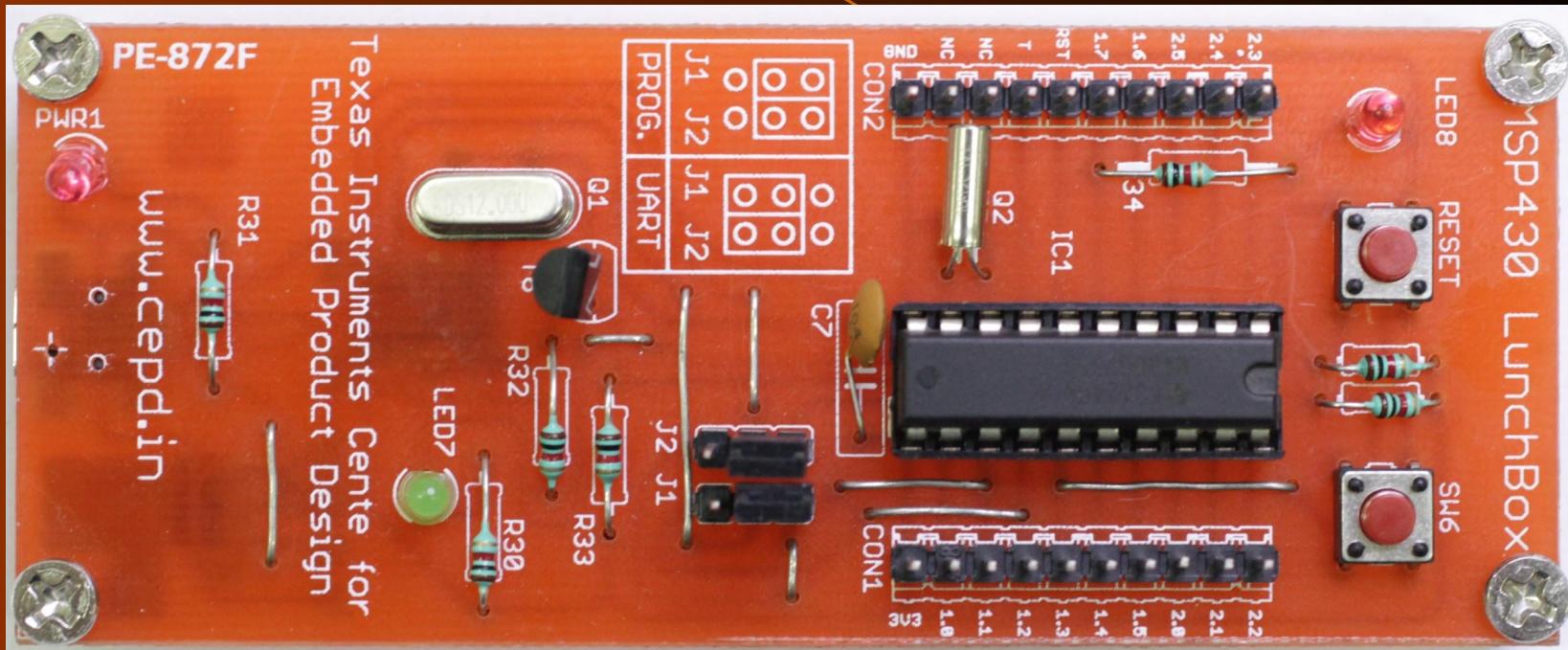
As/Ad	Addressing Mode	Syntax	Description
00/0	Register mode	Rn	Register contents are operand
01/1	Indexed mode	X(Rn)	(Rn + X) points to the operand. X is stored in the next word.
01/1	Symbolic mode	ADDR	(PC + X) points to the operand. X is stored in the next word. Indexed mode X(PC) is used.
01/1	Absolute mode	&ADDR	The word following the instruction contains the absolute address. X is stored in the next word. Indexed mode X(SR) is used.
10/-	Indirect register mode	@Rn	Rn is used as a pointer to the operand.
11/-	Indirect autoincrement	@Rn+	Rn is used as a pointer to the operand. Rn is incremented afterwards by 1 for .B instructions and by 2 for .W instructions.
11/-	Immediate mode	#N	The word following the instruction contains the immediate constant N. Indirect autoincrement mode @PC+ is used.

Introduction to MSP430 Lunchbox

MSP430 LunchBox is a low cost DIY platform for learning microcontrollers and physical computing.



MSP430 Lunchbox



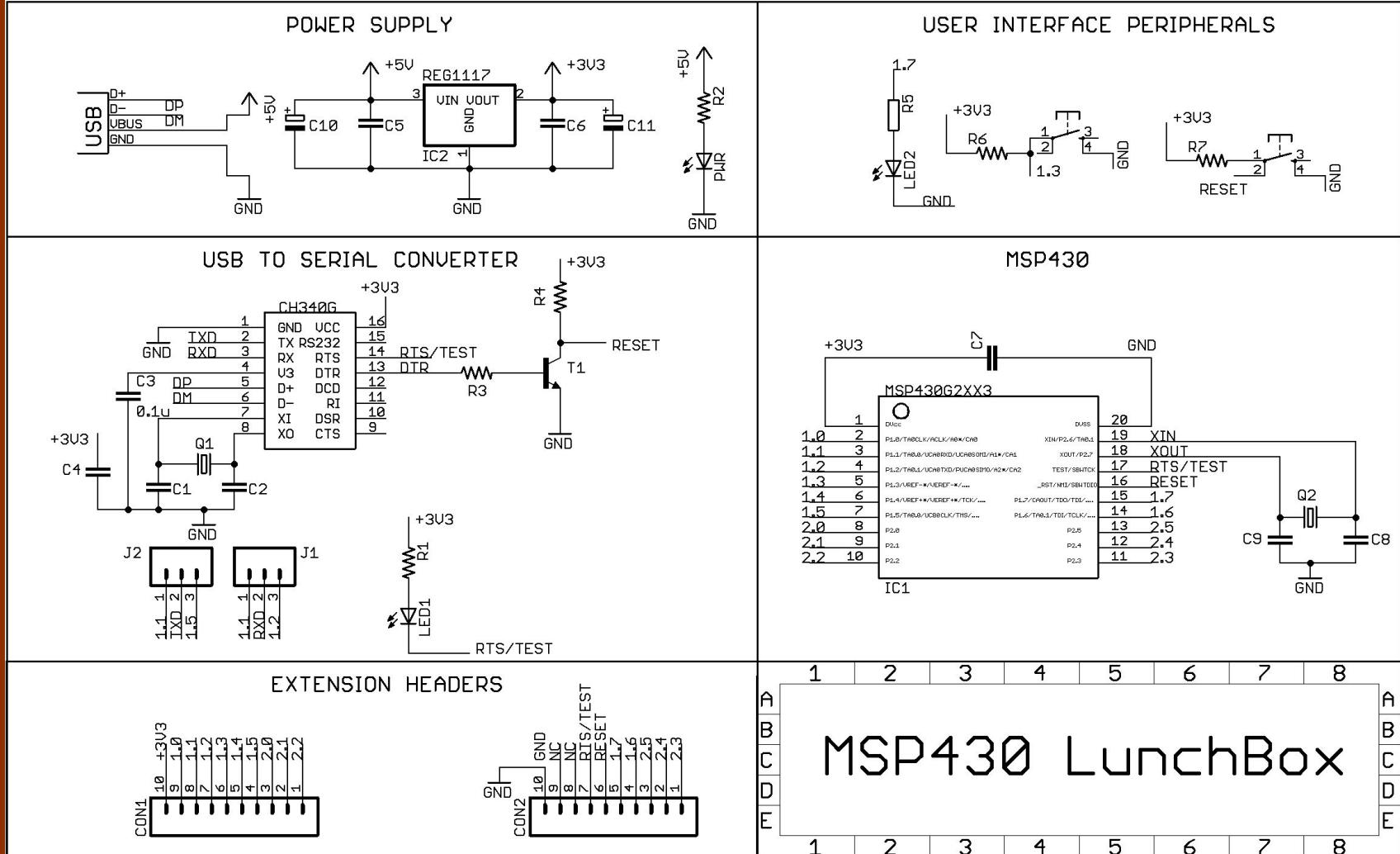
- Based on MSP430G2553 MCU
- On-board LED and push button for experimentation
- Programmable via TI Code Composer Studio

MSP430G2553

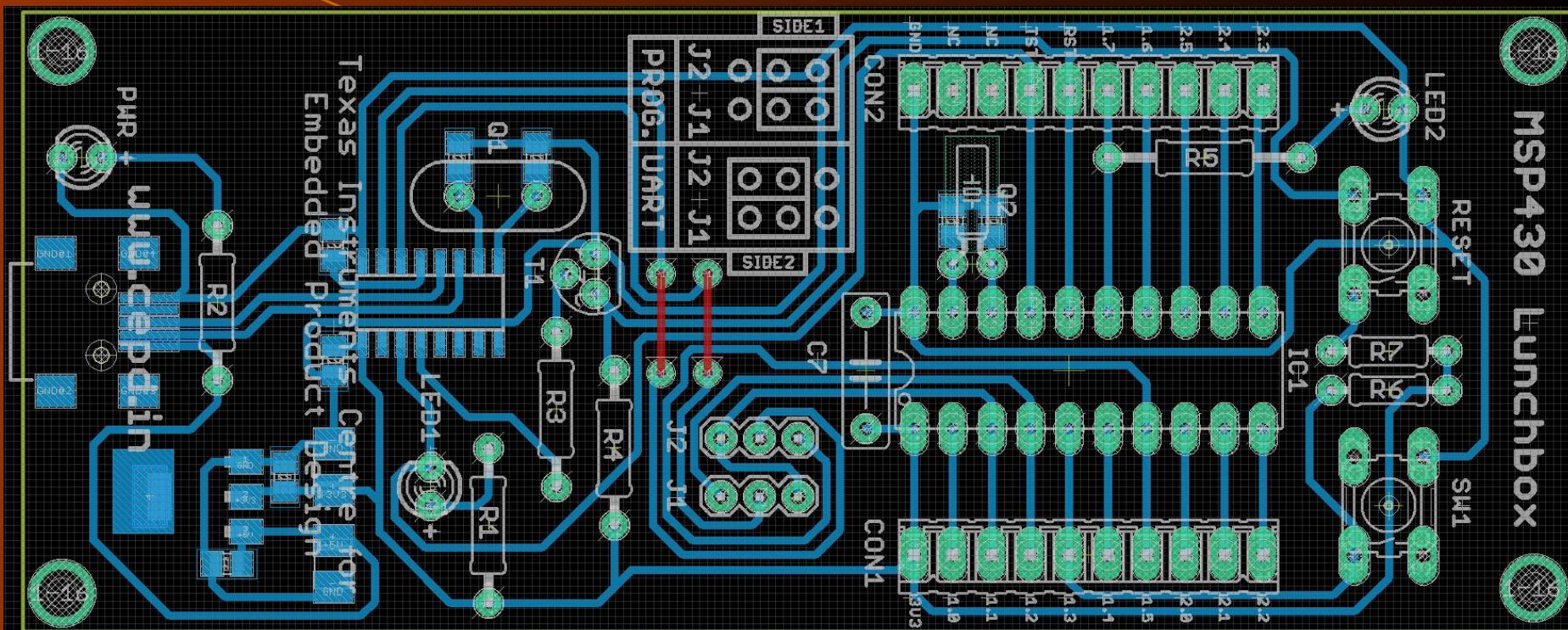


- 16 KB FLASH
- 512 BYTE RAM
- 16 GPIOs
- 8 CHANNEL ADC
- 2 TIMER_A3
- 8 CHANNEL COMPARATOR_A+

Lunchbox Schematic



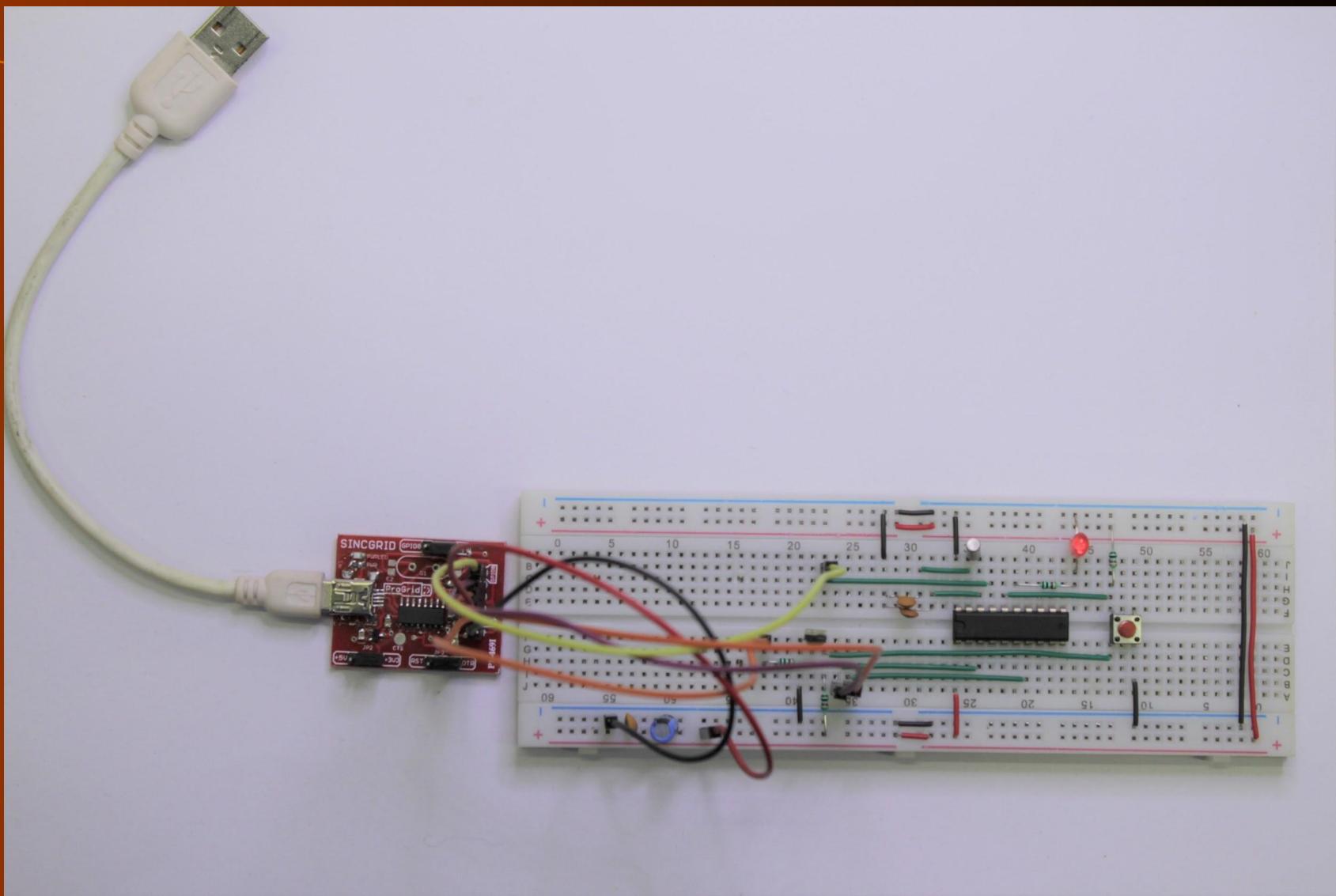
Lunchbox Board Layout



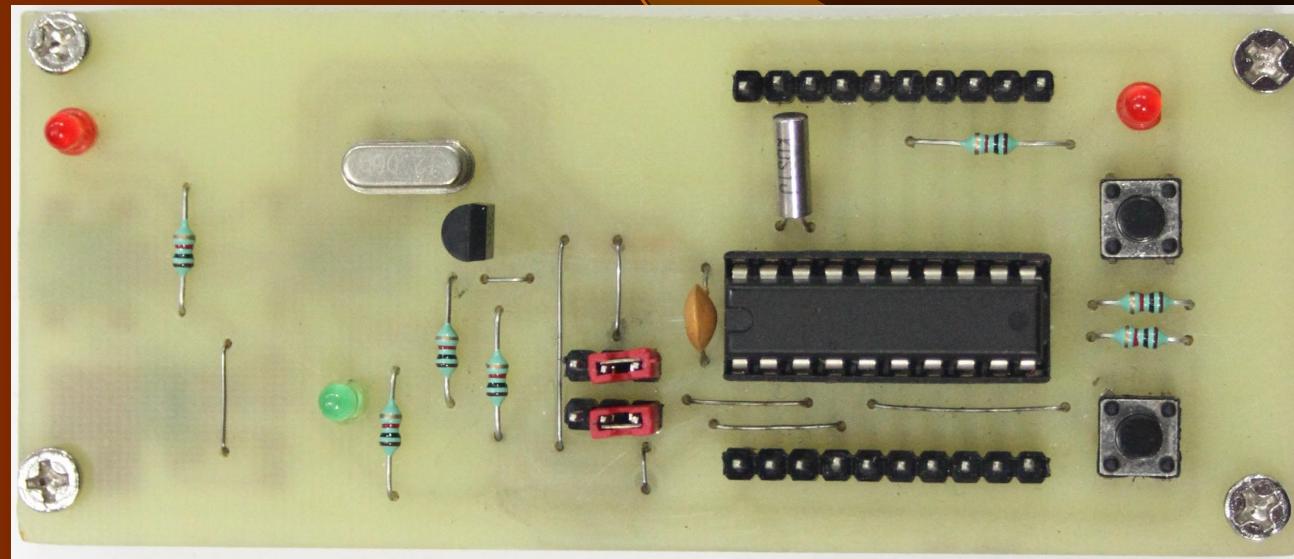
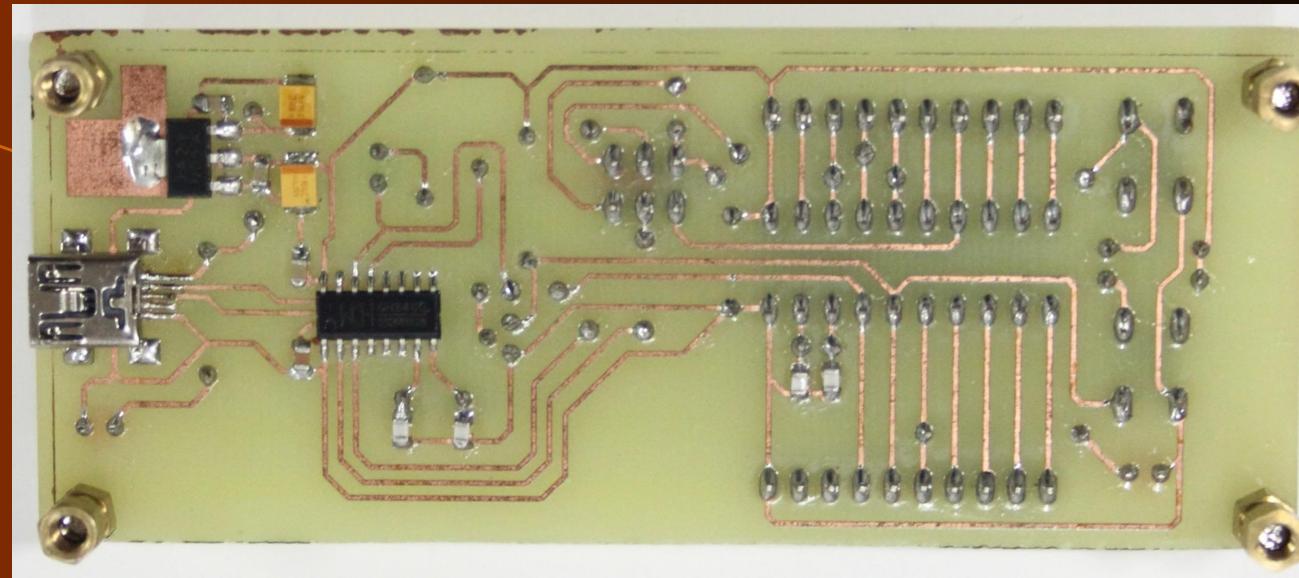
Lunchbox Development Process

- Lunchbox on a Breadboard/Zero Board
- Inhouse PCB
- Manufactured PCB

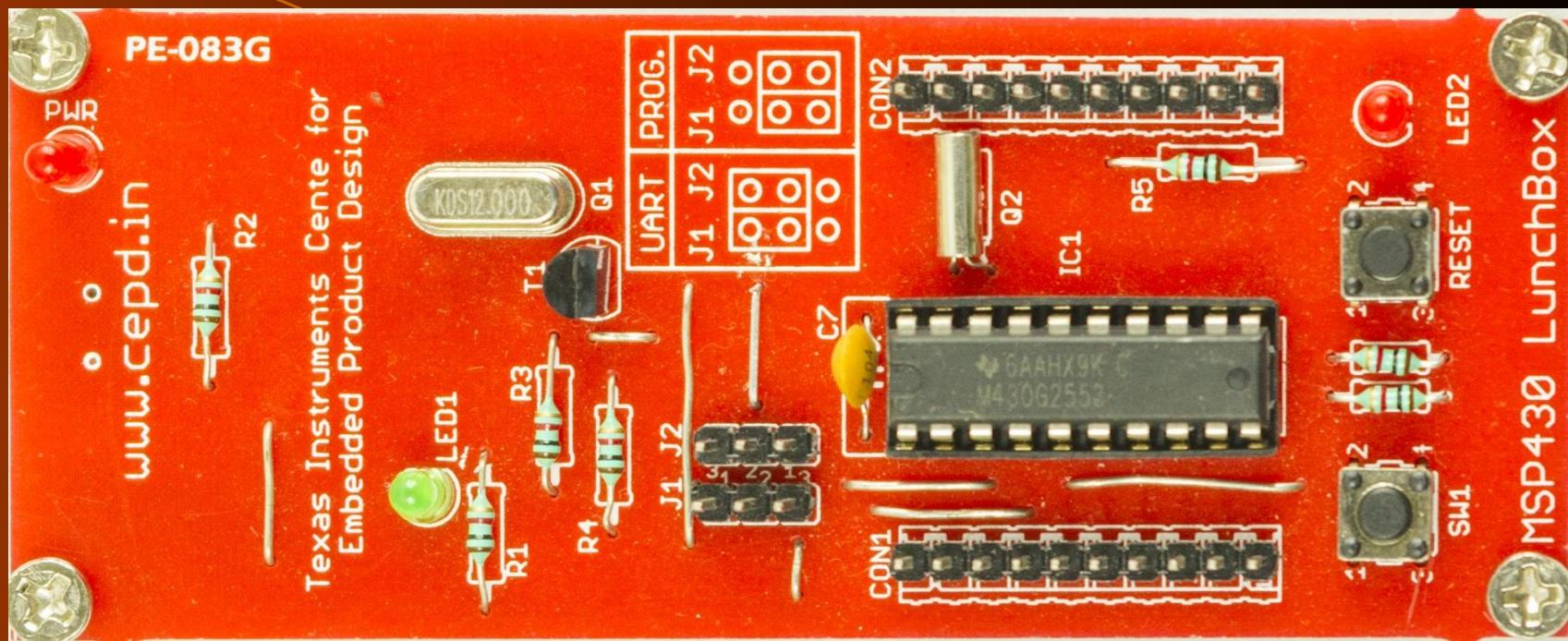
Lunchbox on BreadBoard



Lunchbox In-house PCB



Manufactured Lunchbox





Thank you!