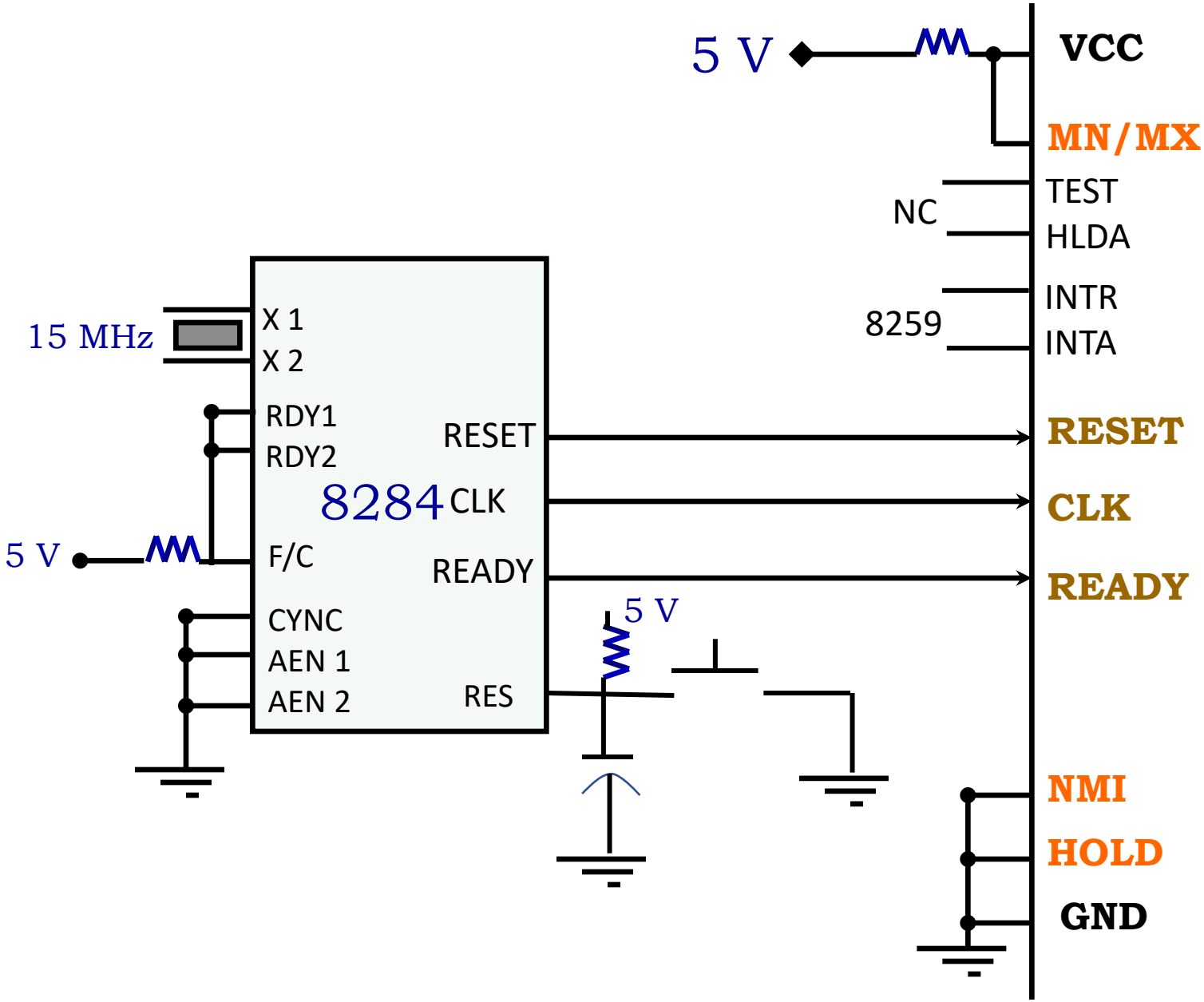
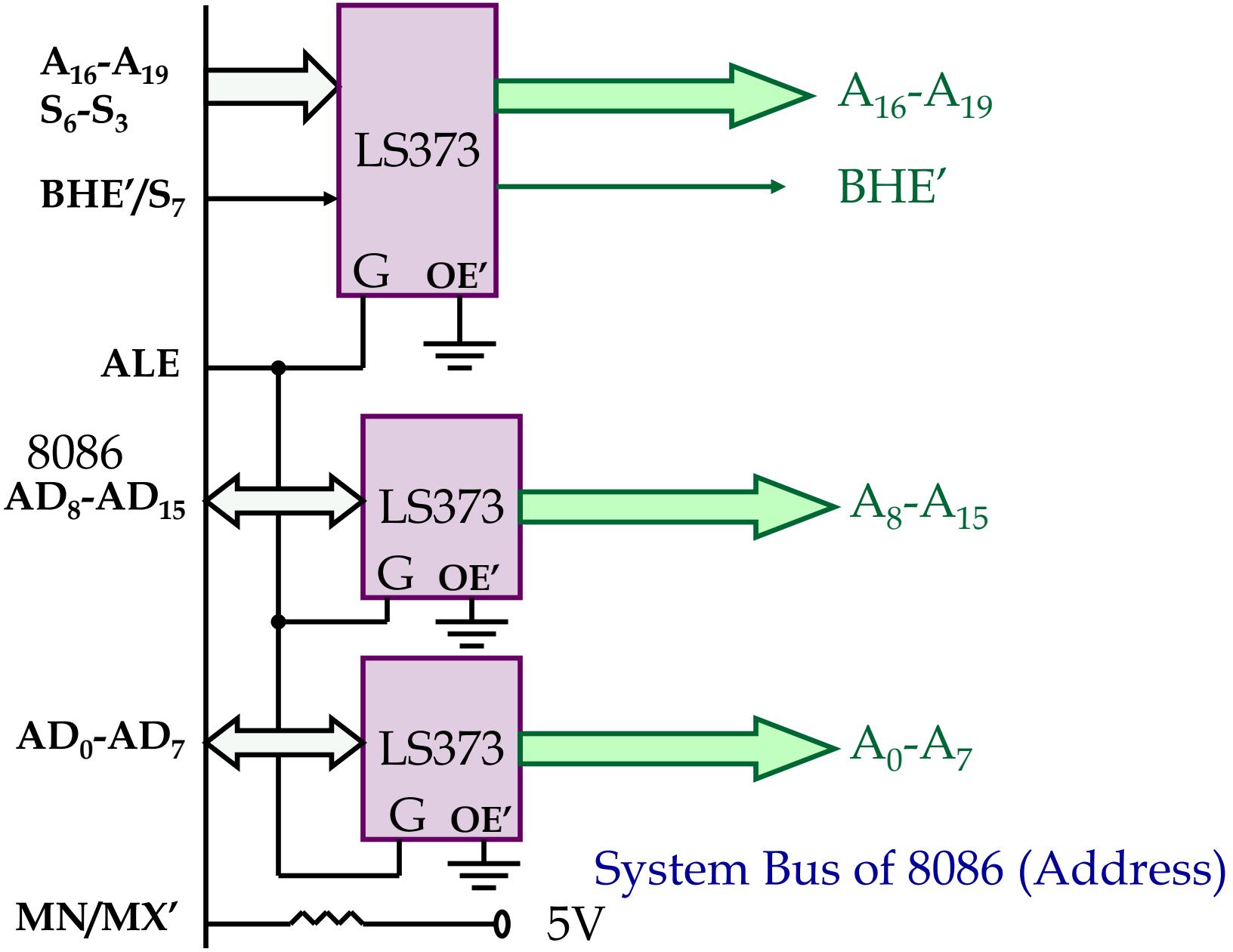
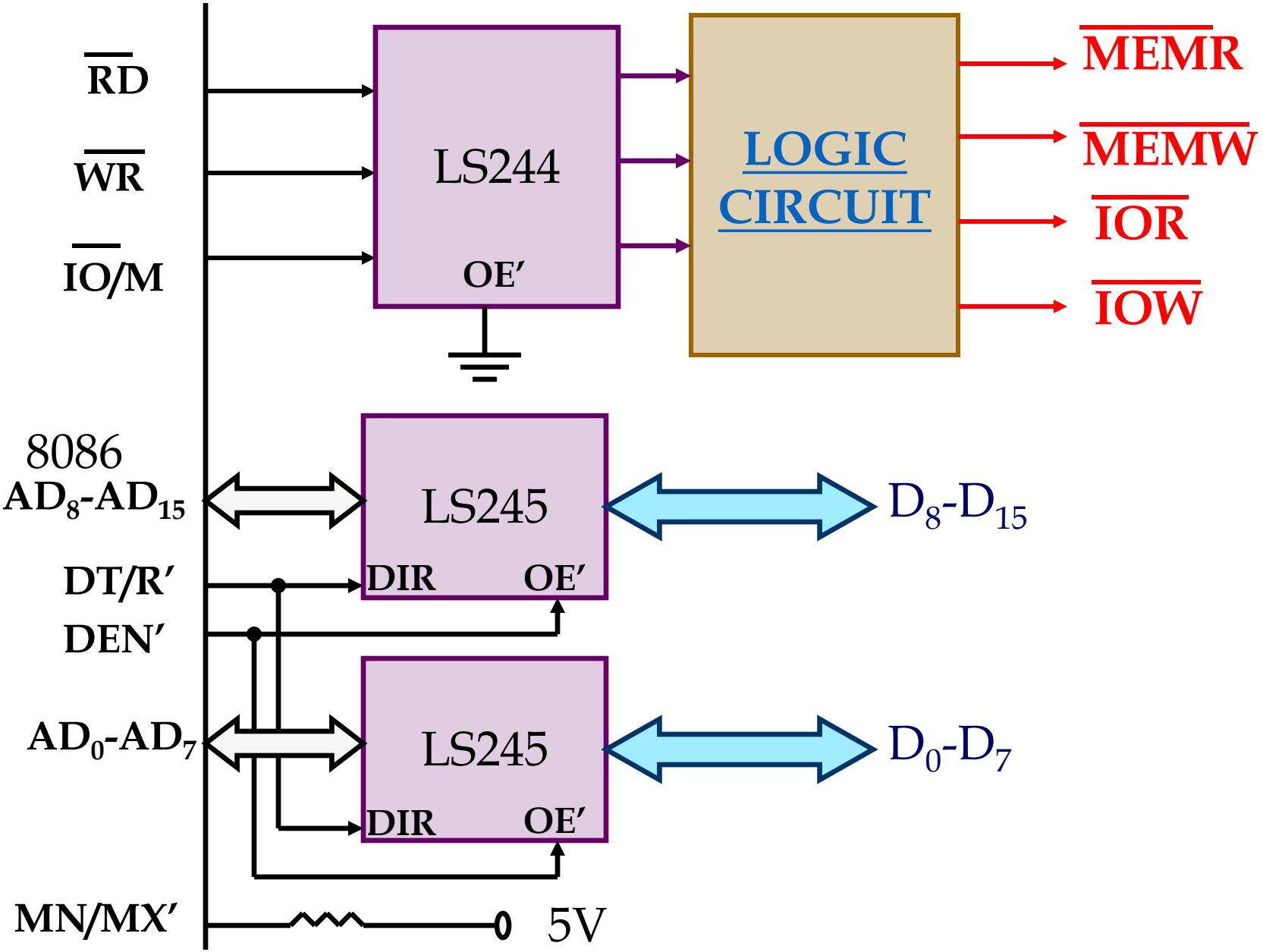

5 V
VCC
MN/MX
TEST
NC
HLDA
INTR
8259
INTA
15 MHz
X 1
X 2
RDY1
RDY2
RESET
8284
CLK
5 V
F/C
READY
CYNC
AEN 1
AEN 2
RES
5 V
RESET
CLK
READY
NMI
HOLD
GND

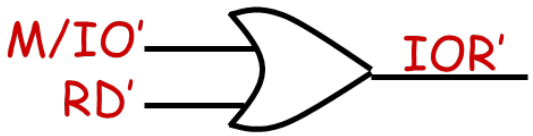
8086 Inputs

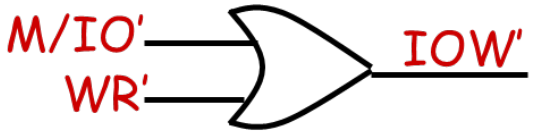


System Bus of 8086 (Address)

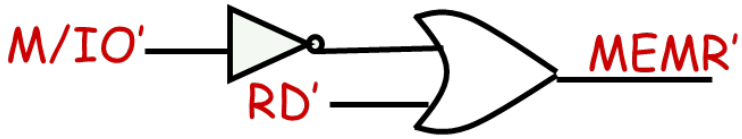


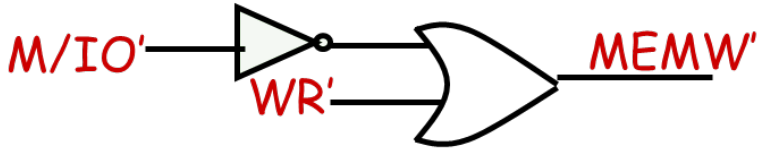
System Bus of 8086(Data + Control)



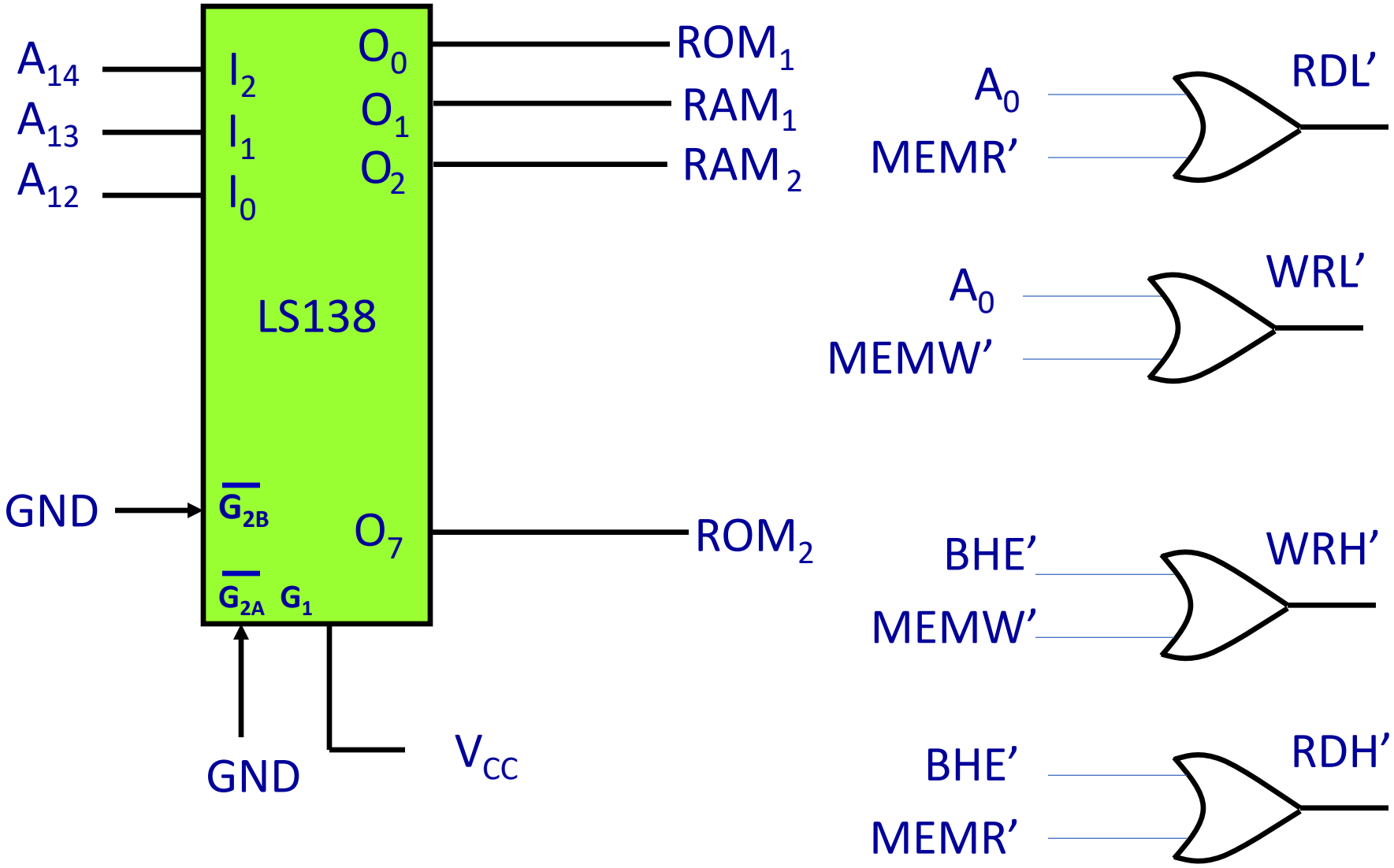


M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

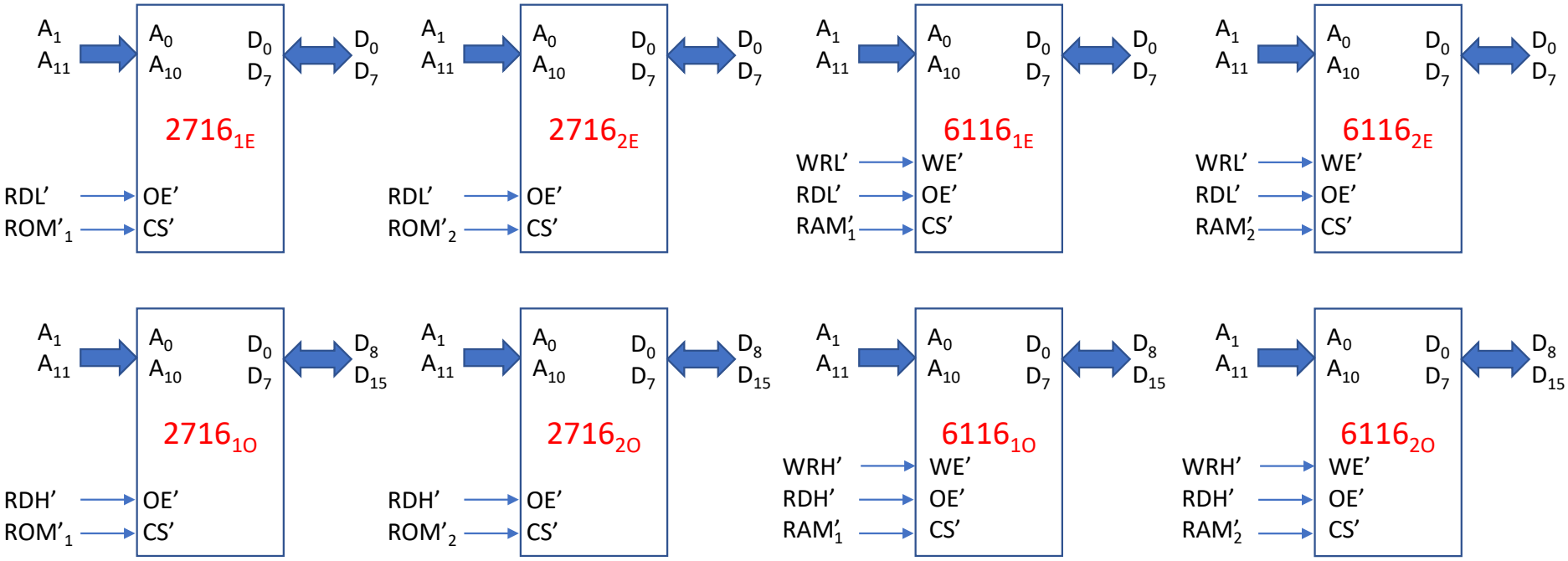




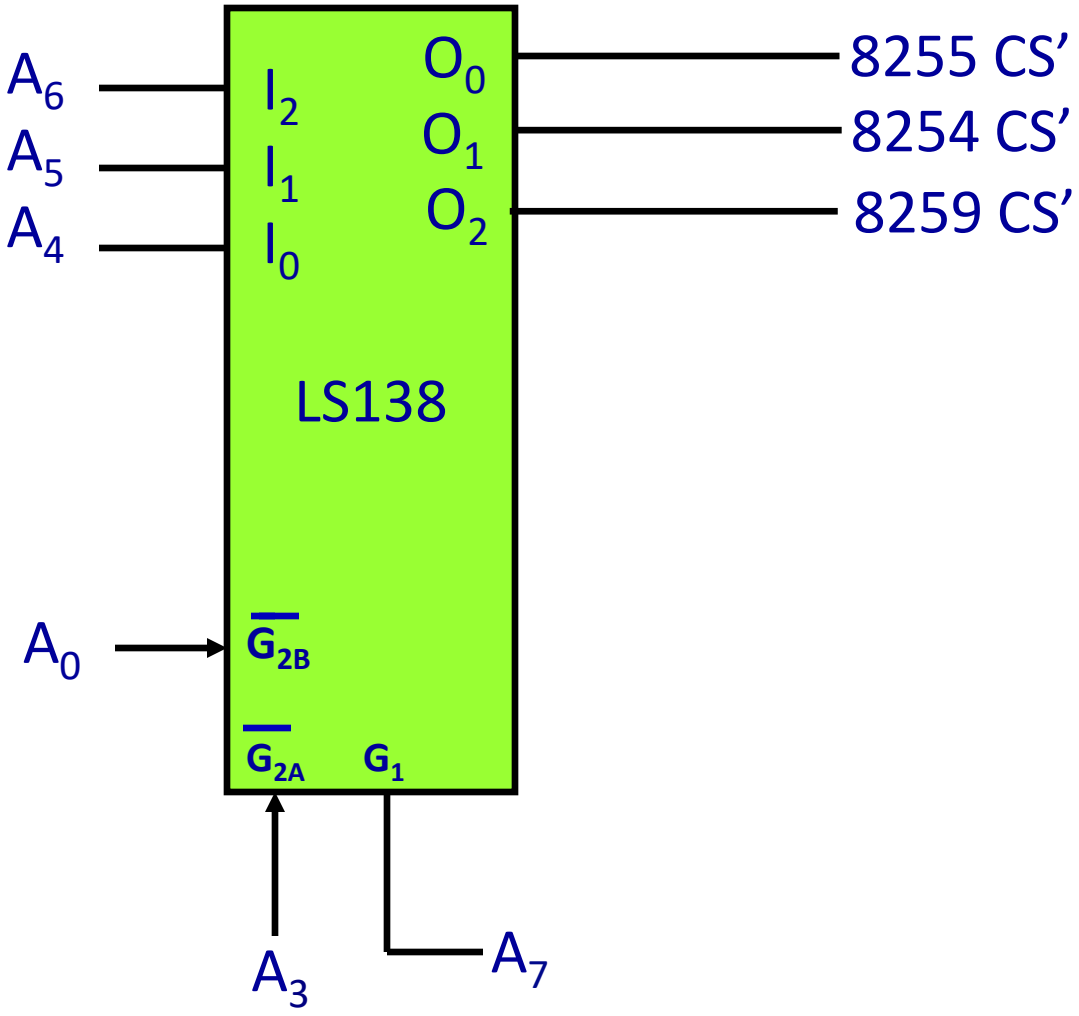
back



Memory Decoder

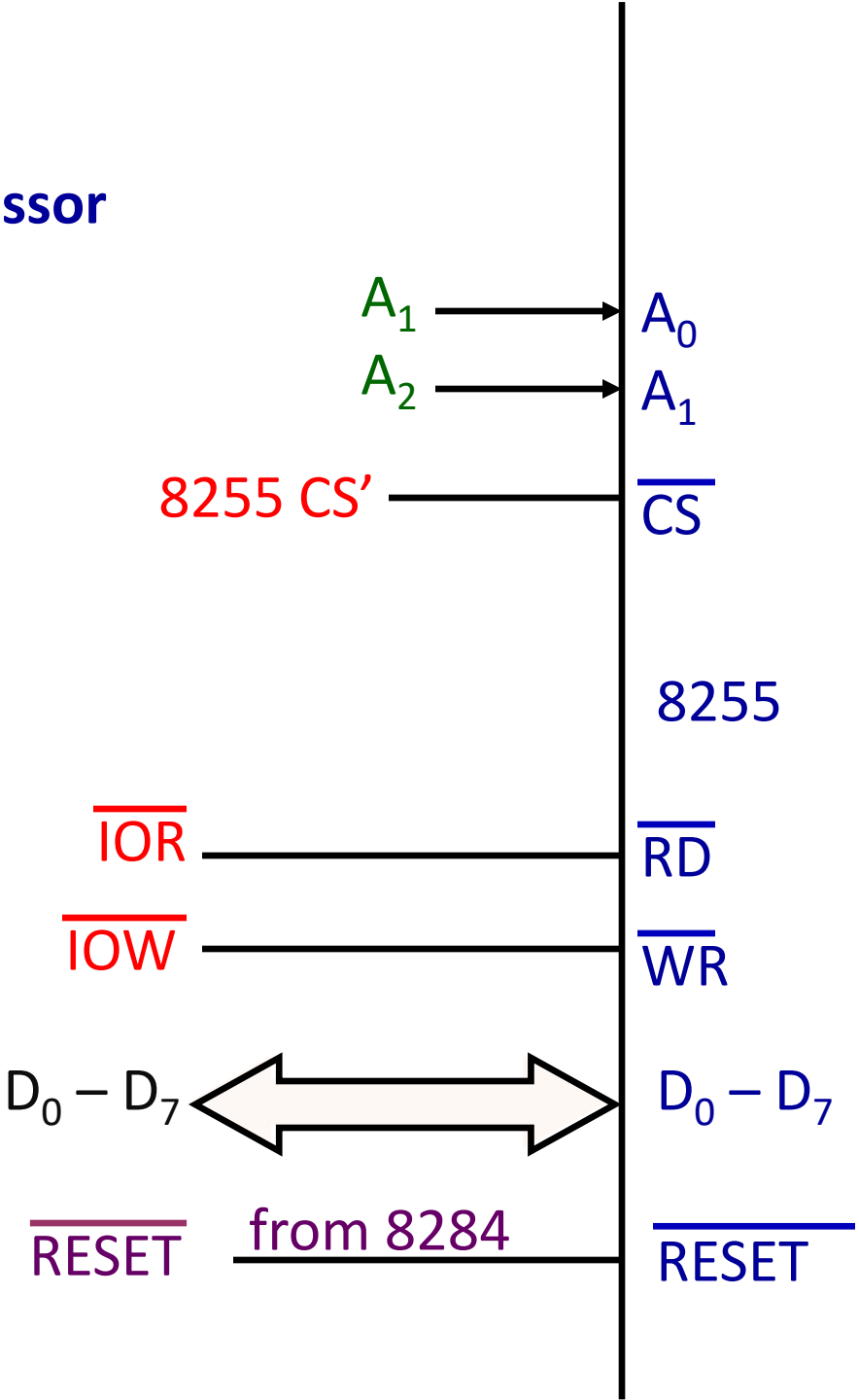


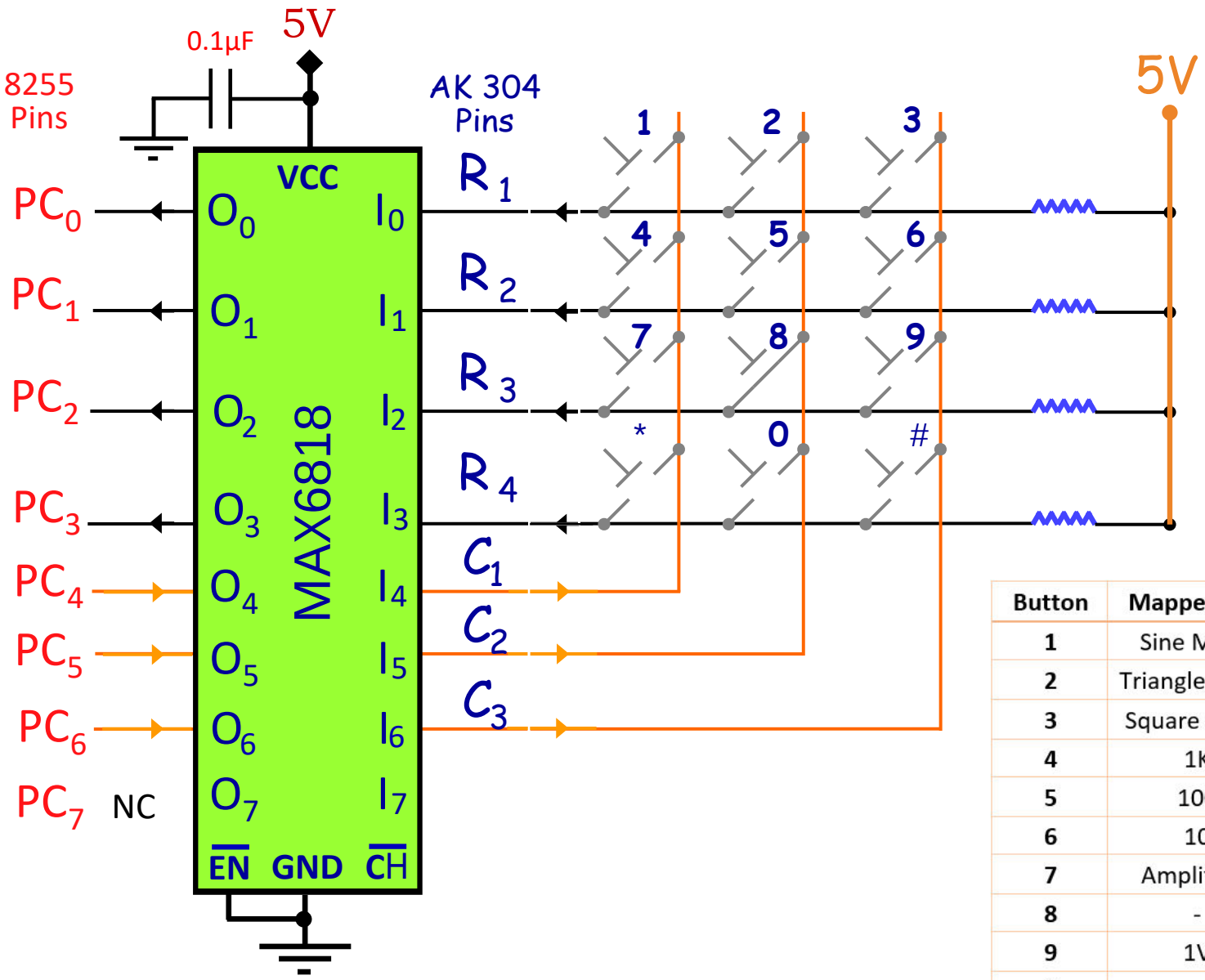
Memory Interfacing


A6
A5
A4
I2
I1
I0
O0
O1
O2
8255 CS'
8254 CS'
8259 CS'
LS138
A0
G2B
G2A
G1
A3
A7

I/O Decoder

8255 Interface to the processor

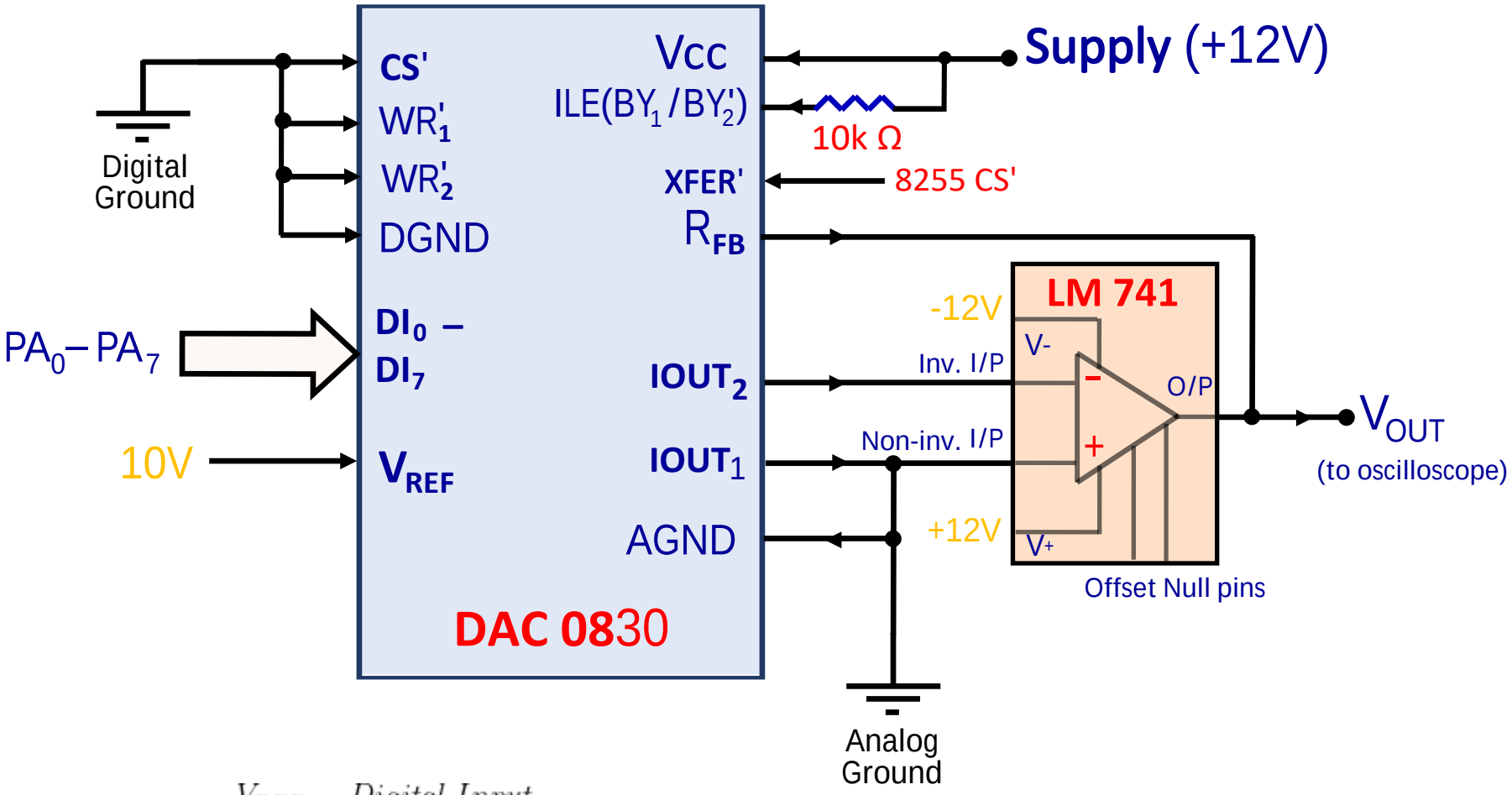




Button	Mapped Key	PC6-PC0
1	Sine Mode	110 1110$_b$
2	Triangle Mode	101 1110$_b$
3	Square Mode	011 1110$_b$
4	1K	110 1101$_b$
5	100	101 1101$_b$
6	10	011 1101$_b$
7	Amplitude	110 1011$_b$
8	-	101 1011$_b$
9	1V	011 1011$_b$
*	-	110 0111$_b$
0	-	101 0111$_b$
#	-	011 0111$_b$

8255 and AK 304 Interfacing

Debouncing IC: MAX 6818



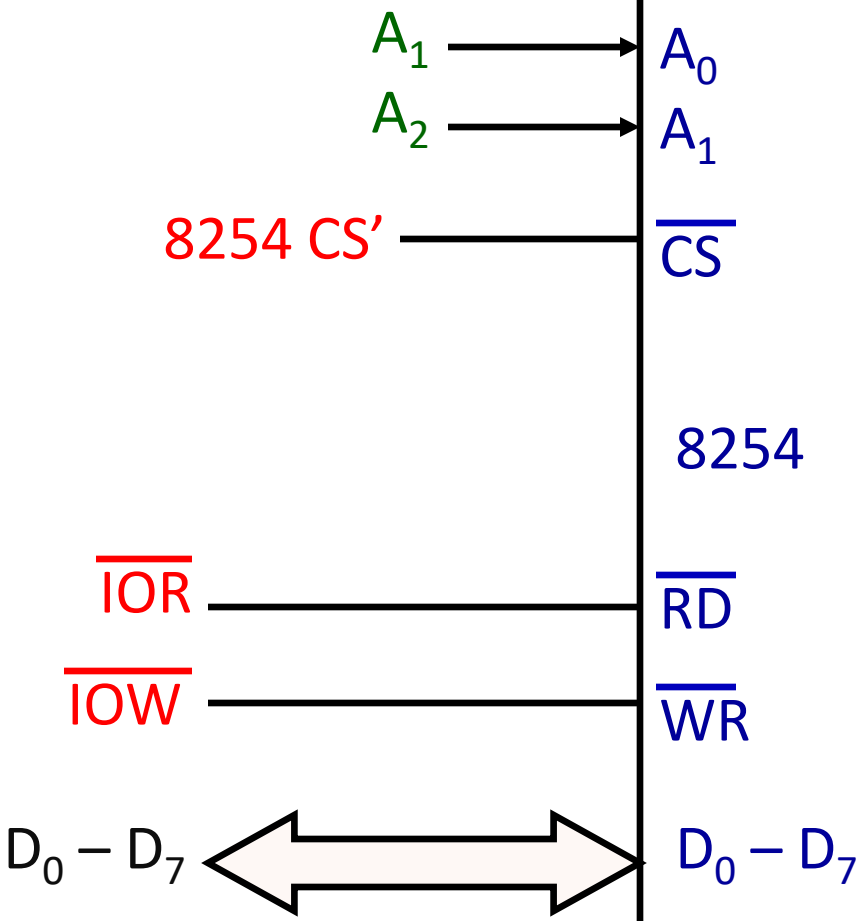
$$I_{OUT1} = \frac{V_{REF}}{15k\Omega} \times \frac{Digital\ Input}{255}$$

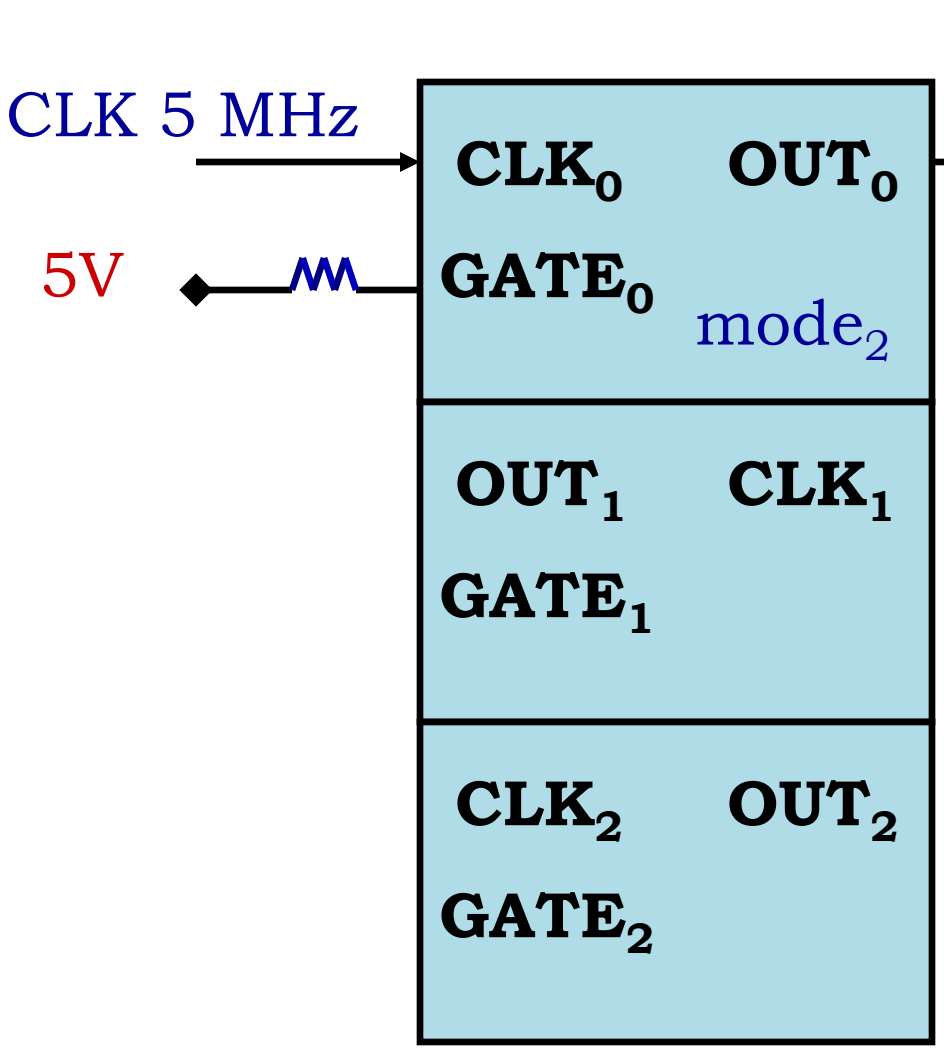
$$I_{OUT2} = \frac{V_{REF}}{15k\Omega} \times \frac{255 - Digital\ Input}{255}$$

$$V_{OUT} = V_{REF} \times \frac{Digital\ Input}{255}$$

8255 and [0830 and 741] Interfacing

8254 Interface to the processor





F_{req}* SR KHz

Timer INT

Count

Let:

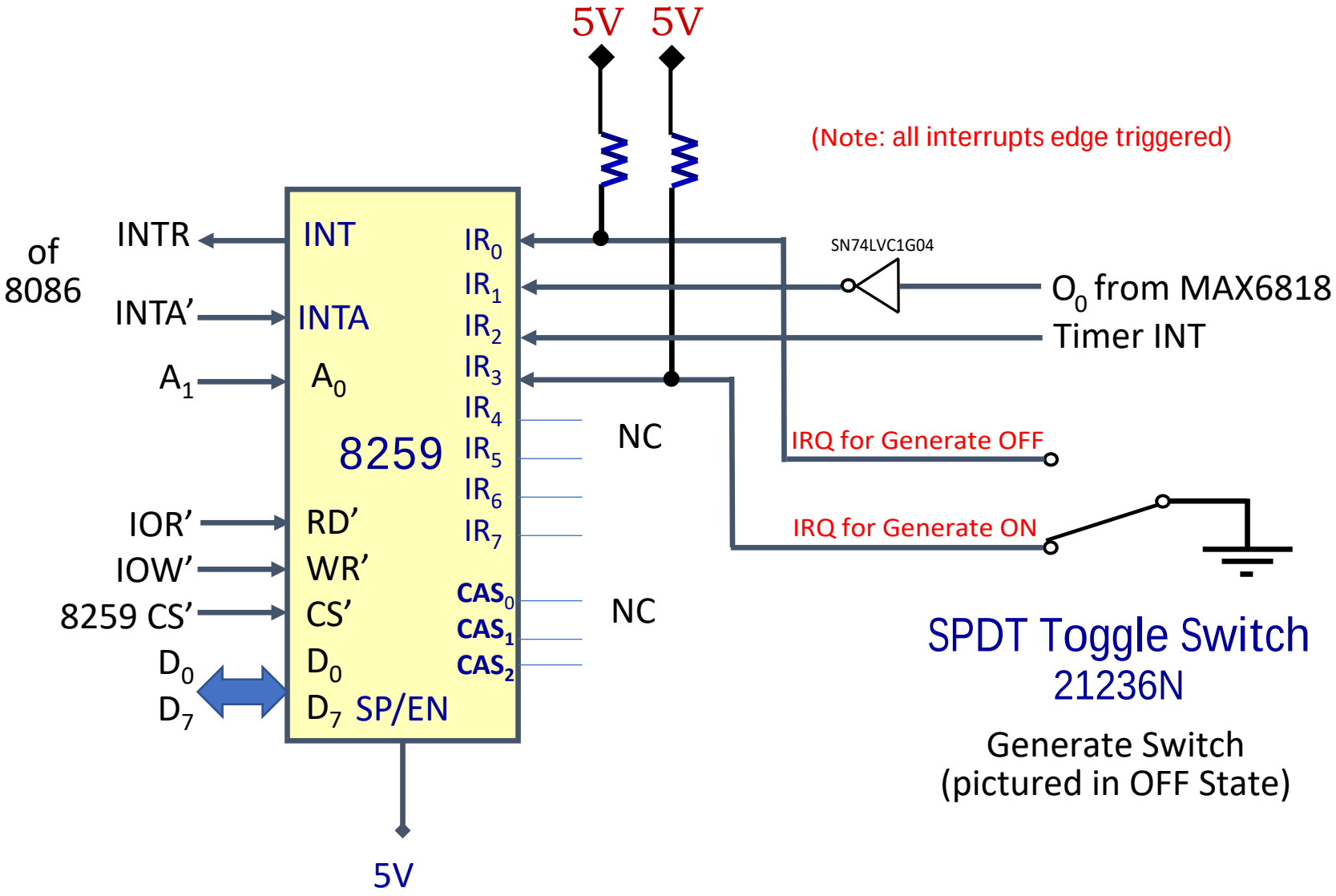
F_{req} = Required Freq in KHz

SR = Sampling Rate (50 here)

Then:

$$Count = \left\lfloor \frac{5000}{F_{req} \times SR} \right\rfloor$$

8254



8259 and Generate Switch