Analog Comparator

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1) Two Stage Open Loop Comparator

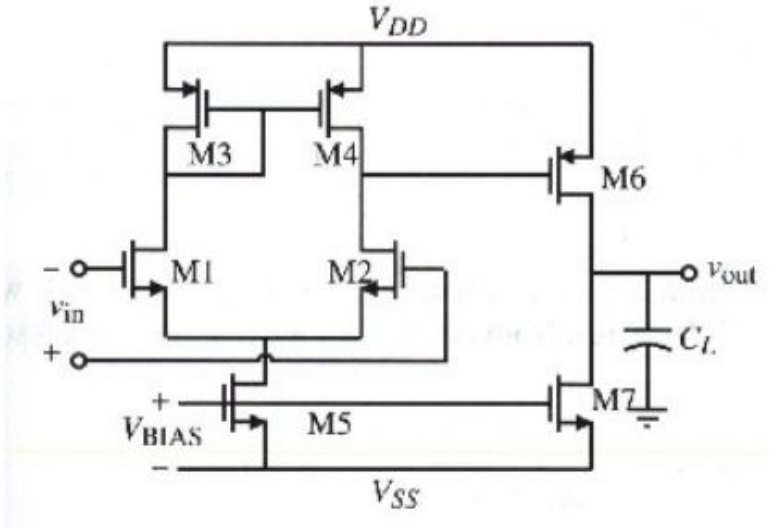


Fig 1 Two stage CMOS Comparator

Theory

- A comparator requires a differential input and sufficient gain to be able to achieve the desired resolution.
- The two stage opamp used in an open loop mode makes an excellent implementation of the comparator.
- It is preferred not to compensate the comparator so that it has the largest bandwidth possible, which will give a faster response.

Theory

- The output stage is a current sink inverter.
- The maximum output voltage, assuming that the gate of M6 has a minimum voltage given as VG6(min), can be expressed as

$$V_{OH} = V_{DD} - (V_{DD} - V_{G6(min)} - |V_{TP}|)[1 - \sqrt{1 - (2 I_7 / B_6(V_{DD} - V_{G6(min)} - |V_{TP}|)^2)}]$$

- The minimum output voltage is

$$V_{OL} = V_{SS}$$

Working

- Firstly we will be choosing one of the input gates equal to a dc voltage and find output voltage of the first and second stages when the other input gate is above and below the dc voltage on the first gate.
- Let us begin by assuming that VG1 > VG2 . MOSFETS M3 and M4 are current mirror therefore i1 = i3 = i4 which is greater than i2. Consequently, vo1 increases because of the difference current flowing into c1. Hence we obtain Vout as High ie. VOH

Working

- Next we assume VG1 < VG2. In this case i1 = i3 = i4 which is less than i2. Consequently, vo1 decreases because of the difference current flowing into c1. Therefore Vout obtained is low.
- The sum of currents in the 2 branches of the first stage is equal to Iss.
- When VG1 = VG2, current Iss is equally divided in the 2 branches of first stage.

2) Preamplifier Latch based Comparator

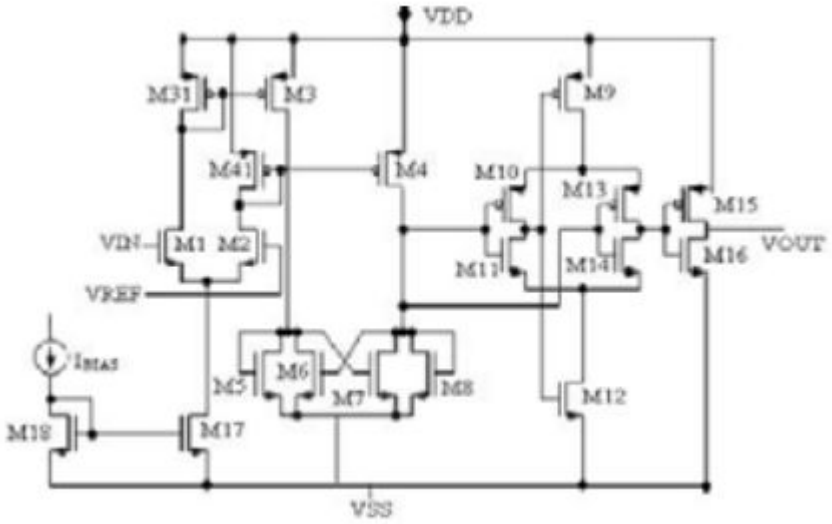


Fig.2 Preamplifier latch based comparator

Theory

- Preamplifier latch based comparator circuit consists of a preamplifier followed by a latch.
- The major drawback of the latch comparator is the offset error caused by transistor mismatch and unbalanced charge residues .To overcome this a preamplifier circuit is used.
- The basic principle of the preamplifiers is that it amplifies the input signal and feeds it to the input of latch which is designed by using back to back inverter
- High performance comparators are needed to amplify a small input (or the difference between the input voltage and a reference voltage) to a level large enough to be detected by digital logic circuits within a very short time.

Working

- The comparator consists of three stages: The input preamplifier, A positive feedback or decision stage, and an output buffer. Differential amplifier will act as a preamplifier circuit.
- Preamplifier:

  Preamplifier is used to avoid kickback noise. It is implemented using Differential amplifier.

- This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the diff-amp transconductance and the input capacitance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of Ml and M2.

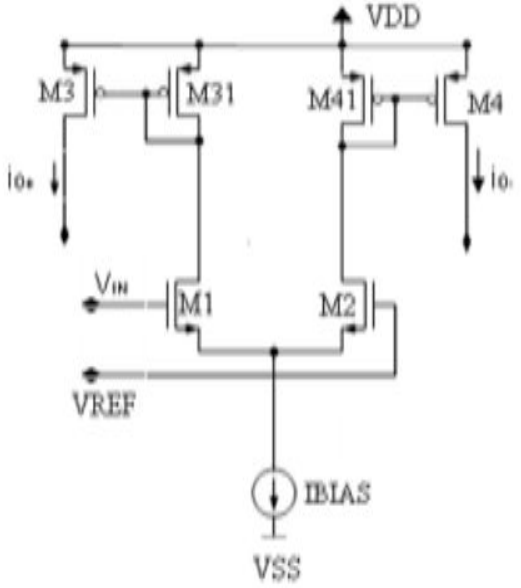


Fig.3 Preamplifier

LATCH – A decision circuit

- This circuit must be capable of discriminating the mV signals.
- The circuit uses positive feedback from the cross-gate connection transistor to increase the gain of the decision element.If iO- increases iO+ decreases, switching takes place when $V_{DS7} = V_{THN6}$. At this point M_6 start to take current away from M_5.
- This decreases V_{DS5} and thus M_7 turns off.
- Assuming that the maximum value of vO- or vO+ equal to $2V_{THN}$, then M_6 and M_7 operate in either cutoff or triode regions. V_{DS7} reaches V_{THN}, and thus M_7 enters the saturation region

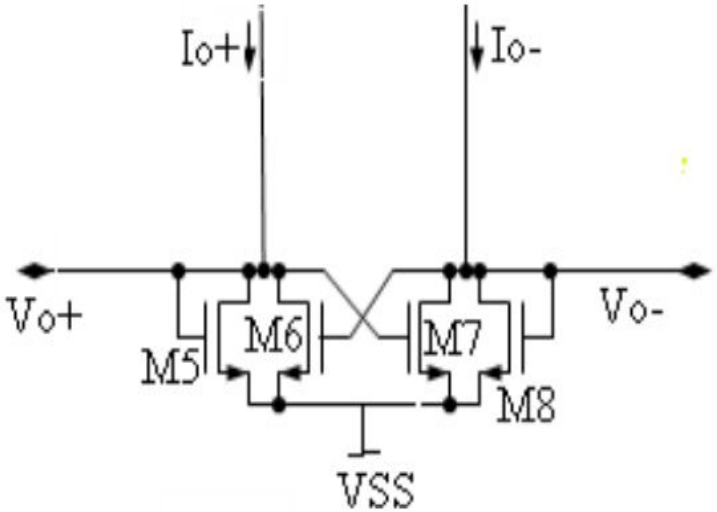


Fig.4 Latch

Output Buffer

- The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e. 0 or 5 V).
- The output buffer should accept a differential input signal and not have slew rate limitations.
- A self-biasing differential amplifier is used as the comparator output buffer.

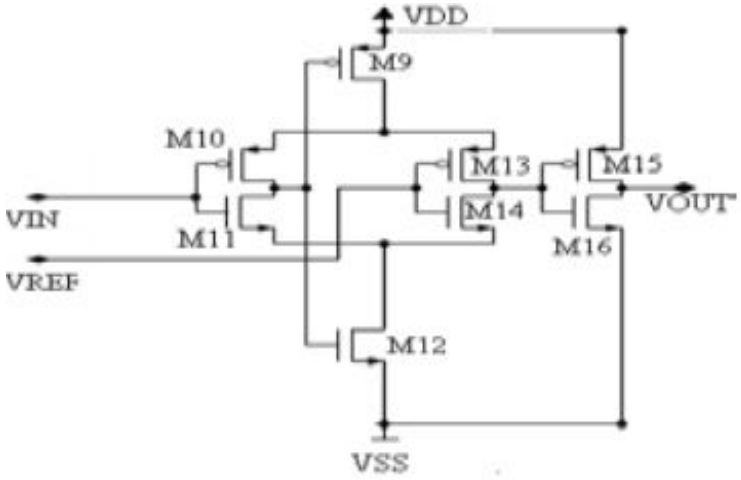


Fig.5 Output Buffer

Current Mirror

- The current source/sink is a basic building block in CMOS IC design and is used extensively in analog integrated circuit design.
- Ideally, the output impedance of a current source/sink should be infinite and capable of generating or drawing a constant current over a wide range of voltages.
- However, finite values of ro and a limited output swing required to keep devices in saturation will ultimately limit the performance of the mirror.

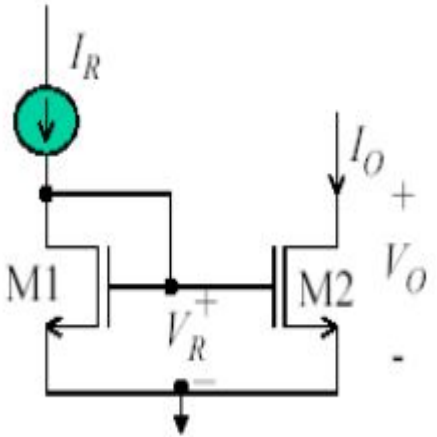
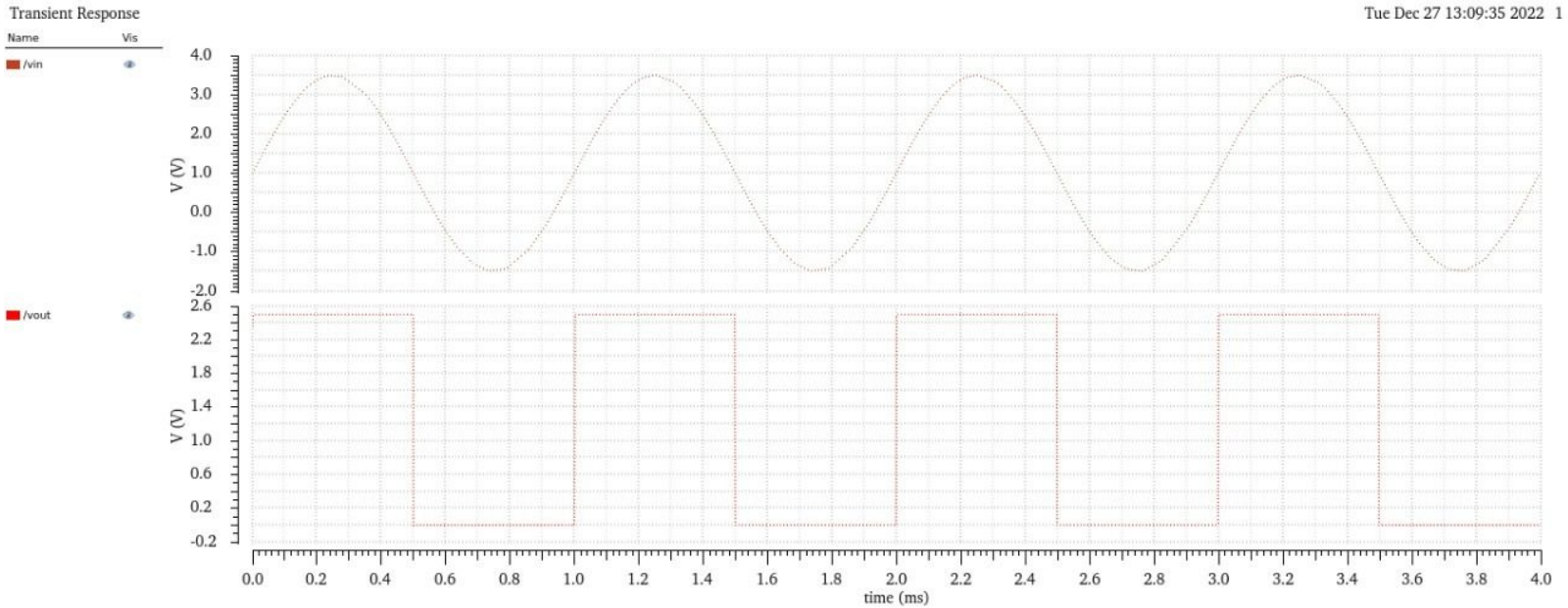


Fig.6 Current Mirror

Results


Transient Response
Tue Dec 27 13:09:35 2022 1
Name
Vis
/vin
/vout
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
V (V)
2.6
2.2
1.8
1.4
1.0
0.6
0.2
-0.2
V (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
time (ms)

Results

- Performs when the input has a difference which is in the range of **5mV to 100V** without any output noise.
- For the least difference of 5mV the **delay time** of the comparator was to be calculated as **89ns.**
- The power dissipated during this process is **888.168uWatt.**

References

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