A

Project Report on

"BETA Processor"

Submitted by
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Under The Guidance of

Mrs. Dr. S. S. Deshpande

For The Award of The Degree of

Bachelor of Technology

Department of Electronics

WALCHAND COLLEGE OF ENGINEERING, SANGLI

(An Autonomous Institute)

(2018-19)

Department of Electronics

WALCHAND COLLEGE OF ENGINEERING, SANGLI

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CERTIFICATE

This is to certify that the project entitled

"BETA Processor"

Submitted by

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in the partial fulfillment for the award of the Degree of
Bachelor of Technology
in
ELECTRONICS ENGINEERING
is a record of student's own work carried out under our supervision
and guidance during the academic year 2018-2019

Mrs. Dr. S. S. Deshpande
(Project Guide)

Dr. B. G. Patil
(Head of Department)

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INTRODUCTION

Most of us are aware with open source software projects like linux/Unix. In past decade open source hardware started to come in to the picture the most common example of it is Arduino, Raspberry Pi. Similar to that a massive open source project known as ‘RISC V’ is royalty free and open source Instruction Set Architecture(ISA) started at UC Berkeley in 2007. In this project we are trying to implement computer architecture based on simplistic version of this ISA for the educational purpose.

In our project, with the help of simple digital design concepts we are trying to provide a gateway to learn about amazing world of computer architecture and digital systems.

In this project we are trying to create a board(based on fpga) like a hardware kit which explains the detailed architecture of computer, its instructions, their execution and many other important concepts of computer organization. We also like to add functionality which helps

to execute instructions step by step almost like a software debugger but on hardware level .

We are trying to achieve all this by implementing a computer architecture developed by **MIT(beta processor*)** in a hardware description language known as '**VERILOG**'. All the task of simulation and verification is to be done on **XIlinx ISE** software. And for actual implementation **FPGA** will be used.

OBJECTIVES

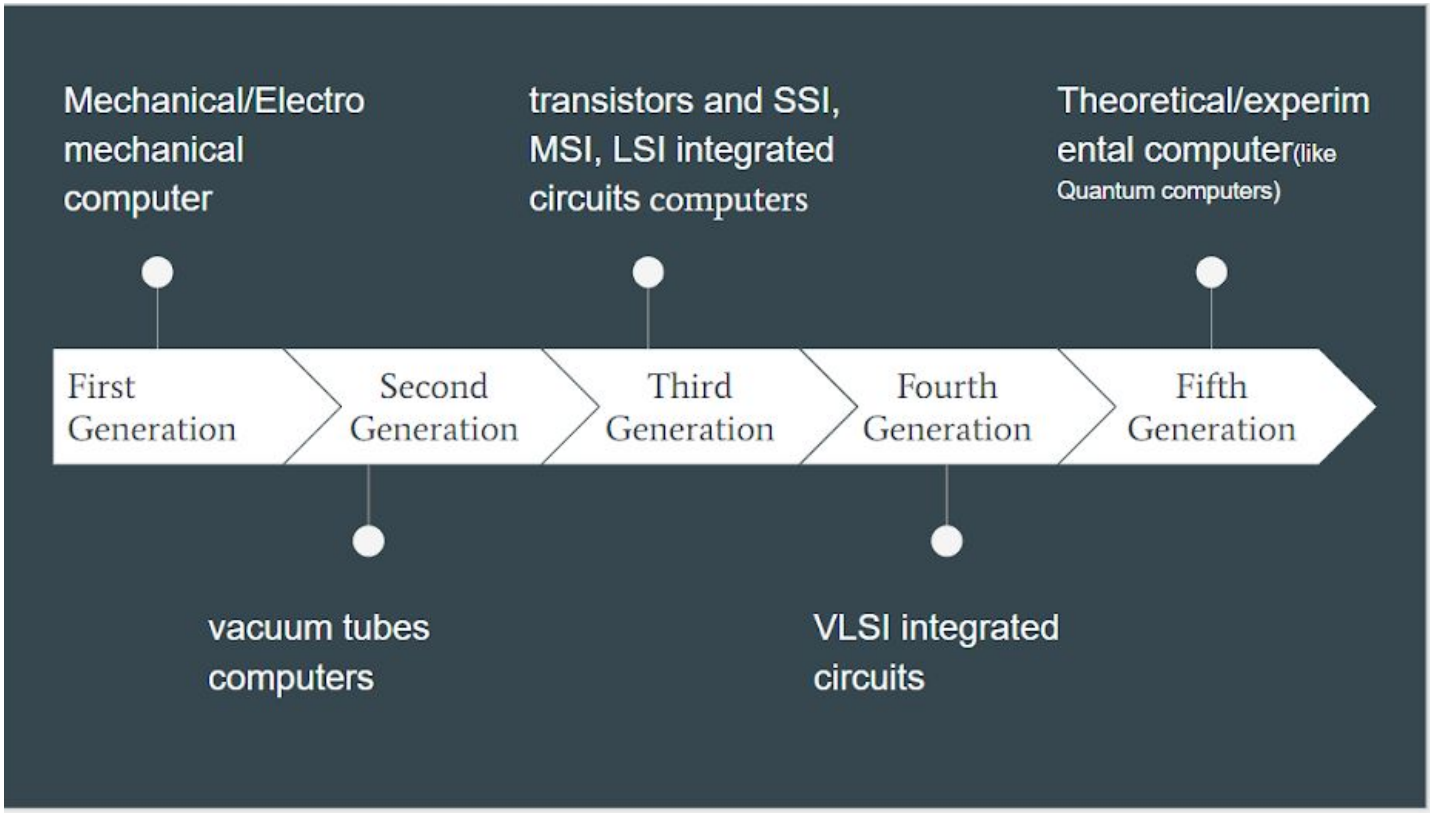
1. To implement 32 bit microcontroller in FPGA.
2. To create necessary software support like assembler for it.
3. Implementing communication protocol on FPGA to send data to external hardware for display purpose.
4. Creating hardware which can show the necessary processes in the processor.
5. Most importantly create a unique learning experience .
6. Introduce users to principles of computer architecture and Digital System Design .
7. Create a gateway for user to learn about more complicated and practically used digital systems.

Literature Survey

HISTORY OF MODERN COMPUTERS :

The principle of the modern computer was proposed by Alan Turing in his seminal 1936 paper on *Computable Numbers*. Turing proposed a simple device that he called "Universal Computing machine" and that is now known as a universal Turing machine. He proved that such a machine is capable of computing anything that is computable by executing instructions (program) stored on tape, allowing the machine to be programmable. The fundamental concept of Turing's design is the stored program, where all the instructions for computing are stored in memory. Von Neumann acknowledged that the central concept of the modern computer was due to this paper. Turing machines are to this day a central object of study in theory of computation. Except for the limitations imposed by their finite memory stores, modern computers are said to be Turing-complete, which is to say, they have algorithm execution capability equivalent to a universal Turing machine.

EVOLUTION OF COMPUTER

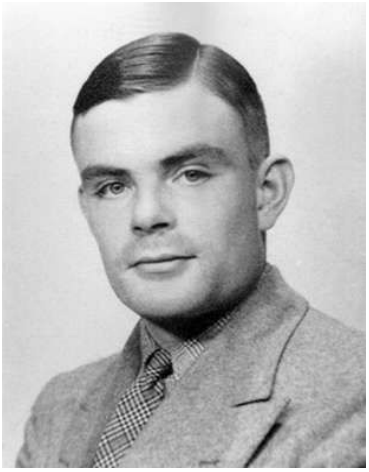


MODELS OF COMPUTATION :

In computer science, and more specifically in computability theory and computational complexity theory, a **model of computation** is a model which describes how a set of outputs are computed given a set of inputs. This model describes how units of computations, memories, and communications are organized. The computational complexity of an algorithm can be measured given a model of computation. Using a model allows studying the performance of algorithms independently of the variations that

are specific to particular implementations and specific technology.

Following are the three basic models of computations :



Sir Alan Turing

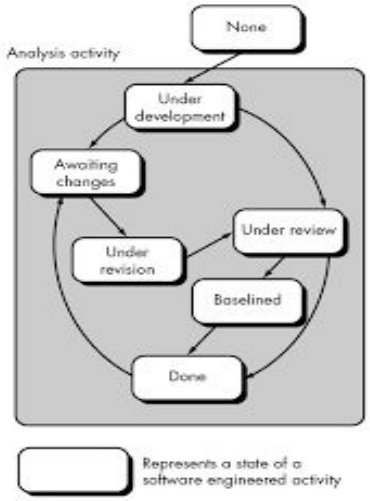
Sequential models include:

- Finite state machines
- Pushdown automata
- Turing Machine

Alonzo Church

Functional models include:

- Lambda calculus
- Recursive functions
- Combinatory logic
- Cellular automaton
- Abstract rewriting systems

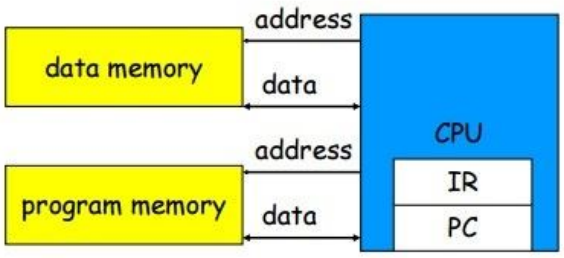


Concurrent models include:

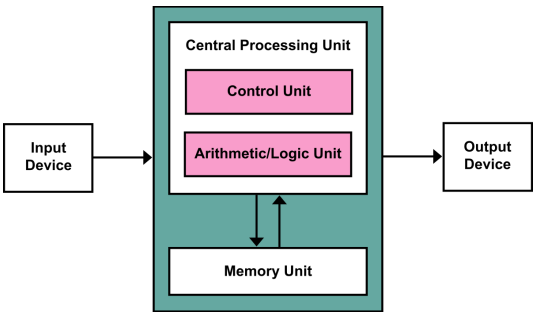
- Kahn process networks
- Petri nets
- Synchronous Data Flow
- Interaction nets

MODERN COMPUTER ARCHITECTURE

Most of the general purpose computer that we use today are based on the sequential model of computation.Depending upon the organisation of memory most of the modern computer architecture are of following two architecture type



HARVARD ARCHITECTURE



VON NEUMANN ARCHITECTURE

INSTRUCTION SET

An **instruction set architecture** (**ISA**) is an abstract model of a computer. It is also referred to as **architecture** or **computer architecture**. A realization of an ISA is called an *implementation*. An ISA permits multiple implementations that may vary in performance, physical size, and monetary cost (among other things); because the ISA serves as the interface between software and hardware. Software that has been written for an ISA can run on different implementations of the same ISA. This has enabled binary compatibility between different generations of computers to be easily achieved, and the development of computer families. Both of these developments have helped to lower the cost of computers and to increase their applicability. For these reasons, the ISA is one of the most important abstractions in computing today.

Following are two major categories of Instruction set found in most of the computers

Reduce Instruction set computer (RISC)	**Complex Instruction set computer(CISC)**
• Simple , standardized and less no. of instructions • Single-cycle execution. • Single layer of instruction • Use more RAM • Software centric design • Simple to implement	• More number of relatively complex instructions • Multi cycle execution. • Multiple layer of instruction • Use less RAM • Hardware centric design • Hard to implement

OUR BUCKET OF WATER FROM THE SEA OF LITERATURE :

Our project is heavily inspired by an open source project know as **RISC - V** and a ISA known as **MIT BETA** developed by MIT for **COMPUTATIONAL STRUCTURES** course (course number 6.004) . Following part of the document provided an glams of our inspiration.

RISC - V

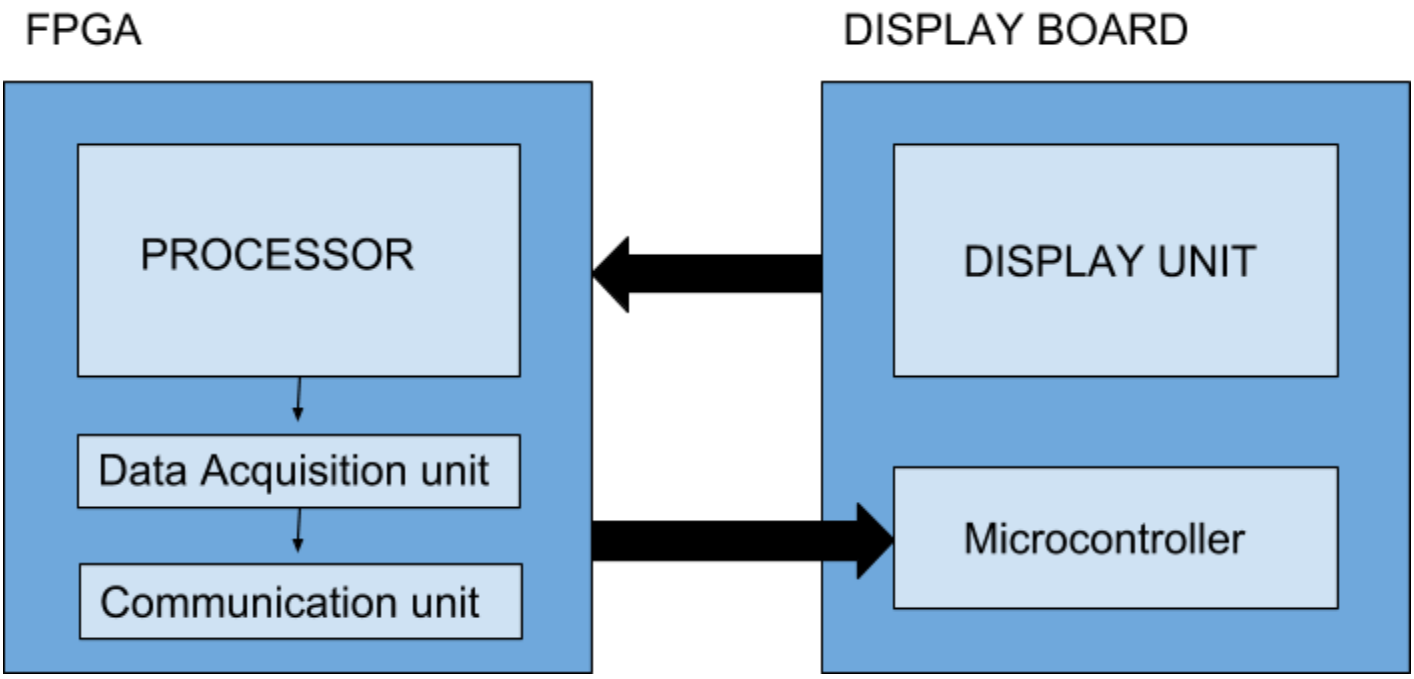
RISC-V (pronounced “risk-five”) is an open, free ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

MIT BETA :

Its an simple computer architecture developed by MIT to make students familiar with the fundamentals of digital system design and computer architecture. Its an single cycle instruction RISC processor base on von Neumann architecture

PROPOSED MODEL

HARDWARE LAYOUT



A basic model of our system consist of two major parts as far as hardware concerned FPGA and DISPLAY BOARD(microcontroller)

FPGA :

The hart of our product, our 32-bit microprocessor is physically implemented in the FPGA. Then all the important data of processor like all the register values , memory values , all values of control signals is collected by Data Acquisition Unit .The collected data is sent to the DISPLAY BOARD to explain its

working by displaying all the important components of the processor in a systematic manner. This data is collected in real time and send by a communication unit to microcontroller .

DISPLAY BOARD :

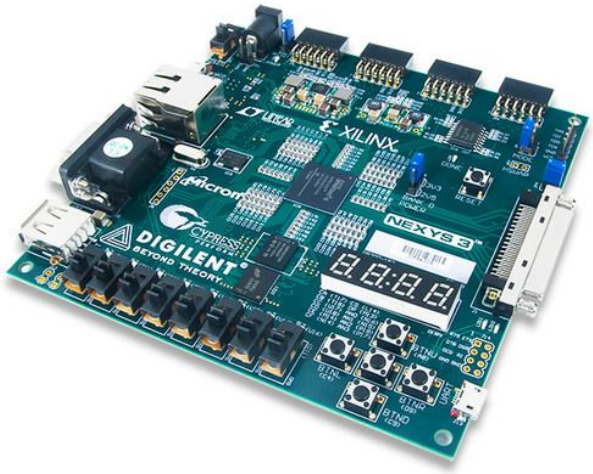
The display board is equipped with a microcontroller with few seven segment display on it.The received data from the FPGA then systematically formatted and represented by using the Display unit. This unit contin LEDS and 7 segment display to represent the 32-bit values of the registers from the processor in an interactive manner .

SOFTWARE SUPPORT PACKAGE

No hardware is complete without a beautiful software. So we are providing the user with a software interface which will help to boost the user experience and the usability of the product. This software package mainly consist of an **ASSEMBLER** for our processor. This ASSEMBLER is written in a elegant and simple to understand programming language **PYTHON**. The ASSEMBLER plays a crucial role in the product as it is design in such a way that it itself describe few principles of ISA designing . Our Software also contain a board support package for the microcontroller present in Display Board.

REQUIREMENT ANALYSIS AND COSTING

HARDWARE :



1. Xilinx spartan 6 or spartan 3 FPGA board

2. Arduino UNO (₹ 250 - 300)
3. 7 Segment Display module X 10 (₹ 120 x 10)

4. Communication module (UART/ SPI)

5. PCB

SOFTWARE :

1. XIlinx ISE Design Suite for FPGA programming (Free)

2. µVision IDE - Keil or arduino IDE for microcontroller programming (Free)

3. Anaconda IDE for python.(Free)

UPCOMING TIME PLANNING

MONTH	PROJECT WORK
July, ,August	Team Formation, FInalization of the project topic / area
September	Literature Survey and Finalization of project
October, November	Requirement analysis
December	Simulation and testing of system
January	Board Design and assembling the components
February	Physical testing and debugging of the board
March	Final touch up
April	Submissions

PROJECT OUTCOME

When we look at digital devices like microcontrollers and microprocessors, it seems very complicated from their working but under the hood the real beauty of these things lies in their simplicity. Yet most of the students fails to realise this, so we decided to create something that will be helpful for them to learn about it, and how there working.

We want to create a getaway for user to get into the amazing world of digital systems computer architecture , computer science and engineering .

FUTURE SCOPE

1. This project is very basic implementation of actual modern processors. By doing further development in the architecture this processor will able to do some complex processes as well.

2. Since every processor is incomplete without its supporting softwares, a standard assembler and compiler can be created to increase the pace of prototyping and debugging.

3. To make this processor further useful, a small scale version of OS like ‘TinyOS’ can be implemented on it.

4. Advanced architecture like RISC-V can further be developed from this by adding well designed base components.

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