Date: 16/6/21

Experiment no. 9

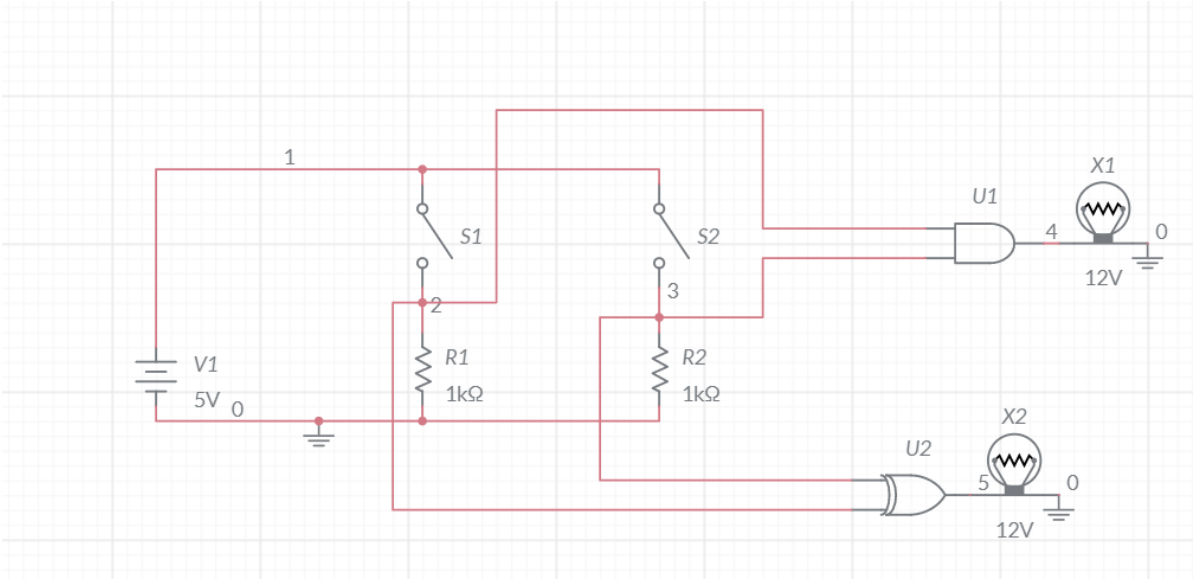
Objective: To study design of half and full adder using logic gates

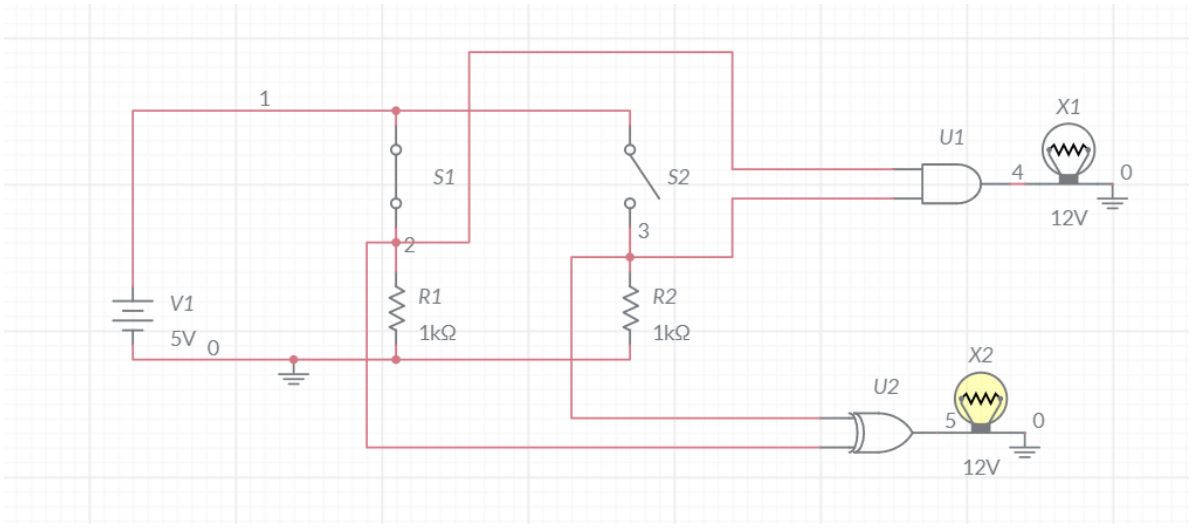
Software used: Multisim Live.

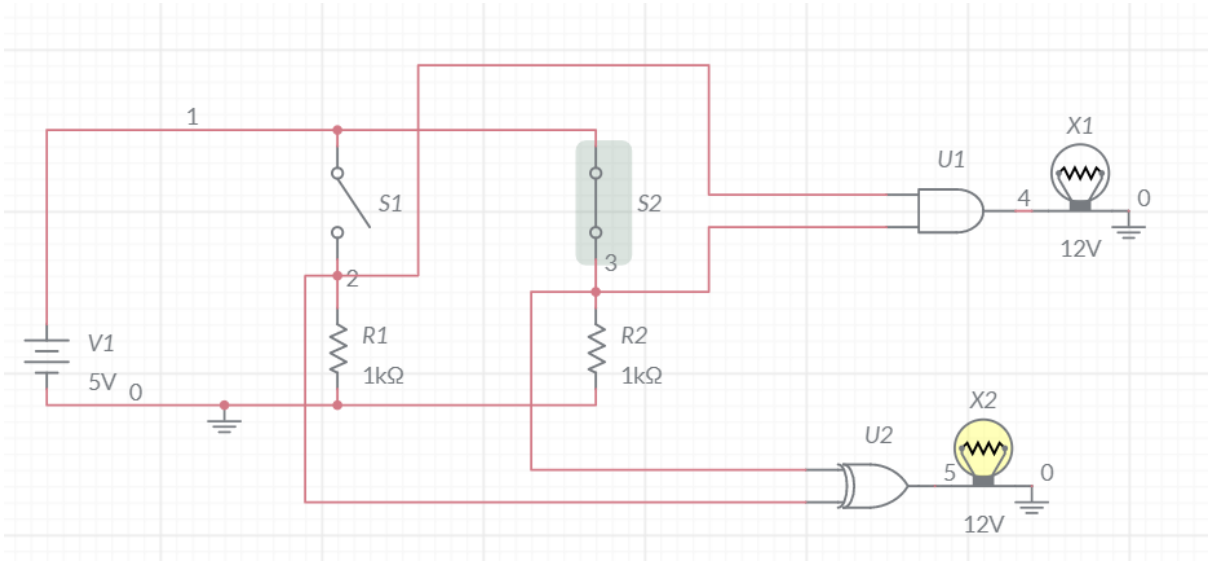
Theory: Half Adder is a combinational logic circuit which is designed by connecting one XOR gate and one AND gate. The half adder circuit has two inputs: A and B, which add two input digits and generates a carry and a sum. Full Adder is the adder which adds three inputs and produces two outputs which consists of two XOR gates, two AND gates and one OR gate. The first two inputs are A and B, and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

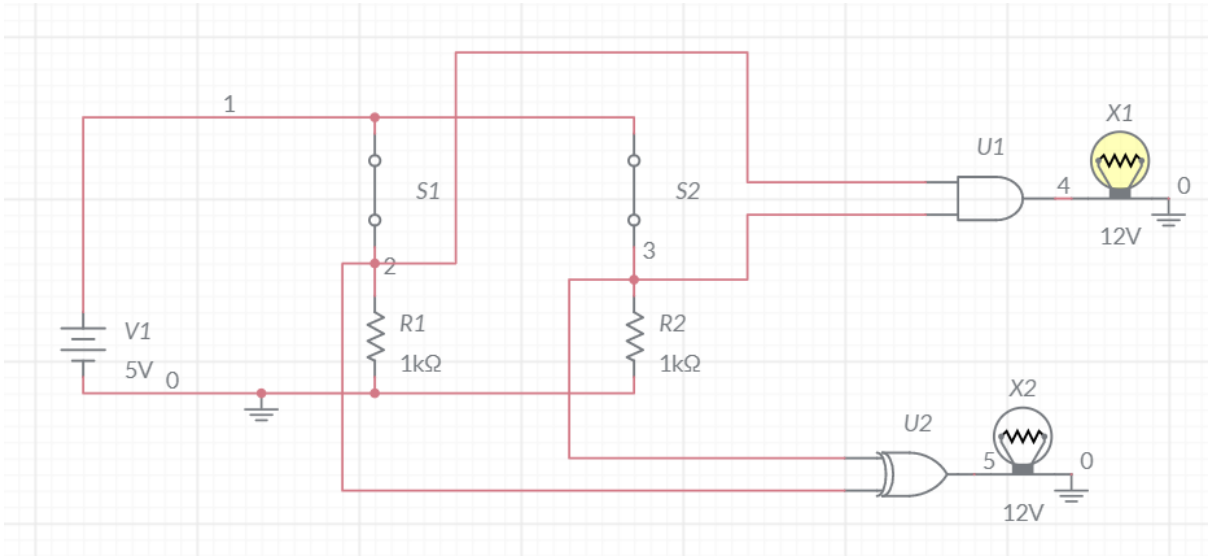
Circuit diagram:

1.Half adder circuit

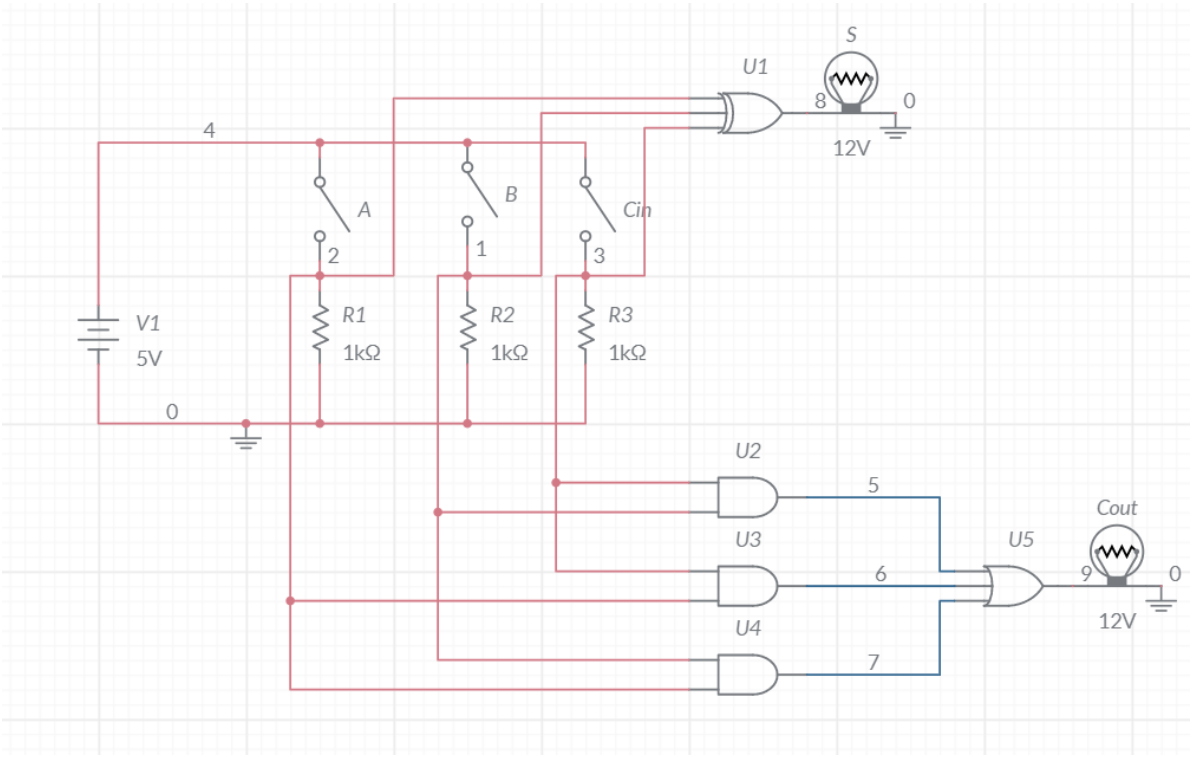


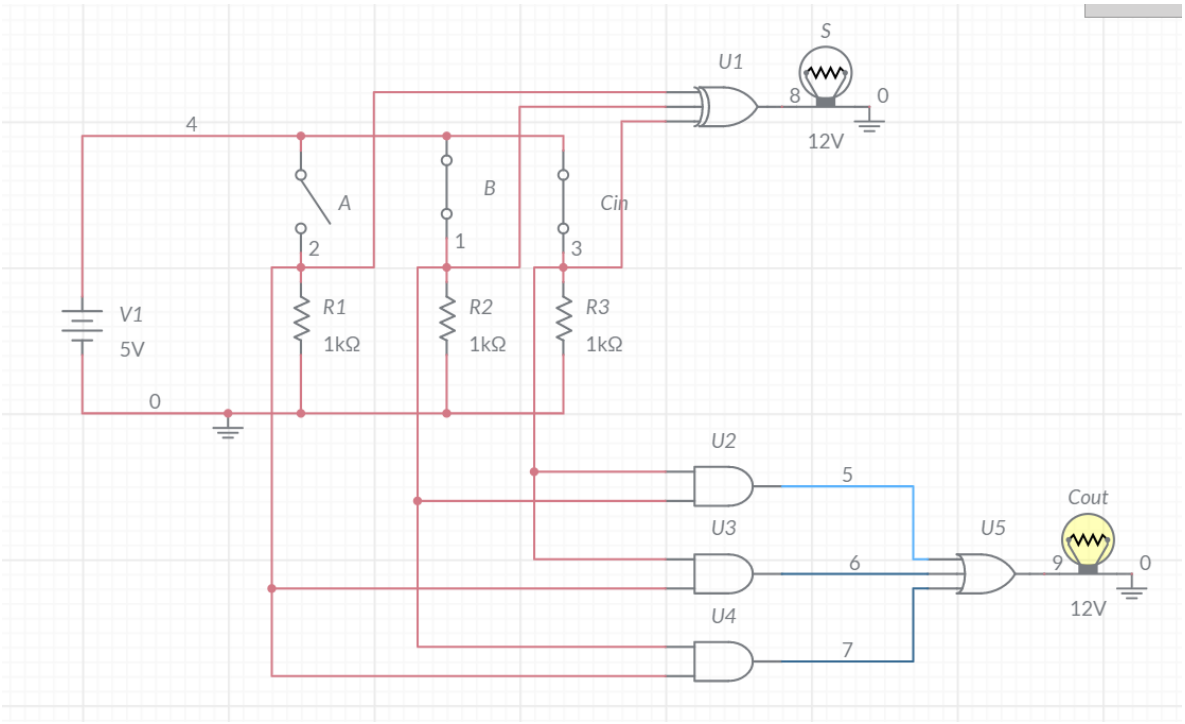

1
S1
S2
2
3
V1
5V
0
R1
1kΩ
R2
1kΩ
U1
X1
4
0
12V
U2
X2
5
0
12V

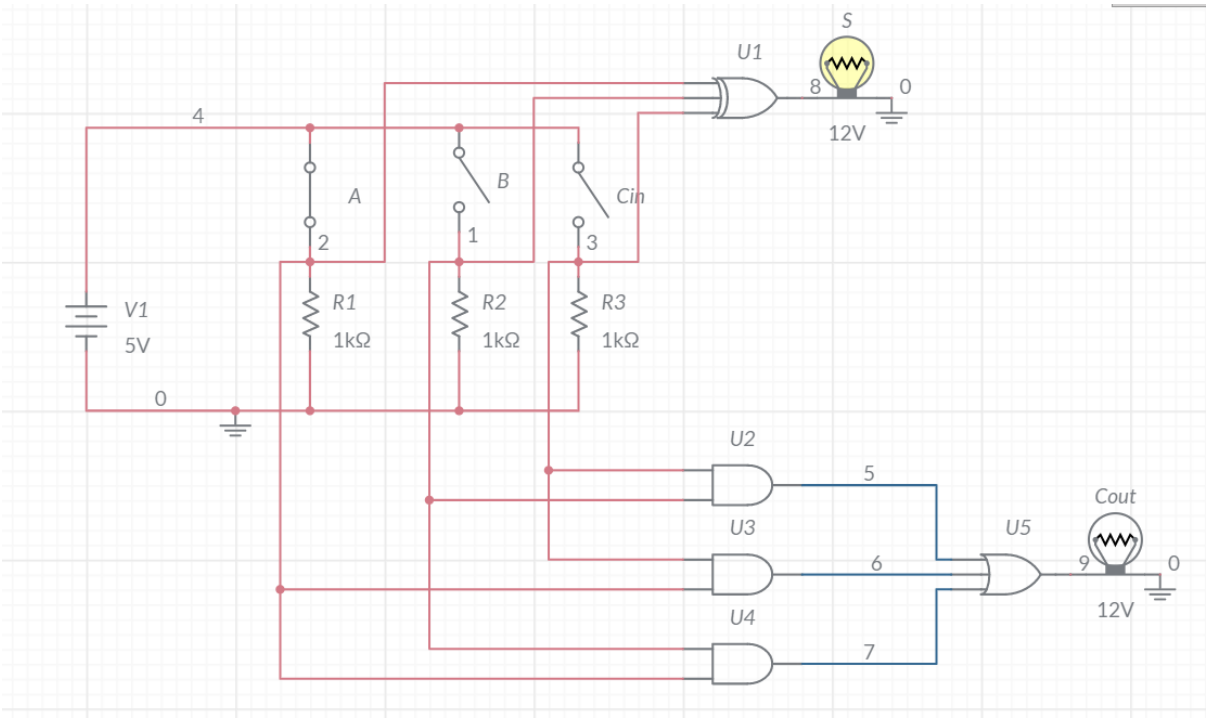

1
S1
S2
2
3
V1
5V
0
R1
1kΩ
R2
1kΩ
U1
X1
4
0
12V
U2
X2
5
0
12V

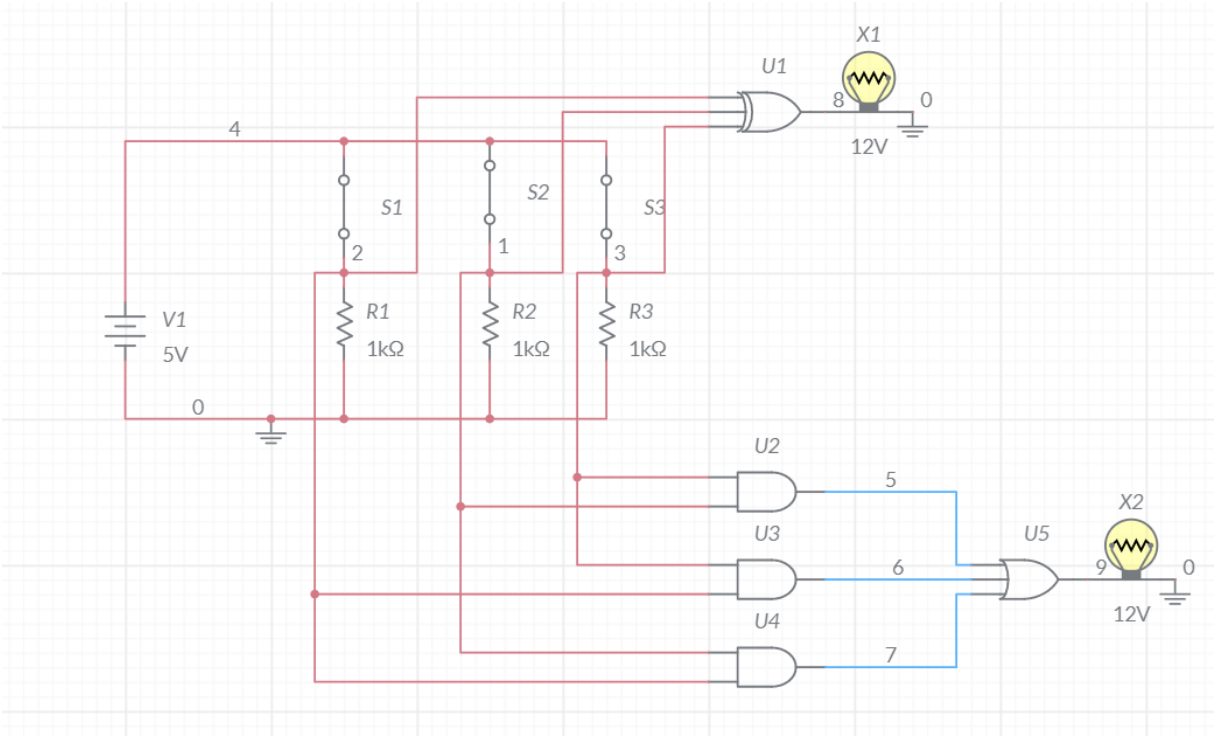

1
S1
S2
2
3
V1
5V
0
R1
1kΩ
R2
1kΩ
U1
X1
4
0
12V
U2
X2
5
0
12V

2.Full adder circuit

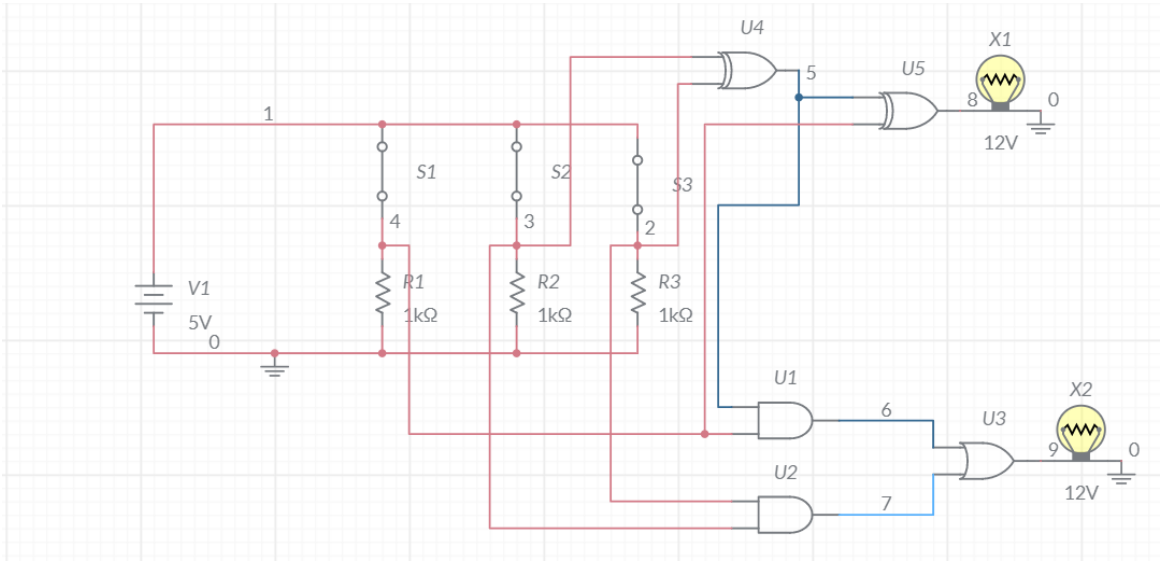





S
U1
8
0
12V
4
A
B
Cin
2
1
3
V1
5V
R1
1kΩ
R2
1kΩ
R3
1kΩ
0
U2
5
U3
U5
Cout
6
9
0
12V
U4
7


X1
U1
8
0
12V
4
S1
S2
S3
2
1
3
V1
5V
R1
1kΩ
R2
1kΩ
R3
1kΩ
0
U2
5
U3
U5
X2
6
9
0
12V
U4
7

Alternative circuit for Full adder



Result and Observations: By above circuit diagrams we can study the characteristics and design of half and full adder using logic gates.

Submitted by: G. Hruthesh Reddy(20BCB7031)