Integrated Circuit Design
Final Project Report

b05901069 鄭　昕
b05901033 莊永松

1. RTL level design methodology

We maintain a table, which has a size of 4x66, to store the input data from the testbench. The width of the table is 66 because we can set all element of this table to zero at the reset stage of the program, and store the input data from table[1] to table[64]. By doing so, the zero-padding task is fulfilled automatically.

After that, we calculate the result of convolution, then do the "ReLU" step, and store the result into the testbench. We request the input data from the testbench by using the address signal in the following order: 0, 64, 1, 65, 2, 66, ... This can make sure that we can output the result to layer 0, layer 1, and layer 2 continuously.

When all the data are generated successfully, the program will go to the idle state, waiting for the next image to process. The program will start to process the next image when the "ready" signal is triggered again.

Our RTL code can pass the simulation successfully.

```
--------------------------------------------------

START!!! Simulation Start .....

--------------------------------------------------

Layer 0 (Convolutional Output) with Kernel 0 is correct !
Layer 0 (Convolutional Output) with Kernel 1 is correct!
Layer 1 (Max-pooling Output) with Kernel 0 is correct!
Layer 1 (Max-pooling Output) with Kernel 1 is correct!
Layer 2 (Flatten  Output) is correct!

--------------------------------------------------

-------------------- S U M M A R Y -----------------

Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

Congratulations! Layer 2 data have been generated successfully! The result is PASS!!

--------------------------------------------------

Simulation complete via $finish(1) at time 327740 NS + 0
./testfixture.v:268       #(`CYCLE/2); $finish;
ncsim> exit
```

2. Gate level simulation

Our CONV_syn.v can also pass the simulation under a clock cycle of 6ns. The following are the area report and the simulation result.

```
****************************************
Report : area
Design : CONV
Version: N-2017.09-SP2
Date   : Sat Jun 22 22:33:59 2019
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          105
Number of nets:                         54940
Number of cells:                        48153
Number of combinational cells:          42285
Number of sequential cells:              5868
Number of macros/black boxes:               0
Number of buf/inv:                       3698
Number of references:                     180

Combinational area:             379212.744149
Buf/Inv area:                    26457.373902
Noncombinational area:          188559.068085
Macro/Black Box area:                0.000000
Net Interconnect area:         6769780.914246

Total cell area:                567771.812234
Total area:                    7337552.726479
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
```

```
--------------------------------------------------

--------------------- S U M M A R Y ----------------

Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

Congratulations! Layer 2 data have been generated successfully! The result is PASS!!

--------------------------------------------------

Simulation complete via $finish(1) at time 196650458 PS + 0
./testfixture.v:268       #(`CYCLE/2); $finish;
ncsim> exit
```

3. Transistor level simulation

Our CONV_APR.v can pass the simulation under a clock cycle of 10.7ns. During simulation, there will be lots of glitch suppression warnings. But that is acceptable during transistor level simulation. The following are the simulation result and the core area report.

```
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--------------------- S U M M A R Y -----------------

Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

Congratulations! Layer 2 data have been generated successfully! The result is PASS!!

--------------------------------------------------

Simulation complete via $finish(1) at time 350683989 PS + 0
./testfixture.v:268       #(`CYCLE/2); $finish;
ncsim> exit
```

```
Total area of Standard cells: 591978.434 um^2
Total area of Standard cells(Subtracting Physical Cells): 591978.434 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 930344.940 um^2
Total area of Chip: 1133594.256 um^2
Effective Utilization: 6.3630e-01
Number of Cell Rows: 261
```