两位二进制运算电路

实验二

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实验目的

1、实践用中小规模数字集成电路实现组合逻辑电路的分析与设计方法；

2、体会二进制补码的用途，掌握用补码实现减法运算的方法；

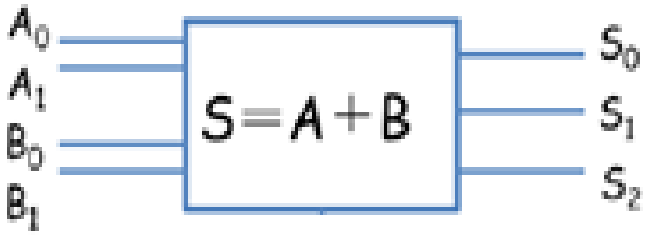
3、学习组合逻辑电路的调试方法。

实验任务

1、基本内容（加法运算）

利用与非门芯片CD4011和异或门芯片74HC86实现运算：S＝A+B

其中A和B的取值范围为0～3；



用三只发光二极管显示运算结果，二极管亮表示1，灭表示0。

实验任务

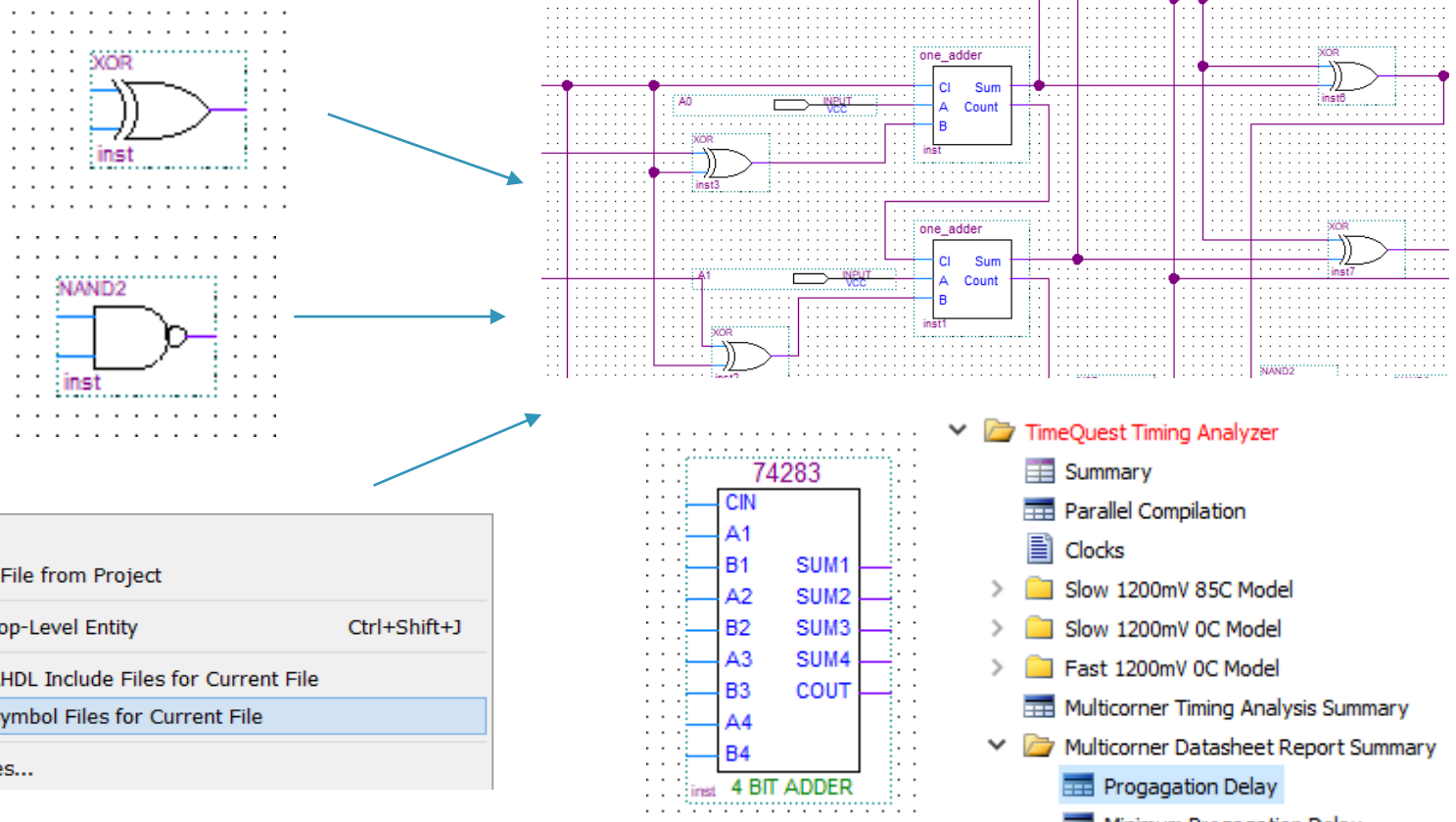
2、进一步的实验研究（减法运算）

1）实现运算**S＝A-B**。一只二极管显示运算结果的符号，亮表示负数，灭表示正数；另外两只二极管显示运算结果的数值（补码形式）。

2）进一步用原码形式显示S＝A-B的运算结果。

3）利用加法器芯片实现两位二进制加法运算，四位二进制加法器74HC283的引脚排列如图4所示，运算结果用数码管显示。

运算电路Quarurs仿真



芯片类型

74 (without letters)—Standard TTL
74S—Schottky TTL
74AS—Advanced Schottky TTL
74LS—Low-power Schottky TTL
74ALS—Advanced low-power Schottky TTL
74F—Fast TTL

TTL

74HC—High-speed CMOS
74AC—Advanced CMOS
74AHC—Advanced high-speed CMOS
74LVC—Low-voltage CMOS
74ALVC—Advanced low-voltage CMOS

CMOS

74LS00—2-input quad NAND
74LS02—2-input quad NOR
74LS04—Hex inverter
74LS08—2-input quad AND
74LS10—3-input triple NAND
74LS11—3-input triple AND
74LS20—4-input dual NAND
74LS21—2-input AND
74LS27—30-input quad OR
74LS30—8-input single NAND
74LS32—2-input quad OR
74LS86—Quad XOR
74LS266—Quad XNOR

芯片型号

前缀+数字+后缀

生产厂商

器件功能

封装、性能

HD74HCT238

3-to-8-line Decoder/Demultiplexer

HITACHI

Description

The HD74HCT238 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determined which one of the eight normally high outputs will go low. Two active low and one active high enables (G_1, $\overline{G_{2A}}$ and $\overline{G_{2B}}$)

Features

- LSTTL Output Logic I
- High Speed Operation:
- High Output Current:

TOSHIBA TC74HC238AP/AF

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC238AP,TC74HC238AF

3-to-8 Line Decoder

The TC74HC238A is a high speed CMOS 3-to-8 DECODER fabricated with silicon gate C²MOS technology.

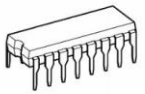
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs (Y0-Y7) will go high.

When enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, decoding function is inhibited and all the outputs go low. G1, $\overline{G2A}$, and $\overline{G2B}$ inputs are provided ease cascade connection and for use as an adress decoder for memory systems.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC238AP



DIP16-P-300-2.54A

TC74HC238AF

SOP16-P-300-1.27A

Weight

DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

- High speed: t_{pd} = 14 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} = t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2~6 V
- Pin and function compatible with 74LS238

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor SCHS147I

October 1997 - Revised August 2004

CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238

High-Speed CMOS Logic 3- to 8-Line Decoder/ Demultiplexer Inverting and Noninverting

Features

- Select One Of Eight Data Outputs Active Low for 138, Active High for 238
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2 V to 6 V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}

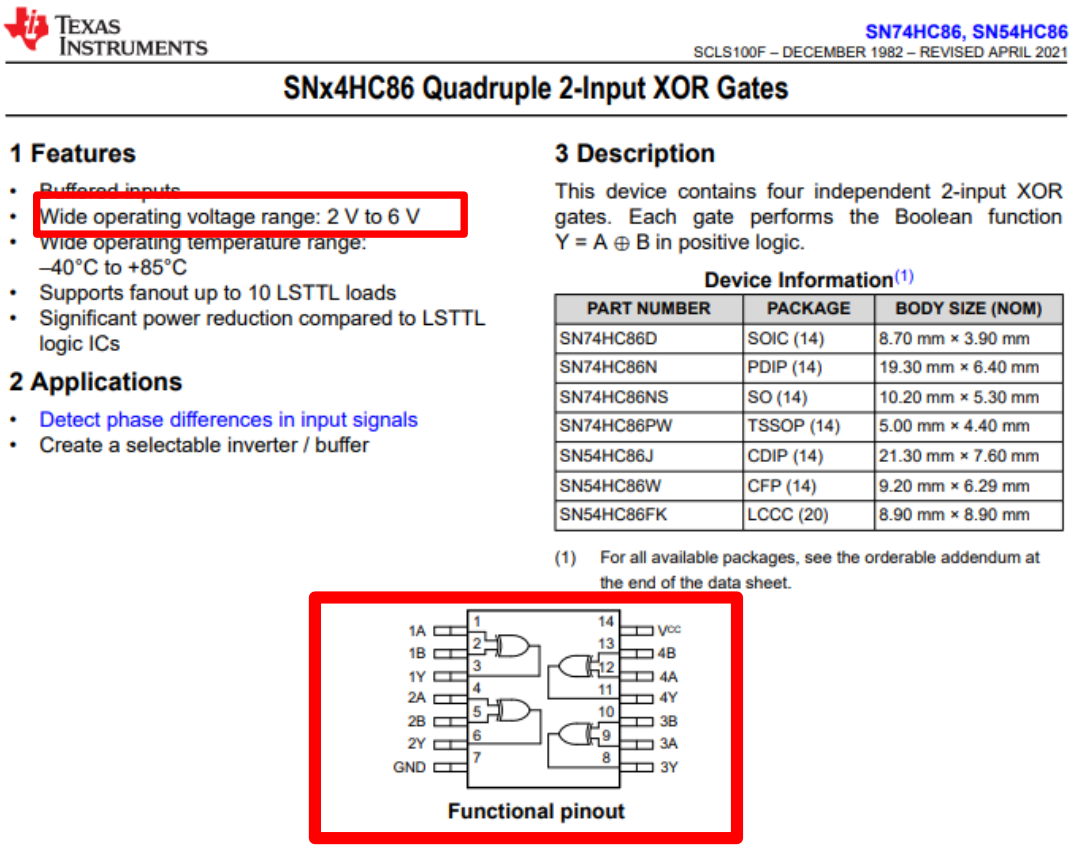
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC138F3A	-55 to 125	16 Ld CERDIP
CD54HC238F3A	-55 to 125	16 Ld CERDIP
CD54HCT138F3A	-55 to 125	16 Ld CERDIP
CD54HCT238F3A	-55 to 125	16 Ld CERDIP
CD74HC138E	-55 to 125	16 Ld PDIP
CD74HC138M	-55 to 125	16 Ld SOIC
CD74HC138MT	-55 to 125	16 Ld SOIC
CD74HC138M96	-55 to 125	16 Ld SOIC
CD74HC238E	-55 to 125	16 Ld PDIP
CD74HC238M	-55 to 125	16 Ld SOIC
CD74HC238MT	-55 to 125	16 Ld SOIC

芯片数据手册（datasheet）

数据手册可以查看：

- ✓ 总体功能及电特性基本参数；
- ✓ 管脚定义、真值表；
- ✓ 极限参数、电特性详细参数；
- ✓ 参考电路及应用；
- ✓ 芯片封装（PCB制板）



TEXAS INSTRUMENTS

SN74HC86, SN54HC86

SCLS100F – DECEMBER 1982 – REVISED APRIL 2021

SNx4HC86 Quadruple 2-Input XOR Gates

1 Features

- Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Wide operating temperature range: –40°C to +85°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

2 Applications

- Detect phase differences in input signals
- Create a selectable inverter / buffer

3 Description

This device contains four independent 2-input XOR gates. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC86D	SOIC (14)	8.70 mm × 3.90 mm
SN74HC86N	PDIP (14)	19.30 mm × 6.40 mm
SN74HC86NS	SO (14)	10.20 mm × 5.30 mm
SN74HC86PW	TSSOP (14)	5.00 mm × 4.40 mm
SN54HC86J	CDIP (14)	21.30 mm × 7.60 mm
SN54HC86W	CFP (14)	9.20 mm × 6.29 mm
SN54HC86FK	LCCC (20)	8.90 mm × 8.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

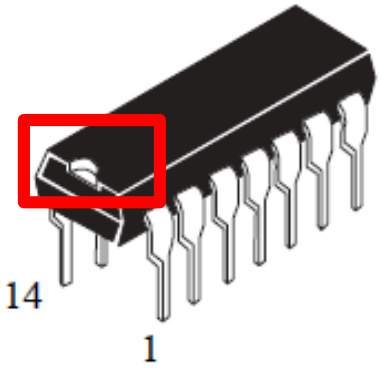
Functional pinout

芯片安装使用

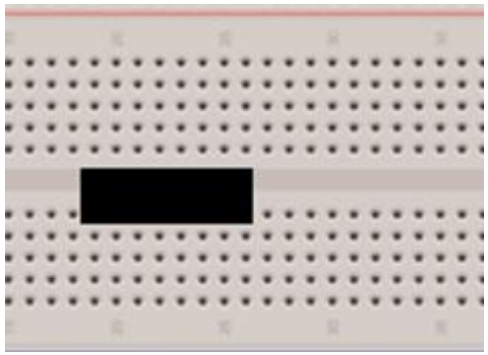
- ✓ 在面包板槽两侧插牢固
- ✓芯片要供电、接地
- ✓不允许带电插拔；
- ✓不允许输入负电压；
- ✓不用的输入端不得悬空。

  与门、与非门接高电平

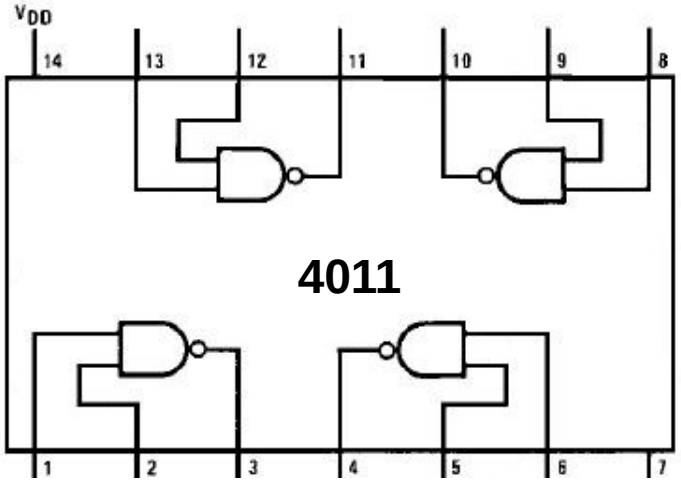
  或门、或非门接低电平



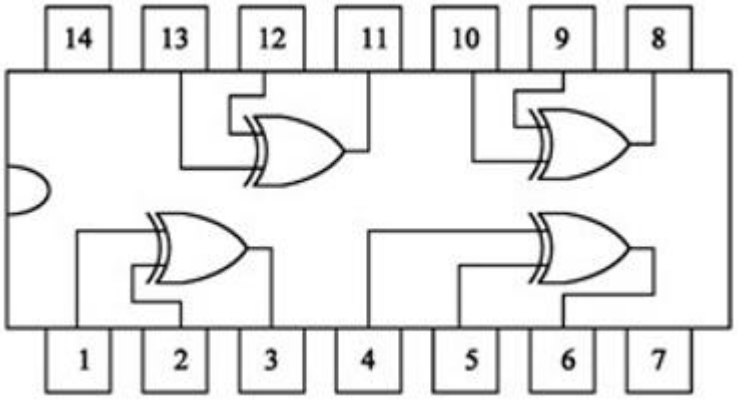
DIP 14(CD4011BE)



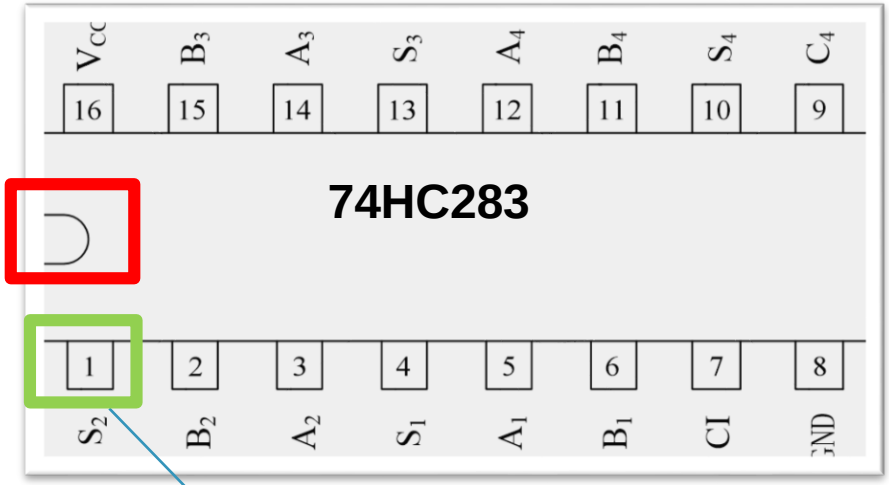
芯片引脚图



4011



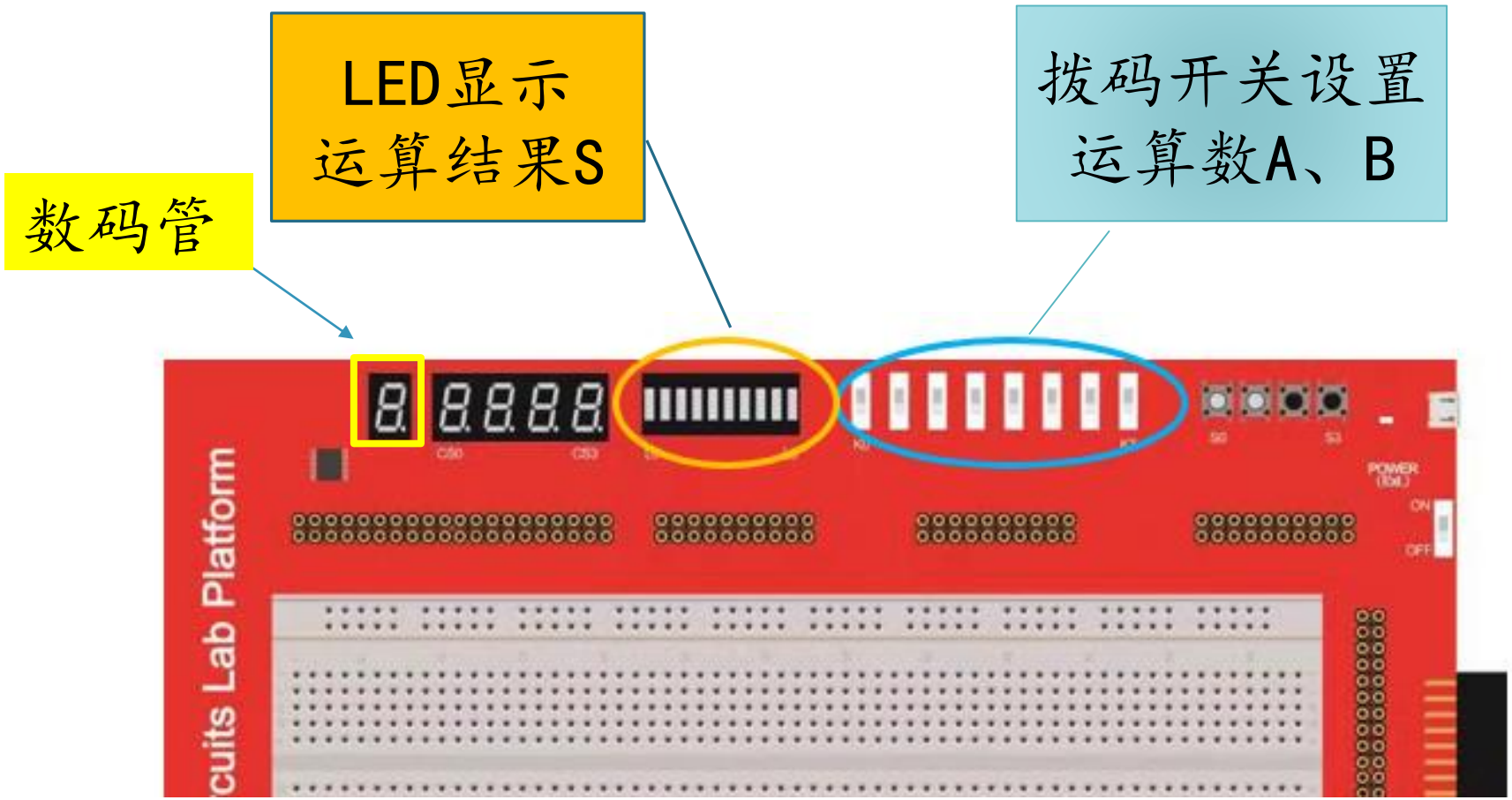
74HC86



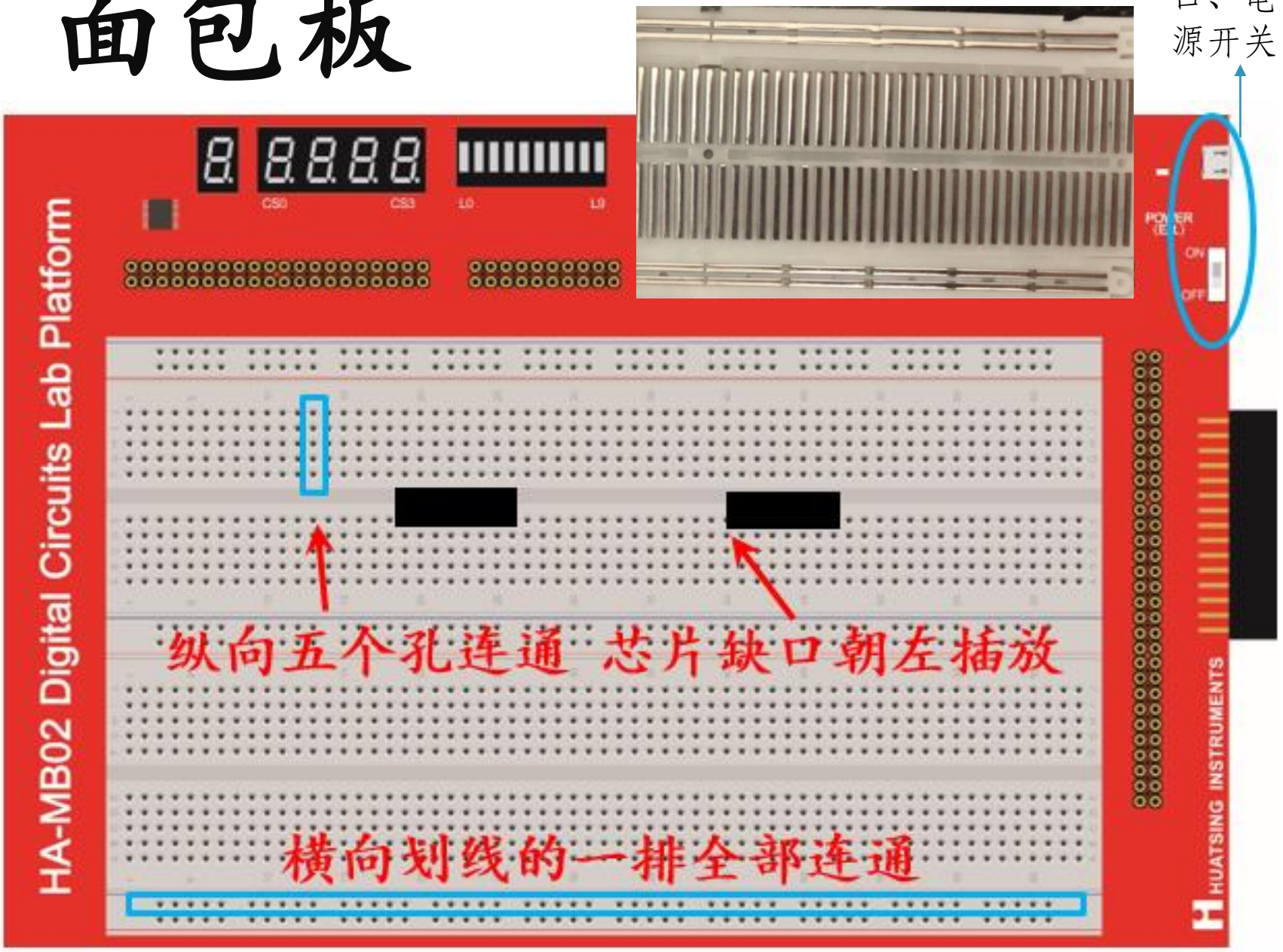
74HC283

芯片缺口左下角表示引脚起始编号

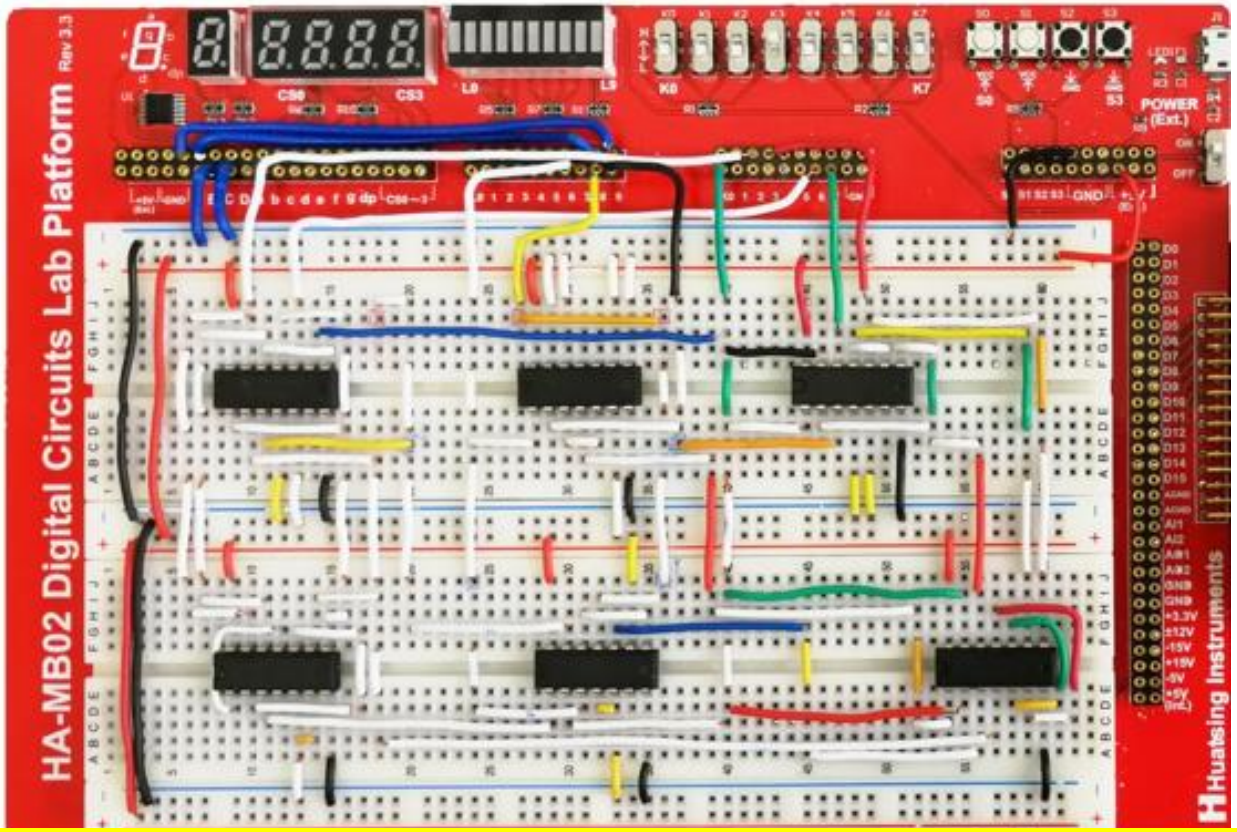
实验板外设使用



面包板


电源接口、电源开关
HA-MB02 Digital Circuits Lab Platform
HUATSING INSTRUMENTS
纵向五个孔连通 芯片缺口朝左插放
横向划线的一排全部连通

布线注意事项



✓导线应贴近面包板，在芯片周围走线；

✓尽量减少导线裸露部分，不允许在芯片上方跨接导线，切忌在一个插孔内插入两根导线。

剥线钳使用

1、拨动剥线钳锁止拨片使剥线钳能够张开。
2、找到比导线粗度略小的剥线孔（0.2mm²）。
3、将电线放入剥线孔，合拢剥线钳，剥下绝缘层。

电路故障排查

测量**电源输出**电压是否符合要求；

测量芯片**引脚**的电源端、接地端的电压是否符合要求；

上电后用手触摸芯片，过烫断电；

在进行芯片和元器件替换的过程中，应切断电源，严禁带电操作；

若输入信号如何变化，输出一直保持高电平不变时，检查地线是否接好；

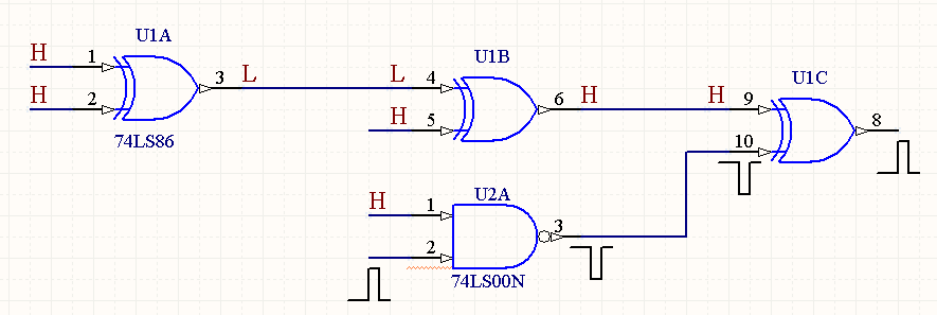
若输出信号的变化规律和输入的相同，检查电源线是否接好；

电路故障排查

- **化整为零**，将整个实验电路划分为单元模块，先单元调试后整体联调。
- 静态测量法**逐级检查信号电平**；
- 检查逻辑门的逻辑功能；
- 检查是否有多个输出端错误地连接在一起。

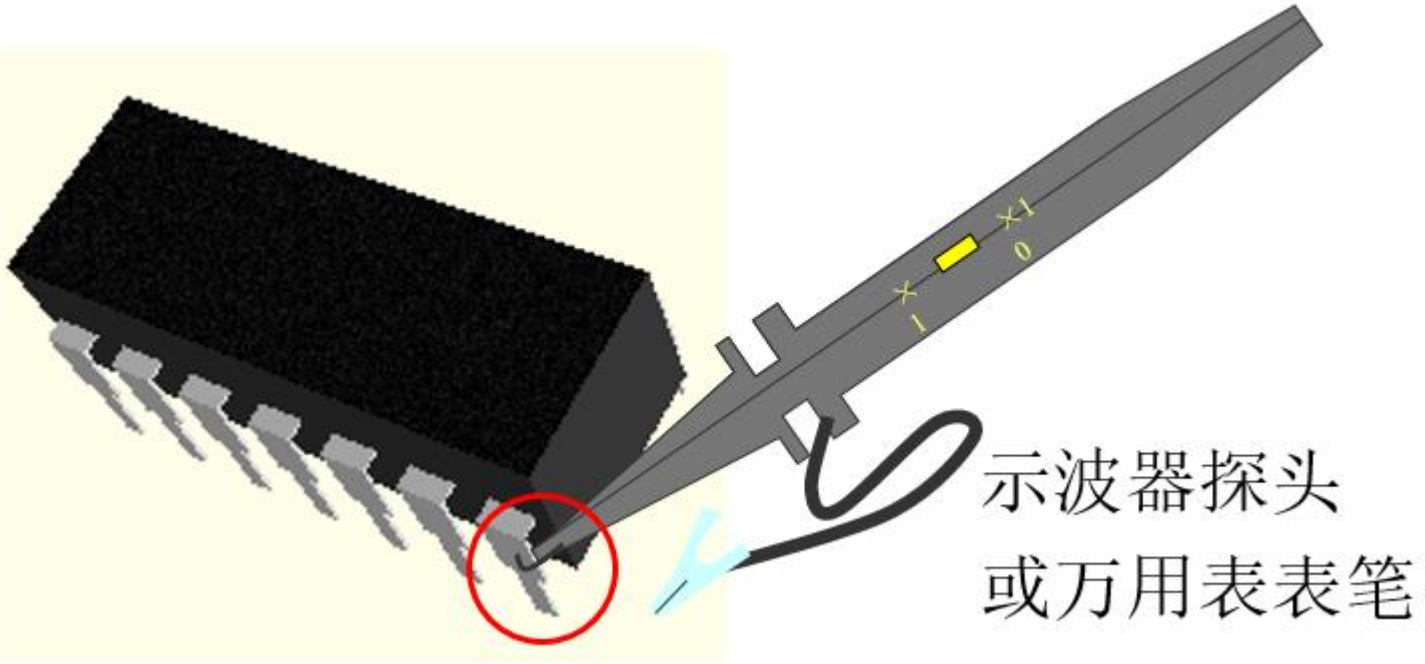
静态测量法

- ✓将电路固定于一故障状态；
- ✓沿信号流向用电压表或LED灯逐级测量电路各级的输入、输出电平；
- ✓观察测量结果是否与设计逻辑值相一致，直到发现故障为止。
- ✓建议由后向前逐级检查，“顺藤摸瓜”

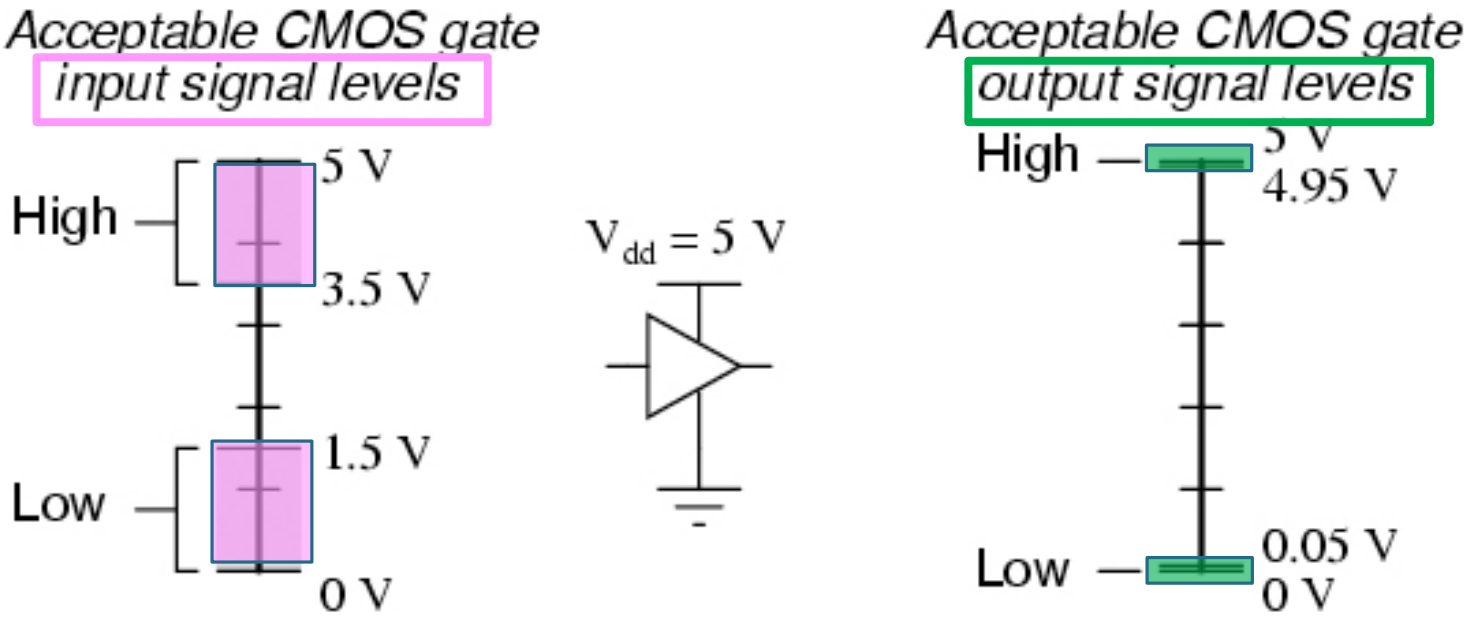


芯片引脚电平不正常原因：断线、错接、漏接、面包板接触不良。

信号测量点应是芯片的管脚处

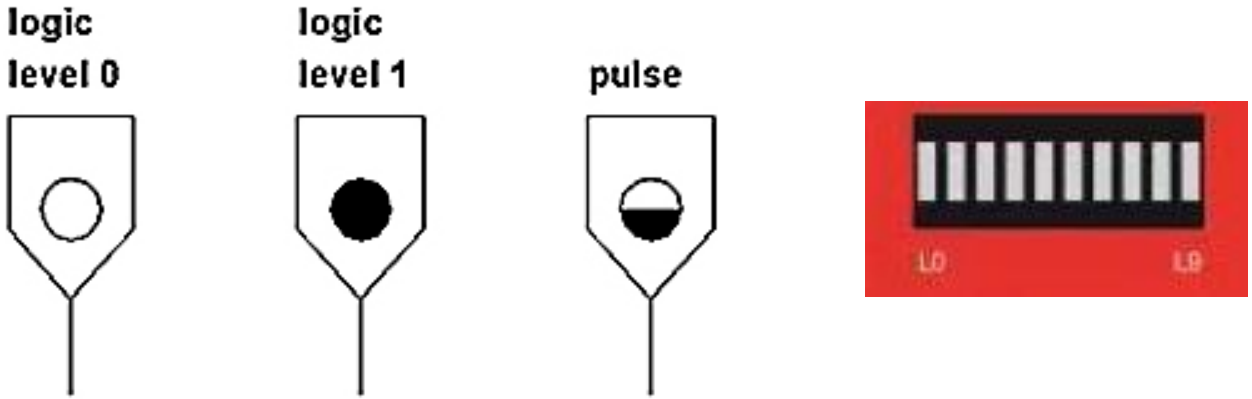


CMOS门电路电平标准



端口允许的电平	低电平	高电平
输入端	0~1.5V	3.5~5V
输出端	0~0.05V	4.95~5V

用LED灯测试电路



逻辑”1”高电平，LED灯亮
逻辑”0”低电平，LED灯灭
逻辑”0”、”1”之间的电平，LED半亮或闪烁。

实验报告要求

一、提交内容

a. 实验电路的设计，包括设计思想、电路原理图、真值表；
b. 整理实验结果，附上整体电路实物图及必要的实现效果图。
c. 整理在实验中遇到的问题及解决方法
d. 实验体会（如有）

二、提交时间

请在网络学堂提交电子版实验报告。截止时间11月21日