2021 ICLAB SPRING (IEE5035)

Syllabus

Instructor:

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Lecture Time:

- W56(3EF, 13:30 ~ 15:30, Wednesday) @ ED415

Teaching Assistant:

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Prerequisites:

- Introduction to VLSI, Logic Design, Digital System Design, Computer Organization (Opt)

Course Objectives:

This course aims to convey the senior and graduated EE students techniques to design the VLSI chips using state-of-the-art CAD tools. In addition to learning CAD tools for performance-driven and cost effective IC designs, a top-down design flow and related environment will also be addressed. Upon completion of the course, the student will be able to design the integrated circuits and systems based on standard cell library as well as full-custom layout approaches. As such he/she will be able to work in a team of designers or stand alone.

Grading Policy

Weekly Lab Exercise x12	**(60%)**
Midterm Project	**(10%)**
Midterm Exam	**(6%)**
Online Test	**(8%)**
Final Project	**(10%)**
Final Exam	**(6%)**
Bonus (Formal Verification)	**(3%)**

Course Schedule:

Week	Date	Course Content	TA
1	02/24	00、Introduction (Environment Setting)	黃熙皓
2	03/03	01、Verilog Combination Syntax	賴林鴻
3	03/10	02、Sequential Logic Design I + generate	何信祁
4	03/17	03、Test Bench Programming Syntax	黃資芸
5	03/24	04、Sequential Logic Design II	王海峰
6	03/31	05、Memory & coding style & nLint	賴劭芃
7	04/07	06、Design Compiler + IP Design with genvar (Release Midterm Project 04/07)	李奐融
8	04/14	No class: study day	黃熙皓
8	04/17 (Sat.)	**Midterm Exam (Online Test)**	黃熙皓
9	04/21	07、Synthesis Static Time Analysis + Cross Clock Domain	王海峰
10	04/28	08、Low power design	賴劭芃
11	05/05	09、System Verilog I (Design) (Midterm project demo 4/26)	許連逢
12	05/12	10、System Verilog II (Verification)	何信祁
13	05/19	Formal Verification (Bonus)	賴林鴻
14	05/26	11、APR I : From RTL to GDSII (Release Final Project 5/28)	李奐融
15	06/02	12、APR II : IR-Drop Analysis	黃資芸
16	06/09	**Final Exam**	黃熙皓
17	06/16	**Final Project Demo**	黃熙皓