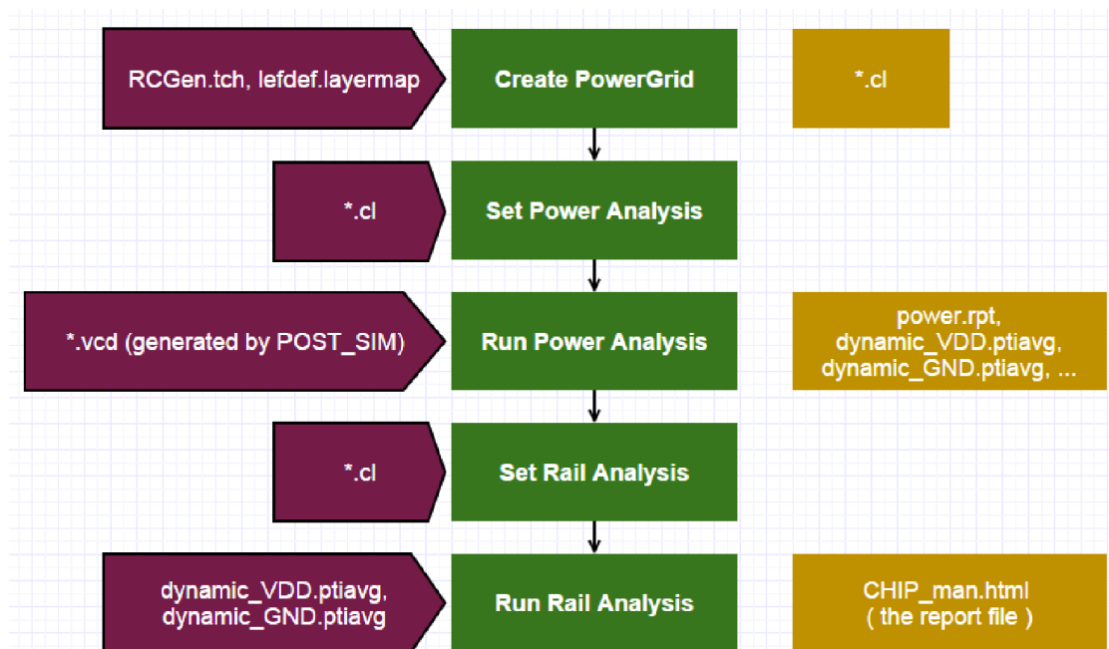# NCTU-EE IC Design LAB - Fall 2023

Lab13 Power Rail Analysis Practice Tutorial

1. Flow overview


2. Set environment

- unix% tar −xvf ~iclabta01/Lab13.tar

- unix% cd Lab12/Practice/05_APR

- unix% mkdir power_log   (You will save all the things here)

- unix% innovus

- Restore the design **DBS/CHIP.inn**

3. Static Power Analysis

1. Save CHIP.v

2. Write CHIP.sdf

3. Run post simulation at 06_POST, the generated waveform CHIP_POST.fsdb will be used for power rail analysis.

4. In the innovus menu, open **Power** -> **Power Analysis** -> **Setup**
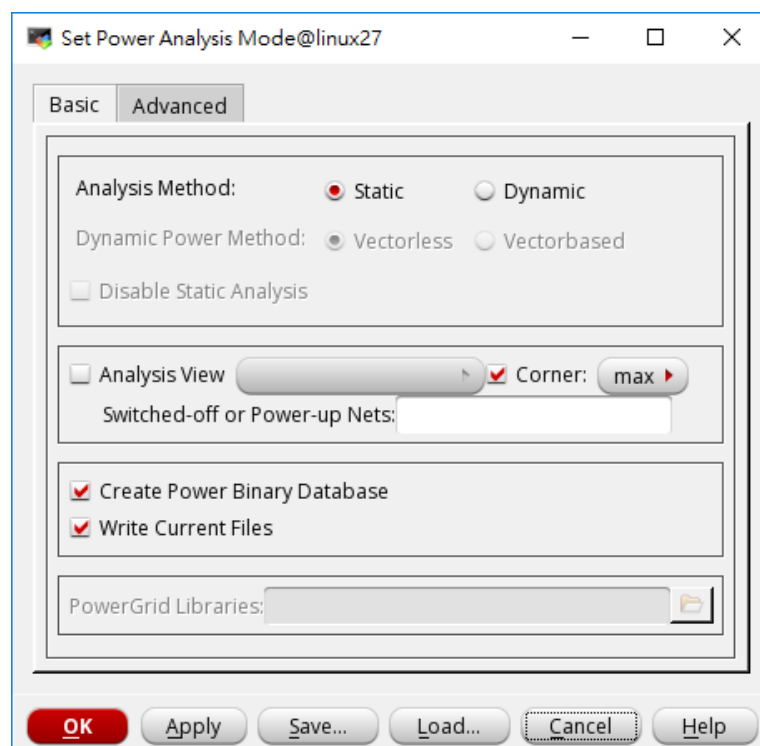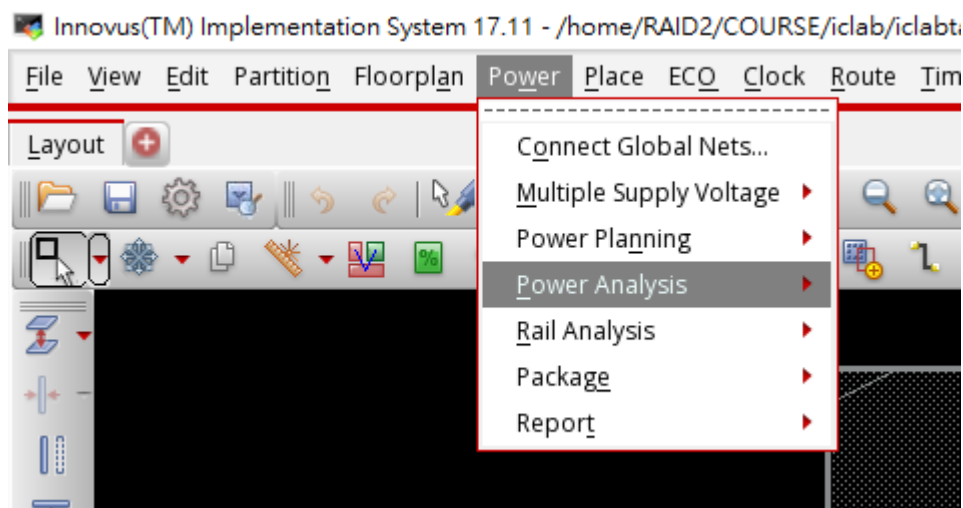
i. Click OK.

5. In the innovus menu, open *Power* -> *Power Analysis* -> *Run*
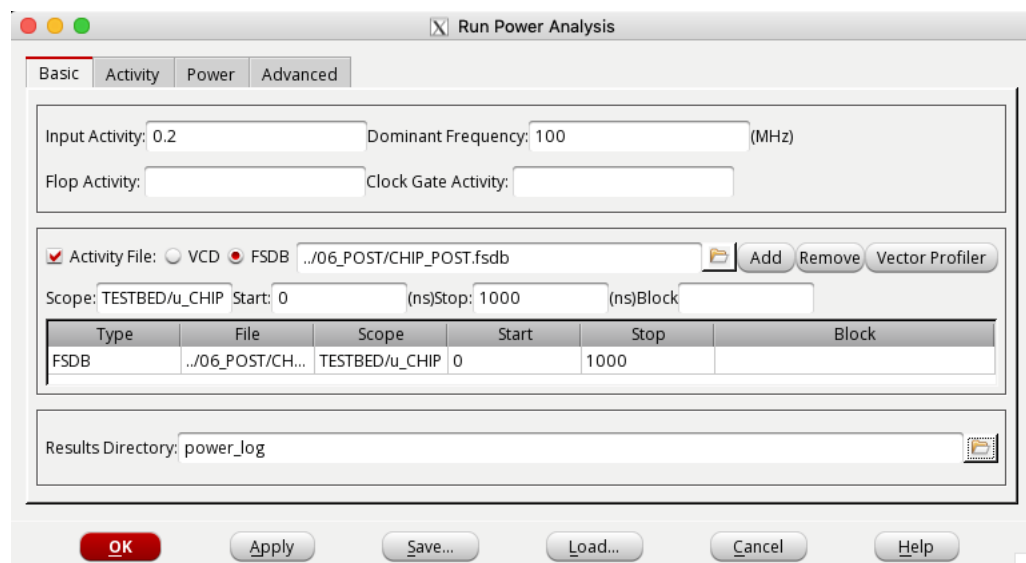
    i. ◆Activity FILE ◆FSDB

    ii. Fill the information:

- Select CHIP_POST.fsdb (from 06_POST)

- Scope: TESTBED/u_CHIP

- Start: 0; Stop: 1000

- Press Add

    iii. Results Directory: power_log

    iv. Click OK.
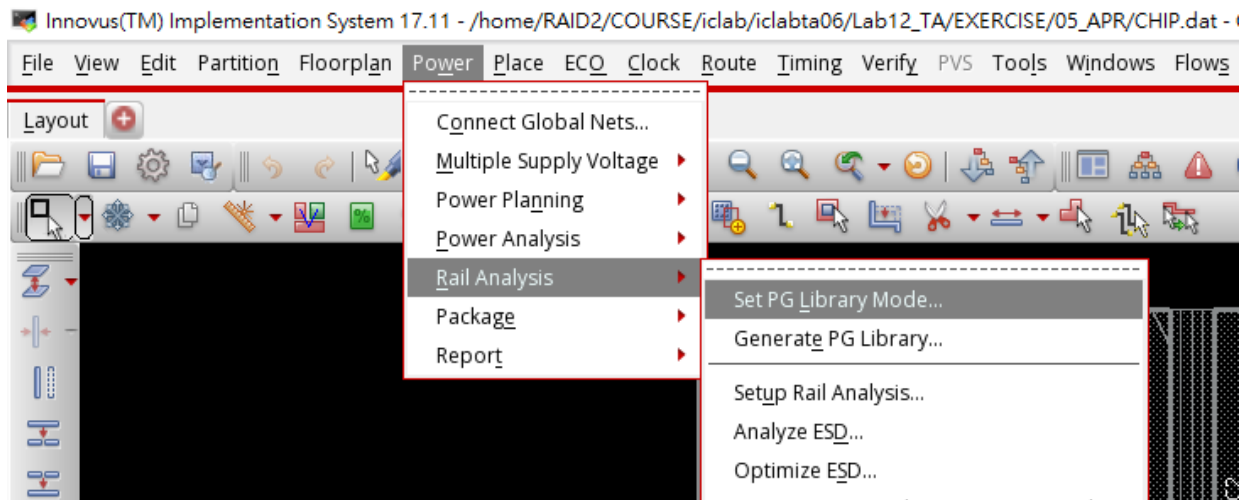

    v. Results appear at terminal
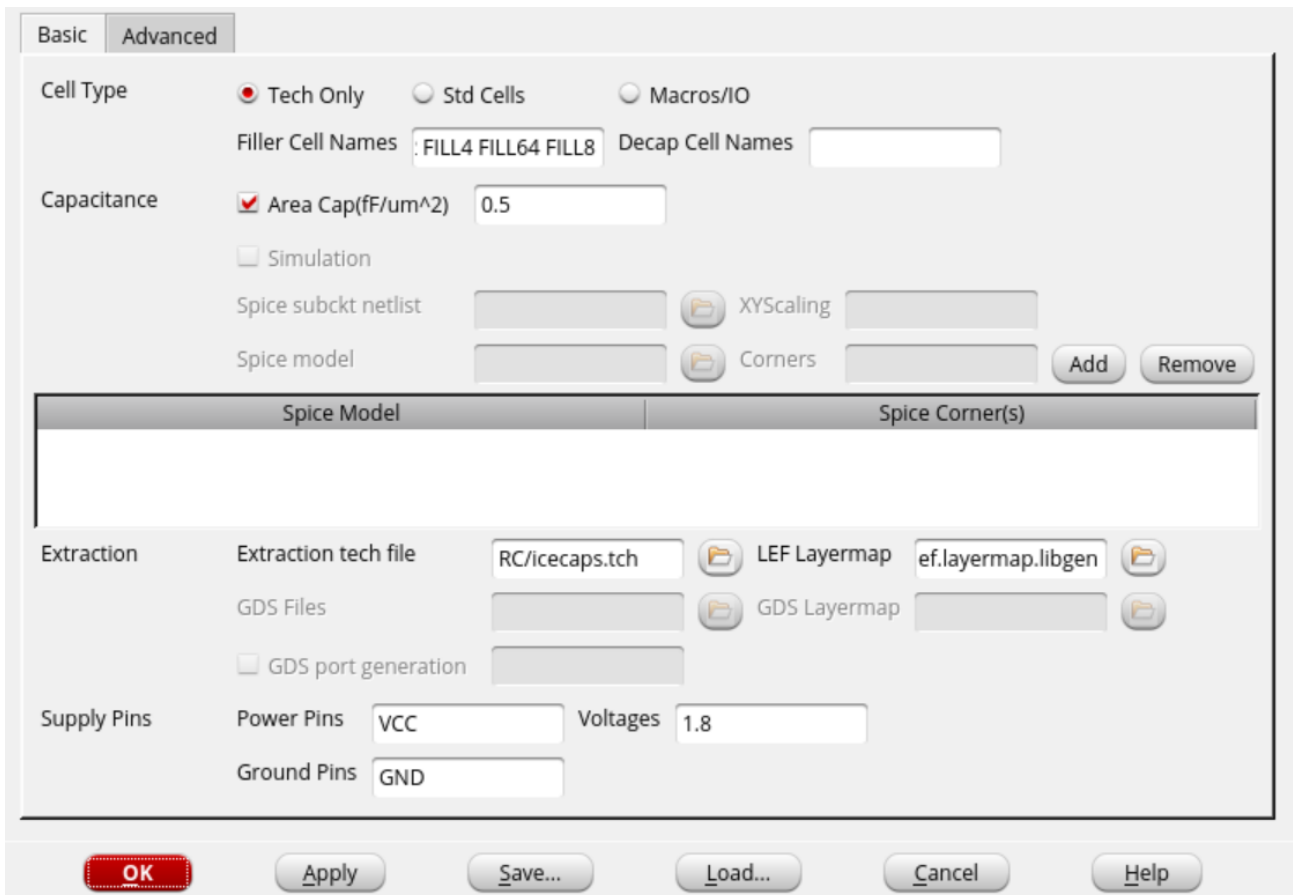
4. Create Power Grid Library

1. In the innovus menu, open **Power** -> **Rail Analysis** -> **Set PG Library Mode**

i.   Cell type: ◆Tech Only

ii. Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**

iii. Extraction

   - Extraction tech file: **05_APR/RC/icecaps.tch** (File of type: All files(*))

   - LEF Layermap: **05_APR/layermap/lefdef.layermap.libgen**(File of type: All files(*))

iv. Supply Pins

   - Voltages: **1.8**

   - Power pin: **VCC**

   - Ground pin: **GND**

v.   Click OK

2. In the innovus menu, open ***Power -> Rail Analysis -> Generate PG Library***

   i.   Choose power_log

   ii.   Click OK

   iii.   Check if the directory **techonly.cl** exists (under power_log/)

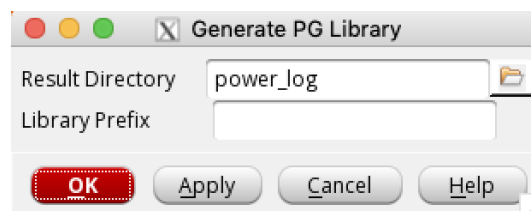**3.** In the innovus menu, open *Power -> Rail Analysis -> Set PG Library Mode*

    i.   Cell type: ◆Std Cells

    ii.   Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**

    iii.   Extraction

- Extraction tech file: **05_APR/RC/icecaps.tch**

- LEF Layermap: **05_APR /layermap/ lefdef.layermap.libgen**

    iv.   Supply Pins

- Voltage: **1.8**

- Power pin: **VCC**

- Ground pin: **GND**

    v.   Click **OK**.

4. In the innovus menu, open *Power -> Rail Analysis -> Generate PG Library*

     i. Click OK

     ii. Check if the directory **stdcells.cl** exists (under power_log/)

5. Rail Analysis

1. In the innovus menu, open *Power -> Rail Analysis -> Setup Rail Analysis*

   i. Analysis Method: ◆ **Static**

     ii. PowerGrid Libraries:

        power_log/**technoly.cl** (should be added first)
        power_log/**stdcells.cl**

     iii. Click **OK**
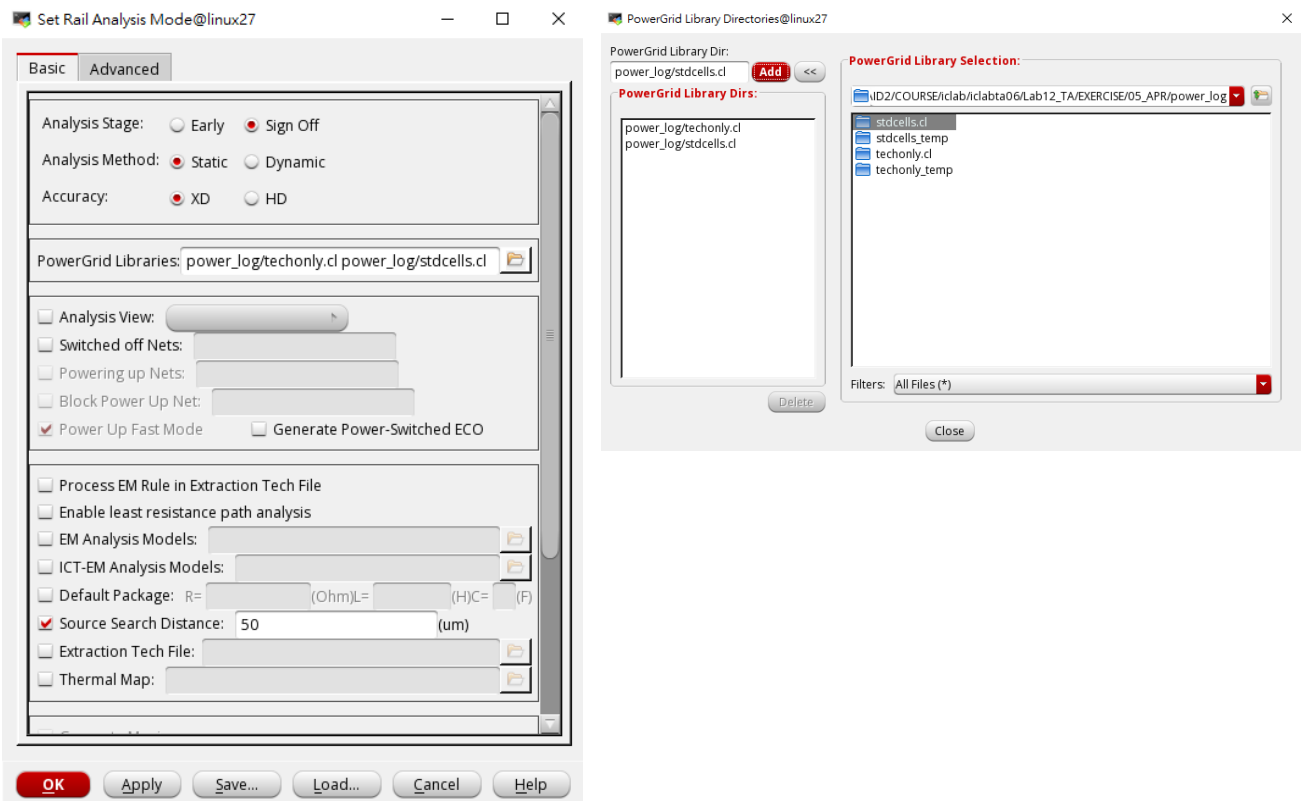
2. In the innovus menu, open *Power -> Rail Analysis -> Run Rail Analysis*

    i.   ◆ Domain Based Domain Name: PD

    ii.   Power Net(s): VCC   Voltage(s): 1.8 Threshold:1.7 (Press ADD)

          Power Net(s): GND   Voltage(s): 0   Threshold:0.1 (Press ADD)

          *(1.8v * 5% ≈ 0.1v)*

    iii.   Power/Current Files(s):

          power_log/static_VCC.ptiavg

          power_log/static_GND.ptiavg

    iv.   Power Pads: ◆ XY File

    v.   Click **Create**

- Net Name: VCC
- Click **Fetch**
- Save as **power_log/CHIP_VCC.pp**

    vi.   Click **Create** again

- Net Name: GND
- Click **Fetch**
- Save as **power_log/CHIP_GND.pp**

    vii.   Click **Cancel**

    viii.   File: **power_log/CHIP_VCC.pp** Net Name: VCC (press ADD)

    ix.   File: **power_log/CHIP_GND.pp** Net Name: GND (press ADD)

    x.   Results Directory: **power_log**

    xi.   Click **OK**
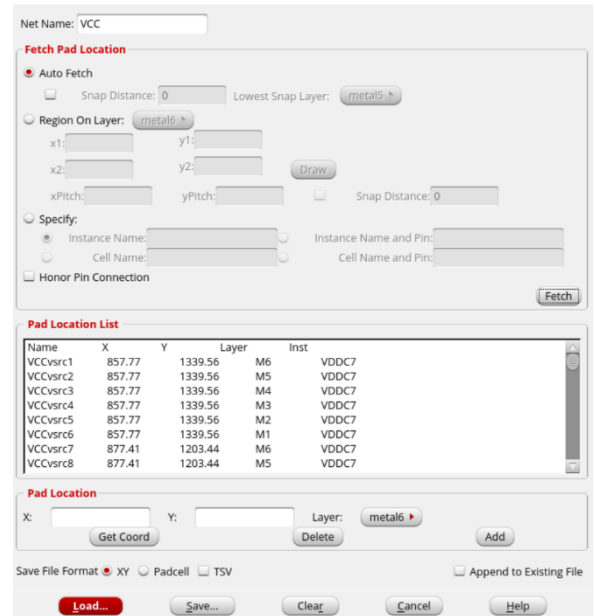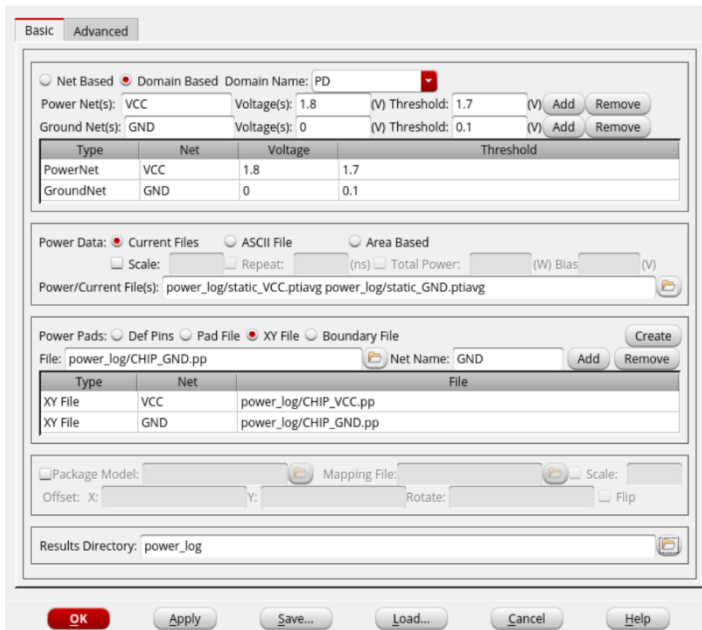
6. Power & IR Drop Results

1. In the innovus menu, open **Power -> Report -> Power & Rail Result**
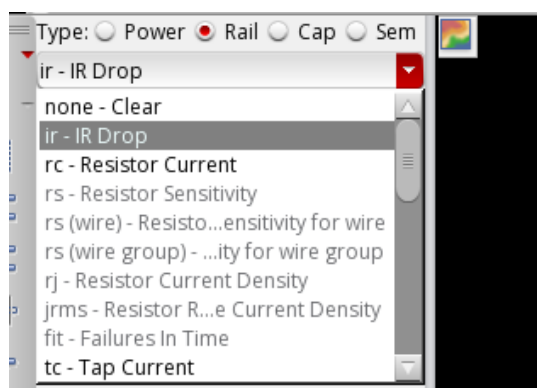
   i. ◆Auto Apply for Color Scale

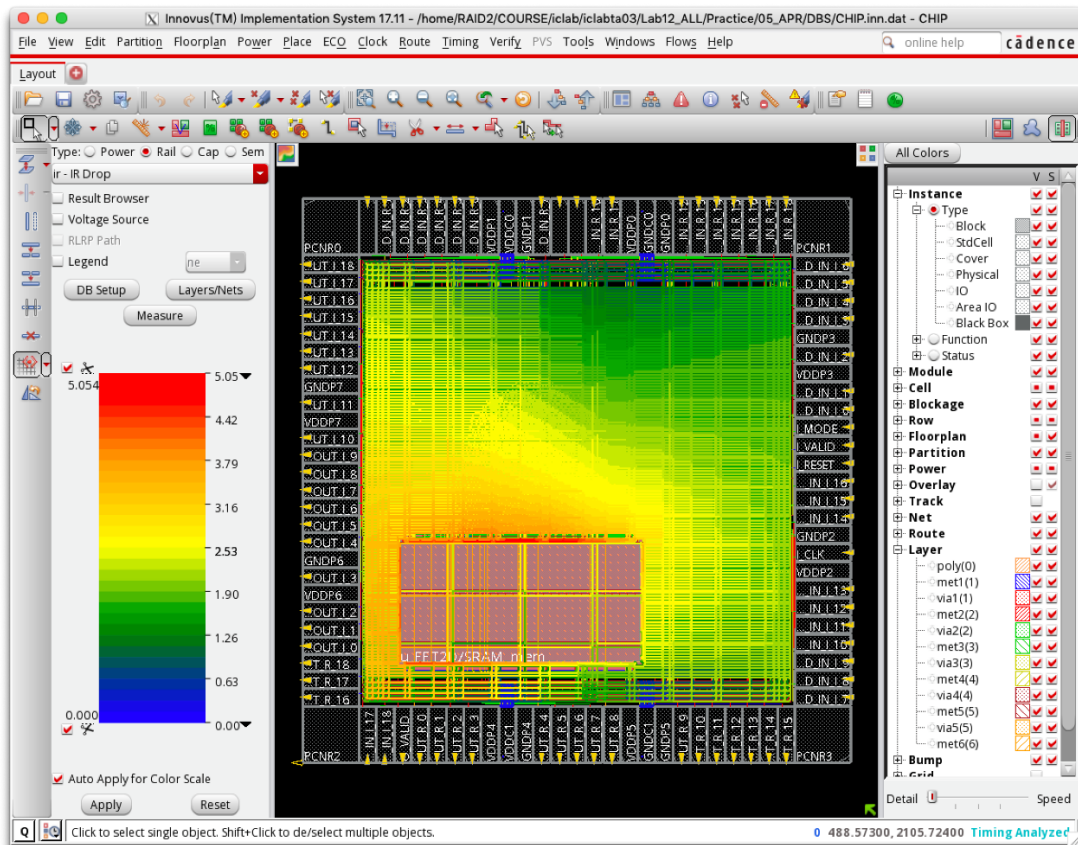   ii. Click DB Setup

      - Power Databas: power_log/power.db

      - Rail Database: power_log/PD_25C_avg_1

      - Click OK

   iii. Type: ◆Rail

   iv. Choose ir – IR Drop

i. ◆Result Browser

The following shows the distribution of IR Drop (they should in the range **0.1V**)