

# Introduction to JasperGold SuperLint

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## Outline

- Lint / Auto-Formal Categories
- Basic Lint / Auto-Formal Execution Steps
- How to use
- Summary
- Reference



## Lint Categories (1/3)

- NAMING
  - Checks naming conventions on RTL elements, for example modules, instances functions, etc. based on a rules file defined by user
- FILEFORMAT
  - Checks file formatting to make files portable and reusable, for example, file name different from module name
- CODINGSTYLE
  - Checks to ensure there are no semantic and functional issues in the code, for example, unconnected ports, unused and unassigned variables, or undriven signals
- SIM\_SYNTH
  - Checks for scenarios that can cause mismatch between pre and post synthesis simulation results, for example, incomplete sensitivity list



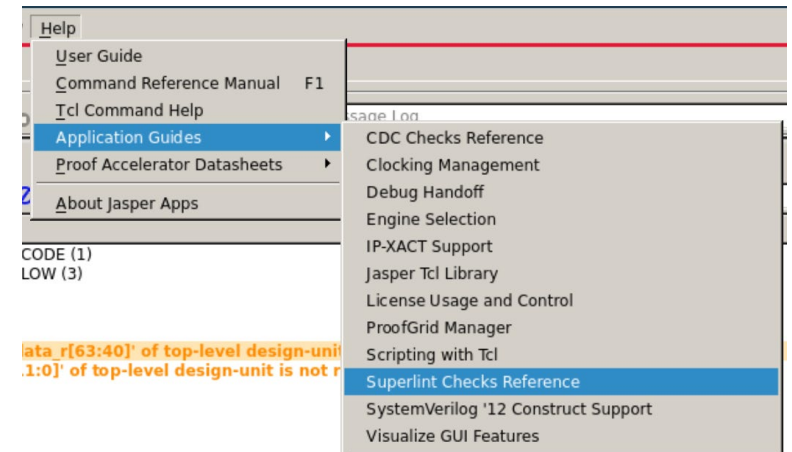
## LINT Categories (2/3)

- SYNTHESIS
  - Checks for constructs that are not synthesizable, for example, the Initial statement to initialize the signal in Verilog code can result in unpredictable synthesis behavior
- STRUCTURAL
  - Checks for design structures that can cause functional or downstream tool issues, for example, Flip-Flops missing resets
- RACES
  - Checks for simulation race condition scenarios. Race conditions occur when two events (with event order dependent code) take place at the same simulation time. For example, read and write on the same register in different always blocks



## LINT Categories (3/3)

- CONNECTIVITY
  - Checks for the connectivity path provided with the `config_rtlDs –connectivity` command. For example, mandatory connections between two nodes in the design
- BLACKBOX
  - Checks for blackbox related scenarios while elaborating the design. For example, explicit blackboxing of module/instance due to the `-bbox_m/-bbox_i` options passed to the `elaborate` command
- For more information, please refer to “Superlint Checks Reference”



## Auto-Formal Categories (1/2)

- AUTO\_FORMAL\_OVERFLOW
  - Overflow in assignments, expressions, divide by zero scenarios and shift operations
- AUTO\_FORMAL\_BUS
  - Bus contention and floating
- AUTO\_FORMAL\_CASE
  - Priority/Unique and default case reachability
- AUTO\_FORMAL\_COMBO\_LOOP
  - Detection of combo loops
- AUTO\_FORMAL\_DEAD\_CODE
  - RTL code block reachability



## Auto-Formal Categories (2/2)

- AUTO\_FORMAL\_FSM\_DEADLOCK\_LIVELOCK
  - FSM deadlock (there is no outgoing path) and FSM livelock (there is no path back to initial state)
- AUTO\_FORMAL\_FSM\_REACHABILITY
  - Unreachable FSM transitions
- AUTO\_FORMAL\_OUT\_OF\_BOUND\_INDEXING
  - Index out of range
- AUTO\_FORMAL\_SIGNALS
  - Stuck-at, signal deadlock, signal not toggled
- AUTO\_FORMAL\_X\_ASSIGNMENT
  - A reachable X-assignment was found



## Basic Lint / Auto-Formal Execution Steps

1. Configure Rules
2. Analyze and Elaborate RTL
3. Design Configuration (Auto Formal Only)
4. Run Checks
5. Analysis and Debug
6. Create Waivers
7. Generate Reports





## Configure Rules (1/2)

- Rules file contains the list of all LINT rules
  - `lint_rule.def`
- Customizations
  - Category names
    - Rules included in each category
    - Enable or disable a category
  - Severity
  - Short message
  - Rule name
  - Specific parameter for a rule, for example, pattern for naming convention rules.



## Configure Rules (2/2)

- You can edit the file (lint\_rule.def) to adjust lint and auto-formal configuration

Category name

```
category SYNTHESIS
{
  MOD_NR_EVRP {severity=Error} {msg="%s %s contains event specification which cannot be synthesized"}
  MOD_NR_FKJN {severity=Error} {msg="%s %s contains non-synthesizable fork-join constructs"}
  MOD_NR_SPFY {severity=Error} {msg="The module '%s' contains non-synthesizable specify block"}
```

Rule name

Severity

Short Message



## Analyze and Elaborate RTL

- `% analyze -sv -f 01_RTL/design.f`
- `% elaborate -top smc_veneer ${DESIGN}`



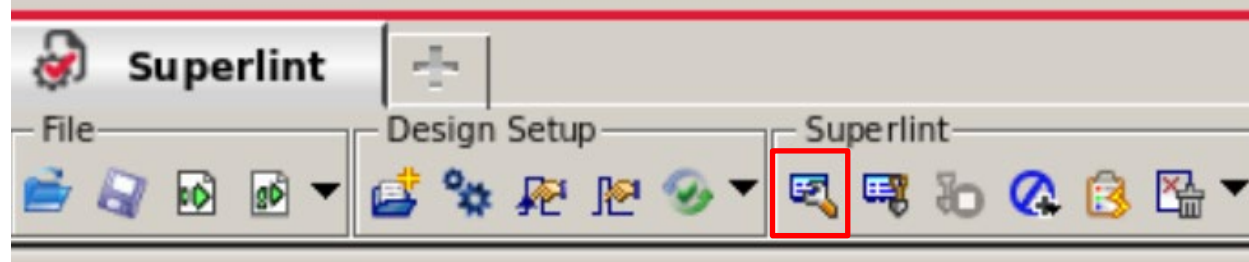
## Design Configuration (Auto Formal Only)

- Clock and reset definition
  - `clock -infer |<specify_clock/s> : Clock Definition`
  - `reset <specify_reset_signals> : Reset Definition`
- Signal configuration required to configure the environment
  - `check_superlint -signal ( -constant {{signal_name value}+}...`
  - `assume -env {...}`



## Run Checks

- `% check_superlint -extract`
- GUI



# Analysis and Debug

Violation Tree

The screenshot displays the Cadence SuperLint tool interface. The top window shows the 'Violation Messages View' with a tree structure of violations. The middle window shows the 'Source Code' for a file named 'EXP\_NR\_MXSU\_130'. The bottom window shows the 'Waiver List' with a table of waivers.

**Violation Tree**

- Domain: LINT (131)
  - Category: STRUCTURAL (2)
    - Tag: MOD\_NO\_IPRG (2)
      - "Input port 'inf.C data r[63:40]' of top-level design-unit is not registered" INF.vsv 65
      - "Input port 'inf.D[11:0]' of top-level design-unit is not registered" INF.vsv 64
    - Category: CODINGSTYLE (128)
      - Tag: EXP\_NR\_MXSU (65)
        - "Expression in design-unit 'BEV' has both signed '360' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 227
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 228
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 754
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 757
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 764
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.milk' expr..." BEV.vsv 765
        - "Expression in design-unit 'BEV' has both signed '540' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 768
        - "Expression in design-unit 'BEV' has both signed '180' and unsigned 'bev\_bal.milk' expr..." BEV.vsv 769
        - "Expression in design-unit 'BEV' has both signed '360' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 772
        - "Expression in design-unit 'BEV' has both signed '120' and unsigned 'bev\_bal.milk' expr..." BEV.vsv 773
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 776
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 777
        - "Expression in design-unit 'BEV' has both signed '360' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 778
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 779
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 780
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 781
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 782
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 783
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 784
        - "Expression in design-unit 'BEV' has both signed '360' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 785
        - "Expression in design-unit 'BEV' has both signed '120' and unsigned 'bev\_bal.milk' expr..." BEV.vsv 786
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 787
        - "Expression in design-unit 'BEV' has both signed '240' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 788
        - "Expression in design-unit 'BEV' has both signed '360' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 789
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.black tea - 180'" BEV.vsv 790
        - "Expression in design-unit 'BEV' has both signed '480' and unsigned 'bev\_bal.pineapple' expr..." BEV.vsv 791
        - "Expression in design-unit 'BEV' has both signed '720' and unsigned 'bev\_bal.pineapple' expr..." BEV.vsv 792

**Source Code**

```

769      bev_bal.milk <= bev_bal.milk - 180;
770    end
771    S: begin
772      bev_bal.black tea <= bev_bal.black tea - 360;
773      bev_bal.milk <= bev_bal.milk - 120;
774    end
775  endcase
776  end
777  Extra_Milk_Tea: begin
778    case(bev_size)
779    L: begin
780      bev_bal.black tea <= bev_bal.black tea - 480;
781      bev_bal.milk <= bev_bal.milk - 480;
782    end
783    M: begin
784      bev_bal.black tea <= bev_bal.black tea - 360;
785      bev_bal.milk <= bev_bal.milk - 360;
786    end
787    S: begin
788      bev_bal.black tea <= bev_bal.black tea - 240;
789      bev_bal.milk <= bev_bal.milk - 240;
790    end
791  endcase
792  end
  
```

**Waiver List**

Comment	Id	Source	Upr	Tag	Category
test1	1			EXP_NR_MXSU	*

**Console**

```

To run "analyze" after elaborating the design, run "clear -all" and "set_elaborate_single_run_mode off" before starting the setup.
NOTE: Disabling this mode can cause larger memory consumption.

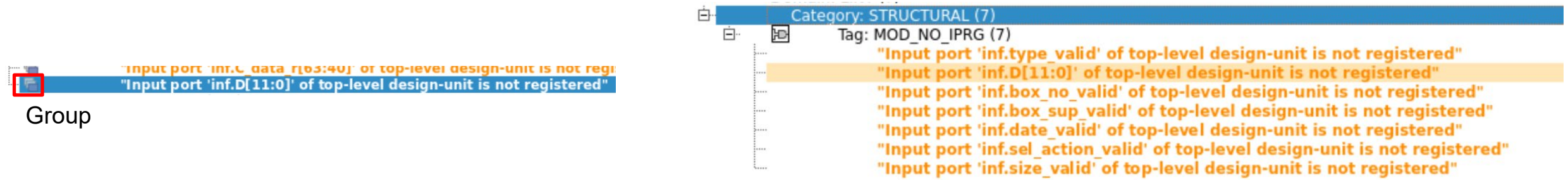
[embedded]> % check superlint -extract
INFO (ISL018): Started extraction of structural checks
INFO (ISL018): Started building clock tree
INFO (ISL018): Finished building clock tree
INFO (ISL018): Started building reset tree
INFO (ISL018): Finished building reset tree
INFO (ISL018): Violation Count: Errors = 12 Warnings = 157 Info = 0
INFO (ISL009): Started detection of ASG_IS_XRCH, ASG_AR_OVFL, CAS_NO_UNIQ, CAS_NO_PRIO, BLK_NO_RCHB, ARY_IS_OOBI, EXP_AR_OVFL, ASG_IS_OVFL, EXP_IS_OVFL, SHF_IS_OVFL, SHF_IS_AB50, VAR_IS_CTOL checks
INFO (ISL014): Started extracting properties for ASG_IS_XRCH, ASG_AR_OVFL, CAS_NO_UNIQ, CAS_NO_PRIO, BLK_NO_RCHB, ARY_IS_OOBI, EXP_AR_OVFL, ASG_IS_OVFL, EXP_IS_OVFL, SHF_IS_OVFL, SHF_IS_AB50, VAR_IS_CTOL checks
INFO (ISL015): Extracted 344 properties of ASG_IS_XRCH, ASG_AR_OVFL, CAS_NO_UNIQ, CAS_NO_PRIO, BLK_NO_RCHB, ARY_IS_OOBI, EXP_AR_OVFL, ASG_IS_OVFL, EXP_IS_OVFL, SHF_IS_OVFL, SHF_IS_AB50, VAR_IS_CTOL checks
INFO (ISL009): Started detection of FSM_IS_LVLK, FSM_IS_DOLK, FSM_NO_RCHB, FSM_IS_PLK, FSM_IS_PDLK, FSM_IS_NLLK, FSM_IS_NDLK checks
INFO (ISL014): Started extracting properties for FSM_IS_LVLK, FSM_IS_DOLK, FSM_NO_RCHB, FSM_IS_PLK, FSM_IS_PDLK, FSM_IS_NLLK, FSM_IS_NDLK checks
INFO (ISL015): Extracted 134 properties of FSM_IS_LVLK, FSM_IS_DOLK, FSM_NO_RCHB, FSM_IS_PLK, FSM_IS_PDLK, FSM_IS_NLLK, FSM_IS_NDLK checks
INFO (ISL014): Started extracting properties for SIG_IS_STCK checks
INFO (ISL015): Extracted 18 properties of SIG_IS_STCK checks
INFO (ISL009): Started detection of BUS_IS_CONT, BUS_IS_FLOT, SIG_IS_MLAS checks
INFO (ISL014): Started extracting properties for BUS_IS_CONT, BUS_IS_FLOT, SIG_IS_MLAS checks
INFO (ISL009): Started detection of MOD_IS_FOMB checks
INFO (ISL014): Started extracting properties for MOD_IS_FOMB checks
INFO (ISL015): Extracted 0 properties of MOD_IS_FOMB checks
INFO (ISL020): Adding automatic assumptions to task "-csl_AUTO_FORMAL_FSM_DEADLOCK_LIVELOCK_POTENTIAL_FREE".
665
[embedded]> % check superlint -show schematic -id 212 -constants values
[embedded]> % check superlint -waiver -add -id (130) -comment test1 -silent
1
[embedded]> %
  
```

Source Code

Waiver List



## Analysis and Debug – Grouping Feature (Lint)



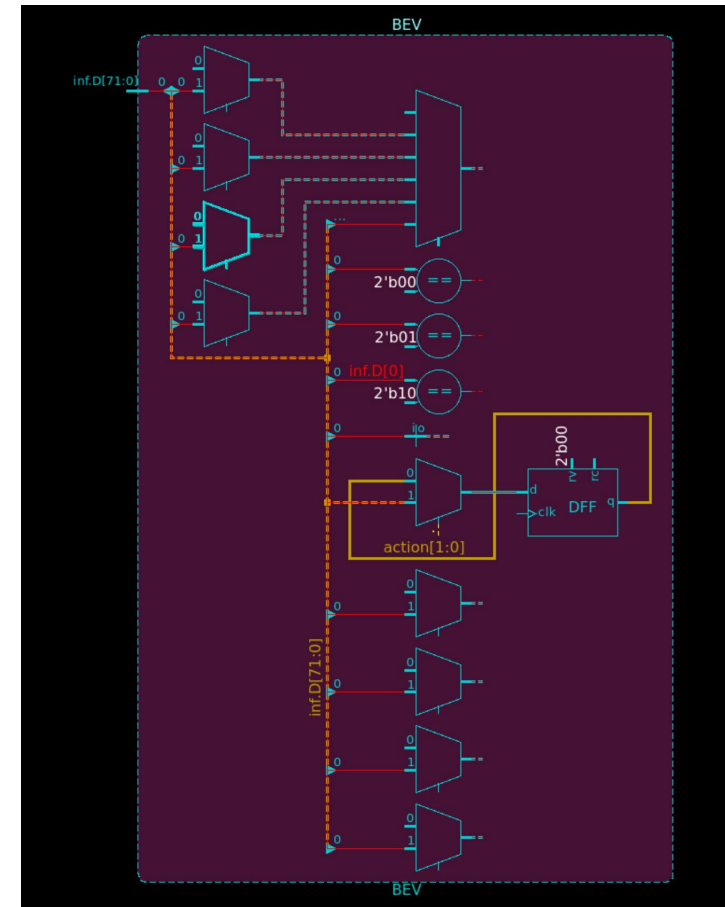
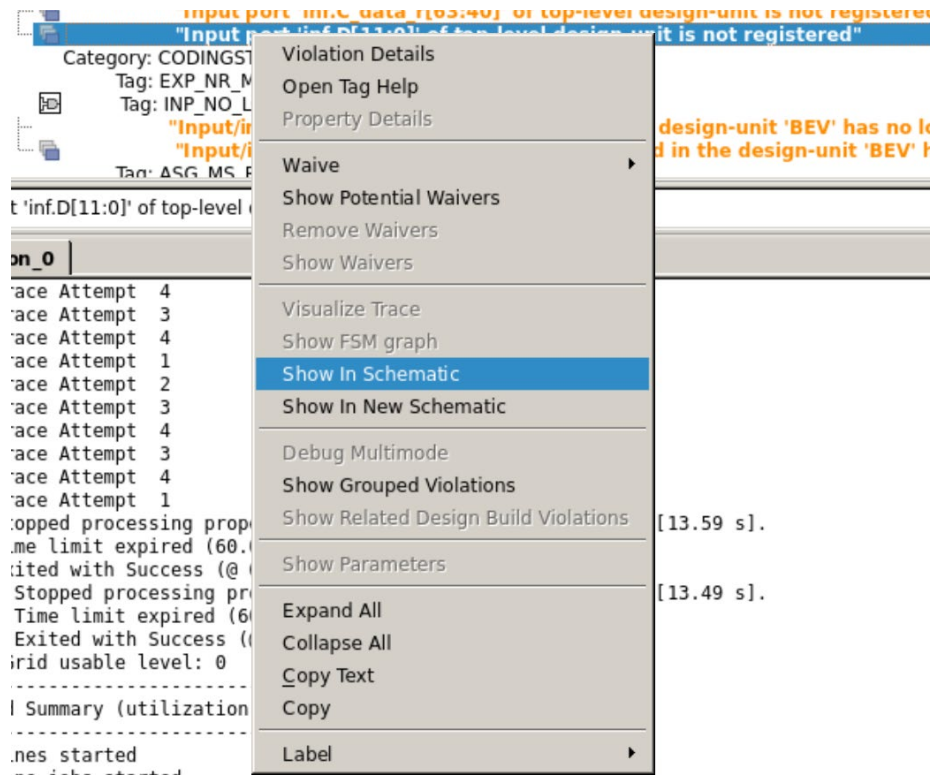
The image shows a screenshot of a linting tool interface. On the left, a small icon of a person is highlighted with a red box, and the word "Group" is written below it. The main area displays a list of linting errors. The first error is highlighted in blue and reads: "Input port 'inf.C\_data\_r[63:40]' of top-level design-unit is not registered". The second error is highlighted in orange and reads: "Input port 'inf.D[11:0]' of top-level design-unit is not registered". To the right, a detailed view of the selected error is shown, listing seven input ports that are not registered: 'inf.type\_valid', 'inf.D[11:0]', 'inf.box\_no\_valid', 'inf.box\_sup\_valid', 'inf.date\_valid', 'inf.sel\_action\_valid', and 'inf.size\_valid'. The category is listed as "STRUCTURAL (7)" and the tag as "MOD\_NO\_IPRG (7)".

Group

Category: STRUCTURAL (7)  
Tag: MOD\_NO\_IPRG (7)

- "Input port 'inf.type\_valid' of top-level design-unit is not registered"
- "Input port 'inf.D[11:0]' of top-level design-unit is not registered"
- "Input port 'inf.box\_no\_valid' of top-level design-unit is not registered"
- "Input port 'inf.box\_sup\_valid' of top-level design-unit is not registered"
- "Input port 'inf.date\_valid' of top-level design-unit is not registered"
- "Input port 'inf.sel\_action\_valid' of top-level design-unit is not registered"
- "Input port 'inf.size\_valid' of top-level design-unit is not registered"

# Analysis and Debug - Using Schematic (Lint)





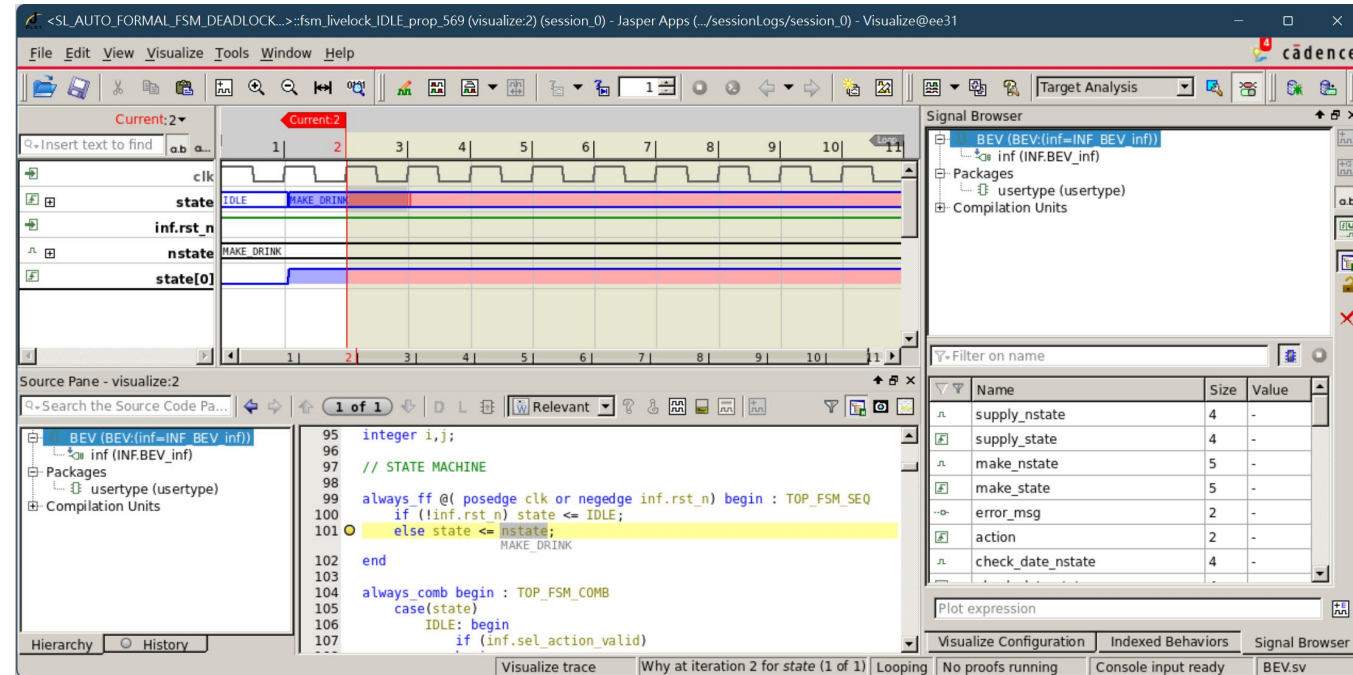
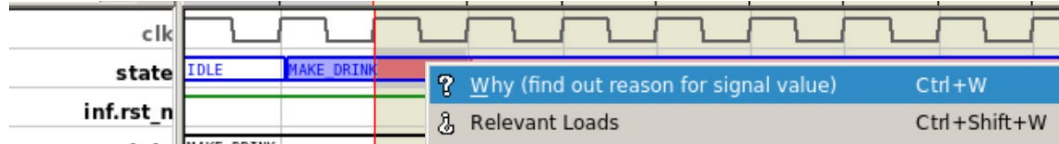
# Analysis and Debug – Visualize Waveform (Auto-Formal) (1/2)

The screenshot displays the Cadence Jasper tool interface for analyzing and debugging a waveform. On the left, a list of violations is shown, including 'Potential Livelock condition found in the FSM state', 'Potential Deadlock condition', and 'The blocking statement'. A context menu is open over the violations, offering options like 'Violation Details', 'Open Tag Help', 'Property Details', 'Waive', 'Show Potential Waivers', 'Remove Waivers', 'Show Waivers', 'Visualize Trace', 'Show FSM graph', and 'Show In Schematic'. The 'Visualize Trace' option is highlighted. The central pane shows a waveform visualization with signals like 'clk', 'state', 'inf.rst\_n', 'nstate', and 'state[0]'. The 'state' signal is selected, and the waveform shows a transition from 'IDLE' to 'MAKE DRINK' at time step 2. The right pane shows the 'Signal Browser' with a list of signals and their values. The 'BEV (BEV:(inf=INF BEV inf))' signal is selected, and its value is 'inf (INF.BEV inf)'. The 'Signal Browser' table is as follows:

Name	Size	Value
supply_nstate	4	-
supply_state	4	-
make_nstate	5	-
make_state	5	-
error_msg	2	-
action	2	-
check_date_nstate	4	-

The bottom status bar shows 'Selected: state', 'Visualize trace', 'Why at iteration 2 for state[0] (1 of 1)', 'Looping', 'No proofs running', 'Console input ready', and 'BEV.sv'.

# Analysis and Debug – Visualize Waveform (Auto-Formal) (2/2)



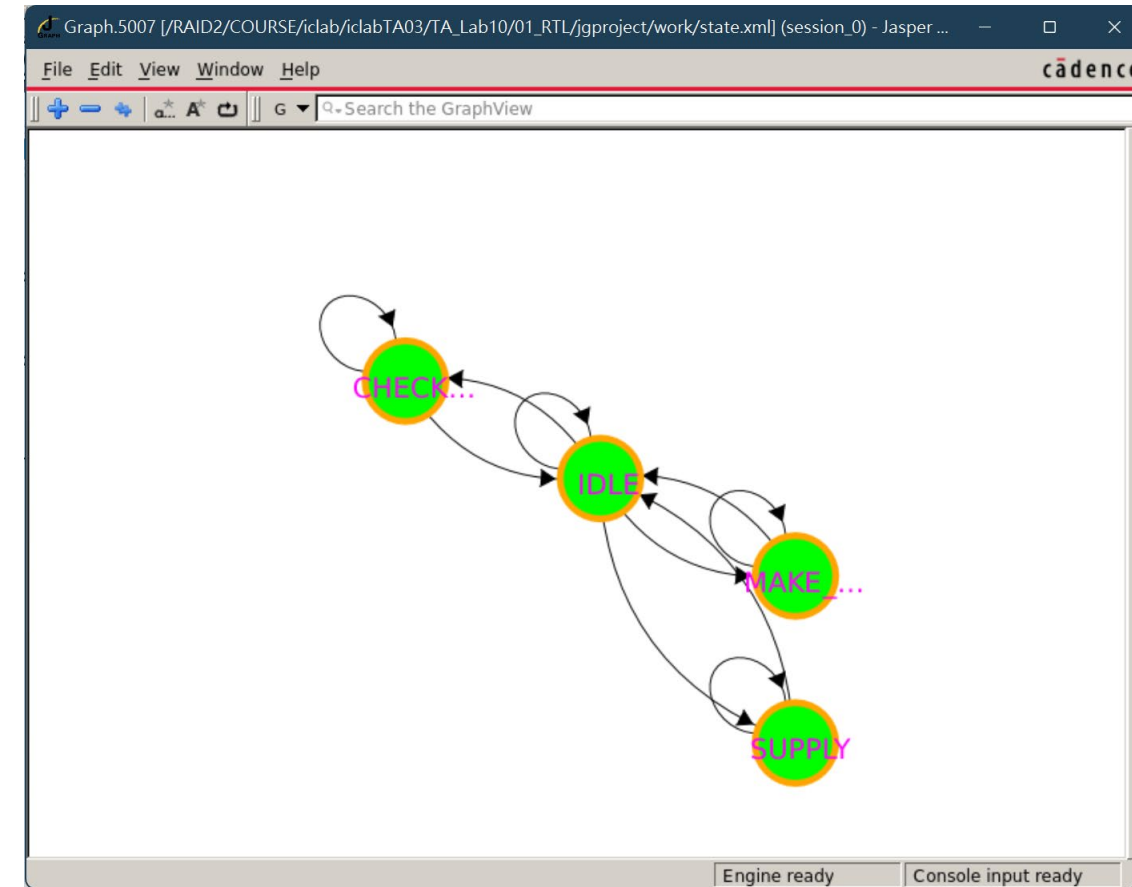
# Analysis and Debug – Using FSM Graph

The screenshot shows the Cadence Jasper tool interface. On the left, a list of violations is displayed, including:

- Tag: FSM\_IS\_PLLK (1)
  - \*W, "Potential Livelock condition found in the FSM 'state'"
- Tag: FSM\_IS\_PDLK (4)
  - \*W, "Potential Deadlock condition found for state 'IDLE' i"
  - \*W, "Potential Deadlock condition found for state 'IDLE M"
  - \*W, "Potential Deadlock condition found for state 'IDLE S"
  - \*W, "Potential Deadlock condition found for state 'IDLE C"
- Tag: FSM\_IS\_NLLK (3)
  - \*I, "FSM 'check\_date\_state' does not have any Livelock co"
  - \*I, "FSM 'make\_state' does not have any Livelock conditio"
  - \*I, "FSM 'supply\_state' does not have any Livelock conditi"
- Tag: FSM\_IS\_NDLK (35)
  - Category: AUTO\_FORMAL\_DEAD\_CODE (1)
  - Tag: BLK\_NO\_RCHB (1)
  - \*E, "The blocking statement 'make\_nstate = 5'b00000 ;' is"
  - Category: AUTO\_FORMAL\_OVERFLOW (3)
  - Domain: LINT (131)

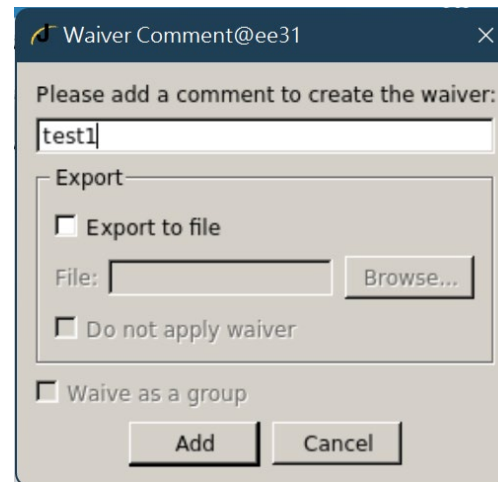
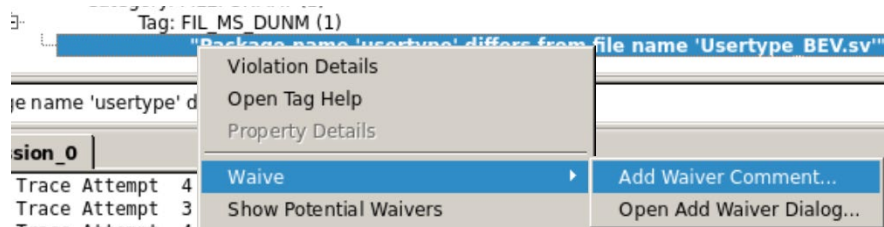
On the right, a context menu is open over the violations, showing options:

- Violation Details
- Open Tag Help
- Property Details
- Waive
- Show Potential Waivers
- Remove Waivers
- Show Waivers
- Visualize Trace
- Show FSM graph
- Show In Schematic
- Show In New Schematic



## Create Waivers

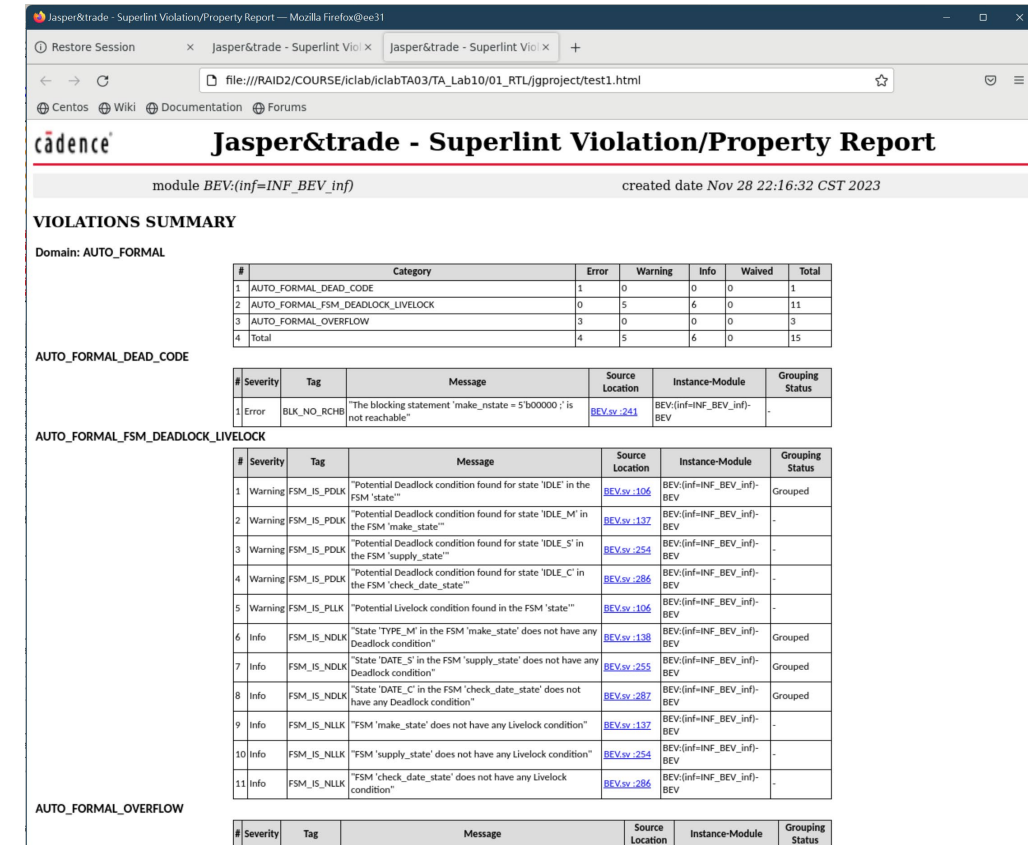
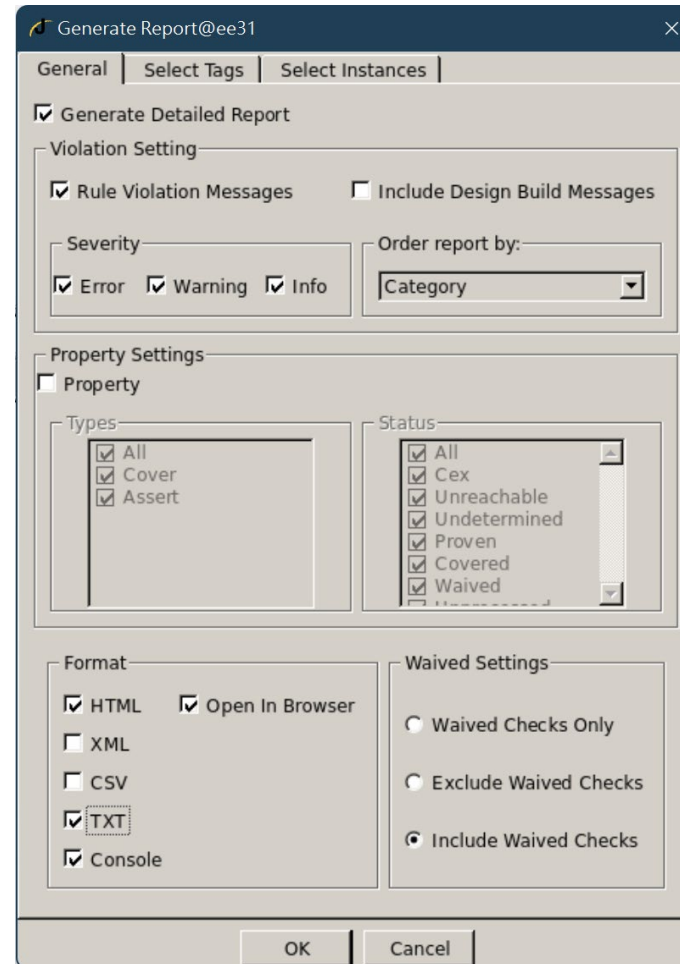
- Some Warning/Error may can be ignored
- Will be removed from the violation messages view tree



A screenshot of the 'Waiver List' table. The table has a title bar 'Waiver List' and a close button. The table has columns: Comment, Id, Source, Uf, Tag, and Category. The table contains one row with the following data: Comment: test1, Id: 1, Source: (empty), Uf: (empty), Tag: FIL\_MS\_DUNM, Category: \*.

Comment	Id	Source	Uf	Tag	Category
test1	1			FIL_MS_DUNM	*

# Generate Report



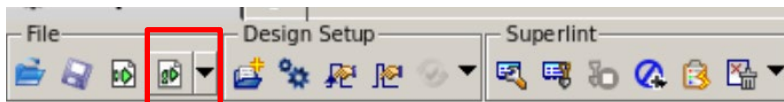
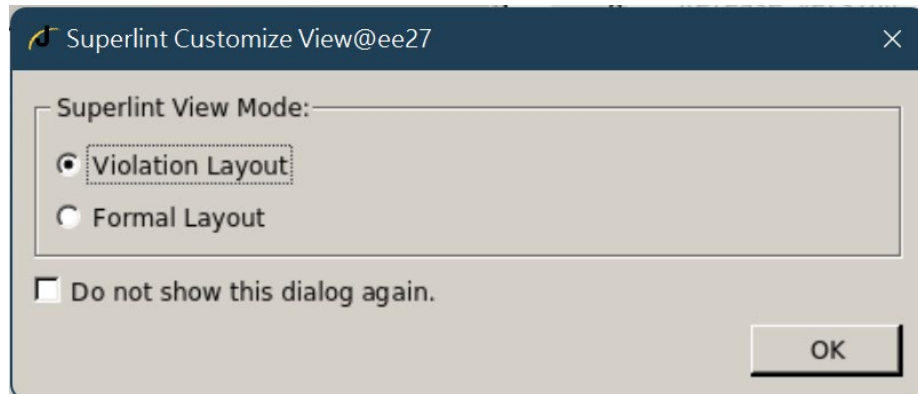
## How to use

- The file we need
  - `jg_superlint.tcl`
  - `lint_rule.def`
  - `design.f`
    - Put all the design file name into this file
- `./06_superlint`

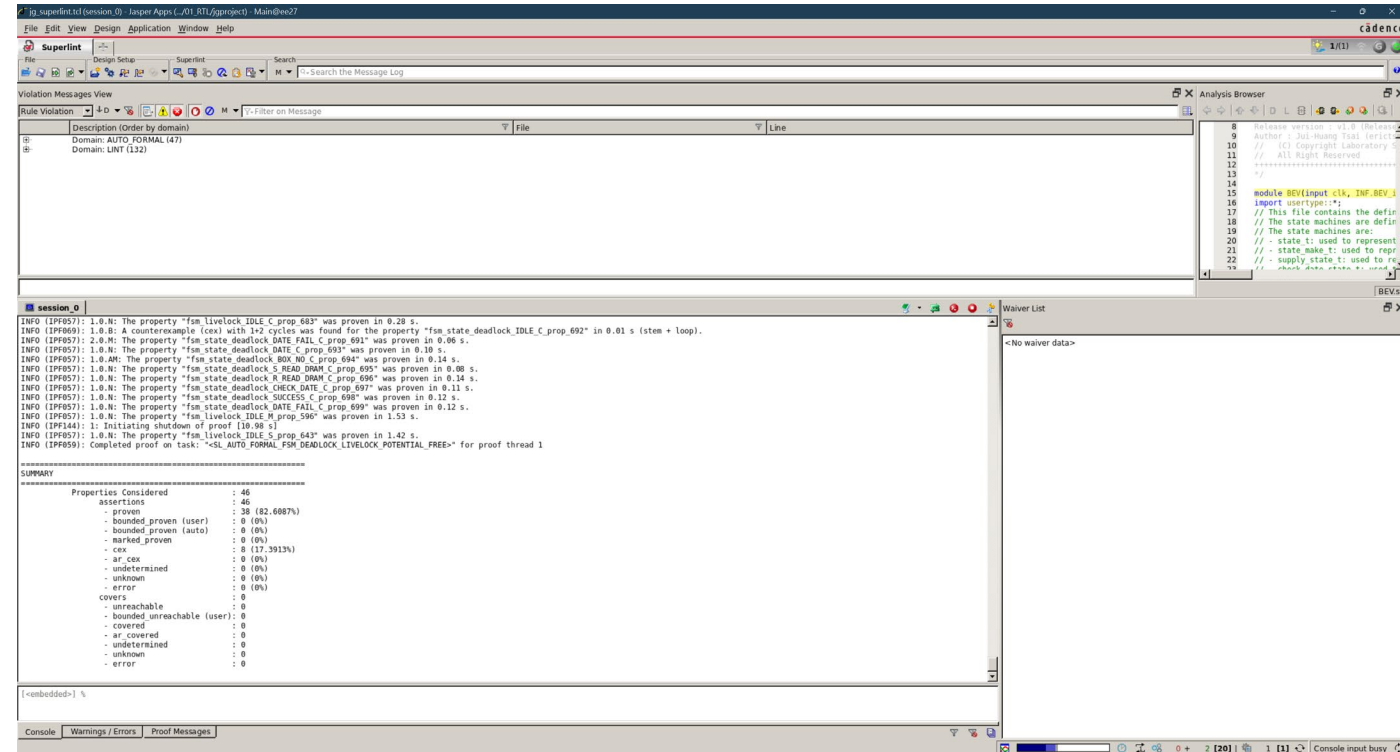




# Startup



This bottom can reload whole design again



## Reference

- rak\_jasper\_superlint\_auto\_formal\_lab\_instructions
- rak\_jasper\_superlint\_auto\_formal\_overview
- rak\_jasper\_superlint\_lint\_lab\_instructions
- rak\_jasper\_superlint\_lint
- 2023 Autumn ICLAB Lab09/Lab10

