NCTU-EE IC LAB – Fall 2022

Lab13 Check List

Self-Verify APR Result

./02_check under 09_SUMBIT to download your Lab13_iclabXXX.tar file back
Create a new directory, enter the directory and decompress the tar file.
Enter the decompressed directory.

1. Invoke innonus and restore CHIP_iclabXXX.inn
   (Remember to create a new folder in case you overwrite previous design)

2. Explore the core size and die size, also verify if the core to IO boundary should be larger than 100.

3. Verifying if the IO Filler and the corner pad is added.

4. Verify the floorplan and powerplan constraints:
   a. Power ring: wire group, interleaving, and at least 4 pairs, width 9.

5. Post-Route Timing analysis with non-negative slacks, 0 DRVs, core filler added.

6. Verifying Geometry and Connectivity after adding core filler cells.

7. Latency cycles in post simulation should be the same as gate level simulation.
   (Clock period : 20ns / Execution cycles : 32000 cycles)