ICLAB 2023-Fall Lab03 Note

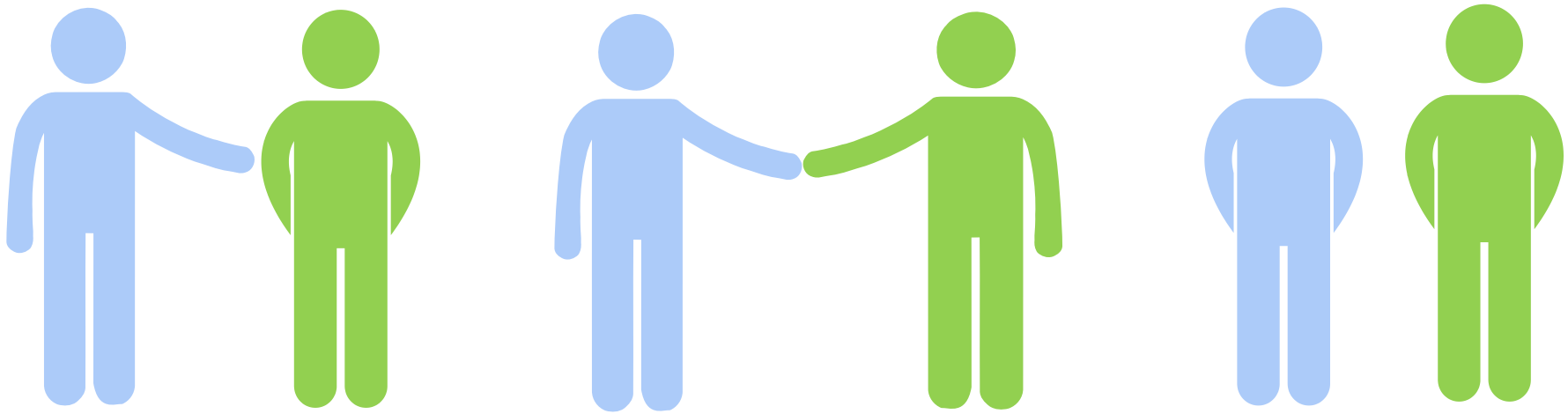
Presenter: Ting-Yu Chang

Advisor: Chen-Yi Lee

AXI Handshake Process

Handshake Process Scenario 1

- **Slave: Valid** **Master: Ready**



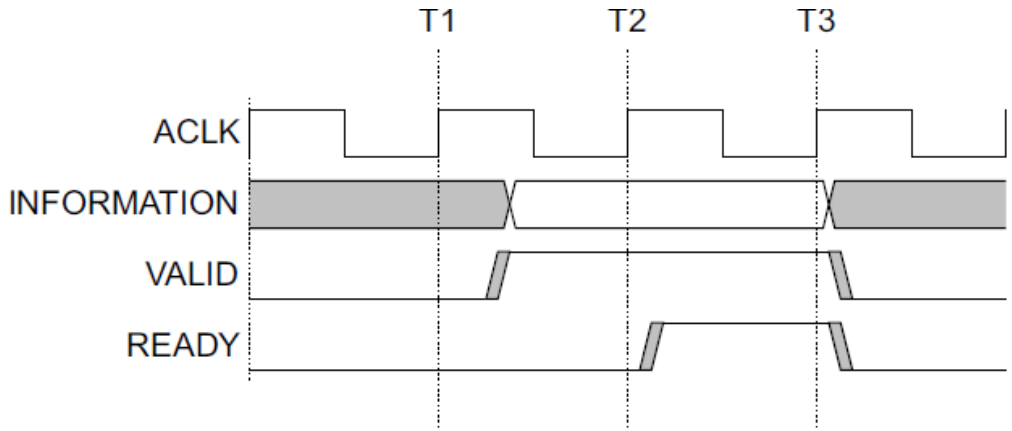
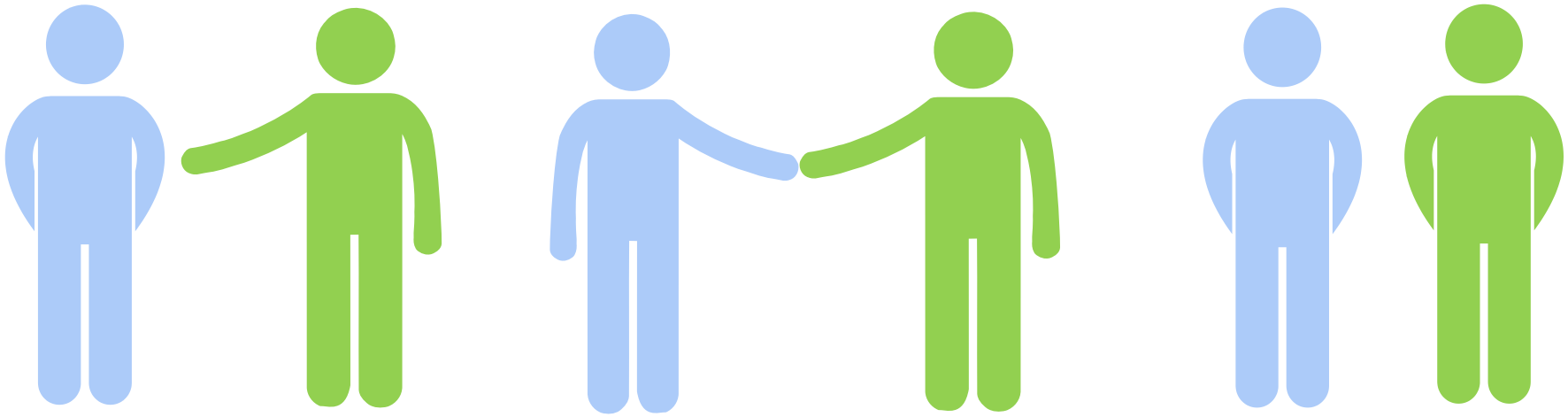


Figure A3-2 VALID before READY handshake

Handshake Process Scenario 2

- **Slave: Valid** **Master: Ready**



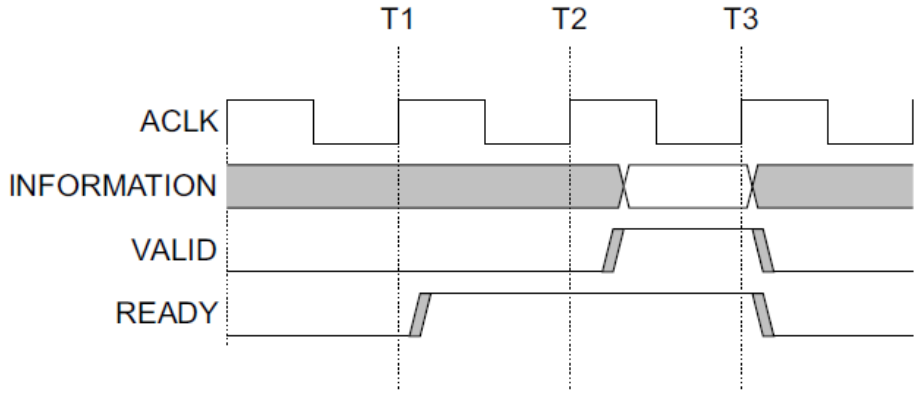
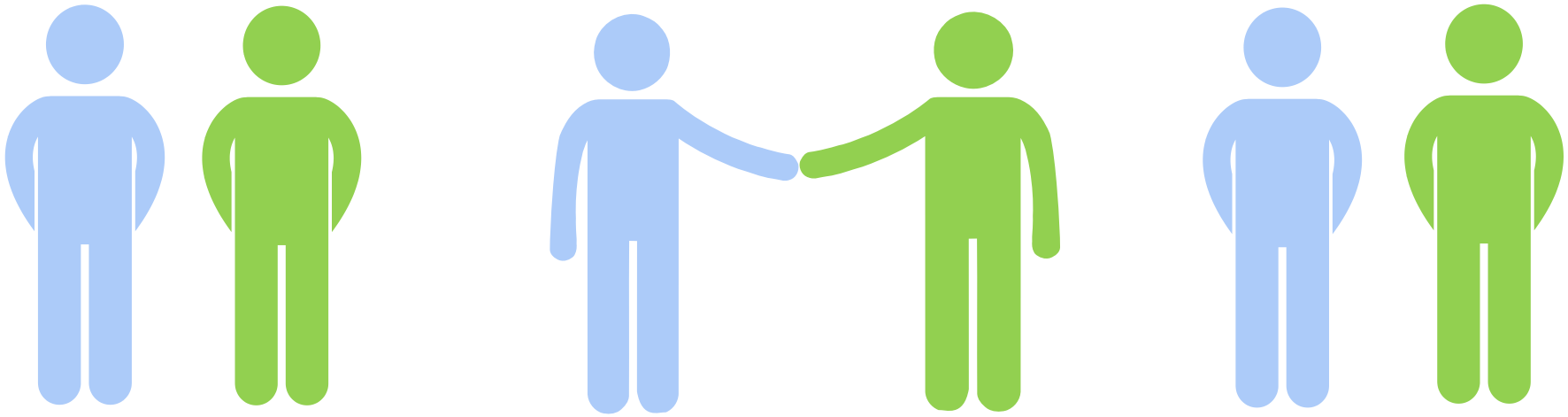


Figure A3-3 READY before VALID handshake

Handshake Process Scenario 3

- **Slave: Valid** **Master: Ready**



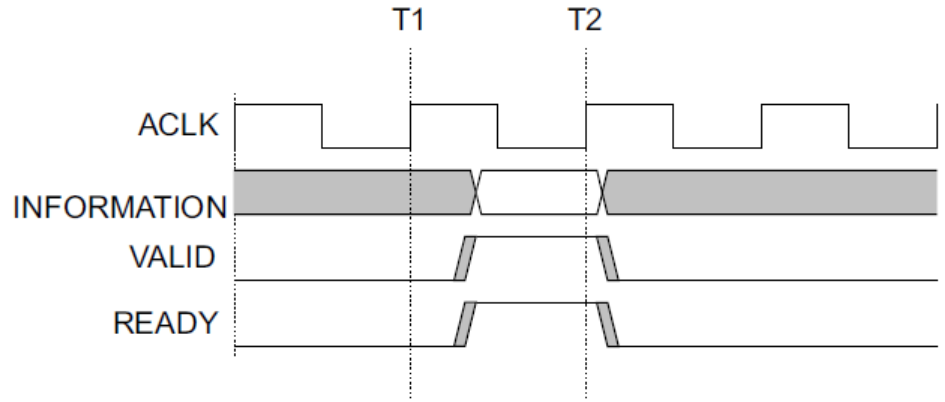


Figure A3-4 VALID with READY handshake

Handshake Process

- the VALID signal of one AXI component must not be dependent on the READY signal of the other component in the transaction.
- the READY signal can wait for assertion of the VALID signal.

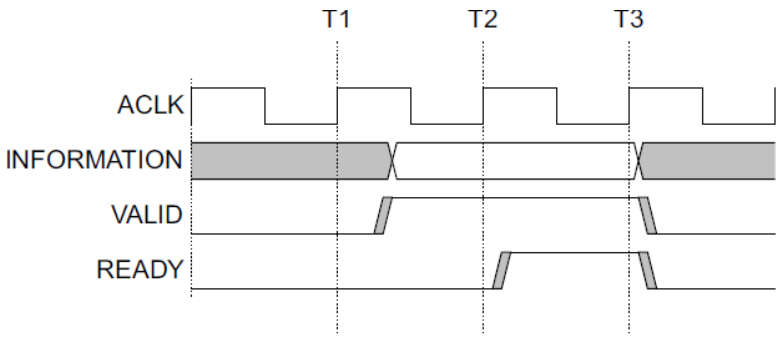


Figure A3-2 VALID before READY handshake

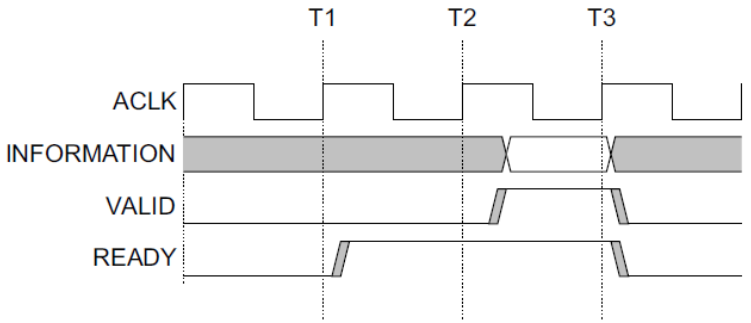


Figure A3-3 READY before VALID handshake

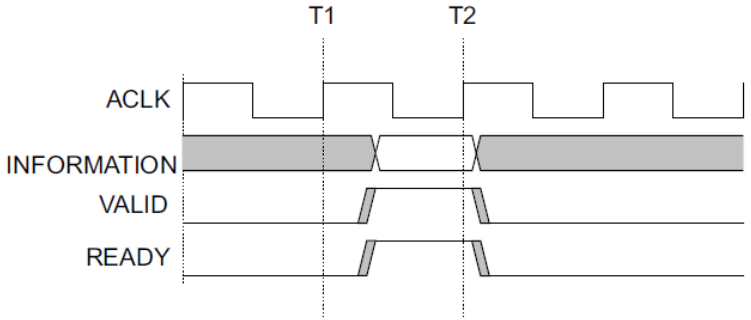


Figure A3-4 VALID with READY handshake

AXI4-Lite Introduction

AXI 4 Basic Transaction

Read Transaction

- Read Address Channel
- Read Data Channel

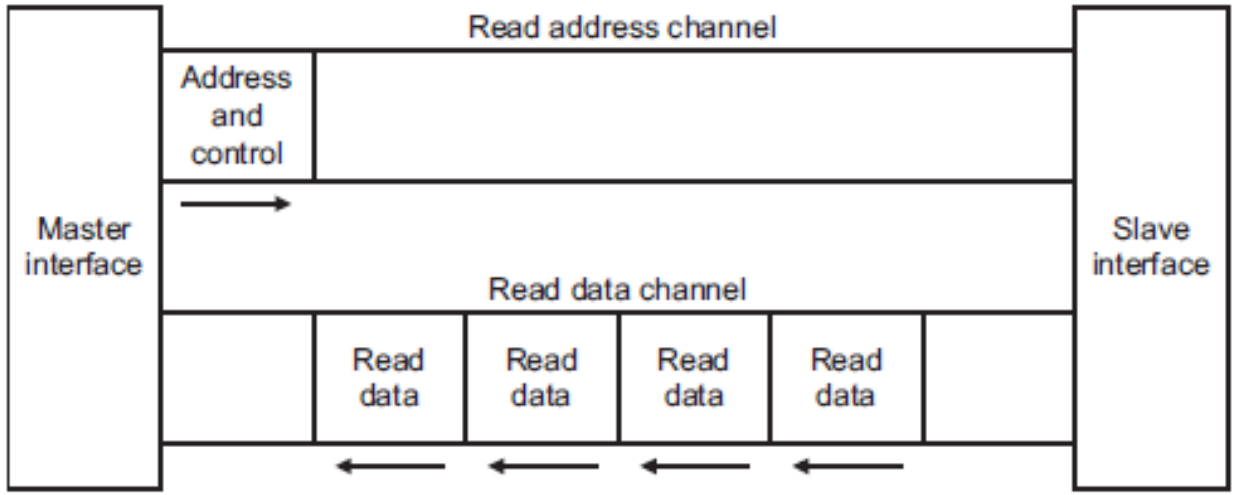


Figure 1-1 Channel architecture of reads

Each channel have valid-ready pair for handshaking process

Ref [2]

AXI 4 Basic Transaction

Write Transaction

- Write Address Channel
- Write Data Channel
- Write Response Channel

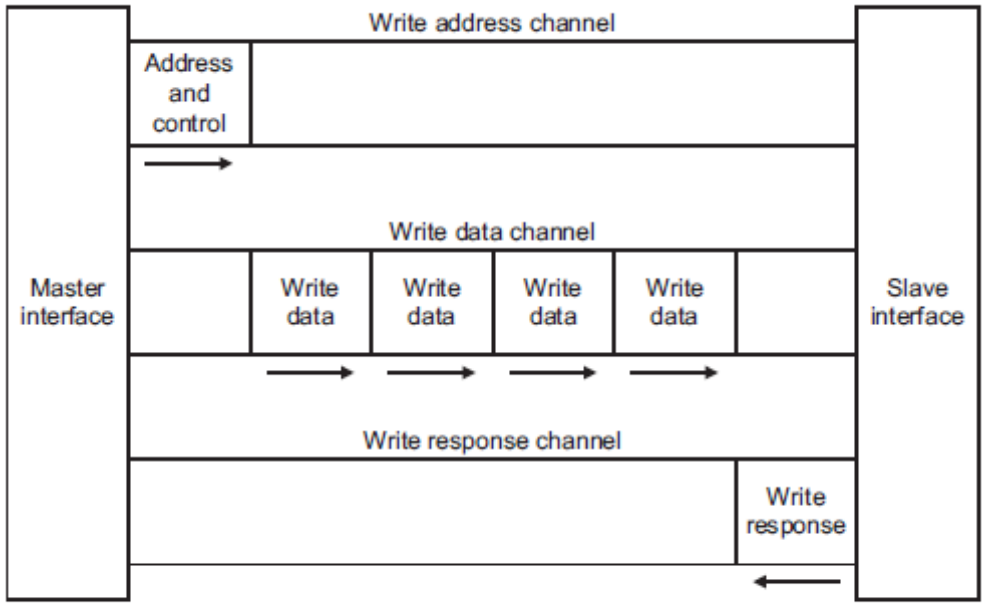


Figure 1-2 Channel architecture of writes

Each channel have valid-ready pair for handshaking process

Ref [2]

Global Signals

Signal	Bit Width	Source	Description
clk	1	Clock source	Global clock signal. All signals are sampled on the **positive** edge of the global clock.
rst_n	1	Reset source	Global reset signal. This signal is active LOW.

Write Address Channel

Signal	Bit Width	Source	Description
AW_ADDR	32	Master	Write address.
AW_VALID	1	Master	Write address valid. This signal indicates that valid write address is available: 1 = address available 0 = address not available. The address remain stable until the address acknowledge signal, **AW_READY**, goes HIGH.
AW_READY	1	Slave	Write address ready. This signal indicates that the slave is ready to accept an address signals: 1 = slave ready 0 = slave not ready.

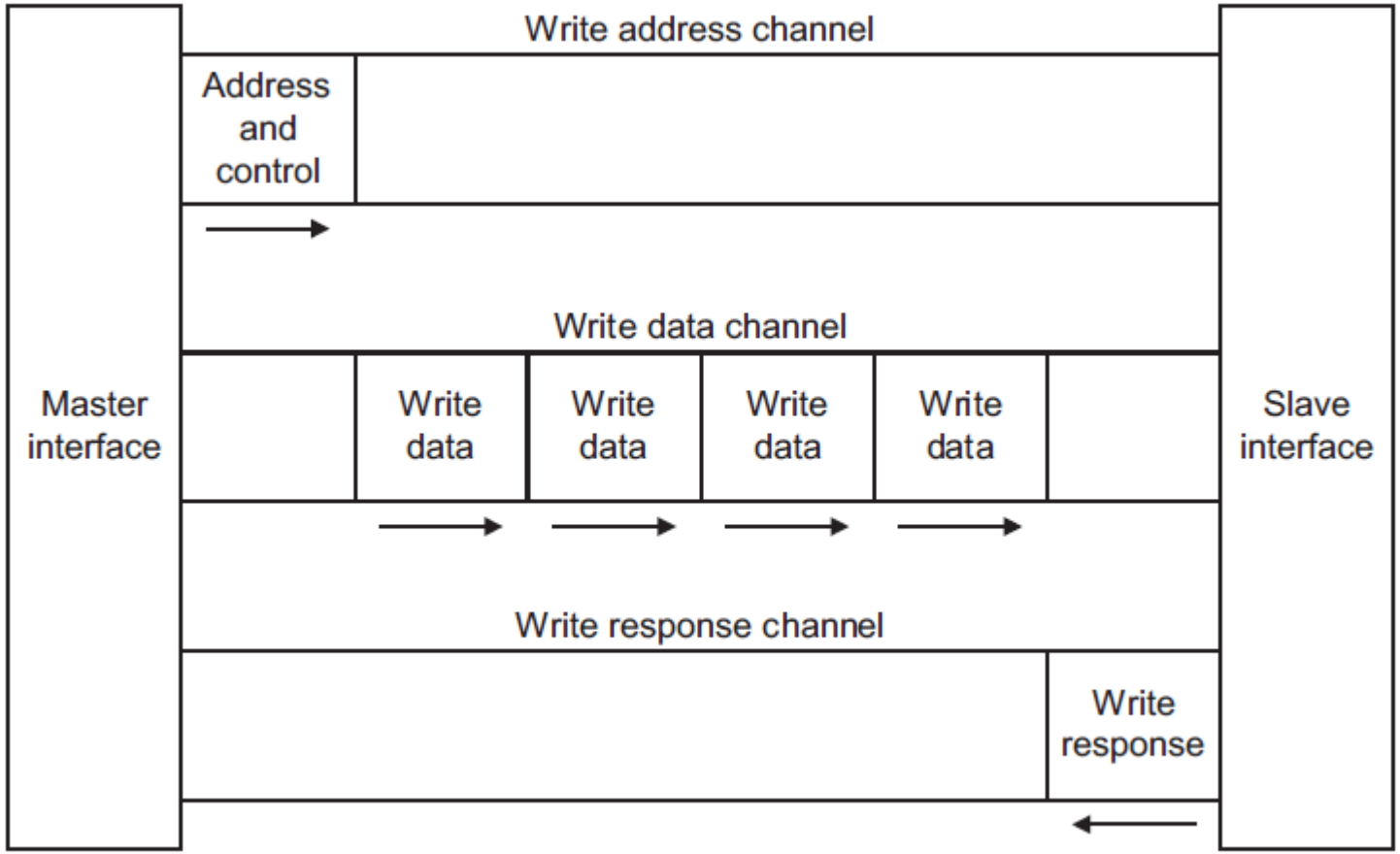
Write Data Channel

Signal	Bit Width	Source	Description
W_DATA	64	Master	Write data bus.
W_VALID	1	Master	Write valid. This signal indicates that valid write data is available: 1 = write data available 0 = write data not available.
W_READY	1	Slave	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready 0 = slave not ready.

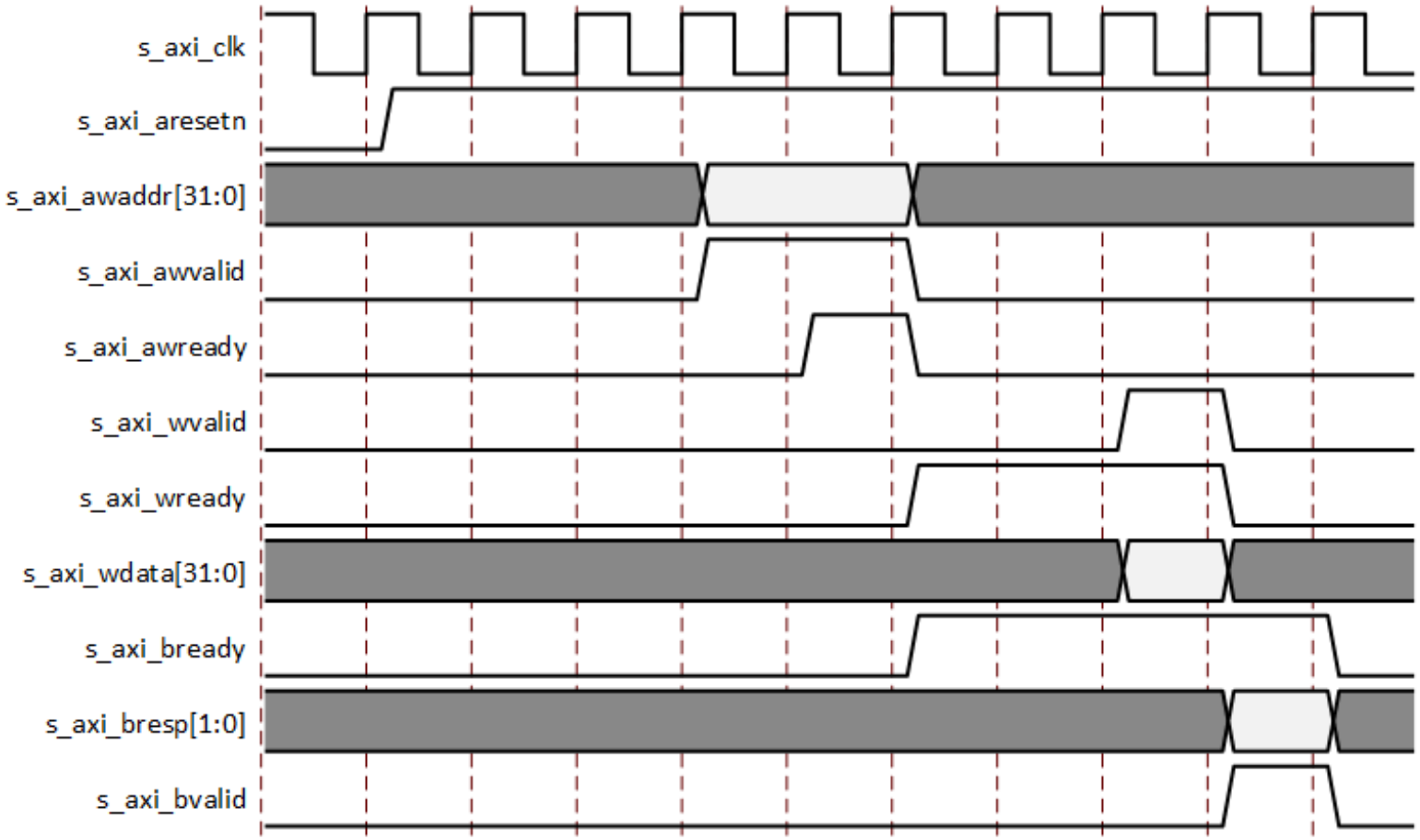
Write Response Channel

Signal	Bit Width	Source	Description
B_RESP	2	Slave	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (In this lab we only issue OKAY(2'b00))
B_VALID	1	Slave	Write response valid. This signal indicates that a valid write response is available: 1 = write response available. 0 = write response not available.
B_READY	1	Master	Response ready. This signal indicates that the master can accept the response information. 1 = master ready. 0 = master not ready.

Write Transaction



Waveform of Write Transaction



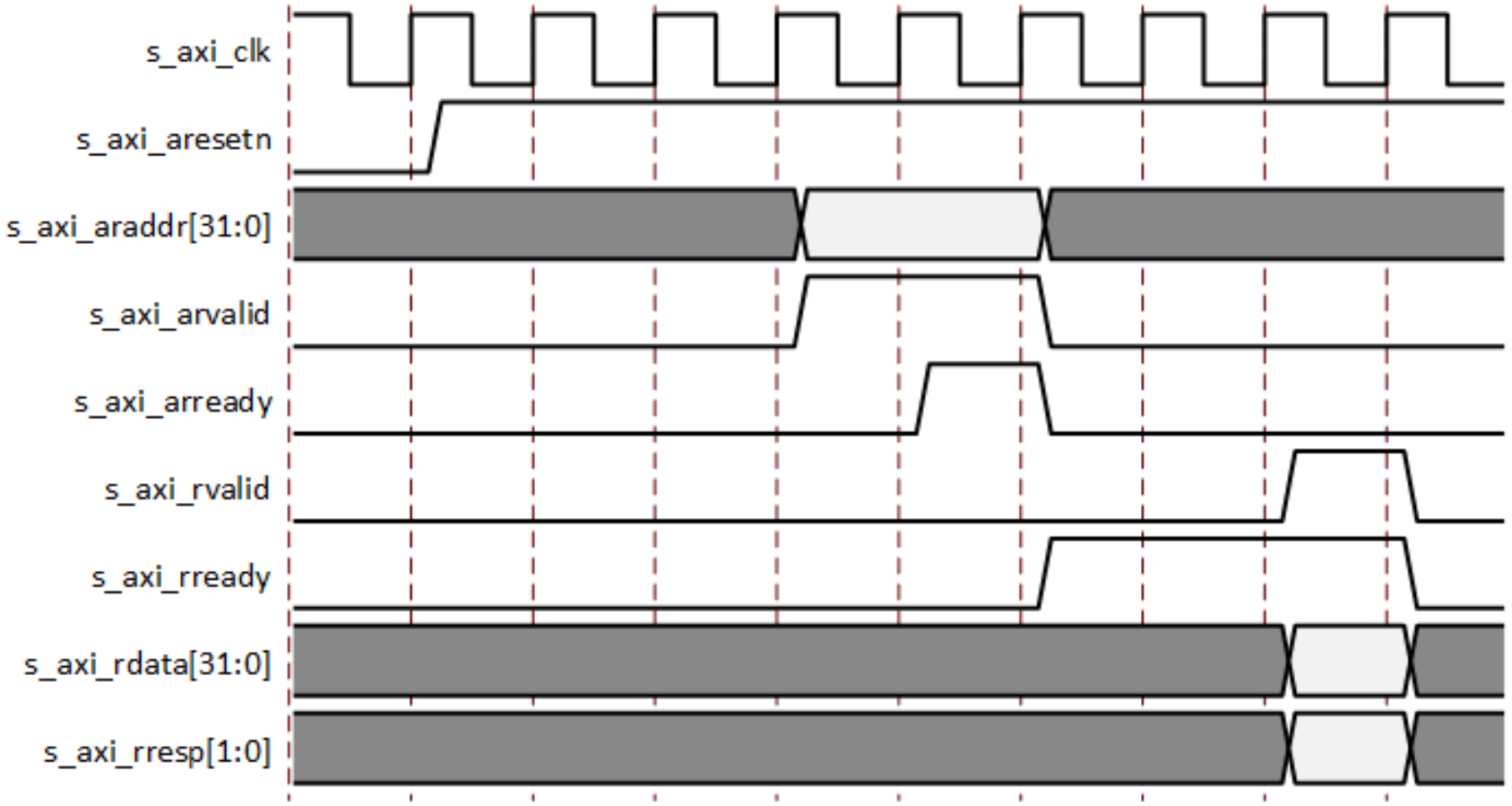
Read Address Channel

Signal	Bit Width	Source	Description
AR_ADDR	32	Master	Read address.
AR_VALID	1	Master	Read address valid. This signal indicates, when HIGH, that the read address is valid and will remain stable until the address acknowledge signal, **AR_READY**, is high. 1 = address and control information valid 0 = address and control information not valid.
AR_READY	1	Slave	Read address ready. This signal indicates that the slave is ready to accept an address signals: 1 = slave ready 0 = slave not ready.

Read Data Channel

Signal	Bit Width	Source	Description
R_DATA	64	Slave	Read data.
R_RESP	2	Slave	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (In this project we only issue OKAY)
R_VALID	1	Slave	Read valid. This signal indicates that the required read data is available, and the read transfer can complete: 1 = read data available 0 = read data not available.
R_READY	1	Master	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready 0 = master not ready.

Read Transaction



SPI Introduction

SD Card Signal

Signal	Bit Width	Source	Description
clk	1	Clock source	Global clock signal. All signals are sampled on the **positive** edge of the global clock.
CS_n	1	Master	Chip Select, active LOW
MISO	1	Slave	Master Input Slave Output. When the data is not transfer, keep HIGH. Serial In Serial Out (SISO) transmission.
MOSI	1	Master	Master Output Slave Input. When the data is not transfer, keep HIGH. Serial In Serial Out (SISO) transmission.

SD Card Read Operation

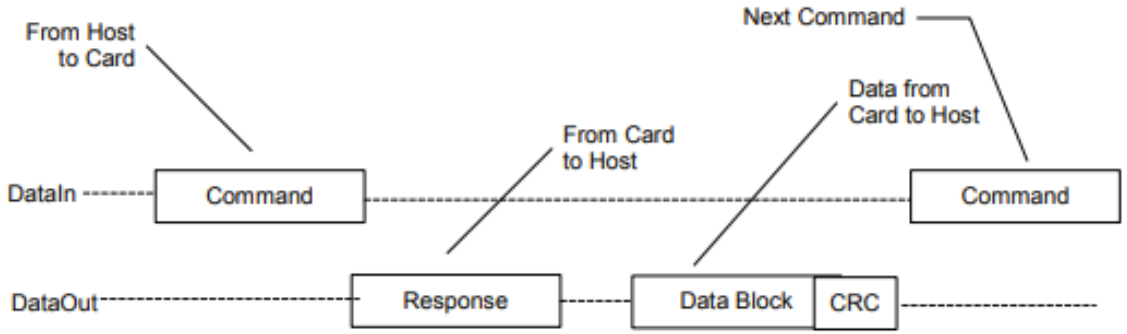
Command (from host)
Start bit + transmission bit = 2'b01
Command: CMD17 = 6'd17
Argument: address
CRC:CRC-7({Start bit, Transmission bit, Command, Argument})
End bit: 1'b1

(wait 0~8 units, units = 8 cycles)

Response (from SD card)
Response: 0x00 (8 bits)

(wait 1~32 units, units = 8 cycles)

Data (from SD card)
Start token: 0xFE (8 bits)
Data block: 64 bits (differ from the original protocol)
CRC: CRC-16-CCITT (Data block)



Command Format

Byte 1				Bytes 2—5		Byte 6	
7	6	5	0	31	0	7	0
0	1	Command		Command Argument		CRC	1

SD Card Write Operation

Command (from host)
Start bit + transmission bit = 2'b01
Command: CMD24 = 6'd24
Argument: address
CRC:CRC-7({Start bit, Transmission bit, Command, Argument})
End bit: 1'b1

(wait 0~8 units, units = 8 cycles)

Response (from SD card)
Response: 0x00 (8 bits)

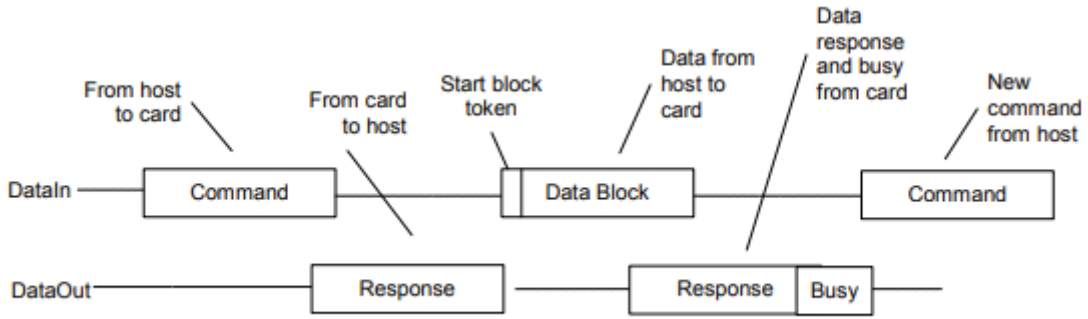
(wait 1~32 units, units = 8 cycles)

Data (from host)
Start token: 0xFE
Data block: 64 bits (differ from the original protocol)
CRC: CRC-16-CCITT (Data block)

(wait 0 units, units = 8 cycles)

Data response (from SD card)
Data_response: 8'b00000101
Busy: keep low until finish write.

(wait 0~32 units, units = 8 cycles)



Command Format

Byte 1				Bytes 2—5		Byte 6	
7	6	5	0	31	0	7	0
0	1	Command		Command Argument		CRC	1