

# **Design Vision™ User Guide**

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**SYNOPSYS®**

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# About This User Guide

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This User Guide is for logic design engineers who have some experience using the Synopsys Design Compiler® or DC Explorer tool and want to use the visualization features of the Design Vision tool for analysis. To use this user guide, you should be familiar with

- Synthesis using Design Compiler or DC Explorer
- VHDL or Verilog HDL
- UNIX or Linux operating system

This preface includes the following sections:

- [New in This Release](#)
- [Related Products, Publications, and Trademarks](#)
- [Conventions](#)
- [Customer Support](#)

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## New in This Release

Information about new features, enhancements, and changes, known limitations, and resolved Synopsys Technical Action Requests (STARs) is available in the Design Vision Release Notes on the SolvNetPlus site.

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## Related Products, Publications, and Trademarks

For additional information about the Design Vision tool, see the documentation on the Synopsys SolvNetPlus support site at the following address:

<https://solvnetplus.synopsys.com>

You might also want to see the documentation for the following related Synopsys products:

- DC Explorer
- Design Compiler
- TestMAX™ DFT and DFTMAX™
- Power Compiler™

## Conventions

The following conventions are used in Synopsys documentation.

Convention	Description
Courier	Indicates syntax, such as <code>write_file</code> .
<i>Courier italic</i>	Indicates a user-defined value in syntax, such as <code>write_file design_list</code>
<b>Courier bold</b>	Indicates user input—text you type verbatim—in examples, such as <code>prompt&gt; write_file top</code>
<b>Purple</b>	<ul style="list-style-type: none"><li>• Within an example, indicates information of special interest.</li><li>• Within a command-syntax section, indicates a default, such as <code>include_enclosing = true   false</code></li></ul>
[ ]	Denotes optional arguments in syntax, such as <code>write_file [-format fmt]</code>
...	Indicates that arguments can be repeated as many times as needed, such as <code>pin1 pin2 ... pinN</code> .
	Indicates a choice among alternatives, such as <code>low   medium   high</code>
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
<b>Bold</b>	Indicates a graphical user interface (GUI) element that has an action associated with it.
<b>Edit &gt; Copy</b>	Indicates a path to a menu command, such as opening the <b>Edit</b> menu and choosing <b>Copy</b> .
Ctrl+C	Indicates a keyboard combination, such as holding down the Ctrl key and pressing C.

## Customer Support

Customer support is available through SolvNetPlus.

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## Accessing SolvNetPlus

The SolvNetPlus site includes a knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. The SolvNetPlus site also gives you access to a wide range of Synopsys online services including software downloads, documentation, and technical support.

To access the SolvNetPlus site, go to the following address:

<https://solvnetplus.synopsys.com>

If prompted, enter your user name and password. If you do not have a Synopsys user name and password, follow the instructions to sign up for an account.

If you need help using the SolvNetPlus site, click REGISTRATION HELP in the top-right menu bar.

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## Contacting Customer Support

To contact Customer Support, go to <https://solvnetplus.synopsys.com>.

# 1

## Design Vision Introduction

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Design Vision tool is the Graphical User Interface (GUI) of the Synopsys synthesis products. It provides features to view and analyze your design at the generic technology (GTECH) level and gate level. It also includes all the synthesis capabilities of the Design Compiler tool. Menu commands and dialog boxes are available for commonly used synthesis features. You can also enter any `dc_shell` command on the command line in the GUI or the shell.

This guide assumes you are familiar with basic Design Compiler concepts. The guide provides guidance to solve specific problems. For example, it presents short procedures that use the visualization analysis feature of the GUI to locate and solve timing problems.

For an overview of the Design Vision tool, see the following topics:

- [About Design Vision](#)
  - [Supported Platforms](#)
  - [Accessing Synthesis Online Help From the Design Vision GUI](#)
  - [Design Vision Tool and Other Synopsys Products](#)
- 

## About Design Vision

For an overview of the Design Vision tool, see the following sections:

- [Features and Benefits](#)
- [User Interfaces](#)
- [Methodology](#)
- [Supported Formats](#)

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## Features and Benefits

The Design Vision GUI provides the following features:

- Window- and menu-driven interface for Synopsys synthesis tools (Design Compiler, DC Explorer, TestMAX DFT/DFTMAX, and Power Compiler)
- Visualization and analysis capabilities that include the following:
  - A hierarchy browser to navigate through the design hierarchy and explore design structures

You can view hierarchical cells and blocks. You can also gather information about the objects (cells, pins, nets, and ports) in a design
  - Histograms to visualize the overall timing performance of the design and to examine trends in various metrics, for example slack and capacitance
  - Schematics to visualize examining timing paths, including fanin and fanout logic, and high-level and low-level design connectivity

Schematics can help you to analyze timing-path problems to focus on the critical paths in your design. You can create schematics to view the top-level design, hierarchical cells, selected timing paths, or selected design objects
  - A path analyzer for performing custom trend analysis on collections of timing paths

You categorize the paths by using predefined or custom category rules based on available timing attributes, and then examine them in a color-coded treemap view
  - *Timing Status Summary* and path data tables to view timing path details, such as attribute values, and to access other timing analysis tools
  - A path inspector for detailed timing path analysis

You can view delay profiles, a path summary, the clock path and datapath elements, and the slack details for an individual timing path
  - Properties viewer and list views to examine object information, such as attribute values
  - The RTL browser to find and debug RTL source problems for selected cells and timing paths
  - A layout view to analyze and debug floorplan elements and physical constraints in a design that you optimize by using the topographical technology in Design Compiler Ultra
  - A congestion map to visually examine highly congested areas in your floorplan

- Visual modes to visually examine specific design information in the physical layout, such as hierarchical cell placement, cell placement in voltage areas, and the distribution of selected groups of cells, nets, ports, and pins
- DFT analysis views (DRC violation browser, violation inspector, and hold time analysis windows) to examine static or dynamic DRC violations and DFT hold time violations
- A UPF diagram view to visually examine a graphic representation of the power architecture as it is described in the multivoltage design database
- A Visual UPF generator to design and implement the power architecture for a multivoltage design

You can create power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy

- A power state table viewer to perform always-on analysis and multivoltage level-shifter analysis in correlation with a UPF diagram
- A MV Advisor violation browser that provides a visual analysis and debug environment for design violations in a multivoltage design
- The HTML-based document browser to view and print man pages and online Help pages
- Reporting capabilities that correlate reported objects to graphical views, including a text report viewer in which you can save or open report files and the HTML report viewer for resource reports with links to RTL files
- An integrated command-line interface with scripting support for all Tool Command Language (Tcl) commands

Using the features of the Design Vision GUI in conjunction with the Design Compiler tool and other Synopsys synthesis tools, you can

- Navigate through the design hierarchy and explore design structures
- Obtain a high-level overview of the timing performance
- Perform timing analysis for blocks you are synthesizing
- Perform detailed visual analysis of selected timing paths and connected logic
- Validate physical constraints and visually examine the physical placement of critical timing path objects in your floorplan

For example, a cell might be placed at a physical distance from the rest of the path because of its fanin or fanout nets

- Visually examine the orientation and physical placement of objects such as macro cells, port locations, placement blockages, and the die area and core area outlines to avoid correlation issues that can result from incorrect or missing physical constraints
- Visually analyze floorplan-related congestion and identify the causes of congestion hotspots
- Analyze and debug congestion problems by cross-probing the RTL for selected cells or timing paths
- Visually examine static and dynamic DRC violations and DFT hold time violations for a test-ready design
- Create UPF power domains and define their supply networks for a multivoltage design
- Visualize the UPF power architecture currently defined in a multivoltage design database to determine whether the domains you have defined match the power intent for the design
- Perform always-on analysis and multivoltage level-shifter analysis using power state tables in correlation with a UPF diagram
- Analyze and debug multivoltage design violations and multivoltage design connections

You can select a design object or timing path and perform any or all of the following actions:

- View or change constraints and attribute values on designs, cells, ports, pins, nets, and clocks
- Display histograms for endpoints, path slack, net capacitance, or other values
- Display timing information for ports, pins, cells, nets, and designs
- Generate, view, and plot schematics
- Highlight individual paths or logic in a schematic or layout view
- View and edit object properties
- View the RTL for selected cells or the cells on a selected timing path
- Generate a variety of design and timing reports

---

## User Interfaces

The Design Vision tool offers two interfaces for synthesis and analysis: the Design Vision graphical user interface (GUI) and a shell command-line interface.

- The Design Vision GUI is an advanced visualization and analysis tool set.

The GUI can perform certain tasks, such as very accurately displaying your design, and it provides visual analysis tools that are available only in the GUI. The look and feel of the Design Vision GUI is consistent with the look and feel of other Synopsys GUI tools.

- The `design_vision` shell command-line interface is a text-only environment that is identical to the Design Compiler shell command-line interface (`dc_shell`).

You enter commands at the command-line prompt the same way you enter them in `dc_shell`. For information about using the shell command-line interface, see the *Design Compiler User Guide*.

The Design Vision GUI offers menus and dialog boxes for important Design Compiler functions. The GUI also provides menus and dialog boxes for visual analysis features that you can use to visualize design data and analyze results. In addition, the GUI provides a command console with a Tcl command-line interface and views of the session log and the command history. You can perform any task in the GUI that you can perform in the shell.

The command-line interface provides access to all the capabilities of the Synopsys synthesis tools. You can execute Tcl commands as follows:

- Enter single commands interactively on the console command line in the Design Vision window
- Enter single commands interactively in the shell
- Run one or more command scripts, that are text files of commands

Using this approach allows you to supplement the subset of Design Compiler commands available through the menu interface. For information about Tcl, see the *Using Tcl With Synopsys Tools* manual.

The shell command-line interface is always available. You can open or close the GUI multiple times during a session. The GUI opens by default when you start the Design Vision tool. Help is available for both interfaces.

---

## Methodology

The Design Vision tool allows you to use the same design methodology and scripts you currently use and to extend your methodology with Design Vision tool visual analysis. Many Design Compiler commands are available on Design Vision tool menus. All Design Compiler tool functions are available through the Design Vision tool command-line interface.

## Supported Formats

The Design Vision tool stores design data in an internal database format. It supports two design database formats: the Synopsys logical database format (.ddc) and the Synopsys Milkyway™ format.

- .ddc format

The .ddc format is a single-file, binary format. The .ddc format stores design data in an efficient manner than the .db format, enabling increased capacity. Also, reading and writing files in .ddc format is faster than reading and writing files in .db format. The .ddc format stores only logical design information.

- Milkyway format

The Milkyway format allows you to write a Milkyway database for use with other Synopsys Galaxy tools, such as IC Compiler tool. The Milkyway format stores both logical and physical design information, but it requires a mapped design.

The Milkyway format is available only when you start the tool in topographical mode. Use the `write_milkyway` command to save netlist and physical design data in a Milkyway design library. You can use a single Milkyway library across the entire Galaxy flow. For more information, see the *Design Compiler User Guide*.

**Note:**

Design Vision tool does not support the `read_milkyway` command.

The Design Vision tool can access all the files that the Design Compiler tool supports. **Table 1** shows the supported design file formats. All netlist formats except .db, equation, PLA, state table, Verilog, and VHDL require special license keys.

*Table 1      Supported File Formats*

Data	Formats
Netlist	Milkyway
	Programmable logic array (PLA)
	Synopsys equation
	Synopsys state table
	Synopsys dc_shell database format (.ddc)
	Verilog
	VHDL

**Table 1      Supported File Formats (Continued)**

Data	Formats
Timing	Standard Delay Format (SDF)
Command Script	Tcl
Library	Synopsys internal library format (.lib) Synopsys database format (.db)
Parasitics	dc_shell command scripts

## Supported Platforms

The Design Vision tool supports the same platforms that Design Compiler tool and other Synopsys synthesis tools support. The hardware and operating system vendor requires patches available for the system. For information about the supported hardware and operating systems and required operating system patches necessary to run the synthesis tools, see *Installing Synopsys Tools* at the following address:

<http://www.synopsys.com/install>

From this Web page you can navigate to the *Synopsys Synthesis Tools Installation Notes* for your release.

## Accessing Synthesis Online Help From the Design Vision GUI

You can access Synthesis Online Help from the Design Vision GUI. The Synthesis Online Help contains the *Design Vision User Guide*. It is a browser-based HTML help system designed for viewing in a Web browser.

To view Synthesis Help,

1. Set the Web browser executable file in your UNIX or Linux path variable.
2. Open the Design Vision GUI > Help > Synthesis Help.

The Web browser appears and displays the Welcome topic for the Synthesis Help.

3. To open the *Design Vision User Guide*, choose Design Vision Documents > Design Vision User Guide.

4. Use the navigation frame (leftmost frame) to find the information you need in one of the following ways:

- Find the topic in the hierarchical organization of the Help system by clicking Contents and expanding the appropriate books until you find the information you need.
- Enter a keyword found in the topic and click Search.

If more than one topic has the words you are searching for, select the appropriate topic from a list of topics.

Synthesis Help makes extensive use of JavaScript and cascading style sheets (CSS). If your browser encounters problems displaying Synthesis Help, open the browser preferences and ensure that JavaScript and style sheets are enabled and check if JavaScript is not blocked by your security preferences.

**Note:**

If you reset preferences while the Help system is open, you might need to click Reload on the browser's navigation toolbar after you reset the preferences.

You can view Synthesis Help as a standalone Help system in your Web browser by opening the file named index.html from the online Help directory: \$SYNOPSIS/doc/syn/html/dvoh/enhanced.

The default Help browser is Mozilla Firefox. If you prefer to use a different browser, note the following limitations:

- Online Help is designed to run in the Firefox browser.
- Online Help is not tested or supported in other browsers, such as Google Chrome, Chromium, SeaMonkey, or Internet Explorer.

To control the size of the text, use the normal controls of your browser. For example, to increase the text size in Firefox, choose View > Zoom > Zoom Text Only. You can also change the default font family or font size.

In Firefox, you can change the default font family and font size as follows:

1. In the menu bar at the top of the screen, click Firefox and select Preferences.
2. In the General panel, scroll down to the Language and Appearance section.
3. Under Fonts and Colors, use the drop-down menus to select the font and font size of your choice.
4. Close the Preferences page.

---

## Design Vision Tool and Other Synopsys Products

As a visual analysis tool and the GUI for Synopsys synthesis, the Design Vision tool works with the Design Compiler, TestMAX DFT/DFTMAX, and Power Compiler tools to synthesize and analyze the design. The Design Vision GUI is also available in the DC Explorer tool.

The Design Vision tool and Synopsys PrimeTime tools have similar timing visualization features. However, these tools have different timing engines and differ in their application to analysis. The Design Vision tool has the same static timing engine as the Design Compiler tool. The Design Vision tool is used to perform timing analysis and modification of the blocks that you synthesize. The PrimeTime tool is used for static timing sign-off or to analyze the timing of a chip or large portions of a chip.

Sources of information include man pages, the SolvNetPlus knowledge base, and the Customer Support Center. For information about accessing these sources of information, see [Customer Support](#).

# 2

## Working With Design Vision Tool

---

The Design Vision tool offers the following interfaces: the design\_vision shell command-line interface or shell and the Design Vision Graphical User Interface (GUI). The shell command-line interface is a text-only environment in which you enter commands at the command-line prompt. The GUI provides menus with frequently-used synthesis commands and visual analysis tools for the Synopsys synthesis environment; use it for visualizing design data and analyzing results.

To learn how to operate the Design Vision GUI, see the following topics:

- [Running Design Vision Tool](#)
  - [Graphical User Interface](#)
  - [Getting Help in the GUI](#)
- 

## Running Design Vision Tool

To learn how to run the Design Vision tool and use the GUI, see the following topics:

- [Design Vision Modes](#)
- [License Requirements](#)
- [The Design Vision Setup Files](#)
- [Starting the Tool](#)
- [Entering Tcl Commands in the GUI](#)
- [Choosing Menu Commands in GUI Windows](#)
- [Opening and Closing the GUI](#)
- [Using Script Files](#)
- [Saving Designs](#)
- [Exiting Design Vision](#)

---

## Design Vision Modes

You can use the Design Vision tool in the following modes:

- Wire load mode
- Topographical mode
- Multimode
- UPF mode

Wire load mode and topographical mode are tool modes. When you start the Design Vision tool, you must choose either wire load mode or topographical mode.

Multimode and UPF mode are not tool modes. Multimode allows you to operate the tool under multiple operating conditions and multiple modes, such as test mode and standby mode. UPF mode allows you to specify advanced low-power methodologies. Multimode and UPF mode are available only in topographical mode.

For more information about these modes, see the *Design Compiler User Guide*.

---

## License Requirements

To use the Design Vision tool, you need the Design-Vision license. Some Design Vision features and `dc_shell` commands require additional licenses. In topographical mode, you also need a DC-Extension license.

In topographical mode, you need following licenses:

- A Design-Vision license, a DesignWare license, and the DC Ultra package to use the Design Vision tool.
- A DC-Extension license to use the Design Compiler Graphical tool Layout window.
- A Milkyway-Interface license. If you use the Milkyway flow; this license is included in the DC Ultra package.

To determine which licenses you need for your design flow, contact your Synopsys representative.

Synopsys licensing software and the documentation describing it are separate from the tools that use it. You can install, configure, and use a single copy of Synopsys Common Licensing (SCL) for all Synopsys tools. By providing a single, common licensing base for all Synopsys tools, SCL reduces license administration complexity and minimizes the effort you expend in installing, maintaining, and managing licensing software for Synopsys tools.

For complete Synopsys licensing information, see the *Synopsys Common Licensing Administration Guide*. This guide provides detailed information about SCL installation and configuration, including examples of license key files and troubleshooting guidelines.

## Allocating Design Vision Licenses

You can view a list of the licenses you are currently using and a list of additional licenses, check out additional licenses, or release licenses you no longer need.

To display current license information,

1. Start the Design Vision GUI.
2. Choose File > Licenses.

The Application Licenses dialog box appears. The Allocated Licenses list shows the licenses you are currently using. The Available Licenses list shows other licenses you can use.

3. When you finish viewing the license information, click Close to close the dialog box.

To check out an additional license,

1. Choose File > Licenses.
2. Select a license in the Available Licenses list.
3. Click Allocate.

The Design Vision tool checks out a copy of the license if one is available or displays an error message if all the licenses are already used.

## Releasing Licenses

To release a license,

1. Choose File > Licenses.
2. Select a license in the Allocated Licenses list.
3. Click Release.

Design Vision tool releases the selected license.

For more information about the licenses required for synthesis and about checking out and releasing licenses in shell, see the *Design Compiler User Guide*.

---

## The Design Vision Setup Files

Before starting the Design Vision tool, make sure the `$SYNOPSYS` variable is set and include the path to the bin directory in the `$PATH` variable. Be sure to specify the absolute

path to indicate the Synopsys root that contains the Design Vision installation, as shown in the following command:

```
/tools/synopsys/2013.03/bin/
```

If you use a relative path (..), as shown, the tool cannot access the libraries that are located in the root directory:

```
.../2013.03/bin/
```

When you start the tool in wire load or topographical mode, it automatically executes commands in the three standard Design Compiler setup files that dc\_shell uses. These files have the same file name, .synopsys\_dc.setup, but they reside in different directories. The same sourcing rules apply for both the design\_vision shell and dc\_shell. For more information about the .synopsys\_dc.setup files and the initialization settings for synthesis, see the *Design Compiler User Guide*.

In addition, the tool reads another set of setup files when you open the GUI, named .synopsys\_dv\_gui.tcl. You can use these files to perform GUI-specific setup tasks. Use the .synopsys\_dc.setup files to perform non-GUI application setup tasks. Settings from the ~/.synopsys\_dc\_gui/preferences.tcl files override settings from the .synopsys\_dc.setup files.

The tool reads the .synopsys\_dc.setup and .synopsys\_dv\_gui.tcl files from three directories in the following order:

1. The Synopsys root directory

These system-wide setup files contain system variables defined by Synopsys and general Design Compiler tool and Design Vision tool setup information for all users at your site. Only the system administrator can modify these files.

2. Your home directory

These user-defined setup files can contain variables that define your preferences for the Design Compiler and Design Vision working environment. The variables in these files override the corresponding variables in the system-wide setup files.

3. The current working directory (the directory from which you start the tool)

These design-specific setup files can contain project-specific or design-specific variables that affect all of the designs in this project directory. To use these files, you must invoke the tool from this directory. Variables defined in these files override the corresponding variables in the user-defined and system-wide setup files.

You can use the setup file in your home or design directory to define Tcl scripts that you need to run during a Design Vision or Design Compiler session. For more information, see [Using Script Files on page 38](#).

In addition to reading the setup files, the tool loads GUI preferences and view settings from a file named `~/.synopsys_dc_gui/preferences.tcl` in your home directory. You should not edit this file. For more information, see [Setting GUI Preferences on page 67](#).

For more information, see the following topics:

- *Synopsys Synthesis Tools Installation Notes*

Provides information about defining the `$SYNOPSYS` and `$PATH` variables.

- *The Design Compiler User Guide*

Provides information about the locations of setup files and initialization settings for synthesis.

---

## Starting the Tool

The Design Vision tool operates in the X windows environment on UNIX or Linux. Before starting a Design Vision session, make sure the `$SYNOPSYS` variable is set and include the path to the bin directory in the `$PATH` variable. Before opening the GUI, make sure your `$DISPLAY` environment variable is set to the name of your UNIX or Linux system display. You can optionally set the `$DISPLAY` variable when you start the session.

The tool provides an option to enable the Design Compiler topographical technology for designs with physical constraints. You can start a Design Vision session in either wire load mode or topographical mode, but you cannot change the mode during a session.

### Note:

You can query the mode by running the `shell_is_in_topographical_mode` command. The command returns 1 if the tool is running in topographical mode; otherwise it returns 0.

To start the Design Vision tool in wire load mode, enter the `design_vision` command in a UNIX or Linux shell:

```
% design_vision
```

If you are using Design Compiler topographical technology or the Design Compiler Graphical tool, you must indicate this by specifying the `-topographical_mode` option with the `design_vision` command:

```
% design_vision -topographical_mode
```

You can abbreviate this option to as short as `-to`. Topographical mode requires a DC Ultra license and a DesignWare license. For information about additional license requirements, see [License Requirements on page 29](#).

These commands start the tool and open the GUI by default. The Design Vision window appears on the screen, and the command-line prompt, which is `design_vision>` in wire load mode or `design_vision-topo>` in topographical mode, appears in the UNIX or Linux shell and on the console in the Design Vision window.

Ensure to specify the absolute path to indicate the Synopsys root that contains the Design Vision installation, as shown:

```
% /tools/synopsys/2014.09/bin/design_vision
```

If you use a relative path `(..)`, as shown, the tool cannot access the libraries that are located in the root directory:

```
% ../../2013.03/bin/design_vision
```

You can start the tool in the shell command-line interface without opening the GUI by specifying the `-no_gui` option. For example, enter one of the following commands:

```
% design_vision -no_gui
% design_vision -topographical_mode -no_gui
```

When you want to open the GUI, enter the `gui_start` command. For more information, see [Opening and Closing the GUI on page 36](#).

To set the `$DISPLAY` environment variable when you start a Design Vision session, specify the `-display host_name` option, where `host_name` is the name of your UNIX display terminal. For example, enter one of the following commands:

```
% design_vision -display 192.180.50.155:0.0
% design_vision -topographical_mode -display my_host:0.0
```

The `design_vision` command provides other startup options for customizing the session. For example, you can specify a remote display, run a batch startup script, or initiate certain `dc_shell` commands.

- Use `-checkout` to access additional licenses.
- Use `-f` to run a script file at startup.
- Use `-x` to run a `dc_shell` command at startup.

To see the complete list of available options without starting the tool, specify the `-help` option with the `design_vision` command:

```
% design_vision -help
```

For detailed information about the startup options, see the `design_vision` man page.

## See Also

- [License Requirements](#)
- [The Design Vision Setup Files](#)
- [Opening and Closing the GUI](#)

---

## Entering Tcl Commands in the GUI

You can interact with the design\_vision shell by using dc\_shell commands, which are based on the Tool Command Language (Tcl) and include certain command extensions needed to implement specific Design Compiler functionality. The dc\_shell command language provides capabilities similar to UNIX command shells, including variables, conditional execution of commands, and control flow commands.

You can run dc\_shell commands in the following ways:

- Enter single commands on the command line at the bottom of the console in the Design Vision window.
- Enter single commands on the command line in the shell.
- Run one or more command scripts, which are text files of commands.

For details about running command scripts in the GUI, see [Using Script Files on page 38](#).

You can enter any dc\_shell command on the console command line just as you would enter commands in the shell. When you enter a command, the tool echoes the command output (including processing messages and any warnings or error messages) in the console log view. For example, if you enter `get_selection`, the log view displays a list of the names of all selected objects.

To enter a command on the console command line,

1. Click the command line to give it the focus.
2. Enter the command.
3. Click the prompt button or press Enter.

When entering a command, option, or file name, you can minimize your typing by pressing the Tab key when you have entered enough characters to specify a unique name; the tool completes the remaining characters. If the characters you entered could be used for more than one name, the tool lists the qualifying names from which you can select by using the arrow keys and the Enter key.

You can find information about dc\_shell commands by viewing man pages in the man page viewer. You can also use the man page and help utilities just as you would use them in dc\_shell.

### See Also

- [Console Command-Line Editing](#)
- [Getting Help on the Command Line](#)
- [Accessing Man Page Viewer](#)

---

## Choosing Menu Commands in GUI Windows

The Design Vision GUI provides menu commands and dialog boxes for most graphic features, such as generating histograms, displaying schematics, and highlighting design objects. In addition, the GUI provides menu and dialog box equivalents for many dc\_shell commands. Menu commands are grouped by function on the menus in each GUI window.

To choose a command on a menu bar menu, click the menu name to open the menu, and click the command name on the menu.

Some frequently used menu commands are also available on menus for individual views.

To choose a command on menu, move the pointer over the object of interest, right-click to display the menu, and click the command name.

A menu command can perform an immediate operation, display a submenu, or display a dialog box.

- Menu commands that display a submenu are followed by a right-pointing arrow.
- Menu commands that open a dialog box that requires a response before performing an operation are followed by an ellipsis (...).

These commands open a dialog box to prompt you for the information. Dialog boxes that require a response before performing an operation contain OK and Cancel buttons and sometimes an Apply button. After selecting options or entering information in the dialog box, you respond by clicking OK or Apply.

- Menu commands without an arrow or ellipsis either perform an immediate operation or open a dialog box that performs immediate operations.

Dialog boxes that perform immediate operations usually display options and contain a Close button. You select options that perform operations and click Close to close the dialog box.

The GUI displays command output, including processing messages and any warnings or error messages, in both the shell and the console log view.

The Design Vision documentation identifies commands with their menus in the following formats:

- *Menu > Command*
- *Menu > Submenu > Command*

where

- *Menu* represents a menu title on the menu bar.
- *Submenu* represents a menu command that displays a submenu.  
Some submenus contain commands that open other submenus.
- *Command* represents a command that performs an operation or displays a dialog box.

Each menu command can also be activated by a keyboard shortcut, which is indicated on the menu by an underscore (\_) below a letter in the command and, if needed, the name of the modifier key (Shift or Ctrl) to the right of the command name. You can view a list of keyboard shortcuts by choosing Help > Report Hotkey Bindings.

## See Also

- [Menu Bar](#)
- [Displaying the List of Keyboard Shortcuts](#)

---

## Opening and Closing the GUI

You can open or close the GUI at any time during a Design Vision session. For example, you can open the GUI to perform visual analysis tasks or close the GUI to perform time-consuming tasks or batch processes in the shell. When you close the GUI, your designs remain loaded in memory and the command-line prompt remains active in the shell. If you reopen the GUI, a new Design Vision window appears.

When you open the GUI, it reads the GUI setup and preferences files and opens a new Design Vision window.

- The setup files perform basic setup tasks, such as initializing variables and declaring design libraries.
- The preference files set schematic and abstract clock graph view properties and global application preferences.

The Design Vision window contains the menus, toolbars, view windows, and panels that you use to perform timing analysis and other visual analysis tasks.

To learn how to open and close the GUI, see the following topics:

- [Opening the GUI](#)
- [Closing the GUI](#)

## Opening the GUI

You can open the GUI at any time during a Design Vision session. If you start a session with the GUI closed, you can open the GUI from the shell command line. Before you open the GUI, make sure that your `$DISPLAY` environment variable is set to your UNIX display name.

To open or reopen the GUI from the `design_vision` shell, enter the following command:

```
prompt> gui_start
```

When you open the GUI, either at startup or from within the shell command-line interface, the tool performs the following tasks:

1. Reads and executes commands from the Design Vision GUI setup files.
2. Opens the Design Vision window.

You can specify a Tcl script that you want to run when you open the GUI by using the `-file` option with the `gui_start` command. For example, to run the script from a file named `my_gui_script.tcl`, enter the following command:

```
prompt> gui_start -file my_gui_script.tcl
```

## See Also

- [Closing the GUI](#)
- [Starting the Tool](#)

## Closing the GUI

You can close the GUI without exiting the tool at any time during the session. For example, if you need to save system resources, you can close the GUI and leave the tool running as a command-line interface.

To close the GUI without exiting the tool, choose File > Close GUI.

Alternatively, you can enter the following command:

```
prompt> gui_stop
```

### See Also

- [Opening the GUI](#)
  - [Saving Designs](#)
  - [Starting the Tool](#)
- 

## Using Script Files

You can use scripts to accomplish routine or repetitive tasks, such as setting constraints or defining other design attributes. You can use the existing Tcl scripts in the Design Vision command-line interface and the GUI.

You can create a script file by placing a sequence of Tcl commands in a text file. You can also define scripts in your setup files. Any dc\_shell command can be executed within a script file. You can run any Tcl script defined in a setup file or in another script file by selecting the file name in the Execute Script File dialog box.

To run a scripts defined in a setup file,

1. Define the script in the setup file.
2. Start Design Vision.
3. Enter the script name on the command line.

The tool executes the script and displays status messages in the console log view and on the status bar.

To run Tcl scripts from a script file,

1. Create the script file with a .tcl extension.
2. Start Design Vision.
3. Choose File > Execute Script.

The Execute Script File dialog box appears which is a standard file browser.

4. Navigate to the directory that contains the script file you want to run.
5. If you need to display file names that do not have a script file extension, select All Files (\*) in the Files of type drop-down list.
6. Select the file name. Make sure the file contains the correct type of script for the mode you are using. File names for Tcl scripts typically have a .tcl extension.
7. Click Open.

To run scripts in the GUI, choose File > Execute Scripts. The Execute Script File dialog box appears.

Alternatively, you can run scripts from the command line by using the `source` command. For information about this command, see the man page.

For information about Tcl, see the *Using Tcl With Synopsys Tools* manual.

## See Also

- [The Design Vision Setup Files](#)
- [Setting Variables](#)
- [Specifying Logic Libraries](#)

---

## Saving Designs

You can exit the Design Vision tool at any time and return to the operating system. By default, the tool saves the session information in the `command.log` file. However, if you change the name of the log file using the `sh_command_log_file` variable after you start the tool, session information might be lost.

The tool does not automatically save the designs loaded in memory before exiting. To save these designs before exiting, use the Save or Save As command on the File menu or the `write_file` command on the command line.

To save the current design and each of its subdesigns in separate .ddc format files named `design_name.ddc`, where `design_name` is the name of the design, choose File > Save.

To save the current design and all of its subdesigns in a single file with a different file name or file format, perform the following steps:

1. Choose File > Save As.
2. Enter or select a file name.
3. Select a file format.
4. Click OK.

For more information about how to save your design, see [Saving Designs on page 321](#).

---

## Exiting Design Vision

To exit the tool, you can do any of the following:

- Choose File > Exit, and then click OK in the message box that appears.
- Enter `exit` or `quit` on the command line.
- Press `Ctrl+C` three times in the UNIX or Linux shell.

### See Also

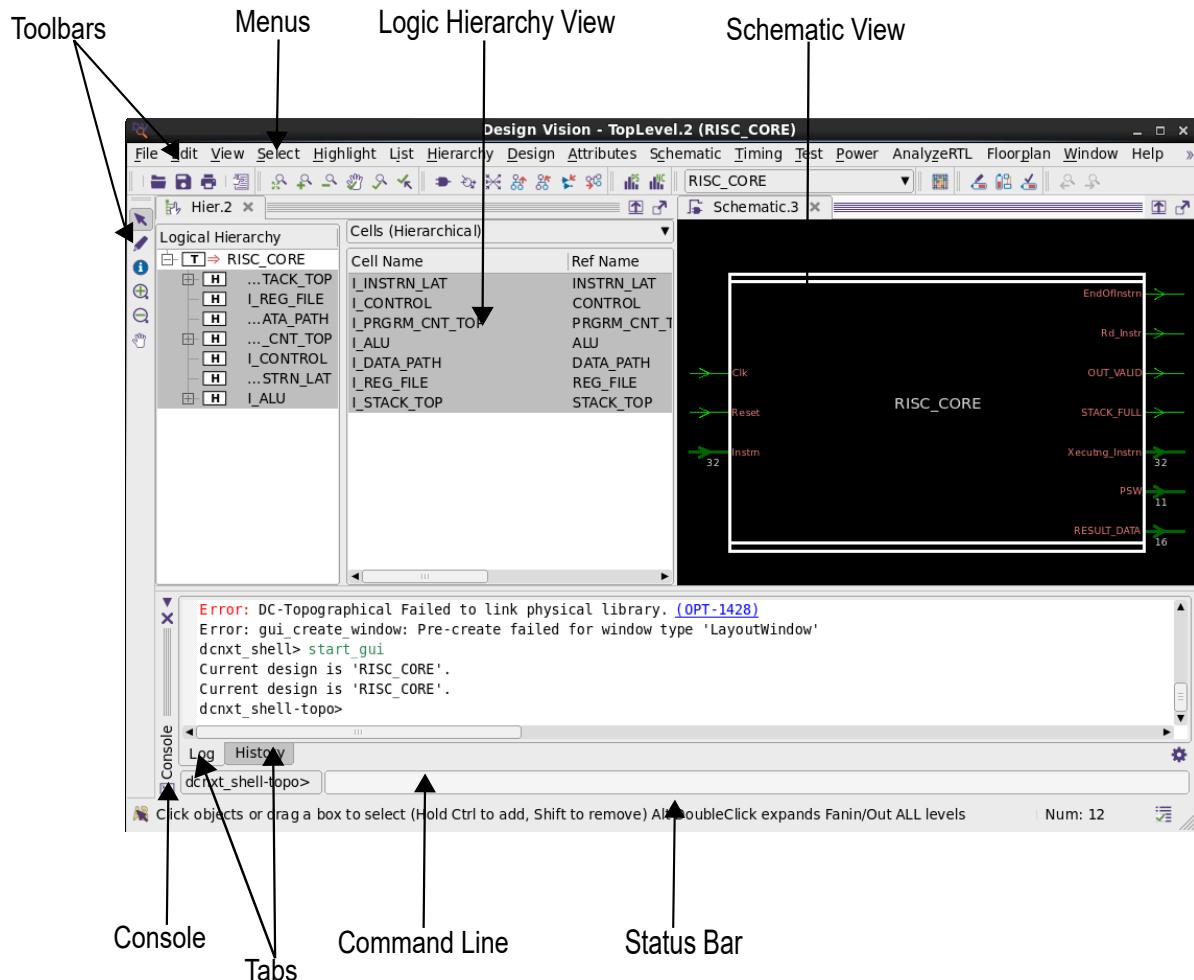
- [Starting the Tool](#)
  - [Opening and Closing the GUI](#)
- 

## Graphical User Interface

The Design Vision window appears by default when you start the Design Vision tool.

[Figure 1](#) shows an example of the window you see when you start Design Vision, read in a design, and open a schematic view.

**Figure 1** The Design Vision Window



The Design Vision window consists of a title bar, a menu bar, and several toolbars at the top of the window and a status bar at the bottom of the window. The title bar and menu bar are always visible. You can display or hide individual toolbars or the status bar.

The workspace area between the toolbars and the status bar displays view windows and panels. View windows provide graphic or textual views of design information. Panels provide interactive tools for setting options or performing often used tasks. View windows and panels can contain tabs with multiple views or pages. The “active view” is the view that has the mouse focus.

The hierarchy browser (logic hierarchy view) and the console appear in the Design Vision window by default. To visualize a design, you can open a schematic view. For information about these features, see the following topics:

- [Design Vision Windows](#)
  - [Design Vision Data View](#)
  - [Design Vision Window Features](#)
  - [The Hierarchy Browser](#)
  - [Schematic Views](#)
  - [The Command Console](#)
  - [The Script Editor](#)
  - [Configuring the GUI](#)
- 

## Design Vision Windows

The Design Vision GUI displays information in application windows that you can move, resize, minimize, or maximize by using the window management tools on your UNIX or Linux desktop. Each window title bar lists the product name (Design Vision), the name of the window, and the name of the active view (the view window that has the mouse focus).

The GUI provides the following application windows:

- The Design Vision window appears automatically when you start a Design Vision session or open the GUI.
- The Layout window is available for visualizing the physical aspects of a design in the Design Compiler Graphical tool product when you start the tool in topographical mode.

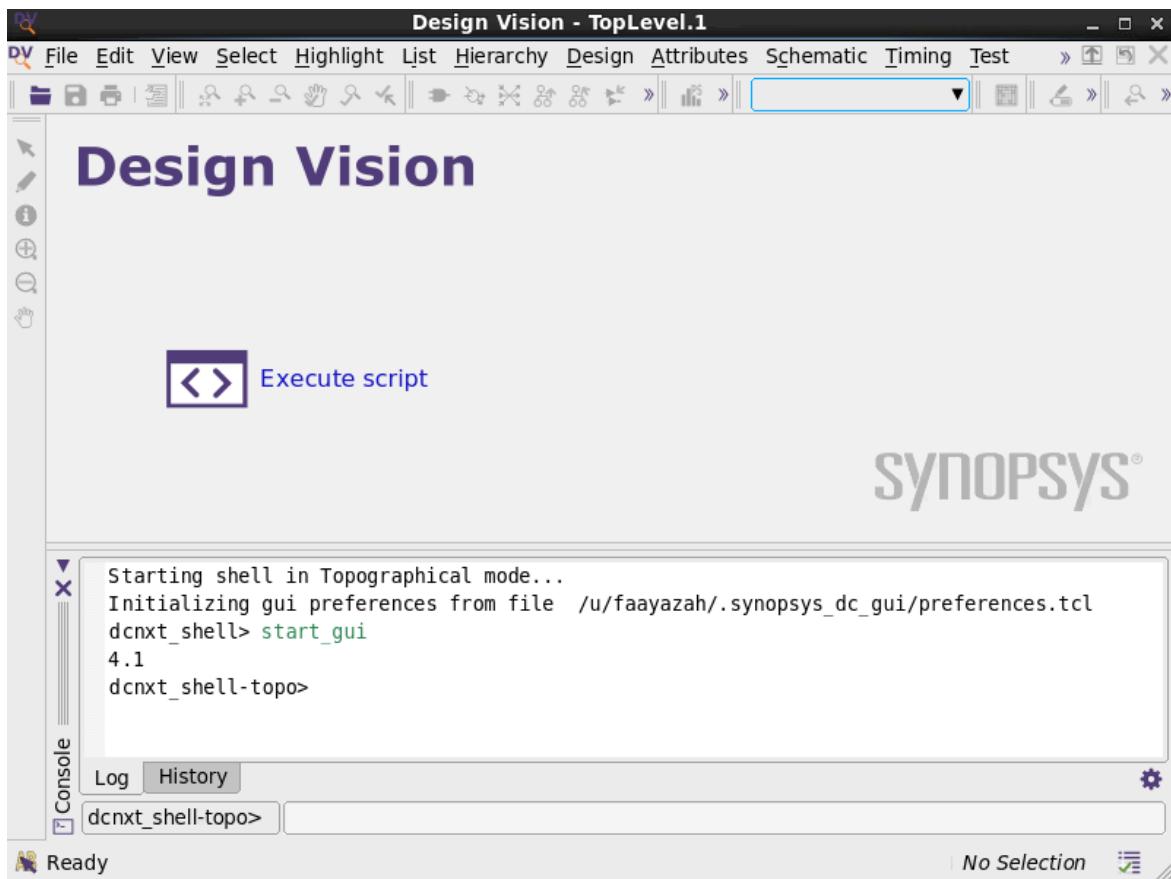
You can open multiple instances of the Design Vision window or the Layout window and use them to compare views, or different design information within a view, side by side. The window name includes the unique instance number of the window.

All open application windows share the same designs in memory and the same current timing information. However, each window is independent of the other windows. You can configure the toolbars, status bar, view windows, and panels independently for each window. The design objects you select in one window are automatically selected in the other windows.

## Design Vision Data View

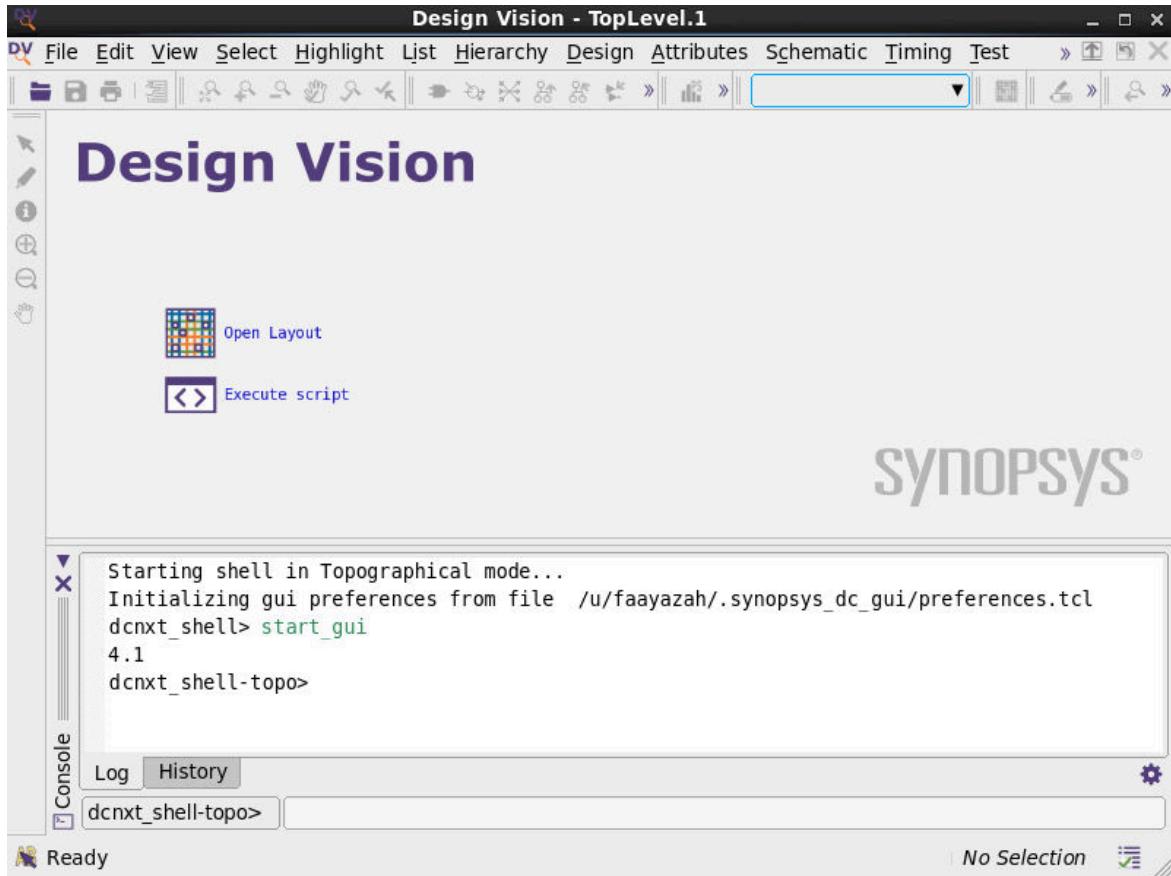
When you have not loaded the design in the tool, only the Execute script option appears in the Design Vision window as shown in [Figure 2](#).

*Figure 2 The Design Vision Window View*



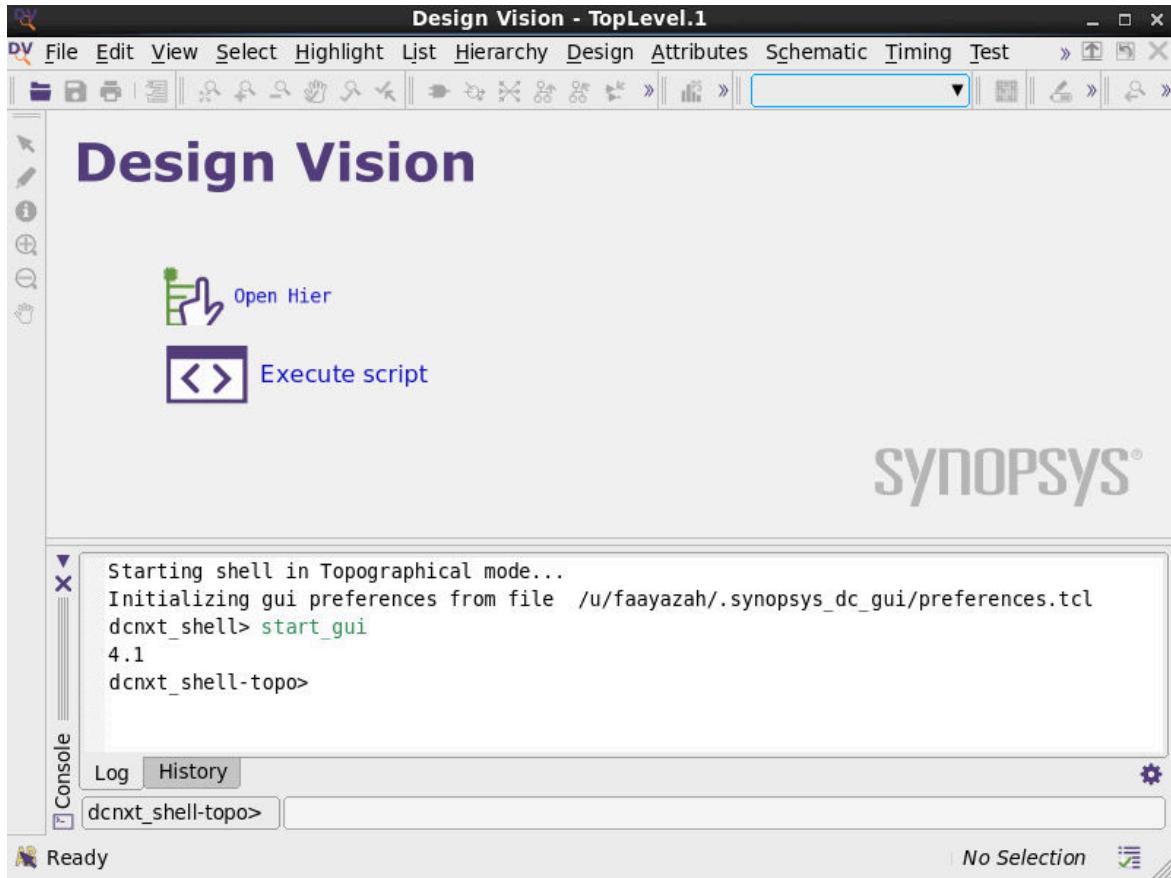
When you open the layout window and load the design in the tool, the Option Layout and the Execute script options appear as shown in [Figure 3](#).

Figure 3 The Design Vision Window View



When the top level window is open and the design is loaded in the tool, the Open Hier and Execute script options appear as shown in [Figure 4](#).

*Figure 4 The Design Vision Window View*



## Design Vision Window Features

For information about Design Vision windows, see the following topics:

- [Title Bar](#)
- [Menu Bar](#)
- [Toolbars](#)
- [Status Bar](#)
- [View Windows](#)
- [Panels](#)

## Title Bar

The title bar at the top of an application window displays the product name (Design Vision), the window name, the top-level design name, and the name of the active view. The window name takes the form TopLevel.N for the Design Vision window or LayoutWindow.N for the layout window, where N is a positive integer. If you open additional windows, the windows are numbered sequentially throughout the session.

View windows display graphical or textual design information. The active view is the view window that has the mouse focus. View window names take the form View\_type.N, where N is a positive integer. If you open multiple view windows for the same type of view, the windows that you open are also numbered sequentially throughout the session (regardless of which GUI window they are in).

## Menu Bar

The menu bar contains menus with the commands you need to work in the window. Menu commands are grouped by function on the menus in each application window.

To choose a command on a menu bar menu, click the menu name to open the menu, and click the command name on the menu. You can display a brief message in the status bar about the action that a command performs by holding the pointer over the command name. For menu commands that can also be used by pressing a toolbar button or typing a keyboard shortcut, the menus show representations of those alternatives.

### Note:

If the window is not wide enough to display all the menu names on the menu bar, the window displays all the menu names that fit, from left to right, followed by an overflow button (⋮). To access the other menus, click the overflow button.

Some frequently used menu commands are also available on menus for individual views. To choose a command on a menu, move the pointer over the object of interest, right-click to display the menu, and click the command.

You can use the left or the right mouse buttons to choose commands on menu bar menus. Each menu contains commands related to the menu title. A menu command can execute a Tcl command, display a submenu, or display a dialog box.

- Commands that execute Tcl commands have no punctuation.
- Commands that include a submenu are followed by a right-pointing arrow.
- Commands that display a dialog box require a response before performing an operation are followed by an ellipsis (...).

- Dialog boxes that require a response before performing an operation contain OK and Cancel buttons and sometimes an Apply button. After selecting options or entering information in the dialog box, you can respond by clicking OK or Apply.
- Dialog boxes that do not require a response usually display information and contain a Close button that you can click to close the dialog box.

You can display a brief message in the status bar about the action that a menu command performs by holding the pointer over the command. For menu commands that can also be used by clicking a toolbar button or pressing a keyboard shortcut, the menus show representations of those alternatives.

### See Also

- [Choosing Menu Commands in GUI Windows](#)
- [Menus](#)

## Toolbars

Each application window provides toolbars with buttons you can use to quickly access frequently used operations or tasks. To determine the function of a toolbar button, hold the pointer over the button. A tooltip displays the name of the button, and the status bar displays a brief description of its use. You cannot disable these messages.

Toolbars are always attached to a window edge. You can enhance your working environment by moving individual toolbars to different positions below the menu bar, or to the left, right, or bottom edge of the window. You can also disable a toolbar, hiding it from view.

If a window edge is not long enough to display all of the toolbars attached to it, the GUI displays the full toolbars that fit and shortened versions of the other toolbars. A shortened toolbar consists of a default toolbar button and an overflow button (»). To access the other toolbar buttons on a shortened toolbar, click the overflow button.

The Design Vision window provides the following toolbars that are available either in the layout window or in the Design Vision window.

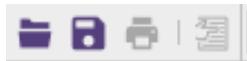
For descriptions of the buttons available on a Design Vision toolbar, click the following toolbar name:

- [Design List Toolbar](#)



Changes the current design.

- [File Toolbar](#)



Opens or saves designs, prints schematic views, and open the Properties dialog box.

- [Layout Toolbar](#)



Opens a new instance of the layout window.

- [Mouse Tools Toolbar](#)



Provides interactive left mouse button tools that you can use in graphic views to select objects, highlight objects (not supported in UPF diagram views), display object information, or magnify and traverse the design.

- [Power Toolbar](#)



Opens the Visual UPF dialog box, a UPF diagram view, and the MV Advisor violation browser.

- [Schematics Toolbar](#)



Opens and performs viewing operations in schematic views.

- [Select By Name Toolbar](#)

Selects or highlights objects in the active schematic or layout view by typing their names or a filter expression. You can select or highlight cells, ports, pins, or nets.

- [Timing Views Toolbar](#)

Opens histogram views.



- [View Zoom/Pan Toolbar](#)



Controls the magnification and position of a design in schematic and layout views.

- [Zoom and Pan History Toolbar](#)



Redisplays previous zoom and pan settings in a schematic or layout view.

For descriptions of the buttons available on a layout toolbar, click the following toolbar name:

- [Analysis Toolbar](#)



Enables or disables visual modes, map modes, and net connections. For visual modes, the toolbar displays the button for the most recently active visual mode or the snapshot visual mode button by default.

- [Highlight Toolbar](#)



Changes the current highlight color, highlights selected objects, and clears highlighting from selected objects or from all highlighted objects in a layout view.

- [Mouse Tools Toolbar](#)



Provides interactive left mouse button tools that you can use in graphic views to select objects, highlight objects (not supported in UPF diagram views), display object information, draw rulers (supported only in layout views), or magnify and traverse the design.

- [Mouse Tool Options Toolbar](#)



Sets options that configure the behavior of the active mouse tool when you click or drag the pointer in a layout view. You can set options on this toolbar for the Selection tool, the Highlight tool, and the Ruler tool.

## See Also

- [Toolbars](#)

## Status Bar

Each application window displays a status bar at the bottom of the window. The status bar displays the information listed in [Table 2](#).

*Table 2 Information Displayed by the Status Bar*

When you do this	The status bar displays this information
Select one object	Object name
Select multiple objects	Number of selected objects
Hold the pointer over a menu command, toolbar button, or tab	Information about the action it performs

You can quickly display the list of selected objects in the Selection List dialog box by clicking the  button at the right end of the status bar.

You can hide or display the status bar in a window by choosing View > Status Bar.

## View Windows

View windows are child windows that display graphic or textual views of design information within the workspace area of an application window. When you click anywhere within a view window, the GUI highlights its title bar to indicate that it has the focus (that is, it is the active view) and can receive keyboard and mouse input.

View windows that contain multiple views provide a tab for each view. When you open a view window that has multiple views, it displays a default view. To change to a different view, you click its tab.

The GUI provides the following types of view windows:

- Graphic views (graphical descriptions of design information such as schematic, histogram, and layout views).
- Hierarchy views (for traversing hierarchical structures and gathering design information at different hierarchy levels).
- Text views (textual design information such as reports and object lists).

When you open the GUI, the logic hierarchy view appears in the workspace area of the Design Vision window. The analysis tasks that you perform during the session determine which other types of views you open. For information about the logic hierarchy view, see [Browsing the Design Hierarchy](#).

You can adjust the sizes of view windows for viewing purposes, and you can move them to different locations within the workspace area. In addition, you can

- Arrange the open view windows by tiling them within the workspace area.
- Minimize individual view windows, or maximize a view window to fill the workspace area.

The view window that has the mouse focus is called the active view. The GUI displays a tab at the bottom of the workspace (above the console) for each open view window. When you click a tab, the GUI displays its view window on top of the other view windows in the workspace and makes it the active view. If a view window and a panel overlap on the screen, the panel appears on top of the view window.

The view appears in the workspace area between the toolbars and the status bar in the Design Vision window or the layout window. The analysis tasks that you perform during the session determine which view you open.

Some view windows contain multiple view types. For example,

- The logic hierarchy view contains a hierarchy tree and an object list.
- Histogram views contain a histogram and an object list.

The Design Vision window provides the following views:

- Logic hierarchy - [The Hierarchy Browser](#)
- Schematic - [Schematic Views](#)
- Histogram - [Viewing High-Level Timing Results](#)
- Path analyzer - [Analyzing Timing Path Collections](#)
- Timing Status - [Examining Timing Path Details](#)
- Path inspector - [Inspecting Timing Path Elements](#)
- RTL browser - [Viewing RTL Files](#)
- UPF diagram - [Viewing the UPF Power Design](#)
- MV Advisor violation browser [Opening the MV Advisor Violation Browser](#)
- DRC violation browser - [DRC Violation Browser](#)
- DRC violation inspector - [Violation Inspector](#)
- Hold time analysis - [Using DFT Analysis Tools](#)
- Report -[Viewing Reports](#)
- Object list - [Viewing Object Lists](#)
- Design list - [Viewing the List of Designs in Memory](#)

The layout window provides the following views:

- Layout view - [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- RTL browser - [Examining Cells in the RTL Browser](#)
- UPF diagram - [Viewing the UPF Power Design](#)
- MV Advisor violation browser - [Analyzing Multivoltage Design Problems](#)

In most views, you can use navigation keys (the arrow keys, Page Up, Page Down, Home, and End) to scroll or navigate through the view.

### See Also

- [Views](#)

## Panels

Panels are enhanced toolbars that contain tools for setting options or performing frequent tasks while working with the design in view windows. Most panels are associated with a particular view and operate on the active view, which is the view that has the mouse focus. An exception is the console, which contains a command line and its own views. A tabbed panel contains tabs that you can click to access different tools or views. The first time you open a panel during a session, it displays the tools or view for its default tab.

When you open the GUI, the console is docked to the bottom edge of the Design Vision window and the other panels are hidden by default. For information about the console, see [The Command Console on page 60](#).

You can adjust the sizes of panels for viewing purposes, and you can move a panel to another location on or off the parent window by dragging the double bars on one of its sides. In addition, you can dock or undock individual panels by attaching them at edges of the window or separating them from the edge so they can float above or outside the window. You can also disable a panel, hiding it from view. A panel that is associated with a particular view is automatically hidden when you close the view window.

If a panel and a view window overlap on the screen, the panel appears above the view window.

Most panels are associated with a particular view window and operate on the active view, which is the view window that has the mouse focus. An exception is the console, which contains a command line and its own views.

### Note:

If you have trouble finding a panel, you can quickly identify it by hiding and redisplaying it. To hide or display a panel, choose View > Toolbar > panel\_name twice.

The Design Vision window provides the following panels:

- [Console](#)
- [Power State Table Panel](#)
- [Query Panel](#)
- [View Settings Panel](#)

The layout window provides the following panels:

- [Console](#)
- [Map Mode Panel](#)
- [Overview Panel](#)
- [Power State Table Panel](#)
- [Query Panel](#)
- [View Settings Panel](#)
- [Visual Mode Panel](#)

#### See Also

- [Panels](#)

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## The Hierarchy Browser

The hierarchy browser (logic hierarchy view) appears by default when you open the GUI. Use it to navigate through your design, see the relationships among its levels, and gather object information. You can also select the designs or objects that you want to examine in graphic views or with other analysis tools.

The view window consists of an instance tree on the left and an object table on the right. When you read in a design, the instance name of the top-level design appears in the left pane. You can

- Click the expansion button (plus sign) for a hierarchical block (an instance that contains subblocks) to expand the instance tree, showing the names of the subblocks at the next level in the hierarchy
- Select an instance or hierarchical block to display information about the cells or other objects that it contains

The object table displays information about hierarchical cells by default. To facilitate your examination of the objects within an instance or hierarchical cell, you can select the type of

objects that appear in the object table. You can display information about hierarchical cells, leaf cells, pins and ports, pins of child cells, and nets.

The logic hierarchy view helps you navigate the design hierarchy and gather design object information. The view window is divided into the following panes, with an instance tree of instantiated cells in the left pane and a table containing object information in the right pane.

### Instance Tree

The instance tree lets you quickly navigate the design hierarchy and see the relationships among its levels. If you select a hierarchical cell (an instance that contains subblocks) in the instance tree, information about the objects in the cell appears in the object table. You can Shift-click or Control-click instance names to select combinations of cells.

The names of hierarchical cells are preceded by expansion buttons (plus or minus signs).

- A plus (+) sign means you can click the button to expand the list and display the names of the subblocks within the cell.
- A minus (–) sign means you can click the button to collapse the list and hide the names of subblocks.

You can use the arrow keys to navigate the instance tree. Use the Up Arrow and Down Arrow keys to move up or down the tree, the Right Arrow key to expand a cell, and the Left Arrow key to collapse a cell.

### Object Information

By default, the object table displays information about hierarchical cells belonging to the selected instance in the instance tree. You can

- Sort the table information alphabetically by clicking a column heading. Click the heading again to reverse the sort.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to information based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

To display information about other types of objects, select the object types in the list above the table. You can display information about

- Hierarchical cells
- All cells

- Pins and Ports
- Pins of child cells
- Nets

For cells, the table columns provide the following information:

Column	Description
Cell Name	Cell instance name
Ref Name	Name of the design the cell references
Cell Path	Full hierarchical name from the top-level design to the cell
Dont Touch	Indicates when a <code>dont_touch</code> attribute is set on the cell, instance, or reference

For pins and ports, the table columns provide the following information:

Column	Description
Pin Name	Object (short) name for the pin within the design
Pin Full Name	Full hierarchical name from the top-level design to the pin

For nets, the table columns provide the following information:

Column	Description
Net Name	Object (short) name for the net within the design
Net Full Name	Full hierarchical name from the top-level design to the net

## See Also

- [Logic Hierarchy Views](#)

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## Schematic Views

Schematic views are the primary tools for visualizing the design. You can use schematic views to analyze timing and logic in the optimized design and to gather information that can help you to guide later optimization operations. A schematic view shows graphic representations of design logic and timing paths in a design or subdesign.

You can create a schematic to

- Examine the logic elements (blocks and gates) and connectivity in the top-level design or a hierarchical cell
- Analyze timing problems by focusing on critical paths in your design
- Examine the power management cells in a multivoltage design

When you create a schematic that includes timing paths, the schematic shows the cells and nets on each path.

You can modify the viewing range and scale in a schematic view by using the interactive zoom and pan tools or the zoom and pan commands on the View menu. In addition, you can use the scroll arrows and scroll box in the schematic view window or the arrow keys on the keyboard to scroll vertically or horizontally through the schematic.

Initially, the full schematic is visible in the schematic view window. For details, see [Magnifying or Shrinking a View](#) and [Traversing a View](#).

**Note:**

Text does not appear in a schematic view when it is below a certain size in pixels. Use the zoom tools and zoom commands to magnify the view if necessary to see object names and annotations in a schematic.

You can select, highlight, and query objects in a schematic view. Objects that you select or highlight in a schematic view are automatically selected or highlighted in other views. This capability allows you to efficiently analyze the logic and timing aspects of your design.

By default, a schematic view displays timing paths and design logic in a flat, single-sheet schematic that can span multiple levels of hierarchy. Hierarchy crossing symbols (diamond shapes) indicate places where a path moves up or down a level in the hierarchy. Each timing path consists of the objects (cells, pins, and nets) that make up the path.

To focus on the area or objects that you need to examine in a schematic view, you can

- Hide or display buffer and inverter chains, buffer and inverter trees, or unconnected macro pins

You can hide chains or trees of buffers, inverters, and hierarchy crossings by collapsing them into abstract metacells. You can also collapse unconnected macro pins into metapins. For details, see [Displaying or Hiding Buffers and Inverters](#).

- Hide or display the contents of hierarchical cells or blocks
- Reorganize the schematic hierarchically and display boundaries for the top-level design and each hierarchical cell or block

In a multivoltage design with UPF power domains, you can color the boundaries based on the hierarchical power relationships of the design

In addition, you can

- Add or remove selected objects (cells, ports, or nets) in a schematic view
- Add fanin logic or fanout logic for selected objects
- Add the worst-case timing paths from, through, or to selected objects

The objects are added or removed only in the active schematic view. The netlist is not changed and other schematic views are not affected.

You can reverse and reapply changes that you make in a schematic view, such as adding logic, expanding a hierarchical cell, or displaying hierarchical boundaries. You can reverse the most recent action or sequentially reverse a series of actions. If you have reversed one or more actions, you can reapply the most recently reversed action or a series of actions.

You can customize a schematic view by setting options on the View Settings panel. You can change

- Object label or annotation visibility, text colors, or text sizes (click the Text tab)
- Object colors (click the Objects tab)
- The display style for highlighted timing paths (click the Settings tab)
- The color brightness

You can print the contents of the active schematic view or save an image of the view in a PDF or PostScript file for printing later from a UNIX or Linux shell.

If you change the netlist for a design (for example, by using netlist editing commands such as `change_link`) when a schematic view is open, the GUI immediately updates the schematic and maintains the current zoom level and pan position.

To open a schematic view,

1. Select the objects or timing paths that you want to display in the schematic.
  - To display the top-level design or a hierarchical block or cell, select its instance name in the hierarchy browser.
  - To display timing paths, design logic, or both, select the paths and design objects.
2. Click the  button on the Schematics toolbar, or choose Schematic > New Schematic View.

You can create a schematic of the power management cells in your design by choosing Power > All PM Cells Schematic. For details, see [Examining Power Management Cells](#).

**Note:**

You can also create schematics by using the `gui_create_schematic` command. For details, see the man page.

When you open a schematic view, a tab appears at the top of the workspace area, above the console. The tab displays the name of the top-level design. You can use this tab to return to the schematic view after working with other views.

A schematic can contain instances (cells), ports, pins, nets, buses, bus rippers, and hierarchy crossings. An instance can be a block (a hierarchical cell representing the top-level design or a subdesign) or a leaf cell. A hierarchy crossing indicates a place where a timing path traverses the design hierarchy. When you select or highlight a timing path, the schematic represents the path as a series of net connections between pins or a pin and a port.

When InfoTips are enabled, you can view information about an object by holding the pointer over the object. The object information appears in an InfoTip, which is a small, temporary box that displays information about the object at the pointer location. For details, see [Previewing Objects in Graphic Views](#).

- To select objects interactively, click the  button on the Mouse Tools toolbar or choose View > Mouse Tools > Selection Tool, and then click or drag the pointer around the objects that you want to select.

Selected objects are displayed in white with a thicker line width. Clicking in the background deselects all selected objects. For more details, see [Selecting Objects in Graphic Views](#).

- To highlight objects interactively, click the  button on the Mouse Tools toolbar or choose View > Mouse Tools > Highlight Tool, and then click or drag the pointer around the objects that you want to highlight.

You can also highlight specific objects or timing paths by selecting them and then clicking a button on the Highlight toolbar or choosing a command on the Highlight menu. In addition, you can highlight the critical path (the path with the worst slack in the current design) or the minimum or maximum delay path from, to, or through an object. For example, to highlight the critical path, which is the default path reported by the `report_timing` command, choose Highlight > Critical Path.

A highlighted object has a different color from the unhighlighted object. When you highlight a path, net connections appear in the highlight color to show the connections between the objects (pins or ports) on the path. For more details, see [Highlighting Selected Objects or Paths](#).

- To query an object interactively, click the  button on the Mouse Tools toolbar or choose View > Mouse Tools > Query Tool, and then click the object that you want to select.

The object information appears on the Query panel, which appears automatically if it is not already visible. You can set options on the Query panel to automatically or manually copy the information to the session transcript in the console log view. For more details, see [Querying Objects in Graphic Views](#).

To focus on the area or objects that you need to examine in a schematic view, you can

- Expand or collapse hierarchical cells

By default, a hierarchical cell appears as a collapsed metacell. You can expand the cell to display its contents or hide the contents of a hierarchical cell by collapsing it into a metacell. For details, see [Displaying or Hiding Buffers and Inverters](#).

- Expand or collapse buses

The collapsed nets are rendered in a darker blue with a thicker line width, and the pins are rendered in a darker green. For details, see [Expanding and Collapsing Buses](#).

- Display rectangular cell and power domain boundaries around each hierarchical set of objects.

You can also color the power domain boundaries based on the hierarchical power relationships of the design. For details, see [Viewing Cells Hierarchically](#).

- Traverse the design hierarchy within a schematic view by expanding into the schematic for any block (subdesign) at the next lower level of the hierarchy or by collapsing (from a subdesign) to the schematic for the (parent) hierarchical cell at the next higher level of the hierarchy. For details, see [Traversing the Design Hierarchy](#).

You can add or remove selected logic (cells, ports, or nets) in a schematic view. The objects are added or removed only in the active schematic view. The netlist is not changed and other schematic views are not affected. You can also add fanin logic, fanout logic, or worst-case timing paths in a schematic view. For more information, see the following topics:

- [Adding or Removing Selected Logic](#)
- [Adding Fanin or Fanout Logic](#)
- [Adding Worst Paths Through Objects](#)

When you add fanin logic, fanout logic, or timing paths, you can control whether the additions appear in the active schematic view or in a new schematic view. You can

- Add the logic or paths to the schematic in the active schematic view.
- Display only the selected objects and the additional logic or paths in the active schematic view.
- Add the logic or paths to the schematic and display it in a new schematic view.
- Display only the selected objects and the additional logic or paths in a new schematic view.

### See Also

- [Examining Hierarchical Cells](#)
- [Examining Timing Paths and Selected Logic](#)
- [Schematic Views](#)
- [Examining Synthetic Operators in GTECH Designs](#)
- [Changing Schematic Settings](#)
- [Printing Schematic Views](#)
- [Saving an Image of a Window or View](#)

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## The Command Console

When you start the tool and open the GUI, the command console is docked above the status bar by default. The console provides a command-line interface and two views; a log view that displays the session transcript (the default view) and a history view that displays the command history list.

You can use the console to

- Enter Design Compiler Tcl commands on the console command line
- View either the session transcript (log view) or the command history list (history view) by clicking the tabs above the command line
- Display an error message man page in the man page viewer by clicking the message number in the console log view
- Copy and edit or reuse commands
- Search for, select, and save commands or messages in the log view or the history view

You can open (or close) one console in each application window. When the console is open, you can dock it to the bottom or top of its window, or move it over or away from the window.

The console displays information about the commands you use during the session in the following views:

- Log view
- History view

To select a view, click the tab above the command line. The log view is displayed by default when you start the Design Vision tool or open the GUI.

You can copy text in the log view and paste it on the command line, the same way you would in a UNIX or Linux shell, by selecting the text with the left mouse button and pasting it with the middle button. You can also select commands in the history view and edit or reissue them on the command line.

You can display or hide the console, and you can increase or decrease its height. You can dock it to the top or bottom edge of the Design Vision window, or you can undock it and resize it or move it around or off its Design Vision window.

For information about the console, see the following sections:

- [Console Log View](#)
- [Console History View](#)
- [Console Command-Line Editing](#)

## See Also

- [Entering Tcl Commands in the GUI](#)

## Console Log View

The console log view displays a transcript of session information that includes the commands you have entered and the Design Vision output and messages resulting from your commands.

To view the session transcript, click the Log tab on the console.

The console displays the log view. This is the view that is visible on the console at the beginning of a session.

You can use this information to

- Check tool status after performing functions
- Troubleshoot problems that you encounter
- Look up information about past functions

You can reenter commands you have already used by copying them from the log view to the console command line.

The log view displays the commands you enter next to a boldfaced prompt. Warnings and error messages are noted with “Warning” or “Error” as the first word. If you need to see information not currently displayed in the display area of the log view, use the scroll bars to scroll through the session information.

You can choose commands on the Change options menu (on the right side of the console above the command line) to

- Find text in the transcript
- Select and copy text in the transcript
- Search the transcript for commands or messages
- Save the transcript, selected text, or just the error and warning messages in a text file

You can copy text in the transcript that you want to paste on the command line or in another application such as a text editor.

To select and copy text,

1. Select text by dragging the pointer over it.

To select all the text in the transcript, choose Change options > Select All.

2. Click and choose Copy.

You can also copy text and paste it on the command line by selecting the text and pasting it with the middle mouse button.

You can search the transcript for commands or messages, and you can set the types of text that you want the search mechanism to find.

To search the transcript,

1. (Optional) Set up the search criteria by enabling or disabling search options.
  - To control whether the search continues when it reaches the end of the transcript, click and choose Wrap Search.
  - To include or exclude commands, click and choose Search Commands.
  - To include or exclude error messages, click and choose Search Error Messages.
  - To include or exclude informational messages, click and choose Search Informational Messages.

Check marks appear on the Change options menu next to the commands for the search criteria that are enabled.

2. Choose one of the following commands:

- To search backward in the transcript, click and choose Find Previous or press the F3 key.
- To search forward in the transcript, click and choose Find Next or press Shift+F3.

The console highlights the previous or next instance of any text type you included in the search.

3. (Optional) To find the command or message repeat step 2.

You can save all the text in the transcript, save selected text, or save just the error and warning messages.

To save text from the transcript in a text file,

1. Choose one of the following commands:

- To save the transcript, click and choose Save Contents As.
- To save selected text, drag the pointer over the text to select it, and click and choose Save Selection As.
- To save error and warning messages, click and choose Save Errors/Warnings As.

2. In the dialog box that appears, navigate to the directory where you want to save the file.

3. Enter the file name in the File name text box.

4. Click Open.

### See Also

- [Entering Tcl Commands in the GUI](#)
- [Console](#)

## Console History View

The console history view lists shell, menu, and dialog box commands you have used in the current session. You can use the history view in the following ways:

- See which commands you have used
- Find and reuse commands you have already used
- Copy commands in the list
- Save the list for later use

If you need to see information not currently displayed in the display area of the history view, use the scroll bars to scroll through the list of commands. Alternatively, you can enter the `history` command on the command line to display the list of commands in the log view.

To view the list of commands used during the session, click the History tab in the console.

The console changes to the history view.

Each command you use, whether from a menu or dialog box or on the command line, is added to this list.

If you select one or more commands in the list, you can

- Copy the commands to the command line, where you can edit them
- Rerun the commands

You can use Shift-click or Control-click to select multiple commands. Design Vision numbers the selected commands. If you need to reorder the commands, Control-click each command in the order you want to enter them on the command line.

To copy a selected command to the command line for editing,

1. Select the command.
2. Click the Edit button.

To rerun a command,

1. Select the command.
2. Click the Execute button.

Alternatively, you can rerun a command by double-clicking it.

To save the command list in a Tcl script file,

1. Click the Save Contents As button

Alternatively, you can click and choose Save Contents As. To save just the selected commands, select the commands in the command list, click and choose Save Selection As.

2. In the dialog box that appears, navigate to the directory where you want to save the file.
3. Enter the file name in the File name text box.
4. Click Open.

You can set options in the Application Preferences dialog box to control which types of GUI commands are included in the history list. For information about GUI preferences, see [Setting GUI Preferences on page 67](#).

## See Also

- [Entering Tcl Commands in the GUI](#)
- [Console](#)

## Console Command-Line Editing

You can display, edit, and reissue commands on the console command line by using the arrow keys to scroll up or down the command stack and to move the insertion point to the left or right on the command line. You can copy text in the log view and paste it on the command line the same way you would in a UNIX or Linux shell, by selecting the text with the left mouse button and pasting it with the middle button. You can also select commands in the history view and edit or reissue them on the command line.

You can enter dc\_shell commands on the console command line just as you would enter them in dc\_shell. When you enter a command, Design Vision tool echoes the command output (including processing messages and any warnings or error messages) in the console log view.

To enter a command on the console command line,

1. Make sure the console is the active view (has the mouse focus).
2. Enter the command.
3. Click the prompt button, or press Enter.

If you need to enter a command or Tcl procedure that uses multiple lines, you can expand the command line vertically by either typing a backslash (\) at the end of a line and pressing Return or clicking in the command line and pressing Shift+Return. The command line automatically shrinks to a single line when you issue the command.

To expand the command line to display multiple lines,

- Press Shift+Return or enter a backslash (\) at the end of the line and press Enter.

To shrink the command line to display a single line, press Control+Enter.

You can display, edit, and reuse commands on the console command line by using the arrow keys to scroll up or down the command stack and to move the insertion point to the left or right on the command line.

- To scroll up to the previous command in the command stack, press the Up Arrow key (or press Shift-Up Arrow when the command line displays multiple lines).
- To scroll down to the next command in the command stack, press the Down Arrow key (or press Shift-Down Arrow when the command line displays multiple lines).
- To move the insertion point to the left, press the Left Arrow key (or press the Home key to move the insertion point to the beginning of the line).
- To move the insertion point to the right, press the Right Arrow key (or press the End key to move the insertion point to the end of the line).
- To complete a partial command, option, or file name, press Tab.
- To display a list of command options, enter the command name followed by a blank space and press Tab.
- To issue a command, press Enter.

## The Script Editor

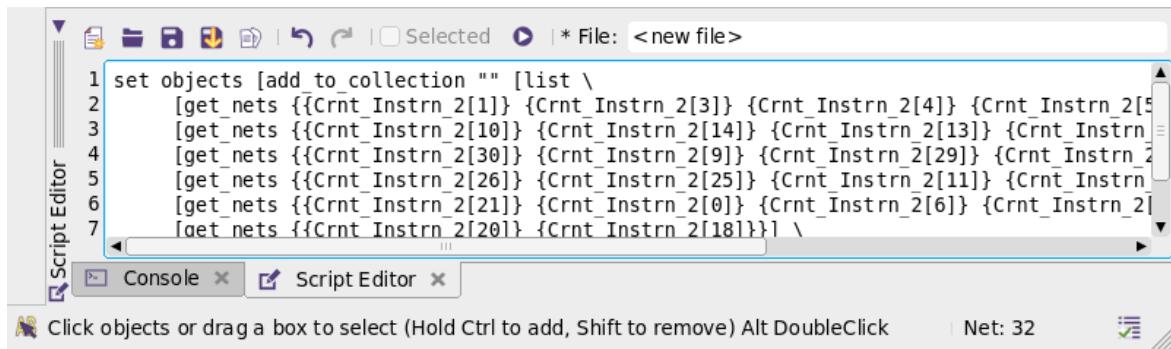
The Script Editor provides an interface that enables you to generate, edit, or execute scripts.

To display the Script Editor,

- Choose View > Toolbars > Script Editor.

The Script Editor appears, as shown in [Figure 5](#).

*Figure 5      Script Editor*



---

## Configuring the GUI

The following topics explain how to configure the Design Vision GUI:

- [Setting GUI Preferences](#)
- [Saving and Restoring View Settings](#)
- [Adjusting the Color Brightness](#)
- [Opening Application Windows](#)
- [Rearranging View Windows](#)
- [Moving Windows](#)
- [Resizing Windows](#)
- [Closing Windows](#)
- [Displaying or Hiding Toolbars and Pane](#)
- [Moving Toolbars](#)
- [Moving Panels](#)
- [Resizing Panels](#)
- [Displaying or Hiding the Status Bar](#)
- [Widening the Status Bar](#)

### See Also

- [Starting the Tool](#)

## Setting GUI Preferences

At the beginning of the GUI session, the tool loads GUI preferences from your preferences file. The default system preferences are set for optimal tool operation and work well for most designs. However, if necessary, you can change GUI preferences during the session. You can set preferences that control how text appears in GUI windows and whether commands for selection or interactive operations appear in the session log. You can also set various global, schematic view, and layout view default controls.

To set GUI preferences,

1. Choose View > Preferences.

The Application Preferences dialog box appears.

2. Select a category in the Categories tree.

The page for that category appears.

3. Set options as needed.
4. (Optional) To set options in a different category repeat steps 2 and 3.
5. Click OK or Apply.

When you change preference settings during a GUI session, choose Save in the Application Preferences dialog box, to save the new preferences settings in the preferences file named ..synopsys\_dc\_gui/preferences.tcl in your home directory. The next time you start the Design Vision tool or open the GUI, it loads the preferences from this file.

## See Also

- [Changing Schematic Settings](#)
- [Changing Layout Display Properties](#)

## Changing GUI Font Styles

You use the Application Preferences dialog box when you need to change global fonts in the GUI. You can change font characteristics used to display

- Variable-width text on application window elements (such as menus, dialog boxes, and buttons)
- Fixed-width text in text views (such as the console and report views)

To change global font characteristics,

1. Choose View > Preferences.  
The Application Preferences dialog box appears.
2. Select Style Settings in the Categories tree.  
The Style Settings page contains options you can use to change the fonts used in the Design Vision window and to enable or disable some automatic capabilities.
3. In the Fonts section:
  - Click Normal to open the Select Font dialog box, for variable-width text used on application window elements.
  - Click Monospaced font to open the Select Font dialog box, for fixed-width text used in text views.
4. Select options as needed.

You can select a font family, a font style (roman, bold, italic, or bold oblique), a font size, and a character set.

5. Click OK.
6. (Optional) To change other font characteristics repeat steps 3 through 5.
7. Click OK or Apply.

### Setting Global Default Preferences

Use the Application Preferences dialog box when you need to change global default settings for the GUI. You can

- Control how object selection operations are treated in the session log (console log view)
- Control how interactive operations in graphic views (interactive `gui_*` commands) are treated in the command log (console history view)
- Enable or disable automatic cycling through the highlight colors
- Enable or disable the display of error alert message boxes
- Configure new histogram view windows to display the object table to the right of the bar graph (the default) or below it

To change global default preferences,

1. Choose View > Preferences.  
The Application Preferences dialog box appears.
2. Select Global Settings in the Categories tree.
3. On the Global Settings page, set options as needed.
  - To enable the logging of selection operations, select the Selection option. This option is deselected by default.
  - To enable the logging of interactive operations, select the GUI option.
  - To increase or decrease the size of the command log, enter or select a value in the maximum number of log lines text box. The default is 10000.
  - To disable the automatic cycling of highlight colors in schematic and layout views, deselect the Automatically increment highlight color option. This option is selected by default.

- To prevent the GUI from displaying error alert message boxes, deselect the Show Errors dialog box option. This option is selected by default.
  - To set the relative position of the object list in new histogram view windows, select a Histogram list position option. The choices are Right and Below. The default is Right.
4. Click OK or Apply.

### See Also

- [Controlling the Highlight Color](#)

## Saving and Restoring View Settings

If you change display properties in a schematic, layout, or UPF diagram view, and you want to use them in another view of the same type or during a future session, you can save them in your preferences file. You can also restore previously saved display properties by loading them from your preferences file.

### Note:

Design Vision does not automatically save display properties when you close the GUI or exit the session.

On the View Settings panel, perform the following options to save and restore the settings,

- To save the current display properties from the active schematic or UPF diagram view, choose Show Options  > Preferences > Save to Preferences.
- To load the display properties from your preferences file, choose Show Options  > Preferences > Set from Preferences.
- To save the current display properties from the active layout view, choose Show Options  > Preferences > Save to Preferences.
- To load the display properties in the active layout view, choose Show Options  > Preferences > Set from Preferences.

You can also export the current display properties to a Tcl script.

To save the current display properties in a Tcl script,

1. Open the Write Settings Script dialog box.
  - For a schematic or UPF diagram view, click  > Write Settings Script.
  - For a layout view, click and choose Write Settings Script.
2. Select a file or enter a file name.
3. Click Save.

#### See Also

- [Changing the Appearance of the Layout View](#)
- [Changing UPF Diagram Display Properties](#)

## Adjusting the Color Brightness

You can use the View Settings panel to control how bright the colors appear in a graphic view such as a schematic or layout view. The default brightness is 100 percent.

For example, when you display the congestion map or a visual mode, the GUI dims the visible objects in the layout view. You can use the Brightness option on the View Settings panel to control the visual contrast between the map or visual mode colors and the other visible objects in the layout view. The GUI automatically dims the visible objects by resetting the color brightness to 33 percent.

To control the brightness in the active schematic or layout view,

1. Make sure the view you want to adjust is the active view.
2. Select an option in the Brightness list on the View Settings panel.

The choices are (in percent)

100  
75  
66  
50  
33  
25  
Off

3. Click Apply.

## See Also

- [Changing the Appearance of the Layout View](#)
- [Changing UPF Diagram Display Properties](#)

## Opening Application Windows

You can open multiple instances of GUI application windows and use them to compare different views side by side or to customize your working environment. When you open a new window, only the title bar, menu bar, toolbars, and status bar are visible.

The title bar displays the product name and the window name. The window name takes the form TopLevel.N, where N is a positive integer. When view windows are open in a GUI window, the title bar also displays the name of the active view in the form View\_type.N, where N is a positive integer.

Application windows that you open are numbered sequentially throughout the session. View windows that you open are also numbered sequentially throughout the session regardless of which GUI window they are in.

You can use multiple application windows to

- Compare different views, such as a histogram in one window and a schematic in another
- Compare different instances of a view, such as schematics focused on different parts of the design in each window
- Manage different tasks in individual windows, such as viewing reports or entering commands in one window and viewing timing or schematic information in another window

All application windows share the same designs currently loaded in memory, the same timing information, and the global selection data in the tool. When you open or close a view or change the current design, the change occurs in all open windows. Similarly, when you select or highlight objects, use a command (by choosing it in a menu or entering it on the command line), or run a script, the results are displayed in all open windows.

However, you can configure each window independently. For example, you can open different views (or different types of design information within a view) in each window. You can also hide, display, or rearrange the views, toolbars, and panels in an individual window.

To open a new Design Vision window,

- Choose Window > New Main Window.

To open a new layout window,

- Click the  button on the Layout toolbar, or choose Window > New Layout Window.

## Rearranging View Windows

You can arrange view windows by tiling or cascading them within the workspace area. You can also minimize, maximize, and restore individual view windows.

To tile the view windows in the workspace area, choose Window > Tile views.

To minimize a view window,

- Move the pointer over the window's title bar or its tab at the bottom of the workspace area.
- Right-click and choose Minimize.

To maximize a view window,

- Move the pointer over the window's title bar or its tab at the bottom of the workspace area.
- Right-click and choose maximize.

## Moving Windows

You can move an application window to change its location on the screen, or move a view window to change its location in the workspace area.

To move an application window,

- Move the pointer over the title bar.
- Drag the window to a different location on the screen.

To move a view window,

- Move the pointer over the title bar.
- Drag the window to a different location in the workspace area.

## Resizing Windows

You can control how much of the screen a window occupies by changing its height, width, or both. You use the same procedures to resize an application window or a view window.

To change a window's height,

1. Move the pointer to the top or bottom edge of the window.

The pointer changes to  for vertical resizing.

2. Drag the window edge up or down until it is the height you want.

To change a window's width,

1. Move the pointer to the right or left edge of the window.

The pointer changes to  for horizontal resizing.

2. Drag the window edge left or right until it is the width you want.

To change a window's height and width,

1. Move the pointer to a corner of the window.

The pointer changes to  for diagonal resizing.

2. Drag the window edge in or out until it is the size you want.

## Closing Windows

You can use commands in the Window menu to close view windows or top-level GUI windows.

To close the active view window,

- Choose Window > Close Window.

To close all open view windows,

- Choose Window > Close All Windows.

To close an application window,

- In the window you want to close, choose Window > Close View.

To close all open application windows,

- Choose Window > Close All Views.

If you close all the open application windows, you end the GUI session but you remain in the shell and your designs remain loaded in memory. You can reopen the GUI with a new Design Vision window by using the `gui_start` command.

### See Also

- [Opening and Closing the GUI](#)

## Displaying or Hiding Toolbars and Pane

You can enhance your viewing area by displaying or hiding individual toolbars or panels.

To display or hide a toolbar or panel,

1. Choose View > Toolbars.

A menu appears with the names of the toolbars and panels that you can display or hide: A check mark next to the name of a toolbar or panel on the Toolbars menu indicates that the toolbar or panel is visible.

2. Choose the name of the toolbar or panel you want to display or hide.

Alternatively, to hide a panel, you can move the pointer to the raised bars near the top or left edge of the panel, right-click, and choose Hide.

## Moving Toolbars

By default, the toolbars appear in a row at the top of the window below the menu bar. You can enhance your working environment by moving toolbars to different locations along the top, bottom, left, or right edge of the window. Toolbars are always attached to a window edge.

To move a toolbar to a more convenient location,

- Move the pointer over the raised bars near the left edge of the toolbar.

The pointer becomes the Move pointer ().

- Drag the toolbar to a different location.

## Moving Panels

When you work with a panel, you can enhance your working environment by moving panels to different locations inside or outside an application window. You can also dock or undock a panel by attaching it to an edge of the window or separating it from the window edge so that it floats inside or outside the window.

To move a panel,

1. Move the pointer over the raised bars near the top or left edge of the panel.
2. Drag the panel to a different location.

To attach a panel to a window edge,

1. Move the pointer over the raised bars near the top or left edge of the panel.
2. Right-click and choose Dock.

A menu appears with the names of the window edges to which the panel can be attached. The names of the other edges are dimmed (unavailable).

3. Choose a window edge.

To separate a panel from the window edge,

1. Move the pointer over the raised bars near the top or left edge of the panel.
2. Right-click and choose Float.

## Resizing Panels

You can control how much of the screen a panel occupies by changing its height, width, or both. You use the same procedures to resize a docked panel or a floating panel.

To change a panel's height,

1. Move the pointer to the top or bottom edge of the panel.
2. When the pointer changes shape, drag the panel edge up or down until it is the height you want.

To change a panel's width,

1. Move the pointer to the right or left edge of the panel.
2. When the pointer changes shape, drag the panel edge left or right until it is the width you want.

To change a panel's height and width,

1. Move the pointer to a corner of the panel.
2. When the pointer changes shape, drag the panel edge in or out until it is the size you want.

## Displaying or Hiding the Status Bar

You can control the visibility of the status bar at the bottom of an application window.

To display or hide the status bar,

- Choose View > Status Bar.

A check mark next to the Status Bar command on the View menu indicates that the status bar is visible.

## Widening the Status Bar

If you cannot read the full text displayed on the status bar at the bottom of an application window, you can widen the status bar by widening the window until the full text is visible.

To widen the window and the status bar,

1. Move the pointer to the right or left side of the window.
2. When the pointer shape changes, drag the window edge until the status bar is wide enough to view the entire message.

---

## Getting Help in the GUI

The GUI provides a variety of user-assistance tools. The following online information resources are available while you are using the Design Vision tool:

- Command help, which is a list of options and arguments used with a specified `dc_shell` command, displayed in the shell and in the console log view when the GUI is open
- Man pages displayed in the shell and in the console log view when the GUI is open
- A man page viewer in the GUI that displays command, variable, and error message man pages that you request while using the GUI
- A report that lists the keyboard shortcuts you can use in the GUI
- An online Help system in a Web browser that explains how to use the GUI

For information about using these tools, see the following topics:

- [Getting Help on the Command Line](#)
- [Displaying the List of Keyboard Shortcuts](#)
- [Accessing Man Page Viewer](#)
- [Viewing the Help System](#)

---

## Getting Help on the Command Line

The GUI provides three levels of command help on the console command line:

- A list of commands
- Command usage help
- Topic help

To get a list of all Tcl commands, enter the command:

```
prompt> help
```

To get help about a particular Tcl command, enter the command name with the `-help` option. The syntax is

```
prompt> command_name -help
```

To get topic help for a Tcl command, variable, or variable group, enter

```
prompt> man topic
```

Replace *topic* with the name of a Tcl command, variable, or variable group. By using the `man` command, you can display the man pages for the topic while you are interactively running the tool. In the GUI, you can view topic help in the man page viewer by choosing Help > Man Pages. For information about viewing man pages, see [Accessing Man Page Viewer on page 79](#).

### See Also

- [Entering Tcl Commands in the GUI](#)

## Displaying the List of Keyboard Shortcuts

You can view a report of the keyboard shortcuts for Tcl commands and commands on menus in the active window. The tool displays the shortcut keys report in a report view.

To display the report of keyboard shortcuts for the active window,

- Choose Help > Report Hotkey Bindings.

The report contains the following columns:

- Hot Key: Lists the keyboard shortcuts or key combinations
- Type: Indicates whether the key is a shortcut for a menu command or a Tcl command
- Action Name or Function: Lists the commands that the shortcut keys launch

### See Also

- [Choosing Menu Commands in GUI Windows](#)

---

## Accessing Man Page Viewer

The Design Vision GUI provides the HTML-based browser window to view, search, and print man pages for commands, variables, and error messages. For information, see the following topics:

- Display a man page ([Viewing Man Pages](#)).
- Browse back and forth between man pages you have already viewed ([Browsing Between Pages](#)).
- Search for text on the man page you are viewing ([Searching for a Word or a Phrase](#)).
- Print the man page you are viewing ([Printing Current Page](#)).

## Viewing Man Pages

To view a man page in the man page viewer,

1. Choose Help > Man Pages.

The Man Page Viewer appears. The home page displays a list of links for the different man page categories.

2. Click the category link for the type of man page you want to view.

The choices are Commands, Application Options, and Error Messages. The contents page for the category displays a list of title links for the man pages in that category.

3. Click the title link for the man page you want to view.

You can also display man pages in the man page viewer by using the `man` command or the `gui_show_man_page` command on the console command line.

### Note:

If you enter the `gui_show_man_page` command in the shell when the GUI is closed, the tool automatically opens the GUI and displays the man page in the man page viewer.

## Browsing Between Pages

You can browse back and forth between pages you previously viewed the same way you browse Web pages in a Web browser, using the following buttons:

- : Go back one page (to the last page you viewed)
- : Go forward one page (to the page you viewed before clicking  button)

-  Reload the current page
-  Go back to the initial contents page
- Select the page name in the File list to view any page viewed during the current viewer session

## Searching for a Word or a Phrase

To search for text on the current page,

1. Click the Find  button to open the Search text box.  
Enter a word or phrase in the Search text box.
2. Click the down arrow at the right of the search texr box to view the search history.
3. To distinguish between uppercase and lowercase characters, select the Find Case Sensitive option.
4. To search in a particular search direction, select Find Prev or Find Next options.
5. The man page viewer highlights (in reverse video) the first instance that it finds of the specified word or character string.
6. Click the Find  button.
7. (Optional) To search for another word or character string repeat steps 2 through 4.

You can use the search mechanism to find words or phrases in a man page.

## Printing Current Page

To print the current page,

1. Click the Print  button to open the Print dialog box.  
You can send the man page to a printer or save it in a file.
2. Select a print destination in the Name list.
  - To print the man page, select a printer name.  
The name of your default printer appears in the Name list by default.

- To save a PDF version of the man page in a file that you can view or print later in Adobe Acrobat, select Print to File (PDF) option in the Name list, and then enter a file name in the Output file text box.
  - To save a PostScript version of the man page in a file you can print later, select Print to File (Postscript) in the Name list, and then enter a file name in the Output file text box.
3. Set printer properties and options as needed.
  4. Click Print.

For more details about using the Print dialog box, see [Printing Schematic Views](#).

---

## Viewing the Help System

Synthesis Online Help is a browser-based HTML Help system that provides detailed information and instructions for using the GUI. You can use Design Vision Help to

- Learn about tool features, including windows, views, toolbars, panels, menus, and dialog boxes
- Learn how to use the interactive visualization and analysis tools
- Learn how to use the Design Vision tool to perform synthesis tasks

You can open Synthesis Online Help from the GUI or standalone in your Web browser. When you open the Help system from the GUI, the browser executable file must be specified in your UNIX or Linux \$PATH variable.

# 3

## Using Visual Analysis Tools

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The Design Vision GUI provides a variety of tools that you can use to visualize design data and analyze results for the Design Compiler, DC Explorer, TestMAX DFT, and Power Compiler tools. The GUI also supports the Design Compiler topographical technology. In the Design Compiler Graphical tool, the GUI provides visual analysis tools that helps you to analyze and debug physical problems related to Design Compiler topographical synthesis. Before you start using the GUI to analyze and troubleshoot a design, you should become familiar with the operations of the GUI and the various tools that it provides.

To learn the general and specific information you need to know before you use the Design Vision tool for the first time, see the following topics:

- [Exploring the Design](#)
- [Analyzing RTL](#)
- [Analyzing Design Timing](#)
- [Creating Path Data Histograms](#)
- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Using DFT Analysis Tools](#)
- [Generating and Implementing UPF Power Domains](#)
- [Using the Visual UPF Dialog Box](#)
- [Examining Power Management Cells](#)
- [Viewing PG Pin Information for Selected Cells](#)
- [Querying the Supply Nets of Selected Pins](#)
- [Defining and Viewing the Power Intent for Multivoltage Designs](#)
- [Analyzing Multivoltage Design Problems](#)
- [Printing the UPF Diagram View](#)

- [UPF Diagram Symbols and Standards](#)
  - [Changing UPF Diagram Display Properties](#)
- 

## Exploring the Design

You can use the hierarchy browser (logic hierarchy view) and schematic views to explore the design and examine design information. You can also select objects that you want to examine with other analysis tools. You can view information about design objects as follows:

- Select an object and view its properties in the Properties dialog box
- View object information in object list views
- View object reports that you generate by choosing commands on the Design and Timing menus

You can view a list of the selected objects in the Selection List dialog box. It displays the names and object types of all the objects in the current selection. When you select objects in other views, their names automatically appear in the selection list.

For more information about these capabilities, see the following topics:

- [Browsing the Design Hierarchy](#)
  - [Examining Hierarchical Cells](#)
  - [Examining Synthetic Operators in GTECH Designs](#)
  - [Viewing and Selecting Objects](#)
  - [Viewing the Selection List](#)
  - [Filtering Object Lists](#)
  - [Viewing and Editing Object Properties](#)
  - [Creating and Editing Attribute Groups](#)
  - [Specifying Path Startpoints, Throughpoints, and Endpoints](#)
- 

## Browsing the Design Hierarchy

You can use the logic hierarchy view to browse the complete hierarchical structure of the current design and observe how many hierarchical blocks are present, the size of each block, and whether any DesignWare components have been inferred (used). If you are not familiar with a design, you can explore the design hierarchy to understand its structure and gather information about objects (cells, nets, or pins) in the design. You can also select the

names of designs or objects you want to examine in graphic views or with other analysis tools.

At the beginning of a Design Vision session by default, the logic hierarchy view is open below the toolbars on the left side of the Design Vision window. You can open additional logic hierarchy views anytime during the session.

To open a logic hierarchy view, choose Hierarchy > New Logic Hierarchy View.

When you open a new logic hierarchy view, a tab appears at the top of the workspace area, above the console. You can use this tab to return to the logic hierarchy view after working with other views.

The view window consists of two panes: an instance tree on the left and an object table on the right. When you read in a design, the instance name of the top-level design appears in the left pane.

To explore the design hierarchy,

- Select the names of hierarchical blocks (instances that contain subblocks) to display information about the cells in the block.
- Click the expansion buttons next to the names of hierarchical blocks to further expand the instance tree.
- Use the arrow keys to navigate the instance tree.

Press the Up Arrow and Down Arrow keys to move up or down the tree, the Right Arrow key to expand a cell and the Left Arrow key to collapse a cell.

You can select objects in the instance tree or the object table that you want to examine with other analysis tools. The objects you select are automatically selected in other views. For example, if you want to examine a schematic representation of a hierarchical cell, select the cell in the hierarchy browser and choose Schematic > New Schematic View. For details about using schematics, see [Examining Hierarchical Cells](#).

By default, the object table contains cell information. You can select an object type in the list above the table to display information about hierarchical cells, all cells, pins, pins of child cells, or nets.

- Cell information includes the cell instance names, the reference names of the designs the cells reference, the paths from the top-level designs to the cells, and the values of the `dont_touch` attribute.
- Pin information includes the pin and port names and the paths from the top-level design to the pins and ports.
- Net information includes the net names and their paths from the top-level design.

You can sort the object table and resize columns in the table. You can also filter the table, limiting it to information based on a character string or regular expression that you define.

To sort the object table,

1. Move the pointer into the heading of the column you want to sort.
2. Click the column heading when the pointer changes shape.

Click again if you want to reverse the sort.

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the column widths.

To resize a column in the object table,

1. Move the pointer over the right edge of the column you want to resize.
2. Drag the column edge right or left to increase or decrease the width of the column when the pointer changes shape.

You can also filter the object table, limiting it to information based on a character string or regular expression that you define. For details, see [Filtering Object Lists](#).

You can use the Up Arrow and Down Arrow keys to scroll up or down in the table.

## See Also

- [Logic Hierarchy Views](#)

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## Examining Hierarchical Cells

You can use schematic views to examine logic connectivity and timing paths in the optimized design and to gather information that can help you to guide later optimization operations. Schematic views show graphic representations of design logic and timing paths in your design.

A schematic view displays the design objects and timing paths in a flat, single-sheet schematic that can span multiple hierarchy levels.

- A schematic can contain instances (cells), ports, pins, nets, buses, bus rippers, and hierarchy crossings.

An instance can be a block (a hierarchical cell representing the top-level design or a subdesign) or a leaf cell.

- A hierarchy (diamond shape) crossing indicates a place where a timing path traverses the design hierarchy.
- A selected or highlighted timing path appears as a series of net connections between pins or a pin and a port.

To create a schematic of the top-level design or a hierarchical cell,

1. Select the cells that you want to view.

You can select the cells in another timing analysis tool, such as the path inspector or a path data table.

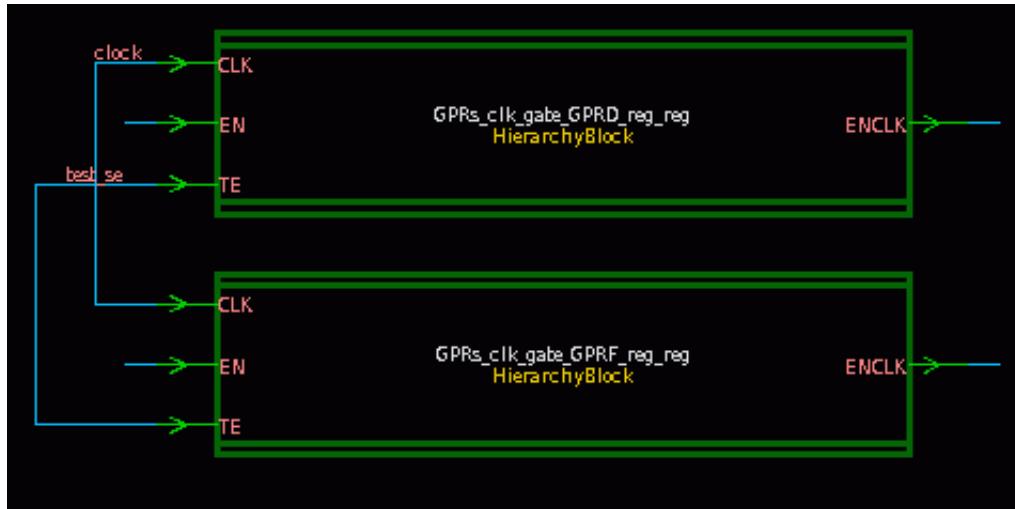
You can also choose **Select > Paths From/Through/To** and set options in the **Select Paths** dialog box.

2. Click the  icon on the Schematics toolbar, or choose **Schematic > New Schematic View**.

When you create a schematic that contains hierarchical cells, the cells initially appear as collapsed metacells. For a set of objects that have a common hierarchical parent, the hierarchy metacell is similar to a design cell but has a thicker line width and a different color.

The following figure shows an example of a schematic with two hierarchical cells collapsed into metacells.

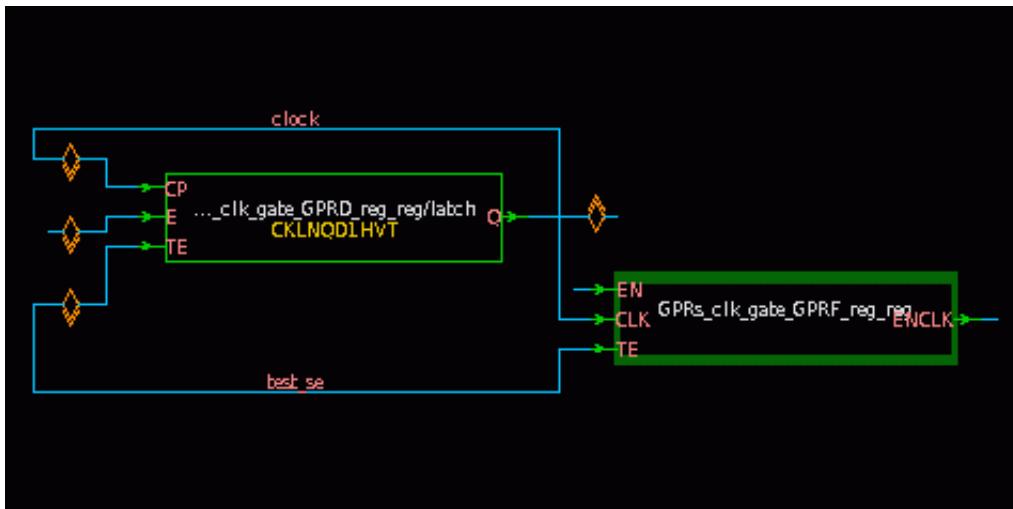
**Figure 6      Hierarchical Metacells**



You can expand a hierarchy metacell to display the objects in the next hierarchy level. If it includes further levels of hierarchy, they appear as metacells.

The following figure shows the same schematic with one hierarchical cell expanded to display its contents.

*Figure 7      Expanded Hierarchical Cell*



To expand all the hierarchical cells in the active schematic view, choose Schematic > Expand > All Hierarchy.

To expand individual hierarchical cells,

1. Select hierarchy metacells that you want to expand.
2. Click the  icon on the Schematics toolbar, or choose Schematic > Expand > Selected Objects.

Alternatively, you can double-click the metacells.

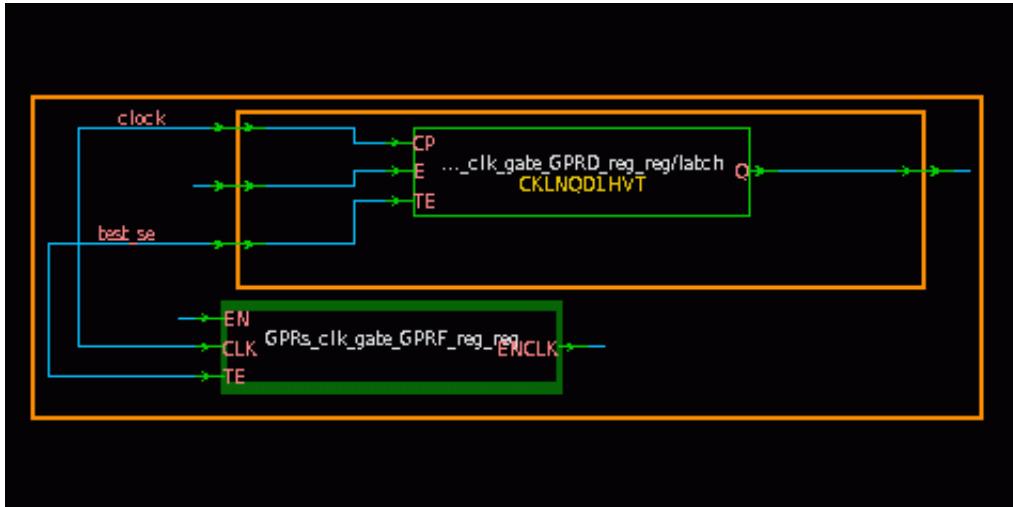
A hierarchy metacell expands to display the objects in the next hierarchy level. If it includes further levels of hierarchy, they appear as metacells. Buffer and inverter metacells expand to display the path containing the buffers, inverters, and hierarchy crossings.

By default, a schematic displays the objects with input ports on the left and output ports on the right. You can reorganize the schematic hierarchically and display rectangular boundaries for the top-level design and each hierarchical set of objects.

You can reorganize the schematic hierarchically and display rectangular boundaries for the top-level design and each hierarchical set of objects.

The following figure shows an example of a schematic organized hierarchically with visible boundaries.

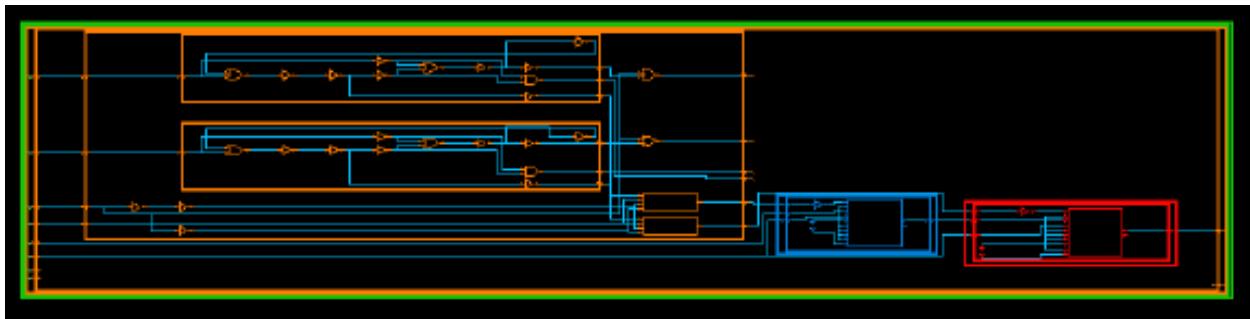
*Figure 8 Hierarchical Cell Boundaries*



The tool rearranges the schematic so that objects are placed hierarchically, which puts objects that share the same hierarchical parent near each other. The logic hierarchy boundaries are orange, and the power domain boundaries are yellow.

In a multivoltage design with UPF power domains, you can color the boundaries based on the hierarchical power relationships of the design. The following figure shows an example of a schematic organized hierarchically with colored boundaries.

*Figure 9 Colored Power Domain Boundaries*



You can also traverse the design hierarchy within the schematic view by expanding the schematic for a block (subdesign) at the next lower level of the hierarchy or by collapsing (from a subdesign) into the schematic for the hierarchical (parent) cell at the next higher level of the hierarchy.

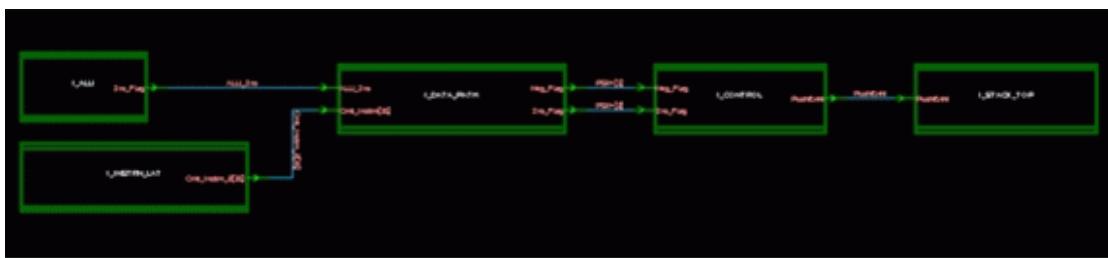
In addition, you can

- Hide or display long chains or trees of buffers, inverters, and hierarchy crossings
- Hide or display unconnected macro pins

- Collapse or expand bus nets and pins
- Add or remove selected objects or add fanin logic, fanout logic, or timing paths for selected objects
- Trace fanin or fanout connections with highlighting for selected cells, pins, or ports

To hide all the hierarchical cells in the active schematic view, click the  button on the Schematic toolbar, or choose Schematic > Collapse > All Hierarchy.

For a set of objects that have a common hierarchical parent, a metacell is similar to a design cell but has a thicker line width and a different color. The following example shows a schematic with the hierarchical cells collapsed into metacells:



To hide individual hierarchical cells,

1. Select objects in the hierarchical cells that you want to hide.
2. Click the  icon on the Schematics toolbar, or choose Schematic > Collapse > Selected Hierarchy By Parent.

To facilitate your analysis of a multivoltage design, you can display rectangular cell and power domain boundaries around each hierarchical set of objects. You can also color the power domain boundaries based on the hierarchical power relationships of the design. For details, see [Viewing Cells Hierarchically](#).

Alternatively, you can traverse the design hierarchy within a schematic view by expanding the schematic for any block (subdesign) at the next lower level of the hierarchy or by collapsing (from a subdesign) to the schematic for the (parent) hierarchical cell at the next higher level of the hierarchy. For details, see [Traversing the Design Hierarchy](#).

You can reverse and reapply changes that you make in a schematic view, such as adding logic, expanding a hierarchical cell, or displaying hierarchical boundaries. You can reverse the most recent action or sequentially reverse a series of actions. If you have reversed one or more actions, you can reapply the most recently reversed action or a series of actions.

## Traversing the Design Hierarchy

You can traverse the design hierarchy within a schematic view by expanding the schematic for any block (subdesign) at the next lower level of the hierarchy or by

collapsing (from a subdesign) to the schematic for the (parent) hierarchical cell at the next higher level of the hierarchy.

To expand a level in the design hierarchy,

1. Select a hierarchical cell in the schematic.

Alternatively, you can select a hierarchical cell in the logic hierarchy view, and then click in the title bar on the schematic view window to make it the active view.

2. Choose Schematic > Expand.

Alternatively, you can double-click the hierarchical cell in the schematic.

To collapse a level in the design hierarchy, Choose Schematic > Collapse.

**Note:**

When you expand or collapse into a different schematic, Design Vision tool changes the design name displayed on the tab for the schematic view window.

## Examining Synthetic Operators in GTECH Designs

Schematic views generate standard symbols to display synthetic operators in a GTECH netlist. These operator symbols can help you to identify the associated functions and to analyze and debug operators and datapaths. The same symbols are used for both signed and unsigned operators.

These symbols are generated automatically for the following operators, with the appropriate drawing geometry and pin sets to match the specific cell:

- Add (+), subtract (-), multiply (x), and divide (/) operators
- Less than (<), greater than (>), equal to (=), and not equal to (/=) operators
- Less than or equal to (<=) and greater than or equal to (=>) operators
- Multiplexor and selector operators

These operator symbols can help you to identify the associated functions and to analyze and debug operators and datapaths. The same symbols are used for both signed and unsigned operators.

The symbols appear only in GTECH designs. They are not visible in synthesized designs even when the operator hierarchies are preserved and are not supported for instantiated DesignWare modules.

**Note:**

The REM\_UNS\_OP operator (%) is not supported. It appears as a rectangle.

## See Also

- [Schematic Views](#)
- [Examining Hierarchical Cells](#)

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## Viewing and Selecting Objects

Design Vision tool provides a variety of views that you can use to examine and analyze your design. These include graphic views, hierarchy views, and textual views.

- Graphic views let you visually examine
  - Design timing in histograms and schematics
  - Design logic in schematics
  - UPF power architecture in the UPF diagram view and the Visual UPF dialog box
  - Physical design objects in layout views, congestion maps, and visual modes
- The logic hierarchy view lets you explore the design hierarchy and examine the objects within a design instance or hierarchical cell.
- The timing status summary lets you examine timing path details.
- Path inspector windows let you inspect the clock and data path elements that comprise a timing path.
- List views let you examine, sort, and filter lists of various types of design objects.
- Report views let you examine the contents of various design and timing reports.

You can locate objects in a graphic view by selecting them in a different view. For example, to locate objects in a schematic view, you can select them in the logic hierarchy view. The selected objects appear with the selected color, which is white by default, in all open schematic views. For details, see [Browsing the Design Hierarchy](#).

You can cross-select objects between logic and physical views. When you select an object in one schematic or layout view, it is automatically selected in all other schematic and layout views. For details, see [Selecting Objects in Graphic Views](#).

You can also locate objects in graphic views by selecting their names in a list or report view. When you select an object name in a list or report view, the object is automatically selected in all other views. For details, see [Viewing Object Lists](#) and [Viewing Reports](#).

You can highlight objects or timing paths that you need to continue viewing after you deselect them or select other objects. You can also select highlight objects. For details, see [Highlighting Objects or Timing Paths](#) and [Selecting Highlighted Objects and Paths](#).

## Viewing Object Lists

You can generate a list of objects (cells, nets, or ports and pins) and display information about them in a list view. You can display information about the following:

- Selected objects (such as selected cells)
- Objects related to other selected objects (such as pins of selected cells)
- Objects with a common function or attribute (such as fixed cells)

You can select some or all of the objects in a list by clicking or dragging the pointer across their names in the list view. You can also use Shift-click or Control-click to select multiple objects. In addition, you can

- Sort the information alphabetically by clicking a column heading. Click the heading again to reverse the sort.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define.

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over it to display the information in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

You can filter an object list, limit it to designs based on a character string or regular expression that you define, by using the Filter List dialog box. For more information, see [Filtering Object Lists](#).

### Opening a list of Cells

To open a list of cells,

- Choose List > Cell View.
- In the Cell View option, choose the collection of cells that you want to display in the list. The choices are:
  - Selected Cells
  - Of Selected Pins
  - Of Selected Logical Nets
  - Leaf Cells of Selected

## Opening a List of Ports and Pins

To open a list of ports and pins,

- Choose List > Ports/Pins View.
- In the Ports/Pins View menu, choose the collection of ports or pins that you want to display in the list. The choices are:
  - Selected Pins/Ports
  - Of Selected Nets
  - Of Selected Cells
  - All Ports
  - Input Ports
  - Output Ports
  - Clock Sources

## Opening a List of Nets

To open a list of nets,

- Choose List > Nets View.
- In the Nets View menu, choose the collection of nets that you want to display in the list. The choices are:
  - Selected Nets
  - Of Selected Pins/Ports
  - Of Selected Cells

## See Also

- [Cell Lists](#)
- [Port and Pin Lists](#)
- [Net Lists](#)

## Selecting a Collection of Objects

Design Vision tool allows you to select groups of one or more related objects. You can also select objects based on their connections to other selected objects.

You can select a collection of cells, a collection of pins and ports, or a collection of nets. The names of the selected objects appear in the selection list (see also [Viewing the Selection List](#)).

To select a collection of cells,

1. Choose Select > Cells.
2. On the Cells menu, choose the collection of cells you want to select. The choices are as follows:
  - Top Design
  - Leaf Cells of Selected
  - Of Selected Pins
  - Of Selected Logical Nets
  - Of Selected Paths

To select a collection of ports or pins,

1. Choose Select > Ports/Pins.
2. On the Pins/Ports menu, choose the collection of ports and pins you want to select.

The choices are

- All Ports
- Input Ports
- Output Ports
- Clock Sources
- Of Selected Nets
- Of Selected Cells
- Of Selected Paths

To select a collection of nets,

1. Choose Select > Nets.
2. On the Nets menu, choose the collection of nets you want to select.

The choices are

- Of Selected Ports/Pins
- Of Selected Cells

You can use the `get_selection` command to create a collection of the selected objects.

### See Also

- [Deselecting All Selected Objects](#)

## Selecting Timing Paths

You can select the paths with the worst slack in the current design or in a path group. You can also select individual timing paths to or from specific inputs, outputs, or registers.

The default path is the path with the worst slack in the current design. You can set options to

- Select paths from a specific path group.
- Select up to a maximum number of paths with the worst slack in the current design (or in the specified path group).
- Select up to a maximum number of paths to any single endpoint.

You can also select specific paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the only paths that are selected are those that start at a specified startpoint, end at a specified endpoint, or pass through one or more specified throughpoints. For details, see [Cross-Probing Selected Timing Paths](#).

By default, the paths are based on maximum delay times. This allows you to view path setup times. You can change the delay type option and base the paths on

- Minimum delay times (to view path hold times)
- Minimum rising delays
- Minimum falling delays
- Maximum rising delays
- Maximum falling delays

In addition, you can set options to

- Enable preset and clear arcs
- Include hierarchical pins

You can also select a selection bus and a selection operation.

The following procedures show how to select the path with the worst slack in the current design (or in a path group), select specific paths, and select multiple paths.

To select the path with the worst slack in the current design or in a path group,

1. Choose Select > Paths From/Through/To.  
The Select Paths dialog box appears.
2. To specify a path group, select its name in the Group name list.
3. (Optional) Change the delay type for the path by selecting an option in the Delay type list. The default (max) is set for maximum delays.
  - For minimum delays, select min.
  - For maximum delays, select max.
  - For maximum rising delays, select max\_rise.
  - For maximum falling delays, select max\_fall.
  - For minimum rising delays, select min\_rise.
  - For minimum falling delays, select min\_fall.
4. Select other options as needed.
5. Click OK or Apply.

To select the worst path to, from, or through a selected object,

1. Select the objects (pins, ports, nets, or clocks).
2. Choose Select > Paths From/Through/To.  
The Select Paths dialog box appears.
3. Enter the name of the selected object.
  - To select the worst path to an object, select an object type in the To drop-down list and click the Selection button.  
You can select paths to a pin, port, net, or clock.
  - To select the worst path from an object, select an object type in the From drop-down list and click the Selection button.  
You can select paths from a pin, port, net, or clock.
  - To select the worst path through an object, select an object type in the Through drop-down list and click the Selection button.  
You can select paths through a pin or net.

For more details, see [Cross-Probing Selected Timing Paths](#).

4. (Optional) Select the name of a path group in the Group name drop-down list.
5. Make sure the delay type you need is selected.
6. Select other options as required.
7. Click OK or Apply.

To select multiple paths,

1. Choose Select > Paths From/Through/To.  
The Select Paths dialog box appears.
2. Set options to control the maximum number of paths.
  - To change the maximum number of paths, enter a value in the Max paths box.
  - To change the maximum number of paths to an endpoint, enter a value in the Nworst paths box.
3. (Optional) Select paths to or from specific inputs, outputs, or registers by specifying their startpoints (From), throughpoints (Through), or endpoints (To).

First, select an object type. Startpoints and endpoints can be pins, ports, nets, or clock. Throughpoints can be pins or nets. Then, perform one of the following:

- Enter one or more object names
- Select one or more objects and click the Selection button
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#))

For more details about specifying paths, see [Cross-Probing Selected Timing Paths](#).

4. (Optional) Select the name of a path group in the Group name drop-down list.
5. Make sure the delay type you need is selected.
6. Select other options as needed. You can
  - Select only paths within a range of slack values, enter minimum and maximum slack values in the Path slack text boxes.  
You can enter a minimum slack value to set the lower bound, a maximum slack value to set the upper bound, or both.
  - Enable preset and clear arcs by selecting the Enable preset clear arcs option.
  - Include hierarchical pins by selecting the Include hierarchical pins option.

- Select a selection bus in the Selection bus list
  - Select a selection operation in the Selection operation list
7. Click OK or Apply.

#### See Also

- [Deselecting All Selected Objects](#)

## Selecting Fanin or Fanout Logic

You can select fanin or fanout paths for one or more selected objects. You can specify the start logic, the stop logic, and the number of logic levels to add.

To select fanin or fanout paths,

1. Select one or more design objects.
2. Choose Select > Fanin/Fanout.

The Select Fanin/Fanout dialog box appears. The names and types of the selected objects appear in the Start Logic table.

3. Select either the Fanin option (to add fanin logic) or the Fanout option (to add fanout logic). By default, Fanout is selected.
4. Select an option to specify the number of logic levels.
  - To select all logic levels, select the All levels option.
  - To select just one logic level, select the One level option.
  - To select any number of logic levels, select the N levels option and select or enter the number of levels in the N levels text box. The default is 2.
5. Edit the Start Logic list as needed.
  - To display different object names in the list, select the objects and click the Set Selected button.
  - To add object names to the list, select the objects and click the Add Selected button.

or

Click the Browse button and select the object name in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

- To remove object names from the list, select the object names and click the Remove button.
  - To remove all the object names from the list, click the Clear button.
6. (Optional) If necessary, click the Stop Logic tab and specify object names in the Stop Logic list.

When you specify stop-logic objects that are within the specified logic levels, each fanin or fanout cone ends at the first stop-logic object it encounters.

- To display object names in the list, select the objects, then click the Set Selected button.
  - To add object names to the list, select the objects and click the Add Selected button.
- or

Click the Browse button and select the object name in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

- To remove object names from the list, select the object names and click the Remove button.
  - To remove all the object names from the list, click the Clear button.
7. If you do not want the fanin or fanout cones to stop at sequential logic objects, deselect the Stop at sequential objects option.
8. Set other options as needed. You can
- Select a selection bus in the Selection bus drop-down list
  - Select a selection operation in the Selection operation drop-down list
9. Click OK or Apply and repeat steps 3 through 5 to add additional fanin or fanout paths.

## See Also

- [Deselecting All Selected Objects](#)

## Selecting Highlighted Objects and Paths

When you have highlighted design objects or timing paths in a schematic or layout view, you can select the highlighted objects and paths.

To select highlighted objects and paths in the active view,

- Choose Select > Highlighted.

If you need to select some but not all of the objects in an area of the layout view, you can enable a layout view constraint to select only highlighted objects. If you enable this option and then click or drag the Selection tool to select objects in the active layout view, the tool selects only those objects that are currently displayed with highlight colors.

To enable the constraint to select only highlighted objects in the active layout view,

1. On the View Settings panel, select the Only select highlighted option.
2. Click Apply.

A check mark appears on the option when the constraint is enabled.

## See Also

- [Following Selected Objects](#)
- [Selecting Objects in Graphic Views](#)
- [Deselecting All Selected Objects](#)

## Selecting Bus Objects

When a bus is selected, you can select the bits (nets) of the bus. In addition, when one or more bits of a bus are selected, you can select the bus.

To select the bits of a selected bus, choose Select > Objects of Selected Buses.

To select a bus from selected nets, choose Select > Buses of Selected.

## See Also

- [Following Selected Objects](#)
- [Selecting Objects in Graphic Views](#)
- [Deselecting All Selected Objects](#)

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## Viewing the Selection List

The selection list displays the names and object types of all selected objects in the current design. When you select objects in other views, their names automatically appear in the selection list.

To open the selection list, click the  icon at the right end of the status bar, or choose Select > Selection List, or choose List > Selection List. The Selection List dialog box contains a table with a row for each selected object and columns that display the object name, the object type, and certain attribute values for each selected object.

You can control which attributes appear in the table by selecting an attribute group. By default, the table displays values for the attributes in the Basic attribute group. To control which attributes appear in the selection list, select an attribute group name in the list at the bottom-left corner of the dialog box.

**Note:**

This list is available only when the objects in the selection list all have the same object type.

To open the Attribute Group Manager dialog box, click the Manage All  button in the Selection List dialog box. You can modify the contents of some predefined attribute groups and create or modify custom attribute groups by using the Attribute Group Manager dialog box.

For more information about attribute groups, see [Creating and Editing Attribute Groups](#).

You can deselect object names and remove their names from the selection list. You can also filter the selection list, limiting it to information based on a character string or regular expression that you define.

You can deselect objects (and remove their names from the list) by

- Selecting names in the list and clicking the Select button to deselect all other selected objects.
- Selecting names in the list and clicking the Deselect button to deselect those objects.

You can also filter the selection list, limiting it to information based on a character string or regular expression that you define. For details, see [Filtering Object Lists](#).

If you want to save the object or timing path information in the selection list, you can export the entire list to a text file. The file is formatted with each object or path on a separate line and the column data delimited by commas.

To save the selection list information in a text file,

1. Click the Export button to open the Export to File dialog box.
2. Select or enter the file name.
3. Click Save.

To close the selection list, click Close.

In addition to viewing the selection list, you can view a summary of information about all selected objects on the Query panel.

To display a summary of all currently selected objects, choose Select > Query Selection.

For details about using the Query panel, see [Querying Objects in Graphic Views](#).

**Note:**

If only one object is selected, choose Select > Query Selection to display the same information about the object that the Query tool displays.

**See Also**

- [Selection List \(Select Menu\)](#)
  - [Selecting Objects in Graphic Views](#)
  - [Querying Objects in Graphic Views](#)
- 

## Filtering Object Lists

Some windows, views, and dialog boxes display design objects or other design information in lists or tables. You can filter a list or table to display only the information in which you are interested.

To filter the list or table, you select the title of a column and specify a filter pattern of one or more characters. The filter displays only the rows for those items in the selected column that match the filter pattern (and hides all the other rows).

When you define the filter, you can

- Control if the filter pattern can include a regular expression
- Control if the filter pattern is case-sensitive
- Specify an inverse filter (hide the list items matched by the filter pattern and display all other items in the list)

A regular expression uses wildcard characters as placeholders to represent alphanumeric characters. You can use the question mark (?) wildcard character to represent a single character. Use the asterisk (\*) wildcard character to represent any number of consecutive characters (including zero). For example, U200\* finds all occurrences of cell names starting with U200 followed by any number of characters.

**See Also**

- [Viewing Object Lists](#)
- [Viewing the List of Designs in Memory](#)
- [Viewing the Selection List](#)
- [Browsing the Design Hierarchy](#)
- [Viewing High-Level Timing Results](#)

- [Examining Timing Path Details](#)
  - [Using DFT Analysis Tools](#)
- 

## Viewing and Editing Object Properties

You can view attributes and other object properties for selected designs, design objects, or timing paths by using the Properties dialog box. You can also set, change, or remove the attribute values for certain properties. For example, to view property values for a cell that you see in a schematic or layout view, you can select the cell and then choose Edit > Properties.

The Properties dialog box lists the object properties in a table with two columns (for property names and property values) and a row for each property.

**Note:**

The Properties dialog box displays properties for the objects that are currently selected. If you change the current selection when the Properties dialog box is open, the dialog box changes to display the properties for the newly selected objects.

The properties you can view include object names, attribute values, and certain timing and placement values. The list of properties differs from one object type to another. To control which properties appear in the Properties dialog box, you select an option in the Attribute group list.

**Note:**

Timing values do not appear until you perform an operation that updates timing information, such as generating a timing report or opening a histogram.

To open the Properties dialog box,

1. Select one or more objects.

You can select a single object, multiple objects of the same type, or multiple objects of different types.

2. Click the  icon on the File toolbar, or choose Edit > Properties.

The Properties dialog box appears, with the number of selected objects displayed above the property list table. The property values for the first selected object appear in the table.

**Note:**

The Properties dialog box displays properties for the objects that are currently selected. If you change the current selection when the Properties dialog box is

open, the dialog box changes to display the properties for the newly selected objects.

You can modify the contents of some attribute groups and create custom, user-defined attribute groups, by using the Attribute Group Manager dialog box. You can also view the contents of the predefined attribute groups.

To control which attributes appear in the Properties dialog box,

- Select an option in the Attribute group list.

To open Attribute Group Manager dialog box,

Click the Manage All  button in the Properties dialog box. For more details about attribute groups, see [Creating and Editing Attribute Groups](#).

If you select multiple objects, the property lists are displayed separately for each object. You can click the previous and next arrow buttons to navigate from one list of object properties to another.

- To display the property values for the next object, click the  icon.
- To display the property values for the previous object, click  icon.

Alternatively, you can select an option to list the property values for all the selected objects together in a single table

To display the properties for all selected objects, select the All option at the top of the Properties dialog box.

**Note:**

If you want to display properties for all objects of the same type, the dialog box shows the values that are identical for all the objects and displays <Multiple values> for other values. If you try to display properties for all objects of more than one type, the dialog box does not display any properties.

Some object properties are attributes that you can edit by changing or removing their values or by applying values if they are not already assigned. A bold border in the value column indicates an editable property value.

- To add or change a value in a list box, select the appropriate option in the list.  
Some lists include an option, such as undefined, to indicate that no value is assigned.  
To remove a value, select this option.
- To add or change a value in a text box, enter the new value. To remove a value, delete the value from the text box.

To apply the edits to the selected object, click OK or Apply.

You can copy the property information to the session transcript in the console log view and the shell by clicking the Log button.

Some object properties are attributes that you can edit by changing or removing their values or by applying values if they are not already assigned. A bold border in the value column indicates an editable property value.

You can control which attributes appear in the properties table. The attributes are organized into attribute groups. For most object types, you can display all attributes, which includes user-defined attributes, or application (predefined) attributes. For nets, pins, or ports, you can also display basic attributes, which are the most frequently used attributes for the object type, or timing attributes. For cells or designs, you can display basic attributes, timing attributes, or placement attributes.

The default attribute group depends on which type of object you select. If you select multiple objects of different types, only the attributes in the basic attribute group appear.

## See Also

- [Creating and Editing Attribute Groups](#)

## Creating and Editing Attribute Groups

Attribute groups are collections of attributes that the GUI uses to determine which attribute values to display in the Properties dialog box and the Selection List dialog box, in layout view InfoTips, and on the Query panel. The content of these groups varies depending on the object type. When you view or edit object properties in the Properties dialog box, you can control which types of attributes are visible in the properties list by selecting an attribute group.

You can view both application attribute groups that are predefined in the GUI and user-defined attribute groups that you create. The GUI provides the following predefined attribute groups:

Attribute group	Contents
All	All the application and user-defined attributes for an object
Application	All the attributes for an object that are predefined in Design Compiler
Basic	The most frequently used attributes for an object
LayoutInfoTipText	The attributes that appear in layout view InfoTips
QueryText	The attributes that appear on the Query panel

Attribute group	Contents
Placement	Placement attributes for cells or designs
Timing	Timing attributes for cells, designs, nets, pins, or ports
User	All the user-defined attributes for an object that you define by using the <code>define_user_attribute</code> command

The tool updates the All and User groups automatically when you create or remove a user-defined attribute.

To open the Attribute Group Manager dialog box,

- Click the  icon in the Properties dialog box.

To view the contents of an attribute group,

- Select an object type in the Object Class list.

The names of the attribute groups appear in the Attribute Groups list.

**Note:**

For port or pin attribute groups, select Pin in the Object Class list.

- Select a group in the Attribute Groups list.

The names of the attributes in the group appear in the Group Attributes list. The list displays a symbol against each attribute group name indicating if the attribute group is predefined in the GUI (A) or a user-defined attribute (U).

You can save attribute groups in your preferences file, load them from the preferences file, or reset the application attribute groups to their system defaults.

- To save attribute groups in your preference file, click Save.
- To restore attribute groups from your preferences file, click Restore.
- To reset attribute groups to their system default configurations, click Reset to system defaults.
- To close the Attribute Group Manager dialog box, click Close.

You can copy an existing attribute group to create a new user-defined attribute group with the same content, and then modify the group to meet the requirements. You can also rename an attribute group that you create.

To copy an attribute group,

1. Select the object type in the Object Class list.
2. Select the group in the Attribute Groups list.
3. Click Copy.

The name of the copy appears in the Attribute Groups list. This name consists of the name of the original group with \_copy appended at the end.

To rename an attribute group,

1. Select the object type in the Object Class list.
2. Select the group in the Attribute Groups list.
3. Click Rename.
4. Edit the name as required in the Attribute Groups list.

You can create, modify, and remove your own attribute groups.

You can create a new attribute group by specifying the group name, selecting one or more attributes, and ordering the attributes as needed.

To create an attribute group,

1. Select an object type in the Object Class list.
2. Click Create.

The Create Attributes Group dialog box appears.

3. Enter a unique name for the new attribute group.

By default, the attribute group name is NewAttrGroup.

4. Click OK in the Create Attributes Group dialog box.

The Attribute Group dialog box appears. The names of the available attributes appear in the attributes list on the left side of the dialog box.

5. Select one or more attribute names in the All attributes list.

To select multiple attributes, you can use Shift-click, Ctrl-click keys, or drag the pointer up or down the list.

6. Click the right arrow.

The selected names move to the Group list. Click the Up arrow or the Down arrow to change the position of a name in the list by selecting the name. To remove names from the list, select the names and click the Left arrow.

7. Click OK in the Attribute Group dialog box.

In the Attribute Group Manager dialog box, the name of the new attribute group appears in the Attribute Groups list and the names of the attributes appear in the Group Attributes list.

Alternatively, you can create a custom attribute group by using the `gui_create_attrgroup` command.

You can modify an attribute group by specifying the group name and adding, removing, or reordering attributes as needed. You can also modify the Basic, LayoutInfoTipText, Placement, QueryText, and Timing attribute groups but not the All, Application, or User attribute groups.

To modify an attribute group,

1. Select the object type in the Object Class list.
2. Select the group name in the Attribute Groups list.
3. Click Modify.

The Edit Attribute Group dialog box appears. The name of the attribute group appears above the Group attributes list and the names of the attributes in the group appear in the Group attributes list.

4. Modify the group as needed by adding, reordering, or removing attributes.
  - To add attributes to the group, select the attribute names in the All attributes list on the left side of the dialog box and click the Right arrow.
  - To reorder attributes in the group, select an attribute name in the Group attributes list and click the Up arrow or the Down arrow.
  - To remove attributes from the group, select the attribute names in the Group attributes list and click the Left arrow.

To select multiple attributes in a list, select Shift-click, Ctrl-click keys, or drag the pointer up or down the list.

If you are modifying a predefined attribute group, click Reset to system defaults to reset the group to its system default configuration.

5. Click OK in the Edit Attribute Group dialog box.

In the Attribute Group Manager dialog box, the Attribute Groups list displays the modified content of the group.

Alternatively, you can modify an attribute group by using the `gui_update_attrgroup` command and specifying the name of the group you are modifying.

You can remove attribute groups that you have created.

**Note:**

You cannot remove predefined attribute groups provided by the Design Vision tool.

To remove an attribute group,

1. Select the object type in the Object Class list.
2. Select the group name in the Attribute Groups list.
3. Click Delete.

The group name is removed from the Attribute Groups list.

Alternatively, you can remove a custom attribute group by using the `gui_delete_attrgroup` command.

**See Also**

- [Viewing and Editing Object Properties](#)

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## Specifying Path Startpoints, Throughpoints, and Endpoints

A timing path is a path through logic along which signals can propagate. Paths normally start at primary inputs or clock pins of registers and end at primary outputs or data pins of registers. A register is any sequential cell—flip-flop, latch, or other leaf cell—with setup and hold requirements. For more details, see [Defining Timing Paths](#).

You can identify individual timing paths by specifying startpoints, throughpoints, or endpoints.

- Valid startpoints are the primary input ports of a design and the clock pins of sequential cells.
- Valid throughpoints are pins and nets on a path between a valid startpoint and a valid endpoint.
- Valid endpoints are the primary output ports of a design and the data pins of sequential cells.

Only paths that begin at valid startpoints or end at valid endpoints are considered during timing analysis. For a clock, paths are included from all startpoints and to all endpoints related to the clock. For a cell, paths are included only from one startpoint or to one endpoint on the cell.

You must specify the startpoints, throughpoints, or endpoints necessary to identify the paths.

- To identify all paths that end at an output port or data pin, specify the endpoint.
- To identify all paths that begin at an input port or clock pin, specify the startpoint.
- To identify only the paths that start at an input port or data pin and end at an output port or data pin, specify both the startpoint and the endpoint.
- To identify all paths that pass through one or more nets or pins, specify each of the throughpoints.
- To identify only the paths that pass through one or more nets or pins and end at an output port or data pin, specify both the throughpoints and the endpoint.
- To identify only the paths that begin at an input port or clock pin and pass through one or more nets or pins, specify both the startpoint and the throughpoints.
- To identify only the paths that start at an input port or data pin, pass through one or more nets or pins, and end at an output port or data pin, specify the startpoint, throughpoints, and endpoint.

If you specify more than one startpoint or endpoint, all paths that start at any of the startpoints or end at any of the endpoints (and meet the other criteria) are considered.

Dialog boxes in which you can identify timing paths contain three rows of options, labeled To, Through, and From. Each row contains

- A list in which you can select an object type
- A box in which you can enter object names
- A  button that you can click to open the Object Choosers dialog box, in which you can select object names and click OK to enter them in the object name box
- A Selection button that you can click to enter the names of selected objects in the object name box

If the object type you select is any (the default) and you select objects and click the Selected button, the names of all selected objects appear in the box. Otherwise, only the names of selected objects that match the selected object type appear.

To specify startpoints (in the From box), throughpoints (in the Through box), or Endpoints (in the To box) in a dialog box,

1. Select an object type in the list.

For startpoints or endpoints, you can select pin, port, net, or clock. For throughpoints, you can select pin or net. The default (any) means any of the valid types.

2. Do one of the following:

- Enter one or more object names in the box (separate names with blank spaces).
- Select one or more objects and click the Selection button.
- Click the  button, select one or more object names in the Object Chooser dialog box, and click OK (for details, see [Selecting Objects in the Object Chooser](#)).

## Defining Timing Paths

A timing path is a path through logic along which signals can propagate. Paths normally start at primary inputs or clock pins of registers and end at primary outputs or data pins of registers. A register is any sequential cell—flip-flop, latch, or other leaf cell—with setup and hold requirements.

- Setup time is a time specified in the technology library for sequential cells.

Setup is the requirement that data be stable for a given time before the active clock edge. This time can be scaled by operating conditions if the library contains scaling factors for setup.

Setup time on a cell creates a maximum delay requirement for paths leading to the data pin of the cell.

- Hold time is a time specified in the technology library for sequential cells.

Hold is the requirement that the signal on the data pin must remain stable for a given time after the active clock edge. A hold time can be scaled by operating conditions if the library contains scaling factors for hold.

Hold time on a cell creates a minimum delay requirement for paths leading to the data pin of that cell. During compilation, hold time violations are fixed if the clock object has the `fix_hold` attribute.

Slack is the amount of margin by which maximum or minimum path delay requirements are met. Positive slack indicates that the requirement is met; negative slack indicates a violation. Slack is displayed in timing reports.

A violation indicates a constraint is not met.

- A setup violation occurs when a timing path is longer than its targeted maximum delay. The cost function considers the worst violator within each path group when calculating maximum delay cost.
- A hold violation occurs when a timing path is shorter than its targeted minimum delay. A violation is the same as a negative slack value.

The compiler recognizes four types of timing paths:

- Primary input to register (in1 to FF1)

These paths are usually constrained by specification of the clock for the register and setting of an input delay relative to a clock on the input port.

- Register to register (FF1 to FF2)

These paths are constrained by specification of the clock for the registers.

- Register to primary output (FF2 to out1)

These paths are usually constrained by specification of the clock for the register and setting of an output delay relative to a clock on the output port.

- Primary input to primary output (in2 to out2)

You can constrain paths by setting an input delay relative to a clock on the input port and an output delay relative to a clock on the output port.

Paths to registers end at the data pins of registers. Paths from registers start at the clock pin of the register (not at the output pin).

Commands that operate on timing paths or endpoints are called path-based commands. Dialog boxes for path-based commands use From, Through, and To options to specify timing paths. The From and To options accept clocks in their object lists.

The following details apply to path-based commands:

- Path startpoints are usually input ports or clock pins of registers.
- Path endpoints are usually output ports or data pins of registers.
- When you specify a clock with the From option, all path startpoints related to that clock are affected. This includes clock pins of registers in the transitive fanout of the clock sources and ports with input delay relative to the clock.
- When you specify a clock with the To option, all path endpoints related to the clock are affected. This includes data pins of registers in the transitive fanout of the clock sources and ports with output delay relative to the clock.

You can use cell names with the From or To option as shorthand for the pin names when there is one relevant pin. For example, specifying FF1 is the same as specifying FF1/D.

**Note:**

Do not use cell names for path endpoints when the cell is a JK flip-flop or a multiplexed flip-flop.

By using the Through option, you can control the timing on each specific path between a startpoint and an endpoint, even when different paths have different timing requirements.

Some path-based commands overwrite the information from other commands. For example, setting the maximum delay on a path removes a previous multicycle path specification on the same path.

For more information about timing paths, see the *Design Compiler Reference Manual: Constraints and Timing*.

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## Analyzing RTL

You can analyze timing and congestion problems by cross-probing cells and timing paths to examine their source in the RTL files. RTL cross-probing can help you find and debug problems during timing analysis, congestion analysis, and datapath analysis. You can cross-probe selected cells or pins, the cells on selected timing paths, the cells in highly-congested areas of the floorplan, and objects in linked resource reports.

The tool displays RTL files in the RTL browser window. You can examine the RTL for objects or timing paths that you cross-probe in the elaborated or compiled design. You can view, select, and copy text in the RTL browser, but you cannot edit the file. You can also search for text in the RTL file or a linked resource report.

You can use the RTL browser to cross-probe from RTL to gates. When you open the RTL file that you used to elaborate or compile the design, you can cross-probe the cells associated with a line in the file. The tool selects the cells associated with the line and displays them in the Selection List dialog box.

For more information about the RTL analysis tools, see the following topics:

- [Cross-Probing the RTL for Cells and Timing Paths](#)
  - [Examining Cells in the RTL Browser](#)
  - [Viewing RTL Files](#)
  - [Finding Text in an RTL File or an HTML Report](#)
  - [Selecting RTL Objects by Name](#)
  - [Opening RTL Files](#)
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## Cross-Probing the RTL for Cells and Timing Paths

You can analyze timing and congestion problems in an elaborated or compiled design by cross-probing the RTL for selected objects and timing paths. RTL cross-probing helps you to identify where certain cells originate in the RTL and to find and debug problems during timing analysis, congestion analysis, or datapath analysis.

**Note:**

The design must be elaborated or compiled using Design Compiler version I-2013.12 or later, and the design files must remain unmodified and in the same locations.

You can cross-probe the RTL for cells and timing paths that you select in other views. You can also cross-probe cells in highly congested areas of the design, cells in a design resources report, and synthetic operators in a datapath extraction report. You can cross-probe the RTL in VHDL, Verilog, and SystemVerilog files.

Cross-probing cells can help you identify where certain gates originate in the RTL.

- During timing analysis, cross-probing a critical path can help you to debug worst-case timing problems.
- During congestion analysis, cross-probing cells in highly congested areas helps you identify the RTL code that is causing the congestion.
- During datapath analysis, RTL links in design resource reports can help you to debug datapaths during worst-case path analysis.

This helps you understand the datapath extraction, which can help you to improve the coding style for better extraction.

You use the RTL browser to examine the RTL for cells and timing paths that you cross-probe from other views. You can view, select, and copy text in the RTL browser, but you cannot edit the RTL file. You can also use the RTL browser to cross-probe from the RTL to gates.

**Note:**

The GUI does not support cross-probing from nets or cross-probing to UPF files.

The RTL browser window contains two panes. The RTL chooser appears in the top pane, and the RTL text view appears in the bottom pane. The RTL chooser lists the RTL file names, line numbers, and cell names for each cell in an expanding tree view. The RTL text view displays the content of the RTL files. The RTL text view is always visible; the RTL chooser appears only when you cross-probe cells or timing paths.

When you cross-probe a cell, the tool attempts to locate the RTL file in which the cell originates and opens the file in the RTL browser. When you cross-probe a timing path, the tool creates a collection of all the cells on the path, attempts to locate the RTL files in which the cells originate, and opens the files in the RTL browser.

If the tool cannot find the RTL file for a cell, the RTL browser displays the following message:

Unable to open RTL File:  
Cross Probe has no RTL File Associated

If you cross-probe multiple cells and the tool cannot find the files for some of the cells, the RTL chooser displays <No RTL Source> instead of the file name for each file it could not find.

The RTL chooser displays file names, line numbers, and cell names in an expanding tree view. You can expand a file name or line number by double-clicking the name or number or by clicking its expansion button (plus sign). When a cell has multiple sources, the additional source files are listed below the cell name, preceded by the words Alternate Source.

The first file name is expanded by default to show all of the line numbers and cell names under it.

- If one cell name appears under the expanded file name, the RTL text view displays the line for that cell.
- If multiple cell names appear under the expanded file name, the RTL text view displays the first line of the file.

The RTL text view displays the RTL for the file name, line number, or cell name that you select in the RTL chooser.

- To display a file, click the file name.

The first time you click a file name, the RTL text view displays the file beginning at line 1 and an icon with the file name appears at the top of the pane.

- To display the RTL for a cell, click its line number or cell name.

The RTL text view displays the line where the cell originates in the RTL file.

In general, when you select a cell name in the RTL chooser, the RTL text view displays the line in the file where the cell is defined. The tool always attempts to maintain the accuracy of the cross probe. For cells that pass through complex optimization steps, such as ungrouping, boundary optimization, or mapping to complex cells, the tool points to the `always` block of the RTL file.

You can configure the RTL browser by setting options at the top of the RTL chooser to hide or display the RTL chooser, enable or disable the follow-selection mechanism, and

reuse the RTL browser window. The columns in the RTL chooser provide the following information:

- The file names, line numbers, and cell instance names
- The number of cells in a file
- The line number, origin, and reference name for each cell

You can select and copy file names, line numbers, and cell names in the RTL chooser or text in the RTL text view. You can also add or remove markers on lines of text and display or hide blocks of code, such as a module, an `always` block, or an `if` statement. The RTL browser also provides tools that you can use to open a design resources report, to find text in the RTL file or a linked resources report, or to search for and select cells by name.

You can cross-probe cells in the current design from a line in the RTL file that you used to elaborate or compile the design. The tool selects the cells associated with the line and displays them in the Selection List dialog box. You can open the RTL file by choosing AnalyzeRTL > Open RTL Files and selecting the file in the Open RTL Files dialog box.

When you cross-probe cells from the RTL file, the tool opens the Selection List dialog box and colors the cells with the selection color in schematic and layout views, but it does not open a new schematic or layout view to display the cells. You can perform operations on the selected cells, such as creating a schematic of the selected logic.

## See Also

- [Cross-Probing From RTL to Gates](#)
- [Viewing RTL Files](#)
- [Examining Cells in the RTL Browser](#)

## Cross-Probing Selected Cells and Pins

You can cross-probe cells or pins in a schematic, cell list, path data table, layout view, or logic hierarchy view and examine the corresponding RTL file. When you cross-probe a cell or pin, the tool searches for the RTL files in which the cells originate and displays the file names and cell names in a new RTL browser window.

To cross-probe cells in an elaborated or compiled design,

1. Select one or more cells, pins, or ports.

You can select objects in a schematic or layout view, the hierarchy browser, a cell list view, or a port and pin list view.

## 2. Choose AnalyzeRTL > Cross Probe to Source.

Alternatively, you can right-click a selected cell, pin, or port and choose Cross Probe to Source.

The tool locates the RTL files in which the cells originate and opens the files in a new RTL browser window.

You can also cross-probe cells in highly congested areas of the design. For details, see [Cross-Probing Cells in Congested Areas](#).

### See Also

- [Analyzing RTL](#)
- [Examining Cells in the RTL Browser](#)

## Cross-Probing Selected Timing Paths

You can analyze and debug timing problems by cross-probing the RTL for selected timing paths. During timing analysis, cross-probing a critical path helps you to debug worst-case timing problems. When you cross-probe a timing path, the tool creates a collection of all the cells on a path, locates the RTL files in which the cells originate, and opens the files in a new RTL browser window.

To cross-probe timing paths,

### 1. Select one or more timing paths.

For example, you can select a critical path in the timing status summary or a path data table.

### 2. Choose AnalyzeRTL > Cross Probe to Source.

Alternatively, you can right-click a selected path and choose Cross Probe to Source.

The tool locates the RTL files for the cells on each path and opens the files in a new RTL browser window.

You can also cross-probe datapath cells on a timing path that you are inspecting in the path inspector. You can cross-probe the entire datapath or individual elements on the datapath.

To cross-probe all the full datapath,

1. Select the full datapath row in the path elements table.
2. Choose AnalyzeRTL > Cross Probe to Source.

The tool locates the RTL files for the cells on the path and opens the files in the RTL browser window.

To cross-probe individual elements on the datapath,

1. Double-click the full datapath row in the path elements table or click the expansion button (plus sign) to display the rows for the individual elements.
2. Select the rows for the elements that you need to cross probe.
3. Choose AnalyzeRTL > Cross Probe to Source.

The tool locates the RTL files for the selected elements and opens the files in the RTL browser window

For information about using the path inspector, see [Inspecting Timing Path Elements](#).

### See Also

- [Analyzing RTL](#)
- [Examining Cells in the RTL Browser](#)

## Cross-Probing Cells in Congested Areas

During congestion analysis, cross-probing cells in highly congested areas can help you to identify the RTL code that is causing the congestion. When you cross-probe cells in a congested area, you can view the RTL in the List by Congested Region dialog box or the RTL browser.

To quickly view the RTL for a cell in the List by Congested Region dialog box,

- Select the cell name in the List by Congested Region dialog box.  
You can Shift-click or Ctrl-click to select multiple cell names.

### Note:

To select a cell name in the tree view, you might need to expand its file name and line number by clicking their expansion buttons.

The first time you select a cell name, the List by Congested Region dialog box opens a new pane below the cell list and displays the RTL for the selected cell in the RTL text view. Each time you select a cell name from a different file, a tab with the file name appears above the RTL text view. You can click this tab to return to the file after viewing other files. For information about working in the RTL text view, see [Viewing RTL Files](#).

To close a file in the RTL text view,

- Right-click its tab and choose Close.

To cross-probe cells in congested areas and view their RTL in the RTL browser,

1. Select one or more cells in the List by Congested Region dialog box.

To select all of the cells in the list view, right-click and choose Select All.

2. Click the Cross Probe button or choose AnalyzeRTL > Cross Probe Congested Cells.

The tool locates the RTL files in which the cells originate, opens the files in the RTL browser, and displays the file names in the RTL chooser.

You can open the RTL file in a new RTL browser window by right-clicking a file name, line number, or cell name and choosing Open Source in New Browser.

For information about viewing cells in congested areas of the design, see [Viewing Cells in Congested Areas](#).

## See Also

- [Analyzing RTL](#)
- [Examining Cells in the RTL Browser](#)
- [Viewing RTL Files](#)

## Cross-Probing Cells in a Design Resources Report

During worst-case datapath analysis, the RTL links in the design resources report can help you to debug the datapaths. Cross-probing cells in a design resource report helps you understand how datapaths are extracted from the RTL, which can help you to improve the coding style for better extraction.

To cross-probe a cell in a design resources report,

1. Choose Design > Report Design Resources.

The Report Design Resources dialog box appears.

Alternatively, you can right-click a cell in the hierarchy browser or a list view, or a file name, line number, or cell name in the RTL browser or the List by Congested Region dialog box, and choose Report Resources of Selected.

2. Set the report and output options as needed.

Make sure the To report viewer option is selected.

3. Click OK.

The report appears in a new HTML report view.

4. Click the RTL file name link for a cell in the HTML report view.

The tool opens the file in a new RTL browser window.

You can use the Find Text dialog box to search for text in a design resources report. In addition, when you view the RTL file that you cross-probed from a design resources report, you can use the Find Text dialog box to search the report for information related to a particular line in the RTL file. For information about using this dialog box, see [Finding Text in an RTL File or an HTML Report](#).

For more information about generating a design resources report, see [Reporting Design Resources](#).

#### See Also

- [Viewing RTL Files](#)

### Cross-Probing Synthetic Operators in a Datapath Extraction Report

During datapath extraction analysis, datapath extraction report links to RTL can help you to understand how the datapath blocks are extracted from your RTL before you optimize the design.

When the tool detects a synthetic operator that is not extracted, it reports the information about what is blocking the datapath extraction, including the file name of the RTL and the line number of the inferred synthetic operator. Cross-probing synthetic operators in a datapath extraction report helps you understand the datapath extraction, which can help you to improve the coding style for better extraction.

To cross-probe a synthetic operator in a datapath extraction report,

1. Choose Design > Analyze Datapath Extraction, or choose AnalyzeRTL > Analyze Datapath Extraction.

The Analyze Datapath Extraction dialog box appears.

2. Set the report and output options as needed.

Make sure the To report viewer option is selected.

3. Click OK.

The report appears in a new HTML report view window.

4. Click the RTL file name link for a synthetic operator in the HTML report view.

The tool opens the file in a new RTL browser window.

You can use the Find Text dialog box to search for text in a datapath extraction report. In addition, when you view the RTL file that you cross-probed from a datapath extraction report, you can use the Find Text dialog box to search the report for information related to a particular line in the RTL file. For information about using this dialog box, see [Finding Text in an RTL File or an HTML Report](#).

For more information about generating a datapath extraction report, see [Reporting Datapath Extraction Analysis](#).

### See Also

- [Viewing RTL Files](#)

## Cross-Probing From RTL to Gates

You can cross-probe cells in the current design from a line in the RTL file that you used to elaborate or compile the design. Lines that you can cross-probe are highlighted with a green background. The tool selects the cells associated with the line in the RTL, opens the Selection List dialog box, and colors the cells with the selection color in schematic and layout views. However, a new schematic or layout view is not opened to display the cells. You can perform operations on the selected cells, such as creating a schematic of the selected logic.

Choose AnalyzeRTL > Open RTL Files and select the file in the Open RTL Files dialog box to open the RTL files. The RTL browser window displays just the RTL text view and not the RTL chooser. The title bar displays the name and location of the RTL file.

To cross-probe cells from a line in the RTL file,

1. Select a line in the RTL text view.
2. Right-click and choose Select Objects of Selected Line(s).

The tool selects the cells associated with the line in the RTL file and displays the selected cells in the Selection List dialog box.

When you open the RTL file that is used to elaborate or compile the design, you can cross-probe from lines in the RTL to cells in the current design. You can also perform other RTL browsing tasks, such as finding text in the RTL file, selecting and copying text, adding or removing markers, or finding text in an open design resources or datapath extraction report.

To open RTL files that were used to compile the design,

1. Choose AnalyzeRTL > Open RTL Files.  
The Open RTL Files dialog box appears.
2. Select the name of the directory containing the RTL files in the Look in pane.

The dialog box displays the RTL file names.

3. Select one or more file names.

You can Shift-click or Ctrl-click to select multiple file names.

4. Click Open.

The tool opens the file in a new RTL browser window. If you open multiple files, the tool opens each file in a separate RTL browser window.

If the RTL files that are used to elaborate or compile the design is moved or their directory is renamed, you can use the `update_cross_probing_files` command to update the location or directory name. To learn the status of the RTL files, use the `report_cross_probing_files` command. For information about using these commands, see their man pages or the *Design Compiler User Guide*.

If you open the RTL file that is moved or that is not used to compile the design, the RTL browser displays the text on a gray background. You can select and copy text and add or remove markers, but you cannot cross-probe cells from the RTL or perform other RTL browsing tasks in the file.

You can also use the Open RTL Files dialog box to open and view other types of text files, such as Tcl script files, report files, and log files.

## See Also

- [Examining Cells in the RTL Browser](#)
- [Viewing RTL Files](#)
- [Finding Text in an RTL File or an HTML Report](#)
- [Selecting RTL Objects by Name](#)
- [Opening RTL Files](#)

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## Examining Cells in the RTL Browser

You can select and cross-probe cells or timing paths in the design and use the RTL browser to view the RTL for the selected cells or the cells on the selected timing paths. By default, the RTL browser displays each file name and the associated line numbers and cell names in a three-level tree structure. To view the content of a file, you click the file name. To view the RTL for a cell, you click its line number or cell name.

When you cross-probe cells, the tool attempts to locate the RTL files in which the cells originate and open the file in the RTL browser. If the tool cannot find the RTL file for a cell, the RTL browser displays the following message:

Unable to open RTL File:

Cross Probe has no RTL File Associated

When you cross-probe a timing path, the tool creates a collection of all the cells on the path, and then attempts to locate the RTL files in which the cells originate, and open the files in the RTL browser.

The RTL browser window contains two panes. The RTL chooser tree view appears in the top pane by default, and the RTL text view appears in the bottom pane. The RTL chooser lists the RTL file names, line numbers, and cell names. The RTL text view displays the content of the RTL files.

The RTL chooser displays file names, line numbers, and cell names in an expanding tree view. You can expand a file name or line number by double-clicking the name or number or by clicking the expansion button (plus sign). You can optimize your viewing area in the window by using the split bars between the panes to adjust their relative heights.

The first file name is expanded by default to show all of the line numbers and cell names. If a cell has multiple sources, the additional source files are listed below the cell name, preceded by the words Alternate Source.

- If only one cell name appears under the expanded file name, the RTL text view displays the line for that cell.
- If multiple cell names appear under the expanded file name, the RTL text view displays the first line of the file.

If you cross-probe multiple cells and the tool cannot find the files for some of the cells, the RTL chooser displays <No RTL Source> instead of the file name for each file it could not find.

The RTL text view displays the RTL for the file name, line number, or cell name that you select in the RTL chooser.

- To display a file, click the file name.

The RTL text view displays the file beginning at line 1. When you display a file for the first time, a tab with the file name appears at the top of the RTL view pane. You can click this tab to return to the file after viewing other files.

- To display the RTL for a line or a cell, click the line number or the cell name.

The RTL text view displays the line where the cell originates in the RTL file.

In general, when you click a cell name, the RTL browser displays the line in the file where the cell is defined. However, the tool always attempts to maintain the accuracy of the cross probe. For cells that pass through complex optimization steps, such as ungrouping, boundary optimization, or mapping to complex cells, the tool points to the always block of the RTL file.

You can select and copy file names, line numbers, and cell names in the RTL chooser and text in the RTL text view. The RTL browser also provides tools that you can use to find text in the RTL file or a linked resources report, select cells by name, and cross-probe cells in the design from lines in the RTL file. You can also open the RTL file in the RTL browser without cross-probing objects in the design by using the Open RTL Files dialog box.

### See Also

- [Cross-Probing the RTL for Cells and Timing Paths](#)
- [Cross-Probing From RTL to Gates](#)
- [Finding Text in an RTL File or an HTML Report](#)
- [Selecting RTL Objects by Name](#)
- [Viewing RTL Files](#)
- [Opening RTL Files](#)

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## Viewing RTL Files

You can use the RTL browser to examine RTL files when you cross-probe cells or timing paths in other views or when you cross-probe objects in linked resource reports. You can also examine RTL files that you open using the Open RTL dialog box.

The RTL browser window contains two panes. The RTL chooser appears in the top pane, and the RTL text view appears in the bottom pane. The RTL chooser lists the RTL file names, line numbers, and cell names for each cell in an expanding tree view. The RTL text view displays the content of the RTL files.

The RTL text view is always visible. The RTL chooser appears only when you cross-probe cells or timing paths.

You can configure the RTL browser by setting options at the top of the RTL chooser to

- Hide or display the RTL chooser
- Enable or disable the follow-selection mechanism
- Reuse the RTL browser window

You can select and copy file names, line numbers, and cell names in the RTL chooser. In the RTL text view, you can select and copy RTL text, insert markers online numbers, and hide or display blocks of text.

To hide the RTL chooser, deselect the Show RTL Chooser option at the top of the RTL browser.

By default, selecting a cell name in the RTL chooser automatically replaces the current selection. You can enable or disable this follow-selection mechanism separately for each RTL browser window.

To disable follow selection in the RTL browser window, deselect the Follow Selection option at the top of the RTL browser window.

By default, the tool opens a new RTL browser window each time you perform a cross-probe operation (for example, by selecting a timing path and choosing AnalyzeRTL > Cross Probe to Source). You can enable a mechanism that reuses the same RTL browser window for subsequent cross-probe operations.

To reuse the RTL browser window for subsequent cross-probe operations, select the Reuse Window option at the top of the RTL browser window.

The columns in the RTL chooser provides the following information:

- The file names, line numbers, and cell instance names
- The number of cells in a file
- The line number, origin, and reference name for each cell

You can copy file names, line numbers, and cell names in the RTL chooser. You can also sort the file and cell name lists alphanumerically by the contents of a column and resize individual columns.

To copy file names, line numbers, or cell names,

1. Select the names and line numbers that you want to copy.
2. Right-click and choose Copy.

To sort the list,

1. Move the pointer into the heading of the column you want to sort.
2. When the pointer changes shape, click the column heading.

Click again if you want to reverse the sort.

To resize a column,

1. Move the pointer over the right edge of the column you want to resize.
2. When the pointer changes shape, drag the column edge right or left to increase or decrease the width of the column.

The tool continues to display subsequent cross-probe results in this window until you either deselect the Reuse Window option or select the option in a different RTL browser window.

The RTL text view displays the line numbers on the left side and the RTL text on the right side. Expansion buttons between the line numbers and the text allow you to display or hide blocks of code, such as a module, an always block, or an if statement.

You can copy text that you want to paste into another tool, such as a text editor. You can also mark lines of code.

To copy text,

1. Select the text by dragging the pointer over it or by pressing Shift and pressing an arrow key.  
To quickly select all the text in the file, right-click and choose Select All.
2. Right-click and choose Copy.

To add a marker to a line of text, right-click the line of text or its line number and choose Add marker.

To remove a marker from a line of text, right-click the marker, the line of text, or its line number and choose Remove marker.

You can open and view the RTL file in a new instance of the RTL browser window.

To open one or more RTL files in a new RTL browser window,

1. Select one or more file names or cell names in the RTL chooser.
2. Right-click and choose Open Source in New Browser.

To open the RTL file that you are currently viewing in a new RTL browser window, right-click in the RTL text view and choose Open Source in New Browser.

## See Also

- [Examining Cells in the RTL Browser](#)
- [Finding Text in an RTL File or an HTML Report](#)
- [Selecting RTL Objects by Name](#)

- [Cross-Probing From RTL to Gates](#)
  - [Opening RTL Files](#)
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## Finding Text in an RTL File or an HTML Report

You can use the Find Text dialog box to find text in the RTL file displayed in the RTL browser. You can also use this dialog box to find text in a design resources report or a datapath extraction report that is displayed in the HTML report view.

To find text in the RTL browser or the HTML report,

1. Right-click in the RTL browser text view or the HTML report view and choose Find.  
The Find Text dialog box appears.
2. Enter the text in the Find box.
3. (Optional) Set the search options and search direction as needed.
4. Click Find.

The tool searches the report and selects the first occurrence of the text.

To find other occurrences of the text, repeat steps 3 and 4. To find a different text string, repeat steps 2 through 4.

If you are viewing the RTL file that you cross-probed from a design resources report or a datapath extraction report and the report is still open in the HTML report window, you can search the report for information associated with a particular line number in the RTL file.

To search the design resources report or datapath extraction report,

- Right-click the line in the RTL text view and choose Search in Resource Report.  
The Find Text dialog box appears, if it is not already open, and displays the file name and line number in the Find box. The tool searches the report and selects the first occurrence of the file name and line number that it finds in the HTML report view.

To search for additional occurrences of the file name and line number,

1. (Optional) Set the search options and search direction as needed in the Find Text dialog box.
2. Click the Find button.

You can search for other text in the report by entering the text in the Find box and clicking the Find button.

To close the Find Text dialog box, click Close.

**See Also**

- [Examining Cells in the RTL Browser](#)
  - [Selecting RTL Objects by Name](#)
  - [Viewing RTL Files](#)
  - [Cross-Probing From RTL to Gates](#)
  - [Opening RTL Files](#)
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## Selecting RTL Objects by Name

You can select an object name in the RTL browser and use the Select by Name dialog box to search for and select the object in the elaborated or compiled design.

To search for and select an object by name,

1. Select the object name in the RTL text view.

You can select the name of a cell, net, port, or pin.

2. Right-click and choose Select By Name.

The Select by Name dialog box appears. The object name appears in the Search for box.

3. Select the appropriate object class option: Cell, Net, Port, or Pin.

4. Click Search.

The object name appears in the Search results list.

5. Select the name and click Select.

The tool selects the object.

For information about using the Select By Name dialog box, see [Searching for Objects by Name or Regular Expression](#).

**See Also**

- [Examining Cells in the RTL Browser](#)
- [Viewing RTL Files](#)
- [Finding Text in an RTL File or an HTML Report](#)
- [Cross-Probing From RTL to Gates](#)
- [Opening RTL Files](#)

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## Opening RTL Files

You can open RTL files and view them in the RTL browser. The RTL browser window displays just the RTL text view and not the RTL chooser. The title bar displays the name and location of the RTL file.

When you open the RTL file that was used to elaborate or compile the design, you can cross-probe from lines in the RTL to cells in the current design. Lines that you can cross-probe are highlighted with a green background. You can also perform other RTL browsing tasks, such as finding text in the RTL file, selecting and copying text, adding or removing markers, or finding text in an open design resources or datapath extraction report.

To open RTL files that were used to compile the design,

1. Choose AnalyzeRTL > Open RTL Files.

The Open RTL Files dialog box appears.

2. Select the name of the directory containing the RTL files in the Look in pane.

The dialog box displays the RTL file names.

3. Select one or more file names.

You can Shift-click or Ctrl-click to select multiple file names.

4. Click Open.

The tool opens the file in a new RTL browser window. If you open multiple files, the tool opens each file in a separate RTL browser window.

If the RTL files have been moved or their directory has been renamed, the icon against the directory name appears gray in the Look in pane; if you select the directory name, the file list is empty. You can use the `update_cross_probing_files` command to update the location or directory name. To learn the status of the RTL files, use the `report_cross_probing_files` command. For information about using these commands, see their man pages or the *Design Compiler User Guide*.

If you open the RTL file that has been moved or that was not used to compile the design, the RTL browser displays the text on a gray background. You can select and copy text and add or remove markers, but you cannot cross-probe cells from the RTL or perform other RTL browsing tasks in the file.

You can also use the Open RTL Files dialog box to open and view other types of text files, such as Tcl script files, report files, and log files. You can select and copy text and add or remove markers, but you cannot edit the text or perform other RTL browsing tasks in the file.

### See Also

- [Examining Cells in the RTL Browser](#)
  - [Viewing RTL Files](#)
  - [Finding Text in an RTL File or an HTML Report](#)
  - [Cross-Probing From RTL to Gates](#)
  - [Selecting RTL Objects by Name](#)
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## Analyzing Design Timing

The Design Vision GUI provides views you can use for both high-level analysis of overall timing in the design and detailed analysis of individual timing paths and object connectivity. For information about the different kinds of timing and design analysis views you can use, see the following sections:

- [Viewing High-Level Timing Results](#)
  - [Analyzing Timing Path Collections](#)
  - [Examining Timing Paths and Selected Logic](#)
  - [Examining Timing Path Details](#)
  - [Inspecting Timing Path Elements](#)
  - [Timing Status Summary](#)
- 

## Viewing High-Level Timing Results

Histograms provide high-level views of design timing for visual timing analysis. You can use histograms to view the overall timing performance of your logic design and to select individual timing paths for further study in timing reports or other analysis views.

The GUI provides the following predefined histograms: path slack and net capacitance.

- Path slack histograms show a distribution of timing slack values for selected paths or for the paths with the worst slack in the design. For details, see [Opening a Path Slack Histogram](#).

You can select a maximum or minimum delay type (setup or hold), set the maximum number of paths and the number of worst paths per endpoint, and select a path group.

You can also specify individual paths to, from, or through selected objects (similar to the way you specify paths for timing reports).

- Net capacitance histograms show a distribution of net capacitance values for selected nets or for all nets in the design. For details, see [Opening a Net Capacitance Histogram](#).

When you use the Timing Status Summary window to view timing path details, you can also generate histograms that show the distribution of values for certain types of path details listed in the window.

**Note:**

You can create histograms that show the distribution of certain path data when you examine timing paths in the path analyzer, the timing status summary, or a path data table. For details, see [Creating Path Data Histograms](#).

The histogram view windows are split into two panes. By default, the histogram bar graph appears in the left pane and the object table appears in the right pane. You can

- Hold the pointer over a bin in the bar graph to display information about its contents in an InfoTip below the pointer.
- Click a bin to display its contents (object names and slack or capacitance values) in the object table.
- Select objects in the object table for further examination with other analysis tools such as schematics or reports.
- Filter the object table, limiting it to certain objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

You can use the split bars between the panes to increase or decrease the relative sizes of the bar graph and object table. You can also set an option in the Application Preferences dialog box that displays the object table below the bar graph when you open a new histogram. For details, see [Setting Global Default Preferences](#).

**See Also**

- [Histogram Views](#)

## Opening a Path Slack Histogram

Path slack histograms provide a high-level overview of the timing quality for selected paths in your design. Create a path slack histogram to identify paths that failed their constraints.

You can create a path slack histogram to show the slack distribution for

- Selected timing paths
- Selected design objects
- Paths with the worst slack in the current design

To generate a path slack histogram for selected timing paths,

1. Select two or more paths.
2. Choose Timing > Slack Histogram of Selected Paths.

To generate a path slack histogram for paths through selected design objects,

1. Select two or more design objects (cells, pins, ports, or nets).
2. Choose Timing > Slack Histogram of Selected Logic.

The default path slack histogram for paths with the worst slack in the current design shows the distribution of slack values for the 50 paths with the worst slack in the current design or in each path group, with a maximum of 10 paths per endpoint. You can set options to

- Limit the histogram to paths in a specific path group
- Increase or decrease the maximum number of paths with the worst slack in the current design (or the specified path group)
- Increase or decrease the maximum number of paths to any single endpoint

You can also generate a histogram that shows the slack distribution for specific paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the histogram includes only paths that start at specified startpoints, end at the specified endpoints, or pass through one or more specified throughpoints. For details, see [Cross-Probing Selected Timing Paths](#).

By default, path slack histograms are based on maximum delay times. This allows you to view the distribution of path setup times. You can change the delay type option to generate a histogram based on

- Minimum delay times (to view path hold times)
- Minimum rising delays
- Minimum falling delays
- Maximum rising delays
- Maximum falling delays

In addition, you can set options to

- Enable preset and clear arcs
- Include hierarchical pins
- Set the distribution (number of bins) and range of slack values

The following sections describe how to generate a default histogram for the worst paths in the design, generate a default histogram for specific paths, and generate a custom path slack histogram.

To generate a default path slack histogram for the worst paths in the design,

1. Click the  button on the Timing Views toolbar, or choose Timing > Path Slack.  
The Paths Slack dialog box appears.
2. Click OK or Apply.

To generate a default path slack histogram for specific paths,

1. Click the  button on the Timing Views toolbar, or choose Timing > Path Slack.  
The Paths Slack dialog box appears.
2. Specify paths to or from specific inputs, outputs, or registers by specifying their startpoints (From), throughpoints (Through), or endpoints (To).

First, select an object type. Startpoints and endpoints can be pins, ports, nets, or clock. Throughpoints can be pins or nets. Then, you can

- Enter one or more object names.
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Cross-Probing Selected Timing Paths](#).

3. Set other options as needed.
4. Click OK or Apply.

To generate a custom path slack histogram,

1. Click the  button on the Timing Views toolbar, or choose Timing > Path Slack.  
The Paths Slack dialog box appears.
2. Set options to control the number of paths in the histogram.

- To change the maximum number of paths in the histogram, enter a value in the Max paths box.
  - To change the maximum number of paths to an endpoint, enter a value in the Nworst paths box.
  - To limit the histogram to paths in a single path group, select a path group name in the Group name drop-down list.
3. To limit the histogram to specific paths, specify their startpoints (From), throughpoints (Through), or endpoints (To).
- For details, see [Cross-Probing Selected Timing Paths](#).
4. To change the type of timing analysis used to generate the histogram, select an option in the Delay type drop-down list. The default (max) is set for maximum delays.
- For minimum delays, select min.
  - For maximum delays, select max.
  - For maximum rising delays, select max\_rise.
  - For maximum falling delays, select max\_fall.
  - For minimum rising delays, select min\_rise.
  - For minimum falling delays, select min\_fall.
5. Set other timing options as needed.
- To enable preset and clear arcs, select the Enable preset clear arcs option.
  - To include hierarchical pins, select the Include hierarchical pins option.
6. If you need to control the distribution of slack values in the histogram, perform one of the following:
- To increase or decrease the maximum number of bins, select the Number of bins option and change the value in the Number of bins list. The default is 8.
  - To limit the range of slack values in each bin, select the Value range per bin option and enter a value in the Value range per bin text box.
7. Set the other bin options as needed.
- To control the range of slack values used to generate the histogram, enter maximum and minimum slack values in the Slack text boxes.

You can enter a minimum slack value to set the lower bound, a maximum slack value to set the upper bound, or both.

- If you want to set the exact minimum slack limit, select the Lower bound strict option.
- If you want to set the exact maximum slack limit, select the Upper bound strict option.

By default, the Lower bound strict and Upper bound strict options are deselected and the histogram shows the smallest possible range that encompasses all the slack values within the limits you specify.

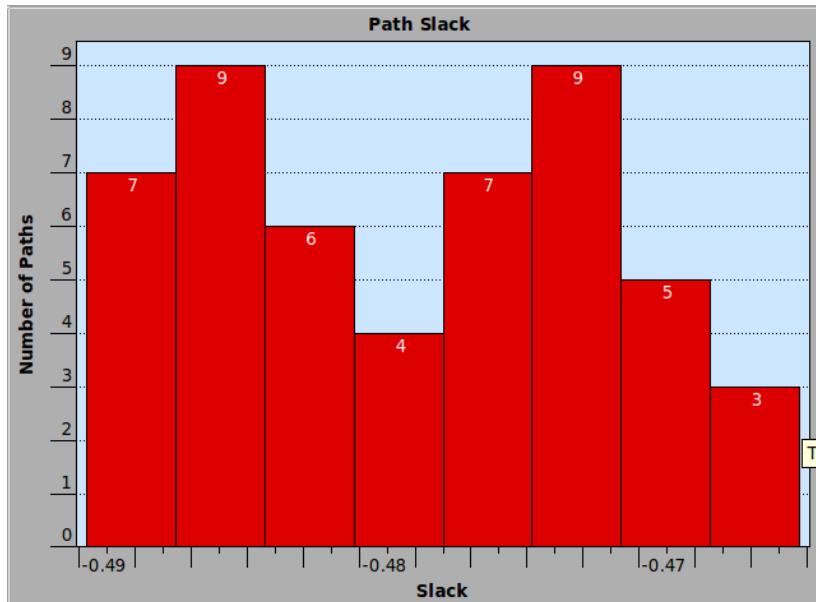
8. Set the histogram options as required.

- To customize the histogram name, change the name in the Histogram title text box.
- To customize the label for the x-axis, change the name in the X-axis title text box.
- To customize the label for the y-axis, change the name in the Y-axis title text box.

9. Click OK or Apply.

When you open a path slack histogram in a new histogram view, a tab appears at the bottom of the workspace area, above the console. You can use this tab to return to the histogram view after working with other views.

The following figure shows an example of a path slack histogram with eight bins, which represent the number of paths (y-axis) versus their slack values (x-axis).



The numbers at the top of the each bin indicate the total paths in the bin. Green bins (on the positive side of 0) contain paths that met their constraints. Red bins (on the negative side of 0) contain paths that failed their constraints.

- If you hold the pointer over a bin, an InfoTip displays the number of paths and the range of slack values in the bin.

An InfoTip might read, for example, Range: 0.08 to 0.496 Contents: 35.

- If you click a bin to select it, the bin turns yellow and the slack value, startpoint name, and endpoint name for each path appear in the table to the right of the histogram.

When you select one or more paths in the table, you can display them in a schematic view by doing one of the following:

- Click the  button on the Schematics toolbar.
- Choose Schematic > New Schematic View.
- Right-click and choose Path Schematic.

For details about viewing schematics, see [Schematic Views](#). For details about selecting paths, see [Selecting Timing Paths](#).

## See Also

- [Path Slack Histograms](#)

## Opening a Net Capacitance Histogram

Net capacitance histograms provide a high-level overview of the capacitance values for selected nets or for all the nets in your design. Create a net capacitance histogram to identify nets that have unacceptably high capacitance values.

You can create a net capacitance histogram to show the capacitance distribution for

- Selected nets
- All nets in the current design

To display a net capacitance histogram for selected nets,

1. Select the nets.
2. Choose Timing > Capacitance of Selected Nets.

To display a net capacitance histogram for all nets in the current design,

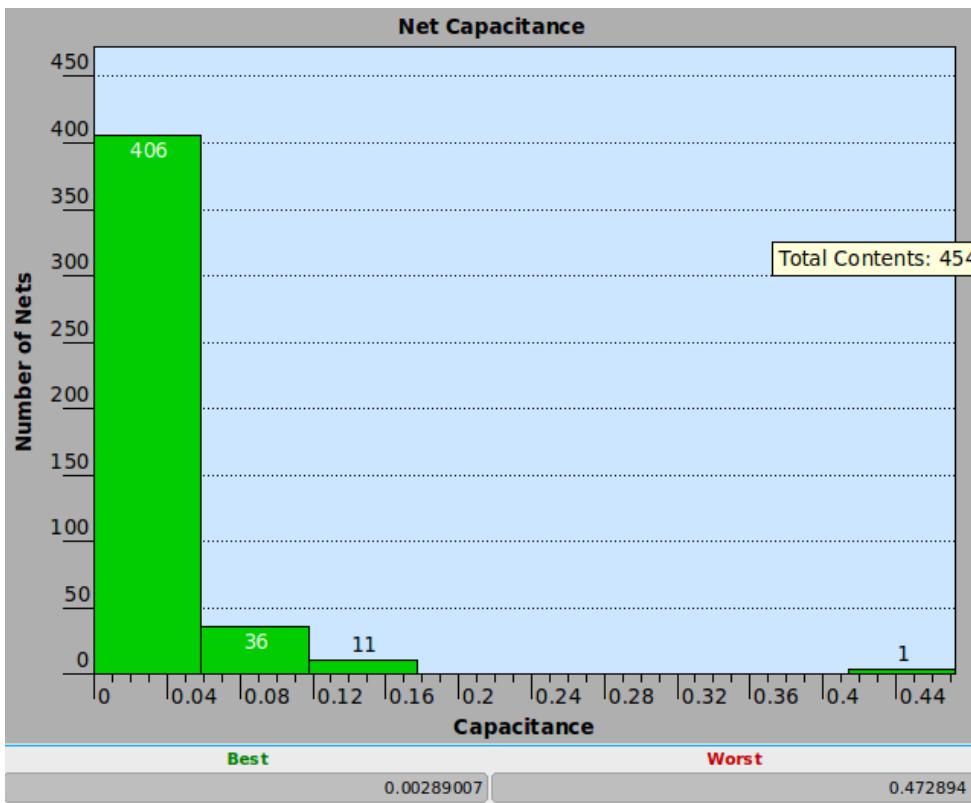
1. Click the  button on the Timing Views toolbar, or choose Timing > Net Capacitance.
- The Net Capacitance dialog box appears.

2. If you need to control the distribution of capacitance values in the histogram, perform one of the following:
  - To increase or decrease the maximum number of bins, select the Number of bins option and change the value in the Number of bins list. The default is 8.
  - To limit the range of capacitance values in each bin, select the Value range per bin option and enter a value in the Value range per bin text box.
3. Set the other bin options as needed.
  - To control the range of capacitance values used to generate the histogram, enter maximum and minimum capacitance values in the Capacitance text boxes.

You can enter a minimum capacitance value to set the lower bound, a maximum capacitance value to set the upper bound, or both.
  - If you want to set the exact minimum capacitance limit, select the Lower bound strict option.
  - If you want to set the exact maximum capacitance limit, select the Upper bound strict option.
4. Set the histogram options as required.
  - To customize the histogram name, change the name in the Histogram title text box.
  - To customize the label for the x-axis, change the name in the X-axis title text box.
  - To customize the label for the y-axis, change the name in the Y-axis title text box.
5. Click OK.

When you open a net capacitance histogram in a new histogram view, a tab appears at the bottom of the workspace area, above the console. You can use this tab to return to the histogram view after working with other views.

The following figure shows an example of a net capacitance histogram with eight bins, which represent the number of nets (y-axis) versus their capacitance values (x-axis).



The numbers at the top of each bin indicate the total nets in the bin.

- If you hold the pointer over a bin, an InfoTip displays the number of nets and the range of capacitance values in the bin.  
An InfoTip might read, for example, Range: 0.08 to 0.496 Contents: 35.
- If you click a bin to select it, the bin turns yellow and the capacitance value and net name for each net appears in the table to the right of the histogram.

### See Also

- [Net Capacitance Histograms](#)

## Analyzing Timing Path Collections

You can use the path analyzer to analyze a collection of timing paths and determine where timing failures occur in the design. The path analyzer analyzes the paths using a rule that you specify, categorizes them based on available attribute values, and displays the categories in a color-coded treemap view. You can select a predefined category rule or define a custom category rule. You can also add subcategories.

The path analyzer allows you to perform custom trend analysis on collections of timing paths. For example, you can

- Categorize paths by path group to see if timing violations are specific to a particular path group
- Create a custom category rule for paths with slack violations of more than one clock cycle to determine whether you need to specify multicycle path constraints on the paths
- Categorize the paths by their start clock and end clock values to identify cross-domain paths, which are the paths where these values are not the same

You can also tag appropriate blocks with block marks, and then categorize the paths by using the block mark attribute. This allows you to see if timing path failures result from a certain block in the design.

To open the path analyzer, choose **Timing > New Path Analyzer**.

The path analyzer window is divided into two panes, with a categories tree on the left and a treemap view on the right. You can adjust the relative widths of these panes by moving the split bar left or right.

You must load and categorize the timing paths before you can view them in the treemap.

To load a collection of timing paths,

1. Specify the collection in the Collections box.

You can enter the collection name or a Tcl command that creates the collection.

2. Click **Apply**.

To categorize the timing paths,

1. Select **All** in the categories tree.
2. Click the **Create** button.

The **Create Category** dialog box appears.

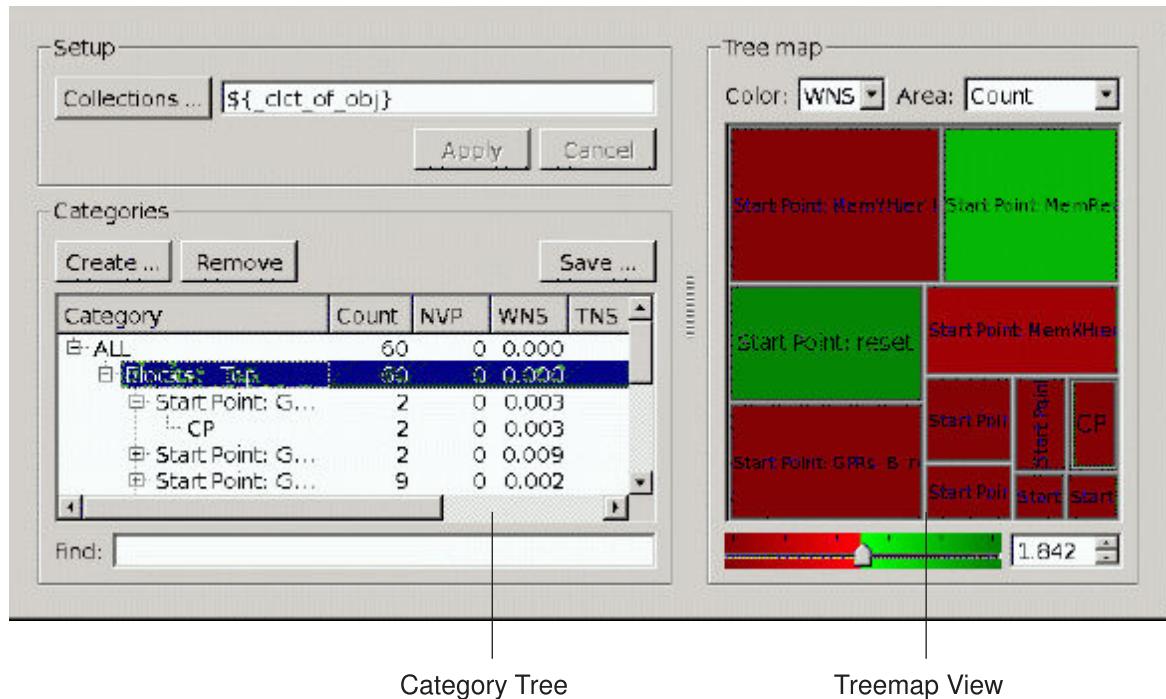
3. Select a rule.
4. Click **OK**.

You can load one or more collections of timing paths from the same design. For more information, see [Loading and Categorizing Path Collections](#).

After categorizing the paths, select **All** at the top of the category tree. The path analyzer displays the categories in the treemap view. The **All** category contains all the paths that you have loaded into the path analyzer.

[Figure 10](#) shows an example of the path analyzer after the path collections have been loaded and categorized.

*Figure 10 Path Analyzer Window*



The category tree on the left side of the window displays the categories and subcategories. Each row represents a category or subcategory. For each category, the columns display the following information:

- Category displays the category name.
- Count displays the number of paths in the category.
- NVP displays the number of violating paths.
- WNS displays the worst negative slack value.
- TNS displays the total negative slack value.
- TPS displays the total positive slack value.

To view the categories in the treemap, select All in the category tree. To view the subcategories for a category, select the category.

The treemap view on the right side of the window displays hierarchical data as a set of nested rectangles. Each category has its own rectangle, which can be tiled with smaller rectangles that represent subcategories.

- The area of a rectangle represents one dimension of the data, such as the total number of paths or the number of violating paths.
- The color of a rectangle represents the worst negative slack in the category. Red means the slack value is lower than the threshold value set at the bottom of the treemap view, and green means the slack value is higher than the threshold value. These colors also change from light to dark to indicate how far the WNS value is from the threshold value.

You can save the categorized paths in a Tcl script file that you can use later to reload the paths.

The treemap view displays the path categories as colored rectangles. The area of a rectangle is proportional to its value in the path data. By default, the rectangles represent the number of paths in each category. You can set the treemap to display the number of violating paths (NVP), the total negative slack (TNS), or the total positive slack (TPS).

- To display the categories in the treemap, select All in the category tree.
- To display the subcategories for a category, select the category.

To set the data type used to calculate the area for each rectangle in the treemap, select an option in the Count list. The choices are Count (the default), NVP, TNS, and TPS.

The color of each rectangle represents the worst negative slack (WNS) value in the category. Red means the WNS value is lower than the threshold value set at the bottom of the treemap view, and green means the value is higher than the threshold value. These colors change from light to dark to indicate how far the WNS value is from the threshold value.

To adjust the threshold value that controls the coloring of the rectangles, move the slide bar left or right, or enter a different value in the box to the right of the slide bar.

To select the paths in a category and make them the current selection in the tool, select Category Paths.

You can select a category to further analyze the paths in another tool.

To view the paths in a path data table, right-click and choose Create Data Table.

To view the distribution of slack in a histogram, right-click and choose Create Histogram.

The Table Histogram dialog box appears.

To view the distribution of slack shifted by a value that you specify,

1. Right-click and choose Shift Category.
2. Enter a value in the Shift Value list.

3. Select a category in the Histogram Category drop-down list.
4. Click OK.

The Table Histogram dialog box appears.

For details about using the Table Histogram dialog box, see [Creating Path Data Histograms](#).

#### See Also

- [Inspecting Timing Path Elements](#)
- [Creating Path Data Histograms](#)

## Loading and Categorizing Path Collections

Use the path analyzer when you want to perform custom trend analysis on collections of timing paths. For example, you can

- Categorize paths by path group to see if timing violations are specific to a certain path group.
- Create a custom category for paths with slack violations of more than a clock cycle to determine whether you need to specify multicycle path constraints on the paths.
- Categorize the paths by their start-clock and end-clock values to identify cross-domain paths, which are the paths where these values are not the same.

In addition, you can tag blocks with block marks and categorize the paths by using the block mark attribute. This allows you to see if timing path failures result from a certain block in the design.

Before you can view timing path data in the path analyzer, you must load and categorize the paths.

To load a path collection,

1. Specify one or more path collections by using one of the following methods:
    - Click the Collections button to open the Collections Dialog dialog box, select the options for the collections that you want to load, and click OK.
    - Enter the names of one or more collections in the Collections box.  
Separate the collection names with blank spaces.
- Alternatively, you can click the Collections button to open the Collections Dialog dialog box, select the options for the collections that you want to load, and click OK.

- Enter a Tcl command that provides a timing path collection.

The command must be enclosed in square brackets ([]), which indicates that the tool must evaluate the command to obtain the collection.

2. Click **Apply**.

You should specify only timing path collections. The path analyzer ignores collections that do not contain timing paths and objects, other than timing paths, within a hybrid collection, are also ignored.

**Note:**

When you open the timing status summary, the tool automatically creates a collection, named \_clct\_of\_obj, containing the paths that you loaded. If you reload the paths, the tool updates the collection.

The path analyzer uses rules based on timing attribute values to categorize the paths in a collection. You can select a predefined category rule or define a custom category rule. In addition, you can select a category and divide it into subcategories.

You can save the categorized timing paths in a Tcl script file that you can use later to reload the categorized paths.

To categorize the timing paths,

1. Select a category in the Categories list.
2. Click the Create button.

The Create Category dialog box appears.

The list at the top of the dialog box displays all the rules that are available.

3. Select a rule.

You can select a predefined rule or a custom rule that you have defined. For details about defining custom rules, see [Creating Custom Category Rules](#).

4. (Optional) Select an option to control how the rule is applied.

The choices are Selection, Siblings, and Leaf descendants. The default is Selection.

5. Click OK.

You can add or remove categories at any time.

To remove a category or all the categories,

1. Select the category that you want to remove.

To remove all the categories, select All.

2. Click Remove.

You can save the categorized paths in a Tcl script file that you can use later to reload the paths.

To save all the categories in a script file,

1. Click Save in the path analyzer window.

The Save Categorization dialog box appears.

2. Select a file or enter the file name in the File name text box.

3. Click Save.

When you source this file, the path analyzer removes the currently loaded paths and loads the categorized paths from the file.

## Creating Custom Category Rules

To create a custom category rule, you define a rule based on a timing attribute value. You define the rule by using a regular expression of the form `attribute_name operator value`

To create a new rule,

1. Click the Create Rule button in the Create Category dialog box.

The Create Rule dialog box appears.

2. Enter a rule name in the Rule text box.

This name is for reference only.

3. Enter a category name in the Category text box.

Alternatively, you can click the  button and select an attribute in the Category Attribute Chooser dialog box.

4. Enter a filter expression in the Filter text box.

Alternatively, you can click the  button and define a filter expression in the Filter Attribute Chooser dialog box.

5. Click OK.

The new category rule appears in the Create Category dialog box.

To define a filter expression,

1. Click the  button in the Create Rule dialog box.

The Category Attribute Chooser dialog box appears with a list of the available category attributes. Some attributes are grouped hierarchically. A folder icon () against a name indicates a hierarchical attribute group.

2. Move down an attribute group hierarchy, if necessary, to find an attribute.
  - To display the names of the attributes in a group, double-click the group name. The path to the attribute group appears in the Object hierarchy name drop-down list and the attribute type appears in the Type text box.
  - To move back up the hierarchy, select a path in the Object hierarchy name drop-down list.
  - To move up one level, click the button.
3. (Optional) Filter the list of attributes to view only the names of categories in which you are interested.
  - a. Enter a name or name pattern in the Filter all columns by pattern drop-down list.
  - b. Click the Apply filter  button.

To clear the filter and display the names of all the available attributes, enter a wildcard character (?) or (\*) and Apply filter  button.
4. Select an attribute in the list of attribute names.  
The attribute name appears in the Attribute box.
5. Select an operator in the Operator list.  
The available operators depend on the type of attribute you selected.
6. Enter an attribute value in the Value text box.
7. Click OK.

## Examining Timing Paths and Selected Logic

You can visually examine timing paths in your design by creating a schematic to display selected timing paths, design objects, or both. You can select the paths in another timing analysis tool, such as a histogram, the Timing Status Summary, a path data table, or the path inspector.

A schematic view displays individual timing paths or design logic in a flat, single-sheet schematic that can span multiple levels of hierarchy. Each timing path consists of the objects (cells, pins, and nets) that make up the path. A selected path appears as a series of net connections between pins or a pin and a port. Hierarchy crossings indicate places where a path traverses the design hierarchy.

To create a schematic of one or more timing paths,

1. Select the paths that you want to view.

You can select the paths in another timing analysis tool, such as the the path inspector or a path data table, or by choosing **Select > Paths From/Through/To** and setting options in the **Select Paths** dialog box.

2. Click the  button on the Schematics toolbar, or choose **Schematic > New Schematic View**.

When you create a schematic, a tab appears at the bottom of the workspace area, above the console. You can use this tab to return to the schematic view window after working with other views.

Initially, the full path is visible in the schematic view window. You can use the zoom and pan tools and commands to magnify and traverse the view. For details, see [Magnifying or Shrinking a View](#) and [Traversing a View](#). In addition, you can use the arrow keys to scroll vertically or horizontally through the view.

**Note:**

Text does not appear in a schematic view when it is below a certain size in pixels. Use the zoom tools and zoom commands to magnify the view if necessary to see object names in a path schematic.

You can view information about an object by holding the pointer over the object. The information appears in an InfoTip. The information content depends on the object type.

- Cell information can include the cell instance name and the full (hierarchical) cell name plus information about each input or output pin on the cell.
- Pin information can include the full (hierarchical) pin name, the pin direction, and the arrival time, transition time, and slack time values.
- Net information can include the full (hierarchical) net name, the total net capacitance value, the number of local fanouts, and the total number of fanouts.

Local fanouts are the loads that directly connect to the net when pin directions are considered. Total fanouts are all the loads on the net that are driven by the same source or driver, regardless of the directions of hierarchical pins. Total fanout is the same as the fanout number provided in the net report.

- Port information can include the full (hierarchical) port name, the port direction, and the arrival time, transition time, and slack time values.
- Hierarchy crossing information can include the direction of the crossing (down a level into a subdesign or up a level to the parent design) and the full (hierarchical) name of the subdesign or parent design.

To select objects in a path schematic, click the button on the Mouse Tools toolbar and click (or drag the pointer around) the objects you want to select. You can Ctrl-click objects to add them to the selection or Shift-click objects to remove them from the selection. Clicking in the background deselects all selected objects. For details, see [Selecting Objects in Graphic Views](#).

You can add or remove selected logic (cells, ports, or nets) in a path schematic,

- To add logic, select the objects you want to add, make the path schematic the active view, and choose Schematic > Add Selected.
- To remove logic, select the objects you want to remove and choose Schematic > Delete Selected.
- The objects are added or removed only in the active schematic view. The netlist is not changed and other schematic views are not affected.

**Note:**

InfoTips are disabled by default. To enable InfoTips, choose View > InfoTips.

A timing path can include long chains of buffers or inverters and multiple hierarchy crossings. To avoid examining the progression of a signal across buffer and inverter chains or through unimportant blocks, you can hide some objects by collapsing them into abstract metacells.

You can collapse buffer and inverter chains, buffer and inverter trees, or the objects in hierarchical blocks. You can also collapse unconnected pins into metapins.

- For a buffer or inverter chain or a buffer or inverter tree that results in a noninverted output, the metacell is similar to a buffer but has a thicker line width and darker color.
- For a buffer or inverter chain or a buffer or inverter tree that results in an inverted output, the metacell is similar to an inverter but has a thicker line width and darker color.
- For a buffer or inverter tree that results in both noninverted and inverted outputs, the metacell combines the appearance of both an inverter and a buffer.

The symbol has both inverted and noninverted outputs with the loads of the chain connected to the appropriate polarity output.

You can add or remove selected logic (cells, ports, or nets) in a schematic. You can also add fanin logic, fanout logic, or worst-case timing paths for objects that you select in a schematic. The tool makes these changes only in the active schematic view. The netlist is not changed and other schematic views are not affected.

When you add fanin logic, fanout logic, or timing paths, you can control whether the additions appear in the active schematic view or in a new schematic view. You can

- Add the logic or paths to the schematic in the active schematic view.
- Display only the selected objects and the additional logic or paths in the active schematic view.
- Add the logic or paths to the schematic and display it in a new schematic view.
- Display only the selected objects and the additional logic or paths in a new schematic view.

You can reorganize a schematic hierarchically and display rectangular boundaries for the top-level design and each hierarchical set of objects. In a multivoltage design with UPF power domains, you can color the boundaries based on the hierarchical power relationships of the design.

You can reverse and reapply changes that you make in a schematic view, such as adding logic, expanding a hierarchical cell, or displaying hierarchical boundaries. You can reverse the most recent action or sequentially reverse a series of actions. If you have reversed one or more actions, you can reapply the most recently reversed action or a series of actions.

## See Also

- [Schematic Views](#)

## Highlighting the Critical Path

You can use highlighting to identify the critical path in a schematic or layout view. When you highlight a timing path, the pins and ports on the path appear in a different color from the unhighlighted objects. Net connections appear in the highlight color to show the connections between the objects on the path.

### Note:

In a schematic, highlighted timing paths can traverse the design hierarchy. For details about moving up or down the hierarchy in a schematic view, see [Schematic Views](#).

To highlight the critical path,

1. Select the critical path by doing one of the following:
  - Select the path in the timing status summary.
  - Select the path in a path slack histogram.
  - Choose Select > Paths From/Through/To to open the Select Paths dialog box, and click OK.
2. Click the  button on the Highlight toolbar, or choose Highlight > Selected.

Highlighted objects and paths change to the highlight color when the selection color is removed. Click in the background to remove the selection color (white) by deselecting the objects or paths.

#### See Also

- [Highlighting Selected Objects or Paths](#)
- [Removing Highlighting](#)
- [Controlling the Highlight Color](#)

## Highlighting Maximum or Minimum Delay Paths

You can use highlighting to identify the minimum or maximum delay path through two or more objects in a schematic or layout view. You can highlight the maximum delay path, the minimum delay path, or the maximum or minimum delay path relative to either the rising edge or the falling edge of the clock.

When you highlight a timing path, the pins and ports on the path appear in a different color from the unhighlighted objects. Net connections appear in the highlight color to show the connections between the objects on the path.

#### Note:

In a schematic, highlighted timing paths can traverse the design hierarchy. For details about moving up or down the hierarchy in a schematic view, see [Schematic Views](#).

Before you can highlight the maximum or minimum delay path through two or more objects, you must select the path.

To highlight the maximum or minimum delay path through selected objects,

1. Choose Select > Paths From/Through/To.

The Select Paths dialog box appears.

2. Specify the path startpoint (From) and endpoint (To), and any throughpoints (Through) you want to include.

3. Select the delay type in the Delay type drop-down list.

The choices are max, min, max\_rise, max\_fall, min\_rise, and min\_fall. The default is max.

4. Click OK to select the path and close the Select Paths dialog box.

5. Click the  button on the Highlight toolbar, or choose Highlight > Selected.

Highlighted objects and paths change to the highlight color when the selection color is removed. Click in the background to remove the selection color (white) by deselecting the objects or paths.

### See Also

- [Highlighting Selected Objects or Paths](#)
- [Removing Highlighting](#)
- [Controlling the Highlight Color](#)

## Tracing Fanin or Fanout Logic With Highlighting

You can trace the fanin and fanout connections for a cell, pin, or port by highlighting them in a schematic view. The tool automatically adds any fanin or fanout logic that it needs to highlight if those objects are not already displayed in the schematic. You can enable or disable the trace highlight operation in all schematic views. Trace highlighting is enabled by default.

To enable or disable trace highlighting in schematics,

In a schematic, highlighted timing paths can traverse the design hierarchy. For details about moving up or down the hierarchy in a schematic view, see [Schematic Views](#).

To highlight the critical path,

- Choose Schematic > Trace Highlight.

A check mark next to the Trace Highlight command on the Schematic menu indicates that this operation is enabled in all schematic views.

To highlight the first fanin or fanout level for an object when trace highlighting is enabled,

1. Select the cell, pin, or port.
2. Choose Schematic > Add Next Fanin/Fanout Level.

Alternatively, you can double-click the cell, pin, or port.

The tool highlights the object and its fanin or fanout connections with the current highlight color in all schematic and layout views:

- For a cell, the tool highlights the cell, its pins, the nets connected to the pins, and the pins and cells connected to the nets.
- For a pin, the tool highlights the pin, its cell, the net connected to the pin, and the pins and cells connected to the net.
- For a port, the tool highlights the port, the net connected to the port, and the pins and cells connected to the net.

### See Also

- [Schematic Views](#)
- [Controlling the Highlight Color](#)

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## Examining Timing Path Details

The Timing Status Summary and path data tables provide detailed information about timing paths in your design. You can examine path details, such as attribute values, generate histograms based on path attributes, and select paths for in other tools, such as a schematic view or the path inspector.

Both the Timing Status Summary and a path data table contain a timing path table and a button bar.

- The timing path table displays a list of paths that you specify. The table columns show the startpoint name, endpoint name, and other details about each path. By default, the tool uses the `get_timing_paths` command.
- The button bar below the table provides buttons that you can use to
  - Select and display one or more paths in a schematic view
  - Generate a histogram for the value distribution of a specific attribute
  - Select and display an individual path in a path inspector window
  - Select one or more paths and generate a timing report (available only in the Timing Status Summary)

You can configure the table by hiding or displaying individual table columns, and you can save the path details in a text file. In the Timing Status Summary, you can also reload the table with a different collection of timing paths.

You can select paths in the timing path table and view or highlight in a schematic or layout view. The selected paths appear in the selection color, which is white by default.

If you want to view the cells connected to the selected paths, choose Select > Cells > Of Selected Paths. You can cross-probe selected paths by choosing AnalyzeRTL > Cross Probe to Source.

When you open the Timing Status Summary, or reload the paths if it is already open, you use the Select Paths dialog box to load a collection of paths into the timing path table. You can

- Set options in the dialog box and run the `get_timing_paths` command.
- Select and run a predefined collection command.  
You can load all selected paths or all highlighted paths.
- Enter a command to define and load a custom collection.

The tool adds the command to the list of predefined commands. If you define a custom collection in a variable, you can use the `get` command to load the paths from the collection.

The dialog box options are set by default to select the 20 timing paths with the worst slack times in the design. Click the Default button to reset the dialog box options to their default.

When you open a path data table, it displays information about the paths that you selected in the path analyzer.

To open the timing status summary,

1. Choose Timing > Timing Status Summary.

The Select Paths dialog box appears. When the timing status summary is open, you can access this dialog box by clicking the Reload button on the button bar.

2. Set dialog box options for the `get_timing_paths` command, or select the Load from command option and either select a predefined command or type a command.

The dialog box options are set by default to select the 20 timing paths with the worst slack times in the design, by running the `get_timing_paths` command. Click the Default button to reset the dialog box options to their default.

For more details, see [Configuring the Path Inspector](#).

3. Click OK or Apply.

A tab appears at the bottom of the workspace area, above the console. You can use this tab to return to the timing status summary after working with other views.

By default, the table lists the paths by increasing order of slack. You can use the Up Arrow and Down Arrow keys to scroll up or down in the table. You can also sort the list by the alphanumerical order of the contents in any column, adjust the column widths, and filter the path list.

To sort the timing path table,

1. Move the pointer into the heading of the column you want to sort.
2. When the pointer changes shape, click the column heading.

Click again if you want to reverse the sort.

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the column widths.

To resize a column in the timing path table,

1. Move the pointer over the right edge of the column you want to resize.
2. When the pointer changes shape, drag the column edge right or left to increase or decrease the width of the column.

You can filter the timing path table by limiting it to information based on a character string or regular expression that you define.

To filter the information in the timing path table,

1. Right-click and choose Filter.
2. Set options as needed in the Filter List dialog box.
3. Click OK.

For details about using the Filter List dialog box, see [Filtering Object Lists](#).

You can use buttons on the button bar to

- Load a different list of paths (ReLoad Paths button)
- Save the path details in a text file (Export button)
- Customize the table by hiding, displaying, or reorganizing table columns (Columns button)
- Analyzer paths in a schematic view, path inspector window, path data histogram, or timing report (Schematic, Inspector, Histogram, and Report buttons)

**Note:**

If the window is too narrow to display all the buttons, you can click the  button and choose a command on the menu that appears.

You can customize the timing path table by hiding, displaying, or reorganizing the columns.

To hide, display, or reorganize the table columns,

1. Click the Columns button, or click the  button and choose Columns.

The Show and Order Columns dialog box appears. Column names appear in the Visible columns list from top to bottom in the same order that they appear in the table from left to right.

2. Hide or display columns as needed:

- To hide a column, select the column title in the Visible columns list and click the  button.
- To display a column, select the column title in the Hidden columns list and click the  button.

3. Reorder the columns as needed:

- To move a column up in the Visible columns list, select the column title and click the  button.
- To move a column down in the Visible columns list, select the column title and click the  button.

4. Click OK.

If you want to save the information in the timing path table, you can export the entire table to a text file. The file is formatted with each path on a separate line and the column data delimited by commas. You can import this file into a spreadsheet program such as Microsoft Excel.

To save the path details in a text file,

1. Click the Export button, or click the  button and choose Export.

The Export dialog box appears.

2. Select or enter the name of the file you want to save the path details in.
3. Click Save.

To examine specific paths or path details side by side with the path data table, you can

- Select one or more paths and click the Schematic button to display graphic representations of the paths in a schematic view.  
For details, see [Schematic Views](#).
- Select a path and click the Inspector button to load detailed information about the path into a path inspector window.

For details, see [Inspecting Timing Path Elements](#).

- Click the Histogram button to generate a histogram that shows the distribution of values in one of the following columns: Slack, Endpoint Clock Skew, Arrival, or Required.

For details, see [Creating Path Data Histograms](#).

- Select one or more paths and click the Report button to generate a worst-path timing report for the path or paths.

For details, see [Reporting Worst Path Timing](#).

You can view timing paths in a schematic or layout view by selecting them in the timing status summary. When you select a path, it appears in the selection color, which is white by default, in any open schematic or layout view. You can highlight the selected path by choosing Highlight > Selected or select the cells on the path by choosing Select > Cells > Of Selected Paths.

You can cross-probe timing paths in the timing status summary by selecting the paths and choosing AnalyzeRTL > Cross Probe to Source. For more details, see [Cross-Probing Selected Timing Paths](#).

## See Also

- [Creating Path Data Histograms](#)

## Loading the Timing Paths

When you open the timing status summary view window or reload the timing path table, the Select Paths dialog box appears. To load the timing paths, you can

- Set dialog box options for the `get_timing_paths` command.
- Select a predefined collection command.

You can load all selected paths or all highlighted paths.

- Enter a command to define a custom collection.

The tool automatically adds the command to the list of predefined commands.

The tool displays the path names and other path information in the timing paths table, and displays the command you used to load the paths in the command display box below the button bar.

You can set dialog box options to

- Select a certain number of timing paths with the worst slack values in the current design.
- Select timing paths based on delay type and other criteria.
- Select individual timing paths to, from, or through specific inputs, outputs, or registers.

The dialog box options are set by default to select the 20 timing paths with the worst slack times in the design, by running the `get_timing_paths` command. You can reset the dialog box options to their default by clicking the Default button.

To load timing paths by setting dialog box options and running the `get_timing_paths` command,

1. Open the Select Paths dialog box.

Click the Reload Paths button in the timing status summary if it is open, or choose Timing > Timing Status Summary.

2. Make sure the Load the paths specified by options below option is selected.

This option is selected by default.

3. Set options as needed.

- To select the paths by using the default dialog box options, click OK.
- To display the timing status summary without loading timing paths in the table, click Cancel.

For details about setting Select Paths dialog box options, see [Selecting Timing Paths](#).

You can read the `get_timing_paths` man page in the man page viewer by clicking the  button.

To load timing paths by running a predefined collection command,

1. Open the Select Paths dialog box.

Click the Reload Paths button in the timing status summary if it is open, or choose Timing > Timing Status Summary.

2. Select the Load from command option.

3. Select a command in the Load from command list.

The tool provides the following prepackaged commands:

- To load all currently selected paths, select  
`get_selection -type path # Get selected paths`

- To load all currently highlighted paths, select

```
get_selection -name [gui_get_highlight -all...us] -type path ; # Get all highlighted paths
```

Any commands that you have already entered in the dialog box during the current session also appear in the list:

4. Click OK or Apply.

To load timing paths by entering a command to define a custom collection,

1. Open the Select Paths dialog box.

Click the Reload Paths button in the timing status summary if it is open, or choose Timing > Timing Status Summary.

2. Select the Load from command option.

3. Enter a command in the Load from command box.

You can enter any command that returns a collection of timing paths.

4. Click OK or Apply.

The tool adds the command to the Load from command list.

You can define a variable with a timing path collection, and then load the timing paths into the timing status summary by entering a command to retrieve the variable in the Select Paths dialog box. For example, to define a variable named my\_clct, enter the following command on the command line:

```
prompt> set my_clct [get_timing_paths -max_paths 10 -nworst 1]
```

To retrieve the collection in the Select Paths dialog box, enter the following command in the Load from command box:

```
get my_clct
```

## Inspecting Timing Path Elements

The path inspector provides tools you can use to examine various aspects of a timing path. When you select a path and open the path inspector, you can view path delay profiles and timing report information about the path.

The path delay profiles display the relative contributions of various clock launch and capture components to the delay and slack calculations of the timing path.

The timing report information appears in three parts: a path summary, a path elements table, and path slack details.

- The path summary provides information about the path attributes that identify the path, such as its path group, startpoint and endpoint, and delay type.
- The path elements table displays information about the elements of the path and their contributions to the path delay and slack calculation.
- The path slack details include information about the required and actual arrival times and the slack values. You can also copy the summary and paste them into text files, export the tables to text files, customize the element tables, and generate delay calculation reports for selected cells or nets.

You can load multiple paths and display the information for each path sequentially by changing from one path to another. You can also select and load different paths at any time when the path inspector is open.

You can use the path inspector to analyze detailed information about a timing path. You can

- View path profiles that represent the relative clock launch and capture delay contributions
- Examine timing report information that includes a path summary, path element data, and path slack data
- Perform additional analysis tasks such as selecting the path, highlighting the path, or finding text in the report information

You can load multiple paths and display the information for each path sequentially by moving between the paths. You can also select and load different paths at any time when the path inspector is open.

To open the path inspector,

1. (Optional) Select one or more timing paths that you want to inspect.

You can select the paths when you open the path inspector or open the path inspector first and then load the timing paths.

2. Choose Timing > New Path Inspector.

A new path inspector view window appears. For assistance using the path inspector, click Help at the bottom of the window.

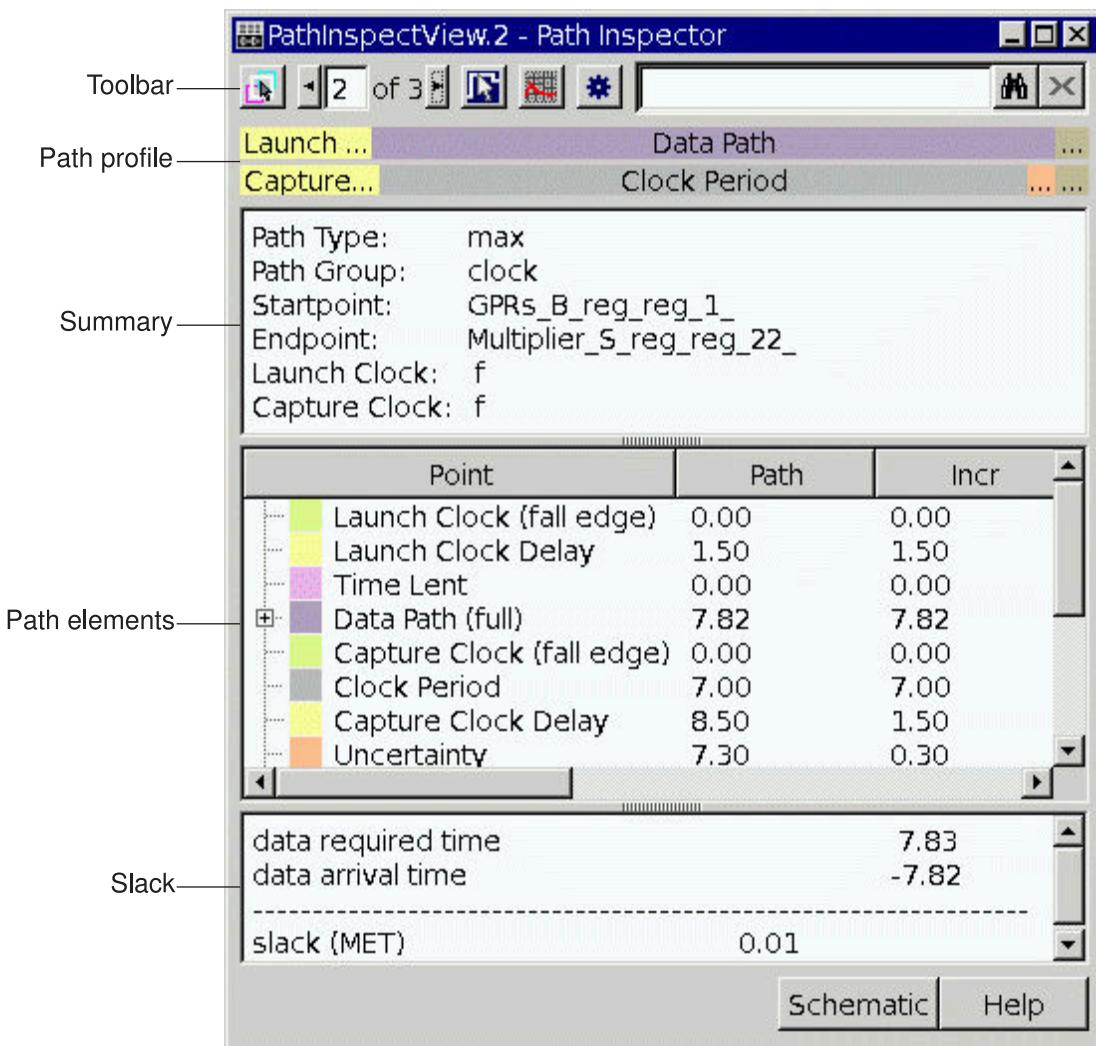
Alternatively, if a path data table is open, you can select the path in the table and click the Inspector button.

The path inspector view window contains a toolbar, launch and capture path profiles, and a timing report that is divided into three panes: summary, path elements, and slack.

- The summary pane displays a summary of the path attributes that identify the path, such as its path group, startpoint and endpoint, and delay type.
- The path elements pane displays a table with information about the elements of the path and their contributions to the path delay and slack calculation.
- The slack pane displays information about the required and actual arrival times and the slack values.

**Figure 11** shows an example of a path inspector window.

**Figure 11 Path Inspector Window**



You can search for text in the timing report sections. You can also select and copy text from the summary and slack sections.

By default, the path elements pane displays a table of timing path elements, such as datapath, clock period, and clock uncertainty. You can expand some elements, such as the datapath, by clicking the expansion button (plus sign) against the element name. Use the path elements table to view.

- A clock, pin, or net design object associated with a path element
- The launch clock path
- The capture clock path
- The timing path

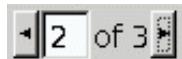
You can view information about a path element by holding the pointer over its row in the path elements table. You can also configure how the path elements table displays the data.

You can adjust the relative heights of the report panes by moving the split bars up or down. For information about configuring the path elements table, see [Configuring the Path Inspector](#).

To load timing paths in the path inspector,

1. Select the timing paths.
2. Click the button on the path inspector toolbar.

If you load multiple timing paths, the path inspector displays the number of paths on the toolbar and displays the path profiles and report data for the first path. You can move back and forth sequentially between the paths.



- To move to the next path, click the button.
- To move to the previous path, click the button.

You can select or highlight the path you are currently inspecting. You can also display the path in a schematic view.

- To select the path and make it the current selection in the tool, click the button.
- To highlight the path in the current highlight color, click the button.
- To display the path in a new schematic view, click the Schematic button at the bottom.

The launch and capture path profiles display the relative contributions of various components to the delay and slack calculations of the timing path. The components are color-coded to match elements in the path elements pane.

To view the delay contribution of a component in the path profile,

- Hold the pointer over the component.

An InfoTip appears showing the element name and the delay value.

You can search for information in the report panes by specifying a text string. The path inspector colors each occurrence of the text with a light-blue background and selects the first occurrence.

To find text in the summary and slack panes,

1. Enter the text in the text box on the path inspector toolbar.

2. Click the  button on the path inspector toolbar.

Repeat this step to select successive occurrences of the text.

To clear the search coloring, click the  button on the path inspector toolbar.

You can select text in the summary pane or the slack pane and copy it for use in another tool, such as a text editor.

To select and copy text in the summary or slack pane,

1. Select the text you want to copy by dragging the pointer over it, or right-click and choose Select All.
2. Right-click and choose Copy.

The path elements pane displays a table of timing path elements, such as data path, clock period, and clock uncertainty. You can expand some elements, such as the data path, by clicking the expansion button (plus sign) against the element name. Use the path elements table to

- View a clock, pin, or net design object associated with a path element
- View the launch clock path
- View the capture clock path
- View the timing path

You can view information about a path element by holding the pointer over its row in the path elements table. You can also highlight path elements.

- To highlight a path element, select its row, and then right-click and choose Highlight Object.
- To remove highlighting from a path element, select its row, and then right-click and choose Clear Highlight from Object.

You can cross-probe datapath cells on a timing path that you are inspecting in the path inspector. You can cross-probe the entire datapath or individual elements on the datapath. For details, see [Configuring the Path Inspector](#).

You can sort and resize the columns in the path elements table. You can also change the table format.

To sort the table alphabetically based on the contents of a column,

1. Move the pointer over the heading of the column you want to sort.

The pointer changes shape.

2. Click the column heading.

Click again if you want to reverse the sort.

To adjust the width of a column,

1. Move the pointer over the right edge of the column you want to resize.

The pointer changes shape.

2. Drag the column edge right or left to increase or decrease the width of the column.

To change the table format,

1. Move the pointer over the path elements table.

2. Right-click and choose Format to open the Format menu.

3. Choose a format option.

You can set additional configuration options by using the Configure the Path Inspector dialog box. To open this dialog box, click the  button.

For more details, see [Configuring the Path Inspector](#)

## See Also

- [Schematic Views](#)
- [Analyzing Timing Path Collections](#)

## Configuring the Path Inspector

You can configure the path inspector view window by setting options in the Configure the Path Inspector dialog box.

To configure the path inspector,

1. Click the  button on the path inspector toolbar.

The Configure the Path Inspector dialog box appears.

2. Select a row format option.

These options control how much information the path elements pane displays for the data path element.

- To display full data and clock path details, select the Full data and clock paths option.

**Note:**

The clock path details might not be available for some paths.

- To display full data path details but not clock path details, select the Full data path option.
- To display only the startpoint and endpoint of the data path, select the Short option.
- To hide the path elements and slack panes and display just the report summary, select the Summary option.

The Full data and clock paths option is selected by default.

3. Set the path visibility options to display or hide elements in the path elements table.

- To hide input pin data and display only driver pin data, deselect the Input pins option.
- To hide hierarchical pin data and display only leaf-cell pin data, deselect the Hierarchical pins option.
- To hide net data and display only pin data, deselect the Nets option.

These options are all selected by default, which means that the input pin, hierarchical pin, and net data appears in the path elements table.

4. Display or hide columns in the path elements table.

All the columns are displayed by default.

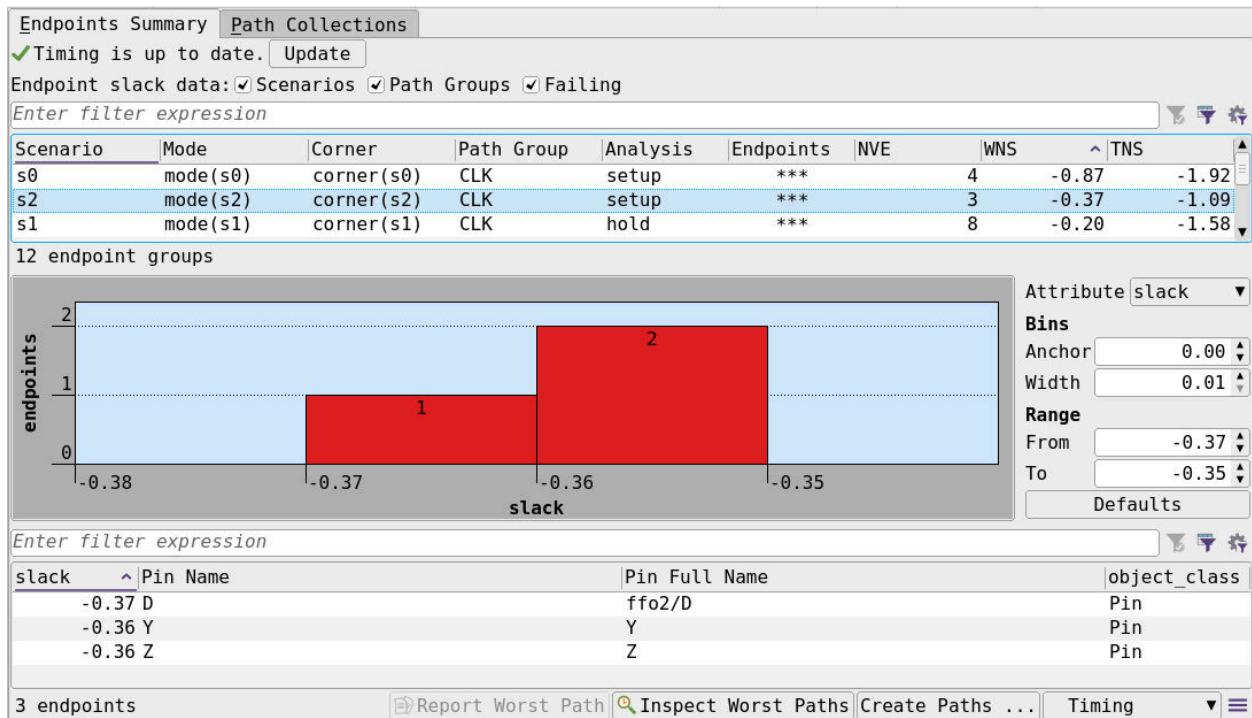
- To hide one or more columns, select the column labels in the Visible columns list and click the left arrow button.
- To display one or more columns, select the column labels in the Hidden columns list and click the right arrow button.
- To reorganize columns, select the columns you want to move left or right in the table and click the up arrow button or the right arrow button.

Repeat this step as needed to configure the columns.

5. Set other options as needed.
6. Click OK.

## Timing Status Summary

The Timing Status Summary panel has two tabs, the Endpoints Summary tab and the Path Collections tab. You can Select, Highlight, Inspect, or Report the worst paths. It also enables you to create path collections based on the selection in the endpoints table.



The Endpoints Summary tab provides the timing update. That is, it provides options to view the Scenarios, Path Groups, or Failing data to classify the endpoints data. It contains the endpoints table with histogram in which the histogram shows the data based on the

sorted columns. The table column can be configured by the Attribute groups. The Timing attribute is the default attribute group.

The Path Collections tab enables you to create and maintain path collections. It shows useful information of the path collection such as, Size, NVP,WNS, and TNS. You can use the Show Paths option to view the PathHist of the selected path collection.

### PathHist View

The PathHist view displays the specified path collection in the path table with histogram. The columns can be configured by the Attribute group. It shows the data distribution of the sorted column. From the path table, the related objects can be selected. For example, the pin, cell, net, or related timing path or timing points, startpoints, or endpoints, and so on. It can also show the selected objects in the PathInspect view and Schematic view.

---

## Creating Path Data Histograms

When you examine timing paths in the timing status summary or a path data table, you can create histograms to analyze the distribution of certain types of path details. Each histogram you create shows the distribution of values for the paths in the timing path table. You can create a histogram for values from any visible column that contains numeric data. By default, the columns that you can use are

- Slack
- Endpoint clock skew
- Arrival
- Required

#### Note:

You can also create histograms to analyze the slack distribution of categorized timing paths in the path analyzer. You can create a histogram to view the distribution of slack or the distribution of slack shifted by a value that you specify. For details, see [Analyzing Timing Path Collections](#).

To display a path data histogram,

1. Open the Table Histogram dialog box by using one of the following methods:
  - In the timing status summary or a path data table, click the Histogram button on the button bar (or click the  button and choose Histogram in the menu that appears).
  - In the path analyzer, select a category, and then right-click and choose Create Histogram.

- In the path analyzer, select a category, and then right-click and choose Shift Category.

The Shift Histogram dialog box appears. Enter a shift value and select a histogram category, and then click OK.

2. Select the histogram data type in the Column list.

The default is Slack.

**Note:**

Some of the labels and option settings in the dialog box change depending on which option you select in the Column list.

3. If you need to control the distribution of data values in the histogram, do one of the following:

- To increase or decrease the maximum number of bins, select the Number of bins option and change the value in the Number of bins box. The default is 8.
- To limit the range of values in each bin, select the Value range per bin option and enter a value in the Value range per bin box.

4. Set the other bin options as needed.

- To control the range of values (slack, endpoint clock skew, arrival, or required) used to generate the histogram, enter a minimum value in the box to the left of the <= symbol, a maximum value in the box to the right of the => symbol, or both.
- To set the exact minimum value limit, select the Lower bound strict option.
- To set the exact maximum value limit, select the Upper bound strict option.

By default, the Lower bound strict and Upper bound strict options are deselected, and the histogram shows the smallest possible range that encompasses all the values between the minimum and maximum values you specify.

5. Set the histogram options as needed.

- To set the maximum value for the y-axis, select or enter a value in the Y maximum list.

By default, the y-axis is automatically scaled to match the height of the tallest bin.

- To customize the histogram name, change the name in the Histogram title box.

The default name depends on the type of histogram data you select in the Column list.

- To customize the label for the x-axis, change the name in the X-axis title box.

The default label depends on the type of histogram data you select in the Column list.

- To customize the label for the y-axis, change the name in the Y-axis title box.

The default label depends on the type of histogram data you select in the Column list.

6. Click OK.

The histogram appears in a new histogram view window. The bins represent the number of paths (y-axis) versus their data values (x-axis).

The numbers at the top of each bin indicate the total paths in the bin. Green bins (on the positive side of 0) contain paths that met their constraints. Red bins (on the negative side of 0) contain paths that failed their constraints.

- If you hold the pointer over a bin, an InfoTip displays the number of paths and the range of values in the bin.

An InfoTip might read, for example, Range: 0.08 to 0.496 Contents: 35.

- If you click a bin to select it, the bin turns yellow and the value, startpoint name, and endpoint name for each path appear in the table to the right of the histogram.

When you select one or more paths in the table, you can display them in a schematic view by performing one of the following:

- Click the  button on the Schematics toolbar.
- Choose Schematic > New Schematic View.
- Right-click and choose Path Schematic.

For details about viewing schematics, see [Schematic Views](#).

## See Also

- [Viewing High-Level Timing Results](#)
- [Analyzing Timing Path Collections](#)
- [Examining Timing Path Details](#)

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## Viewing the Floorplan in Design Compiler Graphical Tool

The Design Vision tool layout view lets you analyze physical constraints, timing, and congestion in your floorplan. A layout view displays floorplan constraints, critical timing paths, and congested areas in a single, flat view of the physical design.

When you start the tool in topographical mode, you use the layout view to visually examine block and hierarchical cell placement, floorplan constraints, critical timing paths, and global routing congestion, and gather information that can help you to guide later optimization operations in the Design Compiler tool and other Synopsys tools.

You can view the floorplan before or after you optimize the design. To examine the floorplan in a layout view, you can

- Change your view of the design in a layout view, or change between layout views, by using the Overview panel
- Select, highlight, and query objects and magnify or shrink the view by using the interactive mouse tools
- Measure distances by drawing rulers
- View cell-to-cell or pin-to-pin connectivity by displaying net connections
- Visually analyze floorplan-related congestion by viewing the congestion map
- Visually analyze block and cell placement by coloring objects with visual modes

You can display or hide objects, control object selection, and customize object appearance by changing options on the View Settings panel. Objects you select or highlight in other views, such as a schematic view, are automatically cross-selected or cross-highlighted in the layout view. This capability allows you to efficiently examine both the layout and timing aspects of your floorplan.

You can view the floorplan before or after you optimize the design.

- Before you can view a design in the layout window, you must provide the necessary physical design setup information and link the design without any errors.

You can define the physical constraints by using a DEF file or physical constraints Tcl script. For more information, see the *Design Compiler User Guide*.

- To view the optimized design, you must either optimize the design during the current session or load it from a .ddc file.

For more information, see [Opening the Layout Window](#).

Before optimization, the layout window can display an elaborated GTECH design or a partially-synthesized design. You can use the layout window to

- Validate the physical constraints for your floorplan
- View the locations for block abstractions, physical hierarchy blocks, and preplaced macro cells

- View cross-selected standard cells that are mapped to specific locations by either the `set_cell_location` command or topographical technology virtual placement

You can select the cells in a logic design view such as the hierarchy browser or a schematic.

If you select unmapped GTECH cells or mapped standard cells that have not been assigned a location, they appear at the layout view origin (0,0).

**Note:**

The bounds, relative placement groups, the congestion map, and visual modes are not available in the layout window until you optimize the design.

After optimizing the design, you can use the layout window to

- Debug QoR problems related to the physical aspects of your design, including
  - Why particular cells have a given drive strength
  - Why particular timing paths contain long buffer chains that are not related to high fanout
  - Why particular I/O paths contain high concentrations of buffer
  - What causes the huge transition or capacitance on particular pins
- Validate any user-defined physical constraints that you applied to the design
- Analyze congested areas in the physical design

You can open multiple layout views to work simultaneously with different areas of the design. Each layout view displays the same flat view of the physical design.

To open a layout view,

- Choose **View > New Layout View**.

When the layout view appears, Design Vision tool displays a tab at the bottom of the workspace area. You can use this tab to return to the layout view after working with other views.

When you move the pointer over a layout view, the status bar displays the relative coordinates of the pointer position. If you select an object, the object name appears in the status bar.

Initially, the full design is visible in the layout view. You can quickly change your view of the design by clicking or dragging the pointer on the Overview panel, which by default is docked to the left side of the layout window. For more information, see [Navigating Through Layout Views](#).

You can magnify and traverse the design by using the zoom and pan tools and commands. For more information, see [Magnifying or Shrinking a View](#) and [Traversing a View](#). In addition, you can use the arrow keys to scroll vertically or horizontally through the view.

You can use interactive mouse tools to explore the physical design and examine objects and physical constraints in your floorplan. You can select objects, highlight objects, query objects, and draw rulers to measure object sizes or distances between objects. For more information, see [Selecting a Mouse Tool](#).

You can adjust layout view display properties by setting options on the View Settings panel.

- To control which types of objects are visible and which are hidden in a layout view, you can enable or disable visibility options on the View Settings Panel.

The die area is always visible. By default, the core area, ports, cells, and preroutes are visible, and other types of objects are hidden.

- To identify objects in the layout view, you can enable or disable visibility options that display object labels for ports, cells, site rows, bounds, or relative placement groups.

By default, cell labels are visible and the other object labels are hidden. You can also set an option that displays an object's label only when you select the object.

**Note:**

The text does not appear in a layout view when it is below a certain size in pixels. Magnify the view if necessary to see object labels in a layout view.

- To control which types of objects can be selected when you use the Selection tool in a layout view, you can enable or disable selection options on the View Settings Panel.

By default, selection is enabled for ports and cells and disabled for the other types of objects.

- To customize the appearance of objects in a layout view, you can change style properties such as color or fill pattern for individual object types or subtypes.

For example, you can use style properties to customize the layout view for a particular design or working environment. The default style properties are set for optimal viewing and work well for most designs.

You can save the current display property settings in your preferences file. For more information, see [Changing Layout Display Properties](#).

**See Also**

- [Solving Floorplan and Congestion Problems](#)

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## Using DFT Analysis Tools

If you are using the TestMAX DFT tool, you can access tools from the Test menu to DRC violations and hold time violations. For information about the test analysis views you can use, see the following sections:

- [Checking Scan Test Design Rules](#)
- [DRC Violation Browser](#)
- [Violation Inspector](#)
- [Viewing Test Protocols](#)
- [DFT Hold Time Analysis Window](#)

For more information, see the *TestMAX DFT User Guide*.

### See Also

- [Viewing High-Level Timing Results](#)
  - [Inspecting Timing Path Elements](#)
- 

## Checking Scan Test Design Rules

You should check the current design for DRC violations, fix any problems in the RTL, and resynthesize the design before performing other TestMAX DFT operations.

To check the current design for DRC violations, choose Test > Run DFT DRC.

The TestMAX DFT tool checks the design for DRC violations and displays messages in the console log view. You can click the underlined message numbers in the console log view to display man pages for the messages in the man page viewer.

If violations exist, the GUI automatically opens a new Design Vision window and displays the violation messages in the violation browser view window.

TestMAX DFT displays the following types of violation messages in the console log view:

- Information
- Warning

You should analyze these violations because they might exclude sequential cells from their scan chains.

- Fatal

You must fix these violations before proceeding because they prevent certain DFT Compiler commands from running.

The DFT DRC command requires a valid test protocol. You can generate a test protocol by using the `create_test_protocol` command or view an existing test protocol by using the `read_test_protocol` command. For details about these commands, see their man pages.

**Note:**

You can also check the design for DRC violations by entering the `dft_drc` command on the command line. For details, see the man page.

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## DRC Violation Browser

If you are using the TestMAX DFT tool, you can use the DRC violation browser to search for and view information about DFT unified DRC violations in the current design. The violation browser can display both static and dynamic violation messages. Static violations occur as a result of the design topology. For dynamic violations, you can view waveforms for pins on the violated path.

To open the DRC violation browser,

- Choose Test > Browse Violations.

The violation browser view window appears in a new Design Vision window at the left side of the window.

The violation browser window consists of two panes. A violation category tree appears in the left pane. When you select a violation category, a list of violations appears in the right pane.

- The violation category tree groups warning and error messages into categories that help you to find the problems you are interested in.
- The violation list displays the violation ID and pin name for each violation in the list.

You can select pin names and view information about the pins. You can also display man pages (in the man page viewer) for warning and error messages. If you want to visually inspect violations, you can display them in the violation inspector window.

To examine violations in the violation browser,

1. Click the expansion button (plus sign) against a violation category to view the violation groups in the category.
2. Select a violation group.

The violation IDs and pin names appear in the violation list.

3. (Optional) To filter the violation list, enter pin names or name patterns in the Include text box, the Exclude text box, or both, and click Apply.
  - a. To show only violating pins that match the names or name patterns, enter them in the Include text box.
  - b. To suppress violating pins that match the names or name patterns, enter them in the Exclude text box.

You can use the ? and \* wildcard characters to create name patterns. Separate multiple names or name patterns with blank spaces.

4. Select a violation in the violation list.

The violation error or warning message appears in the Description text box.

5. (Optional) To see the man page for the violation warning or error message, click Help.

The man page viewer appears and displays the man page. For details about using the man page viewer, see [Accessing Man Page Viewer](#).

6. To display violations in the violation inspector window, select the violations and click the Inspect Violation button.

The following section describes the violation inspector. For more information about the DRC violation browser, see the *TestMAX DFT User Guide*.

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## Violation Inspector

If you are using the TestMAX DFT tool, you can analyze and debug DFT unified DRC violations by inspecting them in a violation inspector window. You can inspect one or more violations of the same type. The violation inspector provides both a violation schematic for inspecting static violations and a coordinated waveform view for inspecting dynamic violations.

The violation inspector displays the pin data that corresponds to the most suitable pin data type for debugging the violation. If you need to, you can change to a different pin data type.

- The pin data for static violations is constant; the simulation values do not change over time.
- The pin data for dynamic violations represents simulation values for a series of initialization cycles.

For more information about pin data types, see the *TestMAX documentation*.

You can analyze and debug static violations by inspecting the design topology. Use the violation schematic to view and probe the signal and clock pins where the violations occur.

The violation schematic is an enhanced schematic. You can perform any schematic view operation in a violation schematic, including selecting objects, viewing object information, highlighting objects or timing paths, and magnifying and traversing the view.

To debug dynamic violations, you can select pins in the violation schematic and view their simulation values in the waveform view. Simulation values can be constant or they can vary over time in a series of simulation “events.” The violation inspector displays the pin data that corresponds to the most suitable pin data type for debugging the violation. To simulate pin data for a dynamic violation, you must use a pin data type that supports simulation values.

For more information about violation inspector, see the *TestMAX DFT User Guide*.

## Static DRC Violations

To display violations in a violation schematic,

1. Select one or more pin names in the DRC violation browser.

For details about using the violation browser, see [DRC Violation Browser](#).

2. Click the Inspect Violation button.

A violation schematic appears in a violation inspector view window. The schematic displays contextual information and details about the violation and its components. Red-colored cells indicate pins with violations.

3. (Optional) Select a data type in the Pin data type list.

By selecting a pin data type, you change the pin data that appears in the violation schematic. The default pin data type is Clock off.

The other options are:

- a. Clock on
- b. Clock off
- c. Constraint value
- d. Load
- e. Master observe
- f. Shadow observe
- g. Shift
- h. Stability patterns

i. Test setup

j. Tie data

Some pin data types provide additional choices.

- a. If you select the Shift data type, select a shift character in the Character list that appears.

The choices are the letters A through Z. The default is S.

- b. If you select the Clock on data type, select a pin name in the Clock pin list that appears.

For descriptions of the pin data types, see the section about displaying pin data in the *TestMAX ATPG User Guide*.

4. Display the object information in an InfoTip by moving the pointer over a pin, cell, net, or other type of object.

- Pin information includes the cell name, pin direction, and simulation values.
- Cell information includes the cell name and the names and directions of the attached pins.
- Net information includes the net name, local fanout value, and fanout value.

If you define a test pin with the `set_dft_signal` command, the pin appears with a hatched fill pattern and the InfoTip displays the pin information.

5. View and probe the violation schematic as needed. You can

- Magnify the view as needed to read the annotations near a pin symbol.

Symbol annotations (name, properties, and so forth) appear near the symbols and the text scales when you magnify or shrink the view

- Select a pin, cell, or net if you need to view other information such as object properties or a report
- Add fanin or fanout logic and timing paths to the schematic
- Remove (hide) selected logic
- Highlight selected objects and timing paths

For details about working in a schematic view, see [Schematic Views](#). You can also display or hide object names or annotations by setting options in the Application Preferences dialog box. For details, see [Setting GUI Preferences](#).

Design Vision tool can display custom symbols in violation schematics. Missing cell symbols automatically appear as black boxes with the same number of input and output pins. You can identify internal pins that TestMAX DFT treats as virtual ports by their color and the information in their Info Tips.

You can select objects in other views and add the objects to the violation schematic. Design Vision tool also adds any connecting logic (nets, pins, and so forth) between the selected objects.

To add selected objects,

1. Select the objects you need to add.

For example, you can select objects in a schematic view, histogram view, or by using commands on the Select menu.

2. Click the Add button in the violation inspector.

If your design contains Core Test Language (CTL) models, the violation schematic displays them as black boxes with a hatched fill pattern to distinguish them from other cells. You can display feedthrough and scan connection net connections for a CTL model. This allows you to examine information about the logic that drives, or is driven by, the problem path.

To display feedthrough net connections for a CTL model,

1. Select an input or output pin on the model.
2. Right-click and select Show feed throughs.

To display scan connection net connections for a CTL model,

1. Select an input or output pin on the model.
2. Right-click and select Show scan chain connectivity.

Design Vision tool retains multiple violation schematics in the violation inspector, but only the most recent schematic is visible. For example, when you add or remove logic, Design Vision generates a new violation schematic and saves the old schematic on a memory stack. You can browse the memory stack and sequentially redisplay the violation schematics.



Click ( in the violation inspector to redisplay the violation schematic most recently saved on the memory stack.



Click ( in the violation inspector to return to the violation schematic that is visible before you redisplayed the current schematic.

## Dynamic DRC Violations

The pin data for dynamic violations represents simulation values for a series of initialization cycles. To debug dynamic violations, you can select pins in the violation schematic and view their simulation values in the waveform view. Simulation values can be constant or they can vary over time in a series of simulation events.

The violation inspector displays the pin data that corresponds to the most suitable pin data type for debugging the violation. To simulate the pin data for a dynamic violation, you must change to a pin data type that supports simulation values.

To display waveforms for pins with dynamic violations,

1. Select one or more pin names in the DRC violation browser.

For details about using the violation browser, see [DRC Violation Browser](#).

2. Click the Inspect Violation button.

The violation schematic appears in a violation inspector view window. Red highlighting on a cell indicates pins with violations.

The pin data type appears in the Pin data type list.

Examine the violation schematic as needed. For details about working in a violation schematic, see [Inspecting Static DRC](#).

3. To display the waveform view, select Test setup in the Pin data type list.

The waveform view appears below the schematic view in the violation inspector window. You can adjust the relative heights of these views by dragging the split bar up or down.

The waveform view consists of two panes: an expandable signal list on the left and the waveform viewer on the right. You can adjust the relative widths of the panes by dragging the split bars left or right.

4. Select one or more objects (pins, cells, nets, or buses) for the signals that you want to inspect.

5. Click Add to Wave view button.

The signal names and values appear in the signal list, and a waveform for each signal appears in the waveform viewer.

The signal list can contain signal names and group names. A signal name represents a pin or a net. A group can represent the pins on a cell or the nets in a bus, or it can consist of signal names that you select. For example, you can create one group for input signals and another group for output signals.

To create a group of signals, select one or more signal names in the signal name list and drag them over new group at the bottom of the signal name list.

To expand a group and display the signal names in the group, click the expansion button (plus sign) to the left of the group name.

**Note:**

When you select signal names in the signal list, the selection is confined to the waveform view. The global selection list does not change.

The waveform for a signal represents a sequence of events as the signal value changes over time. The local timescale above the waveforms represents the visible time range. The global timescale below the waveforms represents the full range of time values that are available for display.

To change the visible time range, drag the pointer left or right over the portion of the global time range that you want to view.

You can use the reference and target markers, C1 and C2, to measure the time between events. C1 marks the current event. C2 marks the event you want to measure. The number of events or time units between the markers appears in the marker region above the upper timescale.

- To move C1, click or drag the pointer in the marker region.
- To move C2, middle-click or drag the pointer with the middle mouse button in the marker region.

You can use the buttons below the global timescale to magnify or shrink the waveforms horizontally and to traverse the waveform display left or right from one event to another.

- Click (  ) to magnify the waveforms
- Click (  ) to shrink the waveforms
- Click (  ) to fit the waveforms in the visible display
- Click (  ) to traverse the waveforms forward to the next event
- Click (  ) to traverse the waveforms back to the previous event

You can move or copy signals into a group or from one group to another. You can also remove selected signals or clear the waveform view.

To move signals into a group or from one group to another,

1. Select the signal names in the signal list pane.
2. Drag the selected signals over the group name.

To copy signals into a group or from one group to another,

1. Select the signal names in the signal list pane.
2. Shift-drag the selected signals over the group name.

To remove signals from the waveform view,

1. 1. Select the signal names in the signal list pane.
2. 2. Click the Selected button.

To clear the waveform view, click the All button.

---

## Viewing Test Protocols

You can view details about the default test protocol and any user-defined test protocols that you created for the design. The details include the name, signal type, and active state for control signals and the name, rise time, and fall time for clock signals.

To view test protocols,

1. Choose Test > Browse Test Modes.

The Test Modes Details dialog box appears. Alternatively, you can open this dialog box by clicking the Test Modes button in the violation inspector window.
2. Select a test protocol name in the Test Modes list.
3. View the information in the Control Signals list and the Clock Signals list.
4. Drag the split bars to adjust the relative heights of these lists. You can also
  - Click the column heading to sort a list alphanumerically based on the contents of a column.
  - Drag a column edge left or right to adjust the width of a column.
  - Press the Up Arrow and Down Arrow keys to navigate a list.
5. To close the Test Modes Details dialog box, click OK.

---

## DFT Hold Time Analysis Window

If you are using the TestMAX DFT tool, you can use the hold time analysis window to view information about scan cells that have hold time violations. You can also select scan cells in the window for further examination with other analysis tools.

The hold time analysis window contains a scan cell table that displays a list of scan cells with hold time violations. The table columns show the scan cell names and other details about each cell. A button bar below the table lets you load a different list of scan cells, save the scan cell details in a text file, customize the table columns, and access other analysis tools.

To open a hold time analysis window,

- Choose Test > Hold Time Analysis.

The hold time analysis window appears.

By default, the table columns display the following details from left to right for each path:

- Slack value
- Scan cell name
- Startpoint name
- Endpoint name
- Scan chain number

If some of the text in a column is not available because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the column widths.

By default, the table lists the scan cells by increasing order of slack. You can use the Up Arrow and Down Arrow keys to scroll up or down in the table. You can also

- Sort the list by alphabetical order of the contents in any column
- Adjust the column widths
- Customize the scan cell table by hiding, displaying, or reorganizing the columns
- Filter the path list

You can filter the timing scan cell table by limiting it to information based on a character string or regular expression that you define.

For more details, see Configuring the Scan Cell Table.

You can use buttons on the toolbar below the scan cell table to

- Load a different list of scan cells (ReLoad Paths button)
- Save the scan cell details in a text file (Export button)
- Customize the table by hiding, displaying, or reorganizing table columns (Columns button)
- Access other analysis tools (Schematic, Inspector, Histogram, and Report buttons)

Alternatively, you can click () button and choose a command on the menu that appears.

By default, the scan cell table lists all scan cells that have hold violations. You can reload the table to display only scan cells on timing paths within a certain slack range.

If you want to save the information in the scan cell table, you can export the entire table to a text file. The file is formatted with each path on a separate line and the column data delimited by commas.

You can access other analysis tools to examine specific scan cells or certain path details side by side with the hold time analysis window. You can

- Select one or more scan cells and click the Schematic button to display graphic representations in a schematic view of the path or paths that contain the cells  
 For details, see [Schematic Views](#).
- Select one or more scan cells and click the Report button to generate a worst-path timing report for the path or paths that contain the cells  
 For details, see [Reporting Worst Path Timing](#).

## Generating and Implementing UPF Power Domains

You can create, review, or edit your IEEE 1801 power architecture by using the Visual UPF dialog box. You can create power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy. IEEE 1801 is also known as Unified Power Format (UPF).

To open the Visual UPF dialog box,

- Click the  button on the Power toolbar, or choose Power > Visual UPF.  
 If your design already contains power domains, information about them appears in the dialog box.

When you open the Visual UPF dialog box, you cannot access any other GUI features or enter commands on the command line until you close the dialog box.

To view online Help for the Visual UPF dialog box while it is open, click the Help button.

The Visual UPF dialog box contains the work environment for power domain generation. It displays the design hierarchy and power domains for the top-level design and its subdesigns (blocks and hierarchical cells).

You can use the Visual UPF dialog box to define your power intent any time before you compile the design. After compiling the design, you can open the dialog box to view information about the power domains, supply sets, and their properties, but you cannot make any changes.

The general flow for generating UPF power domains includes the following steps:

1. Define the power architecture.

Start by creating power domains, and then define their properties. Add or edit property values as needed, such as primary and secondary supply nets, power switches, and design elements. You can also define supply sets and their properties.

2. Review the generated UPF commands.

After defining the power architecture, review the UPF commands that the tool generates to verify that it meets your intent. If the commands are not satisfactory, return to step 1.

3. Create the power objects in your design.

You can either save the UPF commands in a UPF file and run the `load_upf` command, by clicking OK in the Visual UPF dialog box, or save the UPF commands in a Tcl script file by clicking the Save Script button.

When you click OK, the tool removes any existing power objects in the design and replaces them with the new power objects. The tool does not make any changes in the design until you click OK.

The Visual UPF dialog box is split into two panes:

- The pane on the left displays information about the design hierarchy and the power domains in five synchronized views.
- The pane on the right provides options for defining power domains, supply sets, and their properties on two tabbed panels.

For general information about the Visual UPF dialog box and its panes and views, see [Using the Visual UPF Dialog Box](#).

For descriptions of the views and panes in the Visual UPF dialog box, see [Using the Visual UPF Dialog Box](#). For general information about UPF and defining your power intent, see the *Power Compiler User Guide* and the *Synopsys Multivoltage Flow User Guide*.

---

## Defining the Power Architecture

To create a power domain, you specify the scope, which is the hierarchy level in the logic design where the domain is defined, a domain name that is unique within the scope, and whether the domain uses supply nets or a supply set as its primary power and ground. A supply set is a collection of power and ground supply nets that are not specific to a power domain. You can use a supply set within the scope in which it is defined and in scopes that are under it in the logic hierarchy.

A power domain is a group of elements in the design that share a common set of power supply needs. By default, all logic elements in a power domain use the same primary supply and primary ground, although you can optionally define additional power supplies. A power domain is typically implemented as a contiguous voltage area in the physical chip layout.

Each power domain has a scope and an extent.

- The scope is the level of logic hierarchy designated as the root of the domain.
- The extent is the set of logic elements that belong to the power domain and share the same power supply needs.

The scope is the hierarchical level at which the domain is defined and is an ancestor of the elements that belong to the power domain, whereas the extent is the actual set of elements that belong to the power domain.

Each scope in the design has supply nets and supply ports at the defined hierarchical level of the scope.

- A supply net is a conductor that carries a supply voltage or ground throughout a given power domain.

A supply net that spans more than one power domain is said to be “reused” in multiple domains.

- A supply port is a power supply connection point between two adjacent levels of the design hierarchy, between the parent and child blocks of the hierarchy.

A supply net that crosses from one level of the design hierarchy to the next passes through a supply port.

For information about defining power domains and their supply networks, see the following topics:

- [Creating and Removing Power Domains](#)
- [Associating Power Domains With Design Blocks](#)
- [Adding and Editing Power Domain Properties](#)

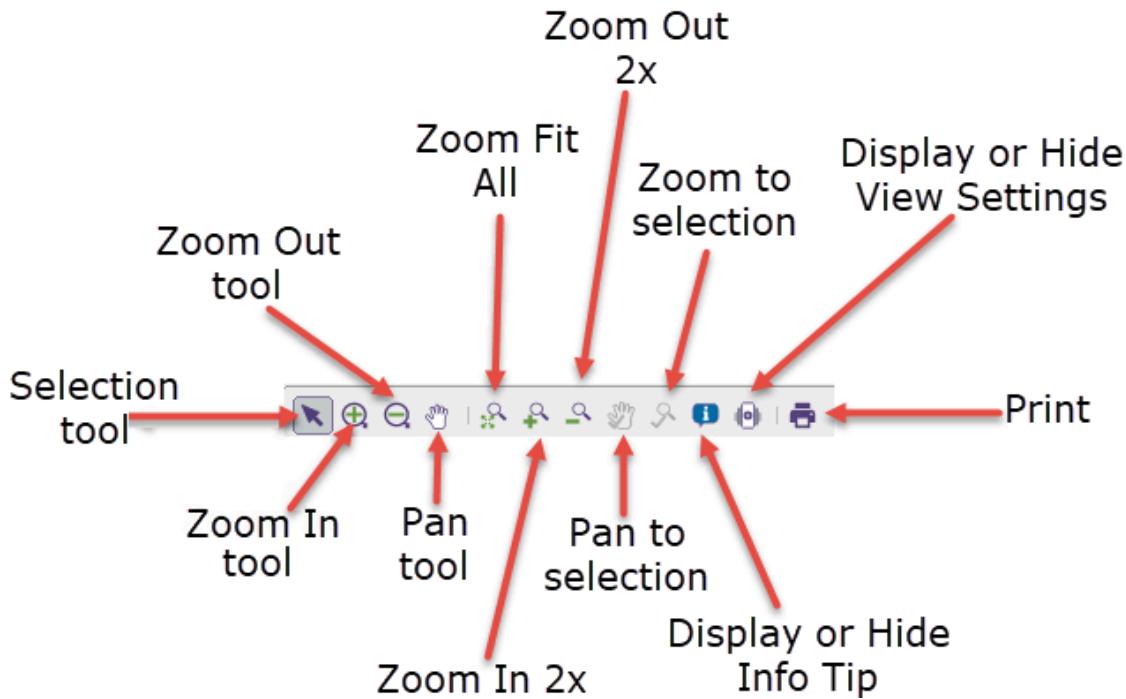
- Generating and Implementing UPF Power Domains
- Adding and Editing Supply Set Properties

## Viewing the UPF Diagram

You can view a graphic representation of the UPF power intent as it is currently defined in the Visual UPF dialog box. As you create power domains and add or edit properties, you should view this UPF diagram periodically to make sure the domains and their properties match your power intent for the design.

The diagram view is synchronized with the power intent defined by the UPF commands in the UPF script view. When you make changes to the commands, for example, by adding a property to a power domain, the tool immediately updates the diagram. The diagram can also display partial UPF data. For example, UPF requires a power switch to have an input supply net. However, if you define a power switch without specifying the input supply net, the diagram shows the switch without the input connection.

You can view the UPF diagram at any time by clicking the Diagram tab. Use the toolbar at the top of the view to magnify and traverse the diagram, select objects, view object information in an InfoTip, customize the appearance of the diagram, and print the diagram.



You can select objects in the UPF diagram the same way you select objects in a schematic view. When you drag the pointer to select or deselect objects in a rectangular

area, scopes and power domains are included only if they fit completely within the area. For more information, see [Selecting Objects in Graphic Views](#).

You can use the zoom and pan tools and commands that are available on the toolbar the same way you use them in a schematic view. You can also use the scroll arrows and scroll boxes on the diagram or the navigation keys on the keyboard to scroll through the diagram vertically or horizontally. For more information, see [Magnifying or Shrinking a View](#).

**Note:**

Text does not appear in a UPF diagram when it is below a certain size in pixels.

Use the zoom tools and zoom commands to magnify the view if necessary to see text in a diagram.

In addition, you can use buttons on the toolbar to enable or disable InfoTips, display or hide the View Settings panel, and print the diagram.

Following options are available on the toolbar:

- To enable or disable InfoTips in the diagram, click the  button.

When InfoTips are enabled, you can hold the pointer over an object to view its name, attribute values, and other information.

- To display or hide the View Settings panel, click the  button.

Alternatively, you can drag the vertical split bar between the panel and the diagram. When the panel is hidden, the split bar appears as a blue line at the left edge of the view.

When the View Settings panel is visible, you can use it to customize the appearance of the UPF diagram. For more information, see [Changing UPF Diagram Display Properties](#).

You can print the UPF diagram or save it in a PDF or PostScript file that you can print later.

To print the diagram,

- Click the  button on the toolbar to open the Print dialog box.

- Select a printer in the Name list.

The name of your default printer appears in the Name list by default.

- Set printer properties and options as needed.

- Click Print.

To save the diagram in a file that you can print later,

1. Click the  button on the toolbar to open the Print dialog box.
2. Select the file type in the Name list.
  - To save a PDF version of the view in a file that you can view or print later, select Print to File (PDF) in the Name list.
  - To save a PostScript version of the view in a file you can print later, select Print to File (Postscript) in the Name list.
3. Enter a file name in the Output file box.

Alternatively, you can specify the file name by clicking the browse button and selecting or entering the file name in the Print To File dialog box that appears.

4. Set printer properties and options as needed.
5. Click Print.

For more information about using the Print dialog box, see [Printing the UPF Diagram View](#).

To facilitate your analysis, you can collapse or expand individual scopes or power domains. Initially, all the scopes and power domains are expanded. By displaying or hiding the contents of particular scopes or power domains, you can visually inspect just the data that you are interested in viewing.

To collapse or expand scopes or power domains,

1. Select the scopes and power domains you want to collapse or expand.

You can use Shift-click and Control-click to select or deselect multiple objects.
2. Right-click and choose Collapse Selected Domains or Expand Selected Domains.

For explanations of the appearance and locations of the symbols in the diagram, see [UPF Diagram Symbols and Standards](#).

---

## Reviewing the UPF Commands

When you finish creating power domains and defining their properties, you should review the generated UPF commands. Check the data in the other views to make sure that they match your power intent. You can view the UPF commands at any time by clicking the UPF Script tab.

To add a marker to the script,

1. Select the line in the script where you want to place the marker.
2. Right-click and choose Add Marker.

To copy some or all of the script,

1. Drag the pointer over the lines you want to copy, or right-click and choose Select All.
2. Right-click and choose Copy.

---

## Saving a UPF Script and Implementing the Power Domains

You can save the UPF commands in a Tcl script file at any time. For example, you can save a partial script as a baseline or save a finished script to run later in a batch session.

To save the UPF script,

1. Click the Save Script button.
- A dialog box appears.
2. Select a file or type a file name in the File name box.
  3. Click Save.

When you are satisfied with the UPF commands that the dialog box has generated and have fixed all error messages and any critical warnings, you can save the commands in a UPF file and run the `load_upf` command to implement the power domains in your design.

To run the `load_upf` command, click OK in the Visual UPF dialog box.

---

## Creating and Removing Power Domains

In the Visual UPF dialog box, power domains are color-coded for quick recognition. The tool applies the power domain colors to the associated designs in the design hierarchy view as follows:

- When you define the default power domain for the top-level design or for a scope under the top-level design, the design or block appears in the domain color.

Any of its subblocks and hierarchical cells that are not explicitly assigned to a different power domain automatically become part of the default domain and appear in the domain color.
- When you assign a power domain to a subblock or hierarchical cell, the color on the cell name changes to the color for that domain.

You can create a default power domain for the top-level design and a default power domain for each scope that you define for a subblock or hierarchical cell. You can also create secondary power domains for individual subblocks or hierarchical cells within a scope. When you create a secondary power domain that uses supply nets, you can control whether the primary power net connects to a supply port in the top-level design or to a switch output port inside the scope.

To create a power domain,

1. (Optional) Select a subblock or hierarchical cell name in the design hierarchy view.
2. Click the Power Domains tab if it is not the active tab.

The Power Domains tab is active by default.

3. Click the Create button above the Power Domains legend.

The Create Power Domain dialog box appears.

4. Specify the scope for the power domain by entering the full name of a subblock or hierarchical cell in the Scope box.

Alternatively, you can browse for the cell name by clicking the browse button to open the Select Hierarchical Cell dialog box.

**Note:**

The Scope box must be empty if you are creating a power domain for the top-level design. The tool automatically creates the power domain under the top-level design if you do not specify a scope. Also, if you select a subblock or hierarchical cell then the full cell name appears in the Scope box.

5. Click Next.
6. Enter a domain name in the Creating new power domain box.

The default name for the top-level domain is TOP. The default naming convention for secondary power domains is PDn, where n is a positive integer. For the top-level design and for each scope, these domain names are numbered sequentially in the order that you create them.

7. (Optional) Set options as needed to define the primary power connection for the domain.

By default, the tool connects the primary power net for the domain to a supply port in the default domain of the scope.

- If you want to connect the primary power net to a switch output port inside the current scope, deselect the Connect primary power to a supply port in top design option.

**Note:**

This option is not available when you create the default power domain for the top-level design or a scope.

- If you want to connect the domain to a primary supply set, select the Use supply set option and specify the supply set.

By default, the Create new option is selected and the tool creates a new supply set automatically when you click Finish. If you want to connect the domain to an existing supply set, select the Use existing option and select the supply set in the Use existing list.

8. Click Finish.

The new power domain name and color appear on the Power Domains legend, and the basic power domain properties appear in the Power Domain Properties table.

After creating a power domain and assigning it to a hierarchical cell or subblock in the design hierarchy, you must provide values for some of its properties. You can also add properties later. For more information, see [Adding and Editing Power Domain Properties](#).

To remove a power domain,

1. Click the Power Domains tab if it is not the active tab.
2. Select the domain name on the Power Domains legend.
3. Click the Delete button.

## Associating Power Domains With Design Blocks

When you create the default power domain for the top-level design or a scope, any subblocks and hierarchical cells within the design or scope that are not explicitly assigned to a different power domain automatically become part of the default domain and appear in the domain color. However, when you create a secondary power domain, you must manually assign one or more subblocks or hierarchical cells as elements of the domain.

To assign an element to a power domain,

1. Select a subblock or hierarchical cell name in the design hierarchy view.
2. Right-click and choose Element Of to display a menu of power domain names.
3. Choose a power domain name.

Alternatively, you can assign elements to a power domain by typing their names in the Value box for the Element property in the property list on the Power Domain Properties pane. For example, you can assign a macro cell to a power domain by typing the cell name.

When you assign a hierarchical cell to a power domain, all of its subblocks are implicitly assigned to the domain, and are displayed in the domain color, unless you have explicitly assigned them to a different power domain. If you remove the explicit assignment of a block to a power domain, the block becomes implicitly assigned to the power domain associated with its parent cell.

To reassign a subblock to the power domain for its parent cell,

1. Select the cell name in the design hierarchy view.
2. Right-click and choose Clear.

---

## Adding and Editing Power Domain Properties

The Power Domain Properties table displays property names and values in two columns. The tool indicates required and preferred values with colored dots that indicate error and warning messages:

- Property values marked with a red dot are required.  
For guidance setting these property values, see the related error messages in the error and warning view.
- Property values marked with a blue dot are preferred but not required.  
For guidance setting these properties, see the related warnings in the error and warning view.
- Other property values are optional.

When you create a power domain, the basic properties for the domain appear in the Power Domain Properties table. The tool automatically assigns the Name, Top, and Scope property values and either the Primary Supply Set property value or the Primary Power and Primary Ground property values. For a default power domain assigned to a scope, the tool also assigns elements to the Elements property.

- Name specifies the name of the power domain.
- Top indicates whether the power domain is the default power domain for the top-level design.
- Scope identifies the scope in which the power domain is defined.
- Elements specifies the logic elements that belong to the power domain.

- Primary Supply Set specifies the supply set name if you assigned a supply set to the power domain.
- Primary Power and Primary Ground specify the names of the primary power and ground nets if you assigned the primary power net to the power domain.

**Note:**

You can change the Name property and either the Primary Supply Set property or the Primary Power and Primary Ground properties, but you cannot change the Top and Scope properties.

Some properties require input and other properties are assigned default that you can change. To add or change a property value, click the property value in the table and do one of the following:

- If an insertion point appears, type the value.
- If a list appears, select the value in the list.
- If the object chooser button appears, either type the value or click the button and select the value in the dialog box that appears.

You can filter the values listed in the dialog box. By default, the dialog box lists all of the valid values for the property.

You can add the following properties to a power domain:

- Default isolation set
- Default retention set
- Secondary power
- Switch
- Isolation strategy
- Retention strategy
- Level shifter strategy
- Extra supply set
- No extra supplies

To add a property for a power domain,

1. Click the Power Domains tab if it is not the active tab.
2. Select the domain name on the Power Domains legend.
3. Choose a command on the Create menu above the Power Domain Properties table.

- If you add a secondary power supply to a power domain under the top scope, a message appears asking if you want to connect the secondary power supply to a supply port in the top domain.

Click No to create the secondary power supply without connecting it to a supply port.

- If you add a secondary power supply to a power domain under another scope and it is not the top domain in the scope, a message appears asking if you want to connect the secondary power supply to a supply port in the top domain of the scope.

Click No to create the secondary power supply without connecting it to a supply port.

The tool adds the property in the Power Domain Properties table.

4. Add or edit property values as indicated by the red (required) or blue (preferred) dots in the Value column.

You must set values for properties marked with a red dot, and you should set values for properties marked with a blue dot. The other properties are optional.

You can remove properties that you create by choosing commands on the Create menu.

To remove a power domain property,

1. Click the Power Domains tab if it is not the active tab.
2. Select the domain name on the Power Domains legend.
3. Select the property in the Power Domain Properties table.
4. Click the Delete button above the table.

## **Creating and Removing Supply Sets**

You create a supply set by specifying a unique supply set name and the scope, which is the hierarchy level in the logic design where the supply set is defined.

1. (Optional) Select a subblock or hierarchical cell name in the design hierarchy view.
2. Click the Supply Sets tab if it is not the active tab.
3. Click the Create button above the Supply Sets legend.

The Create Supply Set dialog box appears.

4. Specify the scope for the supply set by entering the full name of a subblock or hierarchical cell in the Scope box.

Alternatively, you can browse for the cell name by clicking the browse button to open the Select Hierarchical Cell dialog box.

**Note:**

The Scope box should be empty if you are creating a supply set for the top-level design. Also, if you select a subblock or hierarchical cell, the full cell name appears in the Scope box.

5. Enter a supply set name in the Creating new supply set box.

The default supply set name is SSET1.

The default naming convention for supply sets is SSETn, where n is a positive integer. For the top-level design and for each scope, these supply set names are numbered sequentially in the order that you create them.

6. Click OK.

The new supply set appears on the Supply Sets legend, and the basic supply set properties appear in the Supply Set Properties table.

After creating a supply set, you must provide values for some of its properties. You can also add properties later. For more information, see [Adding and Editing Supply Set Properties](#).

To remove a supply set,

1. Click the Supply Sets tab if it is not the active tab.
2. Select the supply set name on the Supply Sets legend.
3. Click the Delete button above the legend.

---

## Adding and Editing Supply Set Properties

After creating a supply set, you must provide values for some of its properties. When you create a supply set, the tool automatically assigns the Name, the Scope, and the power and ground Function properties.

**Note:**

You can change the Name, but you cannot the Scope or the Function properties.

Some properties require input and other properties are assigned default that you can change. To add or change a property value, click the property value in the table and do one of the following:

- If an insertion point appears, type the value.
- If a list appears, select the value in the list.
- If the object chooser button appears, either type the value or click the button and select the value in the dialog box that appears.

You can filter the values listed in the dialog box. By default, the dialog box lists all of the valid values for the property.

You can add the following properties to a supply set:

- Power supply power state
- Ground supply power state

To add a property for a supply set,

1. Click the Supply Sets tab if it is not the active tab.
2. Select the supply set name on the Supply Sets legend.
3. Choose a command on the Create menu above the Supply Set Properties table.  
The tool adds the property in the table.
4. Add or edit property values as indicated by the red (required) or blue (preferred) dots in the Value column.

You can remove properties that you create by choosing commands on the Create menu.

To remove a supply set property,

1. Click the Supply Sets tab if it is not the active tab.
2. Select the supply set on the Supply Sets legend.
3. Select the property in the Supply Set Properties table.
4. Click the Delete button above the table.

---

## Using the Visual UPF Dialog Box

You can use the Visual UPF dialog box to create IEEE 1801 power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy. You can also review and edit an existing power architecture. IEEE 1801 standard is also known as Unified Power Format (UPF).

The Visual UPF dialog box contains the work environment for power domain generation. It displays the design hierarchy and provides the tools you use to define the power domains and supply sets for the top-level design and its subdesigns (hierarchical cells).

After you open the Visual UPF dialog box, you cannot access any other GUI features or enter Tcl commands until you close the dialog box. If you need to view online Help for this dialog box while it is open, click the Help button.

The Visual UPF dialog box is split into two panes, with tabbed views on the left side and tabbed panels on the right side.

The left pane displays information about the design hierarchy and the power domains in five synchronized views. The design hierarchy view is visible when you open the dialog box. The following tabs appear near the bottom of the pane.

- Design Hierarchy
- Diagram
- Power Hierarchy
- UPF Script
- Error/Warning

The right pane provides options for defining power domains and supply sets on two tabbed panels. The following tabs appear near the top of the pane:

- Power Domains
- Supply Sets

The power domains panel is visible when you open the dialog box.

For information about using the Visual UPF dialog box to define your power intent, see [Generating and Implementing UPF Power Domains](#).

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## Tabbed Views

The left side of the Visual UPF dialog box displays design and UPF information in five synchronized views. To display a view, click its tab.

- The design hierarchy view shows the relationships between the hierarchical cells in the design and their associated power domains.

This view appears by default when you open the Visual UPF dialog box. If your design already contains power domains, information about the power domains is color-coded in the design hierarchy view.

- The diagram view displays a UPF diagram that visually conveys the power intent as it is described on the power domains and supply sets panels.
  - The power hierarchy view displays information about the defined power domains and their supply networks.
  - The UPF script view displays the UPF commands that the tool generates as you define or modify power domains in the design hierarchy view.
  - The error and warning view displays error and warning messages.
- 

## Design Hierarchy View

The design hierarchy view shows the relationships between the hierarchical cells in the design and their associated power domains. If your design already contains power domains, the top-level design and its subblocks and hierarchical cells appear in the colors of their associated power domains when you open the dialog box.

The design hierarchy view displays colors on an expandable instance tree of hierarchical cells to show the relationships between the hierarchical cells in the design and their associated power domains. A hierarchical cell is an instance that contains subblocks. You can click the expansion button (plus sign) next to an instance name to expand the instance and show the names of the subblocks and hierarchical cells at the next level in the hierarchy.

- A plus (+) sign means you can click the button to expand the list and display the names of the subblocks within the cell.
- A minus (-) sign means you can click the button to collapse the list and hide the names of subblocks.

You can view the design hierarchy at any time by clicking the Design Hierarchy tab. To work with the design hierarchy, you can

- Select instances by clicking them or dragging the pointer over them.
- Click the expansion buttons next to the names of hierarchical blocks to further expand the instance tree.
- Use the arrow keys to navigate through the hierarchy.

Press the Up Arrow and Down Arrow keys to move up or down the tree, the Right Arrow key to expand a cell and the Left Arrow key to collapse a cell.

---

## Diagram View

The diagram view displays a graphic representation of the UPF power intent as it is currently defined. This diagram is synchronized with the power intent defined on the power

domains and supply sets panels. When you make changes in the dialog box, for example, by adding a property to a power domain, the tool immediately updates the diagram.

The UPF diagram displays the following objects, their connectivity, and their hierarchical relationships:

- Scopes
- Power domains
- Supply nets
- Supply ports
- Power switches
- Level shifter strategies
- Isolation strategies
- Retention strategies

For information about examining the UPF diagram, see [Generating and Implementing UPF Power Domains](#).

For explanations of the appearance and locations of the symbols in the diagram, see [UPF Diagram Symbols and Standards](#).

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## Power Hierarchy View

The power hierarchy view consists of two panes: an object hierarchy tree on the top and an object attribute table on the bottom. When you select an object in the object hierarchy tree, information about that object appears in the object attribute table. You can use the split bars between these two panes to increase or decrease their relative heights.

You can click the expansion button (plus sign) next to a power domain name to expand the power domain and show the names of the objects associated with the domain.

- A plus (+) sign means you can click the button to expand the tree and display the names of the objects associated with the power domain.
- A minus (-) sign means you can click the button to collapse the tree and hide the names of the objects.

You can view the power hierarchy at any time by clicking the Power Hierarchy tab. To explore the power hierarchy, you can

- Select the name of a power domain to display information about the associated power domain objects.
- Click the expansion buttons to further expand the object hierarchy tree.
- Use the arrow keys to navigate through the object hierarchy tree.

Press the Up Arrow and Down Arrow keys to move up or down the tree, the Right Arrow key to expand a domain, and the Left Arrow key to collapse a domain.

---

## UPF Script View

The UPF script view displays the UPF commands that the tool uses to create the power domains and power domain properties defined in the design hierarchy view. You can check the command syntax and verify option values. If you see problems with a command, you can fix them by modifying the relevant power domain definitions in the design hierarchy view.

You can select and copy some or all of the commands in the UPF script view. You can also save the script in a file. When you click OK, the tool saves the commands in a UPF file before running the `load_upf` command.

---

## Error and Warning View

The error and warning view displays error messages in red and warning messages in blue. You must fix all errors before you click OK in the dialog box. You should evaluate warning messages and fix warnings as needed for your power architecture.

---

## Tabbed Panels

The right side of the Visual UPF dialog box provides options for defining power domains and supply sets on two tabbed panels.

- The Power Domains panel provides a power domain legend and a power domain properties table that you can use to define power domains, add power domain properties, and set or change property values.
- The Supply Sets panel provides a supply set legend and a supply set properties table that you can use to define supply sets, add supply set properties, and set or change property values.

The Power Domains panel is visible when you open the dialog box.

---

## Power Domains Panel

The Power Domains tab provides access to the Power Domains legend and the Power Domain Properties table.

The Power Domains legend displays the name and color for each power domain defined in the design. When you select a power domain in the legend, its properties appear in the Power Domain Properties table.

The power domains are color-coded for quick recognition. When you create the power domain for the top-level design, the entire design hierarchy view appears in the domain color. When you assign subblocks or hierarchical cells to a different power domain, the cell name colors change to the domain color.

The Power Domain Properties table displays the properties in two columns: property name and property value. If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the column widths.

To resize a column in the object table,

1. Move the pointer over the right edge of the column heading in the column you want to resize.
2. When the pointer changes shape, drag the column edge right or left to increase or decrease the width of the column.

When you define or remove a power domain or add or edit a power domain property, the tool automatically updates the information in the design hierarchy, power domain hierarchy, and diagram views. If any information is missing or invalid, the tool displays error messages or warnings in the error and warnings view.

---

## Supply Sets Panel

The Supply Sets tab provides access to the Supply Sets legend and the Supply Set Properties table.

The Supply Sets legend displays the name of each supply set defined in the design. When you select a supply set in the legend, its properties appear in the Supply Set Properties table.

The Supply Set Properties table displays the supply set properties in two columns: property name and property value. If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the column widths.

To resize a column in the object table,

1. Move the pointer over the right edge of the column you want to resize.
2. When the pointer changes shape, drag the column edge right or left to increase or decrease the width of the column.

When you define or remove a supply set or add or edit a supply set property, the tool automatically updates the information in the design hierarchy, power domain hierarchy, and diagram views. If any information is missing or invalid, the tool displays error messages or warnings in the error and warnings view.

---

## Examining Power Management Cells

You can examine the power management cells in your design by viewing or highlighting them in schematic views. You can create a schematic that contains all the power management cells in the design, and you can highlight all the isolation cells, level-shifter cells, always-on cells, or always-on nets.

Following are the options available to examine power management cells:

- To open a schematic view of power management cells, choose Power > All PM Cells Schematic.
- To highlight isolation cells, choose Power > Highlight Cells > Isolation Cells.
- To highlight level-shifter cells, choose Power > Highlight Cells > Level Shifter Cells.
- To highlight always-on cells, choose Power > Highlight Cells > Always On Cells.
- To highlight always-on nets, choose Power > Highlight Cells > Always On Nets.

The tool highlights the cells or nets with the current highlight color in schematic and layout views.

### See Also

- [Viewing PG Pin Information for Selected Cells](#)
- [Querying the Supply Nets of Selected Pins](#)
- [Schematic Views](#)
- [Controlling the Highlight Color](#)

---

## Viewing PG Pin Information for Selected Cells

You can view a power pin report for cells that you select in a schematic view. You can also view PG pin information in a library report for selected cells. The tool displays the reports in the console log view.

To view a report of power pin information for selected cells,

1. Select the cells in a schematic view.
2. Right-click and choose Report Power Pin Information.

Alternatively, you can select the cells and enter the `report_power_pin_info [get_selection -type cell]` command

To view PG pin information in a library report of selected cells,

1. Select the cells in a schematic view.
2. Right-click and choose Report PG Pin.

Alternatively, you can enter the `report_lib` command with the `-pg_pin` option.

### See Also

- [Querying the Supply Nets of Selected Pins](#)
- [Schematic Views](#)
- [Examining Power Management Cells](#)

---

## Querying the Supply Nets of Selected Pins

You can create and view a collection of the related power supply nets or ground supply nets for pins and ports that you select in a schematic view. The tool displays the supply net names in the console log view.

To view a collection of the related power supply nets for selected pins or ports,

1. Select the pins or ports in a schematic view.
2. Right-click and choose Report Related Power Supply Nets.

Alternatively, you can select the pins or ports and enter the `get_related_supply_net [get_selection -type {pin port}]` command.

To view a collection of the related ground supply nets for selected pins or ports,

1. Select the pins or ports in a schematic view.
2. Right-click and choose Report Related Ground Supply Nets.

Alternatively, you can select the pins or ports and enter the `get_related_supply_net [get_selection -type {pin port}] -ground` command.

#### See Also

- [Viewing PG Pin Information for Selected Cells](#)
- [Examining Power Management Cells](#)
- [Schematic Views](#)

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## Defining and Viewing the Power Intent for Multivoltage Designs

The Design Vision tool supports IEEE 1801 power domains in multivoltage designs. IEEE 1801 is also known as Unified Power Format (UPF). In multivoltage design, the subdesign instances (blocks) operate at different voltages and the voltages of the various subdesigns are the same, but the blocks can be powered on and off independently. Except when stated otherwise, the term multivoltage as used that include multisupply and mixed multisupply-multivoltage designs.

Except when stated otherwise, the term multivoltage as used here includes multisupply and mixed multisupply-multivoltage designs.

To reduce power consumption, multivoltage designs typically make use of power domains that are independently powered up and down, including domains that are defined to have always-on relationships relative to each other. By definition, a power domain is a logical grouping of one or more hierarchical blocks in the design that share the same power characteristics.

A power domain has the following characteristics:

- The domain name
- A scope, which is the hierarchy level in the logic design where the domain is defined
- The design elements that comprise the domain
- An associated set of supply nets that can be used within the domain
- The primary power supply and ground nets
- Synthesis strategies for isolation, level-shifters, always-on cells, retention registers, and secondary power supply and ground nets

When used together, the power domain and supply network objects allow you to specify the power management intentions of the design. For more details, see the *Power Compiler User Guide*.

In the Design Vision GUI, you can generate the UPF commands that create power domains and define their supply networks. By using the Visual UPF dialog box, you can

- Define the initial power architecture
- Edit an existing power architecture
- Review an existing power architecture

You can examine the power management cells in your design by viewing them in a schematic or highlighting them in schematic and layout views. You can generate a schematic of all the power management cells in the design, and you can highlight isolation cells, level-shifter cells, always-on cells, or always-on nets. You can also cross-probe isolation cells in the power state table. For more information, see [Examining Power Management Cells](#).

You can examine a UPF diagram that can help you determine whether the domains you have defined match your power intent for the design. If you have defined power state tables in your design, you can use the Power State Table panel to perform always-on analysis and multivoltage level shifter analysis.

Design Vision provides tools that allow you to specify the power management intentions of the design. It also provides tools that can help you to analyze and debug multivoltage designs. In Design Vision tool, you can

- Generate the UPF commands that creates power domains and defines their supply networks automatically.
- Examine a UPF diagram that can help you determine whether the domains you have defined match your power intent for the design.
- Examine the power management cells in the design by viewing or highlighting them in schematic views.
- Analyze multivoltage design problems by checking the design for errors and viewing the violation report in the MV Advisor violation browser.
- Analyze path-based multivoltage design connections by generating and examining a report of level-shifter drive and load pins or a report of always-on nets.

You can also view the UPF diagram while you are defining the domains in the UPF dialog box.

To facilitate finding and fixing multivoltage design problems, you can check the design for violations and generate a report that you can examine in the MV Advisor violation

browser or in a Web browser. For more information, see [Checking Multivoltage Designs for Violations](#) and [Examining and Debugging Multivoltage Design Violations](#).

You can also analyze multivoltage design connections by generating a report of level shifter drive and load pins or a report of always-on nets. These reports allow you to gather design details that can help you to understand multivoltage-related design problems. For more information, see [Analyzing Multivoltage Design Connections](#).

For information about these subjects, see the following sections:

- [Visually Defining the UPF Power Intent](#)
- [Viewing the UPF Power Design](#)
- [Visualizing Power State Tables](#)

For more information, see the *Power Compiler User Guide* and the *Synopsys Multivoltage Flow User Guide*.

---

## Visually Defining the UPF Power Intent

You can use the Visual UPF dialog box to create UPF power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy. You can also review and edit an existing power design.

The Visual UPF dialog box contains the work environment for power domain generation. It displays the design hierarchy and provides tools you can use to define power domains for the top-level design and its subdesigns (hierarchical cells).

You can use the Visual UPF dialog box to

- Define the initial power design architecture

You can create power domains, define their possible states, and specify their elements. Most of this work requires an overview of the design hierarchy but does not require details, such as those provided by the UPF format.

- Edit an existing power design architecture

You can examine and modify an existing power design in which power domains and supply networks have already been defined. This allows you to define a power design incrementally or to make specific changes to resolve problems found in the initial design.

- Review an existing power design architecture

You can review the existing power domain structures and modify them if necessary to meet the requirements of your UPF specifications.

You can use the Visual UPF dialog box any time before you compile the design. After compiling the design, you can open the dialog box to view information about the power domains and their properties, but you cannot make any changes.

The general use flow for generating UPF power domains includes these steps:

1. Define the power design architecture.

Start by creating power domains and supply sets, and then define their properties. You can add or edit property values as needed, such as primary and secondary supply nets, power switches, and design elements for power domains. You can also create a power state table.

2. Review the generated UPF script.

After defining the power design architecture, review the UPF commands that the tool generates to verify that the power domain definitions they implement meet your power intent. If the commands are not satisfactory, return to step 1.

3. Create the power objects in your design.

You can either save the commands in a UPF file and run the `load_upf` command, by clicking OK in the Visual UPF dialog box, or save the commands in a Tcl script file by clicking the Save Script button.

You can examine information about the current power domains in your design and their power and ground supply networks by viewing a UPF diagram.

For more information, see the [Generating and Running a UPF Script](#) topic and the *Power Compiler User Guide*.

## See Also

- [Viewing the UPF Power Design](#)

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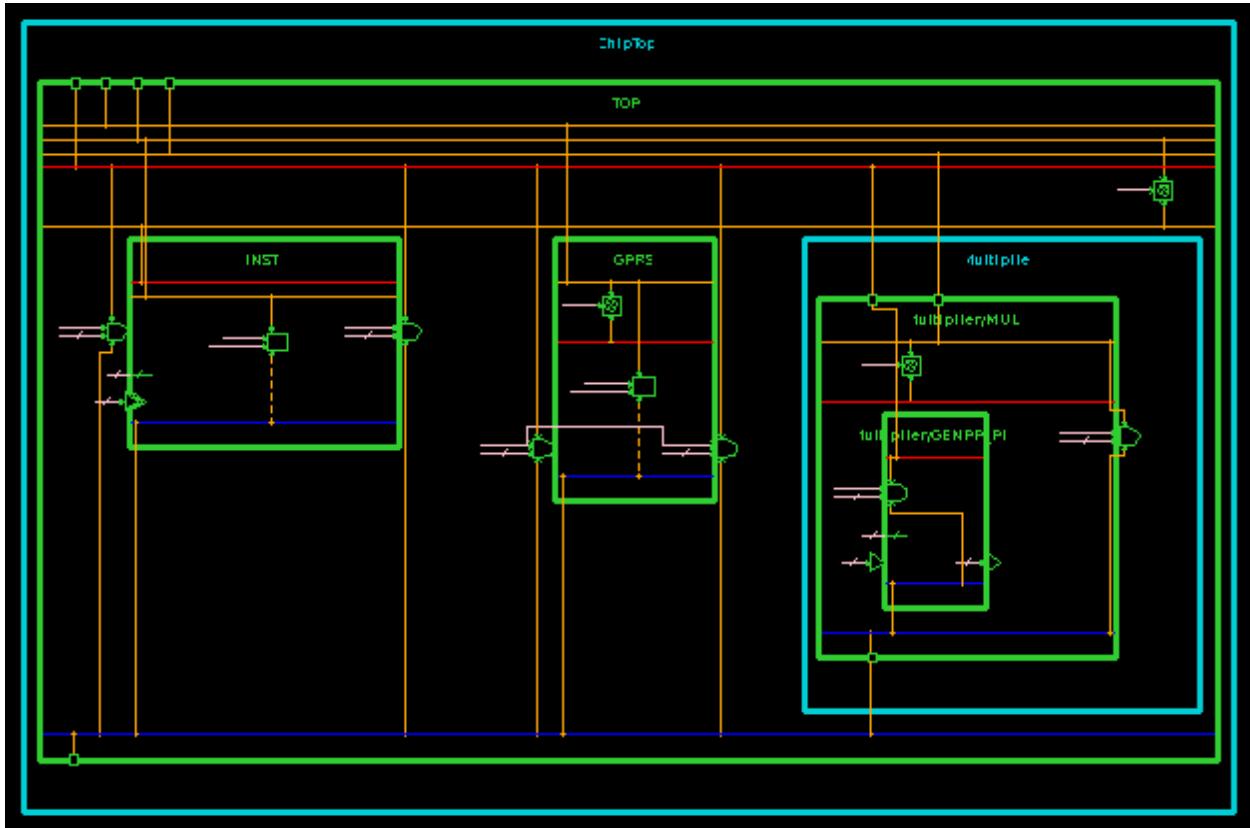
## Viewing the UPF Power Design

You can visually examine a graphic representation of the UPF power architecture in your design by using the UPF diagram view. The diagram displays graphic representations of UPF power domains and the supply network, switches, isolation, retention, and other power-management elements of your design. In this view, you can magnify and traverse the diagram, select objects, and view object information. You can also print the diagram and change the colors used for objects in the diagram.

The UPF diagram view displays the UPF power intent as it is defined in the design database. When you change the database, for example by entering a UPF command, the tool immediately updates the diagram. You can view the UPF diagram at any point in the design flow.

[Figure 12](#) shows many of the aspects of a UPF diagram.

*Figure 12 UPF Diagram Example*



To facilitate your analysis, you can collapse or expand individual power domains or scopes. Initially, all the power domains and scopes are expanded. By displaying or hiding the contents of particular power domains or scopes, you can visually inspect just the power architecture data that you are interested in viewing while hiding unrelated data.

To facilitate your analysis, you can collapse or expand individual power domains or scopes. Initially, all the power domains and scopes are expanded. By displaying or hiding the contents of particular power domains or scopes, you can visually inspect just the power design data that you are interested in viewing while ignoring unrelated data.

Initially, the full diagram is visible in the view. You can magnify and traverse the view by using the zoom and pan tools and commands. You can also use the arrow keys to scroll vertically or horizontally through the view. To examine the UPF diagram, you can

- Select individual objects or objects in a rectangular area by using the Selection tool.

**Note:**

The object selection is local in the UPF diagram view and does not change the global selection list in the tool.

- Preview object information in an InfoTip by holding the pointer over the object.
- Display object information on the Query panel by using the Query tool.

The View Settings panel provides options you can use to customize the appearance of the UPF diagram. You can adjust the brightness, change the colors for individual object types, change the background color, or apply a predefined or user-defined color theme.

You can print the UPF diagram displayed in the UPF diagram view or the Visual UPF dialog box. Make sure that a default printer is set in your .cshrc file. You can also save an image of the UPF diagram in a file for printing later from a UNIX or Linux shell.

The UPF diagram displays the following objects, their connectivity, and their hierarchical relationships:

- Scopes
- Power domains
- Supply nets
- Supply ports
- Power switches
- Level shifter strategies
- Isolation strategies
- Retention strategies

For explanations of the symbols used in a UPF diagram, see [UPF Diagram Symbols and Standards](#).

The UPF diagram displays the UPF power intent as it is defined in the design database. When you change the database, for example by entering a UPF command, the tool immediately updates the diagram.

To examine the UPF diagram, you can

- Select individual objects or objects in a rectangular area.

 Click the **Select** button on the Mouse Tools toolbar, and then click an object or drag the pointer around the objects you want to select. For more information, see [Selecting Objects in Graphic Views](#).

**Note:**

When you drag the pointer, any scopes or power domains you want to select must be completely enclosed within the rectangular area.

- Preview object information in an InfoTip by holding the pointer over the object.

The type of information displayed depends on the object type. You can enable or disable InfoTips in the current view by choosing View > InfoTip.

- Display object information on the Query panel.

 Click the **Query** button on the Mouse Tools toolbar, and then click the object. For more information, see [Querying Objects in Graphic Views](#).

**Note:**

Text does not appear in a UPF diagram when it is below a certain size in pixels. Use the zoom tools and zoom commands to magnify the view if necessary to see text in a diagram.

To facilitate your analysis, you can collapse or expand individual power domains or scopes. Initially, all the power domains and scopes are expanded. By displaying or hiding the contents of particular power domains or scopes, you can visually inspect just the power architecture data that you are interested in viewing while hiding unrelated data.

To collapse scopes or power domains,

1. Select the power domains and scopes you want to collapse.

You can use Shift-click and Control-click to select or deselect multiple objects.

2. Choose Power > UPF Diagram > Collapse Selected Domains.

To expand power domains and scopes,

1. Select the power domains and scopes you want to expand.

You can use Shift-click and Control-click to select or deselect multiple objects.

2. Choose Power > UPF Diagram > Expand Selected Domains.

If you have defined power states in your design, you can visually analyze the power state table by using the Power State Table panel. For more information, see [Visualizing Power State Tables](#).

You can control the colors of objects in the UPF diagram view. For more information, see [Changing UPF Diagram Display Properties](#).

You can also view a UPF diagram when you create a UPF script in the Visual UPF dialog box. For more information, see [Using the Visual UPF Dialog Box](#).

For more information, see the Viewing the UPF Power Design topic in the *Power Compiler User Guide*.

---

## Visualizing Power State Tables

You can use the Power State Table panel with the UPF diagram view to analyze and debug your isolation and level-shifter strategies in a UPF multivoltage design. You can view the states for each supply in a power state table and visually examine their relationships in the UPF diagram view.

You can perform the following types of analysis:

- Always-on analysis compares the on-off states between power and ground supplies
- Multivoltage level-shifter analysis compares the voltage relationships between power supplies

The UPF diagram displays a representation of the current UPF power implementation in your design. For information about viewing a UPF diagram, see [Viewing the UPF Power Architecture](#).

To display the Power State Table panel,

- Choose View > Toolbars > Power State Table.

The Power State Table command appears on the menu only when a UPF diagram view is open.

The names of the power state tables that you have defined in the design appear in the list at the top of the Power State Table panel.

Always-on analysis compares the on-off states between supplies, including both power and ground supplies. This analysis produces one of the following states: More AO, Less AO, Equally AO, and Unrelated AO.

To visually compare the on-off states between supplies,

1. Select Always On in the Analysis list on the Power State Table panel.
2. Select a power state table name in the list at the top of the panel.

The power state table appears in a table view with a column for each supply net and a row for each state. You can view the voltage for a particular supply and state by holding the pointer over the corresponding cell in the table.

3. Select a reference supply.

Right-click the column heading in the table and select Use name as Reference Supply where name is the supply net name in the column heading.

The supply net name appears in the Reference box. The tool compares all the other supplies in the power state table against the reference supply, displays the color legend at the bottom of the panel, and colors the supply nets in the UPF diagram view.

4. (Optional) Select one or more supply nets that you want to compare with the reference supply.

Right-click the column heading in the table and select Compare name with reference where name is the supply net name in the column heading and reference is the net name of the reference supply.

The supply net name appears in the Compare box. The tool compares this supply with the reference supply, adjusts the color legend at the bottom of the panel, and colors the supply nets in the UPF diagram view.

5. (Optional) To compare another supply net with the reference supply repeat step 4.

6. (Optional) To compare supplies to a different reference supply repeat steps 3 and 4.

To clear the analysis in the power state table and the UPF diagram view, right-click and select Clear All Comparisons option.

Multivoltage level-shifter analysis compares the voltage relationships between supplies. This analysis produces one of the following states: LH, HL, HL\_LH, or None. For more information, see Power State Table.

To visualize the voltage level relationships between power supplies,

1. Select MV Level Shifter in the Analysis list on the Power State Table panel.

2. Select a power state table name in the list at the top of the panel.

The power state table appears in a table view with a column for each supply net and a row for each state. You can view the voltage for a particular supply and state by holding the pointer over the corresponding cell in the table.

3. Select a supply.

Click the column heading in the table. The tool displays the supply name in the Supply box, displays the color legend at the bottom of the panel, and colors the supply nets in the UPF diagram view to show the type of level shifting required between the selected supply and the other supplies.

4. (Optional) Select a supply and a state.

Click the cell in the table. The tool displays the supply name in the Supply box and the state name in the State box, displays the color legend at the bottom of the panel, and colors the supply nets in the UPF diagram view to show the type of level shifting required between the selected supply and the other supplies for the selected state.

5. (Optional) To view the level shifter requirements for a different supply net repeat steps 3 and 4.

#### See Also

- [Power State Table Panel](#)

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## Analyzing Multivoltage Design Problems

The Design Vision GUI provides tools that can help you to analyze and debug multivoltage designs. In the GUI, you can

- Analyze multivoltage design problems by checking the design for errors and viewing the violation report in the MV Advisor violation browser
- Analyze path-based multivoltage design connections by generating and examining a report of level-shifter drive and load pins or a report of always-on nets

For information about these subjects, see the following sections:

- [Examining and Debugging Multivoltage Design Violations](#)
- [Analyzing Multivoltage Design Connections](#)
- [Checking Multivoltage Designs for Violations](#)

For more information, see the *Power Compiler User Guide* and the *Synopsys Multivoltage Flow User Guide*.

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## Examining and Debugging Multivoltage Design Violations

The MV Advisor violation browser provides a visual analysis and debugging environment for multivoltage design violations. You can check the design for problems such as multivoltage constraint violations, electrical isolation violations, connection rule violations, and operating condition mismatches. After checking a design, you can use the violation browser to examine the violation report.

The violation browser groups violations based on specific properties, displays detailed information about the violations, and guidance for investigating and fixing them. When you select a violation, the violation browser displays details such as an explanation of the warning or error message and suggestions for fixing the violation.

The violation browser also provides access to context aware reports and other analysis tools. You can

- Select pin names and view information about the pins
- Display man pages (in the man page viewer) for warning and error messages
- Visually inspect a violation by displaying it in a schematic view

You can also display the report for an individual violation in a new Design Vision window that serves as a debugging work environment.

You can check the design for violations before or after you open the violation browser. To check the design before opening the violation browser, use the `check_mv_design` command. When the violation browser is open, you can use the Check MV Design dialog box to check the design.

The violation browser takes a violation report that you generate by using the Check MV Design dialog box or the `check_mv_design` command, groups violations based on specific properties, and displays detailed information about the violation, including an explanation of the warning or error message, debugging information, and suggestions for fixing the violation.

The violation browser also provides access to context aware reports and other analysis tools. You can select pin names and view information about the pins. You can also display man pages (in the man page viewer) for warning and error messages. If you want to visually inspect a violation, you can display it in a schematic view.

## Opening the MV Advisor Violation Browser

To open the MV Advisor violation browser, click the  button on the Power toolbar, or choose Power > MV Advisor.

The MV Advisor violation browser window appears, and the tool displays a tab at the bottom of the workspace area, above the console. You can use this tab to return to the violation browser after working with other views.

The violation browser automatically loads the current violation report if a valid report is available for the current state of the design. If a valid report does not exist, the violation browser provides links that you can use to load the saved report or generate a new report. When you select a violation, the report view displays



To load a saved violation report,

1. Click the button or the open a report link.

The Open File dialog box appears.

2. Select the name of the report file you want to open, or type the name in the File name list.
3. Click Open.

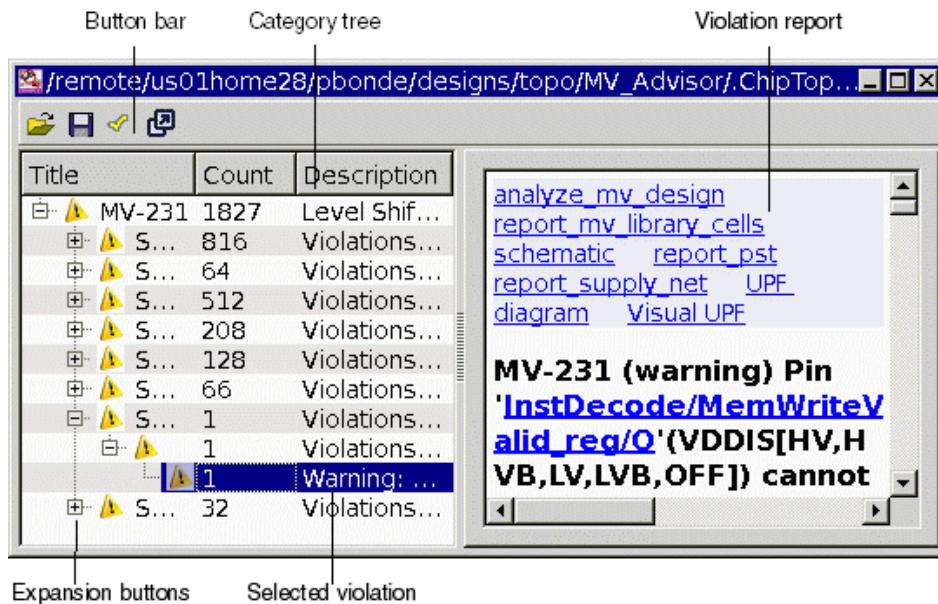
For details about generating a new violation report, see [Checking Multivoltage Designs for Violations](#).

**Note:**

When you open a report file, the violation browser compares the design name and the number of cells with the netlist in the current design, and displays a message if it finds any inconsistencies. If you need to evaluate the status of violations through the design flow or compare the reports from different design checks, you can open more than one report at the same time.

The MV Advisor violation browser view window consists of a toolbar at the top and two panes: a violation category tree on the left and a report view on the right. The violation category tree groups the violations into types, categories, and subcategories. You can use the expansion buttons in the category tree to expand or collapse individual types, categories, and subcategories. The report view displays information about the type, category, or violation that you select in the category tree.

The buttons on the toolbar allow you to open another violation report and to display the report for a selected violation in a new Design Vision window, where you can use other analysis tools to debug the violation. You can use the split bars between the panes to increase or decrease their relative widths.



The category tree consists of the following three columns:

1. Title: Displays the violation type for each category
2. Count: Displays the number of violations in each category or subcategory
3. Description: Displays a description of the category, subcategory, or violation

To explore the violation types and categories, and view the violations within each category, you can

- Expand violation categories, showing the subcategories or violations at the next level in the category tree.

To expand or collapse a violation category, double-click its line in the category tree or click its expansion button in the Title column.

A plus sign on the expansion button means the category is collapsed. A minus sign on the expansion button means the category is expanded.

- Select a violation type, category, or subcategory tree to display information about it in the report view.

When you select a violation type, the report view displays the generic violation message and the number of violations of that type found in the design.

When you select a violation category or subcategory, the report view displays the generic violation message, the number of violations in the category, and the location of the violations.

- Select a violation in the category tree to display a detailed report about it in the report view.

When you select a violation, the report view displays the warning or error message, a brief explanation of the message, and a detailed description of the violation that includes debugging information and suggestions for fixing the violation.

The following figure shows an example of the category tree for level shifter violations:

Type	Category	Subcategory	Violation
Title	Count	Description	
MV-231	1827		Level Shifter Violations
Sou...	32		Violations detected between source domain GP...
P...	1		Violations originated from pin GPRS/A_reg_req[1...
P...	1		Warning: Pin 'GPRS/A_reg_req[10]/Q' [VDDGS/HV...
P...	1		Violations originated from pin GPRS/A_reg_req[22]...
P...	1		Violations originated from pin GPRS/A_reg_req[21]...
P...	1		Violations originated from pin GPRS/A_reg_req[13]...
P...	1		Violations originated from pin GPRS/A_reg_req[1]/Q
P...	1		Violations originated from pin GPRS/A_reg_req[1]...
P...	1		Violations originated from pin GPRS/A_reg_req[3]/Q
P...	1		Violations originated from pin GPRS/A_reg_req[12]...
P...	1		Violations originated from pin GPRS/A_reg_req[1]...
P...	1		Violations originated from pin GPRS/A_reg_req[20]...
P...	1		Violations originated from pin GPRS/A_reg_req[28]...
P...	1		Violations originated from pin GPRS/A_reg_req[1]...
P...	1		Violations originated from pin GPRS/A_reg_req[8]/Q
P...	1		Violations originated from pin GPRS/A_reg_req[1]...
P...	1		Violations originated from pin GPRS/A_reg_req[6]/Q
P...	1		Violations originated from pin GPRS/A_reg_req[27]...
P...	1		Violations originated from pin GPRS/A_reg_req[31]...

For information about the types of violations that you can view in the MV Advisor violation browser, see [Checking Multivoltage Designs for Violations](#).

You can use the arrow keys on the keyboard to navigate through the category tree and to expand or collapse levels in the tree.

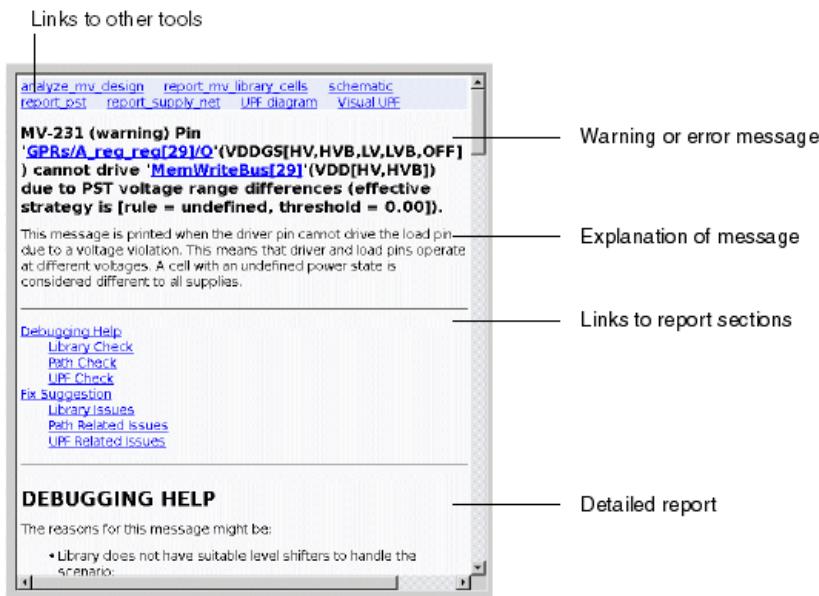
- To move up or down in the category tree, press the Up Arrow key or the Down Arrow key. To move to the top or bottom of the category tree, press the Page Up key or the Page Down key.
- To expand or collapse levels in the category tree, press the Right Arrow key or the Left Arrow key.

You can resize a column by moving the pointer over the right edge of the column heading and when the pointer shape changes, drag the column edge left or right.

**Note:**

You can also view the violation list (the information in the violation category tree) in a Web browser. For details, see [Checking Multivoltage Designs for Violations](#).

The following figure shows an example of a violation report in the report view when you select a violation in the category tree:



You can click the pin name in the warning or error message to select the pin. You can click links in the detailed report section to run commands and access useful tools.

You can use the arrow keys on the keyboard to scroll through the report view. To scroll up or down, press the Up Arrow key or the Down Arrow key. To move to the top or bottom of the view, press the Page Up key or the Page Down key.

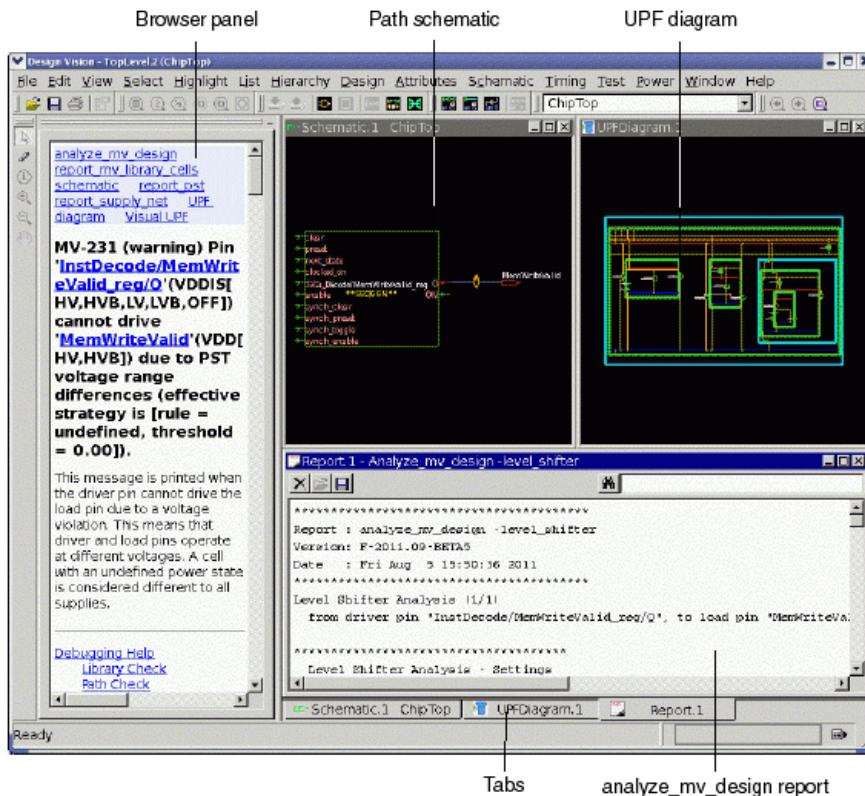
To analyze and debug a violation, you can open the report for the selected violation on the Browser panel in a new Design Vision window. By default, the Browser panel is attached to the left side of the window. You can use the workspace area in this window to debug the violation. Click the links at the top of the violation report to generate and display other reports and open analysis views such as a schematic view or a UPF diagram view.

To display the report for the selected violation in a new Design Vision window,

- Click the  button.

The new Design Vision window appears with the Browser panel attached to the left side of the window. The Browser panel displays only the report for the selected violation.

The following illustration shows an example of the debugging environment provided by the Browser panel in a new Design Vision window. For example, after displaying the violation report on the Browser panel, you can click links at the top of the report to display violation in a schematic view, open the UPF diagram view, and view reports in report views.



The links at the top of the report view allow you to run report commands and access other tools.

- To run the `analyze_mv_design` command and display the level shifter report in a report view, click the `analyze_mv_design` link.
- To run the `report_mv_library_cells` command and display the library cells report in a report view, click the `report_mv_library_cells` link.
- To run the `report_pst` command and display the power state table report in a report view, click the `report_pst` link.
- To run the `report_supply_net` command and display the supply net report in a report view, click the `report_supply_net` link.
- To view the violation in a schematic view, click the schematic link.

The schematic view appears. You can display the power domain boundaries by choosing Schematic > Show Logic/Power Hierarchy and color the boundaries by choosing Schematic > Color by Power Hierarchy. For details, see [Viewing Cells Hierarchically](#).

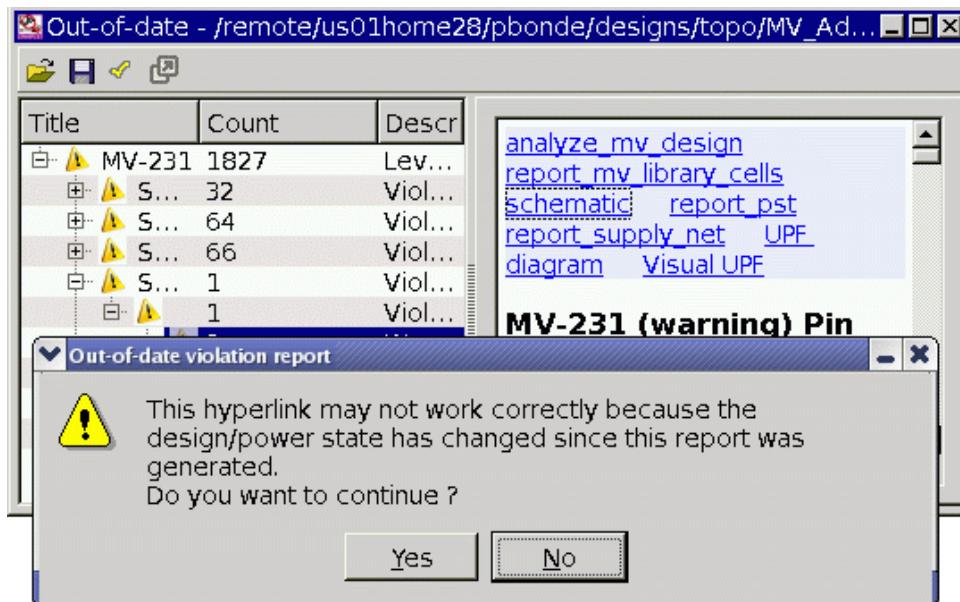
- To open a UPF diagram view, click the UPF diagram link.
- To open the Visual UPF dialog box, click the Visual UPF link.

The tool maintains a single, current repository for the multivoltage design violations that you can view in the MV Advisor violation browser. If you update the violation report that you are viewing, the tool automatically refreshes the report information in the violation browser.

To save the violation report you are viewing in a file,

1. Click the  button.
2. Select a report file name or type the name in the File name list.
3. Click Save.

If you view an out-of-date report in the violation browser, or if a change that you make in the design invalidates the report that you have open in a violation browser window, the term “Out-of-date” appears in the window title bar. In addition, the violation browser now restricts hyperlinks in an out-of-date report when a link action might update the design or manipulate design objects. If you click a restricted hyperlink, the tool displays a warning and prompts you to continue or cancel the link action.



If the warning appears, perform one of the following actions:

- To activate the link, click Yes.
- To cancel the link, click No.

Reports, schematics, the UPF diagram, and the Visual UPF dialog box all work with the up-to-date design. Commands that operate directly on an element reported in a violation, such as the `report_net` command, can cause an error if the element no longer exists in the design due to a previous action. Hyperlinks that are not restricted include internal HTML jumps, man page links, and links to preview commands.

---

## Analyzing Multivoltage Design Connections

You can analyze path-based multivoltage design connections by generating a report of level-shifter drive and load pins and a report of always-on nets. These reports allow you to gather design details that can help you to understand multivoltage-related design problems. They contain details about the variable settings for level-shifter insertion and always-on buffering, relevant power state tables, the driver-to-load pin connections, the pin-to-pin information for specified paths, the target libraries used for insertion of power management cells, and other useful debugging information.

Each report appears in a new analysis view. You can select and copy text in the view that you want to paste into another application, such as a text editor. You can click a hyperlink in the analysis view to generate a schematic containing the objects in the report. By using the schematic view, you can

- View power information for pins and cells
- Create collections of the power and ground supply nets connected to selected pins
- Generate reports of power pin information for selected cells

To display a report of level shifter drive and load pins,

1. Choose Power > Analyze MV Design.  
The Analyze MV Design dialog box appears.
2. Ensure the Level Shifter analysis type option is selected. By default, this option is selected.
3. (Optional) Type the name of a drive pin or top-level port in the From Pin box, or click the  button and select a pin name in the Object Collection Dialog dialog box.  
Alternatively, if the pin or port is currently selected, you can click the Selection button.
4. Enter the names of one or more load pins or top-level ports in the To Pin box, or click the  button and select the pin names in the Object Collection Dialog dialog box.

Alternatively, if the pins or ports are currently selected, you can click the Selection button.

5. Click OK.

Alternatively, you can display the report in the console log view and the shell transcript by using the `analyze_mv_design` command with the `-level_shifter`, `-from_pin`, and `-to_pin` options. For details, see the man page.

To display a report of always-on nets,

1. Choose Power > Analyze MV Design.

The Analyze MV Design dialog box appears.

2. Select the Always On analysis type option.

3. Type the net name in the Target Net box or select the net name from the drop-down list.

Alternatively, if the net is currently selected, you can click the Selection button.

4. Click OK.

Alternatively, you can display the report in the console log view and the shell transcript by using the `analyze_mv_design` command with the `-always_on` option. For details, see the man page.

The report appears in a new analysis view window. The command used to generate the report appears in the window title bar. You can select and copy text that you want to paste into another application, such as a text editor. You can also generate a schematic containing the objects in the report.

To select and copy text,

1. Drag the pointer over the text that you want to copy.

To copy the entire report, right-click and choose Select All.

2. Right-click and choose Copy.

For more details about multivoltage analysis reports, see the *Power Compiler User Guide*.

To generate a special schematic of the objects in the report, click the Schematic link at the top of the report.

The schematic view appears. You can display the power domain boundaries by choosing Schematic > Show Logic/Power Hierarchy and color the boundaries by choosing Schematic > Color by Power Hierarchy. For details, see [Viewing Cells Hierarchically](#).

For general details about viewing a schematic, see [Schematic Views](#).

When InfoTips are enabled, you can view power information for a pin or cell.

- Hold the pointer over a pin to display the related supply net and its possible power states and operation conditions.

Hold the pointer over a cell to display the name of the corresponding power domain and the available supply nets in the domain.

You can create collections of the power and ground supply nets for selected pins. To create a collection of the power supply nets connected to one or more pins,

1. Select the pins.
2. Right-click and choose Get Related Power Supply Nets.

The tool displays the net names in the console log view.

Alternatively, you can use the `get_related_supply_net` command.

To list the ground supply net connections for one or more pins,

1. Select the pins.
2. Right-click and choose Get Related Ground Supply Nets.

The tool displays the net names in the console log view.

Alternatively, you can use the `get_related_supply_net -ground` command.

You can generate a report of power pin information for selected technology library cells or leaf cells. This report contains power pin information for instantiated cells only and not for the library cells.

To generate a report of power pin information for one or more cells,

1. Select the cells.
2. Right-click and choose Report Power Pin Information.

The tool displays a power pin information report in the console log view.

Alternatively, you can use the `report_power_pin_info` command.

You can also generate a report of library information that lists power and ground pin information for selected cells. The power and ground pin information includes the PG pin definition and the PG type and voltage name to which a signal pin has been linked.

To generate a report of power and ground pin library information for one or more cells,

1. Select the cells.
2. Right-click and choose Report PG Pin.

The tool displays the power supply net names in the console.

Alternatively, you can use the `report_lib -pg_pin` command.

For more details about multivoltage analysis reports, see the *Power Compiler User Guide*.

---

## Checking Multivoltage Designs for Violations

You can analyze multivoltage design problems by checking the design for errors and generating a violation report that you can view in the console log view and save in a file. You can check the design for design errors such as multivoltage constraint violations, electrical isolation violations, connection rule violations, and operating condition mismatches. You can also examine a subset of the violation report in the MV Advisor violation browser or in a Web browser.

When you check the design, by using the `check_mv_design` command or the Check MV Design dialog box, the tool creates or updates the current violation report by default. If you specify a file name, the tool saves the report in the specified file and also creates the XSLT file with the same name plus an .xslt extension. If you do not specify a file name, the tool stores the current report information in a temporary file until the end of the current session.

- The violation report file is the XML file that contains the violations you can view in the MV Advisor violation browser or a Web browser.
- The XSLT file, `report_file.xslt`, contains auxiliary information required by the Web browser.

For details about using the MV Advisor violation browser, see [Examining and Debugging Multivoltage Design Violations](#). For details about the `check_mv_design` command, see the man page.

To generate or update the current violation report,

1. Click the  button or the run `check_mv_design` link in the MV Advisor violation browser.  
The Check MV Design dialog box appears.
2. Select or deselect check type options as needed to set the types of checks you need to perform.

By default, the tool performs all types of checks. To disable a check type, deselect its option.

- Use the isolation option to report electrical isolation errors with respect to power domains.
- Use the connection rules option to report violations in always-on synthesis and pass-gate connections.

- Use the clock gating style option to report the feasibility of clock-gate insertion on different hierarchical blocks.
- Use the opcond mismatches option to report incompatible operating conditions between instantiated technology cells and the parent design.
- Use the power nets option to report a summary of power and ground connections that cannot be derived.
- Use the target library subset option to report inconsistent settings among target libraries, target library subsets, and operating conditions.
- Use the level shifters option to report all existing level shifters and connecting nets.

3. Select the To file option.

4. (Optional) Specify a file name if you want to save the report in a file.

You can type the file name in the To file box or click the Browse button and select or enter the file name in the Choose Output File dialog box.

5. Click OK or Apply.

The MV Advisor violation browser can report the following violations:

LIBSETUP-001	MV-231	MV-514b
MV-514	MV-044	MV-252
MV-529	MV-076	MV-513
MV-534	MV-078	MV-232c
MV-545	MV-166	MV-237
MV-038	MV-168	MV-514a

The violation browser groups the following messages based on the source domain-sink domain pair in the first level and the driver pin in the next level:

Title	Description
MV-231	Missing level shifting violations
MV-237	Paths with voltage violations
MV-252	Missing level shifting violations with no_shift
MV-513	Redundant isolation
MV-514	Missing isolation violations
MV-514a	Power state violations on literal constant driver pins
MV-514b	Power state violations on tie cell driver pins

Title	Description
MV-545	Missing isolation violations with no_isolation

The violation browser groups the following messages based on the power domains in which the cells or nets are located:

Title	Description
MV-044	Isolation cells being used as core cells
MV-076	Always-on nets being driven by a normal cell
MV-078	Always-on cells driving a normal net
MV-529	Unused power management cells
MV-166	Retention cells without a strategy
MV-168	Isolation cells without a strategy
LIBSETUP-001 Cells with operating condition mismatches	

In addition, the violation browser groups

- MV-038 messages under one title and without multiple levels of groups.
- MV-534 messages based on the driver pin.
- MV-232c messages based on the power domains in the first level and the power supplies in the next level.
- MV-516 messages under one title and without multiple levels of groups.
- UPF-103 messages based on the ignored strategy.

To view a violation report in your Web browser, open the XML file, `report_file`, in a Web browser window.

The XSLT file, `report_file.xslt`, must be present in the same directory.

The Web browser report groups the violations in the same way that the MV Advisor violation browser groups them. The Web browser displays only the violation list (the information in the violation category tree in the violation browser). It does not display the detailed report information about each violation that the violation browser displays.

## Printing the UPF Diagram View

You can print the UPF diagram view that you use to examine the IEEE 1801 power implementation in your design. IEEE 1801 is also known as Unified Power Format (UPF). You can send the diagram to a printer or save an image of the diagram in a PDF or PostScript file for printing later from a UNIX or Linux shell.

To print or save an image of the UPF diagram view,

1. Click the view you want to print to make it the active view.

2. Click the  button on the File toolbar, or choose File > Print.

The Print dialog box appears.

3. Select a print destination.

You can print the diagram or save it in a file.

- To print the diagram, select a printer name in the Name list.

The name of your default printer appears in the Name list by default.

- To save a PDF version of the diagram in a file that you can view or print later In Adobe Acrobat, select Print to File (PDF) in the Name list, and then enter a file name in the Output file box.

Alternatively, you can specify the file name by clicking the browse button and selecting or entering the file name in the Print To File dialog box that appears.

- To save a PostScript version of the diagram in a file you can print later, select Print to File (Postscript) in the Name list, and then enter a file name in the Output file text box.

Alternatively, you can specify the file name by clicking the browse button and selecting or entering the file name in the Print To File dialog box that appears.

4. (Optional) Click the Properties button and set printer properties as needed in the printer properties dialog box that appears.

You can set the paper size, page orientation, and page margins.

5. (Optional) Click the Options button, and set options as needed.

- To set a page range and the number of copies, click the Copies tab.

By default, these options are set to print all pages and a single copy For multiple copies, you can also set options to collate the pages and reverse the page order.

- To set duplex printing and color mode options, click the Options tab.

By default, duplex printing is disabled and the color mode is set for color.

6. Click Print.

You can also print the UPF diagram in the Visual UPF dialog box. For more information, see [Using the Visual UPF Dialog Box](#).

**See Also**

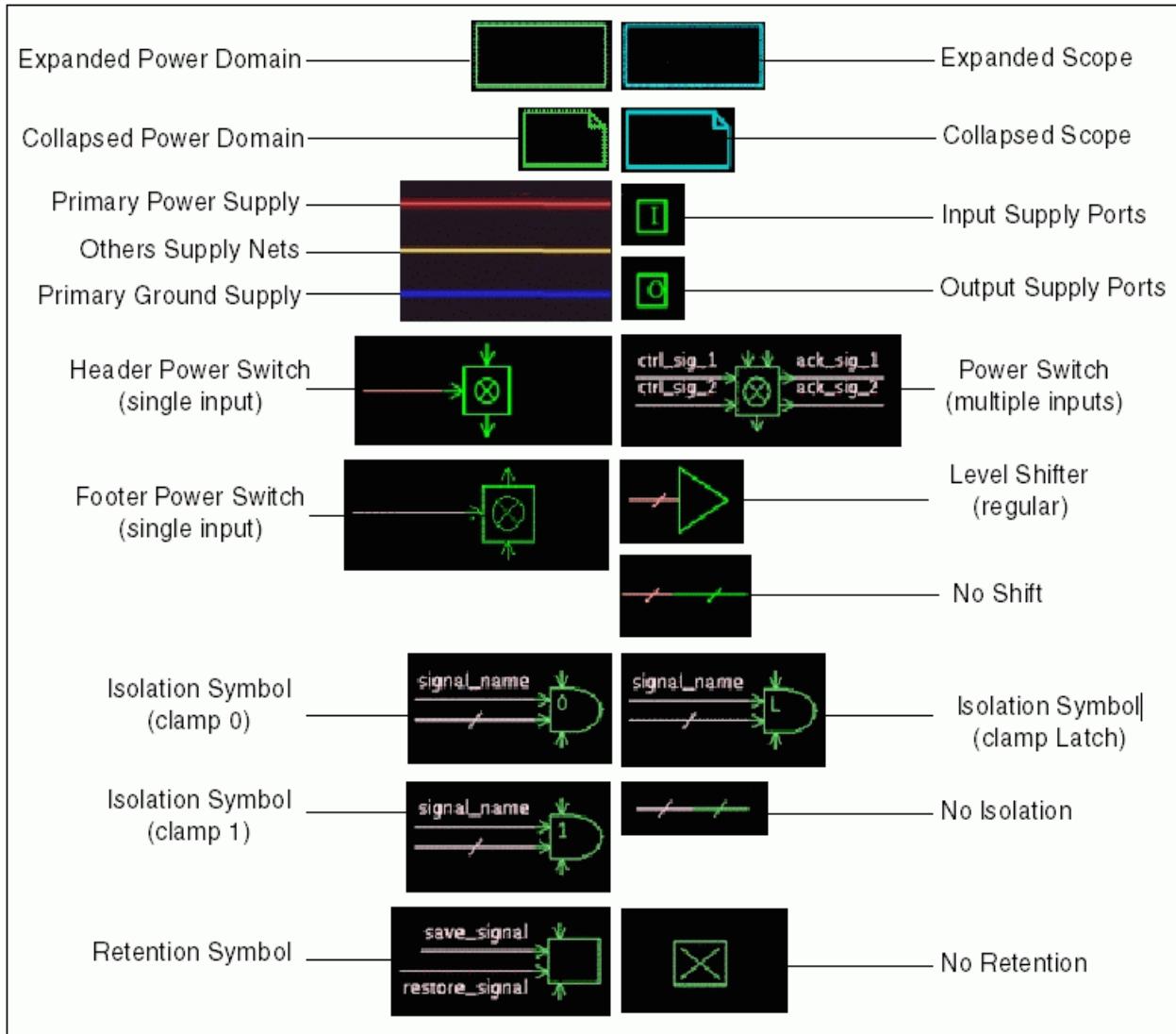
- [Saving an Image of a Window or View](#)

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## UPF Diagram Symbols and Standards

The UPF diagram visually conveys the IEEE 1801 low-power design intent as it is currently defined in the design database or the Visual UPF dialog box. IEEE 1801 is also known as Unified Power Format (UPF). By viewing the diagram, you can verify that the UPF power domains and supply network objects match your intent for the power architecture in your design.

The following legend identifies the symbols that can appear in a UPF diagram:



For explanations of these symbols, see the following sections:

- [Power Domains and Scopes](#)
- [Supply Nets](#)
- [Supply Ports](#)
- [Power Switches](#)
- [Level-Shifter Strategies](#)

- [Isolation Strategies](#)
- [UPF Diagram Symbols and Standards](#)

**Note:**

The symbols are shown here in their default colors. Use the View Settings panel to customize the appearance of the UPF diagram. For more information, see [Changing UPF Diagram Display Properties](#).

A power domain consists of a group of elements in the design that share a common set of power supply needs. By default, all logic elements in a power domain use the same primary supply and ground nets, although other power supplies might also be defined.

Each power domain has a scope and an extent:

- The scope is the logic hierarchy level that you designate as the root of the power domain. Each scope in the design has supply nets and supply ports at the defined hierarchical level of the scope.
- The extent is the set of logic elements that both belong to the power domain and share the same power supply needs.

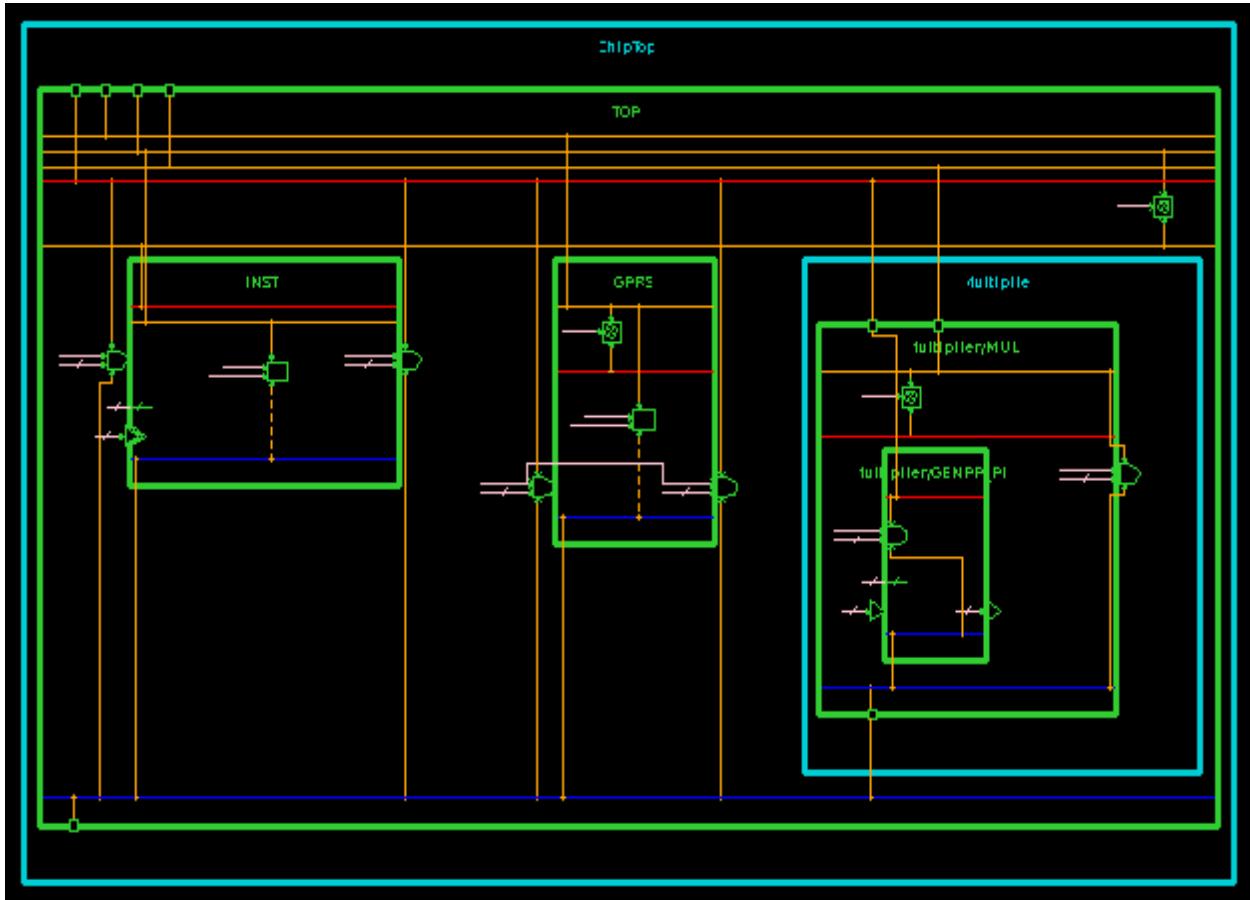
The UPF diagram shows all power domains and scopes that you have defined in the current design and its subdesigns. Power domains (green boxes) and scopes (blue boxes) are organized hierarchically with each child domain located inside its parent power domain.

Supply nets appear as net segments. Each power domain contains a primary supply segment, which is red, and a primary ground segment, which is blue. Other supply nets are yellow. Power supplies extend down from the top of a power domain and ground supplies extend up from the bottom of the power domain. Supply ports connected to power appear at the top of a power domain boundary and supply ports connected to ground appear at the bottom of the boundary.

The symbols for level-shifter and isolation strategies appear at positions relative to their parent power domains based on whether they apply to inputs or outputs and their intended locations in the power domain hierarchy. Retention strategy symbols appear at the center of their parent power domains.

The following example shows many of the UPF diagram symbols. The chip is designed to operate with four power supplies at different voltage levels, and it contains two retention cells.

- The top-level chip, ChipTop, occupies the top-level power domain named TOP. TOP is defined with four supply ports for power, near the top-left corner of the domain boundary, and one supply port for ground, near the bottom-left corner of the boundary.
- The multiplier block, Multiplier, occupies the power domain Multiplier/MUL, which has two supply ports for power and one supply port for ground.



**Note:**

Text does not appear in a UPF diagram when it is below a certain size in pixels.  
Use the zoom tools and zoom commands to magnify the view if necessary to see the text in a diagram.

You can view the UPF diagram in a UPF diagram view or in the Visual UPF dialog box.

- The diagram in a UPF diagram view is synchronized with the Power Compiler database.

When you change the database, for example, by entering a UPF command, the tool immediately updates the diagram. For information about the UPF diagram view, see [Viewing the UPF Power Design](#).

- The diagram in the Visual UPF dialog box is synchronized with the UPF script in the dialog box.

When you make changes to the script, for example, by adding a property to a power domain, the tool immediately updates the diagram. For information about the Visual UPF dialog box, see [Using the Visual UPF Dialog Box](#).

## Power Domains and Scopes

The power domain hierarchy is based on the power domain elements. For example, domain A is the parent of domain B if it has an element that is a hierarchical parent to all the domain B elements.

The diagram displays all power domains that are defined in the current design and its subdesigns. The power domains are organized hierarchically with each power domain located inside its parent power domain.

A power domain appears as a rectangular bounding box. The default color is green.



- The size of the power domain symbol varies according to the number and sizes of objects that reside within the domain. The symbol is big enough to contain all the objects that are contained in it.
- The locations and placement of the power domains are based on the power domain hierarchy. Each power domain is located within its parent power domain.
- The power domain hierarchy is determined by the power domain elements. For example, domain A is the parent of domain B if it has an element that is a hierarchical parent to all the domain B elements.
- An (E) appended to the name of a power domain indicates that extra supplies have been defined for the domain.

If you hold the pointer over the domain name, an InfoTip appears showing the names of the first few extra supplies or the phrase, Not allowed (no elements).

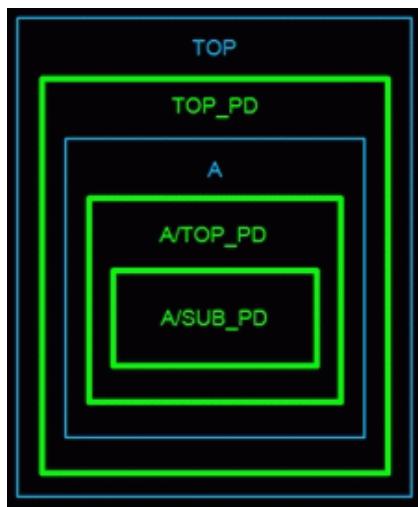
- An (X) appended to the name of a power domain indicates that the implicit supply sets for the domain have been disabled.

A scope appears as a rectangular bounding box. The default color is blue.



When a scope appears in the diagram, it appears within the hierarchy of power domains. A scope appears as a box around the top-most child domain in the scope.

The following figure shows an example of how power domains and scopes appear within the diagram:



The phrase (Black Box) indicates that the scope is on a non-hierarchical instance.

**Note:**

UPF objects that reference cells or nets inside a black box do not appear in the UPF diagram.

You can collapse or expand individual power domains or scopes. Initially, when you open the diagram, all the power domains and scopes are expanded. When you collapse a power domain or scope, its contents are hidden and only the name appears inside the bounding box, as shown in the following examples:



## Supply Nets

A supply net is a conductor that carries a supply voltage or ground throughout a given power domain. A supply net that spans more than one power domain is said to be **reused**.

in multiple domains. The diagram displays all the supply nets in the current design and its subdesigns, identifies the primary power and ground nets in each power domain, and displays the supply net connectivity.

Supply nets appear as net segments. The following figure uses color to indicate the primary power and primary ground supply net segments in a power domain:

- The primary power segment is red.



- The primary ground segment is blue.

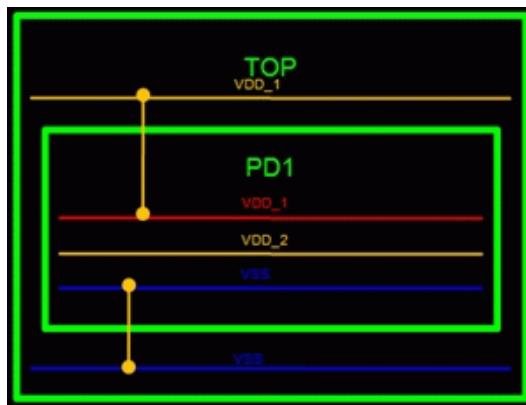


- All other segments, including all connectivity segments, are yellow.



The locations and placement of supply nets are based on the power domains they belong to and whether they are power or ground nets. Each power domain that a supply net belongs to contains a segment indicating that supply net.

- Horizontal segments represent supply nets inside a domain. Power supplies extend down from the top of the domain and ground nets extend up from the bottom of the domain.
- Vertical segments represent supply nets that are reused in multiple domains or supply nets that are connected to another object, such as a supply port or power switch.



**Note:**

When you select a supply net in the diagram, all of its segments appear in the selection color, which is white by default.

An asterisk (\*) next to a supply net name indicates that the supply net has an association or update. You can hold the pointer over the supply net or supply set name to view the original supply net name.

**Note:**

The diagram might show both names for an electrically connected net to indicate the connections between the different names for the same net.

The diagram distinguishes between four types of supply nets: the primary power supply net, other power supply nets, the primary ground supply net, and other ground supply nets. Any net that is not a primary power supply, primary ground supply, or other ground supply is assumed to be a power supply.

UPF does not contain an explicit definition of a ground supply net except for the primary ground. However, in some cases you might have more than one ground net in a domain. The tool determines whether a net is a ground net from its use. For example, a supply net that is specified as a ground net for an isolation or retention strategy is considered to be a ground supply net.

Although the supply nets of a supply set appear in the diagram, it does not explicitly indicate the supply set. Supply-set supply nets and domain-independent supply nets are implicitly available anywhere from their scope downward in the design. They do not appear separately in any power domain except when a supply net segment is used explicitly within a power domain. Explicit usage includes

- The primary supply set or the primary power or ground net for a domain
  - In this case, the segments appear red for primary power or blue for primary ground.
- The default isolation or default retention for a power domain
- The power or ground nets or supply set option for a strategy
- The input or output supply for a power switch
- Supply nets connected to a port inside a power domain

An implicit connection between a strategy and a supply net appears as a dashed line. Implicit connections are connections that you do not explicitly define but is inferred by the tool.

- When an isolation or retention strategy is explicitly connected only to a power or ground net, and the power domain has a supply set defined as the primary power, the tool infers an implicit power or ground connection.

This implicit connection appears in the diagram as a connection between the strategy and the supply-implied power or ground supply net of the supply set.

- When default isolation or default retention supply sets are defined for a power domain, they appear by default as implicit connections in the diagram.

A supply net that appears as a solid line indicates a connection that you have explicitly defined.

You can use the `create_supply_set` command to update the implicit supply net with an explicit supply net. For example, to define the supply set TSet with a supply net VDD, enter

```
prompt> create_supply_set TSet
prompt> create_supply_net VDD
```

The tool displays the following diagram:



To update TSet with the explicit supply net VDD, enter

```
prompt> create_supply_set TSet -function {power VDD} -update
```

The tool updates the following diagram:

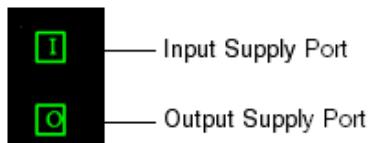


## Supply Ports

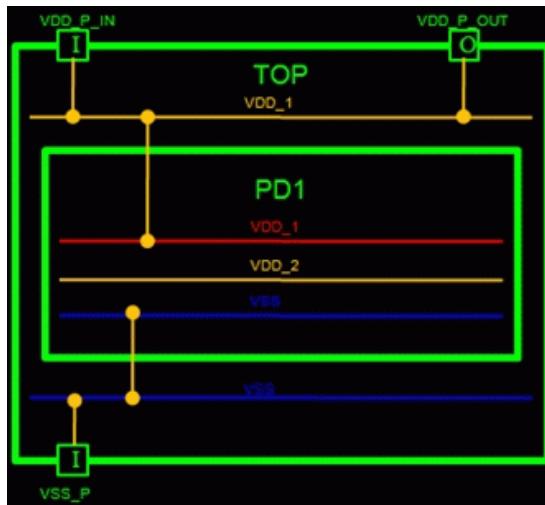
A supply port is a power supply connection point between two adjacent levels of the design hierarchy. A supply net that crosses from one level of the design hierarchy to the next passes through a supply port.

The diagram shows all supply ports in the current design and its subdesigns. It also shows how supply ports are connected to supply nets and in which power domains the supply ports reside.

A supply port appears as a small green bounding box. A letter inside the box indicates whether the port direction is input or output.



A supply port is located on the border of the power domain to which it belongs, on either the top or bottom boundary depending on the supply net to which it is connected. In addition, input supply ports are located on the left side, and output ports are located on the right side.



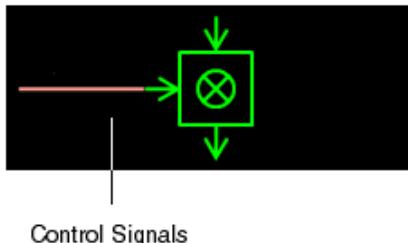
## Power Switches

Power switches turn on and turn off power for supply nets. A power switch has an input supply net, an output supply net that can be switched on or off, and at least one input signal that controls switching. A power switch can have multiple input control signals and one or more output acknowledge signals.

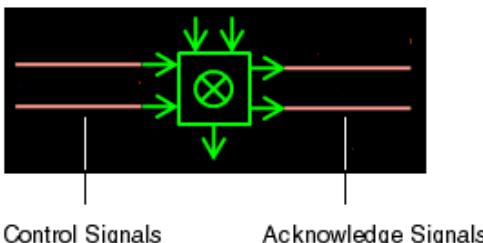
The diagram shows all power switches in the current design and its subdesigns. It also shows how supply nets are connected to the power switches, what domains they belong to, and the control signal of the switch.

Power switches appear as a circle with an **X** inside. The symbol indicates the input and output supply ports with arrows. It includes segments for the control ports and control signals and for any acknowledge ports and acknowledge signals. The direction of the arrows at the top and bottom indicate whether the power switch is a header (down) or footer (up) power switch. The symbol is colored green by default.

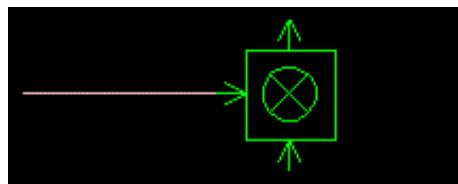
The following figure shows a header power switch with a single control port:



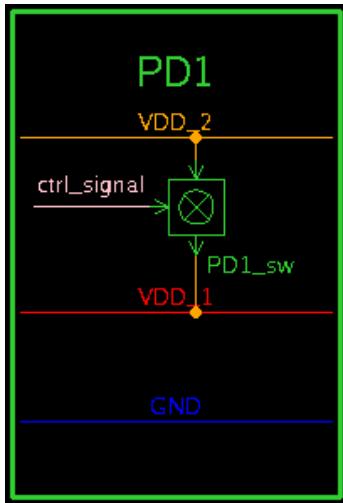
The following figure shows a header power switch with multiple inputs, multiple control ports, and multiple acknowledge ports:



The following figure shows a footer power switch with a single control port. A footer power switch has only ground supplies for input and output. Like header power switches, footer power switches appear between the supply nets, but in this case on the bottom between the ground supplies.



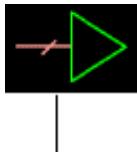
Power switches are located within the boundaries of their parent power domain. Because power switches have supply nets as input and output, they are located between the power supply nets.



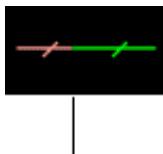
## Level-Shifter Strategies

A level-shifter strategy must be present where a logic signal leaves one power domain and enters another domain at a substantially different supply voltage. The level shifter converts a signal from the voltage swing of the first domain to that of the second domain.

The level-shifter symbol looks like a buffer and includes a segment representing the inputs that are shifted. The no-shift symbol is a line that shows a direct connection without level shifting.



Regular

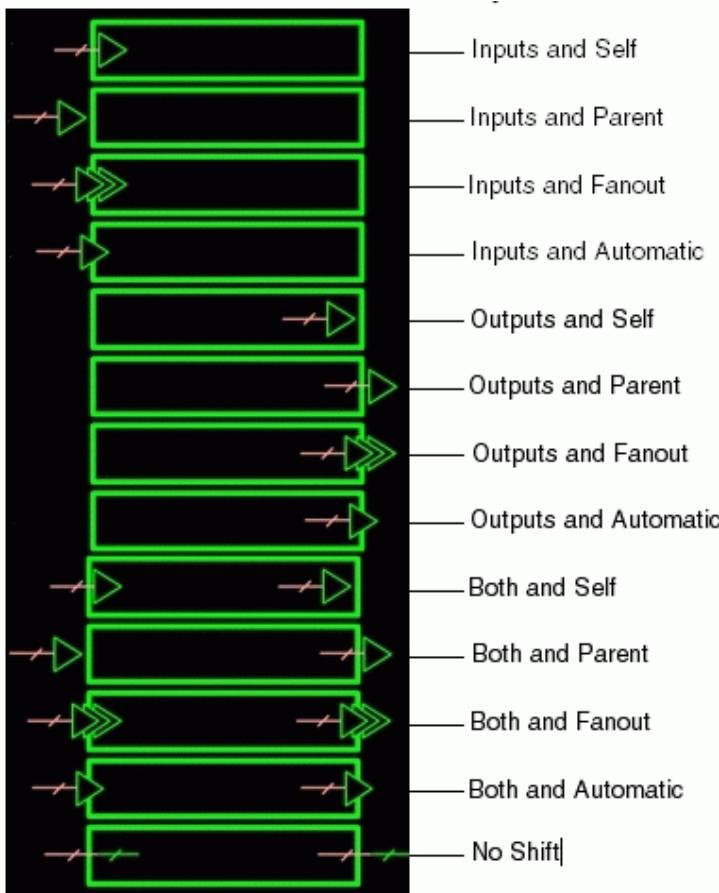


No Shift

The symbol for each level shifter is located adjacent to the boundary of its parent power domain. The location depends on whether it shifts inputs or outputs and the location of the level shifter cells in the logic hierarchy.

- The symbol appears at the left edge of the boundary if the strategy applies to input ports or elements, or it appears at right edge of the boundary if the strategy applies to output ports or elements.  
If the strategy applies to both inputs and outputs, symbols appear at both the left and right edges of the boundary.
- The symbol appears inside the domain boundary if the level-shifter cell is located inside the hierarchy level of the port that it shifts (self) or outside the domain boundary if the cell is located in the parent hierarchy of the port (parent).

The following figure shows all the possible combinations of level-shifter symbols and locations, which are based on the values of the `-applies_to` and `-location` options in the `set_level_shifter` command used to define the level shifters. For information about these options, see the man page.



**Note:**

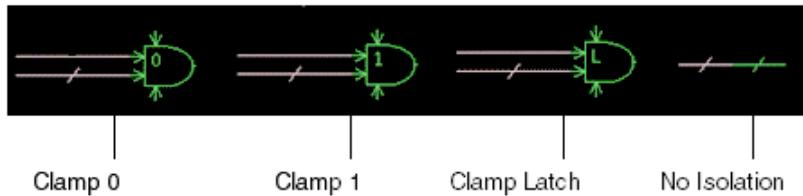
If you specify a list of elements for a level-shifter strategy, by using the `set_level_shifter` command with the `-elements` option, the tool ignores the

`-applies_to` option and determines the symbol position relative to the left or right edge of the boundary based on whether the list contains input elements, output elements, or both types of elements.

## Isolation Strategies

An isolation cell must be present where a logic signal leaves a switchable power domain and enters a different power domain.

The isolation strategy symbol indicates the clamp value (0, 1, or latch) and includes pins for power and ground, a segment representing the isolation control signal, and a segment representing the inputs or outputs that the strategy isolates. The no-isolation symbol is a line that shows a direct connection.



Each isolation symbol is located adjacent to the boundary of its parent power domain. The location of the symbol depends on whether the strategy isolates inputs or outputs and the location of the isolation cell in the logic hierarchy.

- The symbol appears at the left edge of the boundary if the strategy applies to input ports or elements or at right edge of the boundary if the strategy applies to output ports or elements.
- If the strategy applies to both input and output ports or elements, symbols appear at both the left and right edges of the boundary.
- The symbol appears inside the domain boundary if the isolation cell is located inside the hierarchy level of the port that it isolates (self) or outside the domain boundary if the isolation cell is located in the parent hierarchy of the port (parent).

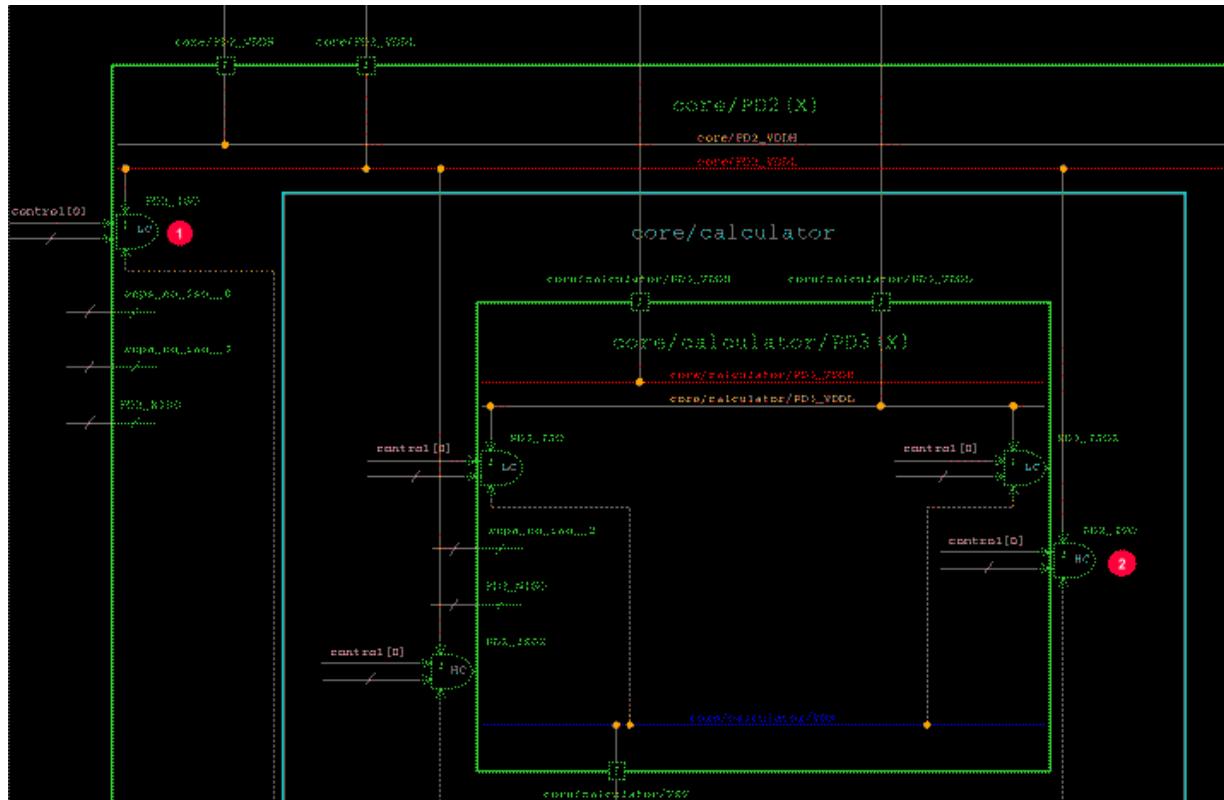
If you set the `lower_domain_boundary` design attribute to `true`, related pairs of isolation strategy symbols appear in the diagram. The symbol representing the cell that isolates the lower-level connection contains the letters LC. The symbol representing the cell that isolates the higher-level connection contains the letters HC and appears adjacent to the lower domain boundary.



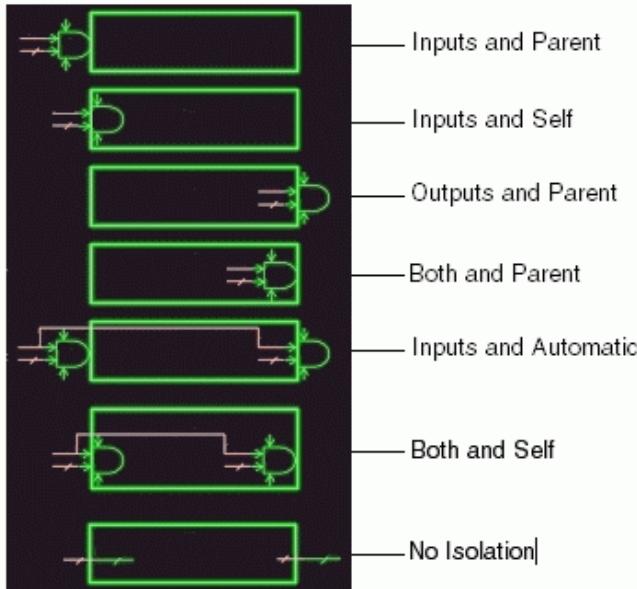


If you select either symbol in a UPF diagram, the related symbol is selected automatically.

The following example shows the placement of these isolation symbols on the power domain boundaries:



The following figure shows all the possible combinations of isolation strategy symbols and locations, which are based on the value of the `-applies_to` option or the `-elements` option in the `set_isolation` command and the value of the `-location` option in the `set_isolation_control` command used to define the isolation strategies. For information about these options, see the man page.



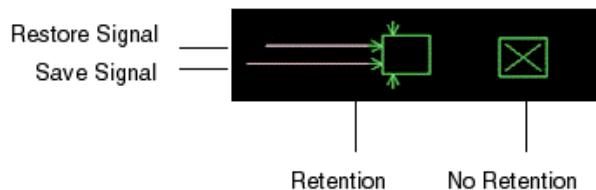
**Note:**

If you specify a list of elements for an isolation strategy, by using the `set_isolation` command with the `-elements` option, the tool ignores the `-applies_to` option and determines the symbol position relative to the left or right edge of the boundary based on whether the list contains input elements, output elements, or both types of elements.

## Retention Strategies

In a power domain that has power switching, any registers that must retain data during shutdown must be implemented as retention registers. A retention register has a separate, always-on supply net, sometimes called the backup supply, that keeps the data stable in the retention register while the primary supply of the domain is shut down.

The retention symbol is a green bounding box. The symbol includes pins for power and ground, and segments for the save and restore signals. The no-retention symbol contains the X in the bounding box.



All retention symbols are located at the center of their parent power domains. The diagram shows how supply nets connect to a retention strategy, what domains the strategy belong to, and their save and restore signals.

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## Changing UPF Diagram Display Properties

The UPF diagram visually conveys the IEEE 1801 low-power design intent as it is currently defined in the design database or the Visual UPF dialog box. IEEE 1801 is also known as Unified Power Format (UPF).

You can change display properties for the active UPF diagram view or the UPF diagram in the Visual UPF dialog box by setting options on the View Settings panel.

You can set options to

- Change the brightness level for colors in the diagram
- Apply a predefined or custom color theme to the entire diagram
- Change the background color in the diagram
- Change the colors of individual object types

To set display properties in the UPF diagram view,

1. Open the View Settings panel if it is not already open.

- For the UPF diagram view, choose View > Toolbars > View Settings.
- For the diagram view in the Visual UPF dialog box, click the  button on the toolbar in the diagram view.

Alternatively, you can drag the vertical split bar between the panel and the diagram. When the panel is hidden, the split bar appears as a blue line at the left side of the view.

The View Settings panel appears. You can attach it to the left or right edge of the Design Vision window or move it to a different location inside or outside the window.

2. Set options as needed.

- To change the color brightness, select an option in the Brightness list.
- To apply a color theme, choose Themes > Set From Theme, select a predefined or custom them in the Set From Theme dialog box, and click OK.

- To change the background color, click the Background button, select a standard custom color in the Select Style dialog box, and click OK.
  - To change an object type color, click the Clr button against the object type name, select a standard color or define a custom color in the Select Style dialog box, and click OK.
3. Click Apply.

By default you must click Apply on the View Settings panel to apply your changes to the active layout view. However, you can enable a mechanism that automatically applies changes when you make them, instead of only when you click Apply.

To enable or disable the automatic apply mechanism,

- Choose Options > Auto Apply.

To reset options to their state the last time you clicked Apply,

- Choose Options > Cancel changes.

This command is available only when the automatic apply mechanism is disabled.

If you change display properties in the active UPF diagram view and want to use the same settings in another view or during a future session, you can save them in your preferences file. You can also restore previously saved view settings by loading them from your preferences file. For details, see [Saving and Restoring View Settings](#).

**Note:**

Design Vision tool does not automatically save display properties when you close the GUI or exit the session.

## Applying a Color Theme

The UPF diagram visually conveys the IEEE 1801 low-power design intent as it is currently defined in the design database or the Visual UPF dialog box. IEEE 1801 is also known as Unified Power Format (UPF).

You can customize the visual display by applying a color theme to the diagram. You can apply a predefined theme or a user-defined theme. Design Vision tool provides several predefined themes, including themes that are configured for presentations or printing and themes that highlight certain aspects of the diagram.

To apply a theme to the UPF diagram view,

1. Display the View Settings panel if it is hidden.
2. Choose Themes > Set From Theme.

The Set From Theme dialog box appears.

3. Select a theme in the Select Theme category tree.

The Preview box displays the theme. Repeat this step as needed until you find the theme you want to apply.

4. Click OK in the Set From Theme dialog box.

5. Click Apply on the View Settings panel.

In addition to the predefined themes, you can create your own themes. You can also modify or remove a theme that you created.

To create or modify a user-defined theme from the current color settings,

1. Display the View Settings panel if it is hidden.
2. Choose Themes > Save To Custom Theme.

The Save To Custom Theme dialog box appears.

3. Enter a name for the theme in the Theme name box .

For a new theme, enter a unique name. For an existing theme, enter the name of the theme you are modifying.

4. Click OK.

The next time you open the Select From Theme dialog box, the name of your new theme appears in the custom category in the Select Theme category tree.

Design Vision tool saves custom themes in your preferences file automatically and retains them for future sessions until you remove them. You can remove custom themes but you cannot remove predefined themes.

To remove a custom theme from your preferences file,

1. Display the View Settings panel if it is hidden.
2. Choose Themes > Remove Custom Theme.

The Remove Custom Theme dialog box appears.

3. Select the name of the theme you want to remove.
4. Click OK.

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## Changing the Background Color

The UPF diagram visually conveys the IEEE 1801 low-power design intent as it is currently defined in the design database or the Visual UPF dialog box. IEEE 1801 is also known as Unified Power Format (UPF).

To change the background color in the UPF diagram,

1. Display the View Settings panel if it is hidden.
2. Click the Background button.

The Select Styles dialog box appears.

3. Select a standard color in the color palette, or click the Custom tab and create a custom color.

The preview box (New) displays the color. Repeat this step as needed until you are satisfied with the appearance of the preview box.

For details about using custom colors, see [Creating a Custom Color](#).

4. Click OK to close the Select Styles dialog box.

The Background button on the View Settings panel changes to show the new color.

5. Click Apply on the View Settings panel.

You can save the current color settings in your preferences file, and you can load color settings from the preferences file. For details, see [Saving and Restoring View Settings](#).

# 4

## Performing Basic Tasks

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The Design Vision GUI is a menu-driven interface. If you have experience using the Synopsys synthesis tools, you can accomplish familiar pre-synthesis and synthesis tasks by using Design Vision windows and menus. If you are new to the Synopsys synthesis tools, see the *Design Compiler User Guide* or the *DC Explorer User Guide* to learn the standard tasks for working in the synthesis environment and running a synthesis flow.

For information about performing these tasks, see the following sections:

- [Specifying Logic Libraries](#)
  - [Viewing a Design Interactively](#)
  - [Viewing Schematics](#)
  - [Using User Tables](#)
  - [Using a Milkyway Database](#)
  - [Working With Designs in Memory](#)
  - [Defining the Design Environment](#)
  - [Setting Constraints](#)
  - [Compiling the Design](#)
  - [Using Logic Synthesis Tools](#)
  - [Working With Reports](#)
- 

### Specifying Logic Libraries

Before you start work on a design, specify the location of your libraries. You can define your library locations directly in the .synopsys\_dc.setup file or indirectly by entering the locations in the Application Variables dialog box. You can also specify library locations by running a script when you start the tool or by using the Execute Script dialog box. For details, see [Starting the Tool on page 32](#) and [Using Script Files on page 38](#).

The link and target libraries are logic libraries that define the semiconductor vendor's set of cells and related information, such as cell names, cell pin names, delay arcs, pin

loading, design rules, and operating conditions. The symbol library defines the symbols for schematic viewing of the design.

Symbol libraries contain definitions of the graphic symbols that represent library cells in schematic views. Semiconductor vendors maintain and distribute the symbol libraries. When you generate a schematic in Design Vision tool, the compiler performs a one-to-one mapping of cells in the netlist to cells in the symbol library.

DesignWare libraries are collections of reusable circuit-design building blocks (components) that are tightly integrated into the Synopsys synthesis environment.

- Synopsys provides a standard DesignWare library with components that implement many of the built-in HDL operators. You do not need to specify the standard DesignWare library. However, you must specify any additional, specially licensed, DesignWare libraries with the `synthetic_library` variable (you do not need to specify the standard DesignWare library).
- You can develop additional DesignWare libraries at your site, or you can license DesignWare libraries from Synopsys or from third parties. You must specify any additional, specially licensed DesignWare libraries that you want to use.

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## Searching for Application Variables

Choose File > Setup to open the Application Variables dialog box. Perform the following options to search for the application variables.

1. To filter the list of application variables, enter a search term in the filter text box. As you enter, the tool filters the application variables and displays only the variable names that contain the search term.
  - To search for library search path, enter `search_path` in the filter text box.
  - To search for link libraries, enter `link_path` in the filter text box.
  - To search for target libraries, enter `target_library` in the filter text box.
  - To search for symbol libraries, enter `symbol_library` in the filter text box.
  - To search for DesignWare libraries, enter `synthetic_library` in the filter text box.
2. To filter by the Value column, enter Value followed by the search term. For example, enter `Value:true` to display only application options with a setting of true in the Value column.

To further limit the application options displayed in the list, click the filter button to the right of the filter text box. Deselect the Show if value is default option to hide all default application option settings. Deselect the Show read-only option to hide all read-only application options.

Application variables which have a nondefault setting are displayed in bold font. Move the pointer over the text to display an infotip. The infotip shows the option name, option type, current setting, user default setting, system default setting, scope, and a brief description.

3. To display the man page for an application variable, click the  button to select it, then click near the top right of the dialog box. The tool opens the man page for the selected application variable.
4. To set the application variable to its default, click the  button.

For more information about the function of link libraries, target libraries, symbol libraries, and DesignWare libraries, see the *Design Compiler User Guide*.

## Viewing a Design Interactively

The Design Vision GUI displays graphic representations of design data in several types of views. You can view graphic representations of your design in schematic and layout views, perform high-level timing analysis with histogram views, and view the UPF multivoltage power implementation in a UPF diagram view.

- Schematic views display schematic representations of specific types of design data.  
You can examine logic designs (hierarchical cells), selected timing paths (including fanin and fanout logic), or selected design objects.
- The layout view is the focal point for floorplan analysis in Design Vision tool.  
It displays graphic representations of design objects in a single, flat view of the physical design. You can open multiple layout views to simultaneously work with different areas of the design.

To help visualize your design data, the GUI provides tools and commands to examine the design data and to select or highlight objects of interest in the active view. In the active view, do the following:

- Select or deselect individual objects or timing paths or objects in a rectangular area.  
Selection is global in Design Vision tool. Any objects or timing paths that you select appear selected in all open views.
- Use color to highlight individual objects or timing paths or objects in an area of the design.

Highlighting is global in graphic views. When you highlight objects or timing paths in a view, the GUI highlights them with the same color in every view where they appear.

- Display (query) object properties for individual objects (such as design and timing attribute values).
- Traverse (pan) the design and magnify or shrink (zoom in) areas of interest.

In layout views, you can also measure distances by drawing rulers.

To learn more about viewing the design interactively, see the following topics:

- [Selecting a Mouse Tool](#)
- [Previewing Objects in Graphic Views](#)
- [Selecting Objects in Graphic Views](#)
- [Highlighting Objects or Timing Paths](#)
- [Querying Objects in Graphic Views](#)
- [Configuring the Query Panel](#)
- [Magnifying or Shrinking a View](#)
- [Traversing a View](#)
- [Following Selected Objects](#)
- [Selecting Objects by Name](#)
- [Reusing Zoom and Pan Settings](#)
- [Redrawing the Active View](#)
- [Saving an Image of a Window or View](#)

### See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Schematic Views](#)

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## Selecting a Mouse Tool

When you click or drag the pointer in a graphic view such as a schematic or layout view, the interactive left button mouse tools control the actions performed by the GUI. You can enable a mouse tool by clicking a button on the Mouse Tools toolbar or by choosing the corresponding View menu commands. When you change the mouse tool, you change it only in the active view.

You can set the mouse tool options to one of the following:

- Selection tool
- Highlight tool
- Query tool
- Zoom In tool
- Zoom Out tool
- Pan tool
- Ruler tool (available only in the layout window)

When you enable a mouse tool, the left mouse button remains in that tool until you enable a different mouse tool. The default mouse tool is the Selection tool, which allows you to select objects in a schematic or layout view by clicking them or by dragging the pointer diagonally to define a rectangular box around them.

as described in the following table:

Mouse Tool	Description	How to Set
Selection Tool	To set the left mouse button to select objects in the active schematic or layout view, click or drag the Selection tool. This is the default mouse tool.	Click the Selection Tool  button, or choose View > Mouse Tools > Selection Tool
Highlight Tool	To set the left mouse button to highlight objects in the active schematic view, click or drag with the Highlight tool .	Click the Highlight Tool  button, or choose View > Mouse Tools > Highlight Tool
Query Tool	To display object information on the Query panel, click an object with the Query tool in the active schematic or layout view to set the left mouse button.	Click the Query Tool  button, or choose View > Mouse Tools > Query Tool.
Zoom In Tool	To set the left mouse button to magnify the design in the active schematic or layout view	Click the Zoom In Tool  button, or choose View > Mouse Tools > Zoom In Tool. Alternatively, you can right-click and choose Zoom In Tool.

Mouse Tool	Description	How to Set
Zoom Out Tool	To set the left mouse button to shrink the design in the active schematic or layout view	Click the Zoom Out Tool  button, or choose View > Mouse Tools > Zoom Out Tool. Alternatively, you can right-click and choose Zoom Out Tool.
Pan Tool	To set the left mouse button to traverse the design in the active schematic or layout view	Click the Pan Tool  button, or choose View > Mouse Tools > Pan Tool. Alternatively, you can right-click and choose Pan Tool.
Ruler Tool	To set the left mouse button to draw rulers in the active layout view by clicking with the Ruler tool	Click the Ruler Tool  button, or choose View > Mouse Tools > Rule Tool.

## See Also

- [Mouse Tools Toolbar](#)

## Previewing Objects in Graphic Views

You can preview information about an object before you interact with the object by using a mouse tool. This preview mechanism is available for the Selection tool, the Highlight tool, and the Query tool. You can preview objects in a schematic, layout, or UPF diagram view. For example, if you need to interact with an object in an area of the design where objects are densely packed or overlapped, you can preview information about the objects at the location before clicking the object to interact with.

When you move the pointer over an object, the tool displays the object in the preview color. The preview color is white by default and has a thinner line width than the selection coloring. If InfoTips are enabled, the tool displays the object information in an InfoTip. This information can include the object name, the object type, and the attribute values. In a schematic view, layout view, or UPF diagram view, the InfoTip displays the object name and object information such as attribute values. The information varies depending on the type of object and the type of view in which you are previewing it.

InfoTips are enabled by default in the layout views and disabled by default in schematic views.

To enable or disable InfoTips globally in the active view, choose View > InfoTip.

A check mark against the command on the View menu indicates that InfoTips are enabled.

In a layout view, if more than one object occupies the same location, you can display information sequentially for each object.

- To display the information for the next object in the sequence, press F1.
- To display the information for the previous object in the sequence, press Shift+F1.

For tools that operate on selected objects in the layout view, you can preview any selectable object that is enabled for selection on the View Settings panel. For other tools, such as the Query tool, you can preview any object that the tool can operate on, regardless of whether the object can be selected.

**Note:**

If you have trouble previewing small objects, try magnifying the view. In a large design, some objects or object outlines are too small to preview at low magnification. For details, see [Magnifying and Traversing the Design](#).

The information that InfoTip displays varies depending on the type of object. You can add or remove attributes in InfoTip for an object type by modifying the `LayoutInfoTipText` attribute group in the Attribute Group Manager dialog box. To open this dialog box, click

the  button in the Properties dialog box or the Selection List dialog box. For more details, see [Creating and Editing Attribute Groups](#).

**See Also**

- [Selecting Objects in Graphic Views](#)
- [Highlighting Objects or Timing Paths](#)
- [Querying Objects in Graphic Views](#)

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## Selecting Objects in Graphic Views

You can select objects interactively in the active schematic, layout, histogram, or UPF diagram view by using the Selection tool. You can select individual objects or objects in a rectangular area. In a layout view, you can also select objects along a straight line. You can replace the current selection, add objects to the current selection, or remove objects from the current selection. The Selection tool is the default mouse tool that is enabled by default when you open a schematic or layout view.

Design Vision tool displays selected objects in the selection color, which is white by default, and displays their names in the selection list. The objects are also cross-selected in all other open views. The status bar displays the object name when a single object is selected or the number of selected objects when multiple objects are selected.

To enable the Selection tool,

- Click the Selection Tool  button on the Mouse Tools toolbar or choose View > Mouse Tools > Selection Tool.

The pointer shape changes to the Selection Tool pointer ().
- When you enable the Selection tool in a layout view, the Selection tool options appear in the Mouse Tool Options toolbar.
- Click the Show Online Help  button on the Mouse Tool Options toolbar, for viewing the online help using the Selection tool in a layout view.

**Note:**

Before you can select objects in a layout view, they must be visible and enabled for selection. Use the View Settings panel to set object or layer visibility and selection options as needed. For details, see [Controlling Object Visibility](#) and [Controlling Object Selection](#).

By default, you can select or deselect objects by clicking or dragging the pointer as follows:

- To select an object and deselect any other selected objects, click the object.
- To select multiple objects at the same time and deselect other selected objects, drag the pointer to draw a rectangular box around the objects that you want to select.
- To add objects to the current selection, press the Control key while you click or drag the pointer.
- To remove an object from the current selection, press the Shift key while you click or drag the pointer.

When you move the Selection tool over an object, the tool shows the object in the preview color, which is white by default but with a thinner line width than the selection coloring. In a schematic or layout view, if InfoTips are enabled, the information about the object appears in an InfoTip. For more details, [Previewing Objects in Graphic Views](#).

In a layout view, you can display information sequentially for overlapping objects by pressing the F1 key. When you move the pointer over the objects, information about the first (uppermost) object appears in the InfoTip. Press F1 to display information about the next object (from top to bottom) or Shift+F1 to display information about the previous object. When the tool displays the name of the object you need to select, click the object.

You can fine-tune the Selection tool in a layout view by setting the options on the Mouse Tool Options toolbar as follows:

- To select or deselect objects in a rectangular area by either dragging the pointer or clicking two diagonally opposite corners of the rectangle, select the Rectangle input mode option.

This allows you to click one corner of the rectangle and then use the nested zoom and pan tools before clicking the other corner.

- To select objects along a straight line by dragging across an edge of each object, select the Line input mode option.
- To select or deselect objects that are partially outside a rectangular area when the Smart or Rectangle input mode option is selected, select the Enable rectangle intersect option.
- To control whether the tool replaces, adds objects to, or removes objects from the current selection, select an option in the Selection list.

The options are Replace, Add, and Remove. The default is Replace.

- To deselect all selected objects, click Clear.

To deselect all selected objects, choose Select > Clear. Alternatively, in a layout view, you can click Clear in the Mouse Tool Options toolbar.

You can view information about selected objects in the Selection List dialog box (choose Select > Selection List), in the Properties dialog box (choose Edit > Properties), or on the Query panel (choose Select > Query Selection).

For information about other options to select objects in the GUI, see

- [Selecting Objects by Name](#)
- [Selecting Highlighted Objects and Paths](#)
- [Selecting Bus Objects](#)
- [Selecting a Collection of Objects](#)
- [Selecting Timing Paths](#)
- [Selecting Fanin or Fanout Logic](#)
- [Searching for Objects by Name or Regular Expression](#)

### See Also

- [Selecting a Mouse Tool](#)
- [Following Selected Objects](#)
- [Deselecting All Selected Objects](#)

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## Highlighting Objects or Timing Paths

You can highlight objects interactively in the active schematic or layout view by using the Highlight tool (). You can also remove the highlighting from highlighted objects. In addition, you can highlight selected objects or timing paths by using commands in the Highlight menu.

When you highlight a timing path, net connections appear in the highlight color to show the connections between the pins or ports on the path.

**Note:**

In a schematic, highlighted timing paths can traverse the design hierarchy. For details about moving up or down the hierarchy in a schematic view, see [Schematic Views](#).

To enable the Highlight tool in the active schematic or layout view,

- Click the  button on the Mouse Tools toolbar, or choose View > Mouse Tools > Highlight Tool.

The pointer becomes the Highlight Tool pointer ().

When you enable the Highlight tool in a layout view, the Highlight tool options appear on the Mouse Tool Options toolbar.

To highlight objects interactively in the active schematic or layout view,

1. (Optional) Select a highlight color.

By default, the tool applies the same color each time you highlight, until you change the color. You can change the highlight color by choosing a color command on the Highlight menu. Alternatively, you can enable an automatic color cycling mechanism. For details, see [Controlling the Highlight Color](#).

2. (Optional) If you want to display object information on the Query panel when you highlight an object in a layout view, select the Query on Highlight option on the Mouse Tool Options toolbar.

For information about the Query panel, see [Querying Objects in Graphic Views](#).

3. Highlight objects or remove highlighting in one of the following methods:
  - To highlight individual objects, click the objects.
  - To highlight objects in a rectangular area, drag the pointer diagonally to draw a box around the area.

The tool highlights objects that are completely inside the box.
  - To remove highlighting from individual objects, press Shift and then click the objects.
  - To remove highlighting from objects in a rectangular area, press the Shift key and drag the pointer diagonally to draw a box around the area.

The tool removes highlighting from objects that are completely inside the box.

When you move the Highlight tool over an object, the tool shows the object in the preview color, which is white by default but with a thinner line width than selection highlighting. If InfoTips are enabled for a schematic or layout view, information about the object appears in an InfoTip.

**Note:**

When you highlight objects or timing paths in the active schematic or layout view, the objects or timing paths are automatically shown in the highlight color in all open schematic and layout views in which they appear.

To highlight selected design objects or timing paths in the active schematic or layout view,

1. Select the objects or paths you want to highlight.

You can select timing paths by clicking the path names in a histogram or the timing analysis driver, or by choosing Select > Paths From/Through/To and setting options in the Select Paths dialog box. For details, see [Selecting Timing Paths](#).

2. Choose Highlight > Selected.

Alternatively, in a layout view, you can click the  button on the Highlight toolbar.

The objects or paths change to the highlight color when the selection color is removed. Click the background to remove the selection color (white) by deselecting the objects or paths.

**See Also**

- [Highlighting Selected Objects or Paths](#)
- [Controlling the Highlight Color](#)
- [Removing Highlighting](#)

- [Selecting a Mouse Tool](#)
- [Highlighting the Critical Path](#)
- [Highlighting Maximum or Minimum Delay Paths](#)

## Highlighting Selected Objects or Paths

You can use highlighting in schematic and layout views to easily identify design objects or timing paths that you have selected. The objects or paths are highlighted only in the active view.

A highlighted object or path has a different color than the not highlighted object. When you highlight a selected path, net connections appear in the highlight color, to show the connections between the pins or ports on the path. By default, Design Vision tool automatically changes to the next color each time you highlight objects or paths. For details, see [Controlling the Highlight Color](#).

**Note:**

In a schematic, highlighted timing paths can traverse the design hierarchy. For details about moving up or down the hierarchy in a schematic view, see [Schematic Views](#).

To highlight selected objects or paths,

1. Select the objects or paths you want to highlight.
2. Click the  button on the Highlight toolbar, or choose [Highlight > Selected](#).

Highlighted objects and paths change to the highlight color when the selection color is removed. Click in the background to remove the selection color (white) by deselecting the objects or paths.

### See Also

- [Highlighting the Critical Path](#)
- [Highlighting Maximum or Minimum Delay Paths](#)
- [Removing Highlighting](#)
- [Controlling the Highlight Color](#)

## Controlling the Highlight Color

By default, Design Vision tool automatically cycles through the highlight colors. Each time you apply highlighting to a timing path or selected objects, Design Vision tool uses the next highlight color in the cycle.

You can use commands in the Highlight menu to reset the color cycle to a certain color. You can also disable the auto-cycling of highlight colors and always use the same color.

To set the automatic color cycle,

1. Choose Highlight > Set Current Color.
2. Choose a color on the Set Current Color menu.

Alternatively, in a layout window, you can choose a color on the  menu on the Highlight toolbar.

To enable autocycling,

- Choose Highlight > Auto Cycle Colors.

A check mark next to the `Auto Cycle Colors` command on the Highlight menu indicates that autocycling is enabled.

## See Also

- [Highlighting the Critical Path](#)
- [Highlighting Maximum or Minimum Delay Paths](#)
- [Highlighting Selected Objects or Paths](#)

## Removing Highlighting

You can remove the highlighting from selected objects or remove the current highlight color or all highlighting from all highlighted objects and paths, in a schematic or layout view. The highlighting is removed only in the active view.

To remove highlighting from selected highlighted objects or timing paths in the active view,

1. Select the objects from which you want to remove the highlight color.

2. Click the  button on the Highlight toolbar, or choose Highlight > Clear Selected.

To remove the current highlight color from objects and paths that are highlighted with that color in the active view,

- Choose Highlight > Clear Current Color.

To remove highlighting from all highlighted objects and paths in the active view,

- Choose Highlight > Clear All.

Alternatively, in a layout window, you can click the  button on the Highlight toolbar.

## See Also

- [Highlighting the Critical Path](#)
- [Highlighting Maximum or Minimum Delay Paths](#)
- [Highlighting Selected Objects or Paths](#)

---

## Querying Objects in Graphic Views

You can display object information interactively in the active schematic, layout, histogram, or UPF diagram view, by using the Query tool. When you click an object in the active view, information about the object, such as the design and timing attributes, appears on the Query panel. You can also set options on the Query panel to automatically or manually copy the information to the session transcript in the console log view.

To enable object queries in the active view, click the  button on the Mouse Tools toolbar, or choose View > Mouse Tools > Query Tool. The pointer becomes the Query Tool pointer () , and by default the Query panel appears.

When you move the Query tool over an object, the tool shows the object in the preview color, which is white by default but with a thinner line width than selection coloring. In a schematic or layout view, if InfoTips are enabled, information about the object appears in an InfoTip. For more details, [Previewing Objects in Graphic Views](#).

In a layout view, you can display information sequentially for overlapping objects by pressing the F1 key. When you move the pointer over the objects, information about the first (uppermost) object appears in the InfoTip. Press F1 to display information about the next object (from top to bottom) or Shift-F1 to display information about the previous object. When the tool displays the name of the object you need to query, click the object.

To display information for an object,

1. Make sure the  button is selected on the Mouse Tools toolbar and then click the object.
2. The object is displayed in the query color (white). The information about the object appears on the Query panel. You can select and copy text on the panel, but you cannot edit it.
3. Click the object to display information for other objects.

Each time you click an object with the Query tool, information about the new object replaces the information about the previous object on the Query panel.

**Note:**

Query coloring has a thinner line width than selection coloring.

You can select and copy text on the Query panel. You can send the query text to the session transcript in the console log view.

To copy text on the Query panel,

1. Select the text to copy.

If you want to copy all the text on the panel, right-click and choose Select All.

2. Right-click and choose Copy.

You can copy text and paste it on the command line by selecting the text and pasting it with the middle mouse button.

To copy the current object information into the session transcript in the console log view,

- Click the  button at the top of the Query panel.

You can set an option to automatically copy the information to the session transcript. You can also set options to wrap long lines of text on the Query panel and to control whether the Query panel opens automatically when you activate the Query tool. In addition you can open the Customize Query Toolbar dialog box to customize the information content of the queries for particular types of objects. For details, see [Configuring the Query Panel](#).

The information that the Query panel displays varies depending on the type of object. You can configure the default query information for a design, cell, port, pin, net, or netlist, by adding or removing attributes in the `QueryText` attribute group. For details, see [Creating and Editing Attribute Groups](#).

**See Also**

- [Selecting a Mouse Tool](#)

---

## Configuring the Query Panel

You can configure the Query panel to open it automatically when you activate the Query tool, wrap long lines of text, or automatically log the query text to the session transcript in the console log view. You can also open the Customize Query Toolbar dialog box to customize the information content of the queries for individual object types.

Following are the options available in the Query tool,

- To control whether the Query panel appears automatically when you activate the Query tool, click  and select or deselect the Auto Show when Query Tool is Chosen option. This option is enabled by default.

**Note:**

If you click an object with the Query tool when the Query panel is hidden, it appears automatically regardless of whether this option is selected.

- To enable text wrapping on the Query panel, click  and select the Wrap Text option. This option is disabled by default.
- To enable the automatic logging mechanism, click  and select the Auto Print Text to Log option. This option is disabled by default.

You can customize the information that appears on the Query panel by controlling which attributes the tool displays for objects and different types of queries (single-object query or multiple-object query).

The default attribute groups for a design, cell, net, port, pin, or netlist are `QueryText` for single-object queries and `Basic` for multiple-object queries. For object types that do not have `QueryText` or `Basic` attribute groups, the default attribute group is `All`.

The All attribute group is available for every object and query type. The availability of other groups varies depending on the object and query type. You can select any attribute group that appears in the list for a particular object and query type.

To configure the query content for one or more object queries,

- Click  and choose Customize Text.

The Customize Query Toolbar dialog box appears.

- Select attribute groups as required in the lists, for one or more object and query types.

If you need to restore the dialog box options to their default, click Default.

- (Optional) Click the Attribute Groups button if you need to modify the `QueryText` attribute group to open the Attribute Group Manager dialog box.

You can add or remove attributes in the attribute groups for one or more object types. For details about viewing and modifying the contents of an attribute group, see [Creating and Editing Attribute Groups](#).

- Click OK or Apply in the Customize Query Toolbar dialog box.

## See Also

- [Querying Objects in Graphic Views](#)

---

## Magnifying or Shrinking a View

You can use the zoom tools and the zoom commands to magnify or shrink the design in the active schematic or layout view or the histogram in the active histogram view. You can also use zoom commands to adjust the zoom level to display all selected objects or all highlighted objects in the active schematic or layout view.

To display the entire design,

- Click the  button on the View Zoom/Pan toolbar, or choose View > Zoom > Zoom Fit All.

To double the magnification,

- Click the  button on the View Zoom/Pan toolbar, or choose View > Zoom > Zoom In.

To magnify an area in the design interactively, click the  button on the Mouse Tools toolbar, or choose View > Zoom In tool, and perform either or both of the following actions:

- Click where you want to recenter the view and magnify it by a factor of 2.
- Drag the pointer diagonally across a rectangular area to magnify it to fill the view.

If the rectangular area is disproportional to the current view area, Design Vision tool uses the rectangular area to determine the height and width of the magnified area.

To shrink a view by half the magnification,

- Click the  button on the View Zoom/Pan toolbar, or choose View > Zoom > Zoom Out.

To shrink the design into a box that you specify interactively, click the  button on the Mouse Tools toolbar, or choose View > Zoom Out tool, and perform either or both of the following actions:

- Click where you want to recenter the design and shrink it by a factor of 2.
- Drag the pointer diagonally across a rectangular area to shrink the view by fitting it within the area.

If the rectangular area is disproportional to the current view area, Design Vision tool fits the current view into the width of the area you define.

To adjust the magnification level to fit the selected objects in a view,

- Click the  button on the View Zoom/Pan toolbar, or choose View > Zoom > Zoom Fit Selection.

To adjust the magnification level to fit the highlighted objects,

- Choose View > Zoom > Zoom Fit Highlight.

To display a rectangular area anywhere in the design by specifying its coordinates in the layout view,

- Choose View > Zoom > Zoom To.

The Zoom To dialog box appears.

- Enter the coordinates for the top-left and bottom-right corners of the rectangle.
- Click OK.

To apply the magnification level in the active layout view to other open layout views in the same layout window,

- Choose View > Zoom > Zoom Layout View to Current View.

## See Also

- [Selecting a Mouse Tool](#)
- [Traversing a View](#)
- [Navigating Through Layout Views](#)
- [Following Selected Objects](#)
- [Reusing Zoom and Pan Settings](#)

---

## Traversing a View

When only part of the design is visible in the active schematic or layout view or part of the histogram is visible in the active histogram view, you can use the Pan tool or the scroll bars to traverse the view to see different areas of the design or histogram. You can also use the pan commands to recenter the design by displaying selected objects or highlighted objects in the active schematic or layout view.

To traverse a view in any direction,

1. Click the  button on the Mouse Tools toolbar, or choose View > Mouse Tools > Pan Tool.
2. Drag the pointer toward the part of the design you want to see.

To recenter a view and display selected objects,

- Click the  button on the View Zoom/Pan toolbar, or choose View > Zoom > Pan To Selection.

To recenter a view and display highlighted objects,

- Choose View > Zoom > Pan To Highlight.

To traverse a view by using the scroll bars,

- Perform either or both of the following actions:
  - Click the horizontal scroll arrows or drag the horizontal scroll box to move the view left or right.
  - Click the vertical scroll arrows or drag the vertical scroll box to move the view up or down.

The scroll boxes represent the visible part of the view. When you move a scroll box, the view moves in that direction.

You can also use navigation keys (the arrow keys, Page Up, Page Down, Home, and End) to scroll or navigate through the view.

## See Also

- [Selecting a Mouse Tool](#)
- [Magnifying or Shrinking a View](#)
- [Navigating Through Layout Views](#)
- [Following Selected Objects](#)
- [Reusing Zoom and Pan Settings](#)

---

## Following Selected Objects

You can control whether the active schematic or layout view automatically zooms to an object when you select it, increasing or decreasing the magnification of the design to fit the object within the view.

To enable or disable the follow-selection mechanism for the active view,

- Choose View > Zoom > Zoom Follow Selection.

A check mark next to the `Zoom Follow Selection` command on the View menu indicates that the follow-selection mechanism is enabled.

You can enable or disable this automatic operation separately for each open schematic or layout view. When you enable this operation for a view, the operation remains enabled even when the view is not the active view. The follow-selection mechanism is disabled by default.

### See Also

- [Magnifying or Shrinking a View](#)
- [Traversing a View](#)

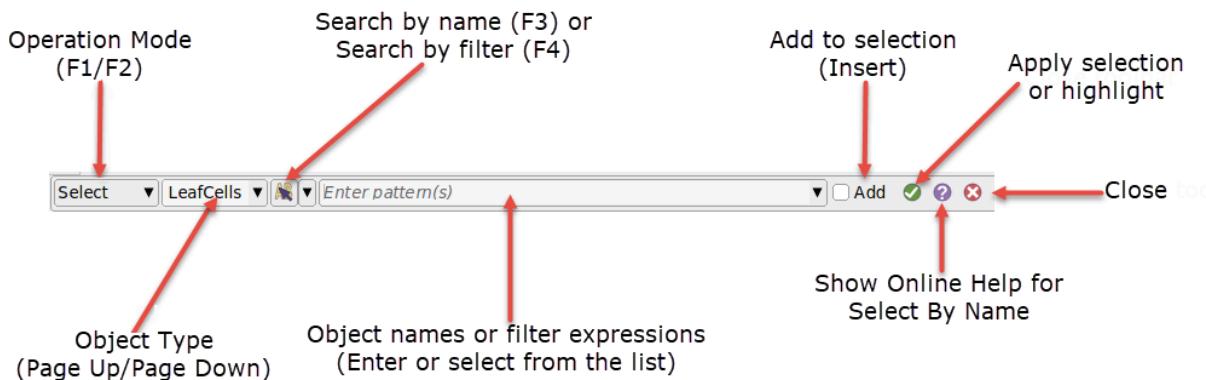
## Selecting Objects by Name

When you work in a schematic or layout view, you can find objects of interest by using the Select By Name toolbar. You can select or highlight objects in the active view by using keys on the keyboard or by setting options on the toolbar. To specify the objects, you can enter the names an expression to filter the names. You can also select object names or filter expression parts from a list.

To display the Select By Name toolbar and set the keyboard focus, choose Select > By Name Toolbar.

By default, the toolbar appears below the console tab as shown in [Figure 13](#). For help using the Select By Name toolbar, click the  icon.

*Figure 13     Select By Name Toolbar*



The Select By Name toolbar options are set by default to select cells by name and replace the current selection. To select one or more cells, you can enter the cell names and press Enter. You can enter multiple names, by separating them with blank spaces. You can also use wildcard characters (?) or (\*) to specify a name pattern for multiple names.

If an object name contains a space, enclose the name in braces ({} ) to treat it as a single name. If an object name is invalid because nothing matches the specified name or name pattern, the tool highlights it on a light red background.

You can set options to:

- Change the operation that you want to perform.

The options are Select, Highlight, and Tabulate. When you select objects, you can control whether the tool replaces or adds objects to the current selection.

- Change the type of objects that you want to find.

The options are LeafCells, Cells, LeafNets, Nets, LeafPins, Pins, Ports, or LibCells.

- Change the search type.

The options are Search by name and Search by filter.

When you begin entering an object name or filter expression, the characters appear in the text box on the toolbar. You can allow the tool to complete the name or the filter expression that you are entering by pressing the Tab key. The tool completes the name or filter to its longest match.

If the tool finds multiple objects or values that match the text you entered, the object name or filter expression list appears and the keyboard focus changes to the list. You can continue entering or selecting a name and close the list.

To select or highlight objects by using the Select By Name toolbar,

1. Select the operation that you want the tool to perform.

- To select objects, press F1 or select the Select option in the Operation Mode list.
- To highlight objects, press F2 or select the Highlight option in the Operation Mode list.

If you want to select objects instead of replacing the current selection, add them to the current selection instead of replacing the current selection, press the Insert key or select the Add option.

2. Select the object type.

You can select an option in the Object Type list or press the Page Up or Page Down key until the option you want appears in the list.

3. Select the search type.

- To search for objects by specifying their names, press the F3 key or click the arrow button and select the Search by name option.
- To search for objects by specifying a filter expression, press the F4 key or click the arrow button and select the Search by filter option.

The default search type is Search by name option.

4. Enter or select the object names or a filter expression.

- To open the object name or filter expression list, press the Down Arrow key.

Any characters that you type while the list is open automatically appear in the text box. This allows you to continue entering the object name or filter expressions, which automatically updates the list.

- To navigate up and down the list and select an object name or filter expression, press the Up Arrow and Down Arrow keys.
- To select multiple names in the object name list, press the Shift or Ctrl and click the names.

- To select all the names in the list, click  icon or press Ctrl+A.

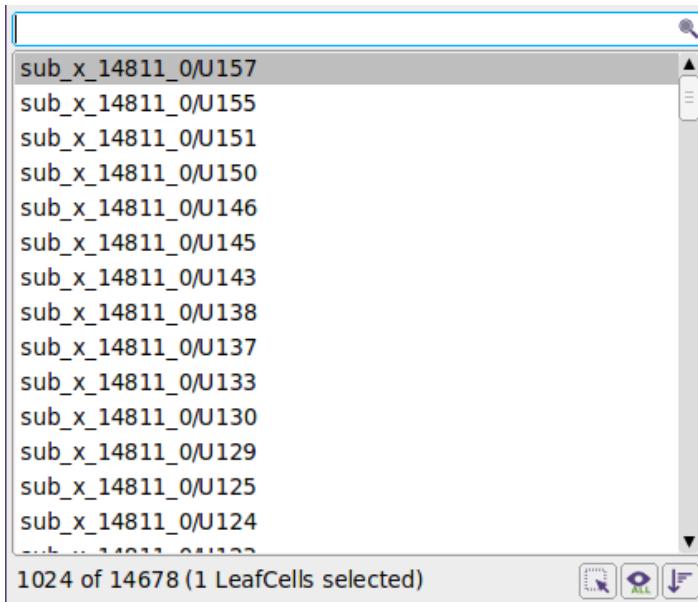
- To sort the names alphanumerically, click  icon.

- To include all matching names in the list, click the  icon.

- To display the selected object names or filter expression in the text box and close the list, press Enter.
- To close the list without changing the text box, press Escape.

5. Press the Enter key or click the  icon.

The following figure shows an example of the object name list with one name selected:



To close the Select By Name toolbar, press the Esc key or click the icon on the toolbar.

#### See Also

- [Select By Name Toolbar](#)

### Searching for Objects by Name or Regular Expression

You can use the Select By Name dialog box to search for objects by specifying the object names or a regular expression filter, and then select some or all of the objects found in the search. You can define and save filters for different object types based on object name patterns and attribute or function values. You can also copy or modify existing filters.

Selected objects are displayed in the selection color (white, by default) in graphic views and are indicated by reverse video in hierarchy views. The names of the selected objects appear in the selection list, and the number of selected objects appears in the status bar.

You can search for

- All objects in the design.
- Selected objects.
- All or selected objects found in the previous search.

The search results include the total number of objects found and a list of object names with the values of any attributes or functions used to generate the search. You can select object names in the list for the objects that you want to

- Replace in the current selection.
- Add to the current selection.
- Highlight in schematic and layout views.
- Remove from the current selection.

Alternatively, you can display the selected object names in a new list.

**Note:**

The Select By Name dialog box is designed for sophisticated object searches using filters or regular expressions. For faster object selection using object searches based on names or name patterns, use the Select By Name toolbar.

To search for and select design objects by name or regular expression,

1. Choose Select > By Name to open the Select By Name dialog box.
2. Select an object type and a design scope in the left and in the right Search for drop down lists.

The default object type is LeafCells and the default design scope is In entire design.

3. Perform one of the following searches:
  - To search for objects by name, select the Wildcard matching option (the default), and type an object name or name pattern (with wildcards) in the Name text box.
  - To search for objects by using a previously defined search filter, select the Full regular expressions option and select the filter name in the Filter list.
  - To search for objects by defining a new search filter, select the Full regular expressions option and define the filter.

You can build a search filter with one or more terms. To start a new filter, click the Add Term button and select an object name, an operator, and a value in the table below the Name text box. To add a term, select AND or OR in the Next Term list.

If you want to save the filter for future use, click the Save button to open the Save Filter As dialog box, type a filter name, and click OK. The GUI adds the filter name to the Filter list and saves the filter definition in your preferences file.

You can delete a saved filter by selecting the filter name in the Filter list and clicking the Delete button.

4. Set other options as needed.

A preview of the `get_cells` command (based on the search options you set) appears above the Search button. You can copy and paste it for reuse.

- To make the search case sensitive, select the Match case option.
- To add new search results to the list (instead of replacing previous results in the list), select the Append to results option.

5. Click Search.

The names of the objects found in the search appear in the Search results list. Initially, all the names in the list are selected.

6. Select the names of objects in the Search results list that you want to select, deselect, or highlight in the layout view.

- To select all the object names in the list, click the All button.
- To deselect all the object names in the list, click the None button.
- To select some object names and remove unselected names from the list, select the names you want to keep in the list and click the Keep button.
- To remove some object names from the list, select the names you want to remove and click the Remove button.

7. Select or highlight objects by performing one or more of the following tasks:

- To select objects and replace the current selection, select the object names, select the Replace option, and click the Change Selection button.
- To select objects and add them to the current selection, select the object names, select the Add to option, and click the Change Selection button.
- To highlight objects, select the object names and click the Add to Highlight button.  
The tool highlights the objects in the current highlight color.
- To deselect objects (remove them from the current selection), select the object names, select the Remove from option, and click the Change Selection button.
- To display object names in a new list view, select the object names and click the Show in Table View button.

## Deselecting All Selected Objects

You can deselect all selected design objects and timing paths in the current design.

To deselect all selected objects and paths, choose Select > Clear.

Alternatively, you can click anywhere in the background of the active schematic or layout view.

### See Also

- [Selecting Objects in Graphic Views](#)
  - [Selecting Highlighted Objects and Paths](#)
  - [Selecting Bus Objects](#)
  - [Selecting a Collection of Objects](#)
  - [Selecting Timing Paths](#)
  - [Selecting Fanin or Fanout Logic](#)
- 

## Reusing Zoom and Pan Settings

Design Vision tool maintains a list of zoom and pan settings for each open schematic or layout view. A zoom and pan setting consists of both a zoom (magnification) level and a pan position (visible area). When you change the magnification or traverse the view (by panning or scrolling), the previous zoom and pan setting is added to the list.

You can:

- Reverse the zoom level and pan position to the last zoom and pan setting by stepping backward in the list toward the initial display when you opened the view
- Reapply the next (previously reversed) zoom level and pan position by stepping forward in the list after stepping backward in the list
- Save the current zoom level and pan position in a list named zoom and pan settings
- Return the view to a certain zoom level and pan position by selecting a named zoom and pan setting that you saved earlier in the session

To return to the last zoom level and pan position in the list,

1. Click the  button on the Zoom and Pan History toolbar.  
or  
Choose View > Back in Zoom and Pan History.
2. (Optional) To step backward in the list of zoom and pan settings toward the initial zoom level and pan position when you opened the view repeat step 1.

To reapply the next zoom level and pan position in the list,

1. Click the  button on the Zoom and Pan History toolbar.

or

Choose View > Forward in Zoom and Pan History.
2. (Optional) To step forward in the list of zoom and pan settings toward the last zoom level and pan position displayed in the view repeat step 1.

#### See Also

- [Magnifying or Shrinking a View](#)
- [Traversing a View](#)

---

## Redrawing the Active View

You can redraw the active schematic or layout view.

To redraw the active view,

- Choose View > Refresh.

---

## Saving an Image of a Window or View

You can save an image of a top-level GUI window or view window in an image file. The image format can be PNG (the default), BMP, JPEG, or XPM. The image shows the window exactly as it appears on the screen but without the window border or title bar. For example, if you save an image of the active schematic view, the image shows the visible portion of the schematic at the current zoom level and pan position.

- To save an image of the current top-level window or the active view, use the Save Screenshot As dialog box.
- To save an image of any open GUI window or view window, use the `gui_write_window_image` command.

You cannot save images of dialog boxes or other GUI elements such as toolbars or panels.

To save an image of the current window or active view,

1. Choose View > Save Screenshot As.

The Save Screenshot As dialog box appears.
2. Select the file, or enter the path and file name in the File name text box.

The default format is PNG. You can specify a different format by specifying its extension in the File name.

3. (Optional) To save an image of the active view window instead of the top-level GUI window in which you are working, select the Grab screenshot of active view only option.
4. Click Open.

To save an image of any open GUI or view window, use the `gui_write_window_image` command to specify the file name, image format, and window name. Window instance names appear in the window title bars and on the Window menu.

- Use the `-file` option to specify the file name which is the required option. For example, to save a PNG image of the active schematic view in a file named `my_schematic.png`, you can enter
 

```
prompt> gui_write_window_image -file my_schematic
```
- You can use a file name extension or the `-format` option to specify the image format. The default image format is PNG. For example, to save the XPM image of the active layout view in a file named `my_layout.xpm`, enter either of the following commands:

```
prompt> gui_write_window_image -file my_layout.xpm
prompt> gui_write_window_image -file my_layout -format xpm
```

- Use the `-window` option to specify the window. For example, to save a PNG image of the Layout window named `Layout.1` in a file named `mx_1.png`, enter the following command:

```
prompt> gui_write_window_image -file mx_1.png -window Layout.1
```

If you want to save an image or a window or view when running the tool with a batch script, you can use the `gui_write_window_image` command in a Tcl script.

The following script is an example to show the commands to use to open the GUI, open a Layout window, save a PNG image of the Layout window, and close the GUI:

```
## Set the DISPLAY environment variable before opening the GUI.
## Replace "my_display_name" with the host name of your display terminal.
setenv DISPLAY my_display_name

## Open the GUI.
gui_start

## Create a new Layout window and store its name in a Tcl variable.
## Replace "window_name" with the name of your variable.
set window_name [gui_create_window -type LayoutWindow]
```

```
## Save an image of the window in a file named my_layout.png.  
## Replace "window_name" with the name of your variable.  
gui_write_window_image -file my_layout.png -window $window_name  
  
## Remove the comment (#) from the next line to close the GUI here.  
#gui_stop
```

The following script example includes the commands to use to save a JPEG image of the congestion map:

```
## Set the DISPLAY environment variable before opening the GUI.  
setenv DISPLAY my_display_name  
  
## Open the GUI.  
gui_start  
  
## Create a new Layout window and store its name in a Tcl variable.  
set window_name [gui_create_window -type LayoutWindow]  
  
## Hide preroutes in the layout view.  
gui_set_setting -window [gui_get_current_window -types Layout -mru] \  
    -setting showRoute -value false  
  
## Display the congestion map.  
gui_show_map -window [gui_get_current_window -types Layout -mru] \  
    -map {Global Route Congestion} -show true  
  
## Save an image of the window in a file named my_congestion.jpg.  
gui_write_window_image -format jpg -window $window_name \  
    -file my_congestion.jpg  
  
## Remove the comment (#) from the next line to close the GUI here.  
#gui_stop
```

Similarly, you can save an image of a visual mode after displaying it in the Layout window.

For more information, see the [gui\\_write\\_window\\_image command man page](#).

## See Also

- [Printing Schematic Views](#)

---

## Viewing Schematics

Schematic views display graphic representations of design logic and timing paths in a flat, single-sheet schematic that can span multiple hierarchy levels. You can use schematic views to visually analyze timing and logic in the optimized design and to gather information to guide later optimization operations.

You can create a schematic for the top-level design, for a hierarchical cell, or for selected timing paths, design objects, or both. A schematic can consist of instances (cells), ports, pins, nets, buses, bus rippers, and hierarchy crossings. When you select or highlight a timing path, the schematic represents the path as a series of net connections between pins or a pin and a port.

To learn more about viewing schematics, see the following topics:

- [Viewing Cells Hierarchically](#)
- [Displaying or Hiding Buffers and Inverters](#)
- [Displaying or Hiding Unconnected Macro Pins](#)
- [Expanding and Collapsing Buses](#)
- [Adding or Removing Selected Logic](#)
- [Adding Fanin or Fanout Logic](#)
- [Adding Worst Paths Through Objects](#)
- [Reversing and Reapplying Schematic Changes](#)
- [Printing Schematic Views](#)
- [Changing the Appearance of Schematics](#)

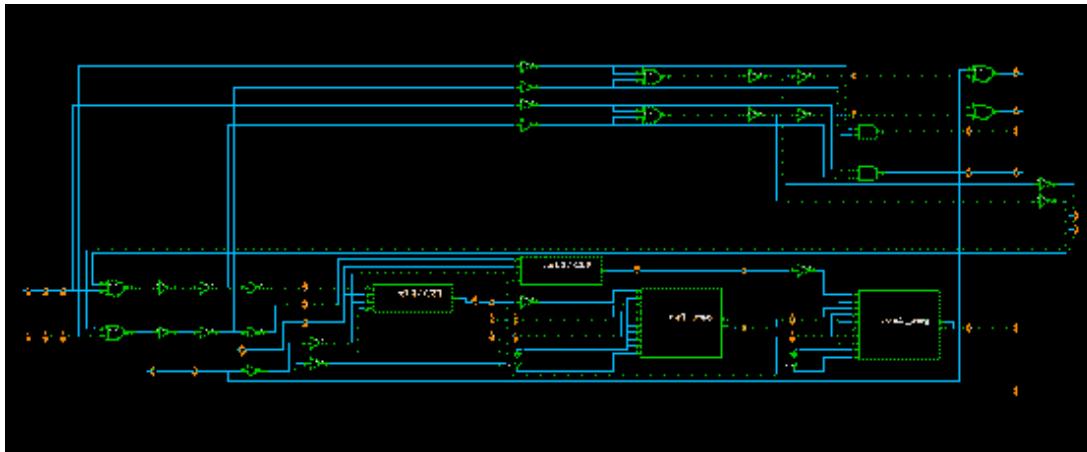
### See Also

- [Viewing a Design Interactively](#)

---

## Viewing Cells Hierarchically

By default, a schematic that contains multiple levels of hierarchy displays the objects in a flat, single-sheet schematic with input ports on the left and output ports on the right. Hierarchy crossings (diamond shapes) indicate where nets traverse a level of hierarchy.

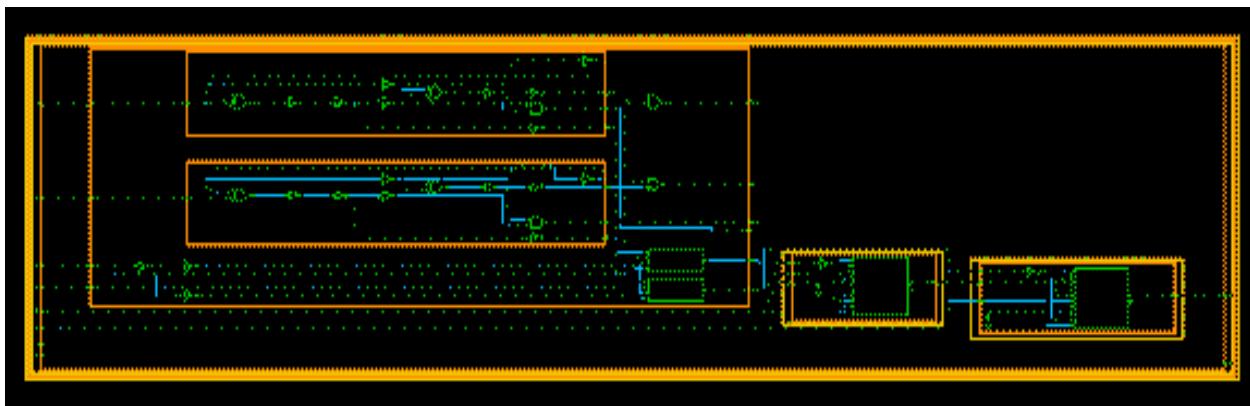


You can reorganize the schematic hierarchically and display rectangular boundaries for the top-level design and each hierarchical set of objects.

To display or hide hierarchical cell boundaries in the active schematic view, choose Schematic > Show Logic/Power Hierarchy.

A check mark against the command on the Schematic menu indicates that the boundaries are visible.

The tool rearranges the schematic so that objects are placed hierarchically, which puts objects that share the same hierarchical parent near each other. The logic hierarchy boundaries are in orange, and the power domain boundaries in yellow.



To facilitate your analysis of a multivoltage design with IEEE 1801 power domains, you can color the boundaries based on the hierarchical power relationships of the design. IEEE 1801 is also known as Unified Power Format (UPF).

To display or hide boundary coloring based on their power domains, choose Schematic > Color by Power Hierarchy.

A check mark against the command on the Schematic menu indicates that the boundary coloring is visible.

The tool displays the objects for each power domain with a unique color.



For more information about working with multivoltage designs, see [Defining and Viewing the Power Intent for Multivoltage Designs](#).

### See Also

- [Schematic Views](#)
- [Examining Hierarchical Cells](#)

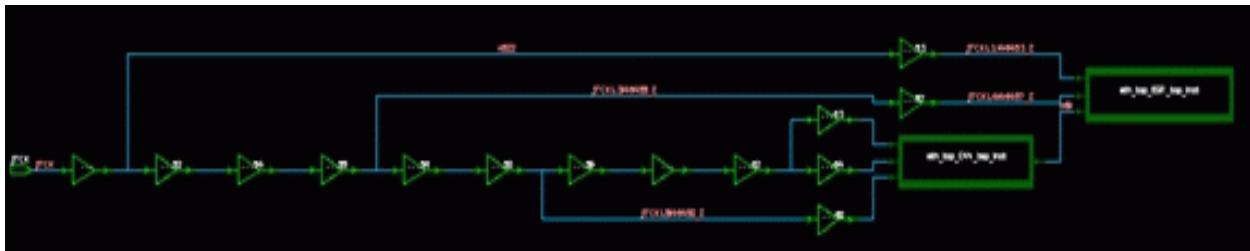
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## Displaying or Hiding Buffers and Inverters

By default, a schematic view displays design objects and timing paths in a flat, single-sheet schematic, with hierarchy crossings (diamond shapes) showing where nets traverse a level of hierarchy. Each timing path consists of the objects (cells, pins, and nets) that make up the path. A path can include long chains of buffers or inverters and multiple hierarchy crossings.

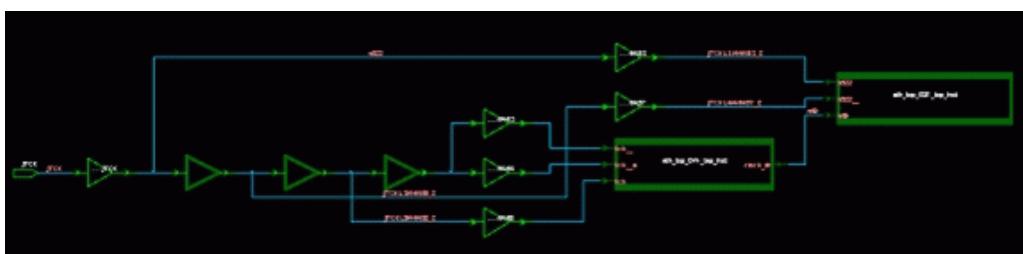
To avoid examining the progression of a signal across long buffer and inverter chains or through unimportant blocks, you can hide some objects by collapsing them into abstract metacells. You can hide buffer and inverter chains or buffer and inverter trees.

The following example shows a schematic with the buffers and inverters fully expanded:



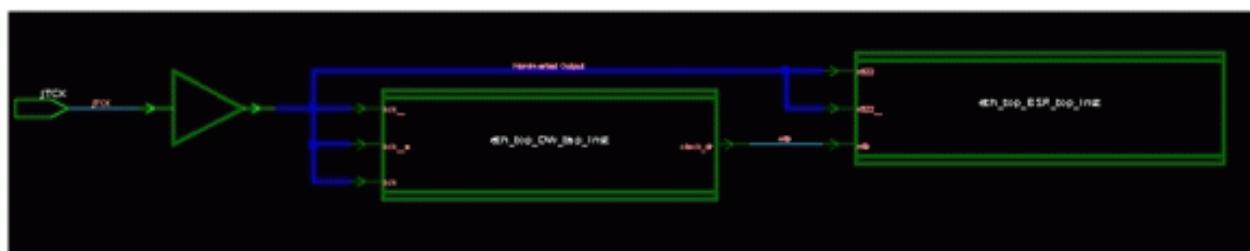
To hide buffer and inverter chains,

- Choose Schematic > Collapse > All Buffers/Inverters/Crossings By Chain.



To hide buffer and inverter trees,

- Choose Schematic > Collapse > All Buffers/Inverters/Crossings By Tree.



To hide individual buffers, inverters, and hierarchy crossings,

- Select the buffers, inverters, and hierarchy crossings that you want to hide.

- Click the  button on the Schematic toolbar, or choose Schematic > Collapse > Selected Buffers/Inverters/Crossings.

For a buffer or inverter chain or a buffer or inverter tree that results in a noninverted output, the metacell is similar to a buffer but has a thicker line width and darker color. For a buffer or inverter chain or a buffer or inverter tree that results in an inverted output, the metacell is similar to an inverter but has a thicker line width and darker color.

For a buffer or inverter tree that results in both noninverted and inverted outputs, the metacell combines the appearance of both an inverter and a buffer. The symbol has both

inverted and noninverted outputs with the loads of the chain connected to the appropriate polarity output.

To expand all buffer and inverter metacells and display the buffers and inverters,

- Choose Schematic > Expand > All Buffers/Inverters/Crossings.

To expand individual buffer and inverter metacells,

- Select the metacells that you want to expand.

- Click the  button on the Schematics toolbar, or choose Schematic > Expand > Selected Objects.

Alternatively, you can double-click the metacells.

## See Also

- [Schematic Views](#)
- [Displaying or Hiding Unconnected Macro Pins](#)
- [Expanding and Collapsing Buses](#)
- [Examining Hierarchical Cells](#)

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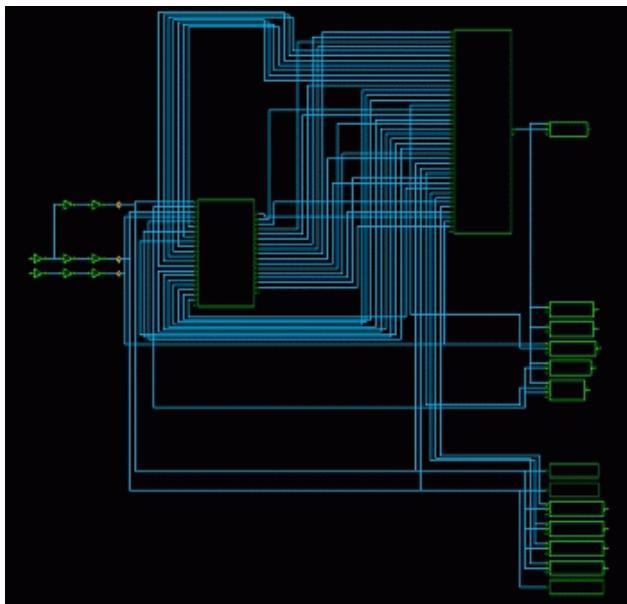
## Displaying or Hiding Unconnected Macro Pins

To simplify a schematic and hide unimportant details, you can hide the unconnected pins of macro cells by collapsing them into metapins. The hidden pins are represented by metapins of the same type: in, out, in/out, and bidirectional. A metapin is similar to a design pin but has a thicker line width and a different color.

To hide the unconnected pins of macro cells,

- Choose Schematic > Collapse > All Unconnected Pins.

Unconnected pins are represented by metapins of the same type: in, out, in/out, and bidirectional. A metapin is similar to a design pin but has a thicker line width and a different color.



To expand all unconnected pin metapins, choose Schematic > Expand > All Unconnected Pins.

### See Also

- [Schematic Views](#)
- [Displaying or Hiding Unconnected Macro Pins](#)
- [Expanding and Collapsing Buses](#)
- [Examining Hierarchical Cells](#)

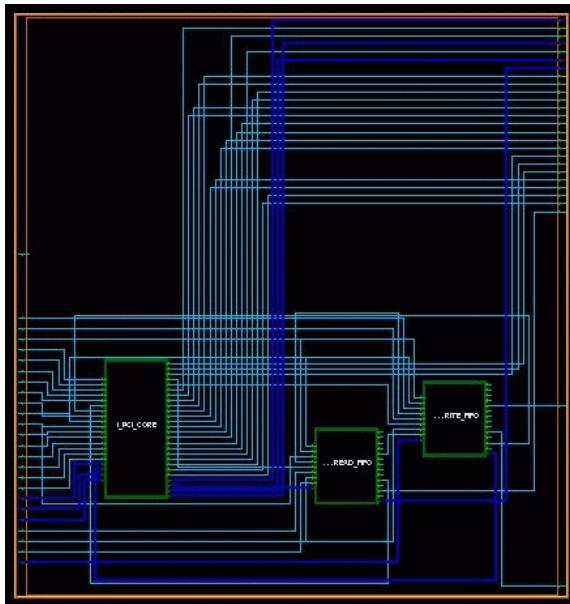
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## Expanding and Collapsing Buses

You can save space in a schematic by collapsing nets and pins that are members of a bus. This allows you to focus on the nets that are of interest while keeping the overall context in view, as you debug timing and connectivity problems.

To collapse bus nets and pins, choose Schematic > Collapse > All Bussed Pins/Nets.

The collapsed nets are rendered in a darker blue with a thicker line width, and the pins are rendered in a darker green.



You can view the names of the collapsed nets or pins in InfoTips or by using the Query tool.

To expand bus nets and pins, choose Schematic > Expand > All Bussed Pins/Nets.

### See Also

- [Schematic Views](#)
- [Displaying or Hiding Unconnected Macro Pins](#)
- [Displaying or Hiding Buffers and Inverters](#)
- [Examining Hierarchical Cells](#)

---

## Adding or Removing Selected Logic

You can add or remove selected objects (cells, ports, or nets) in the active schematic view.

To add logic to a schematic,

1. Select one or more objects (cells, ports, or nets) to add.

You can select the objects in another schematic view, the logic hierarchy view, the layout view, or an object list, or you can choose a command on the Select menu.

2. Click in the schematic view window to make it the active view.
3. Choose Schematic > Add Selected.

To remove logic from a schematic,

1. Select one or more objects (cells, ports, or nets) to remove.
2. Choose Schematic > Delete Selected.

The objects are added or removed only in the active schematic view. The netlist is not changed and other schematic views are not affected.

When you add or remove the selected logic, a new schematic appears and the old schematic (with the selected logic) is retained and saved on a memory stack.

#### See Also

- [Schematic Views](#)

---

## Adding Fanin or Fanout Logic

You can view fanin or fanout logic for a selected cell, pin, port, or net by displaying objects in a schematic view. You can add logic levels in the active schematic view or open a new schematic view. You can also quickly add the next logic level for a pin or the pins of a cell in the active schematic view.

#### Note:

You can also add fanin or fanout logic to the schematic in a path inspector window.

To quickly add the next fanin or fanout logic level for a pin or the pins of a cell,

- Select the pin or cell and choose Schematic > Add Next Fanin/Fanout Level.

Alternatively, you can double-click the pin or cell.

You can display any number of fanin or fanout logic levels by using the Add Fanin/Fanout to Path Schematic dialog box. You can set options to control the number of logic levels and how the logic is displayed. You can also control where the tool displays the fanin or fanout logic.

- If you display the fanin or fanout logic in the active schematic view, you can control whether the logic is added to or replaces the timing paths and logic in the schematic.
- If you open a new schematic view, you can control whether the paths and logic from the active schematic view are included in the new schematic view.

To display any number of fanin or fanout logic levels for an object,

1. Select one or more cells, pins, ports, or nets.
2. Click the  button on the Schematics toolbar, or choose Schematic > Add Fanin/Fanout.

The Add Fanin/Fanout to Path Schematic dialog box appears. The name, full name (including the path from the top-level design), and type of each selected object appear in the Start Logic list.

3. Select either the Fanin option (to add fanin logic) or the Fanout option (to add fanout logic). Fanout is selected by default.
4. Select an option to specify the number of logic levels.
  - To add all logic levels, select the All levels option.
  - To add just one logic level, select the One level option.
  - To add any number of logic levels, select the N levels option and select or enter the number of levels in the N levels text box. The default is 2.
5. (Optional) Edit the Start Logic list as needed.
  - To display different object names in the list, select the objects and click the Set Selected button.
  - To add object names to the list, select the objects and click the Add Selected button.Alternatively, you can click the Browse button and select the object name in the Object Chooser dialog box. For details, see [Selecting Objects in the Object Chooser](#).
  - To remove object names from the list, select the object names and click the Remove button.
  - To remove all the object names from the list, click the Clear button.
6. (Optional) Edit the Stop Logic list as needed.
  - a. Click the Stop Logic tab.
  - b. Specify object names in the Stop Logic list.

When you specify stop-logic objects that are within the specified logic levels, each fanin or fanout cone ends at the first stop-logic object it encounters.

- To display object names in the list, select the objects and click the Set Selected button.
- To add object names to the list, select the objects and click the Add Selected button.

Alternatively, you can click the Browse button and select the object name in the Object Chooser dialog box. For details, see [Selecting Objects in the Object Chooser](#).

- To remove object names from the list, select the object names and click the Remove button.
  - To remove all the object names from the list, click the Clear button.
7. If you do not want the fanin or fanout cones to stop at sequential logic objects, deselect the Stop at sequential cells option.
8. Set options to control whether the fanin or fanout logic is added to the active schematic view or displayed in a new schematic view.

By default, the fanin or fanout logic is added to the active schematic view.

- To replace the current paths or objects in the active schematic view (instead of adding the fanin or fanout logic to them), deselect the Base on netlist of active window option.
- To open a new schematic view and display both the fanin or fanout logic and the paths or objects in the active schematic view, deselect the Reuse active window if applicable option.
- To open a new schematic view and display only the fanin or fanout logic, deselect both the Base on netlist of active window and Reuse active window if applicable options.
- To replace the schematic displayed in the active schematic view (rather than retain it on the memory stack), deselect the Push new netlist option (effective only when the Reuse active window if applicable option is selected).

9. Click OK.

You can also add worst-path logic to a schematic. For details, see [Adding Worst Paths Through Objects](#).

## See Also

- [Schematic Views](#)

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## Adding Worst Paths Through Objects

You can view one or more timing paths by displaying them in a schematic. You can add the timing paths to the active schematic view or open a new schematic view. You can display either the timing paths with the worst slack in the current design or the paths with the worst slack from, to, or through selected cells, nets, pins, or ports.

You can set options in the Add Paths to Path Schematic dialog box to set the type and number of timing paths and control how the paths are displayed. You can also specify the startpoints, endpoints, and throughpoints for specific paths.

The default timing path is the path with the worst slack in the current design. You can set options to

- Display paths from a specific path group.
- Display up to a maximum number of paths with the worst slack in the current design (or in the specified path group).
- Display up to a maximum number of paths to any single endpoint.

You can display specific paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the only paths that are added are those that start at the specified startpoints, end at the specified endpoints, or pass through one or more specified throughpoints. For details, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

By default, the paths are based on maximum delay times. This allows you to view path setup times. You can change the delay type option and base the paths on

- Minimum delay times (to view path hold times)
- Minimum rising delays
- Minimum falling delays
- Maximum rising delays
- Maximum falling delays

You can also set options to

- Enable preset and clear arcs.
- Include hierarchical pins.

In addition, you can control where the tool displays the timing paths in the following ways:

- If you display the timing paths in the active schematic view, you can control whether the paths are added to or replace the paths and logic in the schematic.
- If you open a new schematic view, you can control whether the paths and logic from the active schematic view are included in the new schematic view.

To display the timing paths in a schematic view,

1. Click the  button on the Schematics toolbar, or choose Schematic > Add Paths From/Through/To.

The Add Paths From/Through/To to Path Schematic dialog box appears.

2. (Optional) Specify the path startpoints (From), throughpoints (Through), or endpoints (To).

First, select an object type. Startpoints and endpoints can be pins, ports, nets, or clock. Throughpoints can be pins or nets. Then, do one of the following:

- Enter one or more object names.
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

3. Set options to control the maximum number of paths.
  - To change the maximum number of paths, enter a value in the Max paths box.
  - To change the maximum number of paths to an endpoint, enter a value in the Nworst paths box.
4. To specify a path group, select its name in the Group name drop-down list.
5. (Optional) Change the delay type for the path by selecting an option in the Delay type drop-down list (see the following table). The default (max) is set for maximum delays.

Delay type	Description
min	For minimum delays
max_rise	For maximum rising delays
max_fall	For maximum falling delays

Delay type	Description
min_rise	For minimum rising delays
min_fall	For minimum falling delays,

6. (Optional) Select other options:
  - To include preset and clear arcs in the paths, select the Enable preset clear arcs option.
  - To exclude hierarchical pins from the paths, deselect the Include hierarchical pins option.
7. Set options to control whether the paths are added to the active schematic view or displayed in a new schematic view.  
By default, the paths are added to the active schematic view.
  - To replace the current paths or objects in the active schematic view (instead of adding the paths to them), deselect the Based on netlist of active window option.
  - To open a new schematic view and display both the new paths and the paths or objects in the active schematic view, deselect the Reuse active window if applicable option.
  - To open a new schematic view and display only the new paths, deselect both the Based on netlist of active window and Reuse active window if applicable options.
  - To replace the schematic displayed in the active schematic view (rather than retain it on the memory stack), deselect the Push new netlist option (effective only when the Reuse active window if applicable option is selected).

8. Click OK or Apply.

You can also add fanin or fanout logic to a schematic. For details, see [Adding Fanin or Fanout Logic](#).

## See Also

- [Schematic Views](#)

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## Reversing and Reapplying Schematic Changes

You can reverse and reapply changes that you made in a schematic view, such as expanding or collapsing design logic or adding or removing objects or timing paths.

To reverse changes in a schematic,

1. Choose Schematic > Back.
2. (Optional) To reverse the next most recent change repeat step 1.

When you reverse a change, the GUI retains a copy of the changed schematic, and redisplays it if you reapply the change.

To reapply changes in a schematic,

1. Choose Schematic > Forward.
2. (Optional) To reapply the next most recent change repeat step 1.

#### See Also

- [Schematic Views](#)
- 

## Printing Schematic Views

You can print the schematic displayed in the active schematic view. Before printing a schematic view, make sure that a default printer is set in your .cshrc file. You can print the contents of a schematic view or save an image of the view in a PDF or PostScript file, for printing later from a UNIX or Linux shell.

To print the active schematic view,

1. Generate the schematic.
2. Make sure the schematic to print is in the active view.

Click the corresponding tab at the bottom of the workspace if you need to make the view active.

3. Click the  button on the File toolbar or choose File > Print.

The Print dialog box appears.

4. Select a print destination.

You can send the schematic to a printer or save it in a file.

- To print the view, select a printer name in the Name list.

The name of your default printer appears in the Name list by default.

- To save a PDF version of the view in a file that you can view or print later in Adobe Acrobat, select Print to File (PDF) option in the Name list and enter a file name in the Output file text box.

Alternatively, you can specify the file name by clicking the browse button and selecting or entering the file name in the Print To File dialog box.

- To save a PostScript version of the view in a file you can print later, select Print to File (Postscript) option in the Name list and then enter a file name in the Output file text box.

Alternatively, you can specify the file name by clicking the browse button and selecting or entering the file name in the Print To File dialog box.

5. (Optional) Click the Properties button and set the printer properties in the printer properties dialog box.

You can set the paper size, page orientation, and page margins.

6. (Optional) Click the Options button and set the print options:

- To set a page range and the number of copies, click the Copies tab.

By default, these options are set to print all pages and a single copy. You can also set options to collate the pages and reverse the page order.

- To set duplex printing and color mode options, click the Options tab.

By default, duplex printing is set to None and the color mode is set to Grayscale.

7. Click Print.

## See Also

- [Saving an Image of a Window or View](#)

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## Changing the Appearance of Schematics

For display purposes only, when the GUI generates a schematic, it applies the same display characteristics to all the objects or text of a given object type. The default display characteristics work accurately for most designs. However, if you need to customize schematics for a specific design or environment, you can use the View Settings panel to perform the following:

- Change the colors for different types of design objects (cells, ports, pins, nets, buses, bus rippers, or hierarchy crossings)
- Change the colors or text sizes for different types of object names or object annotations
- Hide or display different types of object names or object annotations
- Display options for the background color, highlighted timing paths, and InfoTips

The changes apply only to the active view. However, you can save the new settings for use in the new schematic views that you open in future Design Vision tool sessions.

To change visual display settings in the active schematic view:

1. Choose View > Toolbars > View Settings to open the View Settings panel if it is not already open.
2. To change object type colors, click the Objects tab.
3. Set the required options.
4. Click Apply.

**Note:**

By default, you must click Apply on the View Settings panel to apply your changes to the active layout view. However, you can enable a mechanism that automatically applies changes when you make them, instead of only when you click Apply.

You can perform the following functions on the View Settings panel:

1. To enable or disable the automatic apply mechanism, choose Show Options > Auto Apply.  
Alternatively, when the automatic apply mechanism is disabled, you can reverse changes that you have not already applied.
2. To reset options to their state the last time you clicked Apply, choose Show Options > Cancel changes.

You can also restore previously saved view settings by loading them from your preferences file.

You can use the View Settings panel with any schematic view or DRC violation schematic. Each new schematic you open reads the default display characteristics from your preferences file.

**Note:**

Design Vision tool does not automatically save display properties when you close the GUI or exit the session.

## Changing Object Colors

You can use the View Settings panel to change object colors in the active schematic view. You can change the color for cell outlines, ports, pins, nets, buses, bus rippers, or hierarchy crossings.

**Note:**

Make sure the schematic view you want to customize is the active view.

To change object colors,

1. Click the color button for the object type you want to change .

The Select Styles dialog box appears. You can hold the pointer over a color to see its name and color values.

2. Select a color on the color palette.

Alternatively, you can click the Custom tab and define a custom color.

The preview box (New) displays the new color.

3. When you are satisfied with the color in the preview box, click OK to close the Select Styles dialog box.

The color button on the View Settings panel changes to show the new color.

4. (Optional) If you want to change the color for another object type repeat steps 2 through 4.

5. Click Apply.

## Changing Schematic Settings

You can use the View Settings panel to change the display options for the active schematic view. You can set the display style for highlighted timing paths and enable or disable InfoTips.

To change the timing path highlighting style,

1. Make sure the schematic view you want to customize is the active view.

2. Click the Settings tab on the View Settings panel.

3. Set options as needed.

- To change the background color, click the Background color button to open the Select Style dialog box, select a standard color on the color palette, and click OK.

The button on the View Settings panel changes to show the new color.

Alternatively, you can create a custom color. For details, see [Creating a Custom Color](#).

- To change the display of highlighted timing paths from net segments to net connections, deselect the Highlight net segments option.
- To enable InfoTips, select the Show InfoTip option.

Enable or disable InfoTips as needed.

- To enable InfoTips, select the Show InfoTip option.
- To disable InfoTips, deselect the Show InfoTip option.

**Note:**

You can enable or disable InfoTips in the active schematic view by choosing View > InfoTip.

4. Click Apply.

## Saving New Settings

To save the settings in the preferences file, on the View Settings panel

- For saving new settings, choose Show Options > Save to Preferences.
- For the active schematic or UPF diagram view, choose Show Options > Preferences > Save to Preferences.
- For the active layout view, choose Show Options > Preferences > Save to Preferences.

## Loading New Settings

To load the display properties from your preferences file, on the View Settings panel,

- For saving new settings, choose Show Options > Set to Preferences.
- For the active schematic or UPF diagram view, choose Show Options > Preferences > Set to Preferences.
- For the active layout view, choose Show Options > Preferences > Set to Preferences.

## Saving the Current Display Properties in a Tcl Script

To save the current display properties in a Tcl script,

1. Open the Write Settings Script dialog box.
  - a. For a schematic or UPF diagram view, choose Show Options > Write Settings Script.
  - b. For a layout view, click and choose Write Settings Script.
2. Select a file or enter a file name.
3. Click Save.

You can also export the current display properties to a Tcl script.

## Using User Tables

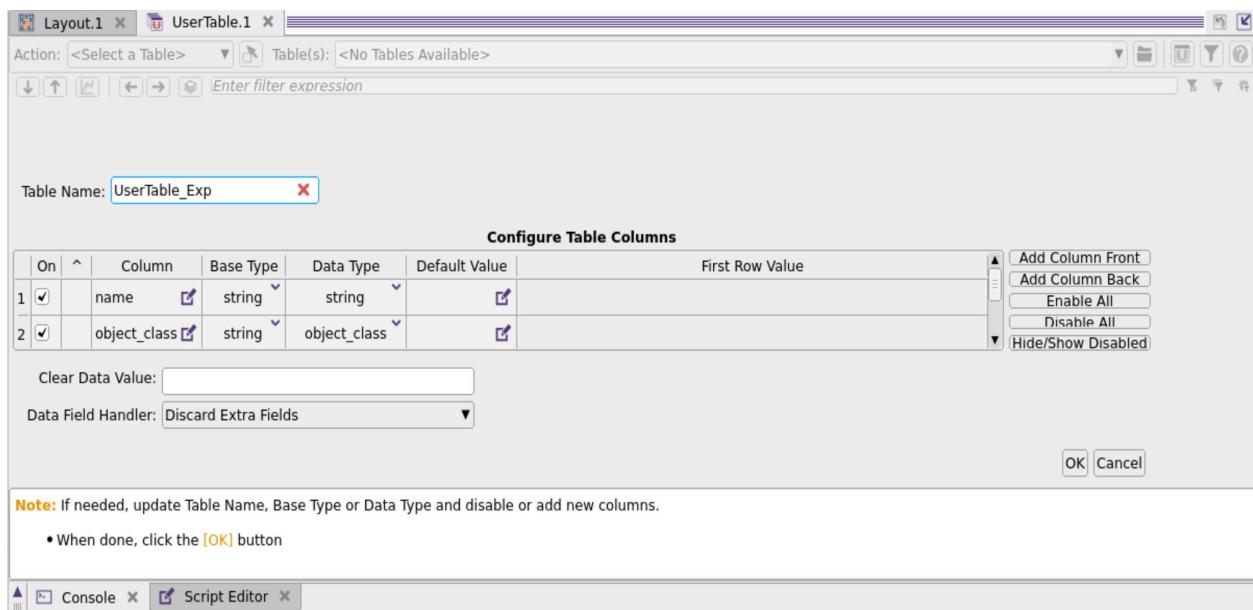
User tables provide a way to import, define, interact, and save tables of data. You can save a user table to a file that exists apart from the design database and reload the file in a later tool session. User tables can be generated from a selection list or from a comma- or tab-separated file.

User tables support many common spreadsheet operations, such as editing, sorting, filtering, summing, viewing distributions of column values, and so on. In addition, you can change the current selection by clicking rows in the user table.

### Creating a User Table

To create a user table from an existing selection set in the design,

1. Open the Selection List dialog box by clicking the Selection List button ( ) or choose **Select > Selection List** from the menu.
2. Click the **Export > User Table** button to create the user table based on the current values in the selection list.  
The tool copies the values to the user table import form.
3. (Optional) Change the table name in the Table Name box.
4. Click **OK** to import the data and build the user table.



To create a user table by importing a comma- or tab-separated text file,

1. Choose **View > User Tables** from the menu.
  2. Click the **Open** button () near the top of the user table form.
  3. Complete the form by selecting the separator (comma or tab). Optionally, enter a table name.
  4. Enter or choose a file name.
  5. In the Configure Table Columns form, set the data type for each column as needed.
  6. Click **OK** to create the user table.
- 

## Saving and Reloading a User Table

To save a user table,

1. Choose **Save** in the **Action** box near the top of the form.
2. Enter the file name in which to save the database. User tables typically have a .utable extension.
3. Click **OK**.

The tool writes out the user table data to the specified file.

To load a saved user table,

1. Click the **Open** button () near the top of the user table form.
  2. Choose **Open UserTable file** from the **Select** drop-down box.
  3. Enter the user table file name to be loaded.
  4. Click **OK**.
- 

## Analyzing Data in a User Table

After creating a user table, you can perform the following operations:

- Sort or reverse the sort of the table by right-clicking a column header and choosing the up or down arrow buttons.
- Filter the table by using one of the following methods:
  - Clicking the filter button ()
  - Entering column iterator and reduction functions in the filtering field.

The supported functions include: approx(), abs(), round(), scale(), offset(), min(), max(), sum(), count(), avg(), mean(), median(), lower\_quartile(), upper\_quartile(), stdev(), second\_stdev(), and third\_stdev().

An example of an iterator function is Tot Power > @Lkg Power, which shows all the rows where this expression is true. You refer to a column by using the @column\_name syntax.

An example of a reduction function is Lkg\ Power > #mean(Tot\ Power).

In the following example, the filtering query shows all the rows where the “Tot Power” in a given row is approximately equal to 10% of “Lkg Power” in that same row.

#### Note:

The approx() function can only appear on the right-hand side of the expression.

	status	comment	Logical Hierarchy	Object	Tot Power	Int Power	Swt Power	Lkg Power	Ge
1	0		ORCA	block	482.000m	-2.160m	838.000μ	483.000m	
2	0		Local_Logic	cell	22.176m	169.300μ	146.680μ	20.728m	
3	0		I_CLOCKING	cell	4.710m	62.800μ	35.700μ	4.610m	
4	0		I_PCI_TOP	cell	71.400m	-173.000μ	70.200μ	71.500m	
5	0		I_PARSE	cell	14.600m	23.800μ	16.800μ	14.600m	

- Rearrange the order of columns in the table by clicking and dragging the column header. Alternatively, right-click a column header and choose **More Column Options > Configure Columns** from the context menu to open the Configure Columns dialog box.
- Select a user table to display by clicking the Tables box near the top of the user table form and selecting a new table name.
- Change the currently selected objects in the layout or schematic view by right clicking a cell in the table, choosing **Selection > Toggle Auto Select Mode**, and clicking a cell to select or deselect.

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## Creating a Report Summary

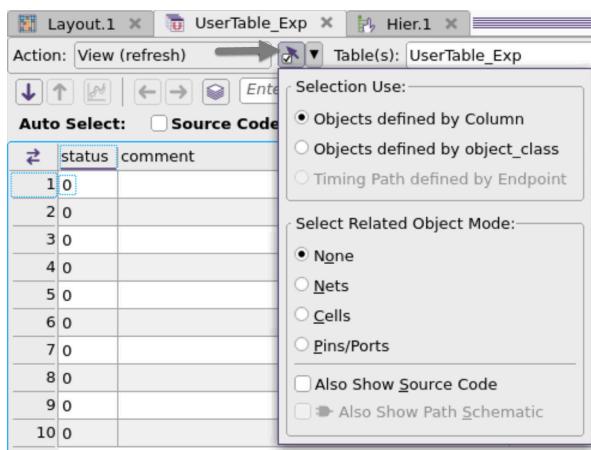
The summary report in a user table provides basic statistics on data in the table columns. To generate a summary report for a user table, choose **Report (summary)** from the Action box near the top of the user table form. The tool displays statistics (min, max,

average, and so on) for columns of numerical data in the table. A link to a histogram of numeric and categorical values is shown in the first row for each column.

Click any link in the first row to display the distribution report for that column. In the distribution report, click a column header to sort the table by the values in the column. Choose **Report (summary)** in the **Action** box to return to the summary report.

## Automatically Selecting Objects in a User Table

You can direct the tool to automatically select objects in a user table using the Auto Select Object drop down option.



By default, **Objects defined by Column** and **None** are selected, which means that for a given value in a column, the tool tries to select the object according to the type of object defined by its column.

If you select **Objects defined by object\_class**, the tool tries to find and select the object type given by the object class with the name given in the **full\_name** column.

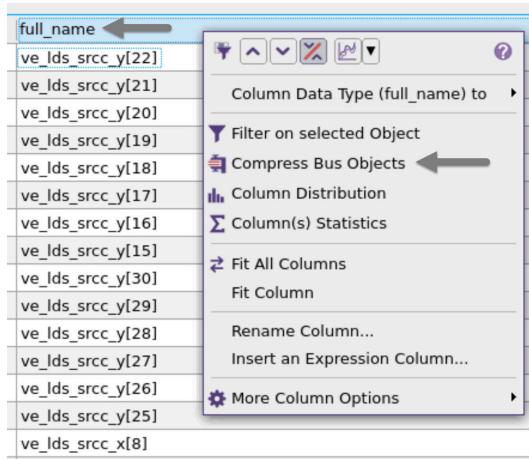
## Improved Bus Compression

You can compress bus signals that match the [\*] bus notation [#], \_#\_/, or \_#/ where # is some number.

This option is available

- As a column context menu option for any column that contains some sort of full name for nets, pins, cells and timing points
- In the hierarchy view and in the Child List view

## Chapter 4: Performing Basic Tasks Using User Tables



This action creates a user table that contains all the signals that match the bus notation bused together.

## Chapter 4: Performing Basic Tasks Using User Tables

The screenshot shows two tables in the Design Vision User Tables interface:

- UserTable\_Exp\_^full\_name\_bussed** (Top Table):
 

	status	comment	Show	Count	name	object_class	full_name
1	0		Table	41	cell	ctmi_*	
2	0		Table	36	cell	boundarycell_HDBULT06_CAPR14_*	
3	0		Table	27	cell	HFSBUF_2_*	
4	0		Table	23	port	ve_lds_srcc_y[*]	
5	0		Table	13	port	ve_lds_srcc_x[*]	

 Annotations for this table:
  - Remove filter to also see non bussed signals (points to the 'Show' column)
  - Show table of bussed signals (points to the 'Show' column)
  - Count of how many signals bussed (points to the 'Count' column)
  - Signals bussed (points to the last column)
- UserTable\_Exp\_^full\_name\_bus\_content** (Bottom Table):
 

	status	comment	name	object_class	full_name
1	0		ve_lds_srcc_x[8]	port	ve_lds_srcc_x[8]
2	0		ve_lds_srcc_x[7]	port	ve_lds_srcc_x[7]
3	0		ve_lds_srcc_x[6]	port	ve_lds_srcc_x[6]
4	0		ve_lds_srcc_x[9]	port	ve_lds_srcc_x[9]
5	0		ve_lds_srcc_x[3]	port	ve_lds_srcc_x[3]
6	0		ve_lds_srcc_x[4]	port	ve_lds_srcc_x[4]
7	0		ve_lds_srcc_x[2]	port	ve_lds_srcc_x[2]
8	0		ve_lds_srcc_x[1]	port	ve_lds_srcc_x[1]
9	0		ve_lds_srcc_x[10]	port	ve_lds_srcc_x[10]
10	0		ve_lds_srcc_x[0]	port	ve_lds_srcc_x[0]
11	0		ve_lds_srcc_x[11]	port	ve_lds_srcc_x[11]
12	0		ve_lds_srcc_x[12]	port	ve_lds_srcc_x[12]
13	0		ve_lds_srcc_x[5]	port	ve_lds_srcc_x[5]

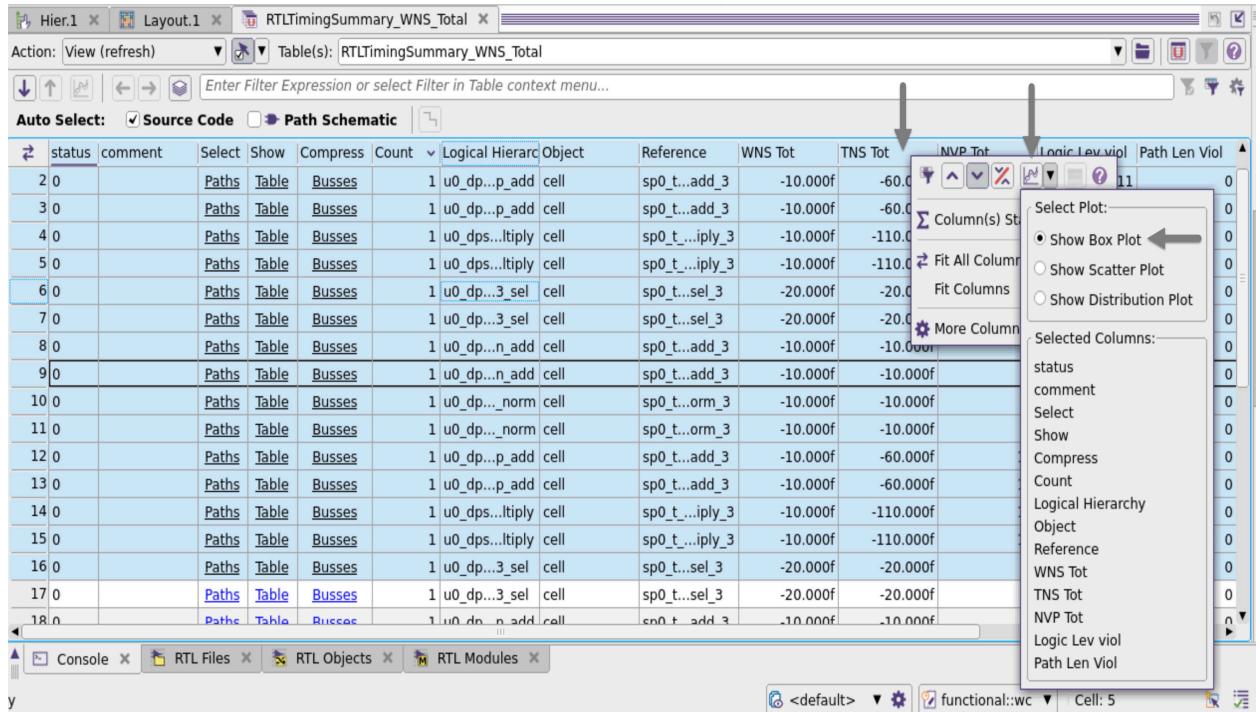
Click on one of the links under the Show column to bring up a new “child” table that contains the individual bussed signals. From this child table, if the signals are endpoints of timing paths, you might also have links to view a child table of timing path points in the table.

Use the up and down arrows at the top left to navigate back and forth between parent and child tables that were created in the drill down analysis.

## Viewing the Data as a Chart or Plot

To view the data in a user table as a chart or plot, use the column context menu button, **Select Plot**. The tool button is enabled only if the data in the selected columns contains numeric values.

You can select multiple columns and then create a plot based on the data in the selected columns of the user table.



The following figure shows the generated plot.

To filter the data by the values in the columns, mouse over the resultant plot and click **Filter**. You can use **Plot Control** to customize and control various options of the plot.

## Chapter 4: Performing Basic Tasks Using a Milkyway Database



To view the last viewed plot, click on the last viewed plot tool button. This button is enabled only if you previously viewed a plot for this table.

	status	comment	Paths	Table	Bus	Object	Reference	WNS Tot	TNS Tot	NVP Tot	Logic Lev viol	Path Len Viol
1 0			Paths	Table	Busses	1 BART_...esign block		-20.000f	-520.000f	119	119	0
2 0			Paths	Table	Busses	1 u0_dp...p_add cell	sp0_t...add_3	-10.000f	-60.000f	11	11	0
3 0			Paths	Table	Busses	1 u0_dp...p_add cell	sp0_t...add_3	-10.000f	-60.000f	11	11	0
4 0			Paths	Table	Busses	1 u0_dps...ltply cell	sp0_t...ltply_3	-10.000f	-110.000f	19	19	0
5 0			Paths	Table	Busses	1 u0_dps...ltply cell	sp0_t...ltply_3	-10.000f	-110.000f	19	19	0
6 0			Paths	Table	Busses	1 u0_dp...3_sel cell	sp0_t...sel_3	-20.000f	-20.000f	1	1	0

For more information see `*utable` commands man pages.

## Using a Milkyway Database

Design Compiler topographical technology provides the capability to accurately predict post-layout timing, area, and power during RTL synthesis without the need for wire load model-based timing approximations. It uses Synopsys' placement and optimization technologies to drive accurate timing prediction within synthesis, ensuring better correlation to the final physical design. This new technology is a part of the DC Ultra

feature set and is available only by using the `compile_ultra` command in topographical mode.

To use the Design Compiler topographical features in the Design Vision tool, you must run the tool in topographical mode. In this mode, the command-line prompt appears as `design_vision-topo>` on the console and in the shell. For more information about starting the tool, see [Starting the Tool on page 32](#).

Topographical technology leverages the Synopsys physical implementation solution to derive the “virtual layout” of the design so that the tool can accurately predict and use real net capacitances instead of wire load model-based statistical net approximations. If wire load models are present, they are ignored. In addition, the tool updates capacitances as synthesis progresses by adjusting placement-derived net delays based on an updated “virtual layout” at multiple points during synthesis.

This approach eliminates the need for over constraining the design or using optimistic wire load models in synthesis. The accurate prediction of net capacitances drives the tool to generate a netlist that is optimized for all design goals including area, timing, test, and power. It also results in a better starting point for physical implementation.

Topographical technology supports all synthesis flows, including

- Test-ready compile flow (basic scan and DFT MAX adaptive scan)
- Clock-gating flow
- Register retiming

When you use the `Compile Ultra` command in topographical mode, the Design Compiler topographical features are automatically used. All `compile_ultra` command options are supported. In addition, the `Compile Design` command (Design menu), the `Report Wire Load` command (Timing menu), and the `Wire Load` command (Attributes > Operating Environment menu) are not available in topographical mode.

For more information about using Design Compiler topographical technology, see the *Design Compiler User Guide*.

For information about working with Milkyway design libraries in topographical mode, see the following sections:

- [Using Design Vision Tool in Topographical Mode](#)
- [Creating a Milkyway Design Library](#)
- [Setting the Milkyway Reference Libraries](#)
- [Opening or Closing a Milkyway Design Library](#)

- [Copying a Milkyway Design Library](#)
- [Setting the TLUPlus Extraction Files](#)

#### See Also

- [Optimizing Critical Delays](#)

---

## Using Design Vision Tool in Topographical Mode

DC Ultra topographical technology provides the capability to accurately predict post-layout timing, area, and power during RTL synthesis without the need for wireload model-based timing approximations. It uses Synopsys placement and optimization technologies to drive accurate timing prediction within synthesis, ensuring better correlation to the final physical design. This new technology is built in as part of the DC Ultra feature set and is available only by using the `compile_ultra` command.

To use the DC Ultra topographical features in Design Vision tool, you must run Design Vision tool in topographical mode. In this mode, the command-line prompt appears as `design_vision-topo` in the console and the shell. For more details about starting Design Vision, see [Starting the Tool](#).

#### Note:

Topographical mode supports only a subset of `dc_shell` commands, command options, and variables. For information, see the *Design Compiler User Guide*.

You can query the mode by running the `shell_is_in_topographical_mode` command. The command returns 1 if Design Vision tool is running in topographical mode; otherwise it returns 0. Topographical mode requires a DC Ultra license and a DesignWare license. A Milkyway-Interface license is also necessary if the Milkyway flow is used.

Topographical technology leverages the Synopsys physical implementation solution to drive an accurate timing prediction within the RTL synthesis engine. Timing and synthesis are based on a virtual layout analysis. This ensures excellent correlation with the physical design.

When you start Design Vision tool in topographical mode,

- Wire load models are not needed (they are ignored if present). Topographical technology predicts and uses real net capacitances. Capacitances are updated as synthesis progresses.
- If you run the `compile_ultra` command (on the command line or by choosing Design > Compile Ultra), the DC Ultra topographical features are automatically used. All

`compile_ultra` command options are supported. For more details, see [Optimizing Critical Delays](#).

- The Compile Design command (Design menu), the Report Wire Load command (Timing menu), and the Wire Load command (Attributes > Operating Environment menu) are not available.

DC Ultra topographical technology supports multivoltage designs, supports all synthesis flows (including test-ready compile, clock gating, and register retiming), and it is shared with IC Compiler tool. The following inputs are required to run topographical synthesis:

- RTL design or an existing gate-level netlist
- Timing and optimization constraints

**Note:**

If you specify wire load models, the tool ignores them.

- Liberty format logic library (.lib and .db)
- Physical library
  - Milkyway format (the default)
  - .pdb library format

You can save the synthesized design in .ddc format, Milkyway format, or as a Verilog netlist.

## Previewing Dialog Box Commands

Some Design Vision dialog boxes support a preview mechanism that you can use to view the commands without running them. You can view the command equivalents for various dialog box options, or combinations of options, or generate a `dc_shell` command that you want to copy into a script. When you enable the preview mechanism, it remains on for all dialog boxes that support the feature until you disable it.

When you click OK or Apply in a dialog box that supports the preview mechanism while the mechanism is enabled, the `dc_shell` command equivalent appears in the console history log preceded by a pound sign (#), but Design Vision tool does not execute the command and it does not appear in the console log view or the shell transcript.

To enable or disable the dialog box command preview mechanism,

- Click the  button in the bottom right corner of a dialog box, and choose `Preview command only` or `Ctrl+P`.

A check mark next to `Preview command only` on the menu indicates that the preview mechanism is enabled.

---

## Creating a Milkyway Design Library

You need a Milkyway design library to save a design in Milkyway format for use in other Synopsys Galaxy platform tools, such as the IC Compiler tool. You can use a single Milkyway design library across the entire Galaxy flow.

The Milkyway tool stores design data in the Milkyway design library and physical library data in the Milkyway reference library. Before creating a Milkyway design library, you must prepare the design and reference libraries.

- The Milkyway directory structure used to store design data (the unqualified, mapped netlist and constraints) is referred to as the Milkyway design library. You can specify a design library for the current session by setting the `mw_design_library` variable to the root directory path.
- The Milkyway directory structure used to store physical library data is referred to as the Milkyway reference library. Reference libraries contain standard cells, macro cells, and pad cells. The Design Vision tool uses the FRAM view of the reference libraries as the default physical model for your design. You can specify a reference library for the current session by setting the `mw_reference_library` variable to the root directory path.

In topographical mode, you create a Milkyway design library when you need to save a design in Milkyway format for use with other Synopsys Galaxy platform tools, such as IC Compiler. When you use a Milkyway design library, you do not need to use an intermediate netlist file exchange format such as Verilog or VHDL to communicate with other Synopsys Galaxy platform tools.

Before you can create a Milkyway design library in Design Vision tool, you must prepare the design and reference libraries. The Milkyway tool stores design data in the Milkyway design library and physical library data in the Milkyway reference library.

- The Milkyway directory structure used to store design data (the unqualified, mapped netlist and constraints) is referred to as the Milkyway design library. You can specify a design library for the current session by setting the `mw_design_library` variable to the root directory path.
- The Milkyway directory structure used to store physical library data is referred to as the Milkyway reference library. Reference libraries contain standard cells, macro cells, and pad cells. You can specify a reference library for the current session by setting the `mw_reference_library` variable to the root directory path. For information on creating reference libraries, see the *Milkyway documentation*.

To create a Milkyway design library, you must specify the design library name and directory path, the technology file name, and the reference library file names. Design Vision tool uses the FRAM view of the reference libraries as the default physical model for your design. You can create a Milkyway design library at any time when a design library is

not open in Design Vision tool. If a design library is already open, you must close it before you can create a design library. For details, see [Opening or Closing a Milkyway Design Library](#).

When you create a Milkyway design library, the Design Vision tool sets the reference libraries for the design. For more information about using Milkyway design libraries in topographical mode, see the *Design Compiler User Guide*.

You can specify the Milkyway reference library files directly or by using a reference control file. For information about using these options, see the *Creating a Milkyway Design Library* topic in the *Design Compiler User Guide*.

Using the Create Library dialog box is equivalent to using the `create_mw_lib` command.

1. Choose File > Create MW Library.

The Create Library dialog box appears. If the `Create MW Library` command is not available, check to see if a Milkyway design library is already open in Design Vision tool. You cannot create a library when another library is open.

2. Specify the design library information as follows:

- Enter the path to the library directory in the New library path text box, or click the  button and select the library directory in the path browser.
- Enter the name of the new library in the New library name text box.
- Enter the technology file name in the Technology file text box, or click the  button and select the file in the file browser.

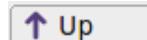
3. Select a reference library option, and specify the reference libraries as needed.

You can specify the Milkyway reference library files directly or by using a reference control file.

- To specify the Milkyway reference library files directly, select the Input reference libraries option and add the files to the Files list. You can add or remove files in the Files list, and you can reorder the files by moving them up or down in the list.

To add a file to the list, click the Add button and select the file in the file browser. To remove a file from the list, select the file name and click the Delete button.

The order in the list implies priority for reference conflict resolution. If more than one reference library has a cell with the same name, the first reference library has precedence. To move a file up in the list, select the file name and click the



button. To move a file down in the list, select the file name and click the



button.

- To use a reference control file to specify the Milkyway reference library files, select the Reference control file option, and either enter the file name or click the  button and select the file in the file browser.
  - If you do not need to specify either the Milkyway reference library files or a reference control file, select None.
4. Set other options as needed.
    - To specify a character that separates hierarchical names in the libraries, type the character in the Hierarchical separator text box.
    - To specify a bus naming style, type the style in the Bus naming style text box.
  5. (Optional) To open the library immediately after creating it, select the Open library option.

**Note:**

For maximum re-usability of scripts, do not use this option. Instead, open the library separately by choosing File > Open Library (for details, see [Opening or Closing a Milkyway Design Library](#)).

6. Click OK.

Using the Create Library dialog box is equivalent to using the `create_mw_lib` command.

**Note:**

You can preview the equivalent Tcl command for the current option settings in this dialog box, without executing the command, by enabling the command preview mechanism. For details, see [Previewing Dialog Box Commands](#).

## Setting the Milkyway Reference Libraries

The Milkyway directory structure used to store physical library data is referred to as a Milkyway reference library. Reference libraries contain standard cells, macro cells, and pad cells. For information on creating reference libraries, see the *Milkyway documentation*.

In topographical mode, you can set the Milkyway reference libraries used with your design library at any time when a design library is not open in Design Vision tool. If a design library is already open, you must close it before you can set reference libraries. For details, see [Opening or Closing a Milkyway Design Library](#).

To set the Milkyway reference libraries,

1. Choose File > Set MW Library Reference.

The Set Library Reference dialog box appears. If the Set MW Library Reference command is not available, check to see if a Milkyway design library is already open in Design Vision. You cannot change the reference libraries when a design library is open.

2. Type the reference library name in the Library name text box, or click the  button and select the library directory in the path browser.
3. Select a reference library option, and specify the reference libraries as needed.

You can specify the Milkyway reference library files directly or by using a reference control file.

- To specify the Milkyway reference library files directly, select the Input reference libraries option and add the files to the Files list. You can add or remove files in the Files list, and you can reorder the files by moving them up or down in the list.

To add a file to the list, click the Add button and select the file in the file browser. To remove a file from the list, select the file name and click the Delete button

The order in the list implies priority for reference conflict resolution. If more than one reference library has a cell with the same name, the first reference library has precedence. To move a file up in the list, select the file name and click the  button. To move a file down in the list, select the file name and click the  button.

- To use a reference control file to specify the Milkyway reference library files, select the Reference control file option, and either enter the file name or click the  button and select the file in the file browser.

4. Click OK.

Using the Set Library Reference dialog box is equivalent to using the `set_mw_lib_reference` command.

**Note:**

You can preview the equivalent Tcl command for the current option settings in this dialog box, without executing the command, by enabling the command preview mechanism. For details, see [Previewing Dialog Box Commands](#).

## Opening or Closing a Milkyway Design Library

After you create a Milkyway design library, you must open it before you can read in the design. You cannot have more than one library open at the same time. If another library is already open, you must close it before opening a different library.

To open a Milkyway design library,

1. Choose File > Open MW Library.

The Open Library dialog box appears. If the Open MW Library command is not available, make sure that another Milkyway design library is not already open in Design Vision tool.

2. Type the library name in the Library name text box, or click the  button and select the library directory in the path browser.
3. (Optional) Select a permissions option.
  - To open the design library with read-only permission, click the Open library as read-only option.
  - To open the reference libraries with read and write permissions, click the Open reference library for writing option.

These options are mutually exclusive. By default, Design Vision tool opens the design library for reading and writing and the reference libraries for reading only.

4. Click OK.

Using the Open Library dialog box is equivalent to using the `open_mw_lib` command.

To close a Milkyway design library,

- ▶ Choose File > Close MW Library.

Using the Close MW Library command is equivalent to using the `close_mw_lib` command.

**Note:**

You can preview the equivalent Tcl command for the current option settings in this dialog box, without executing the command, by enabling the command preview mechanism. For details, see [Previewing Dialog Box Commands](#).

## Copying a Milkyway Design Library

In topographical mode, you can make a copy of a Milkyway design library and save it in a different location.

To copy a Milkyway design library,

1. Choose File > Copy MW Library.

The Copy Library dialog box appears.

2. Type the name of the library you want to copy in the From library text box, or click the  button and select the library directory in the path browser.
3. Type the path to the directory where you want to save the copied library in the To library text box.
4. Click OK.

Using the Copy Library dialog box is equivalent to using the `copy_mw_lib` command.

**Note:**

You can preview the equivalent Tcl command for the current option settings in this dialog box, without executing the command, by enabling the command preview mechanism. For details, see [Previewing Dialog Box Commands](#).

---

## Setting the TLUPlus Extraction Files

TLUPlus is a binary table format in the Milkyway library for RC coefficients. You do not need to specify TLUPlus files if resistance and capacitance models are present in your vendor technology physical library. These files provide more accurate capacitance and resistance data, thereby improving correlation with back-end results.

To use TLUPlus, you must specify the maximum TLUPlus model files. You can also specify minimum TLUPlus model files and a map file that maps layer names between the Milkyway technology file and the process Interconnect Technology Format (ITF) file.

Design Vision tool stores the names and locations of these files in Milkyway, but it does not store the TLUPlus information found in these files. For each Design Vision tool session you work on your design, you must specify the TLUPlus files that you need to use during the session.

To select the TLUPlus files,

1. Choose File > Set TLU+.

The Set TLU+ dialog box appears.

2. Enter the maximum TLUPlus model file names in the Maximum TLU+ file text box, or click the  button and select the files in the file browser.

3. (Optional) Enter the minimum TLUPlus model file names in the Minimum TLU+ file text box, or click the  button and select the files in the file browser.
4. (Optional) Enter the ITF to Milkyway layer map file name in the Layer name mapping file between technology library and ITF file text box, or click the  button and select the file in the file browser.
5. Click OK.

Using the Set TLU+ dialog box is equivalent to using the `set_tlu_plus_files` command.

**Note:**

You can preview the equivalent Tcl command for the current option settings in this dialog box, without executing the command, by enabling the command preview mechanism. For details, see [Previewing Dialog Box Commands](#).

Using the Set TLU+ dialog box is equivalent to using the `set_tlu_plus_files` command. The Design Vision tool stores the names and locations of the TLUPlus files in Milkyway, but it does not store the TLUPlus information found in these files. For each Design Vision tool session, you must specify the TLUPlus files that you need to use during the session.

## Working With Designs in Memory

The Design Vision tool reads designs into memory from design files. Many designs can be in memory at any time. After reading in a design, you can change it in numerous ways, such as grouping or ungrouping its subdesigns or changing subdesign references.

To learn how to work with designs in memory, see the following topics:

- [Preparing Design Files for Synthesis](#)
- [Setting Variables](#)
- [Reading Designs](#)
- [Analyze Files](#)
- [Elaborating a Design](#)
- [Viewing the List of Designs in Memory](#)
- [Setting the Current Design](#)
- [Importing the Design Timing Information](#)
- [Linking Designs](#)
- [Removing Attributes and Constraints](#)

- [Removing Designs From Memory](#)
- [Saving Designs](#)

#### See Also

- [Using Logic Synthesis Tools](#)
- [Using a Milkyway Database](#)

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## Preparing Design Files for Synthesis

You generally use a hardware description language (HDL) such as Verilog or VHDL to create the input design files for Design Compiler. You should write the design descriptions carefully to achieve the best possible synthesis results.

**Note:**

Even though this is the first step in the synthesis process, it is not a Design Compiler step. You do not use Design Compiler tools to create HDL files.

When you write HDL code, consider design data management, design partitioning, and your HDL coding style. Partitioning and coding style directly affect the synthesis and optimization processes.

For more details, see the information about preparing design files for synthesis in the *Design Compiler User Guide*.

---

## Setting Variables

You use variables to preset the defaults for some Design Vision tool options that appear in menus or dialog boxes.

- Before you start a Design Vision tool session, you can set variables in your .synopsys\_dc.setup file.
- During a Design Vision tool session, you can set or change variables in the Application Setup dialog box. These variables apply only to the current session.

To view variable names and values,

1. Choose File > Setup.  
The Application Variables dialog box appears.
2. Select the Variables.
3. If you want to display only variables with certain characters in their names, enter a name pattern in the Filter by name text box and press Enter.

You can find information on Design Vision tool and Design Compiler tool variables by viewing man pages in the man page viewer.

### See Also

- [Specifying Logic Libraries](#)
- [The Design Vision Setup Files](#)
- [Using Script Files](#)

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## Reading Designs

To begin working on your design, read the design from disk into the tool's active memory. This is where all changes in the design take place before you save the design by writing it back to disk.

When you read in a netlist or precompiled design file, it is loaded into memory in .ddc format. You can read a file with any supported format. However, only the .ddc, EDIF, equation, PLA, and state table formats do not require a special license key. For a list of supported formats, see [Supported Formats](#).

To read in a design,

1. Click the  button on the Standard toolbar or choose File > Read.  
The Read Designs dialog box appears.
2. (Optional) If you want to change the types of file names that appear in the dialog box, select an option in the Files of type drop-down list.
  - To display only files with supported Synopsis database file suffixes, select the Database Files option.  
The suffix list for the Database Files option is set by the view\_read\_file\_suffix variable. For details about viewing variables or changing their values, see [Setting Variables](#).
    - To display all files in a directory, select the All Files option.
3. Navigate to the directory that contains the file you want to read (or enter the path name in the File name text box).
4. Select the name of the file you want to open (or enter the file name in the File name text box).
5. (Optional) Select a file format in the Format list. The default is Auto.

By default, Design Vision tool automatically determines how to read the files based on the file name suffix. If you select a Format option other than Auto, Design Vision tool reads the file based on the selected format regardless of the file name suffix.

If you select or enter multiple file names, the files must all have the same format, and you must select the format in the Format drop-down list.

**Note:**

Your site license determines which file formats are available in the Format list. For descriptions of the formats, see the *Design Compiler User Guide*.

6. Click Open.

The file name you selected appears in the logic hierarchy view.

The File menu contains the commands for reading in a design:

- Analyze and Elaborate

Use Analyze and Elaborate to read HDL designs and convert them to .ddc format. These commands open dialog boxes in which you can set options that are equivalent to the `analyze` and `elaborate` command-line options.

- Read

Use Read (`read_file` is the command-line equivalent) to read designs that are already in .ddc format. This command opens a dialog box in which you can set options that are equivalent to the `read_file` command-line options.

## Read Command

If you use the Read command to read in HDL files, the Analyze and Elaborate read functions are combined. However, Read does not perform certain design checks that Analyze and Elaborate perform.

The GUI can access all of the files supported by the Design Compiler tool. The following table shows the supported design file input formats. All netlist formats except .db, equation, PLA, state table, Verilog, and VHDL require special license keys.

Table 3     Supported Design File Input Formats

Format	Description
.ddc	Synopsys internal database format (recommended)
.db	Synopsys internal database format
Verilog	IEEE Standard Verilog (see the HDL Compiler documentation)

**Table 3      Supported Design File Input Formats (Continued)**

Format	Description
VHDL	IEEE Standard VHDL (see the HDL Compiler documentation)
SystemVerilog	IEEE Standard SystemVerilog (see the HDL Compiler documentation)
equation	Synopsis equation format
pla	Berkeley (Espresso) PLA format

### See Also

- [Linking Designs](#)
- [Viewing the List of Designs in Memory](#)
- [Setting the Current Design](#)
- [Removing Designs From Memory](#)

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## Analyze Files

The Analyze command checks the HDL designs for proper syntax and synthesizable logic, translates the design files into an intermediate format, and stores the intermediate files in the directory you specify. The Elaborate command first checks the intermediate format files before building a .ddc design. During this process, Elaborate determines whether it has the necessary synthetic operators to replace the HDL operators, and it also determines correct bus size.

To analyze files,

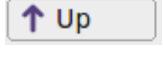
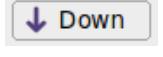
1. Choose File > Analyze

The Analyze Designs dialog box appears.

2. When you click the  button in a dialog box, the Specify File names in analysis order dialog box appears. You can use this dialog box to select the names of one or more design objects.
3. To select the files you want to analyze, click Add to open the file browser, select one or more files, and click  button.

The file names appear in the File names in analysis order list.

4. If you need to reorganize files in the list, select one or more file names and

- Click the  Up button to move them up in the list
- Click the  Down button to move them down in the list

Repeat this step until the files are listed in the order that you want them to be analyzed.

If you need to remove a file from the list, select the file name and click the Delete button.

5. (Optional) Select a library from the Library list. (The WORK library is selected by default.)
6. (Optional) Select a file format in the Format list. The choices are Auto (the default), VERILOG, SVERILOG, and VHDL.

By default, Design Vision tool automatically determines how to read the files based on the suffix of the file names. If you select a Format option other than Auto, Design Vision tool reads the file based on the selected format regardless of the file name suffix.

7. If you need to use a WORK library that does not already exist, select the Create new library if it does not exist option.
8. Click OK.

### See Also

- [Linking Designs](#)
- [Viewing the List of Designs in Memory](#)
- [Setting the Current Design](#)
- [Removing Designs From Memory](#)

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## Elaborating a Design

You elaborate a design to create a technology-independent design from the intermediate format files created by the Analyze command (choose File > Analyze).

Elaboration replaces HDL arithmetic operators with DesignWare components and determines the correct bus size. You must analyze the HDL files before you can elaborate the design (for details, see [Analyze Files](#)).

To elaborate a design,

1. Choose File > Elaborate.

The Elaborate Designs dialog box appears.

2. Select a library name in the Library drop-down list.

The designs in the library automatically appear in the Design list.

3. Select a design name in the Design drop-down list.

If there are any parameters in the design, their names and values automatically appear in the Parameters table. (You can edit this table to change the default parameter specification.)

4. If you want to prevent the compiler from reanalyzing out-of-date libraries, make sure the Reanalyze out-of-date libraries option is deselected.
5. If you are using the Power Compiler tools and need to enable automatic clock gating of registers, select the Gate clock option.

**Note:**

You must run the `set_clock_gating_style` command before you elaborate a design with this option selected. For more details about clock gating, see the *Power Compiler Reference Manual*.

6. Click OK.

## See Also

- [Linking Designs](#)
- [Viewing the List of Designs in Memory](#)
- [Setting the Current Design](#)
- [Removing Designs From Memory](#)

---

## Viewing the List of Designs in Memory

You can generate a list of the designs loaded in memory and display information about them in a list view. The list includes the name, the area, the design directory path, the DesignWare implementation, and the states of the structure, flatten, and `dont_touch` attributes for each the design.

To open the design list view, choose List > Designs View.

You can select some or all of the designs in the list by clicking or dragging the pointer across their names in the list view. You can also use Shift-click or Control-click to select multiple designs. In addition, you can

- Sort the information alphabetically by clicking a column heading. Click the heading again to reverse the sort
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over it to display the information in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

You can select a design and make it the current design.

To change the current design,

1. Select a design in the design list view.
2. Click right and choose Set Current Design.

You can filter the design list, limiting it to designs based on a character string or regular expression that you define, by using the Filter List dialog box. For more information, see [Filtering Object Lists](#).

## See Also

- [Reading Designs](#)
- [Setting the Current Design](#)
- [Linking Designs](#)
- [Removing Designs From Memory](#)

---

## Setting the Current Design

When you start a Design Vision tool session and read a design, the current design is automatically set to the top-level design. Some commands require you to set the current design to a subdesign before you issue them (the man pages provide such information).

To set the current design,

1. Click the drop-down list on the Design List toolbar to display the design names.
2. Select a design name.

Alternatively, you can open a design list view (by choosing List > Designs View), select a design name in the list, right-click, and choose Set Current Design. The command-line equivalent is `set current_design`.

## See Also

- [Reading Designs](#)
- [Viewing the List of Designs in Memory](#)
- [Linking Designs](#)
- [Removing Designs From Memory](#)

---

## Importing the Design Timing Information

You can load the leaf cell and net timing information saved from a subdesign and use it to annotate the current design. The current design must be a fully mapped netlist.

To import design cell and net timing information,

1. Choose File > Import > Design Timing.

The Import Design Timing Information dialog box appears.

2. Select a design name in the Cell path drop-down list.

3. Enter the path and file name in the Timing file name text box.

or

Click Browse, select or enter the file name in the file browser, and then click Open.

4. Select a delay type option in the Load delay type drop-down list. The default is cell.

◦ Select cell if the load delays in the timing file are included in the cell delays.

◦ Select net if the load delays in the timing file are included in the net delays.

5. Set any other options you need to use.

◦ If a value from the SDF delay triplet is annotated for maximum delay analysis, you can select the Specify the SDF triplet value for maximum delay option and select a value option in the Maximum delay type drop-down list.

◦ If a value from the SDF delay triplet is annotated for minimum delay analysis, you can select the Specify the SDF triplet value for minimum delay option and select a value option in the Minimum delay type drop-down list.

◦ If you want to apply only those delay values from the timing that are worse than the current delay values, select the Annotate only with delays worse than the annotated ones option.

6. Click OK or Apply.

## See Also

- [Reading Designs](#)

---

## Linking Designs

For a design to be complete, it must be connected to all of the designs and library components that it references. For a subdesign to be complete, there must be a reference that links the subdesign or component to the link libraries. This process is called linking the design or resolving references.

When you link a design, the tool locates and connects all of the designs and library components referenced in the current design and connects them to the current design.

**Note:**

If you read in a linked design from a .ddc file, you do not need to relink the design.

Designs can be linked either automatically or manually.

Automatic linking occurs when you optimize the design, open a schematic view of the design, group cells into subdesigns, check design consistency, or generate reports. During automatic linking, the tool links only unlinked components and subdesigns and does not remove existing links.

When you manually link a design, the tool removes existing links before starting the link process.

To manually link the current design,

1. Choose File > Link Design.  
The Link Design dialog box appears.
2. Specify the design file search paths.

You can either enter the paths in the Search path text box (use blank spaces to separate individual paths) or click the Browse button and select directories in the file browser.

3. Enter the library paths and file names in the Link library text box.
4. If you want the compiler to search for referenced subdesigns in memory before searching files in the specified search path directories, select the Search memory first option.
5. Click OK.

The GUI displays the names of the linked designs and libraries in the console log view.

### See Also

- [Viewing the List of Designs in Memory](#)
- [Setting the Current Design](#)

---

## Removing Attributes and Constraints

Attributes and constraints describe logical, electrical, physical, and other properties of objects in a design. You can remove all the attributes and constraints from the current design.

To remove all attributes and constraints from a design,

1. Make sure the design is set as the current design.
2. Choose Design > Reset Current Design.

Design Vision tool displays a message box asking if you want to remove all the constraints and attributes.

3. Click OK if you want to remove the constraints and attributes, or click Cancel if you do not want to remove the constraints and attributes.

**Note:**

When you remove the timing constraints from a design, Design Vision tool closes any timing views (such as histograms or schematics) that you have opened.

### See Also

- [Removing Designs From Memory](#)
- [Saving Designs](#)

---

## Removing Designs From Memory

You can remove designs from memory without exiting the tool. You can either remove all the designs or one or more individual designs.

To remove all designs from memory,

- Choose File > Remove All Designs.

To remove an individual design,

1. Select the design name in the design list view.
2. Click right and choose Remove Design.

For information about opening a design list view, see [Viewing the List of Designs in Memory on page 316](#).

After removing designs, you can load different designs or reload the same designs by using either the Read command or the Analyze and Elaborate commands on the File menu. For information about these commands, see [Reading Designs on page 312](#).

#### See Also

- [Setting the Current Design](#)
- [Linking Designs](#)
- [Saving Designs](#)

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## Saving Designs

You can save (write to disk) the designs and subdesigns of the design hierarchy at any time, using different names or formats. After modifying a design, you should save it manually. the Design Vision tool does not automatically save designs before it exits.

For information about saving designs, see the following topics:

- [Supported Design Output Formats](#)
- [Writing a Design Netlist](#)
- [Writing to a Milkyway Database](#)
- [Saving a Design Setup](#)

#### See Also

- [Reading Designs](#)
- [Viewing the List of Designs in Memory](#)
- [Removing Designs From Memory](#)

## Supported Design Output Formats

The tool stores design data in an internal database format. It supports two design database formats: .ddc and Milkyway.

- .ddc format

The .ddc format is a single-file, binary format. The .ddc format stores design data in an efficient manner than the .db format, enabling increased capacity. In addition, reading and writing files in .ddc format is faster than reading and writing files in .db format.

The .ddc format stores only logical design information.

- Milkyway format

The Milkyway format allows you to write a Milkyway database for use with other Synopsys Galaxy tools, such as the IC Compiler tool. The Milkyway format stores both logical and physical design information, but it requires a mapped design.

The Milkyway format is available only when you start the Design Vision tool in topographical mode. Use the `write_milkyway` command to save netlist and physical design data in a Milkyway design library. You can use a single Milkyway library across the entire Galaxy flow. For more information, see the *Design Compiler User Guide*.

**Note:**

The Design Vision tool does not support the `read_milkyway` command.

The GUI can access all of the design file formats supported by the Design Compiler tool. [Table 4](#) shows the supported design file output formats.

*Table 4      Supported Design File Output Formats*

Format	Description
.ddc	Synopsys internal database format
Verilog	IEEE Standard Verilog (see the HDL Compiler documentation)
svsim	SystemVerilog netlist wrapper. <b>Note:</b> Specifying this format causes the tool to write out only the netlist wrapper, not the gate-level design under test (DUT). To write out the gate-level DUT, use the <code>write_file -format verilog</code> command. For more information, see the <i>HDL Compiler for SystemVerilog User Guide</i> .
VHDL	IEEE Standard VHDL (see the HDL Compiler documentation)
Milkyway	Format for writing a Milkyway database

## See Also

- [Writing a Design Netlist](#)
- [Writing to a Milkyway Database](#)

## Writing a Design Netlist

The Design Vision tool does not automatically save designs before exiting. When you make changes to a design, save it in a file before you exit the tool.

To save the current design and its subdesigns,

- ▶ Click the  button on the File toolbar or choose File > Save.

By default, the files are saved in .ddc format files named *design\_name.ddc*, where *design\_name* is the name of the design. You can save a design in any supported design file output format.

To save the current design and all of its subdesigns in a single file or with a different file name or file format,

1. Choose File > Save As.

The Save Design As dialog box appears.

2. (Optional) If you want to change the types of file names that appear in the dialog box, select an option in the File type drop-down list.

- To display only files with supported Synopsys database file suffixes, select the Database Files option.

The suffix list for the Database Files option is set by the `view_read_file_suffix` variable. For details about viewing variables or changing their values, see [Setting Variables](#).

- To display all files in a directory, select the All Files option.

3. Navigate to the directory where you want to save the design, or enter the path name in the File name text box.

4. Select a file name or enter a file name in the File name box.

If you select or enter the name of an existing file, Design Vision tool overwrites the file.

5. (Optional) Select a file format in the Format list.

By default, the tool automatically selects the format based on the file name suffix. If the file name you specify does not contain a suffix or the suffix does not indicate the appropriate format, you must select a format option.

6. Navigate to the directory where you want to save the design, or enter the path name in the File name text box.

7. Select a file name, or enter a file name in the File name text box.

If you select or enter the name of an existing file, the tool overwrites the file.

8. (Optional) If you want to save all the designs in the hierarchy instead of just the current design, make sure the Save all designs in hierarchy option is selected.

9. Click OK.

### See Also

- [Supported Design Output Formats](#)
- [Writing to a Milkyway Database](#)

## Writing to a Milkyway Database

The Milkyway format allows you to write a Milkyway database for use with other Synopsys Galaxy tools, such as the IC Compiler tool. The Milkyway format stores both logic design and physical design information, but it requires a mapped design.

The Milkyway format is available only when you start the tool in topographical mode. Use the `write_milkyway` command to save netlist and physical design data in a Milkyway design library. You can use a single Milkyway library across the entire Galaxy flow. For more information, see the *Design Compiler User Guide*.

### Note:

The tool does not support the `read_milkyway` command.

## Saving a Design Setup

You can save the design attributes for the current design in a Tcl script file, then use the script during a future Design Vision tool session to re-create the design attributes for your design.

To save a design setup,

1. Choose File > Save Info > Design Setup.

The Save Design Setup dialog box appears.

2. Navigate to the directory where you want to save the design setup.

3. Select a file name.

or

Enter a file name in the File name text box.

If you select or enter the name of an existing file, the compiler overwrites the file.

4. Click OK, or click Apply and to save the design setup in a different file repeat step 2 and 3.

### See Also

- [Saving Designs](#)

---

## Defining the Design Environment

The Design Compiler tool requires that you model the environment of the design to be synthesized. This model comprises the external operating conditions (manufacturing process, temperature, and voltage), loads, drive characteristics, fanout loads, and wire loads. It directly influences design synthesis and optimization results.

Defining the design environment can involve using a large number of commands. Many designers find it convenient to define the design environment by using the default target library settings and by running scripts to define differences or additions. To define the design environment by using Design Vision menus, choose commands on the Operating Environment submenu under the Attributes menu.

Before you can optimize a design, you must define the environment in which you expect the design to operate. You define the environment by selecting operating conditions, wire load models, and system interface characteristics. You can also select timing ranges to model statistical variations in the nominal operating conditions.

- Operating conditions include temperature, voltage, and process variations.
- Timing ranges are scaling factors for best-case and worst-case timing conditions.
- Wire load models estimate the effect of wire length on design performance.
- System interface characteristics include input drives, input and output loads, and fanout loads.

The environment model directly affects design synthesis results. In the compiler, the model is defined by a set of attributes and constraints that you assign to the design.

In most technologies, variations in operating temperature, supply voltage, and the manufacturing process can strongly affect circuit performance (speed). Most technology libraries have predefined sets of operating conditions, timing ranges, and wire load models. The compiler uses this library information when it performs a static delay analysis. This analysis helps you determine whether your design meets performance requirements.

For details about selecting operating conditions, timing ranges, and wire load models, see

- [Selecting Operating Conditions](#)
- [Selecting a Wire Load Model](#)
- [Selecting Timing Ranges](#)

The system interface models the design's interaction with the external system. For details about defining the system interface, see

- [Defining Drive Characteristics for Input Ports](#)
- [Setting Capacitive Loads on Input Ports](#)
- [Setting Capacitive and Fanout Loads on Output Ports](#)

For more information, see the *Defining the Design Environment* topic in the *Design Compiler User Guide*.

---

## Selecting Operating Conditions

Operating conditions define temperature, voltage, and manufacturing process conditions that affect design timing. Most technology libraries contain predefined sets of operating conditions.

You can view a design report to see the operating conditions defined for the current design. For details, see [Reporting Design Information](#).

To select operating conditions for the current design,

1. Choose Attributes > Operating Environment > Operating Conditions.  
The Operating Conditions dialog box appears.
2. Set the maximum operating conditions by selecting a Library and a Condition option under the Maximum operating condition section.
3. To set minimum operating conditions that are different from the maximum conditions, select the Min/max case option and select a Library and a Condition option under Minimum operating condition section.
4. Click OK or Apply.

### Note:

You can use the `set_operating_conditions` command to specify explicit operating conditions that override the default library conditions.

### See Also

- [Operating Conditions \(Attributes > Operating Environment\)](#)
- [Selecting Timing Ranges](#)
- [Selecting a Wire Load Model](#)

---

## Selecting a Wire Load Model

Wire load models attempt to predict the effect of wire length and fanout on the resistance, capacitance, and area of nets. These values are used during optimization to calculate wire delays and circuit speeds. Most technology libraries contain predefined wire load models based on the number of fanout pins on a net.

You can view a design report or a timing report to see the wire load models defined for the current design. For details, see [Reporting Design Information](#) and [Reporting Worst Path Timing](#).

If you need to remove the wire load model, use the `remove_wire_load_model` command with no model name.

To set the wire load model on the current design,

1. Choose Attributes > Operating Environment > Wire Load.  
The Wire Load dialog box appears.
2. Select a model and library in the Wire load model drop-down list.
3. Click OK or Apply.

**Note:**

You can also develop custom wire load models. For details, see the *Library Compiler documentation*.

**See Also**

- [Wire Load \(Attributes > Operating Environment\)](#)
- [Selecting Timing Ranges](#)
- [Selecting Operating Conditions](#)

---

## Defining Drive Characteristics for Input Ports

Drive characteristics model is the drive capability of an external driver. You can define drive characteristics for top-level input or inout (bidirectional) ports of the current design by associating them with a cell or pin in the technology library. You can use different library cells to model the drive characteristics for the rising clock edge and the falling clock edge.

You can define drive characteristics on an input port to buffer nets in the case of a weak driver. The drive capability of a port includes both the drive strength and the port transition delay.

Drive strength is the reciprocal of the driver resistance. The transition time delay at an input port is the product of the drive resistance and the capacitance load of the input port. You can also apply to the ports any design rule requirements (such as maximum fanout or maximum transition time) that have been assigned to the library cell.

The default drive resistance is 0 (infinite drive strength), which is appropriate for heavily loaded driving ports such as clock lines. You should keep the drive strength at 0 for these ports because each semiconductor vendor has a different way of distributing these signals within the silicon.

**Note:**

For some input ports, the port drive capability cannot be characterized with a cell in the technology library. You can use the `set_drive` and `set_input_transition` commands to assign drive resistance and transition delay values to these ports. However, these commands are not as accurate for nonlinear delay models.

For more information about setting the drive characteristics for input ports, see the *Design Compiler User Guide*.

The following sections explain how to apply and remove drive characteristics for top-level input ports.

To define the drive characteristics for one or more ports,

1. Select one or more input or inout ports.
2. Choose Attributes > Operating Environment > Drive Strength.

The Drive Strength dialog box appears.

3. Select the Use library cell options to enable the library cell options.
4. Specify a cell name by performing one of the following:
  - Enter the cell name in the Library cell name text box.
  - Click the  button and select a cell name.

The name of the technology library in which the cell is defined appears in the Library name text box. If cells with the same name are defined in more than one library, Design Vision displays the name of the first library in which it finds the cell.

If you want to use a cell defined in a different library, enter the library name in the Library cell name text box.

5. If the cell has more than one output pin, select a pin name in the Cell's output pin name drop-down list.

This option is required when the cell has more than one output pin.

6. If the cell has more than one input pin, select a pin name in the Cell's input pin name drop-down list.

This option is required when the driving cell has more than one input pin and the arcs from those pins have different drive characteristics.

7. Set options as required to control if the drive characteristics apply to the rising clock edge, the falling clock edge, or both.

- To apply the drive characteristics to both the rising and falling clock edges, make sure the Rise only option and the Fall only option are both deselected.
- To apply the drive characteristics to just the rising clock edge, select the Rise only option and enter a value in the Input rise transition time text box.

The input rise transition time value sets the rising edge transition time associated with the input pin of the driving cell. The default is 0.

- To apply the drive characteristics to just the falling clock edge, select the Fall only option and enter a value in the Input fall transition time text box.

The input fall transition time value sets the falling edge transition time associated with the input pin of the driving cell. The default is 0.

8. Set other options as required.

- To specify a factor by which the compiler multiplies the port delay characteristics, enter a value in the Multiplication factor text box.

Both the load delay and the transition times are affected. The default multiplication factor is 1.0.

- To prevent the compiler from scaling the port drive capability, select the Don't scale option.

By default, this option is deselected and the port drive capability is scaled for operating conditions that exactly match the way the driving cell would be scaled.

- To prevent the compiler from deriving design rule attributes from the driving cell and applying them to the ports it drives, select the No design rule option.

The design rules that can be applied to the ports are maximum and minimum fanout, maximum and minimum capacitance, and maximum and minimum transition time.

By default, this option is deselected and the design rule attributes are automatically applied to the ports.

**Note:**

Timing attributes derived from the driving cell are always applied to the ports the cell drives.

9. Click OK or Apply.
  - (Optional) To define the drive characteristics for a different clock edge on the same ports, click Apply and repeat steps 3 through 8.
  - (Optional) To define the drive characteristics for other ports, click Apply and repeat steps 2 through 8.

To remove the drive characteristics from one or more ports,

1. Select one or more input or inout ports.
2. Choose Attributes > Operating Environment > Drive Strength.

The Drive Strength dialog box appears. The Port name text box displays the names of the selected ports.

3. Select the Remove cell attributes option.
4. Click OK or Apply.

**See Also**

- [Drive Strength \(Attributes > Operating Environment\)](#)
- [Setting Capacitive Loads on Input Ports](#)
- [Setting Capacitive and Fanout Loads on Output Ports](#)

---

## Setting Capacitive Loads on Input Ports

You can set the capacitive load on top-level input ports to help model the transition delay on input pads. The default load is 0.

To set the capacitive load,

1. Select one or more input or inout ports.
  2. Choose Attributes > Operating Environment > Load.
- The Load dialog box appears.
3. Enter a value in the Capacitive load text box.
  4. Click OK or Apply.

### See Also

- [Load \(Attributes > Operating Environment\)](#)
- [Defining Drive Characteristics for Input Ports](#)
- [Setting Capacitive and Fanout Loads on Output Ports](#)

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## Setting Capacitive and Fanout Loads on Output Ports

You can set the capacitive load on top-level output ports to help the compiler select the appropriate drive strength of the output pads. You can also set expected fanout loads to model the external fanout effects.

When you set the expected fanout load for a port, the compiler adds this fanout value to all other loads on the pin driving the port and tries to make the total load less than the maximum fanout load of the pin.

To set the capacitive load and the expected fanout load for top-level ports,

1. Select one or more output or inout ports.
2. Choose Attributes > Operating Environment > Load.  
The Load dialog box appears.
3. To set the capacitive load, enter a value in the Capacitive load text box.
4. To set the fanout load, enter a value in the Fanout load text box.
5. Click OK or Apply.

### See Also

- [Load \(Attributes > Operating Environment\)](#)
- [Defining Drive Characteristics for Input Ports](#)
- [Setting Capacitive and Fanout Loads on Output Ports](#)

---

## Selecting Timing Ranges

The compiler optimizes designs according to operating temperature, supply voltage, and manufacturing process variations. You can use timing ranges to model statistical variations in the nominal operating conditions. This modeling produces accurate results in cases where all delays have a linear dependency on the operating conditions. In cases where delays do not scale linearly with operating conditions, this method provides only a first-order approximation.

A timing range consists of two multipliers used to calculate the range of delays for the best-case and worst-case timing conditions. These multipliers, or scaling factors, are applied to the nominal path delays when the compiler times the design.

The compiler uses these scaling factors to modify the calculations of the following timing constraints:

- Maximum path delay (setup) multiplied by the slowest (largest) factor of all the specified ranges
- Minimum path delay (hold) multiplied by the fastest (smallest) factor of all the specified ranges

For more information about maximum and minimum path delay computation, see the *Design Compiler Reference Manual: Constraints and Timing*.

Timing ranges are defined by the `timing_range` attribute specification in the technology library. If no timing ranges are selected, no timing range is used.

You can define or change the timing range scaling factors for the current design. You can select a single scaling factor or select different factors for maximum and minimum path delays. Maximum path delays are scaled by the slowest factor, and minimum delays are scaled by the fastest factor.

Timing ranges affect timing reports and the delay-cost computations for the `compile` and `report_constraint` commands. For details, see the *Design Compiler Reference Manual: Constraints and Timing*. You can view a constraints report or a timing report to see information about the range and factor used to scale a path delay. For details, see [Reporting Constraint Violations](#) and [Reporting Worst Path Timing](#).

To set or remove the timing range scaling factors for the current design,

1. Choose Attributes > Operating Environment > Timing Range.

The Timing Ranges dialog box appears. The current timing ranges appear in the Timing ranges text boxes.

2. Perform one of the following options:

- To set or change the timing ranges, select the timing range scaling factors in the list below the Timing ranges text boxes.
- To remove the timing ranges, select <NONE> in the list below the Timing ranges text boxes

3. Click OK or Apply.

### See Also

- [Timing Range \(Attributes > Operating Environment\)](#)
- [Selecting a Wire Load Model](#)
- [Selecting Operating Conditions](#)

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## Setting Constraints

Setting design constraints can involve using a large number of commands. Most designers find it convenient to use scripts to set design constraints.

The Design Compiler tool uses design rule and optimization constraints to control the synthesis of the design.

To learn about defining the design environment and setting design rule and optimization constraints in Design Vision, see the following topics:

- [Constraining Designs](#)
- [Creating Clocks](#)
- [Setting Design Rule Constraints](#)
- [Setting Optimization Constraints](#)
- [Setting Exceptions to Single-Cycle Timing](#)
- [Deriving Timing Constraints](#)
- [Characterizing the Context of a Subdesign Instance](#)

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## Constraining Designs

Before you can optimize your design, you must

- Define the design environment
- Set design rule constraints
- Set optimization constraints

You can define the environment and set constraints in Design Vision tool by

- Choosing commands on the Attributes menu
- Entering commands on the command line
- Running a Tcl script that contains constraint commands

The design environment models the conditions in which you expect the design to operate. You define the environment by selecting

- Operating conditions
- Wire load models
- System interface characteristics (input drives, capacitive loads, and fanout loads)

The environment model directly affects design synthesis results. For details, see [Defining the Design Environment](#).

Design rule and optimization constraints define the goals for the compiler to meet as it synthesizes your design. Constraints are measurable circuit characteristics such as timing, area, and capacitance.

Design rule constraints are technology-specific restrictions implicitly defined in the technology library. They can include

- Transition time constraints
- Fanout load constraints
- Capacitance constraints

These constraints are requirements for a design to function correctly, and they apply to any design using the library. You can explicitly define more restrictive constraints for individual designs. For more details, see [Setting Design Rule Constraints](#).

Optimization constraints are performance objectives that you define. They can include

- Timing constraints
- Area constraints
- Porosity (routability) constraints
- Power constraints

These constraints apply to the design on which you are working for the duration of the Design Vision session and represent the design's goals. They must be realistic. Optimization constraints are the most essential part of the description that drives the synthesis process. For more details, see [Setting Optimization Constraints](#).

The compiler tries to meet both design rule constraints and optimization constraints, but design rule constraints take precedence.

---

## Creating Clocks

You can create a clock by defining its period and (optionally) its waveform. If you do not define a waveform for a clock, the compiler uses a 50 percent duty cycle. For example, to create a 25-megahertz clock with a 50 percent duty cycle, you define a clock period of 40. You can create both real and virtual clocks.

You create real clocks for selected clock sources (ports or pins). Real clocks can be ideal or propagated.

- An ideal clock incurs no delay through the clock network. Ideal clocks can represent expected clock network delay and uncertainty. Real clocks are ideal by default.

You set the clock network delay and uncertainty by using the `set_clock_latency` and `set_clock_uncertainty` commands. For details, see the *Design Compiler User Guide*.

- A propagated clock is the opposite of an ideal clock. Registers clocked by a propagated clock have edge times skewed by the path delay from the clock source to the register clock pin.

You define a propagated clock by using the `set_propagated_clock` command. For details, see the *Design Compiler User Guide*.

A virtual clock has no sources. It exists in memory but is not part of a design. You create virtual clocks to represent delays that are relative to clocks outside the block.

Clocks are necessary to constrain a design. For synchronous designs, the clock period is the most important timing constraint because it constrains all register-to-register paths in the design. Timing for sequential paths is considered relative to clock edges. The compiler automatically finds the relevant setup and hold relations by expanding the clock waveforms. If you want nonsingle-cycle behavior, you can set multicycle paths.

If your design contains multiple clocks, pay close attention to the common base period of the clocks. The common base period is the least common multiple of all the clock periods. For example, if you have clock periods of 10, 15, and 20, the common base period is 60. For more details, see the *Design Compiler User Guide*.

The compiler reports timing delays from clock to clock: from synchronous logic to synchronous logic or to the logic between synchronous cells. You can generate a clock report to view information about all the clock sources in your design. For details, see [Reporting Clock Information](#).

To create or change a clock,

1. Select the input port or pin associated with the clock.

**Note:**

Ignore this step if you are defining a virtual clock.

2. Choose Attributes > Specify Clock to open the Specify Clock dialog box.

The name of the selected port or pin appears in the Port name text box. If you have already defined a clock for the port, the name of the clock appears in the Clock name text box

3. Enter a name in the Clock name text box.

You can edit the name in the Clock name text box to create a new clock. If you specify a new clock name for a port or pin that already has a clock, the new clock replaces the existing one.

4. Enter a value in the Period text box.

5. Define the clock waveform by entering one or more edge pairs of rising and falling values in the table below the Period text box.

The waveform must consist of an even number of monotonically increasing time values over an entire clock period. The compiler treats these time values as alternating rise and fall times. You must enter at least one pair of rising and falling edge values.

Use the following options on the right of the table to add or remove edge pairs or to invert the waveform (by reversing the order of edge pairs in the table).

- To add a new pair of Rising and Falling rows to the table, click the Add edge pair button.
- To remove a pair of Rising and Falling rows from the table, Shift-click the rows to select them and click the Remove edge pair button.

You must select adjacent rows.

- To reverse the order of edge pair (Rising and Falling) rows in the table, click the Invert wave form button.

6. (Optional) If you want the compiler to preserve the clock network during design optimization, select the Don't touch network option.

This option sets the `dont_touch_network` attribute on the clock, which prevents the compiler from modifying the clock buffer network. During design optimization, the compiler assigns `dont_touch` attributes to the cells and nets in the transitive fanout of the clock. For more details, see the man page for the `set_dont_touch_network` command and the *Design Compiler Reference Manual: Constraints and Timing*.

7. (Optional) If you want the compiler to fix hold time violations on timing paths that end at registers fed by the clock, select the Fix hold option.

This option sets `fix_hold` attributes on the selected clock objects (ports or pins). During design optimization, the compiler does not fix hold time violations unless this attribute is applied to the related clocks. For more details, see the man page for `theSet_fix_hold` command and the *Design Compiler Reference Manual: Constraints and Timing*.

8. Click OK or Apply.

To remove a clock from the current design,

1. Select the input port or pin associated with the clock.

**Note:**

Ignore this step if you are removing a virtual clock.

2. Choose Attributes > Specify Clock to open the Specify Clock dialog box.

The name of the selected port or pin appears in the Port name text box. If you are removing a source clock associated with the port or pin, the name of the clock appears in the Clock name text box.

3. If you are removing a virtual clock, enter its name in the Clock name text box.
4. Select the Remove clock option.
5. Click OK.

**See Also**

- [Specify Clock \(Attributes Menu\)](#)
- [Fixing Hold Time Violations](#)

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## Setting Design Rule Constraints

Design rules are provided in the vendor logic library to ensure that the product meets specifications and works as intended. Typical design rules constrain transition times, fanout loads, and capacitances. These rules specify technology requirements that you cannot violate. (You can, however, specify stricter constraints.)

To set design rule constraints for the current design by using the GUI,

- Choose Attributes > Optimization Constraints > Design Constraints, set options as needed, and click OK.

To set design rule constraints for certain input ports by using the GUI,

- Select the ports, choose Attributes > Optimization Directives > Input Port, set options as needed, and click OK.

Design rule constraints are attributes specified in the technology library and, optionally, specified explicitly by you in a design. The designs reflect technology-specific restrictions your design must meet to function as required. Design rules constrain the nets of a design but are associated with the pins of cells from a technology library.

Most technology libraries specify default design rules. The compiler implicitly applies them to any design using that library when it compiles the design or creates a constraint report. The compiler cannot violate design rule constraints, even if it means violating optimization constraints (delay and area goals).

You cannot remove the implicit design rule constraints set in a technology library because they are requirements for the technology. However, you can explicitly set more-restrictive values. If implicit or explicit values are set on both a design and a port, the more restrictive value applies. You can remove design rule constraint values that you have set.

The following table shows the attributes that correspond to each design rule.

Design Rule	Attribute Names
Transition time	max_transition
Fanout load	max_fanout
Capacitance	max_capacitance min_capacitance
Cell degradation	cell_degradation
Connection class	connection_class

The most commonly specified design rule constraints are

- Maximum transition time
- Maximum fanout load
- Maximum capacitance

A technology library specifies a default maximum transition or a default maximum capacitance, but not both. To achieve the best result, do not mix maximum transition and maximum capacitance.

The compiler also supports minimum capacitance, cell degradation, and connection class constraints. For information about setting these constraints, see the Design Compiler

Reference Manual: Constraints and Timing and the Setting Design Rule Constraints topic in the *Design Compiler User Guide*.

For more information about setting design rules, see the following topics:

- [Setting Transition Time Constraints on Nets](#)
- [Setting Fanout Load Constraints on Nets](#)
- [Setting Capacitance Constraints on Nets](#)

## Setting Transition Time Constraints on Nets

You control transition times on nets in a design by applying maximum transition time constraints on input ports and output ports. Maximum transition time is a design rule constraint.

The transition time of a net is the time required for its driving pin to change logic values. This transition time is based on the technology library data. For the nonlinear delay model (NLDM), output transition time is a function of input transition and output load.

You can apply smaller (more conservative) transition time constraints than the limits specified in the technology library by setting maximum transition time (`max_transition` attribute) values for all nets in the design, for nets attached to individual input ports and output ports, or both.

To set the maximum transition time for nets in the current design,

1. Choose Attributes > Optimization Constraints > Design Constraints.  
The Design Constraints dialog box appears.
2. Enter a value in the Max transition text box.
3. Click OK or Apply.

To set the maximum transition time for nets attached to input ports,

1. Select one or more input or inout ports.
2. Choose Attributes > Optimization Directives > Input Port.  
The Input Port Attributes dialog box appears.
3. Enter a value in the Maximum transition text box.
4. Click OK or Apply.

To set the maximum transition time for nets attached to output ports,

1. Select one or more output or inout ports.
2. Choose Attributes > Optimization Directives > Output Port.

The Output Port Attributes dialog box appears.

3. Enter a value in the Maximum transition text box.
4. Click OK or Apply.

### See Also

- [Design Constraints \(Attributes > Optimization Constraints\)](#)
- [Output Port \(Attributes > Optimization Directives\)](#)
- [Input Port \(Attributes > Optimization Directives\)](#)

## Setting Fanout Load Constraints on Nets

You control fanout on nets in a design by applying maximum fanout load constraints on input ports and fanout load constraints on output ports. Maximum fanout load is a design rule constraint. The maximum fanout load for a net is the maximum number of loads the net can drive.

The compiler calculates the fanout of a driving pin by adding the fanout load values of all inputs driven by that pin. To determine whether a pin meets the maximum fanout load restriction, the compiler compares the calculated fanout load value with the value of the pin's maximum fanout load constraint. For details about fanout load constraints, see [Setting Capacitive and Fanout Loads on Output Ports](#).

The technology library can specify fanout by assigning default fanout constraints on the entire library or by assigning fanout constraints for specific pins in the library descriptions of individual cells. The compiler models fanout restrictions by associating a maximum fanout load (`max_fanout` attribute) value with each input port and cell output (driving) pin and a fanout load (`fanout_load` attribute) value with each output port and cell input pin.

### Note:

The fanout load value represents the weighted numerical contribution to the total fanout load. The fanout load imposed by an input pin is not necessarily 1.0. Library developers can assign higher fanout load values to model internal cell fanout effects.

You can apply smaller (more conservative) fanout constraints than the limits assigned in the technology library by setting maximum fanout load values for all nets in the design, for nets attached to individual input ports, or for both. In cases where fanout limits have been set for both the design and an input port, the compiler tries to meet the smaller (more restrictive) fanout limit.

To determine whether the technology library is set up to model fanout calculations, you can search for the `fanout_load` attribute on the cell input pins by using the `get_attribute` command. For more details, see the *Design Compiler User Guide*.

To set the maximum fanout loads for nets in the current design,

1. Choose Attributes > Optimization Constraints > Design Constraints.

The Design Constraints dialog box appears.

2. Enter a value in the Max fanout text box.

3. Click OK or Apply.

To set the maximum fanout loads for nets attached to certain input ports,

1. Select one or more input or inout ports.

2. Choose Attributes > Optimization Directives > Input Port.

The Input Port Attributes dialog box appears.

3. Enter a value in the Maximum fanout text box.

4. Click OK or Apply.

## See Also

- [Design Constraints \(Attributes > Optimization Constraints\)](#)
- [Input Port \(Attributes > Optimization Directives\)](#)

## Setting Capacitance Constraints on Nets

If you need to control net capacitance directly (in addition to setting transition time constraints), you can set maximum capacitance constraints on input ports. Maximum capacitance is a design rule constraint.

The compiler models capacitance restrictions by associating maximum capacitance (`max_capacitance` attribute) values with the output ports or pins of a cell. The compiler calculates the capacitance on an output port by adding the wire capacitance of the net to the capacitance of the pins attached to the net. To determine whether a net meets the maximum capacitance restriction, the compiler compares the calculated capacitance value with the value of the output pin's maximum capacitance constraint.

You can apply smaller (more conservative) capacitance constraints than the limits specified in the technology library by setting maximum capacitance values for nets attached to individual input ports.

To set the maximum capacitance for nets attached to input ports,

1. Select one or more input or inout ports.
2. Choose Attributes > Optimization Directives > Input Port.

The Input Port Attributes dialog box appears.

3. Enter a value in the Maximum capacitance text box.
4. Click OK or Apply.

**Note:**

You can also define minimum capacitance for input ports or pins. If the compiler attempts to ensure that the load at the input port does not fall below the minimum capacitance value, it does not specifically optimize for this constraint. For details, see the *Design Compiler Reference Manual: Constraints and Timing*.

**See Also**

- [Input Port \(Attributes > Optimization Directives\)](#)
- 

## Setting Optimization Constraints

Optimization constraints define the design goals for timing (clocks, clock skews, input delays, and output delays) and area (maximum area). During optimization, the tool attempts to meet these goals. However, it does not violate your design rules. To optimize a design correctly, you must set realistic optimization constraints.

Optimization constraints reflect your performance objectives for a design. The compiler uses these constraints to guide the optimization process. Timing and area are usually the primary considerations.

Optimization constraints consist of

- Timing constraints (performance and speed)

These typically include input and output delays for synchronous paths and minimum and maximum delays for asynchronous paths.

- Maximum area (number of gates)
- Minimum porosity (routability)
- Maximum dynamic power and maximum leakage power

**Note:**

The power constraints are used with the Power Compiler tool. They require a Power-Optimization license and supporting libraries characterized for power. For details, see the *Power Compiler documentation*.

Optimization constraints represent design goals and restrictions that you want but that might not be crucial to the operation of a design. Speed (timing) constraints have higher priority than area and porosity. Optimization constraints are secondary to design rule constraints.

To get the most effective results from the compiler, set the constraints close to your design goals.

- If no timing goals are set (the default), the compiler applies only design rule checks to the design.
- If timing goals are set to be small (for example, 0), the compiler adds buffers to critical paths or duplicates logic on heavily loaded nets when trying to meet this goal, which can cause a significant increase in area.
- With realistic timing goals, the compiler produces the smallest circuit that most closely satisfies the goal.

When you set an optimization constraint, the change is made the next time you optimize the design.

Timing constraints specify the required performance of the design. When defining timing constraints you should consider that your design has both synchronous and asynchronous paths.

- Synchronous paths are constrained by specifying clocks in the design. After specifying the clocks, you should also specify the input and output port timing specifications.
- Asynchronous paths are constrained by specifying minimum and maximum delay values.

To set optimization constraints by using the GUI,

1. Click Attributes in the menu to open the Attributes menu.
2. Choose the command for the constraints you want to set.

Choose Specify Clock option if you want to set clock periods and waveforms. Following are the optimization constraints and settings submenus under the Attributes menu:

- Operating Environment (input and output delays)
- Optimization Constraints (maximum and minimum delays and maximum area)
- Optimization Directives (design attributes, object attributes, and timing exceptions)

Explore these submenus to find the settings you need. For more information about menu items in the Attributes menu, see the [Attributes Menu](#).

To set the timing constraints, you can

- Define the clocks (for details, see [Creating Clocks](#)).
- Specify the I/O requirements relative to the clocks (for details, see [Setting Input Timing Requirements](#) and [Setting Output Timing Requirements](#)).

If you do not assign timing requirements to an input port, the compiler responds as if the signal arrives at the input port at time 0. In most cases, input signals arrive at staggered times.

If you do not assign timing requirements to an output port, the compiler does not constrain any paths which end at an output port.

- Specify the combinational path delay requirements (for details, see [Setting Combinational Path Delay Requirements](#)).
- Specify the timing exceptions (for details, see [Setting Exceptions to Single-Cycle Timing](#)).

Maximum area represents the number of gates in the design, not the physical area the design occupies.

- Usually the area requirements for the design are stated as the smallest design that meets the performance goal.
- Defining a maximum area directs the compiler to optimize the design for area after timing optimization is complete.

The compiler computes the area of a design by adding the areas of each component on the lowest level of the design hierarchy (and the area of the nets). The compiler ignores the following components when it calculates circuit area:

- Unknown components
- Components with unknown areas
- Technology-independent generic cells

The area of a cell (component) is technology-dependent and obtained from the technology library.

For details about setting area constraints, see [Setting Area Constraints](#).

Porosity is the ratio of routing track area to cell area. You can optimize the porosity to increase the routability of an ASIC design. One measure of the routability of an ASIC design is the number and area of tracks available for routing over cells.

- In standard cell technologies, the routing tracks are called feedthroughs.
- In gate array technologies, the routing tracks are called over-the-cell routing tracks.

For details about porosity constraints, see the *Design Compiler Reference Manual: Constraints and Timing*.

## Setting Timing Constraints

Timing constraints define the timing goals for your design. These constraints, which are user-specified and must be realistic, control how the compiler optimizes your design. You can

- Define clock periods and waveforms.
- Set the I/O timing requirements relative to the clocks.
- Set the combinational path delay requirements.
- Set timing exceptions.

For a synchronous design, the clock period is the most important constraint because it constrains all register-to-register paths in the design. If you do not define the clock waveform, the compiler uses a 50 percent duty cycle.

You can define a clock on an input port or pin. You can also define a virtual clock for modeling clock signals present in the system but not in the block. For details, see [Creating Clocks](#).

Synchronous designs also require timing constraints for the top-level input and output ports. You can set input and output delay constraints to define the arrival times for top-level input and output ports.

- If you do not assign timing delays to an input port, the compiler assumes that the signal arrives at the input port at time 0. In most cases, input signals arrive at staggered times.
- If you do not assign timing requirements to an output port, the compiler does not constrain any paths that end at an output port.

For details, see [Setting Input Timing Requirements](#) and [Setting Output Timing Requirements](#).

For purely combinational delays that are not bounded by a clock period, you can define the maximum delays on specific paths. For details, see [Setting Combinational Path Delay Requirements](#).

### Note:

Minimum delay constraints are not available for FPGA.

By default, the compiler automatically infers single-cycle timing from clock waveforms and from input delay and output delay information. Single-cycle timing means that data from an active edge of the startpoint clock is expected to be available at the path endpoint before the active edge of the endpoint clock that follows the startpoint edge.

The compiler automatically determines the maximum and minimum path delay requirements for the design. It examines the clock waveforms at the path startpoint and

endpoint. The default for setup is to allow a single clock cycle for data to reach the path endpoint. The path length calculation considers library setup time and clock delay and uncertainty values. The hold data is launched one cycle later at the path startpoint.

The compiler calculates the default setup and hold relations and derives single-cycle timing, based on active edges. The data must be available before the active edge of the endpoint clock (following an active edge at the startpoint) to satisfy the single-cycle setup relation.

- At the startpoint, the active edge is the register's opening edge.
- At the endpoint, the active edge is the register's closing edge.
- For a rising-edge-triggered flip-flop, the rising edge is both the open and the close edges.

Timing exceptions define timing relationships that override the default single-cycle timing relationship for one or more timing paths. You can use timing exceptions to constrain or disable asynchronous paths or paths that do not follow the default single-cycle behavior.

You can set the following timing exceptions in Design Vision tool:

- False paths
- Multicycle paths
- Maximum and minimum delay requirements

For details, see [Setting Exceptions to Single-Cycle Timing](#).

## See Also

- [Defining Timing Paths](#)

## Setting Area Constraints

You can control the area in a design by assigning it a maximum area attribute. Design area consists of the areas of each component and net. When design area is calculated, the following components are ignored:

- Unknown components
- Components with unknown areas
- Technology-independent generic cells

Cell area is technology dependent and is obtained from the technology library.

To assign a maximum area value to the current design,

1. Choose Attributes > Optimization Constraints > Design Constraints.  
The Design Constraints dialog box appears.
2. Enter a value in the Max area text box.
3. Click OK or Apply.

#### See Also

- [Setting Transition Time Constraints on Nets](#)
- [Setting Fanout Load Constraints on Nets](#)

## Setting Input Timing Requirements

You can set input delays to constrain input (or inout) ports. An input port delay represents the timing of an external path leading to the port from an external flip-flop. You can specify input delays relative to a clock edge or other inputs.

In most cases, input signals arrive at staggered times. If you do not assign timing requirements to an input port, signals are assumed to arrive at the port at time 0.

If you have applied drive resistance or a driving cell to the port, it already has a cell delay that is the load-dependent value of the external driving-cell delay. To prevent this delay from being counted twice, estimate the load-dependent delay of the driving cell, then subtract that amount from the input delays on the port.

The input delay should equal the path length from the clock pin of the source flip-flop to the output pin of the driving cell, minus the load-dependent portion of the driving cell's delay.

To set input delays on ports,

1. Select one or more input or inout ports.
2. Choose Attributes > Operating Environment > Input Delay.

The Input Delay dialog box appears.

3. To set the delays relative to a clock edge, select the clock name in the Relative to clock drop-down list.

or

To set the delays relative to time 0 for combinational designs, select <NONE> in the Relative to clock drop-down list. For sequential designs, the delays are considered relative to a new clock with the period determined by considering the sequential cells in the transitive fanout of each port.

4. To set the setup time delays, enter maximum and minimum delay values in the Max rise and Min rise text boxes.
5. If you want to set hold time delays that are different from the setup time delays, deselect the Same rise and fall option and enter maximum and minimum delay values in the Max fall and Min fall text boxes.
6. Click OK or Apply.

**Note:**

For a complete and correct analysis, specify the correct reference clock. If the clock is not input to this design, create a virtual clock and use that clock as the reference.

**See Also**

- [Input Delay \(Attributes > Operating Environment\)](#)

## Setting Output Timing Requirements

You can set output delays to constrain output (or inout) ports. An output port delay represents the timing of an external path from the port to a register. You specify output delays relative to a clock edge.

If you do not assign timing requirements to an output port, the signals are assumed to be unconstrained.

The maximum output delay value should be equal to the length of the longest path to the register data pin, plus the setup time of the register. The minimum output delay value should be equal to the length of the shortest path to the register data pin, minus the hold time.

To set output delays on ports,

1. Select one or more output or inout ports.
2. Choose Attributes > Operating Environment > Output Delay.

The Output Delay dialog box appears.

3. To set the delays relative to a clock edge, select the clock name in the Relative to clock drop-down list.

or

To set the delays relative to time 0 for combinational designs, select <NONE> in the Relative to clock drop-down list. For sequential designs, the delays are considered relative to a new clock with the period determined by considering the sequential cells in the transitive fanout of each port.

4. To set the setup time delays, enter maximum and minimum delay values in the Max rise and Min rise text boxes.
5. If you want to set hold time delays that are different from the setup time delays, deselect the Same rise and fall option and enter maximum and minimum delay values in the Max fall and Min fall text boxes.
6. Click OK or Apply.

**Note:**

For a complete and correct analysis, specify the correct reference clock. If the clock source is not in this design, create a virtual clock and use that clock as the reference.

**See Also**

- [Output Delay \(Attributes > Operating Environment\)](#)

## Setting Combinational Path Delay Requirements

You can use maximum and minimum delays to constrain purely combinational timing paths that are not bounded by a clock period.

You can produce asynchronous logic in HDL code by using asynchronous sets or resets on latches and flip-flops. Since the reset signal crosses several blocks, you can constrain this signal at the top level of the design.

The compiler performs critical path tracing to check minimum and maximum delays for every timing path in the design. The most critical path is not necessarily the longest combinational path in a sequential design, because paths can be relative to different clocks at path startpoints and endpoints. The compiler calculates minimum and maximum signal rise and fall path values based on the timing values and environmental information in the technology library.

The compiler automatically determines maximum delay target values for each timing path in the design after considering clock waveforms and skew, library setup times, external delays, multicycle or false path specifications, and any maximum delay times you have set. Load, drive, operating conditions, wire load model, and other factors are also taken into account.

The compiler fixes minimum delay constraints when it fixes design rule violations. Minimum delays are set implicitly due to hold time requirements. The minimum delay to a pin or port must be greater than the target delay. The compiler considers minimum delays only when the `fix_hold` attribute is set (for details, see [Fixing Hold Time Violations](#)).

You can generate a timing requirements report (choose Timing > Report Timing Requirements) to see a list of minimum and maximum delay requirements for your design. For details, see [Reporting Timing Requirements](#).

For details about setting maximum and minimum delays, see [Setting Maximum and Minimum Delay Requirement](#).

### See Also

- [Timing Constraints \(Attributes > Optimization Constraints\)](#)

## Creating Path Groups

A path group is a collection of timing paths that represent a group in maximum delay cost calculations. By default, the compiler groups paths based on the clocks that control the path endpoints. Each time you create a clock, the compiler creates a path group that contains all the paths associated with the clock.

The default path group is an implicit path group. It contains the paths that are not in any other group. All paths not associated with a clock are in the default path group. If your design has complex clocking, complex timing requirements, or complex constraints, you can create path groups to focus the compiler on specific critical paths.

By creating path groups, or by adding or removing paths in existing groups, you can

- Control the optimization of your design

Create and prioritize path groups that affect only the maximum delay cost function. By default, the compiler works only on the worst violator in each group.

- Optimize near-critical paths

When you add a critical range to a path group, you change the maximum delay cost function from worst negative slack to critical negative slack. The compiler optimizes all paths within the critical range.

### Note:

Specifying a critical range can increase runtime. To limit the increase, use critical ranges only during the final implementation phase of the design, and use a reasonable critical range value. A guideline for the maximum critical range value is 10 percent of the clock period.

- Optimize all paths

Create a path group for each endpoint in the design. This enables total negative slack optimization but results in long compile runtimes.

For more information about path groups, see the *Design Compiler User Guide* and the man page for the `group_path` command.

Only timing paths that have valid reference points are recognized by the compiler. The valid startpoints in a design are the primary input ports and clock pins of sequential

cells. The valid endpoints are the primary output ports of the design and the data pins of sequential cells.

If you do not select any valid startpoints, all paths that end at the selected endpoints are added to the group. If you do not select any valid endpoints, all paths that start at the selected startpoints are added to the group.

To create a path group or add paths to an existing group,

1. Select one or more ports, pins, or cells to identify the startpoints and endpoints for the paths.
2. Choose Attributes > Optimization Constraints > Timing Constraints to open the Timing Constraints dialog box.

The From list (for path startpoints) displays the names of the selected input ports. The To list (for path endpoints) displays the names of the selected pins, cells, and output ports.

3. Adjust the path startpoints and endpoints, if necessary.
  - To move an object name from the From list to the To list, select the name and click the down arrow button.
  - To move an object name from the To list to the From list, select the name and click the up arrow button.
  - To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)
4. Enter the name of a path group in the Group name text box. If the group does not exist, the compiler creates the group. If you enter the name of an existing group, the compiler adds the paths to the group.
5. Set other options as needed.
6. Click OK or Apply.

## See Also

- [Timing Constraints \(Attributes > Optimization Constraints\)](#)

## Fixing Hold Time Violations

You can direct the compiler to fix hold time (minimum delay) violations during design optimization by setting `fix_hold` attributes on clock objects (ports or pins). When the `fix_hold` attribute is set on a clock source, the compiler inserts delays to fix hold violations for timing paths that end at registers fed by the clock.

The compiler does not fix hold time violations unless the `fix_hold` attribute is applied to the related clocks.

**Note:**

Meeting hold time requirements is less difficult than meeting setup time requirements. Minimum delay violations are exaggerated under best-case operating conditions; use the worst-case operating condition until setup is met.

For more details, see the man page for the `set_fix_hold` command and the *Design Compiler Reference Manual: Constraints and Timing*.

To fix hold time violations on paths related to a clock,

1. Select the clock port or pin.
2. Choose Attributes > Specify Clock.

The Specify Clock dialog box appears. The clock name appears in the Clock name text box, and the name of the selected port or pin appears in the Port name text box.

3. Select the Fix hold option.
4. Click OK.

**See Also**

- [Specify Clock \(Attributes Menu\)](#)
- [Creating Clocks](#)

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## Setting Exceptions to Single-Cycle Timing

Timing exceptions define timing relationships that override the default single-cycle timing relationship used to determine maximum and minimum delay requirements for paths in a design. Single-cycle timing means that data propagates to its destination in less than one clock cycle.

In some cases, single-cycle timing might not be appropriate. For example, some paths are multicycle paths that require more than one clock cycle to propagate data, and others are false (invalid) paths.

**Note:**

Specifying numerous timing exceptions can increase the compile runtime. However, some designs can require many timing exceptions.

You can use the following timing exceptions to constrain or disable asynchronous paths or paths that do not follow the default single-cycle behavior:

- False paths
- Multicycle paths
- Maximum and minimum path delays

False paths are logic paths that exist but are not considered during timing optimization. These paths are not included in timing reports. For details, see [Setting False Paths](#).

Multicycle paths are paths that require more than one clock cycle to propagate. You can set the multiplier for setup checks, hold checks, or both. For details, see [Setting Multicycle Paths](#).

Maximum path delays are typically used in the following cases:

- To set a target delay for output ports in a combinational design
- To override the default single-cycle timing for paths where setting multicycle paths is not sufficient

Minimum path delays are used to override the default hold relation for paths in a sequential design where setting multicycle paths is not sufficient. For details, see [Setting Maximum and Minimum Delay Requirement](#).

You can generate a timing requirements report to view a list of the timing exceptions in your design. For details, see [Reporting Timing Requirements](#).

The compiler recognizes only timing exceptions that have valid startpoints and endpoints.

- Valid startpoints are the primary input ports of a design and the clock pins of sequential cells.
- Valid endpoints are the primary output ports of a design and the data pins of sequential cells.

The compiler ignores paths with invalid startpoints or endpoints and does not issue a warning message. You can include a list of these paths in the timing requirements report by selecting the Show ignored path attributes option in the Report Timing Requirements dialog box. For details, see [Reporting Timing Requirements](#).

## See Also

- [Defining Timing Paths](#)
- [Setting Timing Constraints](#)

## Setting False Paths

False paths are logic paths that, although they exist, are not considered during timing optimization and are excluded from timing reports. You can specify false-path timing exceptions when you want to ignore paths that

- Are not timing critical
- Can mask other paths that must be considered during optimization
- Never occur in normal operation

Only timing exceptions that have valid reference points are recognized. The valid startpoints in a design are the primary input ports and clock pins of sequential cells. The valid endpoints are the primary output ports of the design and the data pins of sequential cells.

**Note:**

The compiler does not generate a warning message if you specify invalid reference points. Use the `report_timing_requirements` command with the `-ignored` option to find timing exceptions that are ignored by the compiler.

If you do not select any valid startpoints, the false-path exceptions you select apply to all paths that end at the selected endpoints. If you do not select any valid endpoints, the false-path exceptions you select apply all to paths that start at the selected startpoints.

To set false-path timing exceptions,

1. Select one or more pins or ports to identify the startpoints and endpoints of the paths.
2. Choose Attributes > Optimization Directives > Timing Paths to open the Timing Paths dialog box.

The From list (for path startpoints) displays the names of the selected input ports. The To list (for path endpoints) displays the names of the selected pins, cells, and output ports.

3. Adjust the path startpoints and endpoints, if necessary.
  - To move an object name from the From list to the To list, select the name and click the down arrow button.
  - To move an object name from the To list to the From list, select the name and click the up arrow button.
  - To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)

4. To disable setup (maximum delay) constraints on the paths, select the False path option under Setup.
5. To disable hold (minimum delay) constraints on the paths, select the False path option under Hold.
6. Click OK or Apply.

### See Also

- [Timing Paths \(Attributes > Optimization Directives\)](#)

## Setting Multicycle Paths

Multicycle paths are paths that require more than one clock cycle to propagate. Use multipath exceptions for paths that are longer than a single clock cycle and for cases when data is not expected within a single cycle.

You can set the cycle multiplier (the number of cycles within which data is expected to reach the path endpoint) for setup checks, hold checks, or both.

By default, setup is checked at the next active edge of the clock at the endpoint after the data is launched from the startpoint (default multiplier of 1). Hold data is launched one clock cycle after the setup data but checked at the edge used for setup (default multiplier of 0).

Only timing exceptions that have valid reference points are recognized. The valid startpoints in a design are the primary input ports and clock pins of sequential cells. The valid endpoints are the primary output ports of the design and the data pins of sequential cells.

### Note:

The compiler does not generate a warning message if you specify invalid reference points. You can generate a timing requirements report to find timing exceptions that are ignored by the compiler. For details, see [Reporting Timing Requirements](#).

If you do not select any valid startpoints, the multicycle path exceptions you select apply to all paths that end at the selected endpoints. If you do not select any valid endpoints, the multicycle path exceptions you select apply to all paths that start at the selected startpoints.

To set multicycle-path timing exceptions,

1. Select one or more pins or ports to identify the startpoints and endpoints of the paths.
2. Choose Attributes > Optimization Directives > Timing Paths to open the Timing Paths dialog box.

The From list (for path startpoints) displays the names of the selected input ports. The To list (for path endpoints) displays the names of the selected pins, cells, and output ports.

3. Adjust the path startpoints and endpoints, if necessary.
  - To move an object name from the From list to the To list, select the name and click the down arrow button.
  - To move an object name from the To list to the From list, select the name and click the up arrow button.
  - To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)
4. To disable setup (maximum delay) constraints on the paths, select the Multi cycle path option under Setup.
5. To disable hold (minimum delay) constraints on the paths, select the Multi cycle path option under Hold.
6. Click OK or Apply.

#### See Also

- [Timing Paths \(Attributes > Optimization Directives\)](#)

### Setting Maximum and Minimum Delay Requirement

You can use maximum and minimum delays to specify timing path requirements that are more conservative than those derived from clock timing. Setting the maximum delay on a path removes a previous multicycle path specification on the same path.

Maximum path delays typically are used in the following cases:

- To set a target delay for output ports in a combinational design  
For details, see [Setting Combinational Path Delay Requirements](#).
- To override the default single-cycle timing for paths where setting multicycle paths is not sufficient.  
For details, see [Setting Exceptions to Single-Cycle Timing](#).

Minimum path delays are used to override the default hold relation for paths in a sequential design where setting multicycle paths is not sufficient.

You can generate a timing requirements report (choose Timing > Report Timing Requirements) to see a list of minimum and maximum delay requirements for your design. For details, see [Reporting Timing Requirements](#).

Slack is the amount of margin by which maximum or minimum path delay requirements are met. Positive slack indicates that the requirement is met; negative slack indicates a violation. Slack is displayed in timing reports.

A violation indicates a constraint is not met.

- A setup violation occurs when a timing path is longer than its targeted maximum delay. The cost function considers the worst violator within each path group when calculating maximum delay cost.
- A hold violation occurs when a timing path is shorter than its targeted minimum delay. A violation is the same as a negative slack value.

The compiler recognizes only the timing paths that have valid reference points. The valid startpoints in a design are the primary input ports and clock pins of sequential cells. The valid endpoints are the primary output ports of the design and the data pins of sequential cells.

If you do not select any valid startpoints, the delay values you specify apply to all paths that end at the selected endpoints. If you do not select any valid endpoints, the delay values you specify apply to all paths that start at the selected startpoints.

To set maximum and minimum delay requirements,

1. Select one or more ports, pins, or cells to identify the startpoints and endpoints for the paths.
2. Choose Attributes > Optimization Constraints > Timing Constraints to open the Timing Constraints dialog box.

The From list (for path startpoints) displays the names of the selected input ports. The To list (for path endpoints) displays the names of the selected pins, cells, and output ports.

3. Adjust the path startpoints and endpoints, if necessary.
  - To move an object name from the From list to the To list, select the name and click the down arrow button.
  - To move an object name from the To list to the From list, select the name and click the up arrow button.
  - To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)

4. To set the setup time delays, enter maximum and minimum delay values in the Max rise and Min rise text boxes.
5. (Optional) If you need to set hold time delays that are different from the setup time delays, deselect the Same rise and fall option and enter maximum and minimum delay values in the Max fall and Min fall text boxes.
6. (Optional) If you need to remove other timing exceptions before applying the delays, select the Reset path option.

When you select this option, the compiler removes exceptions only on the delays types for which you enter values (setup rise, setup fall, hold rise, or hold fall). If you do not enter any delay values, the compiler removes all timing exceptions from the paths.

7. Click OK or Apply.

#### See Also

- [Timing Constraints \(Attributes > Optimization Constraints\)](#)

### Restoring Single-Cycle Timing

If you have set point-to-point timing exceptions for paths in your design, you can remove exceptions and restore paths to single-cycle timing. Single-cycle timing is the default timing requirement for a path.

You can restore paths set as false paths or multicycle paths and paths to which you have applied maximum or minimum delay constraints. You can restore setup (maximum rise and fall delay) checking, hold (minimum rise and fall delay) checking, or both.

To reset paths to single-cycle timing,

1. Select one or more pins or ports to identify the startpoints and endpoints of the paths.
2. Choose Attributes > Optimization Directives > Timing Paths to open the Timing Paths dialog box.

The From list (for path startpoints) displays the names of the selected input ports. The To list (for path endpoints) displays the names of the selected pins, cells, and output ports.

3. Adjust the path startpoints and endpoints, if necessary.

- To move an object name from the From list to the To list, select the name and click the down arrow button.
  - To move an object name from the To list to the From list, select the name and click the up arrow button.
  - To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)
4. To set maximum rise and fall delay checking to single-cycle timing, select the Single cycle path option under Setup.
  5. To set minimum rise and fall delay checking to single-cycle timing, select the Single cycle path option under Hold.
  6. Click OK or Apply.

### See Also

- [Timing Paths \(Attributes > Optimization Directives\)](#)

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## Deriving Timing Constraints

You can derive timing constraints from existing timing information for timing paths in the current design. Both sequential and combinational constraints are derived for all previously unconstrained timing paths. You can derive

- Maximum and minimum delay constraints for combinational paths
- Maximum period constraints and hold constraints for clocks
- Separate rise and fall constraints for combinational timing endpoints

You can also set maximum delay, minimum delay, and maximum period scaling factors.

To derive constraints for timing paths,

1. Choose Attributes > Optimization Constraints > Derive Constraints to open the Derive Constraints dialog box.
2. Select the options you need to use.
  - To derive maximum period constraints for clocks in the current design, select the Maximum period option.
  - To derive separate rise and fall constraints for each combinational timing endpoint, select the Separate rise and fall option.

- To derive hold constraints for unconstrained clocks in the design, select the Fix hold option.
  - To derive maximum delay constraints for unconstrained combinational paths in the current design, select the Maximum delay option.
  - To derive minimum delay constraints for unconstrained combinational paths in the current design, select the Minimum delay option.
3. (Optional) Set scaling factors as needed.
- To set the scaling factor for maximum delay constraints, enter a value in the Max delay text box.
  - To set the scaling factor for minimum delay constraints, enter a value in the Min delay text box.
  - To set the scaling factor for maximum clock period constraints, enter a value in the Max period text box.
4. Click OK.

#### See Also

- [Derive Constraints \(Attributes > Optimization Constraints\)](#)

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## Characterizing the Context of a Subdesign Instance

You can characterize the context of a subdesign by deriving environment information from an instance of the subdesign based on its context in the parent design and then using this information to optimize the subdesign or to time it by itself.

To characterize the context of a design,

1. Select a cell.
2. Choose Attributes > Operating Environment > Characterize.

The Characterize dialog box appears.

3. Select the options you want to use.

- To characterize the timing of the selected cell, select Timing.
  - To characterize the area, power, connection class, and design rule constraints of the selected cell, select Constraints.
  - To characterize the logical connection (port) information of the selected cell, select Connections.
4. Click OK or Apply.

#### See Also

- [Characterize \(Attributes > Operating Environment\)](#)

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## Compiling the Design

You can use the Design Vision GUI to initiate Design Compiler synthesis and optimization, thus compiling your high-level design description to your target technology. The Design Vision tool supports standard synthesis methodology, that is, either a top-down compile or a bottom-up compile.

To control the optimization process, you can

- Set the relative design mapping and area recovery efforts
- Set compile options
- Set design rule options
- Set background compilation options to run the compiler in the background or across the network on another machine

If you are using TestMAX DFT, you can set a compile option that performs a test-ready compile by replacing all sequential elements

with scan-equivalent cells.

For information about compiling the design in the Design Vision GUI, see the following topics:

- [Using the Compile Command](#)
- [Using the Compile Ultra Command](#)

For information about compile methodologies, see the *Design Compiler User Guide*.

---

## Using the Compile Command

To compile the current design,

1. Choose Design > Compile Design.

The Compile Design dialog box opens.

2. Select the mapping options you need to control the relative efforts for design mapping and area recovery.

- Select a Map effort option: medium or high. The default is medium.
- Select an Area effort option: low, medium, or high. The default is high.

**Note:**

If you want the compiler to use generic Boolean equations and generic flip-flops to represent the optimized design instead of mapping the design to the technology library, deselect Mapping options.

3. Select the compile options you need to use.

- To fix design rule and top-level timing violations, select the Top level option.
- To map the circuit by using only local mapping transformations that improve the circuit, select the Incremental mapping option.
- To remove all levels of hierarchy in the design (except for subdesigns assigned the `dont_touch` attribute), select the Ungroup all option.
- To optimizes the design across all hierarchical boundaries, select the Allow boundary conditions option.
- To enable the compiler to automatically remove levels of hierarchy in the design, select the Auto ungroup option and select either Area (to improve area recovery in small designs) or Delay (to improve overall design timing).
- To exactly match sequential elements with their descriptions in the HDL code (for designs that contain SEQUEM elements), select the Exact map option.

4. (Optional) If you are using TestMAX DFT and need to perform a test-ready compile, select the Scan option.

5. (Optional) If you need to control whether and how the compiler fixes design rule violations, select the appropriate design rule option.

- If you want the compiler to fix design rule violations during design optimization, select the Fix design rules and optimize mapping option.
- If you do not want the compiler to fix design rule violations, select the Optimize mapping only option.
- If you want the compiler to fix design rule violations without optimizing the design, select the Fix design rules only option.
- If you want the compiler to fix hold time violations for clocks that have been assigned the `hold_fix` attribute (and ignore all other design rule violations) during design optimization, select the Fix hold time only option.

When you select this option, the compiler attempts to fix `hold_fix` attribute violations if the delay (setup) cost is not increased or if hold violations have been given a higher priority than maximum delay cost. For details about attribute priorities, see the `set_cost_priority` man page. For details about the `hold_fix` attribute, see the `set_fix_hold` man page.

6. (Optional) If you want to run the compiler in the background or on a remote system, select the Background option and enter the path to the run directory and the host name of the remote system, and select the architecture type of the remote system.
7. (Optional) If you selected the Background option and you want to display the compiler results on the X-terminal, select the Xterm Window option. This option is valid only in the X11 environment.
8. Select or deselect options you require.
9. Click OK to begin compiling.

Use the default settings for your first-pass compile. For most designs, the default settings provide good initial results. For more information about `compile` command options, see the man page and the *Design Compiler User Guide*.

After compiling the design, save the design as described in [Saving Designs on page 321](#).

## See Also

- [Using the Compile Ultra Command](#)

## Using the Compile Ultra Command

For high-performance designs that have significantly tight timing constraints, you can use the Design Vision GUI to initiate the DC Ultra solution for better quality of results (QoR). The `compile_ultra` command is a push-button solution that allows you to apply the best

possible set of timing-centric variables or commands during compile for critical delay optimization as well as improvement in area QoR.

**Note:**

Since the Compile Ultra includes all compile options and starts the entire compile process, a separate Compile command is not necessary.

To use the `compile_ultra` command, you need a DC Ultra license and a DesignWare Foundation license.

To compile the current design by using Compile Ultra,

1. Choose Design > Compile Ultra.

The Compile Ultra dialog box opens.

2. Select or deselect options as you require.

3. Click OK to begin compiling.

Select options according to the requirements of your design. To perform a second-pass incremental compile, select the Incremental option. For more information about `compile_ultra` command options, see the man page and the *Design Compiler User Guide*.

When you run the Design Vision tool in topographical mode, the Compile Ultra command automatically uses the Design Compiler topographical features. All `compile_ultra` command options are supported in this mode.

**Note:**

Using the Incremental option with a topographical netlist results in placement-based optimization only. This compilation should not be thought of as an incremental mapping. For more information about running the tool in topographical mode, see [Using a Milkyway Database on page 300](#).

After compiling the design, save the design as described in [Saving Designs on page 321](#).

**See Also**

- [Using the Compile Command](#)

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## Using Logic Synthesis Tools

Designs (design descriptions) are stored in design files. Design files must have unique names. If a design is hierarchical, each subdesign refers to another design file, which must

also have a unique name. However, different design files can contain subdesigns with identical names.

To learn about preparing and synthesizing designs in Design Vision tool, see

- [Checking Design Consistency](#)
- [Checking Design Timing](#)
- [Adding Levels of Hierarchy](#)
- [Adding Placement Groups](#)
- [Removing Levels of Hierarchy](#)
- [Creating Uniquely Named Copies of a Design](#)
- [Optimizing the Design](#)
- [Optimizing Critical Delays](#)

#### See Also

- [Working With Designs in Memory](#)
- [Using a Milkyway Database](#)

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## Checking Design Consistency

A design is consistent when it does not contain errors such as unconnected ports, constant-valued ports, cells with no input or output pins, mismatches between a cell and its reference, multiple driver nets, connection class violations, or recursive hierarchy definitions.

You can check the internal representation of the current design for consistency. Design Vision tool displays warning and error messages in the report view when problems are found.

- A warning message indicates a problem such as a corrupted design or a design mistake that is not severe enough to prevent you from compiling the design.
- An error message indicates a problem that the compiler cannot resolve. You cannot compile a design that contains consistency errors.

By default, the compiler displays a summary of warning messages. You can set an option to suppress the warnings messages and display only error messages. You can also set options that control the kinds of checking that the compiler performs.

To check a design,

1. Choose Design > Check Design.

The Check Design dialog box opens.

2. To display only error messages, select Suppress option.

3. If you want to check the design for annotated information in a links-to-layout flow, select the Check for correct back annotation option.

This information is annotated on the design after it is placed and routed. You can use this option to validate the back-annotation part of the links-to-layout flow.

4. If you want to check only the annotated information in the links-to-layout flow, select the Do not check design itself option.

This option is available only when the Check for correct back annotation option is selected.

5. Select a hierarchy option.

You can check just the current hierarchy level or check all levels of the design hierarchy.

6. Click OK or Apply.

---

## Checking Design Timing

You can check the attributes placed on the current design for timing problems. The compiler checks the design and displays any warnings in the console log view. For details about the timing check warning messages, see the `check_timing` man page.

To check timing attributes in the current design,

1. Choose Timing > Check Timing.

The Check Timing dialog box appears.

2. The name of the current design appears in the Current design text box.

3. If you want to check the master-slave clock overlap, enter a value in the Minimum allowed distance between master close edge and slave open edge text box.

The value you enter is the minimum distance that is allowed between the master and slave clock edges. When the compiler makes this check, it issues a warning if the distance is less than this value.

4. Click OK or Apply.

---

## Adding Levels of Hierarchy

You can combine cells or instances to create a new subdesign in the current design. This creates a new level of hierarchy in the current design. You can group

- A list of cells

You must group control logic cells (designated as type "c" in the cell report) with the cells they control.

- All combinational cells

A cell is combinational if it is a leaf or library cell and Boolean functions have been specified for its output pins.

- All cells in PLA specification blocks

When your design contains PLA blocks, you can combine the PLA specifications into a new level of hierarchy.

- All cells in FSM designs

When your design contains cells that are part of a finite state machine design, you can group the cells into a new level of hierarchy that is suitable for finite state machine extraction. You must specify the sequential elements used to store the state of the finite state machine first, by using the `set_fsm_state_vector` command.

Combinational cells in the transitive fanin or fanout of the state vector cells are included in the new level of hierarchy; however, non-combinational cells are not included. After grouping the cells, you can extract the new design into a state table format.

You can also specify an exception list to exclude certain cells from the group.

You must specify a unique design name for the design that contains the new level of hierarchy. You can also specify a new instance name for the design. If not, Design Vision tool generates a new instance name by combining the prefix set by the `unique_cell_prefix` attribute on the current design and an integer that assures a unique name within the current design.

To add a new level of hierarchy, Design Vision tool

- Replaces grouped cells or instances with a new instance that references the new subdesign
- Names the ports of the new subdesign after the nets to which they are connected in the design
- Determines the direction of each port of the new subdesign by the directions of the pins on the corresponding net

You can group the hierarchy below a newly grouped block by setting the current design to the newly created design (the grouped block) and then grouping the lower level of the hierarchy.

To group cells into a new subdesign,

1. Choose Hierarchy > Group.

The Group dialog box appears.

2. The Current design text box displays the name of the current design.
3. Identify the type of cells you want to group by performing one of the following:
  - To group a list of cells, select the Cells option.
  - To group combinational cells, select the Combinational logic option.
  - To group cells in PLA specification blocks, select the PLA option.

**Note:**

To group combinational gates in the PLA output, select the Combinational logic option.

- To group cells in FSM designs, select the FSM option.
4. If you selected the Cells option in step 3, specify one or more cell names by performing one of the following:
    - Enter the cell names in the Cells text box (use blank spaces to separate names).
    - Click the  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
    - Select one or more cells, then click the Selection button.
  5. (Optional) To exclude one or more cells from the group, specify the cell names by performing one of the following:
    - Enter the cell names in the Cells text box (use blank spaces to separate names).
    - Click the  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
    - Select one or more cells, then click the Selection button.
  6. Make sure the Hard (change hierarchy) option is selected.
  7. Enter a name for the new subdesign in the New design name text box.

8. (Optional) If you need to specify a new cell name for the instance, enter the name in the New cell name text box.

If you do not enter a new cell name, the tool generates one for you based on the format `Un`, where `U` is the value set for the `unique_cell_prefix` attribute and `n` is an unused cell number.

9. Click OK or Apply.

### See Also

- [Adding Placement Groups](#)
- [Removing Levels of Hierarchy](#)
- [Creating Uniquely Named Copies of a Design](#)

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## Adding Placement Groups

You can use the Group dialog box to combine cells or instances to create a placement group for use with physical implementation tools. When you create a new placement group, Design Vision sets the `group_name` attribute on the cells but does not create a new level of hierarchy in the current design. You can group

- A list of cells
  - You must group control logic cells (designated as type "c" in the cell report) with the cells they control.
- All combinational cells
  - A cell is combinational if it is a leaf or library cell and Boolean functions have been specified for its output pins.
- All cells in PLA specification blocks
- All cells in FSM designs

You can also specify an exception list to exclude certain cells from the group.

You can specify a unique name for the group. If you do not specify a name, the tool generates a group name by combining the prefix set by the `unique_cell_prefix` attribute on the current design and an integer that assures a unique name within the current design.

To create a group of cells for placement,

1. Choose Hierarchy > Group.

The Group dialog box appears.

2. The Current design text box displays the name of the current design.
  3. Identify the type of cells you want to group by performing one of the following:
    - To group a list of cells, select the Cells option.
    - To group combinational cells, select the Combinational logic option.
    - To group cells in PLA specification blocks, select the PLA option.
- Note:**
- To group combinational gates in the PLA output, select the Combinational logic option.
- To group cells in FSM designs, select the FSM option.
4. If you selected the Cells option in step 2, specify one or more cell names by performing one of the following:
    - Enter the cell names in the Cells text box (use blank spaces to separate names).
    - Click the  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
    - Select one or more cells, then click the Selection button.
  5. (Optional) To exclude one or more cells from the group, specify the cell names by performing one of the following:
    - Enter the cell names in the Cells text box (use blank spaces to separate names).
    - Click the  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
    - Select one or more cells, then click the Selection button.
  6. Select the Soft (set group name attribute) option.
  7. (Optional) To specify a group name, enter the name in the New group name text box.  
If you do not enter a new group name, the tool generates one for you based on the format `Un`, where `U` is the value set for the `unique_cell_prefix` attribute and `n` is an unused cell number.
  8. Click OK or Apply.

To remove `group_name` attributes, use the `ungroup -soft` command or the `remove_attribute` command.

## See Also

- [Adding Levels of Hierarchy](#)
- 

## Removing Levels of Hierarchy

You can remove (collapse) the level of hierarchy for a subdesign by ungrouping the cell and merging it with the surrounding logic. You can ungroup

- Selected cells
- All hierarchical cells in the current design
- All hierarchical cells that contain less than a certain number of leaf cells

You can select options to

- Use simple, non-hierarchical names for the ungrouped cells  
By default, Design Vision tool assigns default hierarchical names.
- Force the tool to flatten cells that have been assigned the `dont_touch` attribute
- Specify a hierarchy level below which you want the tool to recursively remove all levels of hierarchy

When you ungroup selected cells, you can either remove just one level of hierarchy in each cell or recursively remove all levels of hierarchy in the cells. In addition, you can specify the prefix you want the tool to use when naming the ungrouped cells.

To ungroup selected cells,

1. Select the cells you need to ungroup.
2. Choose **Hierarchy > Ungroup** to open the Ungroup dialog box.
3. Make sure the **Selected Cells** option is selected.
4. Remove levels of hierarchy by performing one of the following:
  - To remove just the first level of hierarchy under the selected cell, select the **Ungroup one level** option.
  - To remove all the hierarchy levels under the selected cell, select the **Ungroup all levels** option.
5. (Optional) To remove only the hierarchy levels below a certain level, select the **Start level** option and enter or select a level number in the **Start level** text box.
6. (Optional) To specify a prefix for the names of the ungrouped cells, enter the prefix in the **Cell name prefix** text box.

By default, the tool applies prefixes composed of the old cell name and a number. If you want to retain a vestige of the former hierarchy, do not enter a prefix if you selected the Ungroup all levels option.

7. Set other options as needed.
  - To use simple, non-hierarchical names for the ungrouped cells, select the Simple names option.
  - To flatten hierarchical cells that are assigned the `dont_touch` attribute, select the Force option.
8. Click OK or Apply.

To ungroup all hierarchical cells in the current design,

1. Choose Hierarchy > Ungroup to open the Ungroup dialog box.
2. Select All.
3. (Optional) To remove only the hierarchy levels below a certain level, select the Start level option and enter or select a level number in the Start level text box.
4. Set other options as needed.
  - To use simple, non-hierarchical names for the ungrouped cells, select the Simple names option.
  - To flatten hierarchical cells that have been assigned the `dont_touch` attribute, select the Force option.
5. Click OK or Apply.

To ungroup all hierarchical cells that contain less than a certain number of leaf cells,

1. Choose Hierarchy > Ungroup to open the Ungroup dialog box.
2. Select the Small cells option.
3. Enter the number of leaf cells in the Small cells text box.
4. Set other options as needed.
  - To use simple, non-hierarchical names for the ungrouped cells, select the Simple names option.
  - To flatten hierarchical cells that have been assigned the `dont_touch` attribute, select the Force option.
5. Click OK or Apply.

## See Also

- [Adding Levels of Hierarchy](#)
- [Creating Uniquely Named Copies of a Design](#)

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## Creating Uniquely Named Copies of a Design

In a hierarchical design, subdesigns are sometimes referenced by more than one cell instance. If the environment around the instances of a multiply referenced design differ significantly, you can resolve the multiple references by creating a uniquely named copy of a multiply referenced design for each instance.

You can create unique copies of all multiply referenced designs throughout the hierarchy of a design (except for designs that have the `dont_touch` attribute) or just for selected cells.

**Note:**

In earlier releases, you had to manually create uniquely named copies of multiply referenced designs before performing design optimization. However, beginning with version V-2004.06, the compiler automatically creates the uniquely named copies as part of the compile process. For details, see the *Design Compiler User Guide*.

To copy and rename subdesigns throughout the hierarchy of a design,

1. Choose Hierarchy > Uniquify > Hierarchy.  
The Uniquify Hierarchy dialog box appears.
2. Enter or select the name of the design name in the Cell reference name text box.
3. Enter the base name for the new reference names in the Base name for new designs text box.
4. (Optional) If you want to rename designs that are already unique or that have been assigned the `dont_touch` attribute, select the Instances to be renamed even if unique or assigned `dont_touch` option.
5. Click OK or Apply.

To copy and rename designs for selected cells,

1. Choose Hierarchy > Uniquify > Cells.  
The Uniquify Cells dialog box appears.

2. Specify one or more cell names by performing one of the following:
  - Enter the cell names in the Cells text box (use blank spaces to separate names).
  - Click the  button and select cell names in the Object Chooser dialog box.
  - Select one or more cells, then click the Selection button.
3. Specify a new design name or base name.
  - If you specified a single cell, enter a new design reference name in the New design name text box.
  - If you specified multiple cells, enter a base name for the new design reference names in the Base name for new designs text box.
4. (Optional) If you want to rename designs that are already unique or that have been assigned the `dont_touch` attribute, select the Instances to be renamed even if unique or assigned `dont_touch` option.
5. Click OK or Apply.

### See Also

- [Adding Levels of Hierarchy](#)
- [Removing Levels of Hierarchy](#)

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## Optimizing the Design

You can use Design Vision tool to perform logic and gate-level synthesis and optimization on the current design and its subdesigns. During optimization, incremental status reports are displayed in the console log view each time a transformation is applied to the design. These reports include the elapsed time, area, worst negative slack, total negative slack, design rule cost, and endpoint.

To control the optimization process, you can

- Set the relative design mapping and area recovery efforts
- Set compile options
- Set design rule options
- Set background compilation options to run the compiler in the background or across the network on another machine

If you are using TestMAX DFT, you can set a compile option that performs a test-ready compile by replacing all sequential elements with scan-equivalent cells.

For more information about optimization strategies and how design optimization works, see the *Design Compiler User Guide*.

To optimize the current design and its subdesigns,

1. Choose Design > Compile Design.

The Compile Design dialog box appears. For details about the individual options in this dialog box, see [Compile Design \(Design Menu\)](#).

2. Select the mapping options you need to control the relative efforts for design mapping and area recovery.
  - Select a Map effort option: medium or high. The default is medium.
  - Select an Area effort option: none, low, medium, or high. The default is high.

**Note:**

If you want the compiler to use generic Boolean equations and generic flip-flops to represent the optimized design instead of mapping the design to the technology library, deselect Mapping options.

3. Select the compile options you need to use.
  - To fix design rule and top-level timing violations, select the Top level option.
  - To map the circuit by using only local mapping transformations that improve the circuit, select the Incremental mapping option.
  - To remove all levels of hierarchy in the design (except for subdesigns assigned the `dont_touch` attribute), select the Ungroup all option.
  - To optimizes the design across all hierarchical boundaries, select the Allow boundary conditions option.
  - To enable the compiler to automatically remove levels of hierarchy in the design, select the Auto ungroup option and select either Area (to improve area recovery in small designs) or Delay (to improve overall design timing).
  - To exactly match sequential elements with their descriptions in the HDL code (for designs that contain SEQUEM elements), select the Exact map option.
4. (Optional) If you are using TestMAX DFT and need to perform a test-ready compile, select the Scan option.
5. (Optional) If you need to control whether and how the compiler fixes design rule violations, select the appropriate design rule option.

- If you want the compiler to fix design rule violations during design optimization, select the Fix design rules and optimize mapping option.
- If you do not want the compiler to fix design rule violations, select the Optimize mapping only option.
- If you want the compiler to fix design rule violations without optimizing the design, select the Fix design rules only option.
- If you want the compiler to fix hold time violations for clocks that is assigned the `hold_fix` attribute (and ignore all other design rule violations) during design optimization, select the Fix hold time only option.

When you select this option, the compiler attempts to fix `hold_fix` attribute violations if the delay (setup) cost is not increased or if hold violations is given a higher priority than maximum delay cost. For details about attribute priorities, see the `set_cost_priority` man page. For details about the `hold_fix` attribute, see the `set_fix_hold` man page.

6. (Optional) If you want to run the compiler in the background or on a remote system, select the Background option and enter the path to the run directory and the host name of the remote system, and select the architecture type of the remote system.
7. (Optional) If you selected the Background option and you want to display the compiler results on the X-terminal, select the Xterm Window option. This option is valid only in the X11 environment.
8. Click OK or Apply.

## See Also

- [Compile Design \(Design Menu\)](#)
- [Optimizing Critical Delays](#)

## Optimizing Critical Delays

If you have a DC-Ultra license and a DesignWare Foundation license, you can use the Compile Ultra command to perform critical delay optimization on timing-critical high-speed designs. During optimization, the compiler performs a two-pass high-effort flow on the current design for better delay QoR.

Compile Ultra provides a push-button solution for timing-critical, high performance designs. It allows you to apply the best possible set of timing-centric variables for critical delay optimization as well as improvement in area QoR.

**Note:**

This command requires a DC-Ultra license and a DesignWare Foundation license.

You can use the Compile Ultra dialog box to,

- Select the compile options for the type of optimization you need to perform.

For details about the individual compile options, see [Compile Ultra \(Design Menu\)](#).

- Select an option to control design rule fixing.

You can fix design rule violations without mapping the design, or you can perform design optimization without fixing design rule optimization. By default, the compiler attempts to fix design rule violations during design optimization.

- Select a timing or area high effort synthesis option

Each option runs a script that attempts to improve optimization but might increase runtime.

If you are using TestMAX DFT, you can select an option that performs a test-ready compile by replacing all sequential elements with scan-equivalent cells.

To perform critical delay optimization on the current design and its subdesigns,

1. Choose Design > Compile Ultra.

The Compile Ultra dialog box appears.

2. Select the Compile options as needed.

- To fix design rule and top-level timing violations for paths that cross hierarchical boundaries, select the Top level option.
- To prevent optimization across hierarchical boundaries, select the No hierarchical boundary optimization option.
- To perform a test-ready compile, select the Scan option.
- To perform clock gate optimization (by automatically inserting or removing clock gates), select the Gate Clock option.
- To prevent the compiler from inverting sequential elements during mapping and optimization, select the No sequential output inversion option.
- To perform incremental improvements on the gate structure without remapping the design, select the Incremental mapping option.

In topographical mode, using this option with results only in placement-based optimization of the topographical netlist.

- To disable all automatic ungrouping operations and preserve all user hierarchies during optimization, select the No auto ungroup option.
- To force the compiler to match the sequential elements in the optimized design with the descriptions specified in the HDL code, select the Exact map option.

If your design contains SEQUEM elements, select this option when you need to force the compiler to search the target libraries. This matches only the behavior of the SEQUEM elements (without considering the surrounding logic). If an exact match is not available, another sequential element is used.

- To improve worst negative slack by performing local retiming moves (adaptive retiming) during optimization, select the Retime option.

3. If necessary, select a design rule option.

The Fix design rules and optimize mapping option is selected by default, which means the compiler attempts to fix design rules during design optimization.

- To prevent the compiler from fixing any design rule violations during design optimization, select the Optimize mapping only option.

This option allows you to view the violations in a constraint report before fixing them. For details, see [Reporting Constraint Violations](#).

- To force the compiler to fix design rule violations without performing design optimization, select the Fix design rules only option.

4. If necessary, select a high effort synthesis option.

The Dont use timing and Area scripts option is selected by default, that is, the compiler uses the default timing and area effort.

- To enable a strategic optimization process that attempts to improve delays but might increase runtime, select the Use timing script option.

This process can include changes to variables or constraints that modify compile\_ultra behavior and additional passes to achieve better timing results.

- To enable a strategic optimization process that attempts to improve area but might increase runtime, select the Use area script option.

This process can include changes to variables or constraints that modify compile\_ultra behavior and additional passes to achieve better area results.

5. Click OK or Apply.

### See Also

- [Compile Ultra \(Design Menu\)](#)
- [Optimizing the Design](#)
- [Using Design Vision Tool in Topographical Mode](#)

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## Working With Reports

Textual reports are available from the Design menu and the Timing menu. Use Design menu commands to generate design information and design object reports. Use Timing menu commands to generate timing and constraint reports. If these menus do not have the report you need, you can generate any Design Compiler report by issuing `dc_shell` report commands on the command line.

- When you generate a report by choosing a menu command, the GUI opens a new report view and displays the report in both the report view and the console log view.  
If an empty report view is open, the GUI displays the report in that report view instead of opening a new report view.
- When you generate a report by entering the report command on the command line or by running a script, the GUI displays the report in the console log view.  
If an empty report view is open, the GUI also displays the report in the report view.

You use the report view to view report information and select reported objects. You can search for text in a report view. You can also save or append a report in a file or load a report from a file. Use the buttons at the top of the report view window to clear the view (remove the report text), save the report in a text file, display a report saved in a text file, and find text in a report.

In reports that list object names, such as design, cell, net, port, and worst-path timing reports, you can select an object by clicking its name (blue text) in the report view. The GUI displays the schematic for the design in which the object is located and magnifies the schematic to fit the selected object in the view. The name of the selected object also appears in the selection list, and the object is displayed in the selection color, which is white by default, in all schematic and layout views.

For more information about reports and the report view, see the following topics:

- [Viewing Reports](#)
- [Generating Object Reports](#)
- [Selecting Objects in the Object Chooser](#)

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## Viewing Reports

Design Vision tool displays reports in report views. You can use a report view to

- View a report and search for text
- Save the report in a file
- View a report from a file

When you generate a report by choosing a report command on a menu, the GUI opens a new report view to display the report. The GUI provides report commands on the Design menu and the Timing menu.

- Use Design menu commands to generate design information and design object reports.
- Use Timing menu commands to generate timing and constraint reports.

These commands open dialog boxes in which you can set report options and output options. You can

- Display the report in a report view
- Save the report in a file
- Append the report to a file

When you use a menu command to display a report, Design Vision tool opens a new report view and displays the report in both the report view and the console log view.

When you display a report by entering the report command on the command line or by running a script, Design Vision tool displays the report in the console log view. If an empty report view is open, Design Vision tool also displays the report in the empty report view. An empty report view is a new report view that you open by choosing Window > New Report View or a report view in which you have removed the report text.

To remove a report from a report view,

- Click the  button.

To save a report displayed in a report view,

1. Click the  button.

The Save Report to File dialog box appears.

2. Select a file or enter a file name in the File name text box.

If the file already exists, Design Vision tool overwrites it.

3. Click Save.

To open a report saved in a file,

1. Make sure the report view is empty.

2. Click the  button.

The Open Report to File dialog box appears.

3. Select the file or enter its name in the File name text box.

4. Click Open.

To find text in a report,

1. Type the text in the text box at the top of the report view.

2. Click the  button. You can select the names of design objects that you want to view in a schematic. The first time you click an object name (blue text) in a cell, net, port, or worst-path timing report, Design Vision tool.

- Selects the object
- Opens a new schematic view window
- Displays the schematic for the design instance (hierarchical cell) in which the object is located
- Magnifies the design to fit the object in the view

If you click other object names in the report, or in other reports or report views, Design Vision changes the schematic view to display and fit the selected object.

**Note:**

If you close the schematic view window, Design Vision tool opens a new window the next time you select an object in a report view.

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## Generating Object Reports

You can generate a report for one or more selected cells, ports, or nets. The GUI displays the report in a report view. You can also select objects in a report view that you want to examine in a schematic view.

To generate a report for one or more objects of the same type,

1. Select the objects.
2. Choose the appropriate report command in the Design menu.  
The associated report dialog box appears.
3. Click Selection in the report dialog box.  
The names of the selected objects appear.
4. Set other report options as needed.
5. Click OK.

If you click an object name (blue text) in the report view, the GUI selects the object in a schematic view and magnifies the schematic to fit the object in the view window.

## Reporting Area Information

You can generate a report that contains area information and statistics for the design of the current instance, if set, or for the current design. If the design is a block abstraction, the report also contains area information and statistics for the original design from which the block abstraction is created.

The report lists

- The names of the libraries linked to the design
- The number of ports, cells, nets, references, combinational areas, non-combinational areas, and net interconnect areas in the design
- The total area of the design

The report also provides information messages about the design, such as a message that the design contains unmapped logic or that it contains black box components.

To report area information,

1. Choose Design > Report Area.

The Report Area dialog box appears. The name of the current design appears in the Current design text box and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options to control the report content.
  - To prevent line splitting, deselect the Split line option.
  - To include the area used by cells across the design hierarchy, select the Hierarchy option.

When this option is selected, the report includes the absolute value and the percentage of the area used by each of the cells across the design hierarchy. It also includes details about the area used by combinational, non-combinational, and macro and black box cells.

- To include the area of Synopsys DesignWare® synthetic module, select the Show Designware option.

When this option is selected, the report includes the total synthetic module area and the total datapath cell area. If the tool ungrouped the synthetic modules during optimization, the report includes the estimated area of the ungrouped cells.

- To include the area and aspect ratio of the core area, select the Show physical information option.

### 3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

### 4. Click Apply or OK.

For more information about the area report and the report options, see the man page for the `report_area` command.

## Reporting Cell Information

You can generate a report that contains information about a specific cell or set of cells, including

- Corresponding cell reference (the library cell name)
- Name of the library that contains the cell
- Area of the cell
- Connectivity information

To report cell information,

1. Choose Design > Report Cells.

The Report Cells dialog box appears.

2. Specify one or more cell names by performing one of the following:

- Enter the cell names in the Cells text box (use blank spaces to separate names).
- Click the Object Chooser  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
- Select one or more cells, then click the Selection button.

3. Set other options that control the report content.

- To disable line splitting, deselect the Split line option.
- To include all available cell connection information, select the Verbose option.
- To include the orientations and locations of the cells, select the Show physical information option.
- To include the information about physical-only cells, select the Show physical only cells option.
- To include information about input and output pins and their connected nets, select the Show cell connections option.
- To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits box.

This number must be an integer between 0 and 13. The default is 2. This option overrides the `report_default_significant_digits` variable.

4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.

- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

5. Click OK or Apply.

For more information about the cell report and the report options, see the man page for the `report_cell` command.

## Reporting Clock Information

You can generate a report that contain clock-related information for the current design. The clocks report contains design information about each clock, including

- Clock names
- Rise and fall times
- Skew type
- Attributes

To generate a report of design-related information about each clock in the current design,

1. Choose Design > Report Clocks.

The Report Clocks dialog box appears. The name of the current design appears in the Current design text box.

2. Set the report options to control the report content.

- To prevent line splitting, deselect the Split line option.
- To list all clocks in the design and include the clock name, period, waveform, source, and clock attributes for each clock, select the Show Attribute option.
- To include the clock network skew information set on the design by the `set_clock_uncertainty` command, select the Show Skew option.

This information includes the rise and fall delays and the plus and minus uncertainty of the clock network.

- To include the clock group information set on the design by the `set_clock_groups` command, select the Show Groups option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Clock Network Skew Information

You can generate a timing report that contains clock network skew information for the current design, including the rise and fall delays and the plus and minus uncertainty of the rise and fall delays.

To generate a timing report of clock network skew information,

1. Choose Timing > Report Clock Skew.

The Report Clock Skew dialog box appears. The name of the current design appears in the Current design box.

2. To disable line splitting, select the No line split option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the clock skew report and the report options, see the man page for the `report_clock` command.

## Reporting Clock Tree Fanout Information

You can generate a timing report that contains information about the clock tree fanout network for every clock source in the current design. If there are no clocks in the design, or if the clocks have no sources, the clock tree report is empty.

To generate a timing report of clock tree fanout information,

1. Choose Timing > Report Clock Tree.

The Report Clock Tree dialog box appears. The name of the current design appears in the Current design text box.

2. To disable line splitting, select the No line split option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the clock tree report and the report options, see the man page for the `report_clock_tree` command.

## Reporting Compile Options

You can generate a report of compile options for the current instance, if set, or for the current design. This report lists the compilation options (flatten, structure, structure\_boolean, or structure\_timing) and their values (true or false) for the design and each subdesign in the design hierarchy.

To generate a report of compile options,

1. Choose Design > Report Compile Options.

The Report Compile Options dialog box appears. The name of the current design appears in the Current design text box. If you have set the current instance, its name appears in the Current instance text box.

2. (Optional) Disable line splitting by selecting the No line split option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Constraint Violations

You can generate a report that provides information about design rule and optimization constraint violations in the current design. For each constraint, the report includes information about

- If the constraint is violated or met, and by how much
- Which design object is the worst violator

By default, the report includes information about all design rule and optimization constraints in the design. You can limit the report to one or more types of constraints by selecting the options for those constraint types.

If you are using the Power Compiler tools, you can also limit the information about power constraints to dynamic power, leakage, or both.

### Note:

Queries for power constraint information require a Power-Optimization license and supporting libraries characterized for power. For details, see the *Power Compiler documentation*.

To generate a report about constraint violations,

1. Choose Design > Report Constraints.

The Report Constraints dialog box appears. The name of the current design appears in the Current design text box.

2. (Optional) Set options as needed to limit the report to information about certain types of design rule and optimization constraints.

Select one or more options for the types of constraint information you want to include.

- To include maximum capacitance constraint information, select the Show only maximum capacitance option.

Maximum capacitance is a design rule constraint (`max_capacitance`) that sets an upper limit for the total capacitance on a net.

- To include minimum capacitance constraint information, select the Show only minimum capacitance option.

Minimum capacitance is a design rule constraint (`min_capacitance`) that sets a lower limit for the total capacitance on a net.

- To include maximum delay and setup constraint information, select the Show only maximum delay option.

- To include minimum delay and hold constraint information, select the Show only minimum delay option.

- To include maximum dynamic power constraint information, but not other power constraint information, select the Show only maximum dynamic power option.

- To include maximum leakage power constraint information, but not other power constraint information, select the Show only maximum leakage power option.

- To include minimum porosity constraint information, select the Show only minimum porosity option.

Minimum porosity is an optimization constraint (`min_porosity`) for routability.

- To include maximum transition constraint information, select the Show only maximum transition option.

Maximum transition is a design rule constraint (`max_transition`) that sets an upper limit for the transition time on a net.

- To include maximum fanout constraint information, select the Show only maximum fanout option.

Maximum fanout is a design rule constraint (`max_fanout`) that limits the fanout load on a net.

- To include maximum area constraint information, select the Show only maximum area option.

- To include cell degradation constraint information, select the Show only cell degradation option.

Cell degradation is a design rule constraint (`cell_degradation`) that limits the total capacitance on a net. The total capacitance that can be driven by a cell is a function of the transition times at the inputs of the cell.

- To include connection class constraint information, select the Show only connection class option.

The connection class constraint (`connection_class`) is included only when a connection class violation has occurred.

- To include multiple port nets constraint information, select the Show only multiport nets option.

The multiple port nets constraint (`multiport_net`) is included only when the `set_fix_multiple_port_nets` variable is set to none (the default).

- To include critical range constraint information, select the Show only critical range option.

Critical range is a design rule constraint (`critical_range`) that enables optimization of near critical paths in addition to the most critical path.

- To include maximum toggle rate constraint information, select the Show only maximum toggle rate option.

- To include maximum net length constraint information, select the Show only maximum net length option.

- To include maximum total power constraint information, select the Show only maximum total power option.

- To include minimum pulse width constraint information, select the Show only minimum pulse width option.

Minimum pulse width is a design rule constraint (`min_pulse_width`) that limits the minimal length of clock pulses in the clock network.

3. (Optional) To include constraint information for specific scenarios in a multiscenario design, enter the scenario names in the Scenarios text box.

The report lists the constraint information separately for each scenario and does not include constraint information for inactive scenarios.

By default, the report includes constraint information for all active scenarios in the design. However, if you select the Verbose option or the Show all violators option and do not specify any scenarios, the report includes constraint information for the current scenario only.

4. Set other report content options as needed.

- To disable line splitting, deselect the Split line option.
- To include additional information about constraint calculations, select the Verbose option.

If you also select the Show all violators option, the Verbose option provides detailed information about constraint violations.
- To display a summary of all violated design rule and optimization constraints in the current design, select the Show all violators option.

If you also select the Verbose option, the Show all violators option provides detailed information about constraint violations.
- To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits text box.

This number must be an integer between 0 and 13. The default is 2.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

For more information about the constraint report and the report options, see the man page for the `report_constraint` command.

## Reporting Datapath Extraction Analysis

You can analyze the datapath extraction of the current design and view a report of the resources contained in the design. This report can help you to find the resources in the design RTL. You can click the link for an arithmetic operator in the report to view the RTL in the RTL browser.

After reading in the RTL, you can generate a datapath extraction report of the resources contained in the current design and view the report in the HTML report view. This report

can help you to find the resources in the design RTL. You can click the link for an arithmetic operator in the report to view the RTL in the RTL browser.

**Note:**

The datapath names in this report might differ from the datapath names in the design resources report. However, the names of the resources are the same in both reports.

You can use the datapath extraction report to examine how the datapath blocks are extracted from your RTL before you optimize the design. The tool analyzes the arithmetic contents of the design and provides feedback for improving the RTL code.

To get the best QoR results from datapath optimization, it is a must that the biggest possible datapath blocks are extracted from the RTL code. When the tool detects an arithmetic operator that is not extracted, it reports the information about what is blocking the datapath extraction, including the file name of the RTL and the line number of the operator it is inferred from.

See [SolvNet article 015771, “Coding Guidelines for Datapath Synthesis”](#) for information about coding styles to help improve datapath extraction.

To report datapath extraction,

1. Choose Design > Analyze Datapath Extraction, or choose AnalyzeRTL > Analyze Datapath Extraction.

The Analyze Datapath Extraction dialog box appears. The name of the current design appears in the Current design text box and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options as needed.

- To disable all automatic ungrouping operations and preserve all user hierarchies during datapath extraction analysis, deselect the Auto Ungroup option.

Deselecting this option has the same effect as selecting the No auto ungroup option in the Compile Ultra dialog box. If you disabled automatic ungrouping when you ran the `compile_ultra` command, you should also disable automatic ungrouping when you analyze datapath extraction.

- To sort the leakage detection messages in each design based on their potential impact, from high to low, select the Sort message option.
- To enable message filtering, select a message severity level option: Low or Medium.

The tool filters out messages with severity levels that are less than or equal to the severity level that you select. By default, the None option is selected, which means message filtering is disabled.

- To set the maximum number of leakage detection messages to include for each design, enter the number in the Maximum messages text box.

### 3. Set output options as needed.

By default, Design Vision tool displays the report in the HTML report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

### 4. Click OK or Apply.

The tool runs the `analyze_datapath_extraction` command and displays the report in a new HTML report view window.

The HTML report provides direct links to the RTL file. If you click the RTL file name link for an arithmetic operator, the tool opens a new RTL browser window by default and highlights the line number that contains the origin of the corresponding operator in the RTL file. For more details, see [Cross-Probing Synthetic Operators in a Datapath Extraction Report](#).

For more information about the datapath extraction report and the report options, see the *Design Compiler User Guide* and the man page for the `analyze_datapath_extraction` command.

### See Also

- [Cross-Probing Synthetic Operators in a Datapath Extraction Report](#)
- [Examining Cells in the RTL Browser](#)

## Reporting Design Hierarchy Information

You can generate a report that displays the reference hierarchy for the design of the current instance, if set, or for the current design.

You can control whether the report provides single listings for the hierarchies of each subdesign or multiple listings for subdesigns that occur at multiple locations in the design hierarchy.

To report design hierarchy information,

1. Choose Design > Report Design Hierarchy.

The Report Design Hierarchy dialog box appears. The name of the current design appears in the Current design text box. The name of the current instance, if it is set, appears in the Current instance text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
- To include multiple listings for subdesigns that occur at multiple locations in the design hierarchy, select the List all instances option.

The List first instance option is selected by default, that is the report lists subdesign once and uses and ellipsis (...) to indicate the contents of a previously displayed module.

- To exclude leaf cells from the report, deselect the Show leaf level cells option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the hierarchy report and the report options, see the man page for the `report_hierarchy` command.

## Reporting Design Information

You can generate a report that contains a summary of attributes on the current design. The report lists the libraries, flip-flop types, and latch types used in the design. It also

includes information about operating conditions, the wire load model, pin input and output delays, disabled timing arcs, required licenses, and design parameters.

To generate a report about the current design,

1. Choose Design > Report Design.

The Report Design dialog box appears. The name of the current design appears in the Current design box.

2. Set report options to control the report content.

- To prevent line splitting, deselect the Split line option.
- To include physical-only attributes, select the Show physical option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Design Reference Information

You can generate a report that displays information about the references in the design of the current instance, if set, or for the current design. The report lists the reference name, library name, unit area per instance, number of instances, total area, and attributes for each reference in the design.

To report design reference information,

1. Choose Design > Report Reference.

The Report Reference dialog box appears. The name of the current design appears in the Current design text box, and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
  - To include information about references across the design hierarchy, select the Show Hierarchy references option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the references report and the report options, see the man page for the `report_reference` command.

## Reporting Design Resources

You can generate a report that contains information about resources used in the current instance or the current design. A resource is an arithmetic or comparison operator read in as part of the HDL design. Resources can be shared during compile operations. The report includes information about shared resources, parameters used to build the module, and user-declared resources in each module. You can click the link for a cell in the report to view the RTL in the RTL browser.

To report resources used in the current instance or the current design,

1. Choose Design > Report Design Resources.

The Report Design Resources dialog box appears. The name of the current design appears in the Current design text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
- To list resources from all subdesigns in the hierarchy, select the Show resources for subdesigns option.

By default, only resources used in the top-level design are listed.

- To include context information from the DesignWare generator, select the Show Context Information option.

By default, only the power context information is included.

- To include only the DesignWare cells that are optimized for the minimum power flow, select the Show resources with Minimum power option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

The tool runs the `report_resources` command and displays the report in a new HTML report view window.

The HTML report provides direct links to the RTL file. If you click the RTL file name link for a cell, the tool opens a new RTL browser window by default and highlights the line number that contains the origin of the corresponding cell in the RTL file. For more details, see [Cross-Probing Cells in a Design Resources Report](#).

For more information about the design resources report and the report options, see the man page for the `report_resources` command.

## See Also

- [Cross-Probing Cells in a Design Resources Report](#)
- [Examining Cells in the RTL Browser](#)

## Reporting Net Information

You can generate a report that contains information about a specific net or set of nets, including:

- Fanout and fanin
- Capacitance and resistance
- Pins
- Net connections

To report net information,

1. Choose Design > Report Nets.

The Report Nets dialog box appears.

2. Specify one or more net names by doing one of the following:

- Enter the net names in the Nets text box (use blank spaces to separate names).
- Click the Object Chooser  button and select net names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
- Select one or more nets, then click the Selection button.

3. Set other options that control the report content.

- To disable line splitting, deselect the Split line option.
- To include all available net connection information, select the Verbose option.
- To include net information only for the current instance (and not for other levels of the logic hierarchy), select the Do not trace hierarchy option.
- To include cell depreciation data at the end of the report, select the Show cell degradation values option.

Cell depreciation data consists of the capacitance on the net, the limit for the capacitance on the net (calculated from the cell depreciation tables for the drivers of the net), and the violation on the net.

- To include information about input and output pins and their connected nets, select the Show net connections option.
- To include the rise and fall transition times for each net at the end of the report, select the Show rise and fall transitions option.
- To report minimum capacitance, resistance, or transition values (instead of maximum values), select the Show minimum values option.

- To include the maximum toggle rate values for each net, select the Show maximum toggle rate values option.
- To include the total wire length of the net, and the preroutes if preroute information exists, select the Show physical information option.
- To include the preroutes of the physical net, select the Show preroute information only for physical nets option.
- To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits drop-down.

This number must be an integer between 0 and 13. The default is 2. This option overrides the `report_default_significant_digits` variable.

4. (Optional) To include the timing derate for specific scenarios in a multiscenario design, enter the scenario names in the Scenarios text box.

The report lists the timing derate separately for each scenario and does not include the timing derates for inactive scenarios.

By default, the report includes the timing derate for the current scenario only.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

7. For more information about the net report and the report options, see the man page for the `report_net` command.

## Reporting Path Groups

You can generate a report that contains information about path groups in the current design. This report identifies each path group in the current design and lists the weight and critical range for each path group.

To generate a report about path groups in the current design,

1. Choose Timing > Report Path Groups.

The Report Path Group dialog box appears. The name of the current design appears in the Current design text box.

2. (Optional) Disable line splitting by selecting the No line split option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Port Information

You can generate a report that contains information about ports in the design, including

- Port name and direction
- Connections
- Pin capacitance
- Wire capacitance
- Attributes

To report port information,

1. Choose Design > Report Ports.

The Report Ports dialog box appears.

2. Specify one or more port names by doing one of the following:
  - Enter the port names in the Ports text box (use blank spaces to separate names).
  - Click the  button and select port names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
  - Select one or more ports, then click the Selection button.
3. Set other options that control the report content.
  - To disable line splitting, deselect the Split line option.
  - To include all available port information, select the Verbose option.
  - To include only the report sections that show the capabilities of the input and output ports, select the Show only input port drive option.
  - To include information about physical-only ports, select the Show only physical information option.
  - To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits text box.  
This number must be an integer between 0 and 13. The default is 2. This option overrides the report\_default\_significant\_digits variable.
  - To include the physical locations of the ports, select the Show physical information option.
4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

  - To prevent the report view from displaying the report, deselect the To report viewer option.
  - To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
  - To overwrite an existing file, deselect the Append to file option.  
By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.
5. Click OK or Apply.

For more information about the port report and the report options, see the man page for the `report_port` command.

## Reporting Power

You can generate a report that provides a summary of dynamic and static power for the current design. The report includes information about the internal power, net switching power, dynamic power, and cell leakage power used by the design.

**Note:**

The power constraints are used with the Power Compiler tool. Queries for power constraint information require a Power-Optimization license and supporting libraries characterized for power. For details, see the *Power Compiler documentation*.

The default power report provides a summary of power values for the design. You can set options to

- Include power information for individual objects (cells, nets, or both)  
You can include information for all the cells or nets in the design or for only those cells or nets you specify. You can also specify the maximum number of cells or nets to include.
- Include all available information for the cells or nets, including
  - The driver cell's internal and leakage power for each net
  - The contribution of each internal-power group to the internal power of each cell
- Include the cumulative power for each cell or net
- Exclude the power values for boundary nets
- Filter the report to include only a specified number of objects with the highest power values
- Include a histogram showing the range and distribution of power values

You can also set options to control

- The sorting order for cells or nets
- The analysis effort level
- Whether the report is formatted hierarchically, and the number of hierarchical levels to include
- Whether the report includes objects from all levels of the design hierarchy (as if it were flat) and whether lines in fixed-width columns can be split

The following sections show how to generate a summary power report and how to generate a power report that includes information for individual nets or cells.

To generate a summary power report,

1. Choose Design > Report Power.

The Report Power dialog box appears.

2. Make sure the Summary only report type is selected in the Report for drop-down list.

This option is selected by default.

3. Select an effort level option in the Analysis effort drop-down list.

The choices are low, medium, or high. The default is low.

The option you select sets the analysis effort in terms of the relative amount of CPU time spent on analysis. This option controls the depth of logic that is traversed to detect signal correlation. A higher effort means a longer runtime but higher accuracy. Variations in runtime and accuracy depend greatly on the circuit structure.

4. Make sure the other report options are set as you need them.

- To disable line splitting, select the No line split option.
- To include the cell counts of the power groups in the power group summary, select the Verbose option.
- To limit the report to a certain number of nets with the highest power values, enter a value in the Worst number text box.
- To exclude the power values for boundary nets, select the Exclude power of boundary nets option.

5. Set output options as needed.

By default, Design Vision tools displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click OK or Apply.

To generate a power report that includes information for individual nets or cells,

1. Choose Design > Report Power.

The Report Power dialog box appears.

2. Select a report type in the Report for drop-down list.

- Select Nets only to include information for individual nets.
- Select Cells only to include information for individual cells.
- Select Nets and cells to include information for individual nets and cells.

3. (Optional) To limit the report to specific nets or cells, select the Only nets/cells option and specify the net or cell names in one of the following ways:

- Enter the net or cell names in the Only nets/cells text box (use blank spaces to separate names).
- Click the  button and select net or cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
- Select one or more nets or cells, then click the Selection button.

The All nets/cells option is selected by default.

4. (Optional) To include a histogram of power values, select the Show nets histogram option.

You can limit the range of power values in the histogram:

- To set the lower limit, enter a value in the Exclude values <= text box.
- To set the upper limit, enter a value in the Exclude values => text box.

#### Note:

The Show nets histogram option is not available when you select the Use hierarchical format[z] option.

5. Select an effort level option in the Analysis effort drop-down list.

The choices are low, medium, or high. The default is low.

The option you select sets the analysis effort in terms of the relative amount of CPU time spent on analysis. This option controls the depth of logic that is traversed to detect signal correlation. A higher effort means a longer runtime but higher accuracy. Variations in runtime and accuracy depend greatly on the circuit structure.

6. (Optional) To control the sorting order for nets or cells in the report, select an option in the Sort mode drop-down list.

The available choices depend on whether you are generating a report for cells, nets, or both.

- For a cell report, the valid choices are

- name
- cell\_leakage\_power
- cell\_internal\_power
- dynamic\_power
- cumulative\_fanout
- cumulative\_fanin

- For a net report, the valid choices are

- name
- net\_switching\_power
- net\_toggle\_rate
- total\_net\_load
- net\_static\_probability
- cumulative\_fanout
- cumulative\_fanin

7. Set the other report options as needed.

- To format the report hierarchically, select the Use hierarchical format option and enter the number of hierarchy levels in the Hierarchy levels text box.
- To limit the report to a certain number of nets with the highest power values, enter a value in the Worst number text box.
- To disable line splitting, select the No line split option.
- To include all available net or cell information, select the Verbose option.
- To exclude the power values for boundary nets, select the Exclude power of boundary nets option.
- To calculate and list the cumulative power for every net or cell in the report, select the Report cumulative power[k] option.
- To traverse the design hierarchy and include objects at all lower levels (as if the design hierarchy were flat), select the Traverse hierarchy at all levels option.

8. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

9. Click OK or Apply.

For more information about the power report and the report options, see the man page for the `report_power` command.

## Reporting Timing Requirements

You can generate a report of information about timing requirements for the current design or for specific timing paths in the current design.

The default timing requirements report provides a list of all timing attributes set on the design.

You can set options to

- Include any minimum and maximum delay attributes on the path startpoints and endpoints
- Include path exception (false path, multicycle path, and maximum time borrow) attributes
- Include ignored timing attributes

You can also specify individual timing paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the report includes only paths that end at a specified endpoint, start at a specified startpoint, or pass through one or more specified throughpoints. For details, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

To generate a timing requirements report,

1. Choose **Timing > Report Timing Requirements**.

The Report Timing Requirements dialog box appears.

2. Set the report options as needed to control the types of information included in the report.
  - To include minimum and maximum delay times for path startpoints and endpoints, select the Show path delay attributes option.
  - To include false path, multicycle path, and maximum time borrow attributes, select the Show exceptions in expanded format option.
  - To include ignored path attributes, select the Show ignored timing path attributes option.
  - To disable line splitting, select the No line split option.
3. To limit the report to certain paths, define the paths to or from specific inputs, outputs, or registers by specifying path startpoints (From), throughpoints (Through), or endpoints (To).

You can specify any combination of startpoints, throughpoints, or endpoints. The report takes the worst path that meets the criteria.

To specify a startpoint, throughpoint, or endpoint, first select an object type.

- Startpoints and endpoints can be pins, ports, nets, or clocks.
- Throughpoints can be pins or nets.

Perform one of the following:

- Enter one or more object names.
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.

- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

5. Click OK or Apply.

## Reporting Wire Load Information

You can generate a report that provides information about the wire load models you have defined in the current design, including

- Cell name and design name
- Wire load model for the cell
- Library that contains the wire load model
- Fanout, length, points, average capacitance, standard deviation, and percentage of standard deviation for each wire load model

To report wire load information,

1. Choose Timing > Report Wire Load.

The Report Wire Load dialog box appears.

2. Select a design name in the Design name drop-down list.

This is the name of the design for which the wire load models are reported. The default is the name of the current design.

3. If you want to report information about a particular wire load model, select the Single model option and select a model name in the list.

By default, the All models option is selected and all wire load models for the selected design are included in the report.

4. Set other options that control the report content.

- To include wire load models in the libraries that are linked to the selected design, make sure the Report models in the linked libraries option is selected.
- To disable line splitting, select the No line split option.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

## Reporting Worst Path Timing

You can generate a report that provides detailed timing information for any number of paths in the design, and you can vary the level of detail to focus on particular timing violations and to determine the cause of a violation. Only constrained paths are listed; unconstrained paths do not appear in the report.

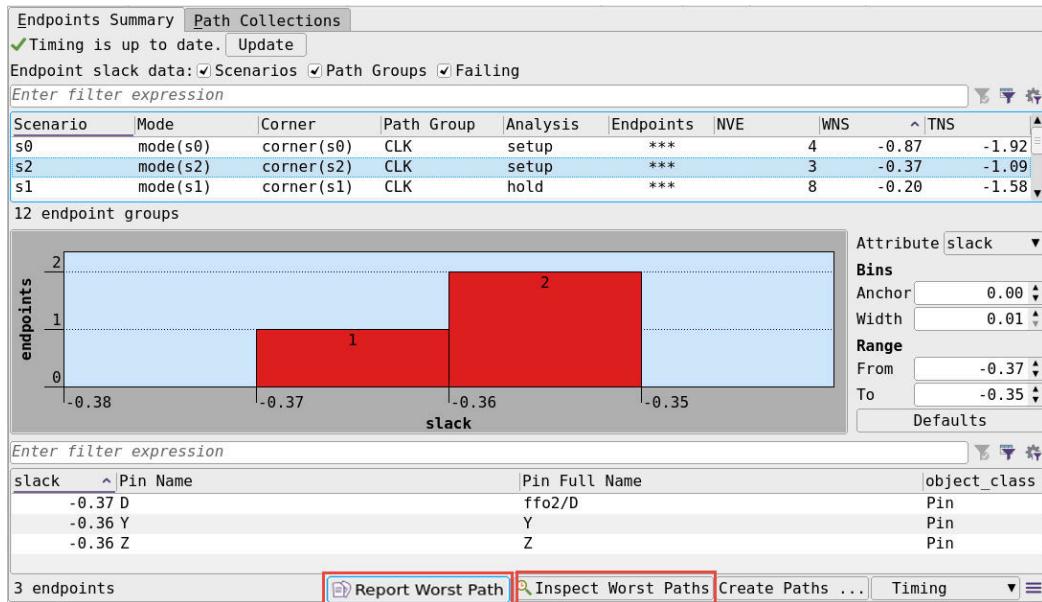
The default timing report provides information about the most critical path (the path with the worst slack) in the current design or for each path group in the current design. You can set options to

- List up to a maximum number of paths with the worst slack in the current design (or each path group in the current design)
- List up to a maximum number of paths to any single endpoint

You can also generate a report of information about specific timing paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the report includes only paths that end at a specified endpoint, start at a specified startpoint, or pass through one or more specified throughpoints. For details, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

You can also analyze and report the target timing path for specific operations. For example, you can generate a report for Report Worst Path and Inspect Worst Paths by selecting the buttons on the Timing Status Summary window. [Figure 15](#) shows an example of generating the report for worst path or to inspect worst path.

Figure 14 Report Worst Path and Inspect Worst Path



By default, timing reports show paths for maximum delay times. This allows you to check for setup violations. You can select a delay type option to generate a report for minimum delay times (to check for hold violations) or for the maximum or minimum delays relative to the rising or falling clock edge.

By default, a timing report lists only the startpoints and endpoints on a path. You can select a path type option to generate a report that includes additional information, such as the cells and pins on a path, the cells and pins on each clock path, the paths but not the time and slack calculations, or just the endpoint path delays and their time and slack calculations.

You can also select options to include

- Net names
- Input pin names and the delays of the nets connected to the pins
- Net transition times for driving pins
- Total (lump) capacitance
- Asynchronous timing arcs
- Certain attributes (such as `dont_touch`, `dont_use`, `map_only`, `size_only`, and `ideal_net`) for nets and cells

In addition, you can set options to

- Sort the paths by either path group or slack value
- Report only the timing loops in the design
- Find and report an input vector that sensitizes the reported paths or, if no input vector is found, report that the path is false
- Report the longest true path (the path with the least slack) in the design
- Disable line splitting
- Control whether the report is displayed in the report view, saved in a file, or both

The following sections show how to generate a default timing report and select output options, generate a default report for a specific path, generate a default report for multiple paths, and generate a custom report for one or more paths.

To generate a default timing report and select output options,

1. Choose Timing > Report Timing Path to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

3. Click OK or Apply.

To generate a default timing report for a specific path,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Define a path to or from a specific input, output, or register by specifying its startpoint (From), throughpoints (Through), or endpoint (To).

You can specify any combination of startpoints, throughpoints, or endpoints. The report takes the worst path that meets the criteria.

To specify a startpoint, throughpoint, or endpoint, first select an object type.

- Startpoints and endpoints can be pins, ports, nets, or clocks.
- Throughpoints can be pins or nets.

Perform one of the following:

- Enter one or more object names
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

3. Set output options as needed.

4. Click OK or Apply.

To generate a default timing report for multiple paths,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Enter the maximum number of worst paths to an endpoint in the Worst paths per endpoint text box.
3. Enter the maximum number of paths to include for each path group in the Max paths per group text box.
4. If necessary, limit the report to paths to or from specific inputs, outputs, or registers by specifying their startpoints (From), throughpoints (Through), or endpoints (To).

Select other report options as needed.

5. Set output options as needed. By default, Design Vision tool displays the report in the report view and does not save it in a file.
6. Click OK or Apply.

To generate a custom timing report,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window.
2. Specify the paths you want to include in the report by setting the options for maximum paths and specific startpoints, throughpoints, or endpoints as needed
3. Set options as needed to control the number of paths and delay time range.
  - To set the maximum number of worst paths to an endpoint, enter a value in the Worst paths per endpoint text box.
  - To set the maximum number of paths to include for each path group, enter a value in the Max paths per group text box.
  - To include only paths with delay times less than a maximum delay value, enter the value in the Maximum path delay text box.
  - To include only paths with delay times greater than a minimum delay value, enter the value in the Minimum path delay text box.
4. To control the amount of information listed for each path, select an option in the Path type drop-down list. The default (short) is set for a report that lists only the path startpoints and endpoints.
  - For a report that lists each cell and pin on a path, select full.
  - For a report that lists each cell and pin on the path from each clock source, select full\_clock.
  - For a report that lists the paths but not the required time and slack calculations, select only.
  - For a report in column format, with one line for each path, that lists only the endpoint path delays and the required time and slack calculations, select end.
5. To change the type of timing analysis used to generate the report, select an option in the Delay type dropdown list. The default (max) is set for maximum delays.
  - For minimum delays, select min.
  - For maximum delays, select max.
  - For maximum rising delays, select max\_rise.
  - For maximum falling delays, select max\_fall.

- For minimum rising delays, select min\_rise.
  - For minimum falling delays, select min\_fall.
6. Set options as needed to control the types of information included in the report.
- To list the nets for each path, select the Show nets in combinational path option.  
To list the delays for the nets, you must also select the Show input pins in combinational path option.
  - To list the input pins, and the delays of the nets connected to those pins, for each path, select the Show input pins in combinational path option.  
By default, only output pins are included in the report. To list the nets, you must also select the Nets option.
  - To list the net transition times for the driving pins on each path, select the Show net transition time option.
  - To include the total (lump) capacitance in the report, select the Show net capacitance option.
  - To include additional attributes in the report, select the `Show dont_touch, size_only` attributes for nets and cells option.  
The attributes include `dont_touch`, `dont_use`, `map_only`, and `size_only` for cells, and `dont_touch` and `iideal_set` for nets.
  - To include asynchronous timing arcs in the report, select the Enable asynchronous arcs option.  
Select this option to report timing information with timing arcs enabled when you have run timing verification with timing arcs disabled. Only the report is affected.
  - If you want the report to include only the timing loops in the design, select the Report timing loops option.
7. Make sure the other report options are set as you need them.
- To control the ordering of paths listed in the report, select an option in the Sort by list.  
For a report sorted by path group, select group. For a report sorted by slack value, select slack.
  - To find and report an input vector that sensitizes the reported paths or, if no input vector is found, report that the path is false, select the Justify paths with input vector option.

- To report the longest true path (the one with the least slack) in the design, select the Find true path option and enter a value in the Path delay threshold text box.

The Find true path option can require long runtimes for designs that contain many false paths. By specifying a positive value in the Path delay threshold text box, you reduce the amount of time spent searching for the longest path because the compiler reports the first path it finds that is equal to or greater than this value.

- To disable line splitting, select the No line split option.
8. Set output options as needed.
9. Click OK or Apply.

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## Selecting Objects in the Object Chooser

 When you click the  button in a dialog box, the Object Chooser dialog box appears. You can use this dialog box to select the names of one or more design objects.

The Object Chooser dialog box is divided into an object browser on top and an object list below the object browser. You can use the horizontal split bar between the object browser and the object list to adjust their relative heights.

The object browser is divided into an instance tree on the left and an object table on the right. You can use the vertical split bar between the instance tree and the object table to adjust their relative widths.

Use the object browser the same way you use the logic hierarchy view (for more details, see [Browsing the Design Hierarchy](#)). You can

- Select an instance name to display cell information in the object table
  - You can Shift-click or Control-click instance names to select combinations of objects.
- Click the expansion button (plus sign) next to the instance name to expand the instance tree, showing the names of the subblocks at the next level in the hierarchy

By default, the object table contains cell information. You can select an object type in the list above the table to display information about hierarchical cells, all cells, pins, pins of child cells, or nets.

- Cell information includes the cell instance names, the reference names of the designs the cells reference, the paths from the top-level designs to the cells, and the values of the `dont_touch` attribute.
- Pin information includes the pin and port names and the paths from the top-level design to the pins and ports.
- Net information includes the net names and the paths from the top-level design to the nets.

You can sort the information in the object table alphabetically by the contents of a column.

To select objects in the Object Chooser dialog box,

1. Select an instance name in the instance tree.
2. Select an object type in the list above the object table.
3. Select objects in the object table by doing either or both of the following:
  - Double-click individual object names.
  - Select one or more object names (use Shift-click or Control-click to select multiple names) and click the Click to Choose Objects button.

The selected object names appear in the object list below the object browser.

4. If you want to modify the list of names in the object list, select one or more names and click the Click to Remove Objects button.

The names disappear from the list.

5. Click OK or Apply.

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## Viewing Reports

Design Vision tool displays reports in report views.

You can use a report view to

- View a report and search for text
- Save the report in a file
- View a report from a file

When you generate a report by choosing a report command on a menu, the GUI opens a new report view to display the report. The GUI provides report commands on the Design menu and the Timing menu.

- Use Design menu commands to generate design information and design object reports.
- Use Timing menu commands to generate timing and constraint reports.

These commands open dialog boxes in which you can set report options and output options. You can

- Display the report in a report view
- Save the report in a file
- Append the report to a file

When you use a menu command to display a report, Design Vision tool opens a new report view and displays the report in both the report view and the console log view.

When you display a report by entering the report command on the command line or by running a script, Design Vision tool displays the report in the console log view. If an empty report view is open, Design Vision tool also displays the report in the empty report view. An empty report view is a new report view that you open by choosing Window > New Report View or a report view in which you have removed the report text.

After opening a report, you can perform the following operations:

- [Removing and Saving a Report](#)
- [Opening a Report Saved in a File](#)
- [Finding the Text in a Report](#)

## Removing and Saving a Report

To remove a report from a report view,

- Click the  button.

To save a report,

1. Click the  button.

The Save Report to File dialog box appears.

2. Select a file or enter a file name in the File name text box.

If the file already exists, Design Vision tool overwrites it.

3. Click Save.

## Opening a Report Saved in a File

To open a report saved in a file,

1. Make sure the report view is empty.

2. Click the  button.

The Open Report to File dialog box appears.

3. Select the file or enter its name in the File name text box.
4. Click Open.

## Finding the Text in a Report

To find text in a report,

1. Type the text in the text box at the top of the report view.
2. Click the  button. You can select the names of design objects that you want to view in a schematic. The first time you click an object name (blue text) in a cell, net, port, or worst-path timing report, Design Vision tool,
  - Selects the object
  - Opens a new schematic view window
  - Displays the schematic for the design instance (hierarchical cell) in which the object is located
  - Magnifies the design to fit the object in the viewIf you click other object names in the report, or in other reports or report views, Design Vision changes the schematic view to display and fit the selected object.

**Note:**

If you close the schematic view window, Design Vision tool opens a new window the next time you select an object in a report view.

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## Generating Object Reports

You can generate a report for one or more selected cells, ports, or nets. The GUI displays the report in a report view. You can also select objects in a report view that you want to examine in a schematic view.

To generate a report for one or more objects of the same type,

1. Select the objects.
2. Choose the appropriate report command in the Design menu.  
The associated report dialog box appears.
3. Click Selection in the report dialog box.  
The names of the selected objects appear.
4. Set other report options as needed.
5. Click OK.

If you click an object name (blue text) in the report view, the GUI selects the object in a schematic view and magnifies the schematic to fit the object in the view window.

- [Reporting Area Information](#)
- [Reporting Cell Information](#)
- [Reporting Clock Information](#)
- [Reporting Clock Network Skew Information](#)
- [Reporting Clock Tree Fanout Information](#)
- [Reporting Compile Options](#)
- [Reporting Constraint Violations](#)
- [Reporting Datapath Extraction Analysis](#)
- [Reporting Design Hierarchy Information](#)
- [Reporting Design Information](#)
- [Reporting Design Reference Information](#)
- [Reporting Design Resources](#)
- [Reporting Net Information](#)
- [Reporting Path Groups](#)
- [Reporting Port Information](#)
- [Reporting Power](#)
- [Reporting Timing Requirements](#)

- [Reporting Wire Load Information](#)
- [Reporting Worst Path Timing](#)

## Reporting Area Information

You can generate a report that contains area information and statistics for the design of the current instance, if set, or for the current design. If the design is a block abstraction, the report also contains area information and statistics for the original design from which the block abstraction is created.

The report lists

- The names of the libraries linked to the design
- The number of ports, cells, nets, references, combinational areas, non-combinational areas, and net interconnect areas in the design
- The total area of the design

The report also provides information messages about the design, such as a message that the design contains unmapped logic or that it contains black box components.

To report area information,

1. Choose **Design > Report Area**.

The Report Area dialog box appears. The name of the current design appears in the Current design text box and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options to control the report content.

- To prevent line splitting, deselect the Split line option.
- To include the area used by cells across the design hierarchy, select the Hierarchy option.

When this option is selected, the report includes the absolute value and the percentage of the area used by each of the cells across the design hierarchy. It also includes details about the area used by combinational, non-combinational, and macro and black box cells.

- To include the area of Synopsys DesignWare® synthetic module, select the Show Designware option.

When this option is selected, the report includes the total synthetic module area and the total datapath cell area. If the tool ungrouped the synthetic modules during optimization, the report includes the estimated area of the ungrouped cells.

- To include the area and aspect ratio of the core area, select the Show physical information option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click **Apply** or **OK**.

For more information about the area report and the report options, see the man page for the `report_area` command.

## Reporting Cell Information

You can generate a report that contains information about a specific cell or set of cells, including

- Corresponding cell reference (the library cell name)
- Name of the library that contains the cell
- Area of the cell
- Connectivity information

To report cell information,

1. Choose Design > Report Cells.

The Report Cells dialog box appears.

2. Specify one or more cell names by performing one of the following:
  - Enter the cell names in the Cells text box (use blank spaces to separate names).
  - Click the Object Chooser  button and select cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
  - Select one or more cells, then click the Selection button.
3. Set other options that control the report content.
  - To disable line splitting, deselect the Split line option.
  - To include all available cell connection information, select the Verbose option.
  - To include the orientations and locations of the cells, select the Show physical information option.
  - To include the information about physical-only cells, select the Show physical only cells option.
  - To include information about input and output pins and their connected nets, select the Show cell connections option.
  - To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits box.

This number must be an integer between 0 and 13. The default is 2. This option overrides the `report_default_significant_digits` variable.

4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

5. Click OK or Apply.

For more information about the cell report and the report options, see the man page for the `report_cell` command.

## Reporting Clock Information

You can generate a report that contain clock-related information for the current design.

The clocks report contains design information about each clock, including

- Clock names
- Rise and fall times
- Skew type
- Attributes

To generate a report of design-related information about each clock in the current design,

1. Choose Design > Report Clocks.

The Report Clocks dialog box appears. The name of the current design appears in the Current design text box.

2. Set the report options to control the report content.

- To prevent line splitting, deselect the Split line option.
- To list all clocks in the design and include the clock name, period, waveform, source, and clock attributes for each clock, select the Show Attribute option.
- To include the clock network skew information set on the design by the `set_clock_uncertainty` command, select the Show Skew option.

This information includes the rise and fall delays and the plus and minus uncertainty of the clock network.

- To include the clock group information set on the design by the `set_clock_groups` command, select the Show Groups option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.

- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Clock Network Skew Information

You can generate a timing report that contains clock network skew information for the current design, including the rise and fall delays and the plus and minus uncertainty of the rise and fall delays.

To generate a timing report of clock network skew information,

1. Choose Timing > Report Clock Skew.

The Report Clock Skew dialog box appears. The name of the current design appears in the Current design box.

2. To disable line splitting, select the No line split option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the clock skew report and the report options, see the man page for the `report_clock` command.

## Reporting Clock Tree Fanout Information

You can generate a timing report that contains information about the clock tree fanout network for every clock source in the current design. If there are no clocks in the design, or if the clocks have no sources, the clock tree report is empty.

To generate a timing report of clock tree fanout information,

1. Choose Timing > Report Clock Tree.

The Report Clock Tree dialog box appears. The name of the current design appears in the Current design text box.

2. To disable line splitting, select the No line split option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the clock tree report and the report options, see the man page for the `report_clock_tree` command.

## Reporting Compile Options

You can generate a report of compile options for the current instance, if set, or for the current design. This report lists the compilation options (flatten, structure, structure\_boolean, or structure\_timing) and their values (true or false) for the design and each subdesign in the design hierarchy.

To generate a report of compile options,

1. Choose Design > Report Compile Options.

The Report Compile Options dialog box appears. The name of the current design appears in the Current design text box. If you have set the current instance, its name appears in the Current instance text box.

2. (Optional) Disable line splitting by selecting the No line split option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Constraint Violations

You can generate a report that provides information about design rule and optimization constraint violations in the current design.

For each constraint, the report includes information about

- If the constraint is violated or met, and by how much
- Which design object is the worst violator

By default, the report includes information about all design rule and optimization constraints in the design. You can limit the report to one or more types of constraints by selecting the options for those constraint types.

If you are using the Power Compiler tools, you can also limit the information about power constraints to dynamic power, leakage, or both.

### Note:

Queries for power constraint information require a Power-Optimization license and supporting libraries characterized for power. For details, see the *Power Compiler documentation*.

To generate a report about constraint violations,

1. Choose Design > Report Constraints.

The Report Constraints dialog box appears. The name of the current design appears in the Current design text box.

2. (Optional) Set options as needed to limit the report to information about certain types of design rule and optimization constraints.

Select one or more options for the types of constraint information you want to include.

- To include maximum capacitance constraint information, select the Show only maximum capacitance option.  
Maximum capacitance is a design rule constraint (`max_capacitance`) that sets an upper limit for the total capacitance on a net.
- To include minimum capacitance constraint information, select the Show only minimum capacitance option.  
Minimum capacitance is a design rule constraint (`min_capacitance`) that sets a lower limit for the total capacitance on a net.
- To include maximum delay and setup constraint information, select the Show only maximum delay option.
- To include minimum delay and hold constraint information, select the Show only minimum delay option.
- To include maximum dynamic power constraint information, but not other power constraint information, select the Show only maximum dynamic power option.
- To include maximum leakage power constraint information, but not other power constraint information, select the Show only maximum leakage power option.
- To include minimum porosity constraint information, select the Show only minimum porosity option.  
Minimum porosity is an optimization constraint (`min_porosity`) for routability.
- To include maximum transition constraint information, select the Show only maximum transition option.  
Maximum transition is a design rule constraint (`max_transition`) that sets an upper limit for the transition time on a net.
- To include maximum fanout constraint information, select the Show only maximum fanout option.  
Maximum fanout is a design rule constraint (`max_fanout`) that limits the fanout load on a net.
- To include maximum area constraint information, select the Show only maximum area option.
- To include cell degradation constraint information, select the Show only cell degradation option.  
Cell degradation is a design rule constraint (`cell_degradation`) that limits the total capacitance on a net. The total capacitance that can be driven by a cell is a function of the transition times at the inputs of the cell.

- To include connection class constraint information, select the Show only connection class option.

The connection class constraint (`connection_class`) is included only when a connection class violation has occurred.

- To include multiple port nets constraint information, select the Show only multiport nets option.

The multiple port nets constraint (`multiport_net`) is included only when the `set_fix_multiple_port_nets` variable is set to none (the default).

- To include critical range constraint information, select the Show only critical range option.

Critical range is a design rule constraint (`critical_range`) that enables optimization of near critical paths in addition to the most critical path.

- To include maximum toggle rate constraint information, select the Show only maximum toggle rate option.

- To include maximum net length constraint information, select the Show only maximum net length option.

- To include maximum total power constraint information, select the Show only maximum total power option.

- To include minimum pulse width constraint information, select the Show only minimum pulse width option.

Minimum pulse width is a design rule constraint (`min_pulse_width`) that limits the minimal length of clock pulses in the clock network.

3. (Optional) To include constraint information for specific scenarios in a multiscenario design, enter the scenario names in the Scenarios text box.

The report lists the constraint information separately for each scenario and does not include constraint information for inactive scenarios.

By default, the report includes constraint information for all active scenarios in the design. However, if you select the Verbose option or the Show all violators option and do not specify any scenarios, the report includes constraint information for the current scenario only.

4. Set other report content options as needed.

- To disable line splitting, deselect the Split line option.
- To include additional information about constraint calculations, select the Verbose option.

If you also select the Show all violators option, the Verbose option provides detailed information about constraint violations.

- To display a summary of all violated design rule and optimization constraints in the current design, select the Show all violators option.

If you also select the Verbose option, the Show all violators option provides detailed information about constraint violations.

- To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits text box.

This number must be an integer between 0 and 13. The default is 2.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

For more information about the constraint report and the report options, see the man page for the `report_constraint` command.

## Reporting Datapath Extraction Analysis

You can analyze the datapath extraction of the current design and view a report of the resources contained in the design. This report can help you to find the resources in the design RTL. You can click the link for an arithmetic operator in the report to view the RTL in the RTL browser.

After reading in the RTL, you can generate a datapath extraction report of the resources contained in the current design and view the report in the HTML report view. This report can help you to find the resources in the design RTL. You can click the link for an arithmetic operator in the report to view the RTL in the RTL browser.

**Note:**

The datapath names in this report might differ from the datapath names in the design resources report. However, the names of the resources are the same in both reports.

You can use the datapath extraction report to examine how the datapath blocks are extracted from your RTL before you optimize the design. The tool analyzes the arithmetic contents of the design and provides feedback for improving the RTL code.

To get the best QoR results from datapath optimization, it is a must that the biggest possible datapath blocks are extracted from the RTL code. When the tool detects an arithmetic operator that is not extracted, it reports the information about what is blocking the datapath extraction, including the file name of the RTL and the line number of the operator it is inferred from.

See [SolvNet article 015771, “Coding Guidelines for Datapath Synthesis”](#) for information about coding styles to help improve datapath extraction.

To report datapath extraction,

1. Choose Design > Analyze Datapath Extraction, or choose AnalyzeRTL > Analyze Datapath Extraction.

The Analyze Datapath Extraction dialog box appears. The name of the current design appears in the Current design text box and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options as needed.

- To disable all automatic ungrouping operations and preserve all user hierarchies during datapath extraction analysis, deselect the Auto Ungroup option.

Deselecting this option has the same effect as selecting the No auto ungroup option in the Compile Ultra dialog box. If you disabled automatic ungrouping when you ran the `compile_ultra` command, you should also disable automatic ungrouping when you analyze datapath extraction.

- To sort the leakage detection messages in each design based on their potential impact, from high to low, select the Sort message option.
- To enable message filtering, select a message severity level option: Low or Medium.

The tool filters out messages with severity levels that are less than or equal to the severity level that you select. By default, the None option is selected, which means message filtering is disabled.

- To set the maximum number of leakage detection messages to include for each design, enter the number in the Maximum messages text box.

3. Set output options as needed.

By default, Design Vision tool displays the report in the HTML report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click OK or Apply.

The tool runs the `analyze_datapath_extraction` command and displays the report in a new HTML report view window.

The HTML report provides direct links to the RTL file. If you click the RTL file name link for an arithmetic operator, the tool opens a new RTL browser window by default and highlights the line number that contains the origin of the corresponding operator in the RTL file. For more details, see [Cross-Probing Synthetic Operators in a Datapath Extraction Report](#).

For more information about the datapath extraction report and the report options, see the *Design Compiler User Guide* and the man page for the `analyze_datapath_extraction` command.

### See Also

- [Cross-Probing Synthetic Operators in a Datapath Extraction Report](#)
- [Examining Cells in the RTL Browser](#)

## Reporting Design Hierarchy Information

You can generate a report that displays the reference hierarchy for the design of the current instance, if set, or for the current design.

You can control whether the report provides single listings for the hierarchies of each subdesign or multiple listings for subdesigns that occur at multiple locations in the design hierarchy.

To report design hierarchy information,

1. Choose Design > Report Design Hierarchy.

The Report Design Hierarchy dialog box appears. The name of the current design appears in the Current design text box. The name of the current instance, if it is set, appears in the Current instance text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
- To include multiple listings for subdesigns that occur at multiple locations in the design hierarchy, select the List all instances option.

The List first instance option is selected by default, that is the report lists subdesign once and uses and ellipsis (...) to indicate the contents of a previously displayed module.

- To exclude leaf cells from the report, deselect the Show leaf level cells option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the hierarchy report and the report options, see the man page for the `report_hierarchy` command.

## Reporting Design Information

You can generate a report that contains a summary of attributes on the current design. The report lists the libraries, flip-flop types, and latch types used in the design. It also includes information about operating conditions, the wire load model, pin input and output delays, disabled timing arcs, required licenses, and design parameters.

To generate a report about the current design,

1. Choose Design > Report Design.

The Report Design dialog box appears. The name of the current design appears in the Current design box.

2. Set report options to control the report content.

- To prevent line splitting, deselect the Split line option.
- To include physical-only attributes, select the Show physical option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Design Reference Information

You can generate a report that displays information about the references in the design of the current instance, if set, or for the current design. The report lists the reference name, library name, unit area per instance, number of instances, total area, and attributes for each reference in the design.

To report design reference information,

1. Choose Design > Report Reference.

The Report Reference dialog box appears. The name of the current design appears in the Current design text box, and the name of the current instance, if set, appears in the Current instance text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
  - To include information about references across the design hierarchy, select the Show Hierarchy references option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

For more information about the references report and the report options, see the man page for the `report_reference` command.

## Reporting Design Resources

You can generate a report that contains information about resources used in the current instance or the current design. A resource is an arithmetic or comparison operator read in as part of the HDL design. Resources can be shared during compile operations. The report includes information about shared resources, parameters used to build the module, and user-declared resources in each module. You can click the link for a cell in the report to view the RTL in the RTL browser.

To report resources used in the current instance or the current design,

1. Choose Design > Report Design Resources.

The Report Design Resources dialog box appears. The name of the current design appears in the Current design text box.

2. Set report options to control the report content.

- To disable line splitting, deselect the Split line option.
- To list resources from all subdesigns in the hierarchy, select the Show resources for subdesigns option.

By default, only resources used in the top-level design are listed.

- To include context information from the DesignWare generator, select the Show Context Information option.

By default, only the power context information is included.

- To include only the DesignWare cells that are optimized for the minimum power flow, select the Show resources with Minimum power option.

3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

The tool runs the `report_resources` command and displays the report in a new HTML report view window.

The HTML report provides direct links to the RTL file. If you click the RTL file name link for a cell, the tool opens a new RTL browser window by default and highlights the line number that contains the origin of the corresponding cell in the RTL file. For more details, see [Cross-Probing Cells in a Design Resources Report](#).

For more information about the design resources report and the report options, see the man page for the `report_resources` command.

#### See Also

- [Cross-Probing Cells in a Design Resources Report](#)
- [Examining Cells in the RTL Browser](#)

## Reporting Net Information

You can generate a report that contains information about a specific net or set of nets.

It also includes the following:

- Fanout and fanin
- Capacitance and resistance
- Pins
- Net connections

To report net information,

1. Choose Design > Report Nets.

The Report Nets dialog box appears.

2. Specify one or more net names by doing one of the following:

- Enter the net names in the Nets text box (use blank spaces to separate names).
- Click the Object Chooser  button and select net names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
- Select one or more nets, then click the Selection button.

3. Set other options that control the report content.

- To disable line splitting, deselect the Split line option.
- To include all available net connection information, select the Verbose option.
- To include net information only for the current instance (and not for other levels of the logic hierarchy), select the Do not trace hierarchy option.
- To include cell depreciation data at the end of the report, select the Show cell degradation values option.

Cell depreciation data consists of the capacitance on the net, the limit for the capacitance on the net (calculated from the cell depreciation tables for the drivers of the net), and the violation on the net.

- To include information about input and output pins and their connected nets, select the Show net connections option.
- To include the rise and fall transition times for each net at the end of the report, select the Show rise and fall transitions option.
- To report minimum capacitance, resistance, or transition values (instead of maximum values), select the Show minimum values option.
- To include the maximum toggle rate values for each net, select the Show maximum toggle rate values option.

- To include the total wire length of the net, and the preroutes if preroute information exists, select the Show physical information option.
- To include the preroutes of the physical net, select the Show preroute information only for physical nets option.
- To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits drop-down.

This number must be an integer between 0 and 13. The default is 2. This option overrides the `report_default_significant_digits` variable.

4. (Optional) To include the timing derate for specific scenarios in a multiscenario design, enter the scenario names in the Scenarios text box.

The report lists the timing derate separately for each scenario and does not include the timing derates for inactive scenarios.

By default, the report includes the timing derate for the current scenario only.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

For more information about the net report and the report options, see the man page for the `report_net` command.

## Reporting Path Groups

You can generate a report that contains information about path groups in the current design. This report identifies each path group in the current design and lists the weight and critical range for each path group.

To generate a report about path groups in the current design,

1. Choose Timing > Report Path Groups.

The Report Path Group dialog box appears. The name of the current design appears in the Current design text box.

2. (Optional) Disable line splitting by selecting the No line split option.
3. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

4. Click Apply or OK.

## Reporting Port Information

You can generate a report that contains information about ports in the design.

It also includes the following:

- Port name and direction
- Connections
- Pin capacitance
- Wire capacitance
- Attributes

To report port information,

1. Choose Design > Report Ports.

The Report Ports dialog box appears.

2. Specify one or more port names by doing one of the following:
  - Enter the port names in the Ports text box (use blank spaces to separate names).
  - Click the  button and select port names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
  - Select one or more ports, then click the Selection button.
3. Set other options that control the report content.
  - To disable line splitting, deselect the Split line option.
  - To include all available port information, select the Verbose option.
  - To include only the report sections that show the capabilities of the input and output ports, select the Show only input port drive option.
  - To include information about physical-only ports, select the Show only physical information option.
  - To set the number of significant digits to the right of the decimal point for values listed in the report, enter the number in the Significant digits text box.  
This number must be an integer between 0 and 13. The default is 2. This option overrides the report\_default\_significant\_digits variable.
  - To include the physical locations of the ports, select the Show physical information option.
4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

  - To prevent the report view from displaying the report, deselect the To report viewer option.
  - To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
  - To overwrite an existing file, deselect the Append to file option.  
By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.
5. Click OK or Apply.

For more information about the port report and the report options, see the man page for the `report_port` command.

## Reporting Power

You can generate a report that provides a summary of dynamic and static power for the current design. The report includes information about the internal power, net switching power, dynamic power, and cell leakage power used by the design.

**Note:**

The power constraints are used with the Power Compiler tool. Queries for power constraint information require a Power-Optimization license and supporting libraries characterized for power. For details, see the *Power Compiler documentation*.

The default power report provides a summary of power values for the design. You can set options to

- Include power information for individual objects (cells, nets, or both)  
You can include information for all the cells or nets in the design or for only those cells or nets you specify. You can also specify the maximum number of cells or nets to include.
- Include all available information for the cells or nets, including
  - The driver cell's internal and leakage power for each net
  - The contribution of each internal-power group to the internal power of each cell
- Include the cumulative power for each cell or net
- Exclude the power values for boundary nets
- Filter the report to include only a specified number of objects with the highest power values
- Include a histogram showing the range and distribution of power values

You can also set options to control

- The sorting order for cells or nets
- The analysis effort level
- Whether the report is formatted hierarchically, and the number of hierarchical levels to include
- Whether the report includes objects from all levels of the design hierarchy (as if it were flat) and whether lines in fixed-width columns can be split

The following sections show how to generate a summary power report and how to generate a power report that includes information for individual nets or cells.

To generate a summary power report,

1. Choose Design > Report Power.

The Report Power dialog box appears.

2. Make sure the Summary only report type is selected in the Report for drop-down list.

This option is selected by default.

3. Select an effort level option in the Analysis effort drop-down list.

The choices are low, medium, or high. The default is low.

The option you select sets the analysis effort in terms of the relative amount of CPU time spent on analysis. This option controls the depth of logic that is traversed to detect signal correlation. A higher effort means a longer runtime but higher accuracy. Variations in runtime and accuracy depend greatly on the circuit structure.

4. Make sure the other report options are set as you need them.

- To disable line splitting, select the No line split option.
- To include the cell counts of the power groups in the power group summary, select the Verbose option.
- To limit the report to a certain number of nets with the highest power values, enter a value in the Worst number text box.
- To exclude the power values for boundary nets, select the Exclude power of boundary nets option.

5. Set output options as needed.

By default, Design Vision tools displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click OK or Apply.

To generate a power report that includes information for individual nets or cells,

1. Choose Design > Report Power.

The Report Power dialog box appears.

2. Select a report type in the Report for drop-down list.

- Select Nets only to include information for individual nets.
  - Select Cells only to include information for individual cells.
  - Select Nets and cells to include information for individual nets and cells.
3. (Optional) To limit the report to specific nets or cells, select the Only nets/cells option and specify the net or cell names in one of the following ways:
    - Enter the net or cell names in the Only nets/cells text box (use blank spaces to separate names).
    - Click the  button and select net or cell names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).
    - Select one or more nets or cells, then click the Selection button.

The All nets/cells option is selected by default.

4. (Optional) To include a histogram of power values, select the Show nets histogram option.

You can limit the range of power values in the histogram:

- To set the lower limit, enter a value in the Exclude values <= text box.
- To set the upper limit, enter a value in the Exclude values => text box.

**Note:**

The Show nets histogram option is not available when you select the Use hierarchical format[z] option.

5. Select an effort level option in the Analysis effort drop-down list.

The choices are low, medium, or high. The default is low.

The option you select sets the analysis effort in terms of the relative amount of CPU time spent on analysis. This option controls the depth of logic that is traversed to detect signal correlation. A higher effort means a longer runtime but higher accuracy. Variations in runtime and accuracy depend greatly on the circuit structure.

6. (Optional) To control the sorting order for nets or cells in the report, select an option in the Sort mode drop-down list.

The available choices depend on whether you are generating a report for cells, nets, or both.

- For a cell report, the valid choices are

- name
- cell\_leakage\_power
- cell\_internal\_power
- dynamic\_power
- cumulative\_fanout
- cumulative\_fanin

- For a net report, the valid choices are

- name
- net\_switching\_power
- net\_toggle\_rate
- total\_net\_load
- net\_static\_probability
- cumulative\_fanout
- cumulative\_fanin

7. Set the other report options as needed.

- To format the report hierarchically, select the Use hierarchical format option and enter the number of hierarchy levels in the Hierarchy levels text box.
- To limit the report to a certain number of nets with the highest power values, enter a value in the Worst number text box.
- To disable line splitting, select the No line split option.
- To include all available net or cell information, select the Verbose option.
- To exclude the power values for boundary nets, select the Exclude power of boundary nets option.
- To calculate and list the cumulative power for every net or cell in the report, select the Report cumulative power[k] option.
- To traverse the design hierarchy and include objects at all lower levels (as if the design hierarchy were flat), select the Traverse hierarchy at all levels option.

8. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

9. Click OK or Apply.

For more information about the power report and the report options, see the man page for the `report_power` command.

## Reporting Timing Requirements

You can generate a report of information about timing requirements for the current design or for specific timing paths in the current design.

The default timing requirements report provides a list of all timing attributes set on the design.

You can set options to

- Include any minimum and maximum delay attributes on the path startpoints and endpoints
- Include path exception (false path, multicycle path, and maximum time borrow) attributes
- Include ignored timing attributes

You can also specify individual timing paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the report includes only paths that end at a specified endpoint, start at a specified startpoint, or pass through one or more specified throughpoints. For details, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

To generate a timing requirements report,

1. Choose **Timing > Report Timing Requirements**.

The Report Timing Requirements dialog box appears.

2. Set the report options as needed to control the types of information included in the report.
  - To include minimum and maximum delay times for path startpoints and endpoints, select the Show path delay attributes option.
  - To include false path, multicycle path, and maximum time borrow attributes, select the Show exceptions in expanded format option.
  - To include ignored path attributes, select the Show ignored timing path attributes option.
  - To disable line splitting, select the No line split option.
3. To limit the report to certain paths, define the paths to or from specific inputs, outputs, or registers by specifying path startpoints (From), throughpoints (Through), or endpoints (To).

You can specify any combination of startpoints, throughpoints, or endpoints. The report takes the worst path that meets the criteria.

To specify a startpoint, throughpoint, or endpoint, first select an object type.

- Startpoints and endpoints can be pins, ports, nets, or clocks.
- Throughpoints can be pins or nets.

Perform one of the following:

- Enter one or more object names.
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

4. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.

- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

5. Click OK or Apply.

## Reporting Wire Load Information

You can generate a report that provides information about the wire load models you have defined in the current design.

It also includes

- Cell name and design name
- Wire load model for the cell
- Library that contains the wire load model
- Fanout, length, points, average capacitance, standard deviation, and percentage of standard deviation for each wire load model

To report wire load information,

1. Choose Timing > Report Wire Load.

The Report Wire Load dialog box appears.

2. Select a design name in the Design name drop-down list.

This is the name of the design for which the wire load models are reported. The default is the name of the current design.

3. If you want to report information about a particular wire load model, select the Single model option and select a model name in the list.

By default, the All models option is selected and all wire load models for the selected design are included in the report.

4. Set other options that control the report content.

- To include wire load models in the libraries that are linked to the selected design, make sure the Report models in the linked libraries option is selected.
- To disable line splitting, select the No line split option.

5. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

6. Click Apply or OK.

## Reporting Worst Path Timing

You can generate a report that provides detailed timing information for any number of paths in the design, and you can vary the level of detail to focus on particular timing violations and to determine the cause of a violation. Only constrained paths are listed; unconstrained paths do not appear in the report.

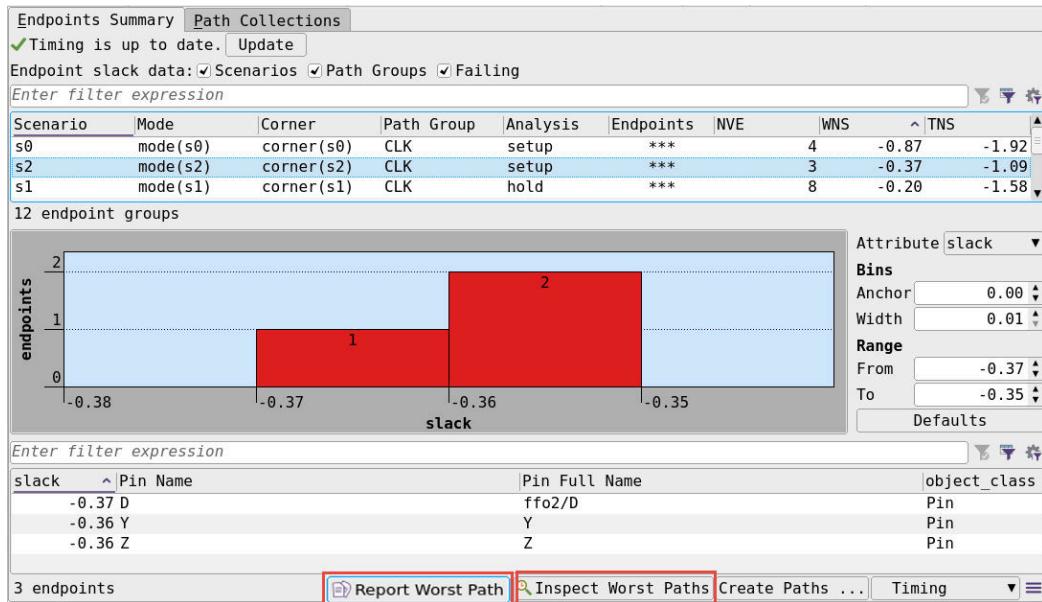
The default timing report provides information about the most critical path (the path with the worst slack) in the current design or for each path group in the current design. You can set options to

- List up to a maximum number of paths with the worst slack in the current design (or each path group in the current design)
- List up to a maximum number of paths to any single endpoint

You can also generate a report of information about specific timing paths by selecting one or more path endpoints, startpoints, or throughpoints. In this case, the report includes only paths that end at a specified endpoint, start at a specified startpoint, or pass through one or more specified throughpoints. For details, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

You can also analyze and report the target timing path for specific operations. For example, you can generate a report for Report Worst Path and Inspect Worst Paths by selecting the buttons on the Timing Status Summary window. [Figure 15](#) shows an example of generating the report for worst path or to inspect worst path.

Figure 15 Report Worst Path and Inspect Worst Path



By default, timing reports show paths for maximum delay times. This allows you to check for setup violations. You can select a delay type option to generate a report for minimum delay times (to check for hold violations) or for the maximum or minimum delays relative to the rising or falling clock edge.

By default, a timing report lists only the startpoints and endpoints on a path. You can select a path type option to generate a report that includes additional information, such as the cells and pins on a path, the cells and pins on each clock path, the paths but not the time and slack calculations, or just the endpoint path delays and their time and slack calculations.

You can also select options to include

- Net names
- Input pin names and the delays of the nets connected to the pins
- Net transition times for driving pins
- Total (lump) capacitance
- Asynchronous timing arcs
- Certain attributes (such as `dont_touch`, `dont_use`, `map_only`, `size_only`, and `ideal_net`) for nets and cells

In addition, you can set options to

- Sort the paths by either path group or slack value
- Report only the timing loops in the design
- Find and report an input vector that sensitizes the reported paths or, if no input vector is found, report that the path is false
- Report the longest true path (the path with the least slack) in the design
- Disable line splitting
- Control whether the report is displayed in the report view, saved in a file, or both

The following sections show how to generate a default timing report and select output options, generate a default report for a specific path, generate a default report for multiple paths, and generate a custom report for one or more paths.

To generate a default timing report and select output options,

1. Choose Timing > Report Timing Path to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Set output options as needed.

By default, Design Vision tool displays the report in the report view and does not save it in a file.

- To prevent the report view from displaying the report, deselect the To report viewer option.
- To save the report in a file, select the To file option and specify the file. You can either enter the path and file name in the box or click Browse and select the file name in the dialog box that appears.
- To overwrite an existing file, deselect the Append to file option.

By default, if the file you specify exists, Design Vision tool appends the report to the file. The Append to file option is available only when the To file option is selected.

3. Click OK or Apply.

To generate a default timing report for a specific path,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Define a path to or from a specific input, output, or register by specifying its startpoint (From), throughpoints (Through), or endpoint (To).

You can specify any combination of startpoints, throughpoints, or endpoints. The report takes the worst path that meets the criteria.

To specify a startpoint, throughpoint, or endpoint, first select an object type.

- Startpoints and endpoints can be pins, ports, nets, or clocks.
- Throughpoints can be pins or nets.

Perform one of the following:

- Enter one or more object names
- Select one or more objects and click the Selection button.
- Click the  button and select the object names in the Object Chooser dialog box (for details, see [Selecting Objects in the Object Chooser](#)).

For more details about specifying paths, see [Specifying Path Startpoints, Throughpoints, and Endpoints](#).

3. Set output options as needed.

4. Click OK or Apply.

To generate a default timing report for multiple paths,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window. If you are using TestMAX DFT, you can click the Report button in a hold time analysis window.

2. Enter the maximum number of worst paths to an endpoint in the Worst paths per endpoint text box.
3. Enter the maximum number of paths to include for each path group in the Max paths per group text box.
4. If necessary, limit the report to paths to or from specific inputs, outputs, or registers by specifying their startpoints (From), throughpoints (Through), or endpoints (To).

Select other report options as needed.

5. Set output options as needed. By default, Design Vision tool displays the report in the report view and does not save it in a file.
6. Click OK or Apply.

To generate a custom timing report,

1. Choose Timing > Report Timing Paths to open the Report Timing Paths dialog box.

Alternatively, you can click the Report button in a timing status summary window or choose Report > Timing Path in a path inspector window.
2. Specify the paths you want to include in the report by setting the options for maximum paths and specific startpoints, throughpoints, or endpoints as needed.
3. Set options as needed to control the number of paths and delay time range.
  - To set the maximum number of worst paths to an endpoint, enter a value in the Worst paths per endpoint text box.
  - To set the maximum number of paths to include for each path group, enter a value in the Max paths per group text box.
  - To include only paths with delay times less than a maximum delay value, enter the value in the Maximum path delay text box.
  - To include only paths with delay times greater than a minimum delay value, enter the value in the Minimum path delay text box.
4. To control the amount of information listed for each path, select an option in the Path type drop-down list. The default (short) is set for a report that lists only the path startpoints and endpoints.
  - For a report that lists each cell and pin on a path, select full.
  - For a report that lists each cell and pin on the path from each clock source, select full\_clock.
  - For a report that lists the paths but not the required time and slack calculations, select only.
  - For a report in column format, with one line for each path, that lists only the endpoint path delays and the required time and slack calculations, select end.
5. To change the type of timing analysis used to generate the report, select an option in the Delay type dropdown list. The default (max) is set for maximum delays.
  - For minimum delays, select min.
  - For maximum delays, select max.
  - For maximum rising delays, select max\_rise.
  - For maximum falling delays, select max\_fall.

- For minimum rising delays, select min\_rise.
  - For minimum falling delays, select min\_fall.
6. Set options as needed to control the types of information included in the report.
- To list the nets for each path, select the Show nets in combinational path option.  
To list the delays for the nets, you must also select the Show input pins in combinational path option.
  - To list the input pins, and the delays of the nets connected to those pins, for each path, select the Show input pins in combinational path option.  
By default, only output pins are included in the report. To list the nets, you must also select the Nets option.
  - To list the net transition times for the driving pins on each path, select the Show net transition time option.
  - To include the total (lump) capacitance in the report, select the Show net capacitance option.
  - To include additional attributes in the report, select the `Show dont_touch, size_only` attributes for nets and cells option.  
The attributes include `dont_touch`, `dont_use`, `map_only`, and `size_only` for cells, and `dont_touch` and `ideal_set` for nets.
  - To include asynchronous timing arcs in the report, select the Enable asynchronous arcs option.  
Select this option to report timing information with timing arcs enabled when you have run timing verification with timing arcs disabled. Only the report is affected.
  - If you want the report to include only the timing loops in the design, select the Report timing loops option.
7. Make sure the other report options are set as you need them.
- To control the ordering of paths listed in the report, select an option in the Sort by list.  
For a report sorted by path group, select group. For a report sorted by slack value, select slack.
  - To find and report an input vector that sensitizes the reported paths or, if no input vector is found, report that the path is false, select the Justify paths with input vector option.

- To report the longest true path (the one with the least slack) in the design, select the Find true path option and enter a value in the Path delay threshold text box.

The Find true path option can require long runtimes for designs that contain many false paths. By specifying a positive value in the Path delay threshold text box, you reduce the amount of time spent searching for the longest path because the compiler reports the first path it finds that is equal to or greater than this value.

- To disable line splitting, select the No line split option.
8. Set output options as needed.
9. Click OK or Apply.

---

## Selecting Objects in the Object Chooser

The Object Chooser dialog box lets you select the names of one or more design objects.

The Object Chooser dialog box is divided into an object browser on top and an object list below the object browser. You can use the horizontal split bar between the object browser and the object list to adjust their relative heights.

The object browser is divided into an instance tree on the left and an object table on the right. You can use the vertical split bar between the instance tree and the object table to adjust their relative widths.

Use the object browser the same way you use the logic hierarchy view (for more details, see [Browsing the Design Hierarchy](#)). You can

- Select an instance name to display cell information in the object table

You can Shift-click or Control-click instance names to select combinations of objects.
- Click the expansion button (plus sign) next to the instance name to expand the instance tree, showing the names of the subblocks at the next level in the hierarchy

By default, the object table contains cell information. You can select an object type in the list above the table to display information about hierarchical cells, all cells, pins, pins of child cells, or nets.

- Cell information includes the cell instance names, the reference names of the designs the cells reference, the paths from the top-level designs to the cells, and the values of the `dont_touch` attribute.
- Pin information includes the pin and port names and the paths from the top-level design to the pins and ports.
- Net information includes the net names and the paths from the top-level design to the nets.

You can sort the information in the object table alphabetically by the contents of a column.

To select objects in the Object Chooser dialog box,

1. Click the  button in any dialog box to open the Object Chooser dialog box.
2. Select an instance name in the instance tree.
3. Select an object type in the list above the object table.
4. Select objects in the object table by doing either or both of the following:
  - Double-click individual object names.
  - Select one or more object names (use Shift-click or Control-click to select multiple names) and click the Click to Choose Objects button.

The selected object names appear in the object list below the object browser.

5. If you want to modify the list of names in the object list, select one or more names and click the Click to Remove Objects button.

The names disappear from the list.

6. Click OK or Apply.

# 5

## Solving Timing Problems

---

The Design Vision GUI provides tools for both high-level timing analysis and detailed path analysis. This chapter presents basic procedures and suggestions for solving timing problems by using the GUI.

For information about these procedures, see the following sections:

- [Before You Analyze](#)
  - [Creating a Timing Overview](#)
  - [Choosing a Strategy for Timing Closure](#)
- 

### Before You Analyze

Before you analyze your design with the Design Vision GUI, follow your normal compile methodology to create a constrained gate-level design. A constrained gate-level design is a prerequisite to any timing analysis.

For more information about using the Design Vision tool to create a gate-level design, see [Chapter 4, Performing Basic Tasks](#).

---

### Creating a Timing Overview

Creating an overview of the timing of a design is a valuable way to start any analysis of the design's timing problems. A timing overview can help you decide what strategy to follow in gaining timing closure.

For example, a timing overview can help answer such questions as

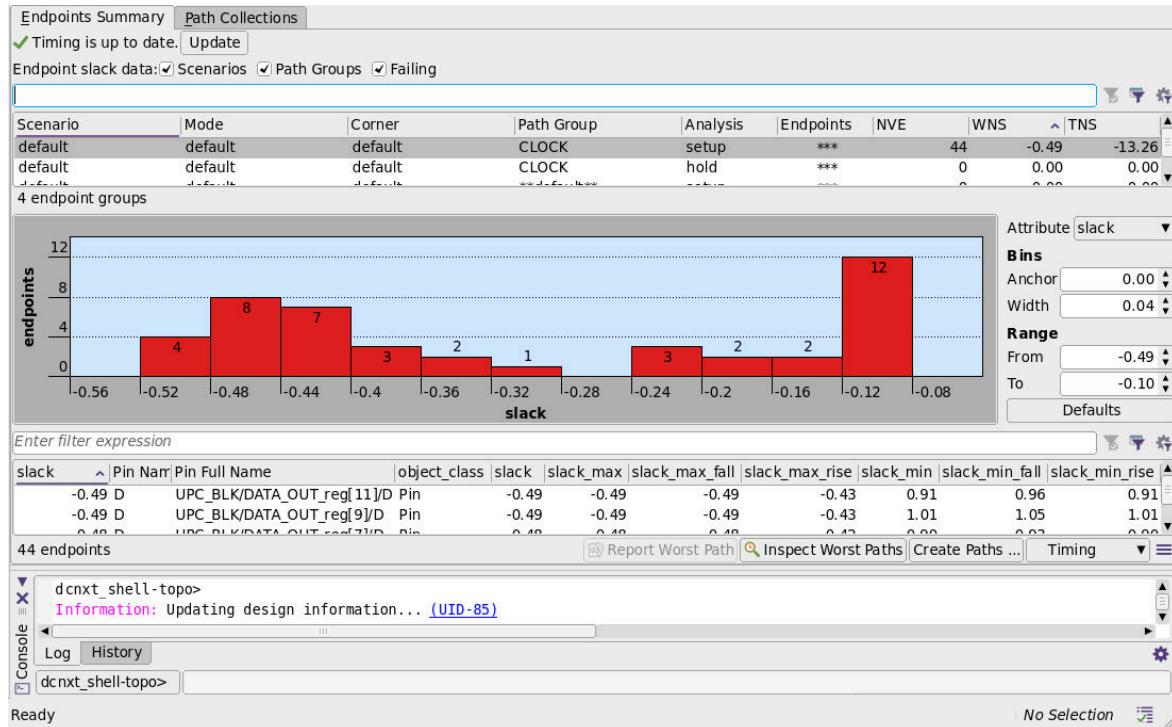
- Do I have many failing paths or just a few?
- Can I apply a local strategy for gaining timing closure?
- Do I need a global strategy for gaining timing closure?

To create a timing overview of your design,

1. Start with a constrained gate-level design.
2. Generate an endpoint slack data.

**Figure 16** is a typical endpoint slack histogram for a design with a 4ns clock cycle.

**Figure 16 Endpoint Slack Data**



Using information such as that in **Figure 16**, you might decide on a local strategy if just a few paths are failing by a small margin (failing path endpoints are in one or more red bins to the left of 0 on the horizontal axis). Conversely, if you find that many paths are failing, or that the design is failing your timing goals by a large margin, you might choose a higher-level or global strategy for problem solving.

## Choosing a Strategy for Timing Closure

There is no single strategy that ensures quick and easy timing closure. However, a strategy based on the size and number of timing violations can be useful.

---

## Assessing the Relative Size of Your Timing Violations

This section suggests guidelines for describing the relative size of timing violations in your design. After you create an endpoint slack histogram, you can use these size guidelines to help you judge what strategy to use for timing closure.

What you consider to be small or large violations depends on the requirements of your design and your design process; however, assessing violation size as a percentage of clock cycle can be useful.

- Small violations

Some designers consider small violations to be about 10 percent of the clock cycle or less.

- Large violations

Some designers consider large violations to be about 20 percent of the clock cycle or greater.

- Medium violations

Medium-size timing failures fall between the limits you set for large and small failures in your design or design process.

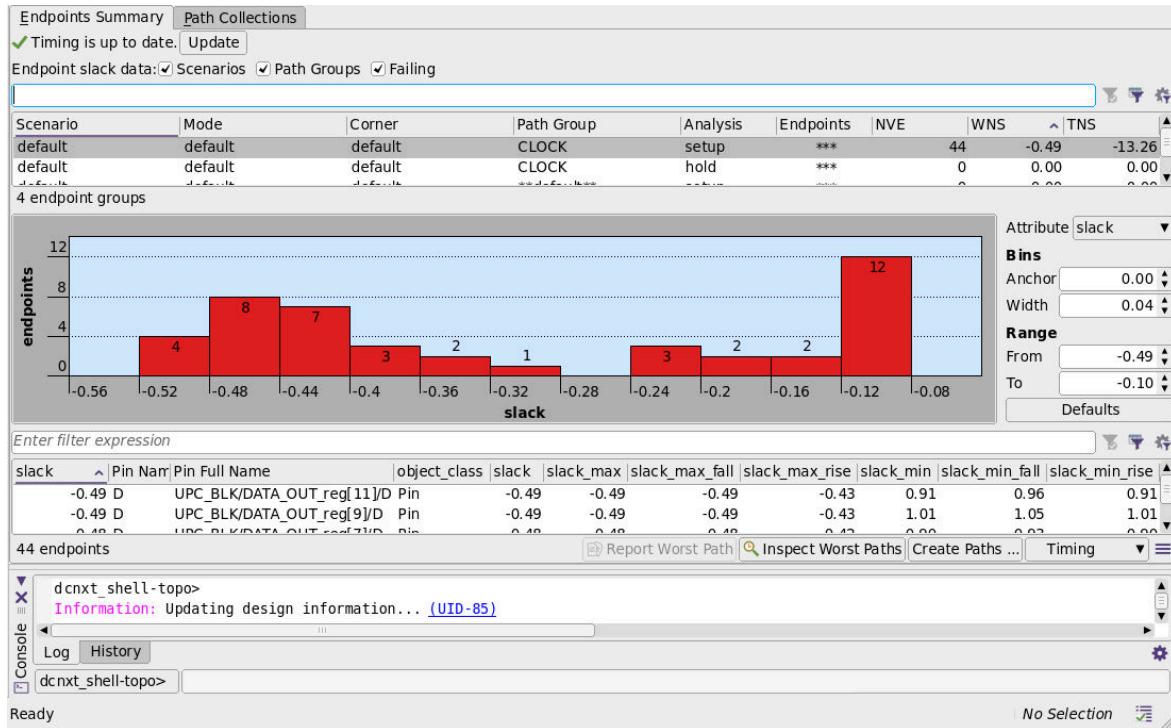
Whether your design is failing timing goals by large or small margins, the best strategy for timing closure is one that uses the least amount of runtime or number of design iterations to achieve timing goals. This principle underlies the methodology suggestions in this chapter. For more information about creating a timing overview, see [Creating a Timing Overview on page 455](#).

---

## When Timing Violations Are Small

[Figure 17](#) is a histogram of a design that is failing timing goals by a small margin. For example, no path is failing by more than 0.14 ns—that is, less than 10 percent of the 4-ns clock cycle (ignoring input and output delay). You can click any bin to see the endpoint names for the paths in the bin.

**Figure 17 Design With Small Timing Violations**



Designs that fail by a small margin can have many failing paths or just a few.

If suggestions for fixing small violations (either globally or locally) do not meet your timing goals, try applying the suggestions in [When Timing Violations Are Medium](#) on page 460 or [When Timing Violations Are Large](#) on page 462.

## Working Globally to Fix Small Violations

To apply a global methodology for fixing small violations, consider recompiling your design using the incremental option and a higher map effort. The incremental option saves runtime by using the current netlist as the startpoint for design improvements.

The incremental compile with higher map effort has the advantage of simplicity—that is, it requires little or no time spent in analyzing the source of timing problems. However, this method can change much of the logic in the design.

## Working Locally to Fix Small Violations

If you have a small number of paths with small violations, or if your violations seem to come from a limited set of problems on a few paths, a local strategy can be effective.

To use a local strategy for fixing small violations,

- Check hierarchy on failing paths

The tool does not optimize across hierarchical boundaries. The snake paths limit the tool's ability to solve timing problems on such paths.

- Look for excessive fanout on failing paths

Because higher fanout causes higher transition times, excessive fanout can worsen negative slack on failing paths.

To check for hierarchy problems on failing paths,

1. Generate the histogram.
2. Click a bin that contains a failing path.

A list of endpoints for failing paths are displayed.

3. Select the endpoint for the path you are interested in.
4. Generate a schematic to see which leaf cells are in which levels of hierarchy.

If your critical path, for example, crosses multiple subblocks of a level of hierarchy, consider ungrouping these subblocks. The tool does not optimize across hierarchy boundaries. Thus, a subsequent compile has further opportunity to optimize the critical path when you ungroup such blocks.

To look for excessive fanout on failing paths,

1. Generate an endpoint slack histogram.
2. Select the endpoints for failing paths.  
Select the failing bin to see the endpoints.
3. Generate a timing report with the following options:
  - net
  - trans

Send the report output to the report view. For more information about report generation, see [Working With Reports on page 379](#) and the [Viewing Reports](#).

4. Examine the report for pins with high transition times and nets with high fanout.

Such paths are candidates for buffering or drive-cell resizing.

5. Create schematics of any paths you would like to see.

A schematic view provides contextual information and details about the path and its components. Such information is often a prerequisite to understanding problems on the path.

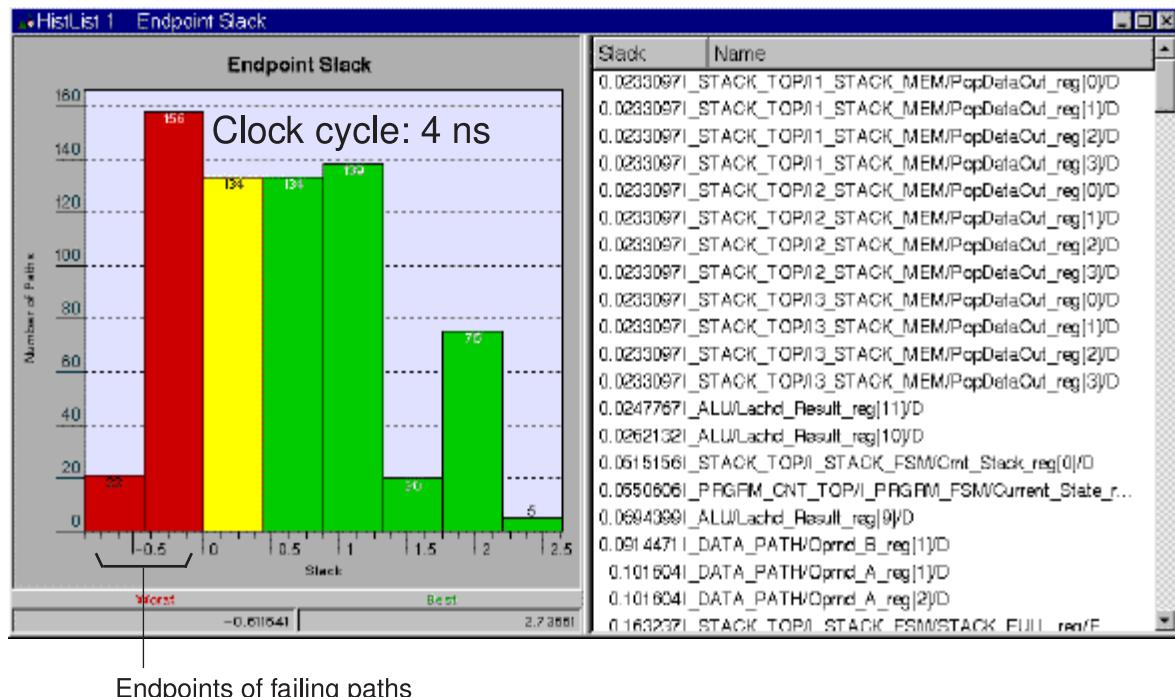
6. View fanin and fanout logic in schematics.

This step can provide useful information about the logic that drives, or is driven by, the problem path. For example, after viewing fanin or fanout, you might choose to resize cells in those logic cones.

## When Timing Violations Are Medium

[Figure 18](#) is a histogram of a design that is failing timing goals by margins that are between the large and small limits that are appropriate to your design methodology (for example, between 10 and 20 percent of the clock cycle). You can click a bin to see the endpoint names for paths that the bin contains. A bin is yellow when selected. In [Figure 18](#), one of the four bins containing endpoints of failing paths is selected.

*Figure 18 Design With Medium Timing Violations*



When negative slack values are medium, you can use the tool to investigate further and focus your recompile on a critical range of negative slack values for path groups. Focusing your compile effort on a critical range can improve worst negative slack and total negative slack.

Defining a critical range for path groups offers the advantage of concentrating compile effort and runtime on those areas that most need it.

To investigate and focus a recompile by defining a critical negative slack range for path groups,

1. Create a path slack histogram for each path group in your design.

Start with an arbitrary value of 1000 for the number of paths to include in each histogram. Raise or lower this value depending on the number of failing paths. The goal is to choose a value that shows all or nearly all of the failing paths.

2. Decide on a critical range for each path group (note the values for use in step 3).

When deciding on a critical range, choose a range that allows the tool to focus on the worst endpoint violations without too large an increase in runtime.

For example, some designers apply one of the following guidelines to decide on a critical range:

- Use a range that includes the worst 50 paths in a group.
- Use a range equal to one generic cell delay in your technology.

These are rough guidelines; for subsequent compiles you can adjust your critical range as necessary.

3. Set a critical range for each path group.

Using the values you decided in step 2, set the critical ranges for each path group with the `group_path` command. For example,

```
prompt> group_path -name my_clock -critical_range 0.25
```

4. Recompile the design.

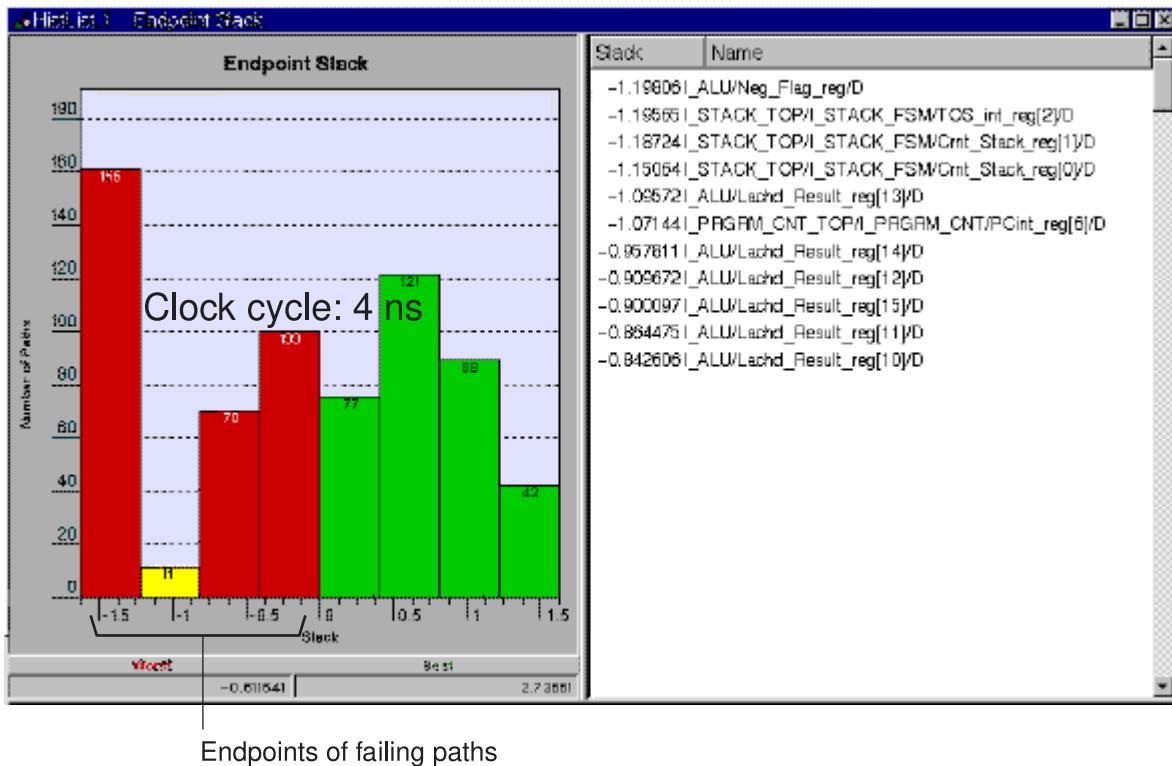
With a critical range defined, the compile effort is now focused. However, you can also choose to increase the compile effort over your previous compile. In the Compile Design dialog box, select medium or high effort. Select the Incremental mapping option to direct the tool to use the current netlist as a starting point for design improvements. An incremental compile can save runtime when your design does not require fundamental changes.

If suggestions in this section do not meet your timing goals, try applying the suggestions in [When Timing Violations Are Large on page 462](#).

## When Timing Violations Are Large

Figure 19 shows a design that is failing timing goals by a large margin. You can click a bin to see the endpoint names for the paths it contains.

Figure 19 Design With Large Timing Violations



Fixing large violations can require a high-level strategy to improve your design's performance. To fix large timing problems, consider any of the following changes:

- Modify your constraints.  
For example, increase the clock cycle or adjust time budgeting for the block or chip.
- Change the target technology.  
For example, target a higher performance technology.
- Modify the RTL.  
For example, you can move late-arriving signals such that you minimize their path length.

# 6

## Solving Floorplan and Congestion Problems

---

The Design Compiler Graphical tool Layout window in Design Vision tool provides tools that can help you to analyze and debug physical problems related to Design Compiler topographical synthesis. This chapter provides general and specific information about analyzing the physical placement of critical timing path objects, avoiding correlation issues that can result from incorrect or missing physical constraints, and visually examining floorplan-related congestion and identifying the causes of congestion hotspots.

For information about performing visual analysis in the Layout window, see the following sections:

- [Physical View Advantage](#)
- [Before You Start](#)
- [Preparing for Physical Analysis](#)
- [Viewing and Highlighting Selected Cells](#)
- [Using the Layout Window](#)
- [Visualizing the Physical Layout](#)
- [Validating Physical Constraints](#)
- [Analyzing the Floorplan](#)
- [Debugging QoR Issues Related to the Floorplan and Placement](#)
- [Visually Analyzing Congestion](#)

---

### Physical View Advantage

As part of the Design Compiler Graphical tool package, the Design Vision GUI provides the Layout window for viewing and analyzing the physical aspects of a design that you are optimizing by using the Design Compiler topographical technology. The Layout window contains a layout view that displays physical design information such as:

- Die area and core placement area
- Ports

- Cells, including standard cells, hard and soft macro cells, I/O cells, block abstractions, physical hierarchy blocks, black boxes, physical-only cells, cell keepout margins, and cell orientations
- Pins, including macro pins and I/O pads
- Physical constraints, including placement blockages, site rows, bounds, pin guides, preroutes (net shapes, vias, and user shapes), and tracks
- Relative placement groups
- Voltage areas

The Layout window is the physical design working environment for the GUI. Layout views provide the focal points for viewing and analyzing the physical layout of your design. The Layout window provides visually customizable layout views with the following tools:

- An Overview panel for quickly magnifying and traversing the active layout view or changing from one layout view to another
- A View Settings panel for controlling object visibility and selection and customizing object appearance in the active layout view
- Interactive left-button mouse tools that you can use to select, highlight, and query objects, magnify and pan your view of the design, and draw rulers to measure distances
- Lithographic and user grids that you can display or hide in the layout view
- Net Connections for examining connections between cells or pins in your floorplan
- A congestion map for identifying areas of high congestion in your floorplan
- Cell and pin density maps for identifying areas of high cell or pin density in your floorplan
- Visual modes for examining specific floorplan data in color overlays on the layout view

**Note:**

The standard cells are not visible by default in the Layout window. To view and select standard cells in the layout view, you must change the standard cell visibility and selection options on the View Settings panel.

---

## Controlling Object Visibility

You can visually inspect the layout data that you want to view while ignoring unrelated data by controlling which types of objects appear in the active layout view. To display or hide object types or subtypes, use the visibility options of the selected objects on the View Settings panel.

For information to display or hide object labels, see [Displaying or Hiding Object Labels](#).

**Note:**

The die area is always visible, so you cannot hide it.

If multiple layout views are open, you can set different visibility options for each view.

To display or hide different types of objects,

1. On the View Settings panel, set object visibility options as follows:

- Select button, to display a particular type of object.
- Deselect button, to display a particular type of object.

The check mark on the button indicates that the object type is visible.

2. Click Apply.

Object subtypes are categories of objects by property or attribute. For example, when cells are visible, you can display macro cells and hide standard cells.

To display or hide individual subtypes of a particular object type,

1. On the View Settings panel, make sure the object type visibility button is selected.
2. Click the plus (+) sign against the object type name.
3. Set object subtype visibility options as follows:
  - To display a particular subtype, select its option.
  - To hide a particular subtype, deselect its option.

The check mark on the option indicates that the object subtype is visible.

4. Click Apply.

To quickly select or deselect the visibility options for all types or subtypes of the object:

- To select the visibility options for all objects, click icon and select Objects > Show All.
- To deselect the visibility options for all objects, click icon and select Objects > Hide All.

- To select the visibility options for all the subtypes of an object type, move the pointer over the object type name or a subtype name.
- To deselect the visibility options for all the subtypes of an object type, move the pointer over the object type name or a subtype name.

### See Also

- [Changing Layout Display Properties](#)
- [Displaying or Hiding Object Labels](#)

---

## Controlling Object Selection

You can control which types of objects to select when you click or drag the pointer in a layout view. You enable or disable selection for all objects or particular types of objects by setting their selection options on the View Settings panel.

To select some object types and disable selection of other objects, you can select objects that you might not be able to select, such as objects that are hidden behind other objects.

If multiple layout views are open, you can set different selection options for each view.

To enable or disable selection for particular types of objects,

1. On the View Settings panel, select  button as needed:
  - To enable selection for an object type, select its  option.
  - To disable selection for an object type, deselect its  option.

A check mark on the  option indicates that the object type is enabled for selection.

2. Click Apply.

Object subtypes are categories of objects by property or attribute. For example, when cell selection is enabled, you can enable selection for macro cells and disable selection for standard cells.

To enable or disable selection for individual subtypes of a particular object type,

1. On the View Settings panel, make sure the object type visibility  button is selected.
2. Click the expansion button (plus sign) against the object type name.
3. Set object subtype options as needed.

A check mark on the  button indicates that the object subtype is enabled for selection.

4. Click Apply.

You can quickly select or deselect the selection options for all object types or subtypes:

- To select the selection options for all object types, click  icon and select Objects > Select All.
- To deselect the selection options for all object types, click  icon and select Objects > Unselect All.
- To select the selection options for all the subtypes of an object type, move the pointer over the object type name or a subtype name.
- To deselect the visibility options for all the subtypes of an object type, move the pointer over a the object type name or a subtype name.

**See Also**

- [Changing Layout Display Properties](#)
- [Changing Object Style Properties](#)

---

## Before You Start

Before you can view the physical layout of a design, you must

1. Provide any necessary physical design setup information, such as libraries, TLUPPlus files, preferred routing layer directions, and ignored layer settings
2. Link the design without any errors

For detailed information, see the *Design Compiler User Guide*.

You can view a design and analyze the physical aspects of a design in the Layout window before or after you optimize the design. Before optimization, the Layout window can display an elaborated GTECH design or a partially-synthesized design. Use the Layout window to

- Validate the physical constraints for your floorplan
- View the locations for block abstractions, physical hierarchy blocks, and preplaced macro cells

- View cross-selected standard cells that have been mapped to specific locations by either the `set_cell_location` command or topographical technology virtual placement
- Select the cells in a logic design view such as the hierarchy browser or a schematic view

If you select unmapped GTECH cells or mapped standard cells that have not been assigned a location, they appear at the layout view origin (0,0).

**Note:**

The bounds, relative placement groups, and the map and visual modes are not available in the Layout window until you optimize the design.

To view a design after optimization, you must optimize the design using the Design Compiler topographical technology. You can either optimize the design during the current session or load the optimized design from a .ddc file.

After optimization, the Layout window displays the optimized floorplan. You can

- Debug QoR Issues related to the physical aspects of your design, including
  - Why particular cells have a given drive strength
  - Why particular timing paths contain long buffer chains that are not related to high fanout
  - Why particular I/O paths contain high concentrations of buffers
  - What causes the huge transition or capacitance on particular pins
- Validate any user-defined physical constraints that you have applied to the design
- Analyze congested areas in the physical design

After performing QoR analysis, you can identify the next step, which might be one of the following:

- If there is a simple way to fix or eliminate the QoR issues, you might decide to continue with the back-end flow.
- If you identify problems in the design source, such as your RTL, timing constraints, or physical constraints, you might need to rerun synthesis with updated source files.

**See Also**

- [Preparing for Physical Analysis](#)
- [Using the Layout Window](#)

---

## Preparing for Physical Analysis

The following steps illustrate the typical setup tasks in the Design Vision tool before you can analyze a design in the Layout window:

1. Start the tool in topographical mode without the GUI by entering the following command:  

```
% design_vision -topographical_mode -no_gui
```
2. Set up the logic and physical libraries required for topographical mode.
3. Read in the .ddc netlist synthesized in topographical mode, and make sure that the design links correctly.
4. Open the GUI by entering the following command:

```
design_vision-topo> start_gui
```

5. Open the Layout window.

Alternatively, you can perform steps 2 through 4 by running a Tcl script. The following example shows a basic setup script:

```
source echo dct.setup.tcl  # Sourcing DC Ultra Topographical setup
read_ddc dct.opt.ddc  # Reading DC Ultra Topographical-synthesized .ddc
current_design top
link
start_gui
```

Design Compiler Graphical tool features are enabled with the DC-Extension license, in addition to any other licenses for your current design configuration. These features are available in topographical shell (dc\_shell-topo). If the DC-Extension license is not available, the tool issues the following error message:

Error: This site is not licensed for 'DC-Extension'. (SEC-51)

If you see this message, contact your local Synopsys representative.

### See Also

- [Before You Start](#)
- [Using the Layout Window](#)

---

## Viewing and Highlighting Selected Cells

You can identify the locations of cells and other objects in your floorplan by cross-selecting them in the logic design. For example, in the logic hierarchy view or a schematic view. The

selected objects appear in the specified color. The default color is white in the layout view. To display design information for a selected object use the Query tool.

You can perform the following tasks using the Query tool:

- Highlight selected objects that you need to continue viewing after you deselect them or select other objects.
- Cross-select and highlight timing paths and fanin or fanout logic. For example, select the objects in a schematic view.
- Select objects in a layout view if you want to view or highlight in a schematic view or in an another logic design view.
- Select highlighted objects in a schematic or a layout view.

### See Also

- [Viewing and Selecting Objects](#)
- [Selecting Objects in Graphic Views](#)
- [Querying Objects in Graphic Views](#)
- [Highlighting Objects or Timing Paths](#)
- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

---

## Using the Layout Window

The Design Vision Layout window in the Design Compiler Graphical tool has a similar user interface and the same look and feel as the IC Compiler tool Layout window. However, the Layout window in Design Compiler Graphical tool is designed to provide the features that you need to analyze and debug synthesis-related problems.

The Layout view provides the focal point for viewing and analyzing your physical floorplan constraints and congested areas in your design. To adjust display of the layout view, use the Overview panel and the View Settings panel examine objects and validate the applied constraints.

- Click or drag the pointer on the Overview panel to magnify and traverse the layout view. If multiple layout views are open, you can change the active view from one view to another.
- Set the options on the View Settings panel, including object visibility, object selection, and object display styles to change the layout view display properties.

The Layout window is not designed to be used for the following applications:

- Floorplan exploration

You cannot use the Layout window as a floorplan exploration tool because it does not allow you to view user-supplied physical constraints until after you have performed topographical-based synthesis.

- Floorplan or physical constraint editing

The Layout window does not allow you to change any physical constraints by using the layout view. You must apply all required physical constraints before running the `compile_ultra` command. The tool does not support physical constraint changes between multipass synthesis runs.

If you significantly change or update the .ddc data, the Layout window closes automatically.

## See Also

- [Before You Start](#)
- [Preparing for Physical Analysis](#)

---

## Opening the Layout Window

The layout view, Overview panel, and View Settings panel open by default when you open the Layout window. When you open the Layout window, all selected objects are deselected.

The layout window is an application window with its own menu bar, toolbars and panels, view windows, and status bar.

To open a layout window, click the Layout  button on the Layout toolbar or choose Window > New Layout Window.

The Design Vision tool deselects all selected objects, opens the layout window, and displays the floorplan in a layout view.

Before you can view the physical layout of a design, you must

- Provide any necessary physical design setup information, such as libraries, TLUPlus files, preferred routing layer directions, and ignored layer settings.

For more information, see the *Design Compiler User Guide*.

- Link the design without any errors.

To view a design that you optimized by using DC Ultra topographical technology, you can

- Optimize the design during the current session.
- Load the optimized design from a .ddc file.

For more information, see [Viewing the Floorplan in Design Compiler Graphical Tool](#). For information about optimizing the design during the session, see [Using Design Vision Tool in Topographical Mode](#).

In the active layout view, you can

- Select an object and view or change property values associated with the object.  
For more information, see [Viewing and Editing Object Properties](#).
- Highlight timing paths to view and check the cell placement for critical paths.

To select a timing path in the timing status summary or a path inspector, and highlight the selected path in the layout view. For details, see [Examining Timing Path Details](#) and [Highlighting Objects or Timing Paths](#).

- Measure distances between objects by drawing rulers  
For more information, see [Drawing Rulers](#).
- Display or hide the lithographic grid or the user grid.  
For more information, see [Displaying Grid Lines](#).
- Display or hide cell orientations.  
For more information, see [Displaying Cell Orientations](#).
- Display a congestion map to view and locate congestion problems.

The congestion map divides the core area into an array of colored boxes. These boxes indicate cell congestion and help you to determine whether the placement is routable. For details, see [Visually Analyzing Congestion](#).

- Display visual modes to view and examine placement quality.

A visual mode groups design objects or other design data into categories and applies a different color to each category. For details, see [Using Visual Modes](#).

You can perform the following in the layout window:

- Open multiple layout views in the same Layout window and work simultaneously with different areas of the design side by side.
- Open multiple instances of the layout window. Each instance has an unique name with an incremented number and displays the same flat view of the physical design.

You can open multiple layout views in the same layout window and work simultaneously with different areas of the design side by side. You can also open multiple instances of the layout window. Each instance has a unique name that includes an incremented number, but displays the same flat view of the physical design.

**Note:**

The layout window is not designed for floorplan or physical constraint editing. If you change the netlist or physical constraint data for a design when a layout window is open, for example by using netlist editing commands such as `change_link`, Design Vision immediately closes the layout window.

**See Also**

- [Using the Layout Window](#)

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## Performing Floorplan Exploration

Design Compiler Graphical tool allows you to perform floorplan exploration within the synthesis environment by using the IC Compiler tool floorplanning tools in the IC Compiler tool Layout window. Although, you use the IC Compiler tool Layout window, the interface between floorplan exploration in Design Compiler Graphical tool and the IC Compiler tool Layout window is transparent, allowing you to move seamlessly between the Design Vision tool and IC Compiler tool Layout windows.

Before performing floorplan exploration, you read the RTL file, specify the physical and logic libraries, define the Synopsys design constraints, specify a floorplan (if you have one), and synthesize the design in Design Compiler Graphical tool. After synthesis, you can evaluate the QoR results and use floorplan exploration to create a new floorplan or improve an existing floorplan. For more information, see the *Design Compiler User Guide*.

To choose commands from the Floorplan menu to set up and start a floorplan exploration session:

1. Choose Floorplan > Set Design Planning Options.

The Set Design Planning Options dialog box appears.

2. In the Work Directory text box, enter the name of your working directory with the relative path from the current directory.

The working directory stores the design planning scripts, floorplan files, and other files that are generated automatically during the floorplan exploration session. The default working directory is `dcg_link` below your current working directory.

3. In the ICC Executable text box, enter the name and location of the `icc_shell` executable that you intend to use for design planning.

By default, Design Compiler Graphical tool uses the `icc_shell` executable specified by your `$path` variable.

4. (Optional) In the File Name Prefix text box, enter the prefix you want to use in the file names for any generated files, such as the floorplanning scripts and floorplan files.

The default file prefix naming style is `%s_%d`, where `%s` is the design name and `%d` is the process ID.

5. (Optional) Select the Keep Files option if you want to retain the files that are generated automatically during the floorplan exploration session.

This option is deselected by default, which means the tool removes the generated files when you end the floorplan exploration session.

6. Click OK.

Alternatively, you can use the `set_icc_dp_options` command to set up a floorplan exploration session.

To start a floorplan exploration session,

- Choose Floorplan > Start Design Planning.

A message appears asking if you want to close the GUI. Click OK to start the floorplan exploration session.

Alternatively, you can use the `start_icc_dp` command to start the floorplan exploration session.

**Note:**

If you run floorplan exploration from a batch script with the `-f` option at the command line when you start the tool, the `start_icc_dp` command closes the GUI automatically before starting the floorplan exploration session.

Floorplan exploration in Design Compiler Graphical tool uses the IC Compiler tool layout window. By default, when you enable floorplan exploration, Design Compiler Graphical tool configures the IC Compiler tool layout window to include only the menus and menu commands to perform floorplanning. For more information, see the *Design Compiler User Guide*.

For detailed information, see the following documents:

- The *IC Compiler Help* for working with editing tools and commands in the IC Compiler tool layout window.
- The *Design Compiler Graphical Floorplan Exploration Application Note* for examples of flows to create a floorplan using Design Compiler Graphical tool floorplan exploration and to modify a floorplan to improve timing or congestion.

You can save the floorplan updates at any time during the floorplan editing session. The floorplan is saved in Design Compiler Graphical tool. You can also discard a saved floorplan.

To save or discard floorplan updates in the IC Compiler tool layout window,

1. Choose Floorplan > Update DC Floorplan.

The Update DC Floorplan dialog box appears.

2. Select an option to save or discard the floorplan file.
  - To save the current floorplan, select the Update DC with current floorplan option.  
If you have previously saved the floorplan, the tool overwrites it.
  - To remove a previously saved floorplan, select the Discard DC floorplan changes option and click OK.

3. Click OK.

When you exit the floorplan exploration session, you can

- Save the current floorplan
- Keep a previously saved floorplan
- Discard all the subsequent updates
- Discard all the floorplan updates including a saved floorplan

To exit a floorplan exploration session,

1. Choose File > Exit in the IC Compiler tool layout window.

The Exit IC Compiler dialog box appears.

2. Select an option to save or discard the floorplan.

- To save the current floorplan for Design Compiler Graphical tool and exit IC Compiler tool, select the Update DC with current floorplan option.
- To discard any floorplan changes that you have made, including a previously saved floorplan, and exit IC Compiler tool, select the Discard DC floorplan updates option.
- To keep a floorplan that you saved previously, discard any subsequent changes that you have not saved, and exit IC Compiler tool, select the Update DC with previously saved floorplan option.

3. Click OK.

The tool saves or discards floorplan changes as specified, exits IC Compiler tool, and returns to the Design Compiler Graphical tool. To view the floorplan changes immediately,

open the GUI and then open the layout window. To see how the changes that affect QoR results, you must first resynthesize the design.

For information about performing floorplan exploration in Design Compiler Graphical tool, see the *Design Compiler User Guide*.

### See Also

- [Using the Layout Window](#)
- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

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## Visualizing the Physical Layout

The Design Vision layout view, like the IC Compiler tool layout view, displays a flat representation of the physical design, and it can display only one top-level design at a time. You do not need to set floorplan constraints before viewing a design in the layout view.

You can cross-select design objects between schematic and layout views. This helps you to understand the functions of the selected cells. When you select logic design objects in the hierarchy browser or a schematic view, the objects are automatically cross-selected in the layout view.

Layout data can be densely packed with overlapping objects. You can control the visibility (display or hide) and selection (enable or disable) of individual object types by setting options on the View Settings panel. You can also customize object properties such as color and fill pattern, and set other layout and object display options. If you open multiple layout views, you can set different options for each view.

You can open multiple layout views in the Layout window. If you change settings in the active layout view and want to use the same settings in another layout view or during a future session, you can save them in your preferences file, `.synopsys_dc_gui/preferences.tcl`. You can also restore previously saved display properties by loading them from your preferences file.

**Note:**

The Design Vision Layout window is not designed for floorplan or physical constraint editing. If you change the netlist or physical constraint data for a design when the Layout window is open (for example, by using netlist editing commands such as `change_link`), the GUI immediately closes the Layout window.

You can visualize the physical layout as explained in the following topics:

- [Navigating Through Layout Views](#)
- [Displaying Grid Lines](#)
- [Displaying Cell Orientations](#)
- [Drawing Rulers](#)
- [Examining Block Abstractions and Physical Hierarchy Blocks](#)
- [Expanding Hierarchical Cells](#)
- [Examining Relative Placement Groups](#)
- [Examining Voltage Areas](#)
- [Analyzing Cell Connectivity](#)
- [Analyzing Cell Placement](#)
- [Analyzing Cell and Pin Density](#)
- [Analyzing CellMap Utilization](#)
- [Changing the Appearance of the Layout View](#)
- [Changing Layout Display Properties](#)

For more information, see [Viewing the Floorplan in Design Compiler Graphical Tool](#).

---

## Navigating Through Layout Views

In the Layout window, the Overview panel shows you what portion of the design is visible in each open layout view.

- The portion of the design displayed in the active layout view is shown as a solid yellow rectangle.
- The portions of the design displayed in other layout views are shown as solid gray rectangles.

To change the magnification of the design in a layout view,

1. On the Overview panel, move the pointer over the outline of the rectangle that represents the layout view until the pointer changes shape.
2. Drag a corner or edge in or out to resize the rectangle.

The magnification of the active layout view changes to display the portion of the design shown within the rectangle.

To traverse the design in a layout view,

1. Move the pointer inside the rectangle that represents the layout view.
2. Drag the rectangle to the area on the Overview panel that represents the portion of the design you need to display.
  - To traverse the design horizontally, drag the rectangle left or right.
  - To traverse the design vertically, drag the rectangle up or down.

The active layout view changes to display the portion of the design shown within the rectangle.

To change the active layout view, click anywhere inside the rectangle which represents the layout view that you want to make the active view.

You can use the Overview panel to magnify or traverse the design in the active layout view. When multiple layout views are open, you can change to a different layout view.

### See Also

- [Opening the Layout Window](#)
- [Overview Panel](#)
- [Magnifying or Shrinking a View](#)
- [Traversing a View](#)

---

## Displaying Grid Lines

You can display or hide the lithography grid and the user grid. Both grids are hidden by default.

Following are the options available to display the grid lines:

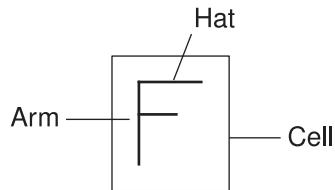
1. To display or hide the lithography grid, choose View > Grid > Show Litho Grid.
2. To display or hide the user grid, choose View > Grid > Show User Grid.
3. To switch between the default grid spacing and ten times the default grid spacing, choose View > Grid > Cycle grid spacing.

### See Also

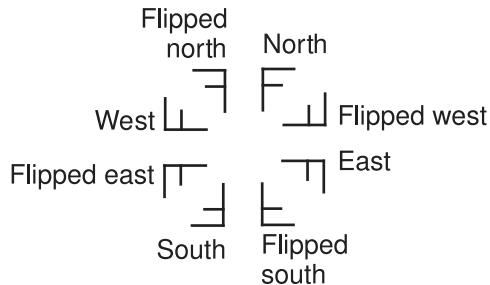
- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

## Displaying Cell Orientations

The GUI represents cell orientation in the layout view as F. The position of the “hat” of the F indicates the first direction; the “arm” indicates the second direction.



Cells can be oriented in any of the following ways:



To display cell orientations in the active layout view,

1. On the View Settings panel, make sure the button is selected.
  2. Click the Cell expansion button (plus sign).
  3. Select the Orientation option.
- A check mark on the option indicates that the cell orientations are visible.
4. Click Apply.

**Note:**

By default, you must click Apply on the View Settings panel to apply your changes to the active layout view. To enable the mechanism that automatically applies changes (instead of only when you click Apply), choose Auto Apply on the Show Options menu.

**See Also**

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

## Drawing Rulers

You draw rulers to measure distances in a layout view. For example, you can measure the distance between two cells or between two pins on a net.

A ruler can be composed of one or more horizontal, vertical, or diagonal segments. The distances from the beginning of the ruler are labeled at the ends of each segment and at every tenth tick mark within a segment.

While you draw a ruler segment, the GUI displays a preview image of the ruler in the layout view and displays the coordinates for the current pointer position on the status bar. The preview image indicates the distance between the initial point and the current pointer position.

To draw a ruler,

1. Click the Ruler tool button on the Mouse Tools toolbar or choose View > Mouse Tools > Ruler Tool.

The pointer becomes the Ruler Tool pointer ( ) and the Ruler tool options appear on the Mouse Tool Options toolbar. By default, cross hair rulers appear attached to the pointer in the layout view.

2. Click the location in the layout view where you want to begin the ruler.
3. (Optional) Set Ruler Tool options as needed on the Mouse Tool Options toolbar.
  - To draw single-segment rulers defined by an origin and an endpoint, select the Two point option.  
To draw multiple-segment rulers with each segment defined by a startpoint and an endpoint, select the Multi point option.
  - To control how ruler segments are drawn, select an option in the Angle list.  
To draw single horizontal or vertical ruler segments, select the X or Y option. This option is selected by default.
  - To draw both a horizontal segment and a vertical segment at the same time, select the X and Y option.  
To draw non-rectilinear ruler segments at any angle, select the Diagonal option.
  - To hide the cross hair rulers attached to the pointer in the layout view when you start a new ruler, deselect the Cross hair option. This option is selected by default.
  - To display labels that show the distance from the ruler origin to the midpoint of each ruler segment, deselect the Mid-line length option.

This option is deselected by default. When you select this option, the tool displays the mid-line length label for each ruler segment and updates the label for the current segment as you draw the segment.

- To hide labels that show the distance from the ruler origin to the endpoint of each ruler segment, deselect the End-point length option.

This option is selected by default, that is the tool displays the labels for each ruler segment and updates the label for the current segment as you draw the segment.

- To control which types of measurements the ruler labels display, select an option in the Tick label drop-down list.

The Ruler Distance option is selected by default, which means the labels display the relative distances from the ruler origin. To display the relative measurements from each segment origin, select the Segment Distance option. To display the relative distance from the ruler origin, select the Coordinate option.

- To control grid snapping for the ruler segments, select an option in the Snap to drop-down list.

The choices are Min Grid, User Grid, and Objects. The default is Min Grid, which means the ruler segments snap to the lithography grid.

- If you need to record the ruler segment lengths or distances in the session log, select the Log option.

4. Move the pointer in the direction that you want to draw the ruler segment, and click to define the segment.

To draw a diagonal segment, press the Shift key when you move the pointer.

5. Click where you want to end the ruler segment.

The ruler segment appears.

6. (Optional) To draw additional ruler segments repeat steps 2 through 4.

7. When you finish the last segment, press the Esc key.

To remove a ruler from the layout view,

1. Move the pointer over the ruler you need to remove.
2. Right-click and choose Remove Nearest Ruler.

To remove all rulers from the layout view, click the  button on the Mouse Tools toolbar (or choose View > Mouse Tools > Clear Rulers).

### See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Selecting a Mouse Tool](#)

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## Examining Block Abstractions and Physical Hierarchy Blocks

If your design contains block abstractions or physical hierarchy blocks, you should visually check them for correct site locations when you validate the floorplan. You should also visually check for block abstractions or physical hierarchy blocks in highly congested areas when you examine the congestion map.

Block abstractions are an extension to interface logic models. However, when you use block abstractions, the tool saves both the full design and the block abstraction information in the same .ddc file. When reading the design in as a block abstraction at the top level, the tool loads only the interface logic from the .ddc file.

**Note:**

Design Vision tool does not support interface logic models. Use block abstractions instead.

A physical hierarchy is a block that you create from a hierarchical cell by using the `set_physical_hierarchy` command. For information about this command, see the man page. The layout view displays a physical hierarchy as a rectangular block that indicates the area in which the leaf cells have been placed. You can view cell placement, pin placement, or net connections within the block by selecting the cells, pins, or nets in the hierarchy browser or a schematic view.

You can set options on the View Settings panel to control the visibility and selection of block abstractions and physical hierarchy blocks in the layout view and to change their color and fill pattern.

For more information about block abstractions and physical hierarchy models, see the *Design Compiler User Guide*.

### See Also

- [Expanding Hierarchical Cells](#)

## Block Abstractions

You can expand block abstractions in the layout view to display the objects (cells, ports, pins, nets, and so forth) inside the blocks. When block abstractions are expanded, you can view the placement of cells within the blocks.

Block abstractions are used in Design Compiler to reduce the number of design objects and the memory requirements when the tool performs top-level optimization on large designs.

A block abstraction is a structural model of a circuit that is displayed as a smaller circuit representing the interface logic of the block. All of the internal logic is retained, but only the interface logic is loaded when using the block abstraction.

If your design contains block abstractions, you should visually check the blocks for correct site locations when you validate the preplacement floorplan. You should also visually check for block abstractions in highly congested areas when you examine the congestion map.

To display block abstractions in the layout view,

1. On the View Settings panel, make sure the Cell visibility  option is selected.
2. Click the Cell expansion button (plus sign).
3. Select the ILM/Block Abstraction visibility (Vis) option.

A check mark on the option indicates that the block abstractions are visible.

4. Click Apply.

You can expand block abstractions to display the interface logic (cells, ports, pins, nets, and so forth) inside the blocks. When block abstractions are expanded, you can use the layout view to inspect the placement of the interface logic within the blocks.

To expand or collapse block abstractions,

1. On the View Settings panel, make sure the Cell and Block Abstraction visibility  options are selected.
2. Select the ILM/Block Abstraction visibility (Vis) option.
  - Use a positive integer to expand the block abstractions.
  - Use 0 to collapse the block abstractions.
3. Click Apply.

Block abstractions contain cells whose timing is affected by the external environment of the block. If you select a timing path that passes through a boundary pin into an expanded block abstraction, the layout view displays the selected path inside the block.

**Note:**

You can distinguish between block abstractions and physical hierarchy blocks by the value of the `cell_type` attribute, which you can view by using the

Query tool or the Properties dialog box. The cell type for a block abstraction is Block Abstraction. The cell type for a physical hierarchy block is Physical Hierarchy.

You can enable or disable selection for block abstractions, and you can change their color and other display style properties. For more information, see [Controlling Object Selection](#) and [Changing Object Style Properties](#).

## See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Changing Layout Display Properties](#)

## Physical Hierarchy Blocks

You can examine hierarchical cell placement in the layout view by creating and viewing physical hierarchy blocks. The layout view displays a physical hierarchy as a rectangular block that indicates the area in which the leaf cells are placed. You can view cell placement, pin placement, or net connections within the block by selecting the cells, pins, or nets in the hierarchy browser. The selected objects are cross-selected in the layout view and displayed in the selection color, which is white by default.

Before you can display a physical hierarchy block in the layout view, you must create the physical hierarchy by using the `set_physical_hierarchy` command and specifying the name of the hierarchical cell. For example, to create the physical hierarchy for a hierarchical cell named `hier_cell_1`, enter the following command:

```
design_vision-topo> set_physical_hierarchy hier_cell_1
```

Only hierarchical cells that the tool places by using the DC Ultra topographical technology can be converted to physical hierarchies. For more information about the `set_physical_hierarchy` command, see the man page.

You set the display properties for physical hierarchy blocks by using the same options on the View Settings panel that you use to set the display properties for block abstractions.

To display physical hierarchy blocks in the layout view,

1. On the View Settings panel, make sure the Cell visibility (Vis) option is selected.
2. Click the Cell expansion button (plus sign).
3. Select the Block Abstraction visibility (Vis) option.

A check mark on the option indicates that physical hierarchy blocks are visible.

4. Click Apply.

**Note:**

You can distinguish physical hierarchy blocks from block abstractions by the value of the `cell_type` attribute, which you can view by using the Query tool or the Properties dialog box. The cell type for a physical hierarchy block is Physical Hierarchy.

You can also enable or disable selection for physical hierarchy blocks, and you can change their color and other display style properties. For more information, see [Controlling Object Selection](#) and [Changing Object Style Properties](#).

**See Also**

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Controlling Object Visibility](#)
- [Browsing the Design Hierarchy](#)

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## Expanding Hierarchical Cells

You can expand hierarchical cells such as soft macros and block abstractions to view the logic (cells, ports, pins, nets, and so forth) inside them. When hierarchical cells are expanded, you can use Layout window analysis tools to analyze their internal cell placement. You can control the visibility and selection of these objects by using the same View Settings panel options you use for other objects in the layout view.

To expand hierarchical cells,

1. Select or enter a value greater than 0 in the Level box on the View Settings panel.
2. Click Apply.

To collapse (close) hierarchical cells,

1. Select or enter 0 in the Level box on the View Settings panel.
2. Click Apply.

**See Also**

- [Examining Block Abstractions and Physical Hierarchy Blocks](#)

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## Examining Relative Placement Groups

If your design contains relative placement groups, you should visually check the groups for correct site locations when you validate the floorplan. You should also visually check

for relative placement groups in highly congested areas when you examine the congestion map.

You can examine relative placement group structures in your floorplan by viewing them in the layout view. You can control the visibility, selection, and display properties of relative placement groups and the visibility of relative placement group labels in the active layout view by setting options on the View Settings panel.

If you have defined relative placement groups in your design, you can use the layout view to

- Determine how the DC Ultra topographical technology placed the relative placement groups, based on the constraints that you provided.

You should examine the size and location of each group.

- Determine how the DC Ultra topographical technology placed relative placement groups that are not constrained.

This allows you to find answers to such questions as what is the best topographical technology-derived location for a relative placement group.

- Examine the timing paths that pass through a relative placement group relative to other relative placement groups that they pass through.
- Debug the relative placement group constraints based on the visual feedback in the layout view.

Relative placement groups are not visible by default. You can display relative placement groups by selecting the  option for the RP Group object type on the View Settings panel. When relative placement groups are visible, you can

- Display information about a relative placement group on the Query panel by clicking the group with the Query tool.
- View the property values for relative placement groups by selecting the groups and choosing Edit > Properties.

## See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

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## Examining Voltage Areas

If your design contains voltage areas, you should visually check the areas for correct site locations when you validate the floorplan. You can examine the voltage areas in your floorplan by viewing and probing them in the layout view. You can control the visibility and

display properties of voltage areas and the visibility of voltage area labels in the active layout view by setting options on the View Settings panel.

If you have defined voltage areas in your design, you can use the layout view to

- Determine how the DC Ultra topographical technology placed the voltage areas. You should examine the size and location of each area.
- Select the standard cells in the hierarchical block related to a voltage area and examine them in the layout view to make sure they are all placed within the area outline.

You can also examine voltage areas by coloring them in a visual mode overlay on the layout view. For more information, see [Analyzing Cell Placement on page 488](#).

When voltage areas are visible, you can

- Preview a voltage area by moving the pointer over the voltage area to display its name and other information in an InfoTip.
- Display information about a voltage area on the Query panel by clicking the voltage area with the Query tool.

## See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

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## Analyzing Cell Connectivity

You can select an object and display the net connections in the layout view to see the locations of the objects that have net connections to the selected object. Net connections represent unrouted straight-line pin-to-pin connections.

A net connection shows the connection between the pins on two cells or a pin and a port. You can display net connection to all types of objects or just to macro cells, I/O cells, or other selected objects.

To display or hide the net connections,

1. In the Layout window, click the  button on the Analysis toolbar or choose View > Net Connections.  
The Net Connections panel appears.
2. Select a cell.

Net Connections appear between the selected cell and each cell to which it has a net connection.

To facilitate your analysis, you can adjust the net connection display and style characteristics in the active layout view by setting options on the Net Connections panel. You can set the following options:

- Select the type of cell connections to display

You can display net connections to all cells, macro cells, I/O cells, or selected cells

- Combine the individual net connections into a minimum span tree

- Skip one or more logic levels

- Set the maximum number of fanouts to display for a net

- Filter nets by type or name

You can display or hide net connections for signal nets, clock nets, power nets, and ground nets. You can include or exclude individual net connections by specifying net names or regular expressions

- Change the net connection color

You can also set an option to display information about the selected cell on the Query panel.

---

## Analyzing Cell Placement

You can analyze cell placement in your floorplan by using visual modes to display design objects or other data in a color overlay on the layout view. A visual mode allows you to focus on the objects of interest while dimming other visible objects.

A visual mode groups cells or other objects into categories called bins. The layout view displays the contents of each bin in a different color. You can set visibility options on the Visual Mode panel to display or hide the objects in each bin.

The Layout window provides the following visual modes:

- Snapshot visual mode

This is the default visual mode. You can analyze the placement quality of cells and other objects in your design by using snapshot visual mode to examine hierarchical cells and design logic in the layout view.

You can identify logic blocks and hierarchical cells, leaf cells, and macro cells by selecting them in the hierarchy browser or a schematic view and coloring their physical locations in the layout view. By using different colors for each cell or logic block, you can identify problems with the distribution of placed cells that can result in areas with poor timing or high congestion.

- Hierarchy visual mode

Use the hierarchy visual mode to display a high-level view of the placement quality of logic blocks and hierarchical cells in your physical design. You can color all the cells on a particular hierarchy level or just the hierarchical cells that you select. Each color represents a different hierarchical cell.

- **Voltage areas visual mode**

Use the voltage areas visual mode to display a high-level view of the placement quality of cells in the voltage areas of a multivoltage design. A voltage area is a placement area for core cells in a logic block that operates under a single voltage level. Each voltage area corresponds to one or more hierarchical cells in the logic design.

Voltage areas visual mode provides a separate bins for the cells in each voltage area and a bin for each of the following types of power management cells: regular level shifters, enable level shifters, always-on cells, and isolation cells.

- **Highlight visual mode**

Use the highlight visual mode to group highlighted objects by color. You can focus on the objects that you highlight with particular colors by displaying or hiding individual bins. You can also select all the objects in a bin.

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## Analyzing Cell and Pin Density

You can analyze cell density and pin density in your floorplan by using map modes to display a cell density map or pin density map in a color overlay on the layout view. A map mode allows you to focus on areas of high cell or pin density in your design while dimming other visible objects.

A cell or pin density map divides the core area into a grid of colored boxes. The boxes are colored and labeled to show the cell or pin density levels. Each map color represents a range of density values called a bin. The ranges are calculated between minimum and maximum thresholds.

The cell or pin density map legend displays the color, the data count, and optionally, the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of density values in the bins. You can set visibility options on the Map Mode panel to display or hide the densities in each bin.

For more information about map modes, see the following topics:

- [Analyzing Cell Placement](#)
- [Visually Analyzing Congestion](#)

## Analyzing CellMap Utilization

The CellMap Utilization available in the Map Mode panel enables you to display effective utilization for cells by allocating different kinds of site rows and various combinations to drive the optimization. It can also be invoked using the following Tcl command:

```
gui_show_map -window [gui_get_current_window -types Layout -mrui] \
-map {cellMap} -show true
```

You can reload the map data automatically if it is available at startup. If the map data is not available, you can click Reload from the Map Mode panel or invoke the following Tcl command to reload the data:

```
cm_density_map -reload [-grid_width <int>] [-grid_height <int>]
```

To adjust the CellMap Utilization settings,

1. Select the Value type from the drop-down list as either combined, short\_site, tall\_site, or short\_minus\_tall.
2. Adjust the Grid dimension.
3. Adjust the Grid size.
4. Select Solid filled grids checkbox to adjust the color in the grids. By default, it is unchecked.
5. Enter the number of bins. By default, the value is 10.
6. Select the Text checkbox to show the utilization values in the map. Only the current map value is displayed.

When you hover the pointer over a grid, following tips are provided:

<b>Query Point</b>	(324.876, 167.257)
<b>Combined Utilization:</b>	0.32026
<b>Short Site Utilization:</b>	0.00000
<b>Tall Site Utilization:</b>	0.00000
<b>Short-Tall Utilization:</b>	0.00000
<b>Total Area:</b>	811.920998
<b>Blocked Area:</b>	0.000000
<b>Free Area:</b>	811.920998
<b>Used Area:</b>	260.024259

**Note:**

The CellMap Utilization does not support multiple physical hierarchy.

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## Changing the Appearance of the Layout View

The View Settings panel provides options you can use to set display properties in the active layout view. You can also save the current settings in your preferences file, or load settings from the preferences file. If you open multiple layout views, you can set different options for each view.

You can set options on the View Settings panel to

- Control object visibility and selection
- Display or hide object labels
- Change object display styles such as colors or fill patterns
- Set layout view display options for cell orientations and cell keepout margins (display or hide), the brightness level, and the hierarchy level for block abstractions

You can set visibility or selection options or change style properties for object types or subtypes. Object subtypes are categories of objects by property or attribute. For example, when cells are visible, you can display core cells and hide macro cells.

By displaying or hiding particular object types, you can visually inspect just the physical layout data that you are interested in viewing while ignoring unrelated data. By enabling or disabling the selection of particular object types, you can control which types of objects are selected when you click or drag the pointer in a layout view.

## Setting Layout View Properties

Following are the options available in the layout view in the View Settings panel:

- To display or hide the View Settings panel, choose View > Toolbars > View Settings.

A check mark against the command on the Toolbars menu indicates that the View Settings panel is visible.

- To change layout view display properties in the active layout view, set options as needed on the View Settings panel, and then click Apply.

By default, when you change settings on the View Settings panel, you must click Apply before the changes take effect in the active view. If you prefer, you can set the panel to automatically apply your changes as soon as you make them.

- To enable or disable the automatic apply mechanism, choose Options > Auto Apply.

A check mark against the command on the Options menu indicates that the auto apply mechanism is enabled.

Alternatively, when the automatic apply mechanism is not enabled, you can reverse changes that you have not already applied.

- To reverse un-applied changes, choose Options > Cancel Changes.

You can customize how objects appear in the layout view by changing their style properties. Object styles set the appearance of objects in the active layout view. You can set the color, fill pattern, outline style, outline width, or exaggeration value for individual object types or layers.

The tool does not automatically save view settings when you close the GUI exit the session. If you change layout view settings during a session and want to use the same settings in a future session, you can save them in your preferences file. You can also restore previously saved view settings by loading them from your preferences file as follows:

- To save the current settings for the active layout view, choose Options > Preferences > Save to Preferences.
- To restore the most recently saved layout view settings, choose Options > Preferences > Set from Preferences.

## See Also

- [Changing the Appearance of the Layout View](#)

## Setting Layout Preferences

Use the Application Preferences dialog box when you need to change global default colors for layout views. You can change

- The background color
- The colors used for various objects and operations, such as object preview, selected objects, rulers, and grids
- The line style for the preview color
- The line width for the selection color
- Global defaults for various operations

To change the global layout view colors,

1. Choose View > Preferences.

The Application Preferences dialog box appears.

2. Select Layout Settings in the Categories tree.
3. Set color options as needed on the Layout Settings page.

For the selection and preview colors, you can hold the pointer over a color button to see the current settings in a tooltip.

- To change the background, foreground, or grid color, click the color button and select a color in the color palette.
- To change the selection or preview color, click the color button, choose Color on the menu that appears, and select a color in the color palette.
- To change the line style for the preview color, click the color button, choose Line Style on the menu that appears, and select a line style in the style palette.
- To change the line width for the selection color, click the color button, choose Line Width on the menu that appears, and type or select a width value.

4. Change global options as needed on the Layout Settings page.
  - To change the Selection tool behavior to add objects to the current selection, select the Click Adds to Selection, instead of replaces it option.  
By default, this option is deselected and the Selection tool replaces the current selection with the objects you select.
  - To change the vector settings, select Show drag vector during editing.
5. Click OK or Apply.

### See Also

- [Setting GUI Preferences](#)

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## Changing Layout Display Properties

You can change display properties for the active layout view by setting options on the View Settings panel. You can set object type options to

- Display or hide individual object types or subtypes
- Display or hide object labels for individual object type or selected objects
- Enable or disable selection for individual object type or subtypes
- Change style properties for individual object types or subtypes

You can set options individually or apply a predefined set of view settings called a preset. You can apply system presets provided by Design Vision tool or custom presets that you create.

In addition, you can

- Adjust the color brightness for all visible objects
- Display or hide cell orientations
- Expand or collapse block abstractions and physical hierarchy blocks

You expand block abstractions and physical hierarchy blocks to display the objects (cells, ports, pins, nets, and so forth) inside the blocks. When block abstractions and physical hierarchy blocks are expanded, you can use layout view analysis tools to analyze the placement of cells within the blocks.

To set layout view display properties,

1. Open the View Settings panel if it is not already open by choosing View > Toolbars > View Settings.

The View Settings panel appears. You can attach it to the left or right edge of the Design Vision window or move it to a different location inside or outside the window.

2. Set options as needed.

- To hide or display objects, click the Show all matching objects  button.
- To enable or disable object selection, click the Select all matching objects  option.
- To change object style properties, click the Clr button, select options as needed in the Select Style dialog box, and click OK.

3. (Optional) Set options for object subtypes as needed.

- a. Click the expansion button (plus sign) for an object type to display its subtypes.

You can quickly expand or collapse all object types. To expand all object types, right-click and choose Expand All. To collapse all object types, right-click and choose Collapse All.

- b. Repeat step 2.

4. Click Apply.

By default, you must click Apply on the View Settings panel to apply your changes to the active layout view. You can enable the mechanism that automatically applies changes when you make them, instead of only when you click Apply.

You can quickly select or deselect all the object visibility or selection options by choosing commands on the Show Options menu.

- To select all the object visibility options, click icon and select Objects > Show All.
- To deselect all the object visibility options, click icon and select Objects > Hide All.
- To select all the object selection options, click icon and select Objects > Select All.
- To deselect all the object selection options, click icon and select Objects > Unselect All.

To enable or disable the automatic apply mechanism,

- Click icon and select Auto apply.

A check mark next to the Auto apply command on the Show Options menu indicates that the automatic apply mechanism is enabled.

Alternatively, when the automatic apply mechanism is disabled, you can reverse changes that you have not already applied.

To reverse unapplied changes,

- Click icon and select Cancel changes.

When Show tooltips are enabled, you can view information about an option by holding the pointer over it.

To enable or disable toolTips,

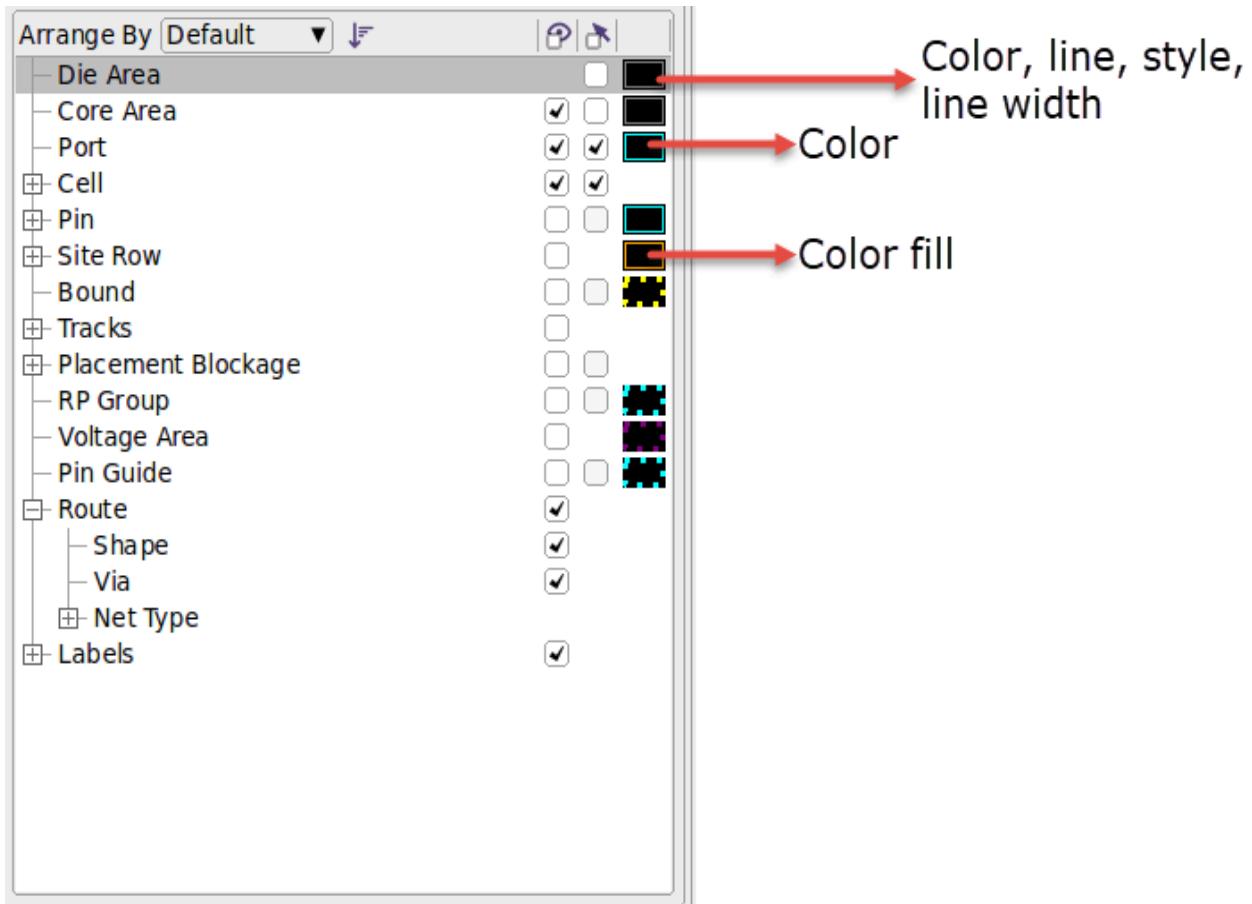
- Click icon and select Show tooltips.

If you change settings in the active view and want to use the same settings in another view or during a future session, you can save them in your preferences file. You can also restore previously saved view settings by loading them from your preferences file. For more information, see [Saving and Restoring View Settings](#).

**Note:**

Design Vision tool does not automatically save display properties when you close the GUI or exit the session.

The following figure shows the properties that are available for each object type and subtype:



### See Also

- [Adjusting the Color Brightness](#)
- [Saving and Restoring View Settings](#)
- [View Settings Panel](#)

## Setting Preset Options

You can configure the layout view by applying a predefined set of view settings called a preset. You can apply a system preset provided by Design Vision tool, or you can apply a custom preset that you create.

By default, when you open a layout window, the tool configures the layout view by using the view settings saved in your preferences file. To apply view settings from a preset, select the preset in the Preset list at the bottom of the View Settings panel.

When you change settings manually, by setting options on the View Settings panel, an asterisk sign (\*) appears in front of the preset name in the Preset list as follows:



- To reconfigure the layout view with the default view settings, select Default in the Preset list.
- To reapply the view settings from a preset, click the button next to the Preset list.

When you create a custom preset, you specify a preset name and the view settings that you want to include in the preset. You can create a new preset or redefine an existing custom preset. You cannot redefine a system preset.

To create a custom preset,

1. Click button and select Save preset as option.  
 The Write Layout Settings Preset dialog box appears.
2. Select an existing preset or enter a new preset name in the Select or type a preset name text box.
3. Set options to control which settings you want to include.

By default, the object displays properties from the Objects tab.

- a. To exclude object display properties, deselect the Objects option.
- b. To include object and layer style properties, select the Include color and pattern settings option.

4. Click OK.

The tool saves the preset and adds the preset name to the Preset list on the View Settings panel.

You can specify a preset as the default configuration when you open a new layout window or layout view.

To set a preset as the default layout view configuration,

1. Select the preset in the Preset list.
2. Click icon and select Set Default as default preset.

To reset the tool to automatically load the default settings, click the icon and select Set preferences as default for layout on the View Settings panel.

You can remove a custom preset but not a system preset.

To remove a custom preset,

1. Select the preset in the Preset list.
2. Click  icon and select Remove preset option.

## Displaying or Hiding Object Labels

You can control which types of object labels appear when the objects are visible in the active layout view. You can set options to display or hide the object labels for cells, ports, site rows, bounds, voltage areas, and relative placement groups.

To display or hide object labels in a layout view, you select or deselect options on the View Settings Panel. If multiple layout views are open, you can use the View Settings panel to set different visibility options for each view.

To display or hide object labels in the active layout view,

1. On the View Settings panel, select the Labels visibility (Vis) option.
2. Click the Labels expansion button (plus sign).
3. Set object label visibility (Vis) options as needed.
  - To display the labels for a particular type of objects, select its Vis option.
  - To hide the labels for a particular type of objects, deselect its Vis option.

A check mark on the Vis option indicates that the object labels are visible.

4. Click Apply.

As an alternative to displaying a label for every object, you can set an option to display an object's labels only when the object is selected.

To display labels for selected objects in the active layout view,

1. Select the Labels visibility (Vis) option on the View Settings panel.
2. Click the Labels expansion button (plus sign).
3. Click the Selected visibility (Vis) option.

A check mark on the Vis option indicates that the labels for selected objects are visible.

4. Click Apply.

### See Also

- [Controlling Object Visibility](#)
- [Controlling Object Selection](#)

## Changing Object Style Properties

Object style properties set the appearance of objects in the active layout view. You can customize the style properties for an object type by clicking its color button and setting options in the Select Style dialog box. You can change the object color, fill pattern, outline style, and outline width. The exact properties that you can change for an object type depend on its graphic representation in the active layout view.

**Note:**

The default style properties are set for optimal viewing and work well for most designs. However, you can change styles for objects if you need to customize the layout view for a particular design or working environment.

You change object style properties in a layout view by setting options on the View Settings panel. The types and subtypes of objects that you can customize have style buttons in the Clr column. If multiple layout views are open, you can set different object style options for each view.

To change style properties for an object type or subtype,

1. On the View Settings panel, click the color (Clr) button for an object type.

The Select Style dialog box appears.

**Note:**

To change properties for cells, you must expand the Cell object type to display the cell subtype options.

2. Change property settings as needed.

You can

- Select a color on the color palette

Alternatively, you can create a custom color. For details, see [Creating a Custom Color](#).

- Select a fill pattern on the fill palette
- Select an outline style on the line style palette
- Type a value, in pixels, in the Line width box

The preview box (New) displays the change.

3. (Optional) Repeat step 2 as needed until you are satisfied with the appearance of the preview box.
4. Click OK to close the Select Style dialog box.

The button on the View Settings panel changes to show the new styles.

5. (Optional) If you need to change styles for another object type repeat steps 2 through 4.
6. Click Apply.

### See Also

- [Controlling Object Visibility](#)
- [Controlling Object Selection](#)

## Creating a Custom Color

When you use the Select Style dialog box to change object style properties, you can either apply a standard color or create a custom color.

To create a custom color,

1. In the Select Style dialog box, click the Custom tab.
2. Select the hue and saturation by clicking in the color swatch (the box below the tabs).

The preview box (New) displays the new color.

Alternatively, you can type values in the Hue and Sat boxes.

3. Adjust the luminescence by clicking in the color gradient box or moving the slider up or down.

The preview box changes to show the luminescence.

4. (Optional) You can adjust the color definition by typing values in the Red, Green, or Blue boxes as needed.
5. (Optional) Repeat steps 2 through 4 as needed until you are satisfied with appearance of the color in the preview box.
6. Click OK.

Alternatively, if you know the color code for the color you want to create, you can skip steps 2 and 3 and type the codes in the Red, Green, and Blue boxes.

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## Validating Physical Constraints

The layout view provides visual feedback about the orientation and physical placement of physical design objects and constraints, such as

- Die area and core placement area
- Port locations
- Macro cell and pin locations
- Cell orientations and keepout margins
- Site rows with cell sites
- Bounds
- Pin guides
- Placement blockages
- Preroute net shapes, vias, and user shapes
- Relative placement groups
- Routing tracks
- Voltage areas
- Wiring keepouts

By visually examining these objects, you can avoid the correlation problems that can occur due to incorrect or missing physical constraints.

You can examine the physical constraints in your floorplan by viewing and probing them in the layout view in the following ways:

- Display or hide the core area, ports, cells, cell orientations and keepout margins, pins, site rows, bounds, placement blockages, preroute shapes and vias, relative placement groups, routing tracks, voltage areas, and wiring keepouts
- Select or highlight the die area, the core area, ports, cells, pins, bounds, placement blockages, relative placement groups, and wiring keepouts
- Query (display information about) the die area, the core area, ports, cells, pins, bounds, placement blockages, preroute shapes and vias, relative placement groups, voltage areas, and wiring keepouts

In addition, you can view object properties for the die area, the core area, ports, cells, pins, bounds, placement blockages, relative placement groups, and wiring keepouts by using the Properties dialog box (choose Edit > Properties).

By default, the core area, ports, cells, and preroutes are visible, and the other physical constraint object types are hidden when you open the Layout window. The die area is always visible. If your design contains preroutes, you should examine them to make sure the tool honors the other physical constraints when it creates the prerouted net shapes.

Physical constraint validation provides the following benefits:

- Helps you improve the physical constraints and achieve better results.

For example, you can identify the need for placement blockages to plug gaps between macros that the synthesis tool might consider free to use but your physical implementation tool does not use.

- Helps you identify mismatched results between Design Compiler topographical technology and the IC Compiler tool.

For example, incorrect application of physical constraints during synthesis can lead to ignored placement blockages in the physical implementation tool.

To examine physical constraints, you can

- Select individual objects or objects in a rectangular area

 Click the  button on the Mouse Tools toolbar, and then click an object or drag the pointer around the objects you want to select. For more details, see [Selecting Objects in Graphic Views](#).

- Preview object information in an InfoTip by holding the pointer over the object

The types of objects that you can preview depend on which mouse tool you are using. By default, the Selection tool is active and you can preview objects that are enabled for selection on the View Settings panel. When the Query tool is active, you can also preview preroutes. If multiple objects overlap, press F1 to cycle the InfoTip through the objects. You can enable or disable tool tips in the current view by choosing View > InfoTip. For more details, see [Previewing Objects in Graphic Views](#).

- Highlight individual objects or objects in a rectangular area

 Click the  button on the Mouse Tools toolbar, and then click an object or drag the pointer around the objects you want to highlight. For more details, see [Highlighting Objects or Timing Paths](#).

- Display object information on the Query panel

 Click the  button on the Mouse Tools toolbar, and then click the object. The object name and information such as the object's location and attribute values appear on the Query panel. For more details, see [Querying Objects in Graphic Views](#).

- Measure objects or distances between objects

 Click the  button on the Mouse Tools toolbar, and then click points or drag the pointer in the layout view to draw a ruler. For more details, see [Drawing Rulers](#).

- View object properties in the Properties dialog box

Select one or more objects, and then choose Edit > Properties. You can also change editable property values. For more details, see [Viewing and Editing Object Properties](#).

- View cell orientation symbols on cells

Select the  option for the Cell orientation subtype under the Objects on the View Settings panel, and then click Apply. For more details, see [Displaying Cell Orientations](#).

- Examine the placement quality of logic blocks and hierarchical cells in your physical design by coloring cells or cell hierarchies in the hierarchy visual mode

Choose View > Visual Mode, and then select Hierarchy in the list at the top of the Visual Mode panel. For details, see [Examining Cells by Hierarchy](#).

- Examine the placement quality of cells in the voltage areas of a multivoltage design by coloring the cells in the voltage areas visual mode

Choose View > Visual Mode, and then select Voltage Areas in the list at the top of the Visual Mode panel. For details, see [Examining Cells by Voltage Area](#).

## See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- [Saving an Image of a Window or View](#)

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## Analyzing the Floorplan

The Design Vision layout view lets you analyze physical constraints, timing, and congestion in your floorplan. You can visually examine floorplan constraints, critical timing paths, and global routing congestion, and gather information that can help you to guide later optimization operations in Design Compiler and other Synopsys tools.

To analyze the floorplan in a layout view, you can

- View cell-to-cell or pin-to-pin connectivity by displaying net connections
- Visually analyze floorplan-related congestion by viewing the congestion map
- Visually analyze block and cell placement by coloring objects with visual modes

For information about these subjects, see the following topics:

- [Examining Preroutes](#)
- [Displaying Net Connections](#)
- [Analyzing Congestion](#)

- [Viewing Cells in Congested Areas](#)
  - [Examining Global Route Congestion](#)
  - [Examining Cell Density](#)
  - [Examining Pin Density](#)
  - [Using Visual Modes](#)
  - [Examining Cells by Hierarchy](#)
  - [Examining Cells by Voltage Area](#)
  - [Examining Snapshots of Selected Objects](#)
- 

## Examining Preroutes

You can examine preroute structures in your floorplan by viewing and querying the net shapes, user shapes, and vias in the layout view. If your design contains preroutes, you should examine them to make sure the tool honors the physical constraints when it creates the prerouted shapes and vias. You can use the layout view to

- Verify that the DC Ultra topographical technology honors the net and user shape constraints
- Examine the size and location of each shape and the location of each via
- Examine the timing paths associated with the prerouted nets
- Debug the preroutes based on the visual feedback in the layout view

When preroutes are visible, you can display information about a preroute shape or via by clicking the shape or via with the Query tool. Preroutes are visible by default.

To display or hide preroutes,

1. Select or deselect the  option for the Route object type on the View Settings panel.  
A check mark on the option indicates that preroutes are visible.
2. Click Apply.

You can control the visibility of preroute shapes and vias in the active layout view by setting options on the View Settings panel. When shapes are visible, you can display or hide net shapes with different types of net connections (signal, clock, power, or ground) and user shapes (shapes with no net connection).

To display or hide preroute shapes and vias in the layout view,

1. Make sure the Route visibility (Vis) option is selected.
2. Click the Route expansion button (plus sign).
3. Select or deselect the Shape visibility (Vis) option to display or hide shapes.  
A check mark on the option indicates that shapes are visible.
4. Select or deselect the Via visibility (Vis) option to display or hide vias.  
A check mark on the option indicates that vias are visible.
5. Click the Net Type expansion button (plus sign).
6. Select or deselect visibility (Vis) options as needed to display or hide different types of shapes based on their net connections:
  - To display or hide different types of net shapes, select or deselect the Signal, Clock, Power, and Ground visibility options as needed.
  - To display or hide user shapes, select or deselect the No net visibility option.Check marks on options indicate the types of shapes that are visible.
7. Click Apply.

## See Also

- [Viewing the Floorplan in Design Compiler Graphical Tool](#)

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## Displaying Net Connections

The Net Connections Tool displays net connections between the driver and load pins of the nets of selected objects or, if the selected object is a route corridor or route corridor shape, it displays net connections from the pins of the route corridor's nets to the nearest route corridor shape.

The non-route corridor net connections have three modes:

- Aggregated Flylines - Displayed when the tracing mode is TraceAggregated (the default). In this mode the load and driver pins of the generated net connections are aggregated by their parent hierarchical cell, move bound, edit group, RP group, or voltage area. These aggregated net connections are displayed as a line, with counts of load or driver pins, from the center of each unique connected parent object pair. The types of parent objects are determined by which trace through options are selected. If the tracing is not tracing through hierarchical cells, edit groups, RP groups then these are included in set of parent object types. If the original selected object is an edit

group, a RP group, a move bound or a voltage area then these object types are also considered as parent object types.

- Pin-to-pin Flylines - Displayed when the tracing mode is TracePinToPin. In this mode the flylines are drawn for each start pin to all traced load pins (if the start pin is a driver pin) or all traced driver pins (if the start pin is a load pin.)
- By Levels - The tracing mode TraceByLevels controls tracing depth by the Driver and Load level options. The Net Connections tool counts each standard cell as a level with exception of buffer cells: if 'Ignore buffers' is on then buffers are not counted as levels. In addition, TraceByLevels mode supports different flyline colors for the selected driver and load pins for better visual feedback. Some options of the Net Connections tool are not applicable for this tracing mode.

To view the net connections from selected cells,

1. Click the button on the Analysis toolbar, or choose View > Net Connections.

The Net Connections panel appears.

2. Select a connectivity display type from the drop-down list.

You can display which objects have connections displayed as follows:

- Selected To All - Displays connections from selected objects to all connected objects.
- Selected To Selected - Displays connections from selected objects to connected objects if they are selected.
- Selected To Not Selected - Displays connections from selected objects to connected objects if they are not selected.

**Note:**

The tracing mode TraceByLevels supports Selected to Not Selected connectivity only.

3. Select any one of the trace through options:

- Buffers - Tracing continues through the buffer cell and level shifter (from the net of the input load pin to the net of the output driver pin or vice versa). By default, this option is selected.
- Hierarchy -Tracing hits a pin which represents a separate physical hierarchy then it continues tracing on the other net of the pin. For example, for a soft macro pin, the tracing continues from the net of the top physical port to the net of the child physical terminal or vice versa. By default, this option is selected.
- Inside nets - Tracing also includes the inside net of the selected pins (normally only the outside net is traced) which allows you to see the external and internal

connections at the same time. This option can be combined with the Through points option to see the full trace of a feedthrough connection when one of the soft macro pins is selected.

- Edit groups - When this option is disabled (the default) tracing stops at edit group interface nets (nets which connect from pins of cells inside the edit group to pins of cells outside the edit group) of an edit group.
- RP groups - When this option is disabled (the default) tracing stops at RP group interface nets (nets which connect from pins of cells inside the RP group to pins of cells outside the RP group) of the RP group.
- Move bounds - When this option is disabled tracing stops at move bound interface nets (nets which connect from pins of cells inside the move bound to pins of cells outside the move bound) of the move bound.

4. Set trace depth options as needed:

- Driver - Specifies the maximum number of levels to trace through starting from selected driver pin.
- Load - Specifies the maximum number of levels to trace through starting from selected load pin.
- Ignore buffers - Specifies whether to count the buffers as tracing level.

5. Net Types - Allows you to select which net types are considered when displaying net connections. Net types which are not enabled are not traced. By default only Signal nets are traced. You can optionally enable or disable Signal, Clock, Reset and Scan nets. At least one net type must be enabled. If all net types are disabled then the tool automatically reenables Signal nets.

**Note:**

This option is not currently supported for route corridors.

6. Set cell type options as needed. You can filter the displayed connection by the type of cell for the connection.

- Macro - Specifies whether to include or ignore macro cells.
- IO - Specifies whether to include or ignore IO cells.
- Standard cell - Specifies whether to include or ignore standard cells.

7. Set net connection options as needed:

- Through points - Checks which pins are traced through when finding the end connection point . The connection is then drawn as a connection graph which shows the start pin, end pin and the locations of all traced through pins.
- Full path - Displays each traced path. If it is disabled (the default) then the number of connections through each pin pair is displayed.
- Connected loads - Tracing does not restrict net connections to those from a driver to a load but also includes connections from a load to a load. This allows you to see all pins that connect to a load pin instead of just the pins that drive it.
- Query selected - Displays textual description of the connections is displayed in the query tool. The actual contents of the text depends on which options are set.
- Pin max fanout - Specifies the maximum fanout of the pins from the driver to the load. If the number of load pins connected to a driver pin exceeds this number, tracing is stopped and no flyline is displayed for this pin. If the Query selected option is enabled then a message is displayed in the query tool to inform about any pins exceeding this limit.
- Only show bundles - Displays connections whose driver or load pin belongs to a bundle.
- Min bundle bits - Specifies the minimum number of bits that a bundle must have. If a bundle has less than this number of bits then it is not considered as a bundle by the tool.

8. Aggregate Limits - The following options provide extra control over which net connections are displayed.

**Note:**

These options have no effect for route corridors.

- Number of connections - Specifies the minimum and maximum number of aggregated connections between two parent objects. If the connection count is less than the minimum or greater than the maximum then the flyline is not displayed.
- Min - Specifies the minimum number of connections. That is, if the number of aggregated connections is below this amount then the flyline is not displayed.
- Max - Specifies the maximum number of connections. That is, if the number of aggregated connections is above this amount then the flyline is not displayed.

9. To change the net connections appearance,

- Click the Color button.

The Select Style dialog box appears.

- Select a color in the color palette.

You can select a standard color or click the Custom tab and create a custom color. For details about custom colors, see [Creating a Custom Color](#).

The New preview box displays the selected color. Repeat this step until you are satisfied with the color in the preview box.

- Click OK to close the Select Styles dialog box.
- The Color button on the Net Connections panel changes to show the new color.
- Click Apply.
- Set appearance options as needed.
  - Connect Position - Determines the position at which the endpoint of a net connection is placed in a connected cell. By default, the net connection connects to the center of the cell but sometimes this can cause a confusing display. Therefore, the tool also allows the connection to be placed at any of the four corners of the cell (Center, Inside, Lower left, Lower right, Upper left, Upper right).
  - Max pixel width - Specifies the maximum pixel width for aggregated lines (which have a line thickness dependent on the number of connections).
  - Nets per pixel - Specifies the number of connections which causes an increase in line width for the aggregated connection net connections.

## Analyzing Congestion

You can use the congestion map to identify areas of high congestion in your design. You should examine the congestion map to determine whether the design is routable.

To display the congestion map for the current design,

- Click the  button on the Analysis toolbar, or choose View > Map Mode.

Alternatively, you can choose the Global Route Congestion command from the Map Mode menu on the Analysis toolbar.

The GUI dims the visible objects in the layout view and displays the Map Mode panel. If you have already generated congestion data during the session, the congestion map grid

appears on top of the design in the layout view. If the map does not appear, you must load the global route congestion (GRC) data. You can reload the data if it changes during the session.

To load or reload the congestion data,

1. Click the Reload button on the Map Mode panel.

The (Re)Calculate Global Route Congestion Map Data dialog box appears.

2. Click OK.

The congestion map divides the core area into a grid of colored boxes. Each box represents a vertical plane and a horizontal plane through which routes can pass. The left and bottom box edges are colored and labeled to show the usage-to-capacity ratios of routing tracks through the planes. Each map color represents a range of congestion values called a bin. The ranges are calculated by using a linear interpolation of the congestion data between minimum and maximum thresholds.

You can control how the tool calculates global route congestion (GRC) by selecting a congestion calculation option.

- To calculate congestion as the sum of the overflow for each layer, select the Sum of overflow for each layer option and click Apply.  
This option is selected by default.
- To calculate congestion as the total demand minus the total capacity, select the Total demand minus total supply option and click Apply.

For information about these global route congestion (GRC) calculations, see the *Design Compiler User Guide*.

To facilitate your analysis, you can

- Adjust the congestion ranges
- View map information in the legend on the Map Mode panel
- Display or hide individual map colors (bins)
- Display or hide map details (box edges, labels, or layers)

To adjust the congestion ranges,

1. Set the number of bins by typing or selecting a value in the Bins box.
2. Set the lower and upper congestion bounds by typing values in the From and To text boxes.
3. Click Apply.

The congestion map legend displays the color, the data count, and optionally the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of congestion values in the bins. You can use the visibility options on the left side of the legend to display or hide map colors for individual bins.

To display or hide map colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click **Apply**.

**Note:**

By default, when you change options on the Map Mode panel, the options turn blue; you must click **Apply** before the changes take effect in the layout view. You can enable a mechanism that automatically applies changes when you make them by choosing **Options > Auto Apply**.

For general information about working with the Map Mode panel, see [Map Mode Panel](#).

To display or hide map details,

1. Set the map display options as needed.
  - To display or hide the horizontal box edges, select or deselect the **Horizontal** option.
  - To display or hide the vertical box edges, select or deselect the **Vertical** option.
  - To display or hide congestion labels, select or deselect the **Text** option.
2. (Optional) To display just the congestion in the current design, select the **Current design only** option.

By default, the congestion map displays congestion in the current design and its subdesigns.

3. Click **Apply**.

You can also customize the map display for individual bins or configure the Map Mode panel for all Map modes. For details, see the following topics:

- [Changing Congestion Map Style Properties](#)
- [Configuring the Congestion Map](#)

You can generate and view a list of cells in a region that you define by drawing a rectangle in the layout view. You can also cross-probe the RTL for cells in congested areas. For details, see [Viewing Cells in Congested Areas](#).

### See Also

- [Map Mode Panel](#)
- [Using Visual Modes](#)
- [Displaying Net Connections](#)

## Changing Congestion Map Style Properties

Style properties determine how map mode data is displayed in the layout view. In the congestion map, you can change the color, fill pattern, or exaggeration for a bin on the Map Mode panel. By default, the data is colored by a bin's place in the color spectrum, and the fill pattern is determined by the map mode.

To change style properties for a bin,

1. On the Map Mode panel, move the pointer over the legend bar, and then right-click and choose Set Style.  
The Select Style dialog box appears.
2. Change style settings as needed by doing any of the following:
  - Select a color in the color palette.

Alternatively, you can create a custom color. For details, see [Creating a Custom Color](#).

- Select a fill pattern in the fill palette.
- Enter or select a value (in pixels) in the Exaggeration box.

Exaggeration defines the minimum size, in pixels, of an object that appears on the screen. For details, see [Configuring the Congestion Map](#).

The preview box (New) displays the changes.

3. (Optional) To change the appearance of the preview box repeat step 2.
4. Click OK to close the Select Style dialog box.
5. Click Apply on the Map Mode panel.

### See Also

- [Using Visual Modes](#)

## Configuring the Congestion Map

You can set global map mode options to

- Display or hide the following columns in the legend on the Map Mode panel:
  - Styles (color boxes)
  - Count (total values or items in each bin)
  - Exaggeration values
  - Histogram bars
  - Histogram bars for colors that are hidden in the layout view
- Set maximum, minimum, and midrange exaggeration threshold values for color exaggeration in the map display

Color exaggeration helps you to focus on the critical data in a map mode. Exaggeration defines the minimum size, in pixels, of an object that appears on the screen. The amount of exaggeration depends on the importance of the data; the most important data has the highest exaggeration values. Exaggerated objects are always visible on the screen.

The most significant exaggeration appears in large designs. In small designs, small shapes are always visible and exaggerating them is less significant.

To configure the Map Mode panel,

1. On the Map Mode panel, choose Show Options > Configure.

The Visual Mode Configuration dialog box appears.
2. Display or hide columns in the legend as follows:
  - Select the options for columns you want to display.
  - Deselect the options for columns you want to hide.
3. Change threshold values for the exaggeration range as needed.
  - To set the maximum threshold, select or type a value in the Top box.
  - To set the minimum threshold, select or type a value in the Bottom box.
4. (Optional) Set a mid-range threshold by selecting the Middle option and selecting or typing a value in the Middle box.

This value is applied to the median congestion range bin.
5. Click OK to close the dialog box.
6. Click Apply on the Map Mode panel.

## See Also

- [Using Visual Modes](#)

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## Viewing Cells in Congested Areas

When the congestion map is visible, you can view and select cells in congested areas of the design. Use the List by Congested Region dialog box to define a rectangular region and generate a list of the cells in congested areas within the region. This cell list includes only those cells that are in areas with a congestion threshold that is within the range specified on the Map Mode panel and is equal to or greater than 1. In addition, you can filter the cells by setting a minimum global route congestion (GRC) threshold.

You can select cells in the cell list to view or highlight them in the layout view, and you can filter the cell list by setting a minimum global routing congestion threshold. You can also save the cell list in a text file. In addition, you can cross-probe the RTL for cells in congested areas to identify the RTL code that might be causing the congestion.

To select and view cells in highly congested areas,

1. Click the List cells in congested region button on the Map Mode panel.

The List by Congested Region dialog box appears. Move this dialog box to a location on the screen where you can work with both the layout view and the congested region at the same time.

2. Define the shape and location for the region:

- To draw the region where you need it, select the  button and either click two points or drag the pointer in the layout view.
- To specify the exact coordinates for the region, deselect the  button and type the x- and y- coordinate values for the upper-left and lower-right corners in the Coordinates box.

3. Click Apply.

The cell names appear below the Coordinates box. Only cells in highly congested areas are listed.

4. (Optional) To filter the cells by their global route congestion (GRC) thresholds, enter a value in the GRC Threshold Minimum box.

Only cells that have a global route threshold value equal to or greater than this value appear in the dialog box.

5. Select cells in the list that you want to view in the layout view.

The layout view displays the selected cells in the selection color, which is white by default.

6. (Optional) To select and view other cells repeat step 5, or To list cells in a different area of the design repeat steps 2 through 5.

The List by Congested Region dialog box displays the cell list in either a tree view or a list view. The tree view appears by default. You select the view in the list at the bottom of the dialog box.

- The tree view contains rows that display the RTL file names, line numbers, and cell instance names in an expanding tree view and columns that display the RTL line number, maximum global route congestion (GRC) value, RTL origin, and cell reference name for each cell. You can expand a file name or line number by double-clicking the name or number or by clicking the expansion button (plus sign).

You can copy file names, line numbers, or cell names and paste them on the command line or in another tool, such as a text editor.

- The list view contains a row for each cell and columns for the cell instance name, cell reference name, cell path, `dont_touch` attribute value, `is_mapped` attribute value, `cell_library` attribute value, RTL file name, RTL origin (such as RTL, DATA\_PATH, DFT, CLKGT, and so forth), and RTL line number.

To select and view congested cells in the layout view,

- Select the cell names in the cell list in the List by Congested Region dialog box.

The layout view displays the selected cells in the selection color, which is white by default.

When you select a cell name, the List by Congested Region dialog box displays the RTL for the cell in the RTL text view below the cell list. You can also view the RTL for one or more cells in the RTL browser by selecting the cell names and clicking the Cross Probe button. Cross-probing cells in highly congested areas can help you to identify the RTL code that is causing the congestion. For more information, see [Cross-Probing Cells in Congested Areas](#).

To copy file names, line numbers, or cell names in the tree view,

1. Select the names and numbers you want to copy.
2. Right-click and choose Copy.

In the list view, you can quickly select or deselect all the cells in the list.

- To select all the cells, right-click and choose Select All.
- To deselect all the cells, right-click and choose Clear All.

You can sort the cell list alphanumerically by the contents of a column and resize individual columns in either view. You can also filter the cells in the list view by using the Filter List dialog box. For information about filtering the cells, see [Filtering Object Lists](#).

You can save the cell list data in a text file with a row for each cell. The column data is delimited by commas.

To save the cell list data in a file,

1. Click the Save List As button.

The Save Cell List As dialog box appears.

2. Select a file or type a file name in the File name text box.
3. Click Save.

#### See Also

- [Analyzing Congestion](#)
- [Map Mode Panel](#)
- [Cross-Probing Cells in Congested Areas](#)

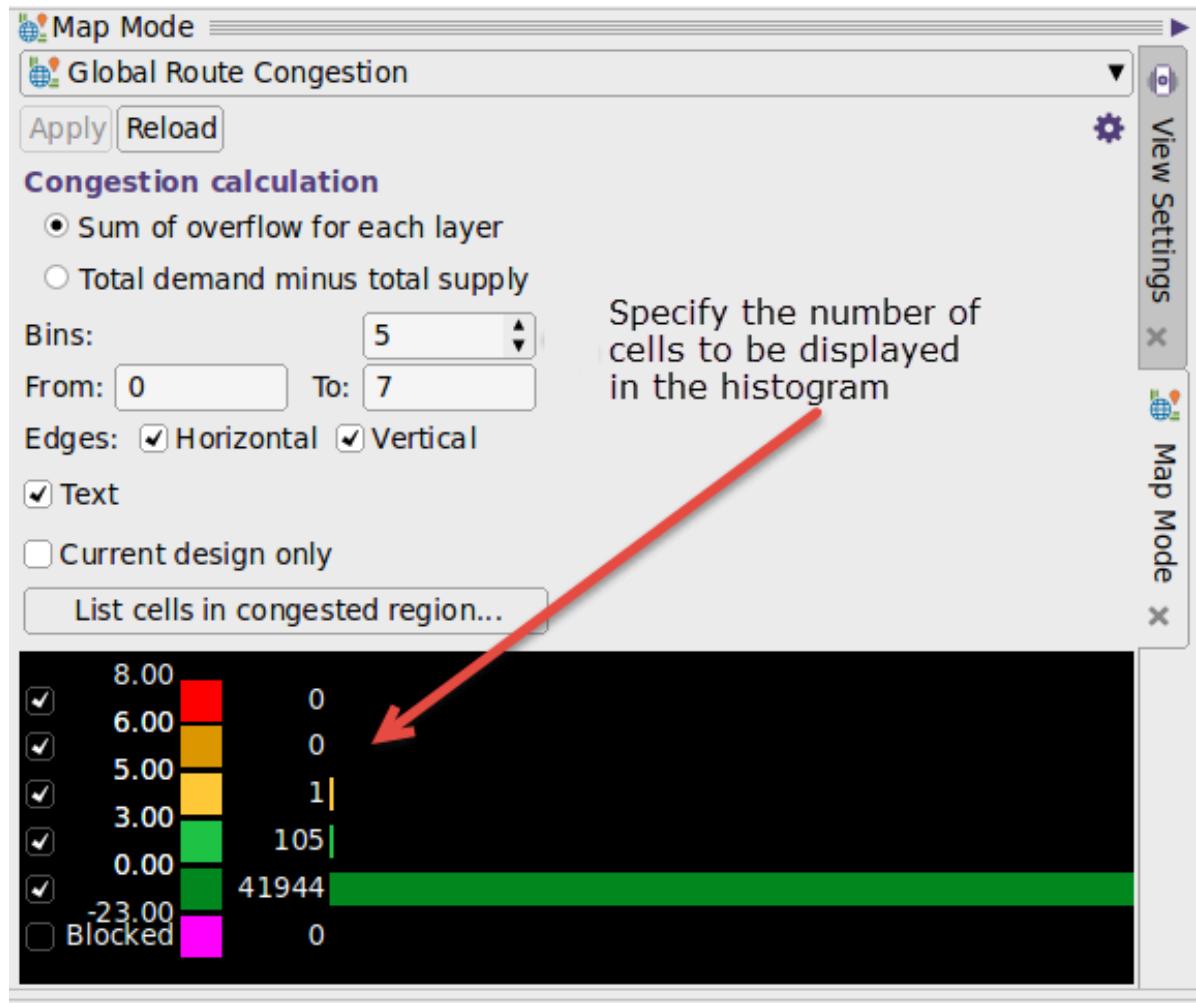
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## Examining Global Route Congestion

You can use the Global Route Congestion to display the congestion data as floating point numbers in the displayed histogram graph.

To display a Global Route Congestion for the current design,

1. Set the congestion threshold as needed.
  - a. Enter a value in the **Bins** box to display the specified number of buckets.



- b. Enter a value in the **From** and **To** text boxes to change the lower and upper congestion bounds.

The default range is between 0 to 7. The number can be a floating point number.

2. Click **List cells in congested region** on the **Map Mode** panel.

The List by Congested Region dialog box appears that displays the congestion data in floating point numbers.

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## Examining Cell Density

You can use the cell density map to identify areas of high cell density in the design or in a rectangular area of the design.

To display a cell density map for the current design,

1. Choose View > Map Mode.

The GUI dims the visible objects in the layout view and displays the Map Mode panel.

2. Select Cell Density in the list at the top of the Map Mode panel.

3. Click Reload.

The Cell Density Map Mode dialog box appears.

4. Select the Whole design area option.

5. Click OK.

To display a cell density map for an area of the current design,

1. Choose View > Map Mode.

The GUI dims the visible objects in the layout view and displays the Map Mode panel.

2. Select Cell Density in the list at the top of the Map Mode panel.

3. Click Reload.

The Cell Density Map Mode dialog box appears.

4. Select the Specified area option.

5. Define the shape and location for the area.
  - To define a rectangular area, either type the x- and y- coordinates for the upper-left and lower-right corners of the rectangle in the Coordinates box or make sure the  button is selected and drag the pointer in the layout view to form the rectangle where you need it.
  - To enable or disable grid snapping, select or deselect the  button.
  - To change the snapping option, click the  button and choose an option on the menu that appears.

6. Click OK.

The cell density map grid appears on top of the design in the layout view.

The cell density map divides the core area into a grid of colored boxes. The boxes are colored and labeled to show the cell density levels. Each map color represents a range of density values called a bin. The ranges are calculated between minimum and maximum thresholds.

To facilitate your analysis, you can

- View map information in the legend on the Map Mode panel
- Display or hide individual map colors (bins)
- Adjust the map grid display
  - Grid dimensions (height in number of standard cells)
  - Grid size (as a function of grid dimensions and number of bins)
  - Filled grids (solid color or fill pattern)
- Recalculate the cell density ranges

The cell density map legend displays the color, the data count, and optionally, the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of density values in the bins.

You can use the visibility options on the left side of the legend to display or hide the map colors for individual bins.

To display or hide map colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click Apply.

**Note:**

By default, when you change options on the Map Mode panel, the options turn blue. You must click Apply before the changes take effect in the layout view.

You can enable a mechanism that automatically applies changes when you make them by choosing Show Options > Auto Apply.

To adjust the map display, you can

1. Adjust the grid size by typing or selecting a value in the Grid dimension list.
2. Adjust the density ranges as needed.
  - To set the number of bins, type or select a value in the Bins box.
  - To set the lower and upper density bounds, type values in the From and To text boxes.

3. Set the map display options as needed.
  - To display solid colors in the density grid, select the Solid filled grids option.
  - To display or hide cell density labels, select or deselect the Text option.
  - To display just the cell density in the current design, select the Current design only option.

By default, the cell density map displays the density values in the current design and its subdesigns.

4. Click Apply.

You can also customize the map display for individual bins or configure the Map Mode panel for all Map modes. For details, see

- [Changing Style Properties in a Map Mode or Visual Mode](#)
- [Configuring Map Modes and Visual Modes](#)

#### See Also

- [Map Mode Panel](#)
- [Examining Pin Density](#)
- [Analyzing Congestion](#)
- [Analyzing the Floorplan](#)

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## Examining Pin Density

You can use the pin density map to identify areas of high pin density in the design or in a rectangular area of the design.

To display a pin density map for the current design,

1. Choose View > Map Mode.
- The GUI dims the visible objects in the layout view and displays the Map Mode panel.
2. Select Pin Density in the list at the top of the Map Mode panel.
  3. Click Reload to reload the pin density.
  4. Select the Whole design area option.
  5. Click Apply.

To display a pin density map for an area of the current design,

1. Choose View > Map Mode.

The GUI dims the visible objects in the layout view and displays the Map Mode panel.

2. Select Pin Density in the list at the top of the Map Mode panel.

3. Click Reload to reload the pin density.

4. Select the Specified area option.

5. Define the shape and location for the area.

- To define a rectangular area, either type the x- and y- coordinates for the upper-left and lower-right corners of the rectangle in the Coordinates box or make sure the



button is selected and drag the pointer in the layout view to form the rectangle where you need it.

- To enable or disable grid snapping, select or deselect the  button.

- To change the snapping option, click the  button and choose an option on the menu that appears.

6. Click Apply.

The pin density map grid appears on top of the design in the layout view.

The pin density map divides the core area into a grid of colored boxes. The boxes are colored and labeled to show the pin density levels. Each map color represents a range of density values called a bin. The ranges are calculated between minimum and maximum thresholds.

To facilitate your analysis, you can

- View map information in the legend on the Map Mode panel
- Display or hide individual map colors (bins)
- Adjust the map grid dimensions and fill
  - Grid dimensions (height in number of standard cells)
  - Grid size (as a function of grid dimensions and number of bins)
  - Filled grids (solid color or fill pattern)
- Recalculate the pin density ranges

The pin density map legend displays the color, the data count, and optionally, the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of density values in the bins.

You can use the visibility options on the left side of the legend to display or hide the map colors for individual bins.

To display or hide map colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click **Apply**.

**Note:**

By default, when you change options on the Map Mode panel, the options turn blue; you must click **Apply** before the changes take effect in the layout view. You can enable a mechanism that automatically applies changes when you make them by choosing **Show Options > Auto Apply**.

To adjust the map display, you can

1. Adjust the grid size by typing or selecting a value in the Grid dimension list.
  2. Adjust the density ranges as needed.
    - To set the number of bins, type or select a value in the Bins box.
    - To set the lower and upper density bounds, type values in the From and To text boxes.
  3. Set the map display options as needed.
    - To display solid colors in the density grid, select the Solid filled grids option.
    - To display or hide pin density labels, select or deselect the Text option.
    - To display just the pin densities in the current design, select the Current design only option.
- By default, the pin density map displays pin density values in the current design and its subdesigns.
- To display the number of pins per square micron within the grid or pins that overlap the grid, select the Pin per square micron option.
  - To display number of pins that are within the grid or overlap the grid, select Pin count.
4. Click **Apply**.

You can also customize the map display for individual bins or configure the Map Mode panel for all Map modes. For details, see

- [Changing Style Properties in a Map Mode or Visual Mode](#)
- [Configuring Map Modes and Visual Modes](#)

#### See Also

- [Map Mode Panel](#)
  - [Examining Cell Density](#)
  - [Analyzing Congestion](#)
  - [Analyzing the Floorplan](#)
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## Using Visual Modes

Visual modes are analysis tools you can use to examine specific design information with color overlays on the active layout view. A visual mode groups design data such as design objects, timing paths, or other information into categories or ranges called bins. The layout view displays the contents of each bin in a different color. You can use tools on the Mouse Tools toolbar to magnify and probe the design in critical areas.

When you enable a visual mode, the GUI dims the visible objects in the layout view by default and opens the Visual Mode panel. The name of the active visual mode appears in the list at the top of the Visual Mode panel.

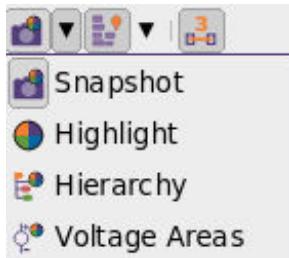
To display or hide the current or default visual mode,

- Click the visual mode button on the Analysis toolbar, or choose View > Visual Mode.

The visual mode button that appears on the Analysis toolbar changes to show the active visual mode (snapshot mode by default). After you disable visual mode, you can click the button to quickly redisplay the most recently active visual mode.

To display a different visual mode, you can

- Click the arrow button and choose a command from the Visual Mode menu on the Analysis toolbar.



- Select the visual mode name in the list on the Visual Mode panel.

You can view information about the active visual mode in the legend on the Visual Mode panel. Each bin displays the color and fill pattern, the data count (total number of objects in the category or values in the range), and optionally the color exaggeration value (hidden by default). The colored histogram bars on the right side of the legend represent the relative distribution of the objects or values.

In a visual mode that colors design objects, you can select or deselect the objects in each bin. In a visual mode that colors discrete, unrelated sets of objects or other information, you can reorder the bars in the legend.

Only one visual mode can be active at a time in the active layout view. If you need to examine more than one visual mode at the same time, you can either switch to a different visual mode or open multiple layout views and activate a different visual mode in each view.

The GUI dims the visible objects in the layout view, displays the Visual Mode panel, and enables the most recently active visual or snapshot visual mode by default.

To display a particular visual mode, you can

- Choose the command from the Visual Mode menu on the Analysis toolbar.
- Select the visual mode name in the list on the Visual Mode panel.

**Note:**

The visual mode button that appears on the Analysis toolbar changes to show the active visual mode (snapshot mode by default). After you disable visual mode, you can click the button to quickly redisplay the most recently active visual mode.

When the Visual Mode panel appears, you should move it to a location on the screen where you can work with both the layout view at the same time. You can dock the panel (attach it to a window edge) or move the panel outside the layout window.

To display or hide the Visual Mode panel,

- Choose View > Toggle Transient Toolbars.

Only one visual mode can be displayed in a layout view. If you need to examine more than one visual mode at the same time, you can either switch to a different visual mode or open multiple layout views and activate a different visual mode in each view.

The color legend on the Visual Mode panel displays a bin (row) for each object category or value range. You can use the visibility options on the left side of the legend to display or hide individual colors in the layout view.

To display or hide visual mode colors,

- Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
- Click Apply.

By default, when you change settings on the Visual Mode panel, you must click Apply before the changes take effect in the layout view. You can also set the panel to automatically apply your changes as soon as you make them.

To enable or disable the automatic apply mechanism,

- Choose Show Options > Auto Apply.

A check mark appears next to the Auto Apply command on the Options menu when the automatic apply mechanism is enabled.

Alternatively, when the automatic apply mechanism is disabled, you can reverse changes that you have not already applied.

To reverse unapplied changes,

- Choose Show Options > Cancel Changes.

You can view information in the legend about the active visual mode. Each bin displays the color and fill pattern, the data count (total number of objects in the category or values in the range), and optionally the color exaggeration value (hidden by default). The colored histogram bars on the right side of the legend represent the relative distribution of objects or values.

In visual modes that color design objects, you can select or deselect the objects in each bin. In visual modes that color discrete, unrelated sets of objects or other information, you can reorder the bars in the legend. For more information, see the following topics:

- [Selecting Objects in Visual Mode Bins](#)
- [Reordering Visual Mode Bins](#)

You can customize individual categories or ranges in a visual mode display by changing one or more of the following style properties:

- Color
- Fill pattern
- Exaggeration value

For more information, see [Changing Style Properties in a Map Mode or Visual Mode](#).

In addition, you can display or hide columns in the legend or adjust the exaggeration range for all visual modes. For details, see [Configuring Map Modes and Visual Modes](#).

For more information about using visual modes, see the following topics:

- [Examining Cells by Hierarchy](#)
- [Examining Cells by Voltage Area](#)
- [Examining Snapshots of Selected Objects](#)

## See Also

- [Visual Mode Panel](#)
- [Analyzing Congestion](#)
- [Displaying Net Connections](#)

## Reordering Visual Mode Bins

In visual modes that color discrete, unrelated sets of objects or other information, you can reorder the bars in the legend.

For example, you might need to reorder the bars to see the distribution of objects that belong to multiple categories. The layout view applies the overlay colors in order from bottom to top according to the order of the bars in the legend. If an object belongs to multiple categories, the object appears in the color of the bar closest to the top of the legend because it blocks the other colors.

### Note:

To see which objects in a category also belong to other categories, disable the visibility option for the category. Then the objects in multiple categories change to the color of the next-highest category to which they belong.

To reorder the legend bars,

1. To change the ordering of the histogram bars right-click on a histogram bar and select the appropriate option.
2.
  - To move the bar to the top of the legend, right-click and choose Move to top.
  - To move the bar up one place in the legend, right-click and choose Move up.
  - To move the bar down one place in the legend, right-click and choose Move down.
  - To move the bar to the bottom of the legend, right-click and choose Move to bottom.
3. (Optional) To reorder other bins as needed, repeat steps 1 and 2.
4. Click Apply.

## Selecting Objects in Visual Mode Bins

For visual modes that color discrete objects (such as design objects or timing paths), you can select (or deselect) the objects in one or more bins.

To select or deselect objects in visual mode bins,

1. Select the objects.
  - To select the objects in the bin and deselect any previously selected objects, right-click and choose Selection > Set Selection.
  - To add the objects in the bin to the current list of selected objects, right-click and choose Selection > Append to Selection.
  - To deselect the objects in the bin and remove them from the current list of selected objects, right-click and choose Selection > Remove from Selection.
2. (Optional) To select objects in other bins repeat steps 1 and 2.
3. Click Apply.

## Changing Style Properties in a Map Mode or Visual Mode

Style properties determine how map mode and visual mode data is displayed in the layout view. You can change the color, fill pattern, or exaggeration for a bin on the Map Mode or Visual Mode panel. By default, the data is colored by a bin's place in the color spectrum, and the fill pattern is determined by the map mode or visual mode.

To change style properties for a bin,

1. On the Map Mode panel or the Visual Mode panel, move the pointer over the legend bar, and then right-click and choose Set Style.

The Select Style dialog box appears.

2. Change style settings as needed by doing any of the following:

- Select a color in the color palette

Alternatively, you can create a custom color. For details, see [Creating a Custom Color](#).

- Select a fill pattern in the fill palette
- Enter or select a value (in pixels) in the Exaggeration box.

Exaggeration defines the minimum size, in pixels, of an object that appears on the screen. For details, see [Using Visual Modes](#).

The preview box (New) displays the changes.

3. (Optional) Repeat step 2 as needed until you are satisfied with the appearance of the preview box.
4. Click OK to close the Select Style dialog box.
5. Click Apply on the Map Mode panel or the Visual Mode panel.

#### See Also

- [Analyzing Congestion](#)

## Configuring Map Modes and Visual Modes

You can set global map mode and visual mode options to

- Display or hide the following columns in the legend on the Visual Mode panel:
  - Styles (color boxes)
  - Count (total values or items in the each bin)
  - Exaggeration values
  - Histogram bars
  - Histogram bars for colors that are hidden in the layout view
- Set maximum, minimum, and midrange exaggeration threshold values for color exaggeration in the visual mode display

Color exaggeration helps you to focus on the critical data in a visual mode. Exaggeration defines the minimum size, in pixels, of an object that appears on the screen. The amount of exaggeration depends on the importance of the data; the most important data has the highest exaggeration values. Exaggerated objects are always visible on the screen.

The most significant exaggeration appears in large designs. In small designs, small shapes are always visible and exaggerating them is less significant.

To configure the Map Mode or Visual Mode panel,

1. On the Map Mode panel or the Visual Mode panel, choose Show Options > Configure.  
The Visual Mode Configuration dialog box appears.
2. Display or hide columns in the legend as follows:
  - Select the options for columns you want to display.
  - Deselect the options for columns you want to hide.
3. Change threshold values for the exaggeration range as needed.
  - To set the maximum threshold, select or type a value in the Top box.
  - To set the minimum threshold, select or type a value in the Bottom box.
4. (Optional) Set a mid-range threshold by selecting the Middle option and selecting or entering a value in the Middle box.

This value is applied to the median visual mode bin.

5. Click OK to close the dialog box.
6. Click Apply on the Map Mode panel or the Visual Mode panel.

## See Also

- [Analyzing Congestion](#)
- [Displaying Net Connections](#)

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## Examining Cells by Hierarchy

The hierarchy visual mode provides a high-level view of the placement quality of logic blocks and hierarchical cells in your physical design. You can color all the cells on a particular hierarchy level or the just hierarchical cells that you select.

To color cells by hierarchy,

1. In the layout window, click the  button if it is visible on the Analysis toolbar, or click the  button to open the Visual Mode menu and choose Hierarchy.

The GUI dims the visible objects in the layout view and opens the Visual Mode panel. For details about other ways to display visual modes, see [Using Visual Modes](#).

2. Click Reload.

The Color By Hierarchy dialog box appears.

3. Set options as needed.

- To color all the cells at a particular hierarchy level, select the Color hierarchical cells at level option, and select a level in the list.
- To color selected hierarchical cells, select the Color specific hierarchical cells option, and select or browse for the cells.
- To remove coloring from all hierarchical cells, select the Clear all option.

4. Click OK or Apply.

The Hierarchy colors appear on the leaf cells in the layout view. Each color represents a different hierarchical cell. Each collection of cells with the same hierarchy color is called a bin.

To facilitate your analysis, you can view information about the hierarchical cells in the legend on the Visual Mode panel. The legend displays the color, the data count, and optionally, the color exaggeration level for each bin in the display. The colored histogram bars on the right side of the legend represent the relative distribution of leaf cells in the bins.

You can use the visibility options on the left side of the legend to display or hide the colors for individual bins.

To display or hide colors in the layout view,

- Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
- Click Apply.

**Note:**

By default, when you change options on the Visual Mode panel, the options turn blue; you must click Apply before the changes take effect in the layout view. You can enable a mechanism that automatically applies changes when you make them by choosing Show Options > Auto Apply.

For general information about working with the Visual Mode panel, see [Using Visual Modes](#).

You can also customize the visual display for individual bins or configure the Visual Mode panel for all visual modes.

## See Also

- [Changing Style Properties in a Map Mode or Visual Mode](#)
- [Configuring Map Modes and Visual Modes](#)

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## Examining Cells by Voltage Area

The voltage areas visual mode provides a high-level view of the placement quality of cells in the voltage areas of a multivoltage design. A voltage area is a placement area for core cells in a logic block that operates under a single voltage level. Each voltage area corresponds to one or more hierarchical cells in the logic design.

A visual mode collects objects into groups called bins and displays the objects in each bin with a different color. Voltage areas visual mode provides separate bins for the cells in each voltage area and a bin for each of the following types of power management cells:

- Regular level shifters
- Enable level shifters
- Always-on cells
- Isolation cells

To color cells by voltage area,

1. In the layout window, click the  button if it is visible on the Analysis toolbar, or click the  button to open the Visual Mode menu and choose Voltage Areas.  
The GUI dims the visible objects in the layout view and opens the Visual Mode panel. For details about other ways to display visual modes, see [Using Visual Modes](#).
2. Load the voltage area data, if necessary, by clicking the Reload button on the Visual Mode panel.

You must load the data when you display the voltage areas visual mode for the first time in a session. You can also click Reload when you need to update the visual mode data after modifying the design.

The layout view colors the voltage area cells and power management cells at full brightness and dims all other objects to 33 percent brightness. By examining the distribution of cells in the voltage areas, you can identify timing problems, such as timing paths between voltage areas that are too far apart or level shifters that are not placed in optimal locations.

To facilitate your analysis, you can view information about the voltage area cells in the legend on the Visual Mode panel. The legend displays the color, the data count, and

optionally, the color exaggeration level for each bin in the display. The colored histogram bars on the right side of the legend represent the relative distribution of leaf cells in the bins.

You can use the visibility options on the left side of the legend to display or hide the colors for individual bins.

To display or hide colors in the layout view,

- Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
- Click **Apply**.

**Note:**

By default, when you change options on the Visual Mode panel, the options turn blue. You must click **Apply** before the changes take effect in the layout view.

You can also enable a mechanism that automatically applies changes when you make them by choosing **Show Options > Auto Apply**.

For general information about working with the Visual Mode panel, see [Using Visual Modes](#).

You can also customize the visual display for individual bins or configure the Visual Mode panel for all visual modes.

**See Also**

- [Changing Style Properties in a Map Mode or Visual Mode](#)
- [Configuring Map Modes and Visual Modes](#)

---

## Examining Snapshots of Selected Objects

You can analyze the placement quality of cells and other objects in your design by using snapshot visual mode to examine hierarchical cells and design logic in the layout view.

You can quickly identify logic blocks (hierarchical cells), leaf cells and macro cells by selecting them in the hierarchy browser or a schematic view and coloring their physical locations in the layout view. By using different colors for each cell or logic block, you can identify problems with the distribution of placed cells that can result in areas with poor timing or high congestion.

To enable snapshot visual mode,

- In the layout window, click the  button if it is visible on the Analysis toolbar, or click the  button to open the Visual Mode menu and choose Snapshot.

The GUI dims the visible objects in the layout view and opens the Visual Mode panel. In snapshot visual mode, the snapshot toolbar buttons appear on the Visual Mode panel. For details about other ways to display visual modes, see [Using Visual Modes](#).

Snapshot visual mode groups selected cells or logic blocks into categories called bins and colors the contents of each bin with a different color in the layout view. By examining the distribution of objects with the same color and controlling which colors are visible, you can identify problems with the distribution of placed cells that can result in areas with poor timing or high congestion.

The Visual Mode panel contains a legend that displays information about the current mode. In snapshot mode, each bar in the legend displays the object names, total objects, and color for each bin.

To view the cell placement for one or more logic blocks,

1. In the hierarchy browser, select one or more hierarchical cells.

2. In the layout view, click the  button on the Visual Mode panel.

A new bin appears in the legend on the Visual Mode panel, and the color appears on the cells in the layout view.

3. (Optional) To color other logic blocks in the design, repeat steps 1 and 2.

If you identify problems with the distribution of placed cells, you can select individual cells, nets, ports, or pins in the hierarchy browser or a schematic view that you want to highlight in the layout view. By applying different snapshot colors, you can identify the physical representation of various design objects.

**Note:**

You can also identify design logic by selecting objects in a layout view and highlighting them in a schematic view.

To view the distribution of objects in the layout view,

1. In the hierarchy browser or a schematic view, select one or more cells, ports, pins, or nets.
2. In the layout view, click the  button on the Visual Mode panel.

A new bin appears in the legend on the Visual Mode panel, and the color appears on the objects in the layout view.

3. (Optional) To show other objects or cells in different colors repeat steps 1 and 2.

You can view information about the snapshot bins in the legend on the Visual Mode panel. The colored bars in the legend correspond to the colored objects in the layout view. In the histogram column on the right side of the legend, the width of the bars represents the relative distribution of the objects.

To facilitate your analysis, you can display or hide snapshot bin colors in the layout view.

To display or hide snapshot bins in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click **Apply**.

**Note:**

By default, when you change options on the Visual Mode panel, the options turn blue; you must click **Apply** before the changes take effect in the layout view. You can enable a mechanism that automatically applies changes when you make them by choosing **Show Options > Auto Apply**.

You can add or remove bins in snapshot visual mode by clicking buttons on the Visual Mode panel.

- To add a new, empty bin, click the  button.
- To remove one or more bins, select the bins and click the  button.
- To remove all of the bins, click the  button.

You can also add or remove objects in a bin.

- To add objects to a bin, select the objects, select the bin on the Visual Mode panel, right-click and choose **Selection > Set Selected**.
- To replace the contents of a bin with the objects in the current selection, select the objects, select the bin on the Visual Mode panel, right-click and choose **Selection > Append to Selected**.
- To remove objects from a bin, select the objects, select the bin on the Visual Mode panel, right-click and choose **Selection > Remove from Selected**.

For general information about working with the Visual Mode panel, see [Using Visual Modes](#).

You can also customize the visual display for individual bins or configure the Visual Mode panel for all visual modes.

#### See Also

- [Changing Style Properties in a Map Mode or Visual Mode](#)
- [Configuring Map Modes and Visual Modes](#)

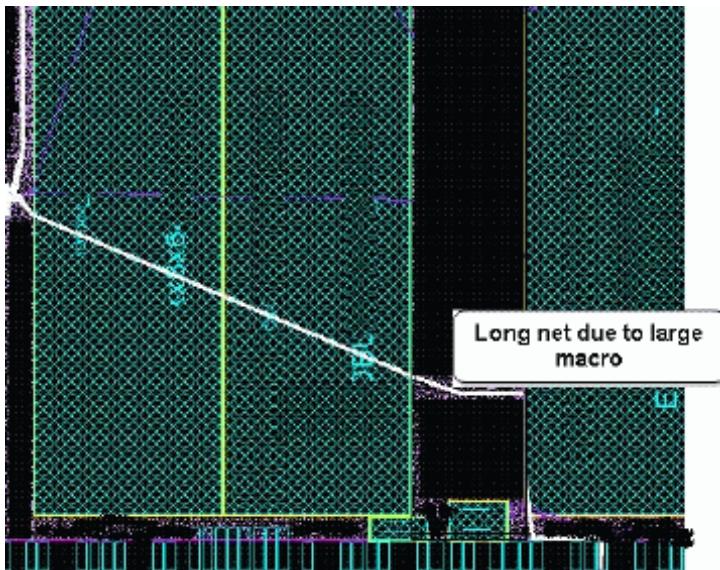
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## Debugging QoR Issues Related to the Floorplan and Placement

The Design Vision layout view allows you to debug the physical design problems that cause QoR degradation, especially timing degradation. The layout view provides visual feedback about the physical placement of timing path objects. By visually examining the critical path in the layout view, you can find answers to questions as

- Why are certain cells of a given drive strength?
- Why does a path contain long buffer chains that are not related to high fanout?
- Why are certain cells placed at a physical distance from the rest?
- Why are there high concentrations of buffers on I/O path?
- Why is there high transition or capacitance on pins?

You can query and highlight design objects on the critical path to find answers to these questions that help you understand Design Compiler topographical placement and the problems that can cause timing degradation. For example, you can perform critical path analysis in the layout view to identify the kinds of physical problems that can cause QoR degradation, such as why a long net is on the critical path.



For more information, see the following topic:

- [Viewing the Critical Path](#)

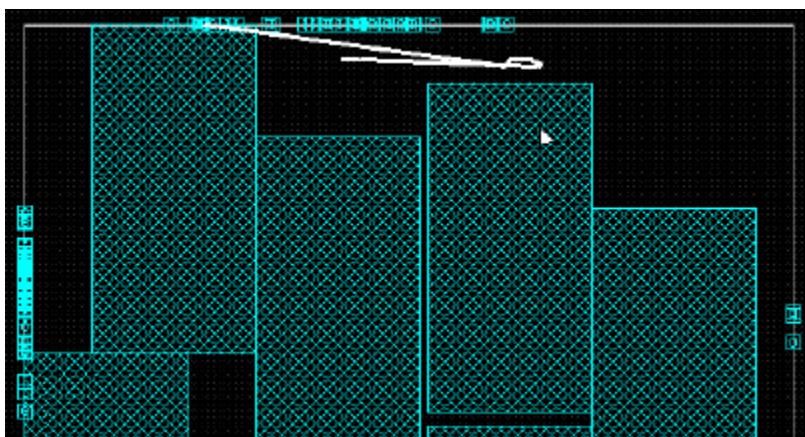
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## Viewing the Critical Path

To view the critical path,

1. In the Design Vision window, choose Timing > Timing Status Summary.
2. In the Timing Status Summary select the path with the worst negative slack.

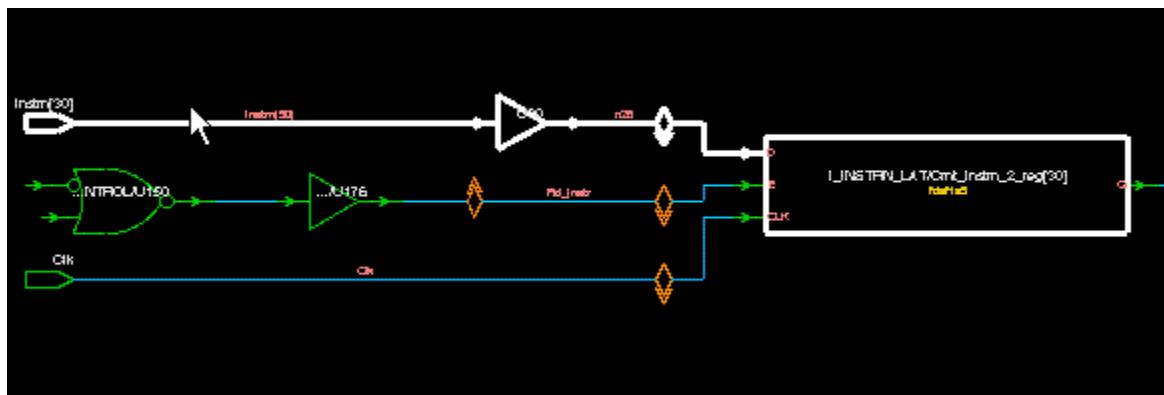
The selected path is automatically cross-selected in the layout view.



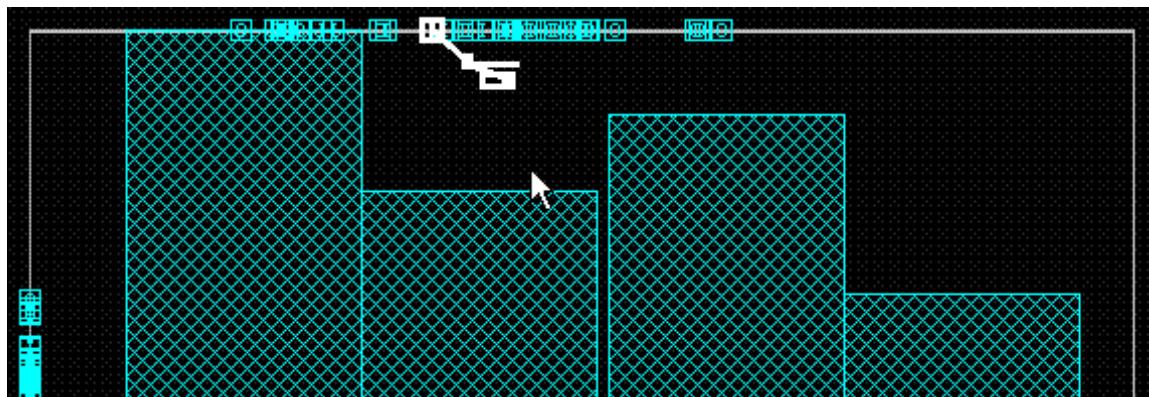
You can analyze the critical path to understand the Design Compiler topographical placement. The following example demonstrates one way to identify why the path startpoint is at a particular location:

1. Select the path startpoint in a schematic view.
2. Choose Select > Fanin/Fanout to open the Select Fanin/Fanout dialog box.
3. Select the Fanin option, set other options as needed, and click OK.
4. Select the startpoint and its input path in the schematic view.

The schematic view displays the startpoint and its input path in the selection color.



The selected logic is automatically cross-selected in the layout view.



For more information, see [Examining Timing Path Details](#) and [Selecting Fanin or Fanout Logic](#).

## See Also

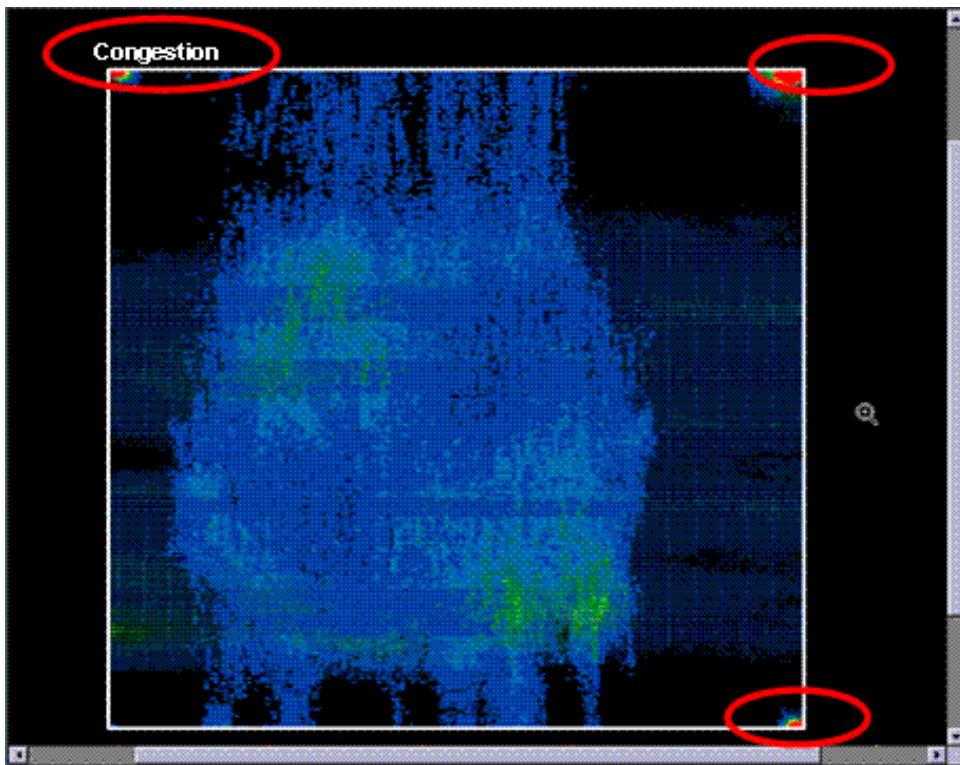
- [Debugging QoR Issues Related to the Floorplan and Placement](#)

## Visually Analyzing Congestion

You can identify areas of high congestion in your design by viewing the congestion map. By visually examining congested areas in your design, you can determine whether the design is routable and identify the causes of the congestion if the design is not routable. You can display or hide the congestion map at any time when a layout view is open in the Layout window.

[Figure 20](#) shows an example of congestion resulting from the layout of the floorplan.

*Figure 20     Floorplan Congestion in Layout View*



For information about viewing the congestion in the layout view, see the following sections:

- [Displaying the Congestion Map](#)
- [Viewing the Congestion Map](#)
- [Examining Cells in Congested Areas](#)

For more information about analyzing congestion, see the *Design Compiler User Guide*.

---

## Displaying the Congestion Map

To display or hide the congestion map,

- In the Layout window, click the Global Route Congestion  button on the Analysis toolbar or choose View > Map Mode.

The GUI dims the visible objects in the layout view and displays the Map Mode panel. If you have already generated congestion data during the session, the congestion map grid appears on top of the design in the layout view. If the map does not appear, you must load the congestion data. You can reload the data if it changes during the session.

To load or reload the congestion data,

1. Click the Reload button on the Map Mode panel.
2. Click OK in the dialog box that appears.

The congestion map divides the core area into a grid of colored boxes. Each box represents a vertical plane and a horizontal plane through which routes can pass. The left and bottom box edges are colored and labeled to show the usage-to-capacity ratios of routing tracks through the planes. Each map color represents a range of congestion values called a bin. The ranges are calculated by using a linear interpolation of the congestion data between minimum and maximum thresholds.

---

## Viewing the Congestion Map

You can view map information in the legend on the Map Mode panel, and you can display or hide individual map colors (bins). The legend displays the color, the data count, and optionally, the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of congestion values in the bins. You can use the visibility options on the left side of the legend to display or hide map colors for individual bins.

You can control how the tool calculates global route congestion (GRC) by selecting a congestion calculation option.

- To calculate congestion as the sum of the overflow for each layer, select the Sum of overflow for each layer option and click Apply.

By default, this option is selected.
- To calculate congestion as the total demand minus the total capacity, select the Total demand minus total supply option and click Apply.

For information about these global route congestion (GRC) calculations, see the *Design Compiler User Guide*.

You can facilitate your congestion analysis by

- Displaying or hiding map details map colors in the layout view
- Displaying or hiding map details (box edges or labels)
- Adjusting the congestion ranges
- Viewing map information in the legend on the Map Mode panel

The congestion map legend displays the color, the data count, and optionally the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of congestion values in the bins. You can use the visibility options on the left side of the legend to display or hide map colors for individual bins.

To display or hide map colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click Apply.

**Note:**

By default, when you change options on the Map Mode panel, the options turn blue. Click Apply for the changes to appear in the layout view. You can enable a mechanism that automatically applies changes when you make them by choosing Show Options > Auto Apply.

To display or hide map details,

1. Set the map display options as needed.
  - To display or hide the horizontal box edges, select or deselect the Horizontal edges option.
  - To display or hide the vertical box edges, select or deselect the Vertical option.
  - To display or hide congestion labels, select or deselect the Text option.
2. (Optional) To display just the congestion in the current design, select the Current design only option.

By default, the congestion map displays congestion in the current design and its subdesigns.
3. Click Apply.

To adjust the congestion ranges,

1. Set the congestion thresholds as needed.
    - To change the number of congestion ranges (bins), select or type a value in the Bins box.
    - To change the lower and upper congestion bounds, type values in the From and To boxes.
  2. Click Apply.
- 

## Examining Cells in Congested Areas

When the congestion map is visible, you can view and select cells in congested areas of the design by using the List by Congested Region dialog box to define a rectangular region in the layout view. The dialog box lists the cells in congested areas within the region. This list includes only the cells in areas with a congestion threshold that is within the range specified on the Map Mode panel and is equal to or greater than 1.

You can select cells in the cell list to view or highlight them in the layout view, and you can filter the cell list by setting a minimum global routing congestion (GRC) threshold. You can also save the cell list in a text file. In addition, you can cross-probe the RTL for cells in congested areas to identify the RTL code that might cause the congestion.

To select and view cells in a congested region,

1. Click the List cells in congested region icon on the Map Mode panel.

The List by Congested Region dialog box appears. You can move this dialog box to a location on the screen where you can work with both it and the layout view at the same time.

2. Define the shape and location for the region by doing one of the following:

- Drag the pointer in the layout view to form the rectangle where you need it.
- Click the  icon in the List by Congested Region dialog box and enter the x- and y-coordinates for the upper-left and lower-right corners of the rectangle in the Coordinates box.

3. Click Apply.

The names of the cells in the region appear in the Cell Name list. Only cells in highly congested areas are listed.

4. (Optional) To filter the cells by their global route congestion (GRC) thresholds, enter a value in the GRC Threshold Minimum box.

Only cells that have a global route threshold value equal to or greater than this value appear in the dialog box.

5. (Optional) To list cells in a different area of the design repeat steps 2 through 4.

The List by Congested Region dialog box displays the cell list in either a tree view or a list view. The tree view appears by default. You select the view in the list box at the bottom of the dialog box. Use the tree view to cross-probe congested areas. Use the list view to examine the cells in the congested areas.

- The tree view displays rows for the RTL file names, line numbers, and cell instance names and columns for the RTL line number, maximum global route congestion (GRC) value, RTL origin, and cell reference name.

You can expand a file name or line number by double-clicking the name or number or by clicking the expansion button (plus sign).

You can copy file names, line numbers, or cell names and paste them on the command line or in another tool, such as a text editor.

- The list view displays a row for each cell and columns for the cell instance name, cell reference name, cell path, `dont_touch` attribute value, `is_mapped` attribute value, `cell_library` attribute value, RTL file name, RTL origin (such as RTL, DATA\_PATH, DFT, CLKGT, and so forth), and RTL line number.

To select and view congested cells in the layout view,

- Select the cell names in the cell list in the List by Congested Region dialog box.

The layout view displays the selected cells in the selection color, which is white by default.

When you select a cell name, the List by Congested Region dialog box displays the RTL for the cell in the RTL text view below the cell list. You can also view the RTL for one or more cells in the RTL browser by selecting the cell names and clicking the Cross Probe button. Cross-probing cells in highly congested areas can help you to identify the RTL code that is causing the congestion. For more information, see [Cross-Probing Cells in Congested Areas](#).

You can also save the cell list data in a file. For more information, see [Saving the Cell List](#).

## See Also

- [Visually Analyzing Congestion](#)

## Saving the Cell List

To save the cell list data in a file,

1. Click the Save List As button.

The Save Cell List As dialog box appears.

2. Select a file or type a file name in the File name text box.
3. Click Save.

The tool saves the cell list data in a text file with a row for each cell and the column data delimited by commas.

## Copying the File names, Line numbers, or Cell names in the Tree View

To copy file names, line numbers, or cell names in the tree view,

1. Select the names and numbers you want to copy.
2. Right-click and choose Copy.

In the list view, you can quickly select or deselect all the cells in the list.

- To select all the cells, right-click and choose Select All.
- To deselect all the cells, right-click and choose Clear All.

You can sort the cell list alphanumerically by the contents of a column and resize individual columns in either view. You can also filter the cells in the list view by using the Filter List dialog box. For information about filtering the cells, see [Filtering Object Lists](#).

### See Also

- [Examining Cells in Congested Areas](#)
- [Map Mode Panel](#)
- [Using Visual Modes](#)

# A

## References

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The following sections provide information about Design Vision menus, toolbars, panels, views, menu commands, dialog boxes, and Tcl commands:

- [Menus](#)
  - [Toolbars](#)
  - [Views](#)
  - [Panels](#)
  - [Menu Commands and Dialog Boxes](#)
  - [Tcl Commands and Variables](#)
- 

## Menus

The following topics provide information about Design Vision menus:

- [AnalyzeRTL Menu](#)
- [Attributes Menu](#)
- [Design Menu](#)
- [Edit Menu](#)
- [File Menu](#)
- [Floorplan Menu](#)
- [Help Menu](#)
- [Hierarchy Menu](#)
- [Highlight Menu](#)
- [List Menu](#)
- [Power Menu](#)
- [Schematic Menu](#)

- [Select Menu](#)
  - [Test Menu](#)
  - [Timing Menu](#)
  - [View Menu](#)
  - [Window Menu](#)
- 

## AnalyzeRTL Menu

When you choose AnalyzeRTL on the menu bar, the following options appear:

- Cross Probe to Source ([Cross-Probing the RTL for Cells and Timing Paths](#)) - Opens the RTL browser and displays the file and line number where the selected cell is defined.
  - Open RTL file ([Opening RTL Files](#)) - Opens one or more RTL files in the RTL browser. You can select the files in the Open RTL Files dialog box. If you select multiple files, the tool opens each file in a separate RTL browser window. Each RTL browser window displays the RTL text view and not the RTL chooser. The title bar displays the name and location of the RTL file.
  - Analyze Datapath Extraction ([Reporting Datapath Extraction Analysis](#)) - Analyzes the arithmetic contents of a generic technology (GTECH) design and provides feedback that can be used to improve the RTL code before optimizing the design. You can view the report and cross-probe the arithmetic operators in the HTML report view.
- 

## Attributes Menu

When you choose Attributes on the menu bar, following options appear. This menu is available only in the Design Vision window.

Specify Clocks ([Specify Clock \(Attributes Menu\)](#)) - lets you define the period and waveform for a clock in the current design. You can also set dont\_touch and fix\_hold attributes on the clock.

You can create a clock on an input port or pin by specifying its name and defining its waveform and period. You can also define virtual clocks that are not associated with a port or pin.

## Operating Environment

When you choose Attributes > Operating Environment on the menu bar, following options appear:

- Input Delay ([Input Delay \(Attributes > Operating Environment\)](#)) - Lets you set input path delays, relative to a clock edge, for selected input ports, inout ports, or internal pins.
- Output Delay ([Output Delay \(Attributes > Operating Environment\)](#)) - Lets you set output path delays, relative to a clock edge, for selected output ports, inout ports, or internal pins.
- Drive Strength ([Drive Strength \(Attributes > Operating Environment\)](#)) - Lets you define drive characteristics for selected top-level input or inout (bidirectional) ports of the current design by associating them with a cell or pin in the technology library. By default, the compiler assumes a zero drive resistance, which means an infinite drive strength, on input or inout ports for which drive characteristics have not been defined.
- Load ([Load \(Attributes > Operating Environment\)](#)) - Lets you set the capacitive load for selected ports or nets and the maximum number of fanout loads for selected output ports. Capacitive load values help the compiler model input delays on input pads and select the appropriate cell drive strengths of output pads.
- Characterize ([Characterize \(Attributes > Operating Environment\)](#)) - Lets you capture environment information about the selected cells, and assign it as attributes on the designs to which the cells are linked.

You can choose which types of environment information to capture from the selected cells (timing, constraint, or connection) and to apply as attributes to the designs the cells reference. By default, only timing information is captured and assigned.

- Operating Conditions ([Operating Conditions \(Attributes > Operating Environment\)](#)) - Lets you select the operating conditions you want to use for timing delay analysis. Operating conditions define the environmental characteristics of a design and are always set on the top design in the hierarchy.
- Wire Load ([Wire Load \(Attributes > Operating Environment\)](#)) - Lets you select a wire load model for the current design. (Not available in topographical mode.)
- Timing Range ([Timing Range \(Attributes > Operating Environment\)](#)) - Lets you set timing range scaling factors for modeling operating condition variations in the current design. Timing ranges are scaling factors used to scale timing path totals. The slowest factor is the largest value of any specified timing range, and the fastest factor is the smallest value.

## Optimization Constraints

When you choose Attributes > Optimization Constraints on the menu bar, following options appear:

- Design Constraints ([Design Constraints \(Attributes > Optimization Constraints\)](#)) - Lets you set design objectives for the top level of the current design.

You can set both optimization constraints (maximum area, maximum dynamic power, and maximum leakage power) and design rule constraints (maximum fanout load and maximum transition time).

For test synthesis, you can also select a minimum fault coverage percentage and control whether area or timing considerations take precedence over fault coverage.

- Timing Constraints ([Timing Constraints \(Attributes > Optimization Constraints\)](#)) - Lets you set maximum and minimum delay constraints for one or more timing paths in the current design. These constraints provide point-to-point timing exceptions for combinational circuits and override the default single-cycle timing relationships for asynchronous paths or paths that do not follow the default single-cycle behavior.
- Derive Constraints ([Derive Constraints \(Attributes > Optimization Constraints\)](#)) - Lets you derive timing constraints from existing timing information for timing paths in the current design. Both sequential and combinational information are derived for all previously unconstrained timing paths.

## Optimization Directives

When you choose Attributes > Optimization Directives on the menu bar, following options appear:

- Design ([Design \(Attributes > Optimization Directives\)](#)) - Lets you set attributes that control design optimization on the current design.
- Input Port ([Input Port \(Attributes > Optimization Directives\)](#)) - Lets you set port attributes for selected input or inout ports.
- Output Port ([Output Port \(Attributes > Optimization Directives\)](#)) - Lets you set port attributes for selected output or inout ports.
- Cell ([Cell \(Attributes > Optimization Directives\)](#)) - Lets you set instance-specific cell attributes throughout the design hierarchy.
- Pin ([Pin \(Attributes > Optimization Directives\)](#)) - Lets you set instance-specific pin attributes throughout the design hierarchy.
- Net ([Net \(Attributes > Optimization Directives\)](#)) - Lets you set instance-specific net attributes throughout the design hierarchy.

- Timing Paths ([Timing Paths \(Attributes > Optimization Directives\)](#)) - Lets you define timing exceptions to constrain or disable asynchronous paths or paths that do not follow the default single-cycle behavior. Timing exceptions are timing relationships that override the single-cycle setup and hold relationship for one or more path.

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## Design Menu

When you choose Design on the menu bar, the following options appear. This menu is available only in the Design Vision window.

- Compile Design ([Optimizing the Design](#)) - Lets you performs logic and gate-level synthesis and optimization on the current design and its subdesigns.
- Compile Ultra ([Optimizing Critical Delays](#)) - Lets you set options and perform critical delay optimization on timing-critical high-speed designs. (Requires DC-Ultra and DesignWare Foundation licenses.)
- Check Design ([Checking Design Consistency](#)) - Checks the internal representation of the current design for consistency, and displays warnings and error messages in the console log view when problems are found.
- Report Design ([Reporting Design Information](#)) - Lets you generate a report of attributes on the current design.
- Report Design Hierarchy ([Reporting Design Hierarchy Information](#)) - Lets you generate a report that shows the reference hierarchy for the design of the current instance, if set, or for the current design.
- Report Design Resources ([Reporting Design Resources](#)) - Lets you generate a report of resources for the design of the current instance, if set, or for the current design. The tool displays the report in an HTML report view. You can cross-probe cells by clicking links in the report and viewing the RTL in an RTL browser window.
- Report Constraints ([Reporting Constraint Violations](#)) - Lets you generate a report of design and timing constraints in the current design.
- Report Reference ([Reporting Design Reference Information](#)) - Lets you generate a report of references for the design of the current instance, if set, or for the current design.
- Report Ports ([Reporting Port Information](#)) - Lets you generate a report about port drives in the current design.
- Report Cells ([Reporting Cell Information](#)) - Lets you generate a report about cells in the current design.
- Report Clocks ([Reporting Clock Information](#)) – Lets you generate a report about clock-related information in the current design.

- Report Area ([Reporting Area Information](#)) - Lets you generate a report showing the combinational area, noncombinational area, net interconnect area, total cell area, and total area occupied by the current design.
- Report Compile Options ([Selecting Objects in the Object Chooser](#)) - Lets you generate a report of compile options for the design of the current instance, if set, or for the current design.
- Report Power ([Reporting Power](#)) - Lets you generate a report that summarizes the dynamic and static power for the current design.
- Analyze Datapath Extraction ([Reporting Datapath Extraction Analysis](#)) - Lets you analyze the arithmetic contents of the design and provides feedback for improving the RTL code. The tool displays the report in an HTML report view. You can cross-probe arithmetic operators by clicking links in the report and viewing the RTL in an RTL browser window.
- Reset Current Design ([Removing Attributes and Constraints](#)) - Removes all constraints and attributes from the current design.

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## Edit Menu

When you choose Edit on the menu bar, the Properties ([Viewing and Editing Object Properties](#)) option appears. This option lets you view and edit properties for a selected object.

If you select multiple objects of the same type, the only property values displayed are those that are the same for all the selected objects. If you select multiple objects of different types, no properties are displayed.

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## File Menu

When you choose File menu on the menu bar, following options appear:

- Read ([Reading Designs](#)) - Opens design files and loads the designs into memory. You select the files and the file format in the Read Designs dialog box. The default file format is .ddc.
- Remove All Designs ([Removing Designs From Memory](#)) - Deletes all designs from memory.
- Analyze ([Analyze Files](#)) - Opens HDL source files, checks them for errors, and translates them into HDL library objects in a HDL-independent intermediate format. You select the files and set `analyze` command options in the Analyze Designs dialog box.

- Elaborate ([Elaborating a Design](#)) - Creates a technology-independent design from the intermediate format files produced by the `analyze` command. You set `elaborate` command options in the Elaborate Designs dialog box.
- Setup ([Specifying Logic Libraries](#)) - Opens the Application Variables dialog box, in which you can set default and define variables.
- Link Design ([Linking Designs](#)) - Links all referenced designs and library components to the current design. You can define the search path, identify the library files, and set options in the Link Design dialog box.
- Import
  - Design Timing ([Importing the Design Timing Information](#)) - Loads leaf cell and net timing information saved from a subdesign, and uses it to annotate the current design. You can select the design name or file name, select the file format, and set annotation options in the Read Design Timing Information dialog box.
- Create MW Library ([Creating a Milkyway Design Library](#)) - Defines a Milkyway design library used to save the current design for use with other Synopsys Galaxy platform tools such as IC Compiler tool. You can specify the file names and locations in the Create Milkyway Design dialog box. (Available only in topographical mode.)
- Set MW Library Reference ([Setting the Milkyway Reference Libraries](#)) - Defines the locations of the Milkyway reference libraries for a Milkyway design library. You can specify the library locations in the Set Library Reference dialog box. (Available only in topographical mode.)
- Open MW Library ([Opening or Closing a Milkyway Design Library](#)) - Opens a Milkyway design library used to save the current design in Milkyway format. You can select the design library in the Open Library dialog box. (Available only in topographical mode.)
- Close MW Library ([Opening or Closing a Milkyway Design Library](#)) - Closes the Milkyway design library. (Available only in topographical mode.)
- Copy MW Library ([Copying a Milkyway Design Library](#)) - Creates a copy of a Milkyway design library. You select the library and the location for the copy in the Copy Library dialog box.(Available only in topographical mode.)
- Set TLU+ ([Setting the TLUPlus Extraction Files](#)) - Sets the TLUPlus files model files and an optional ITF to Milkyway layer map file for RC estimation and extraction. You can specify the file names and locations in the Set TLU+ dialog box. (Available only in topographical mode.)
- Save ([Saving Designs](#)) - Writes the current design and each of its subdesigns in separate .ddc format files named `design_name.ddc`, where `design_name` stands for the name of the design.

- Save As ([Saving Designs](#)) - Saves the current design and its subdesigns in a format and to a file that you specify in the Save Design As dialog box.
- Save Info
  - Design Setup ([Saving a Design Setup](#)) - Creates a script file containing `dc_shell` commands that can help you re-create the current design attribute settings for your design. You can specify the file name in the Save Design Setup dialog box.
- Execute Script ([Entering Tcl Commands in the GUI](#)) - Runs the Tcl script defined in the script file that you select in the Execute File dialog box.
- Licenses ([License Requirements](#)) - Opens the Application Licenses dialog box, in which you can view a list of the licenses you are using and a list of the available licenses, check out licenses, and release licenses.
- Print ([Printing Schematic Views](#)) - Prints the active schematic view or saves an image of the view in a PDF or PostScript (.ps) file. You can select the printer and set options in the Print dialog box.
- Close GUI ([Opening and Closing the GUI](#)) - Closes the Design Vision GUI. However, you are in `dc_shell` or the `design_vision` shell.

**Note:**

You can reopen the GUI by entering the `gui_start` command.

- Exit ([Exiting Design Vision](#)) - Exits Design Vision tool.

## Floorplan Menu

When you choose Floorplan on the menu bar, following options appear:

- Set Design Planning Options ([Performing Floorplan Exploration](#)) - Opens the Set Design Planning Options dialog box, in which you can set up a floorplan exploration session.
- Start Design Planning ([Performing Floorplan Exploration](#)) - Starts the design planning tool for floorplan exploration.

## Help Menu

When you choose Help from the menu bar, following options appear:

- Man Pages ([Viewing Man Pages](#)) - Opens the Man Page Viewer window, in which you can view man pages for `dc_shell` commands, variables, and error messages.
- Report Hotkey Bindings ([Displaying the List of Keyboard Shortcuts](#)) - Displays a report of the keyboard shortcuts for the menu commands in the Design Vision window.

- Online Help ([Getting Help in the GUI](#)) - Opens the Design Vision Help System in your Web browser.
  - Layout Help ([Getting Help in the GUI](#)) - Opens the Design Vision Help System in your Web browser, and displays a list of links to Help topics for layout window features. (Available only on the Help menu in the layout window.)
  - About - Displays information about this version of Design Vision tool.
- 

## Hierarchy Menu

When you choose Hierarchy on the menu bar, following menu options appear. This menu is available only in the Design Vision window.

- Group ([Adding Levels of Hierarchy](#)) - Lets you combine selected cells or cells of a certain type into a new design, which creates a new level of hierarchy in the current design, or into a placement group for use by the layout placement tools.
  - Ungroup ([Removing Levels of Hierarchy](#)) - Lets you ungroup selected cells, which removes a level of hierarchy in the current design.
  - Uniquify ([Creating Uniquely Named Copies of a Design](#)):
    - Hierarchy - Lets you remove multiply instantiated hierarchy for the selected cells, or for all cells in the current design by creating a unique subdesign for each cell.
  - Cells - Lets you make one or more selected cells unique.
  - New Logic Hierarchy View ([Browsing the Design Hierarchy](#)) - Opens a new logic hierarchy view window.
- 

## Highlight Menu

When you choose Highlight on the menu bar, following options appear:

- Selected ([Highlighting Selected Objects or Paths](#)) - Highlights the selected design objects or timing paths in all schematic and layout views.
- Clear Selected ([Removing Highlighting](#)) - Removes the highlighting from selected design objects or timing paths in all schematic and layout views.
- Clear Current Color ([Removing Highlighting](#)) - Opens a menu that lets you choose a highlight color to remove the highlighting in the color from design objects and timing paths in all schematic and layout views.
- Clear All ([Removing Highlighting](#)) - Removes all the highlighting from design objects and timing paths in all schematic and layout views.

- Set Current Color ([Controlling the Highlight Color](#)) - Opens a menu that lets you choose a highlight color to reset the color for the next highlight operation.
  - Next Color ([Controlling the Highlight Color](#)) - Changes the highlight color for the next highlight operation to the next color in the highlight color cycle.
  - Auto Cycle Colors ([Controlling the Highlight Color](#)) - Enables or disables autocycling through the highlight colors. Autocycling is enabled by default.
- 

## List Menu

When you choose List in the menu bar, following options appear. This menu is available only in the Design Vision window.

- Selection List ([Viewing the Selection List](#)) - Opens the Selection List dialog box, which displays the names of all selected objects. You can use this dialog box to select or deselect few or all of the selected objects.
- Designs View ([Viewing the List of Designs in Memory](#)) - Opens a design list view that displays a list of all designs loaded in memory. The list includes the design names, area values, design paths, DesignWare implementations, and the values of the `dont_touch`, `structure`, and `flatten` attributes.
- Cells View ([Viewing and Selecting Objects](#)) - Opens a menu in which you can choose a collection of cells and displays a list view that lists all the cells in the collection. The list includes the cell names, cell paths, and cell library names, and the values of the `dont_touch`, `is_mapped`, and `is_sequential` attributes as follows:
  - Selected Cells - Displays a list of selected cells.
  - Of Selected Pins - Displays a list of cells connected to the selected pins.
  - Of Selected Logical Nets - Displays a list of cells connected to the selected nets.
  - Leaf Cells of Selected - Displays a list of leaf cells within the selected hierarchical cell.
- Ports/Pins View ([Viewing and Selecting Objects](#)) - Opens a menu in which you can choose a collection of ports or pins and displays a list view that lists all the ports and pins in the collection. The list includes the port or pin names, directions, and `dont_touch` attribute values as follows:
  - Selected Ports/Pins - Displays a list of selected ports and pins.
  - Of Selected Nets - Displays a list of ports and pins connected to the selected nets.
  - Of Selected Cells - Displays a list of ports and pins connected to the selected cells.
  - All Ports - Displays a list of all ports in the current design.

- Input Ports - Displays a list of input ports in the current design.
- Output Ports - Displays a list of output ports in the current design.
- Clock Sources - Displays a list of ports designated as clock sources in the current design.
- Nets View ([Viewing and Selecting Objects](#)) - Opens a menu in which you can choose a collection of nets and displays a list view that lists all the nets in the collection. The list includes the net names and `dont_touch` attribute values as follows:
  - Selected Nets - Displays a list of nets connected to the selected nets.
  - Of Selected Ports/Pins - Displays a list of nets connected to the selected ports or pins.
  - Of Selected Cells - Displays a list of nets connected to the selected cells.

## Power Menu

When you choose Power on the menu bar, following options appear:

- Visual UPF ([Generating and Implementing UPF Power Domains](#)) - Lets you create or edit IEEE 1801 power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy by using the [Using the Visual UPF Dialog Box](#).
- The dialog box displays the design hierarchy and provides the tools you use to define the power domains and supply sets for the top-level design and its subdesigns (hierarchical cells). IEEE 1801 is also known as Unified Power Format (UPF).
- UPF Diagram ([Defining the Power Architecture](#)):
  - New UPF Diagram View - Opens a new UPF diagram view window and displays a diagram of the UPF power intent currently defined in the design.
  - Collapse Selected Domains - Collapses any expanded scopes and power domains that are selected in the active UPF diagram view.
  - Expand Selected Domains - Expands any collapsed scopes and power domains that are selected in the active UPF diagram view.
- Highlight Cells ([Examining Power Management Cells](#)):
  - Isolation Cells - Highlights all the isolation cells in the design with the current highlight color.
  - Level Shifter Cells - Highlights all the level-shifter cells in the design with the current highlight color.

- Always On Cells - Highlights all the always-on cells in the design with the current highlight color.
  - Always On Nets- Highlights all the always-on nets in the design with the current highlight color.
  - All PM Cells Schematic ([Examining Power Management Cells](#)) - Opens a new schematic view and displays a schematic of all the power management cells in the design.
  - MV Advisor [Examining and Debugging Multivoltage Design Violations](#) - Opens a new MV Advisor violation browser and loads the current violation report. If no current report is available, the violation browser displays a message with links that you can use to open the Check MV Design dialog box or load a previously saved report file.
  - Analyze MV Design ([Analyzing Multivoltage Design Connections](#)) - Analyzes multivoltage design connections based on options that you set in the Analyze MV Design dialog box, and displays the report in a new analysis view window.
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## Schematic Menu

When you choose Schematic on the menu bar, following options appear. This menu is available only in the Design Vision window.

- New Schematic View ([Schematic Views](#)) - Opens a new schematic view window and displays a schematic of the selected timing paths, design objects, or design instances (hierarchical cells).
- Back ([Reversing and Reapplying Schematic Changes](#)) - Reverses the most recent action that you performed in the active schematic view, such as adding fanout logic or expanding a hierarchical cell, and redisplays the previous schematic in the active schematic view. You can sequentially reverse a series of actions.
- Forward ([Reversing and Reapplying Schematic Changes](#)) - Reapplies the most recently reversed action in the active schematic view and redisplays the next schematic in the list of previously displayed schematics. If you have reversed one or more actions, you can reapply the most recently reversed action or a series of actions.
- Add Paths From/Through/To ([Adding Worst Paths Through Objects](#)) - Lets you add worst slack timing paths to the schematic in the active schematic view but does not change the netlist or affect other schematic views. You can add one or more paths with the worst slack in the current design, in a path group, or from, to, or through selected objects.
- Add Fanin/Fanout ([Adding Fanin or Fanout Logic](#)) - Lets you add fanin or fanout logic to the schematic in the active schematic view but does not change the netlist or affect

other schematic views. You can add either the fanin logic to selected objects or the fanout logic from selected objects.

- Delete Selected ([Adding or Removing Selected Logic](#)) - Removes selected objects from the schematic in the active schematic view but does not change the netlist or affect other schematic views.
- Add Selected ([Adding or Removing Selected Logic](#)) - Adds selected objects to the schematic in the active schematic view but does not change the netlist or affect other schematic views.
- Add Next Fanin/Fanout Level ([Adding Fanin or Fanout Logic](#)) - Adds the next level of fanin or fanout logic to the schematic in the active schematic view but does not change the netlist or affect other schematic views.
- Expand
  - Selected Objects ([Schematic Views](#)) - Expands the selected metacells or metapins to display the objects that they represent.
  - All Hierarchy ([Examining Hierarchical Cells](#)) - Expands all hierarchy metacells to display the objects in the hierarchical blocks that they represent.
  - All Buffers/Inverters/Crossings ([Displaying or Hiding Buffers and Inverters](#)) - Expands all buffer and inverter metacells to display the buffers, inverters, nets, and hierarchy crossings that they represent.
  - All Bussed Pins/Nets ([Expanding and Collapsing Buses](#)) - Expands all bus nets and their associated pins.
  - All Unconnected Pins ([Displaying or Hiding Unconnected Macro Pins](#)) - Expands all metapins to display the unconnected pins that they represent.
- Collapse
  - All Hierarchy ([Examining Hierarchical Cells](#)) - Collapses all the objects within hierarchical cells into hierarchy metacells that represent their associated hierarchical parent blocks.
  - Selected Hierarchy By Parent ([Examining Hierarchical Cells](#)) - Collapses the selected objects into hierarchy metacells that represent their hierarchical parent blocks.
  - All Buffers/Inverters/Crossings By Chain ([Displaying or Hiding Buffers and Inverters](#)) - Collapses all buffers and inverter chains into metacells that represent their constituent buffers or inverters, hierarchy crossings, and the nets that connect them.
  - All Buffers/Inverters/Crossings By Tree ([Displaying or Hiding Buffers and Inverters](#)) - Collapses all buffer and inverter trees into metacells that represent their constituent buffers or inverters, hierarchy crossings, and the nets that connect them.

- Selected Buffers/Inverters/Crossings ([Displaying or Hiding Buffers and Inverters](#)) - Collapses the selected buffers, inverters, and hierarchy crossings into metacells.
  - All Bussed Pins/Nets ([Expanding and Collapsing Buses](#)) - Collapses all bus nets and their associated pins.
  - All Unconnected Pins ([Displaying or Hiding Unconnected Macro Pins](#)) - Collapses all unconnected pins into metapins.
  - Show Logic/Power Hierarchy ([Viewing Cells Hierarchically](#)) - Displays or hides hierarchical cell and power domain boundaries in the active schematic view.
  - Color by Power Hierarchy ([Viewing Cells Hierarchically](#)) - Displays or hides object colors in the active schematic view based on the hierarchical power relationships of the design.
- 

## Select Menu

When you choose Select on the menu bar, following options appear:

- Clear ([Deselecting All Selected Objects](#)) - Deselects all selected objects.
- Highlighted ([Selecting Highlighted Objects and Paths](#)) - Selects objects highlighted in the active view.
- By Name Toolbar ([Select By Name Toolbar](#)) - Lets you select or highlight objects in the active schematic or layout view
- By Name ([Searching for Objects by Name or Regular Expression](#)) - Lets you find and select or highlight objects that match a specific name, name pattern, or regular expression.
- Paths From/Through/To ([Selecting Timing Paths](#)) - Lets you select timing paths with the worst path in the current design, in a path group, or from, through, or to selected objects.
- Fanin/Fanout ([Selecting Fanin or Fanout Logic](#)) - Lets you select fanin or fanout paths for selected objects.
- Cells ([Selecting a Collection of Objects](#))
  - Top Design - Selects the hierarchical cell at the top of the design hierarchy.
  - Leaf Cells of Selected - Selects leaf cells within the selected hierarchical cells.
  - Of Selected Pins - Selects cells connected to the selected pins.

- Of Selected Logical Nets- Selects cells connected to the selected nets.
- Of Selected Paths - Selects all cells on the selected timing paths.
- Ports/Pins ([Selecting a Collection of Objects](#))
  - All Ports - Selects all top-level ports of the current design.
  - Input Ports - Selects all top-level input and input ports of the current design.
  - Output Ports - Selects all top-level output and output ports of the current design.
  - Clock Sources - Selects all input ports designated as clock sources.
  - Of Selected Nets - Selects all ports and pins connected to the selected nets.
  - Of Selected Cells - Selects all ports and pins connected to the selected cells.
  - Of Selected Paths - Selects all ports and pins on the selected timing paths.
- Nets ([Selecting a Collection of Objects](#))
  - Of Selected Ports/Pins - Selects all nets connected to the selected ports and pins.
  - Of Selected Cells - Selects all nets connected to the selected cells.
- Objects of Selected Buses ([Selecting Bus Objects](#)) - Selects all nets on the selected buses. (Available only in the Design Vision window.)
- Buses of Selected ([Selecting Bus Objects](#)) - Selects buses that contain one or more of the selected nets. (Available only in the Design Vision window.)
- Selection List ([Viewing the Selection List](#)) - Opens the Selection List dialog box, which displays the names of all selected objects. You can use this dialog box to select or deselect some or all of the selected objects.
- Query Selection - Displays a summary of all selected objects on the Query panel. If only one object is currently selected, using this command is equivalent to clicking the object with the Query tool.

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## Test Menu

When you choose Test on the menu bar, following options appear. This menu is available only in the Design Vision window.

- Run DFT DRC ([Checking Scan Test Design Rules](#)) - Checks the current design for DRC violations in the scan test implementation specified by the `set_scan_configuration` command.
  - Browse Violations ([DRC Violation Browser](#)) - Opens a new violation browser view window that displays information about scan test DRC violations in the current design.
  - Browse Test Modes ([Viewing Test Protocols](#)) - Displays information about test protocols in the Test Modes Details dialog box.
  - Hold Time Analysis ([DFT Hold Time Analysis Window](#)) - Opens a new hold time analysis view window that displays information about scan cells with hold time violations.
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## Timing Menu

When you choose Timing on the menu bar, following options appear. This menu is available only in the Design Vision window.

- New Path Analyzer ([Analyzing Timing Path Collections](#)) - Opens a new timing path analyzer window, in which you can load a collection of timing paths and categorize them based on available attributes.
- New Path Inspector ([Inspecting Timing Path Elements](#)) - Opens a new path inspector window that provides tools for examining different aspects of a selected timing path. You can examine clock launch and capture delay path profiles, a timing report summary, a path elements table, and details about the path slack.
- Timing Status Summary [Examining Timing Path Details](#) - Opens a new timing status summary window that displays a table of timing path details. The table displays details about paths found by the `get_timing_paths` command. When you open the window, the table displays details for paths with the worst slack in the design. You can adjust the `get_timing_paths` command options and reload the table with details about different paths.
- Path Slack ([Opening a Path Slack Histogram](#)) - Lets you select path and timing options and generate a default or custom path slack histogram for paths with the worst slack in the current design or in a path group, or for paths from, to, or through selected objects.
- Slack Histograms of Selected Logic ([Opening a Path Slack Histogram](#)) - Generates a path slack histogram for all selected design objects (you must select multiple objects).
- Slack Histograms of Selected Paths ([Opening a Path Slack Histogram](#)) - Generates a path slack histogram for all selected timing paths (you must select multiple paths).
- Net Capacitance - ([Opening a Net Capacitance Histogram](#)) - Lets you generate a default or custom net capacitance histogram for all nets in the current design.

- Capacitance of Selected Nets ([Opening a Net Capacitance Histogram](#)) - Generates a net capacitance histogram for selected nets.
- Check Timing ([Checking Design Timing](#)) - Lets you check the attributes placed on the current design for timing problems.
- Report Timing Paths ([Reporting Worst Path Timing](#)) - Lets you generate a timing report for specified timing paths or for the paths with the worst slack in the current design.
- Report Timing Requirements ([Reporting Timing Requirements](#)) - Lets you generate a report containing information about timing requirements for the current design or for specified timing paths in the current design.
- Report Clock Skew ([Reporting Clock Network Skew Information](#)) - Lets you generate a clock skew report for the current design.
- Report Clock Tree ([Reporting Clock Tree Fanout Information](#)) - Lets you generate a clock tree report showing the fanout network for every clock source in the current design.
- Report Path Group ([Reporting Path Groups](#)) - Lets you generate a report of path groups in the current design.
- Report Wire Load ([Reporting Wire Load Information](#)) - Lets you generate a wire load report that identifies the fanout, length, points, average capacitance, standard deviation, and percentage of standard deviation for each wire load model in the current design. (Not available in topographical mode.)

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## View Menu

When you choose View on the menu bar, following options appear:

- Zoom
  - Zoom Fit All ([Magnifying or Shrinking a View](#)) - Decreases the magnification in the active schematic, layout, or histogram view and displays the entire design or histogram, in a slight margin, in the view.
  - Zoom In ([Magnifying or Shrinking a View](#)) - Magnifies the design in the active schematic, layout, or histogram view by a factor of 2, providing more detail in a close-up view of a smaller area around the center of the design or histogram.
  - Zoom Out ([Magnifying or Shrinking a View](#)) - Decreases the magnification of the design in the active schematic, layout, or histogram view by a factor of 2, providing less detail but a wider view of the design or histogram.
  - Zoom Fit Selection ([Magnifying or Shrinking a View](#)) - Increases or decreases the magnification of the design or histogram in the active schematic, layout, or

histogram view by displaying selected objects or bins so that they all just fit within the view.

- Zoom Follow Selection ([Following Selected Objects](#)) - Controls whether the active schematic or layout view automatically zooms to an object when you select it, increasing or decreasing the magnification of the design to fit the object within the view.

You can enable or disable this automatic operation separately for each open schematic view. When you enable this operation for a schematic view, the operation remains enabled even when the view is not the active view. Zoom Follow Selection option is disabled by default.

- Zoom Fit Highlight ([Magnifying or Shrinking a View](#)) - Increases or decreases the magnification of the design in the active schematic or layout view by displaying highlighted objects so that they all fit within the view.
- Zoom To ([Magnifying or Shrinking a View](#)) - Magnifies and traverses the design to display a rectangular area. You specify the coordinates for the top-left and bottom-right corners in the Zoom To dialog box. (Available only in the layout window.)
- Pan To Selection ([Traversing a View](#)) - Traverses the design or histogram in the active schematic, layout, or histogram view to display the most recently selected objects or bins.
- Pan To Highlight ([Traversing a View](#)) - Traverses the design in a schematic or layout view to display the most recently highlighted objects.
- Back in Zoom and Pan History ([Reusing Zoom and Pan Settings](#)) - Redisplays the previous zoom level and pan position in the active schematic or layout view.

Design Vision tool maintains a list of zoom and pan settings for each schematic or layout view. Each time you change the magnification or traverse the view, the previous zoom and pan setting is added to the list. By choosing View > Back in Zoom and Pan History, you can step backward in the list from the current zoom level and pan position to the initial zoom level and pan position when you opened the view.

- Forward in Zoom and Pan History ([Reusing Zoom and Pan Settings](#)) - Redisplays the next zoom level and pan position in the list of previous zoom and pan settings.

Design Vision tool maintains a list of zoom and pan settings for each schematic or layout view. After you have chosen View > Back in Zoom and Pan History (to step backward in the list), you can step forward in the list by choosing View > Forward in Zoom and Pan History.

- Named Zoom and Pan Settings ([Reusing Zoom and Pan Settings](#)) - Lets you save the current zoom level and pan position or change to a zoom level and pan position that you saved earlier in the session.
- Zoom Layout View to Current View ([Magnifying or Shrinking a View](#)) - Applies the current zoom level and pan position in the active layout view to any other open layout views in the same layout window. (Available only in the layout window.)
- Mouse Tools
  - Selection Tool ([Selecting Objects in Graphic Views](#)) - Enables the left mouse button to select objects when you click them or drag the pointer to create a selection box around them in the active schematic, layout, or histogram view. The Selection tool is enabled by default.
  - Highlight Tool ([Highlighting Objects or Timing Paths](#)) - Enables the left mouse button to highlight objects in the active schematic or layout view when you click them or drag the pointer to create a selection box around them. Clicking objects when this tool is enabled does not change the selection list.
  - Query Tool ([Querying Objects in Graphic Views](#)) - Enables the left mouse button to display object information when you click an object in the active schematic or layout view. The GUI displays the information in the Query panel. Clicking objects when this tool is enabled does not change the selection list.
  - Zoom In Tool ([Magnifying or Shrinking a View](#)) - Enables the left mouse button to magnify an area in the active schematic, layout, or histogram view. This provides more detail in a close-up view of the defined area.

You can click to zoom in by recentering the view and doubling its magnification, or you can drag the pointer around an area you want to magnify.
  - Zoom Out Tool ([Magnifying or Shrinking a View](#)) - Enables the left mouse button to shrink the visible part of the design in the active schematic, layout, or histogram view into a defined area. This provides less detail but a wider view of the design.

You can click to zoom out by recentering the design and shrinking it to half its current magnification, or you can drag the pointer to define an area into which you want to shrink the view.
  - Pan Tool ([Traversing a View](#)) - Enables the left mouse button to traverse the design when you drag the pointer in any direction in the active schematic, layout, or histogram view.

- Ruler Tool ([Drawing Rulers](#) - Enables the left mouse button to draw rulers when you click in the active layout view. (Available only in the layout window.)
- Clear Rulers ([Drawing Rulers](#) - Removes all rulers from the active layout view. (Available only in the layout window.)
- Refresh ([Redrawing the Active View](#)) - Redraws the active schematic, layout, or histogram view.
- Grid ([Displaying Grid Lines](#)) - (Available only in the layout window.)
  - Show Litho Grid - Displays or hides the litho grid.
  - Show User Grid - Displays or hides the user grid.
  - Cycle Grid Spacing - Switches the grid display from one grid to the other.
- [Displaying Net Connections](#) - Enables or disables net connections in the active layout view. (Available only in the layout window.)
- Visual Mode ([Using Visual Modes](#)) - Enables or disables visual mode in the active layout view. (Available only in the layout window.)
- Map Mode ([Analyzing Congestion](#)) - Enables or disables the congestion map in the active layout view. (Available only in the layout window.)
- Toggle Transient Toolbars - Displays or hides the Visual Mode panel when a visual mode is enabled, the Map Mode panel when the congestion map is enabled, and the Net Connection panel when the net connections are enabled in the active layout view. (Available only in the layout window.)
- New Layout View - Opens a new layout view in the active layout window. (Available only in the layout window.)
- Save Screenshot As [Saving an Image of a Window or View](#) - Creates an image file containing an image of the active application window or view window. You specify the file name and file format (BMP, PNG, JPEG, or XPM) in the Save screenshot as dialog box
- InfoTip ([Previewing Objects in Graphic Views](#)) - Enables or disables InfoTips in the active schematic, layout, or UPF diagramview.
- Toolbars
  - Analysis ([Analysis Toolbar](#)) - Displays or hides the Analysis toolbar. (Available only in the layout window.)
  - Design List ([Design List Toolbar](#)) - Displays or hides the Design List toolbar. (Available only in the Design Vision window.)

- File ([File Toolbar](#)) - Displays or hides the Standard toolbar. (Available only in the Design Vision window.)
- Highlight ([Highlight Toolbar](#)) - Displays or hides the Highlight toolbar. (Available only in the layout window.)
- Layout ([Layout Toolbar](#)) - Displays or hides the Layout toolbar. (Available only in the Design Vision window.)
- Mouse Tool Options ([Mouse Tool Options Toolbar](#)) - Displays or hides the Mouse Tool Options toolbar. (Available only in the layout window.)
- Mouse Tools ([Mouse Tools Toolbar](#)) - Displays or hides the Mouse Tools toolbar.
- Power ([Power Toolbar](#)) - Displays or hides the Power toolbar. (Available only in the Design Vision window.)
- Schematics ([Schematics Toolbar](#)) - Displays or hides the Schematics toolbar. (Available only in the Design Vision window.)
- Select By Name ([Select By Name Toolbar](#)) - Displays or hides the Select By Name toolbar.
- Timing Views ([Timing Views Toolbar](#)) - Displays or hides the Timing Views toolbar. (Available only in the Design Vision window.)
- View Zoom/Pan ([View Zoom/Pan Toolbar](#)) - Displays or hides the View Zoom/Pan toolbar.
- Zoom and Pan History ([Zoom and Pan History Toolbar](#)) - Displays or hides the Zoom and Pan History toolbar.
- Console ([Console](#)) - Displays or hides the console panel.
- [Displaying Net Connections](#) - Displays or hides the Net Connections panel. (Available only in the layout window when net connections are enabled in the active layout view.)
- Map Mode ([Analyzing Congestion](#)) - Displays or hides the Map Mode panel. (Available only in the layout window when map mode is enabled in the active layout view.)
- Overview ([Overview Panel](#)) - Displays or hides the Overview panel. (Available only in the layout window.)
- Power State Table ([Power State Table Panel](#)) - Displays or hides the Power State Table panel. (Available only in the Design Vision window and appears on the menu only when a UPF diagram view is open.)
- Query ([Overview Panel](#)) - Displays or hides the Query panel.

- View Settings ([View Settings Panel](#)) - Displays or hides the View Settings panel.
  - Visual Mode ([Visual Mode Panel](#)) - Displays or hides the Visual Mode panel.  
(Available only in the layout window when visual mode is enabled in the active layout view.)
  - Script Editor ([The Script Editor](#)) - Displays or hides the script editor panel.
  - Status Bar - Displays or hides the status bar.
  - Preferences ([Setting GUI Preferences](#)) - Sets GUI preferences such as fonts, global display options, and some automatic operations. You use the Application Preferences dialog box to select the options for the preferences that you want to set or change.
  - AutoSave Preferences - Auto saves the GUI preferences.
- 

## Window Menu

When you choose Window on the menu bar, the following menu options appear:

- New Main Window ([Graphical User Interface](#)) - Opens a new Design Vision window.
- New Layout Window ([Opening the Layout Window](#)) - Opens a new layout window.  
(Available only in topographical mode.)
- Close Window ([Closing Windows](#)) - Closes the active Design Vision window or layout window.
- Close All Windows ([Closing Windows](#)) - Closes all open Design Vision windows and layout windows. This is equivalent to closing the GUI (choose File > Close GUI).
- Next Window - Changes the focus to the next Design Vision window or layout window in the list of window names on the Window menu, displaying it on top of the other windows.
- Previous Window - Changes the focus to the previous Design Vision window or layout window in the list of window names on the Window menu, displaying it on top of the other windows.
- Save Window Settings - Saves the window settings.
- AutoSave Window Settings - Auto saves the window settings.
- Close View ([Closing Windows](#)) - Closes the active view window.
- Close All Views ([Closing Windows](#)) - Closes all view windows that are open in the current Design Vision window.
- Maximum Views - closes maximum views.

- Tile Views - ([Rearranging View Windows](#)) - Arranges the open view windows in the current Design Vision window by tiling them between the toolbars and the console.
- Next View - Changes the focus to the next view window in the list of view names at the bottom of the Window menu, displaying it on top of the other view windows and making it the active view.
- Previous View - Changes the focus to the previous view window in the list of view names at the bottom of the Window menu, displaying it on top of the other view windows and making it the active view.

At the bottom of the menu, the names of all open windows and views are listed, in the order they are opened. A check mark against a window name indicates the active window. A check mark against a view name indicates the active view.

You can display a window on top of the other windows and make it the active window by choosing its name in the menu. Similarly, within the active window, you can display a view on top of the other views in the workspace area and make it the active view by choosing its name in the menu.

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## Toolbars

The following topics provide information about Design Vision toolbars:

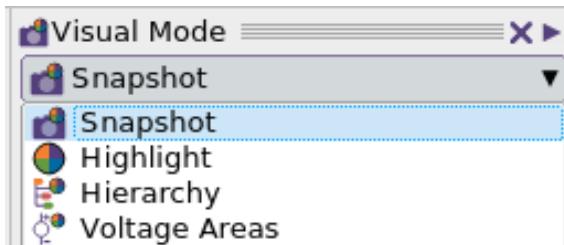
- [Analysis Toolbar](#)
- [Design List Toolbar](#)
- [File Toolbar](#)
- [Highlight Toolbar](#)
- [Layout Toolbar](#)
- [Mouse Tool Options Toolbar](#)
- [Mouse Tools Toolbar](#)
- [Power Toolbar](#)
- [Schematics Toolbar](#)
- [Select By Name Toolbar](#)
- [Timing Views Toolbar](#)
- [View Zoom/Pan Toolbar](#)
- [Zoom and Pan History Toolbar](#)

## Analysis Toolbar

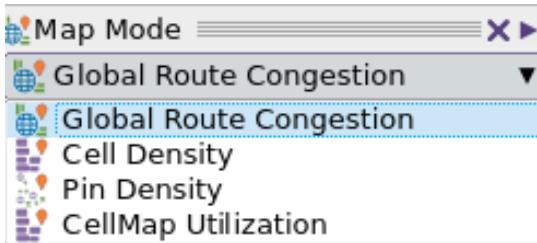
Use the Analysis toolbar to enable or disable visual modes, the congestion map, and net connections in the active layout view. You can display or hide the Analysis toolbar by choosing View > Toolbars > Analysis. This toolbar is available only in the Layout window.

The Analysis toolbar contains the following buttons:

- Visual Mode  - Enables or disables the current visual mode. The Visual Mode button displays the icon for the default visual mode (snapshot) or the most recently active visual mode.
  - To enable or disable the default or most recently active visual mode, click the Visual Mode button.
  - To enable a different visual mode, click the arrow button and choose the visual mode name on the menu that appears.



- Map Mode  - Enables or disables global route congestion map mode.
  - The Map Mode button displays the icon for the global route congestion map. To enable or disable the congestion map, you can click the Map Mode button or click the arrow button and choose Global Route Congestion. The global route congestion map icon always appears on the Map Mode button. To enable a different visual mode, click the arrow button and choose the visual mode name on the menu that appears.



- Net Connections  - Enables or disables net connections in the active layout view.

### See Also

- [Using Visual Modes](#)
- [Analyzing Congestion](#)
- [Displaying Net Connections](#)

---

## Design List Toolbar

Use the Design List toolbar to change the current design. You can display or hide the Design List toolbar by choosing View > Toolbars > Design List. This toolbar is available only in the Design Vision window.

The Design List toolbar contains a list with the names of all the designs that are currently loaded into memory. You can change the current design by selecting the name of a different design in this list.

---

## File Toolbar

Use the File toolbar to read and save design files. You can display or hide the File toolbar by choosing View > Toolbars > File. This toolbar is available only in the Design Vision window.

The File toolbar contains the following options:

- Read  - Opens the Read Designs dialog box, which you can use to read one or more design description files into memory.
- Save  - Saves the current design and each of its subdesigns in separate .ddc format files named design\_name.ddc.
- Print  - Click this button to open the Print dialog box, which you can use to print the active schematic view or save the schematic in a print file that you can print later.
- Properties  - Opens the Properties dialog box, which you can use to view and edit property values for selected objects.

---

## Highlight Toolbar

Use the Highlight toolbar to perform highlight operations in the active layout view. You can display or hide the Highlight toolbar by choosing View > Toolbars > Highlight. This toolbar is available only in the layout window.

The Highlight toolbar contains the following options:

- Selected  - Click the arrow to display the menu and choose a color to reset the current color for the next highlight operation.
  - Clear All  - Click the arrow to remove all highlighting from design objects and timing paths in the active schematic or layout view.
- 

## Layout Toolbar

Use the layout toolbar to open the layout window. You can display or hide the layout toolbar by choosing View > Toolbars > Layout. This toolbar is available only in the Design Vision window.

The Layout toolbar contains the following option:

- Layout window  - Opens a new instance of the layout window.
- 

## Mouse Tool Options Toolbar

Use the Mouse Tool Options toolbar to set options for the active mouse tool. Mouse tools perform actions when you click or drag the pointer in the active layout view. You can set options on this toolbar for the Selection tool, the Highlight tool, and the Ruler tool. When you change an option on the Mouse Tool Options toolbar, the change takes place immediately.

The Mouse Tool Options toolbar displays options only for the active mouse tool.

- When the Selection tool is active, the following options appear:



For details about these options, see [Selecting Objects in Graphic Views](#).

- When the Highlight tool is active, the following options appear:



For details about this option, see [Highlighting Objects or Timing Paths](#).

- When the Ruler tool is active, the following options appear:



For details about these options, see [Drawing Rulers](#).

## See Also

- [Selecting a Mouse Tool](#)

## Mouse Tools Toolbar

Use the Mouse Tools toolbar to set the active tool for the left mouse button. The mouse tool controls the actions performed by the left mouse button when you click or drag the pointer in a schematic, layout, or histogram view. You can use mouse tools to control the magnification and position of the design in any graphic view.

The Mouse Tools toolbar contains the following options:

- Selection Tool (Esc) - Sets the left mouse button to select or deselect objects by clicking them or dragging the pointer to create a selection box around them in the active schematic, layout, or histogram view. This is the default mouse tool.
- Highlight Tool - Sets the left mouse button to highlight objects or remove highlighting from objects by clicking them or dragging the pointer to create a rectangular box around them in the active schematic or layout view.
- Query Tool (Ctrl+Q) - Sets the left mouse button to display object information by clicking an object in the active schematic or layout view. The GUI displays the information in the Query panel. Clicking objects with this tool does not change the selection list.
- Zoom In Tool (Z) - Sets the left mouse button to magnify an area in the active view. This provides more detail in a close-up view of the defined area. You can click to zoom in by re-centering the view and doubling its magnification, or you can drag the pointer around an area you want to magnify. (Available in schematic, layout, and histogram views.)
- Zoom Out Tool - Sets the left mouse button to shrink the visible part of the design into a defined area in the active view. This provides less detail but a wider view of the design. You can click to zoom out by recentering the design and shrinking it to half its current magnification, or you can drag the pointer to define an area into which you want to shrink the view. (Available in schematic, layout, and histogram views.)

- Pan Tool - Sets the left mouse button to traverse the design in any direction by dragging the pointer in the active view. (Available in schematic, layout, and histogram views.)
  - Ruler Tool (Ctrl+U) - Sets the left mouse button to draw rulers in the active layout view. (Available only in the layout window.)
  - Clear rulers - Removes all rulers from the active layout view. (Available only in the layout window.)
- 

## Power Toolbar

Use the Power toolbar to open the Visual UPF dialog box, UPF diagram views, and the MV Advisor violation browser. You can display or hide the Power toolbar by choosing View > Toolbars > Power. This toolbar is available only in the Design Vision window.

The Power toolbar contains the following options:

- Open Visual UPF - Opens the Visual UPF dialog box.
  - Create UPF Diagram - Opens a UPF diagram view.
  - Create MV Advisor - Opens the MV Advisor violation browser.
- 

## Schematics Toolbar

Use the Schematics toolbar to perform viewing operations in the active schematic view. You can display or hide the Schematics toolbar by choosing View > Toolbars > Schematics. This toolbar is available only in the Design Vision window.

The Schematics toolbar contains the following options:

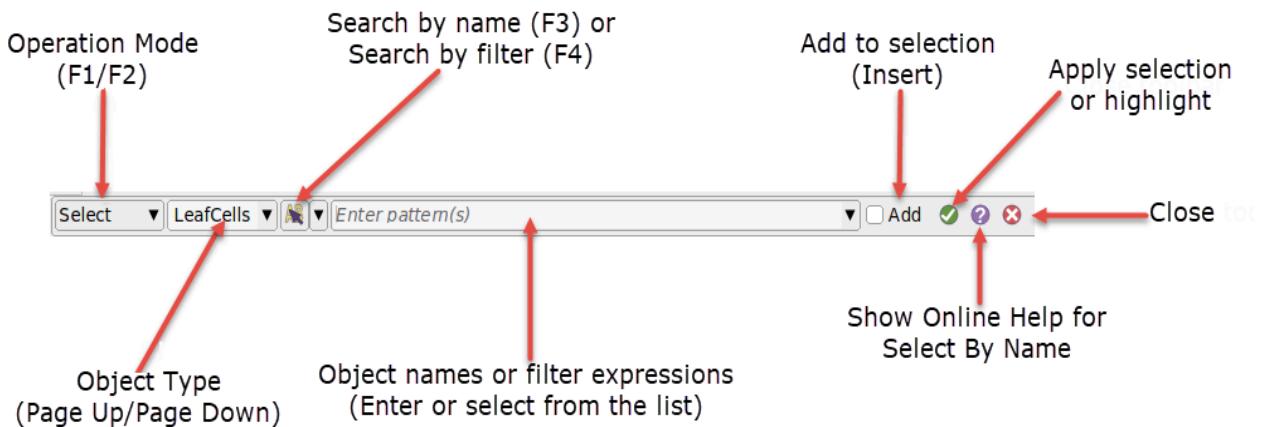
- Create Schematic of Selected Objects - Opens a new schematic view and displays the selected design instance (hierarchical cell), timing paths, or logic (design objects).
- Add Paths to Schematic - Opens the Add Paths From/Through/To to Path Schematic dialog box, which lets you display timing paths with the worst slack from, to, or through selected objects (or the paths with the worst slack in the design or in a path group) in a schematic view. You can add the paths to the active schematic view or display them in a new schematic view.

- Add Fanin/Fanout to Path Schematic  - Opens the Add Fanin/Fanout to Path Schematic dialog box, which lets you display the fanin or fanout logic for selected objects in a schematic view. You can add the fanin or fanout logic to the active schematic view or display it in a new schematic view.
- Collapse all hierarchy  - Collapses all the objects within hierarchical cells into hierarchy metacells that represent their associated hierarchical parent blocks.
- Collapse the hierarchy of the selected instances up one level  - Collapses the selected objects into hierarchy metacells that represent their hierarchical parent blocks.
- Collapse selected buffers, inverters, and crossing cells  - Collapses the selected buffers, inverters, and hierarchy crossings into metacells.
- Expand selected abstract objects  - Expands the selected metacells or metapins to display the objects that they represent.

## Select By Name Toolbar

Use the Select > By Name Toolbar to select or highlight objects in the active schematic or layout view. You can identify the objects by specifying their names or a filter expression.

You can operate the toolbar by setting options on the toolbar or by pressing keys on the keyboard.



The By Name Toolbar contains the following options:

- Operation Mode list - Select the action that you want to perform: Select, Highlight, or Tabulate Objects. The default is Select.
- Object Type list - Select the type of objects that you want to search for LeafCells, Cells, LeafNets, Nets, LeafPins, Pins, Ports, or LibCells options. The default is LeafCells.
- Search Type list - Select the type of search that you want to perform: Search by name or Search by filter. The default is Search by name.
- Object Name box - Specify the object names or a filter expression. You can type the names or filter expressions, or press the Down Arrow key and select them in the list that appears.

You can include wildcard characters (?) and (\*) to specify a name pattern. To specify multiple names or name patterns, separate them with blank spaces. If a name includes a blank space, enclose it in braces ({} ) to treat it as a single name.

- Add to Selection check box - Select this option if you want to add the objects to the current selection instead of replacing the objects in the current selection.
- Apply selection or highlight button - Select this option to perform the selection or highlight operation.
- Show Online Help for Select By Name button - Select this option if you need assistance using the toolbar. An online Help page appears in the man page viewer.
- Close toolbar button - Select this option if you want to hide the toolbar.

### See Also

- [Selecting Objects by Name](#)

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## Timing Views Toolbar

Use the Timing Views toolbar to open timing histograms. You can display or hide the Timing Views toolbar by choosing View > Toolbars > Timing Views. This toolbar is available only in the Design Vision window.

The Timing Views toolbar contains the following options:

- Create Path Slack Histogram  - Opens the Path Slack dialog box, which lets you generate a path slack histogram for the current design. Path slack histograms help you examine and refine the timing paths with the worst slack in the current design or the timing paths with the worst slack from, to, or through selected objects.
  - Create net capacitance histogram  - Opens the Net Capacitance dialog box, which lets you generate a net capacitance histogram for the current design. Net capacitance histograms provide an overview of the capacitance values for the nets in your design.
- 

## View Zoom/Pan Toolbar

Use the View Zoom/Pan toolbar to control the magnification and position of the design in schematic, layout, and histogram views. You can display or hide the View Zoom/Pan toolbar by choosing View > Toolbars > View Zoom/Pan.

The View Zoom/Pan toolbar contains the following options:

- Zoom Fit All (F)  - Decreases the magnification of the active view to display the entire design or histogram, with a slight margin, within the view.
- Zoom In 2x (+)  - Doubles the magnification of the design or histogram displayed in the active view, showing more detail for a smaller area of the design or histogram.
- Zoom Out 2x (-)  - Decreases (by a factor of 2) the magnification of the design or histogram displayed in the active view, showing a wider area but less detail.
- Pan to selection  - Traverses the design or histogram within the active view to display the most recently selected objects or bins.
- Zoom to selection (Ctrl + T)  - Increases or decreases the magnification of the design or histogram in the active view by displaying all selected objects or bins so that the objects fit within the view.
- Zoom Follow Selection  - Controls if the active schematic or layout view automatically zooms to an object when you select it, increasing or decreasing the magnification of the design to fit the object within the view.

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## Zoom and Pan History Toolbar

Use the Zoom and Pan History toolbar to redisplay a zoom level and pan position in the active schematic, layout, or histogram view. You can display or hide the Zoom and Pan History toolbar by choosing View > Toolbars > Zoom And Pan History.

The GUI maintains a list of zoom and pan settings for each open view. Each time you change the magnification or traverse the view, the previous zoom level and pan position is added to the list. You can step backward or forward in the list to redisplay the previous or next zoom level and pan position. You can also save the current zoom level and pan position, and you can redisplay a previously saved zoom level and pan position.

The Zoom and Pan History toolbar contains the following options:

- Go back in zoom and pan history  - Redisplays the previous zoom level and pan position in the active view.
  - Go forward in zoom and pan history  - Redisplays the next zoom level and pan position in the list of previous zoom and pan settings.
- 

## Views

The following topics provide information about Design Vision views:

- [Cell Lists](#)
- [Design List](#)
- [Histogram Views](#)
- [Logic Hierarchy Views](#)
- [Net Lists](#)
- [Path Profile Views](#)
- [Port and Pin Lists](#)
- [Report Views](#)
- [Schematic Views](#)
- [UPF Diagram Symbols and Standards](#)

## Cell Lists

Cell list views display information about collections of cells. The view consists of a table that shows the instance name, the reference name, the cell path, the library name, and the states of the `dont_touch`, `is_mapped`, and `is_sequential` attributes for each cell in the collection.

You can

- Click a column heading to sort the table information alphabetically
- Click the heading again to reverse the sorting
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#))

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

The columns in the cells view table provide the following information:

Column	Description
Cell Name	Cell instance name
Ref Name	Name of the design the cell references
Cell Path	Full hierarchical name from the top-level design to the cell
<code>dont_touch</code>	Indicates when a <code>dont_touch</code> attribute is set on the cell
<code>is_mapped</code>	Indicates when an <code>is_mapped</code> attribute is set on the cell
<code>is_sequential</code>	Indicates when an <code>is_sequential</code> attribute is set on the cell
cell_library	Name of the library in which the cell is defined

## See Also

- [Viewing Object Lists](#)
- [Port and Pin Lists](#)
- [Net Lists](#)
- [Design List](#)

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## Design List

The design list view displays information about the designs loaded into memory. The view consists of a table that shows design names, areas, directory paths, DesignWare implementations, and some attribute values.

You can

- Click a column heading to sort the table information alphabetically
- Click the heading again to reverse the sorting
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#))

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

The columns in the designs view table provide the following information:

Column	Description
Name	The name of the design
Design Area	The library area units occupied by the design
Dont Touch	Indicates when a <code>dont_touch</code> attribute is set on the design
Structure	Indicates when a <code>structure</code> attribute is set on the design
Flatten	Indicates when a <code>flatten</code> attribute is set on the design
DesignWare	The DesignWare implementation for the cell
Design Path	The absolute directory path to the file from which the design was loaded into memory

### See Also

- [Viewing Object Lists](#)
- [Cell Lists](#)
- [Port and Pin Lists](#)
- [Net Lists](#)

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## Histogram Views

Histograms are focal points of visual timing analysis. You can use histograms to view the overall timing performance of your design.

The Design Vision tool provides the following types of histograms for timing analysis:

- [Path Slack Histograms](#)
- [Net Capacitance Histograms](#)

In addition, when you examine timing paths in the path analyzer, the timing status summary or a path data table, you can create histograms that show the distribution of values for various types of path details (such as slack, endpoint clock skew, arrival time, or required time) listed in the timing path table.

The view window for a timing analysis histogram is split into two panes. By default, the histogram bar graph appears in the left pane and the object table appears in the right pane. You can use the split bars between the panes to increase or decrease the relative widths of the panes.

- When you hold the pointer over a bin in a histogram bar graph, the number of objects and the range of values represented by the bin appears in an InfoTip below the pointer.
- When you select a bin in a histogram bar graph, information about the objects and values that the bin represents appears in the object table.

You can use the arrow keys to scroll vertically or horizontally through the histogram bar graph, and you can use the Up Arrow and Down Arrow keys to scroll up or down in the object table. You can also filter the object table, limiting it to information based on a character string or regular expression that you define. For details, see [Filtering Object Lists](#).

You can set an option in the Application Preferences dialog box to display the object table below the bar graph in new histogram view windows. For details, see [Setting Global Default Preferences](#).

### See Also

- [Viewing High-Level Timing Results](#)
- [Creating Path Data Histograms](#)

## Path Slack Histograms

You use path slack histograms to view the overall performance of timing paths in your logic design.

Path slack histograms show a distribution of timing slack values for paths in a path group or for paths from, to, or through selected objects (pins, ports, nets, or clocks), using path selection similar to that for timing reports. The slack distribution provides a picture that helps you locate parts of the design that have the worst timing problems.

When you generate the histogram, you can select

- A maximum or minimum delay (setup or hold) option
- The maximum number of paths in a path group
- The maximum number of paths to any single endpoint

You can limit the histogram to paths between specific inputs, outputs, or registers by identifying their startpoints, endpoints, or throughpoints. You can also set options to customize the histogram, including the number of bins or a value range for the bins, and the lower and upper limits for the range of slack values.

A histogram view consists of a bar graph on the left and an object table on the right. In the bar graph, the number at the top of the tallest bin indicates the number of paths in the bin.

- Green bins (on the positive side of 0) contain paths with positive slack values.
- Red bins (on the negative side of 0) contain paths with negative slack values.

When you click a bin to select it, its color changes to yellow.

- You can hold the pointer over a bin to display the number of paths and the range of slack values in the bin (for example, Range: 0.08 to 0.496 Contents: 35.).
- You can select a bin to display its contents (slack values and startpoint and endpoint names) in the object table.

The table columns provide the following information:

Column	Description
Slack	Slack values
From	Full hierarchical names from the top-level design to the startpoint objects (ports or pins)
To	Full hierarchical names from the top-level design to the endpoint objects (ports or pins)

You can

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sorting information.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

### See Also

- [Histogram Views](#)
- [Opening a Path Slack Histogram](#)

## Net Capacitance Histograms

You use net capacitance histograms to view the overall performance of nets in your logic design.

Net capacitance histograms show a distribution of net capacitance values for all nets in the design. The capacitance distribution provides an overall picture of nets with the highest capacitance values in the design.

When you generate the histogram, you can set options to customize the histogram, including the number of bins or a value range for the bins, and the lower and upper limits for the range of capacitance values.

A histogram view consists of a bar graph on the left and an object table on the right. In the bar graph, the number at the top of the tallest bin indicates the number of nets in the bin.

When you click a bin to select it, its color changes to yellow.

- You can hold the pointer over a bin to display the number of nets and the range of capacitance values in the bin (for example, Range: 0.08 to 0.496 Contents: 35.).
- You can select a bin to display its contents (capacitance values and net names) in the object table.

The table columns provide the following information:

Column	Description
Capacitance	Capacitance values
Name	Full hierarchical names from the top-level design to the nets

You can

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sorting information.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

## See Also

- [Histogram Views](#)
- [Opening a Net Capacitance Histogram](#)

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## Logic Hierarchy Views

The logic hierarchy view helps you navigate the design hierarchy and gather design object information. The view window is divided into two panes, with an instance tree of instantiated cells in the left pane and a table containing object information in the right pane.

### Instance Tree

The instance tree lets you quickly navigate the design hierarchy and see the relationships among its levels. If you select a hierarchical cell (an instance that contains subblocks) in the instance tree, information about the objects in the cell appears in the object table. You can Shift-click or Control-click instance names to select combinations of cells.

The names of hierarchical cells are preceded by expansion buttons (plus or minus signs).

- A plus (+) sign means you can click the button to expand the list and display the names of the subblocks within the cell.
- A minus (-) sign means you can click the button to collapse the list and hide the names of subblocks.

You can use the arrow keys to navigate the instance tree. Use the Up Arrow and Down Arrow keys to move up or down the tree, the Right Arrow key to expand a cell, and the Left Arrow key to collapse a cell.

### Object Information

By default, the object table displays information about hierarchical cells belonging to the selected instance in the instance tree. You can

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sort.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to information based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

To display information about other types of objects, select the object types in the list above the table. You can display information about

- Hierarchical cells
- All cells
- Pins and Ports
- Pins of child cells
- Nets

For cells, the table columns provide the following information:

Column	Description
Cell Name	Cell instance name
Ref Name	Name of the design the cell references
Cell Path	Full hierarchical name from the top-level design to the cell
Don't touch	Indicates when a <code>dont_touch</code> attribute is set on the cell, instance, or reference

For pins and ports, the table columns provide the following information:

Column	Description
Pin Name	Object (short) name for the pin within the design
Pin Full Name	Full hierarchical name from the top-level design to the pin

For nets, the table columns provide the following information:

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**Column Heading Description**

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Net Name	Object (short) name for the net within the design
Net Full Name	Full hierarchical name from the top-level design to the net

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**See Also**

- [Browsing the Design Hierarchy](#)
- 

## Net Lists

Net list views display information about collections of nets. The view consists of a table that shows the net name, the full net name, and the status of the `dont_touch` attribute for each net in the collection.

You can

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sorting information.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

The columns in the cell view table provide the following information:

Column	Description
Net Name	Object (short) name for the net within the design
Net Full Name	Full hierarchical name from the top-level design to the net
<code>dont_touch</code>	Indicates when a <code>dont_touch</code> attribute is set on the net

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**See Also**

- [Cell Lists](#)
- [Port and Pin Lists](#)

- [Design List](#)
  - [Viewing and Selecting Objects](#)
- 

## Path Profile Views

Path profile views help you examine the contributions of individual cells and nets to the total delay in a timing path.

The view consists of a table that shows

- The path name, total delay time, relative pin delay contributions, and full path name for each path.
- The pin name, individual delay time, relative contribution, clock edge (rising or falling), and full pin name for each pin on a path.

At the top of the path profile view window are tabs that you can use to display the cell delay information in either of two different ways:

- Click the Hierarchy tab to display the pin information in an instance tree of hierarchical and leaf cells.
- Click the Flat tab to display the pin information in a flat list of pins.

The combined delays for each path and the relative delay contribution for each pin appear graphically in bar graphs that represent the percentages of the total path delay.

For each timing path listed in the view, the bar graph shows the percentages of the individual pin delays from startpoint to endpoint. For each pin on a path, the bar graph shows the percentage contribution of the pin delay to the total path delay.

Each path name is preceded by an expansion button (plus or minus sign).

- A plus (+) sign means you can click the button to expand the list and display the names of the hierarchical and leaf cell pins.
- A minus (-) sign means you can click the button to collapse the list and hide the pin names.

In the hierarchy display, an expansion button against a pin name indicates a pin on a hierarchical cell.

You can use the arrow keys to navigate through the table. Use the Up Arrow and Down Arrow keys to move up or down, the Right Arrow key to expand a path or hierarchical cell, and the Left Arrow key to collapse a cell.

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sorting information.  
To return the table rows to their initial order, right-click and choose Restore Original Ordering.
- You can scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

The columns in the table provide the following information:

Column	Description
Name	Path name or instance name of a pin on the path
Delay	Total path delay or individual pin delay
Bar	Percentage of total delay contributions to the path or percentage of individual pin delay contribution
Edge	Clock edge
Full Name	Full path name (composed of the name of each pin on the path) or full hierarchical pin name from the top-level design to the pin

## Port and Pin Lists

Port and pin list views display information about collections of ports and pins. The view consists of a table that shows the pin name, the full pin name, and the pin direction for each port or pin in the collection.

You can

- Click the column heading to sort the table information alphabetically. Click the heading again to reverse the sorting information.
- Scroll up and down in the table by pressing the Up Arrow and Down Arrow keys.
- Filter the objects listed in the table, limiting it to objects based on a character string or regular expression that you define (for details, see [Filtering Object Lists](#)).

If some of the text in a column is missing because the column is too narrow, you can hold the pointer over the column to display the text in an InfoTip. You can also adjust the width of a column by dragging its right edge left or right.

The columns in the ports and pins view table provide the following information:

Column	Description
Pin Name	Object (short) name for the port or pin within the design
Pin Full Name	Full hierarchical name from the top-level design to the port or pin
Pin Direction	Indicates whether the port or pin is an input, output, or inout port or pin

### See Also

- [Cell Lists](#)
- [Net Lists](#)
- [Design List](#)
- [Viewing and Selecting Objects](#)

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## Report Views

The report view displays report information. When you use a menu command to generate a report, Design Vision tool automatically opens a new report view. You can also open a blank report view (choose Window > New Report View) and use it to display reports saved in text files.

In reports that list object names (cell, net, port, and worst-path timing reports), you can select an object by clicking its name (blue text) in the report view. When you select an object in a report view, Design Vision tool displays a schematic view for the design in which the object is located and magnifies the schematic to fit the selected object in the view. The name of the selected object also appears in the selection list, and the object is displayed in the selection color (white) in all open schematic views.

You can use the Up Arrow and Down Arrow keys to scroll through the report.

The buttons at the bottom of the report view let you clear the view (remove the report text), save the report in a text file, and display a report saved in a text file.

- Clear contents  - Removes the report text from the report view.
- Open report file  - Displays a report saved in a text file.
- Save as -  - Saves the report in a text file.

## See Also

- [Viewing Reports](#)
- 

## Schematic Views

Schematic views display graphic representations of design logic and timing paths in a flat, single-sheet schematic that can span multiple hierarchy levels. You can use schematic views to visually analyze timing and logic in the optimized design and to gather information that can help you to guide later optimization operations.

A schematic can consist of instances (cells), ports, pins, nets, buses, bus rippers, and hierarchy crossings. An instance can be a block (a hierarchical cell representing the top-level design or a subdesign) or a leaf cell. A hierarchy crossing indicates a place where a timing path traverses the design hierarchy. When you select or highlight a timing path, the schematic represents the path as a series of net connections between pins or a pin and a port.

You can create a schematic for the top-level design, for a hierarchical cell, or for selected timing paths or design objects. The content of a schematic depends on the objects or timing paths that you select before opening the schematic view.

- If you select the instance of the top-level design, the schematic displays the logic elements in the design.

Hierarchical cells are displayed as abstract metacells. You can expand a hierarchical cell to display the logic elements in the subdesign, or you can move down into the cell and replace the schematic of the top-level design with a schematic of the a subdesign.

- If you select a hierarchical cell, the schematic displays the cell as an abstract metacell.

You can expand the cell to display the logic elements in the subdesign. Alternatively, you can move up or down the design hierarchy to display a schematic of the parent design or the subdesign.

- If you select a timing path, the schematic displays the cells, pins, nets, and ports on the path.

The selected path appears as a series of net connections between pins or a pin and a port. Hierarchy crossings indicate places where the path traverses the design hierarchy. You can select an object in the schematic and add fanin or fanout logic or worst case timing paths.

- If you select design objects, the schematic displays the objects and their connecting logic.

For example, if you select two cells, the schematic displays the cells and the pins and net that connect them. You can add or remove objects, add fanin or fanout logic, or add worst case timing paths.

You can also create a schematic of the power management cells in the design.

If you change the netlist for a design (for example, by using netlist editing commands such as `change_link`) when a schematic view is open, Design Vision tool immediately updates the schematic and maintains the current zoom level and pan position.

You can view information about an object in a schematic view by holding the pointer over the object. The object information appears in an InfoTip.

**Note:**

InfoTips are disabled by default. To enable InfoTips, choose View > InfoTips.

The type of information that an InfoTip displays depends on the object type.

- Cell information can include the cell instance name and the full (hierarchical) cell name plus information about each input or output pin on the cell.
- Pin information can include the full (hierarchical) pin name, the pin direction, and the arrival time, transition time, and slack time values.
- Net information can include the full (hierarchical) net name, the total net capacitance value, the number of local fanouts, and the total number of fanouts.

Local fanouts are the loads that directly connect to the net when pin directions are considered. Total fanouts are all the loads on the net that are driven by the same source or driver, regardless of the directions of hierarchical pins. Total fanout is the same as the fanout number provided in the net report.

- Port information can include the full (hierarchical) port name, the port direction, and the arrival time, transition time, and slack time values.
- Hierarchy crossing information can include the direction of the crossing (down a level into a subdesign or up a level to the parent design) and the full (hierarchical) name of the subdesign or parent design.

If you select an object (cell, pin, port, or net) in a schematic view, you can

- View a list of properties and their values associated with the selected object.

The property list differs for each object type. You can also edit some of the property values. For details, see [Viewing and Editing Object Properties](#).

- Generate a report about the object.

For details, see [Reporting Cell Information](#), [Reporting Port Information](#), and [Reporting Net Information](#).

- Apply constraints or other attributes to the object, or change the values of existing attributes.

You can set options on the View Settings panel to control whether object names are visible or hidden in schematic views. You can also change text colors, text sizes, and object colors.

### See Also

- [Schematic Views](#)
- [Examining Hierarchical Cells](#)
- [Examining Timing Paths and Selected Logic](#)
- [Changing the Appearance of Schematics](#)
- [Printing Schematic Views](#)
- [Examining Power Management Cells](#)

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## UPF Diagram Symbols and Standards

The UPF diagram visually conveys the IEEE 1801 low-power design intent as it is currently defined in the design database or the Visual UPF dialog box. IEEE 1801 is also known as Unified Power Format (UPF). By viewing the diagram, you can verify that the UPF power domains and supply network objects match your intent for the power architecture in your design.

For more information, see [UPF Diagram Symbols and Standards](#).

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## Panels

The following topics provide information about Design Vision panels:

- [Console](#)
- [Map Mode Panel](#)
- [Overview Panel](#)
- [Power State Table Panel](#)
- [Query Panel](#)

- [View Settings Panel](#)
  - [Visual Mode Panel](#)
- 

## Console

The console panel, docked by default above the status bar, provides a command-line interface, a log view that displays a transcript log of your session, and a history view that displays a list of the commands you have used during the session.

You can use the console to

- Enter `dc_shell` commands
- View the session transcript log or command history
- Search the session transcript for commands and messages
- Select and copy text in the session transcript
- View man pages by clicking underlined warning and error message numbers in the session transcript
- Save the session transcript in a text file
- Edit and reuse commands in the command history log
- Save the command history log in a Tcl script file

You can enter any `dc_shell` command on the command line at the bottom of the console. Enter the commands just as you would enter them on the `dc_shell` command line. For details, see [Entering Tcl Commands in the GUI](#).

When you enter a command, the command and any messages or output information appear in the session transcript. For example, if you enter `get_selection`, the transcript displays a list of the names of all selected objects.

You can edit and reuse commands on the command line. To display, edit, and reissue a previously entered command, you can

- Press the Up Arrow key to scroll up the command stack to the previous command, or press the Down Arrow key to scroll down in the command stack to the next command
- Press the Left Arrow key or the Right Arrow key to move the insertion point one character to the left or right on the command line
- Press the Home key or the End key to move the insertion point to the beginning or end of the command line

- Press the Tab key to complete a command, option, or file name
- Press the Enter key to issue the command

In addition, you can display a list of command options by typing the command name followed by a blank space and pressing Tab.

If you need to enter multiple-line commands, you can expand or shrink the command line.

- Press Shift-Return to expand the command line to display an additional line, and repeat for each line you want to add.
- Press Control-Return to shrink the command line to display a single line.

When the command line is expanded, you can press Shift+Up Arrow to scroll to the previous command in the command stack, or press Shift-Down Arrow to scroll to the next command in the command stack. The command line automatically shrinks to a single line when you issue a command.

To clear the command line, right-click and choose Clear.

### See Also

- [Console Log View](#)
- [Console History View](#)
- [Console Command-Line Editing](#)

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## Map Mode Panel

Use the Map Mode panel to adjust map mode display and style options for the active layout view. This panel is available only in the layout window and only when map mode is enabled in the active layout view.

When map mode is enabled in the layout view, you can set options on the Map Mode panel to

- View map information in the legend on the Map Mode panel
- Display or hide individual map colors (bins)
- Set map mode options

You can display or hide the Map Mode panel by choosing View > Toggle Transient Toolbars.

Each map color represents a range of values called a bin. The map legend on the Map Mode panel displays the color, the data count, and optionally the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the

relative distribution of map values in the bins. You can use the visibility options on the left side of the legend to display or hide map colors for individual bins.

To display or hide map colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click **Apply**.

By default, when you change settings on the Map Mode panel, you must click **Apply** before the changes take effect in the layout view. If you prefer, you can set the panel to apply your changes automatically as soon as you make them as follows:

To enable or disable the automatic apply mechanism,

- Click  and choose **Auto Apply**.

A check mark appears next to the **Auto Apply** command on the **Show Options** menu when the automatic apply mechanism is enabled.

Alternatively, when the automatic apply mechanism is disabled, you can reverse changes that you have not applied. You can also reset the map mode options to their default settings.

To reverse unapplied changes,

- Click  and choose **Cancel Changes**.

To reset the map mode options,

- Click  and choose **Defaults**.

You can customize individual bins in a map mode by changing one or more of the following style properties:

- Color
- Fill pattern
- Exaggeration value

For details, see [Changing Style Properties in a Map Mode or Visual Mode](#).

In addition, you can display or hide columns in the legend or adjust the exaggeration range for all visual modes and map modes. For details, see [Configuring Map Modes and Visual Modes](#).

### See Also

- [Analyzing Congestion](#)
  - [Viewing Cells in Congested Areas](#)
  - [Examining Cell Density](#)
  - [Examining Pin Density](#)
- 

## Overview Panel

The Overview panel lets you quickly change your view of the design in a layout view. A rectangle with a solid, yellow outline shows the portion of the design that is visible in the active layout view. Rectangles with solid gray outlines show the portions of the design that are visible in other open layout views.

You can use the Overview panel to

- Change the magnification in the active layout view
- Traverse the active layout view at the same magnification
- Control which layout view is the active view

The Overview panel is visible only when a layout view is open.

By default, when you open a layout window, the Overview panel is located to the left of the layout view above the View Settings Panel. If you close all layout views, the Overview panel is hidden automatically.

To enhance your viewing area, you can move the Overview panel to different locations inside or outside the window. You can also disable the Overview panel, hiding it from view. For details, see [Displaying or Hiding Toolbars and Pane](#) and [Moving Panels](#).

### See Also

- [Navigating Through Layout Views](#)
  - [Viewing the Floorplan in Design Compiler Graphical Tool](#)
- 

## Power State Table Panel

When the UPF diagram view is open, you can use the Power State Table panel to visually analyze the power state tables in a multivoltage design. You can view the states for each supply in a power state table and visually examine their relationships in the UPF diagram view.

The Power State Table panel is split vertically into three panes.

- The top pane displays a list with the names of the power state tables that you have defined for your design.
- When you select a power state table name in the top pane, the middle pane displays the power state table in a table view with a column for each supply and a row for each state.
- When you select a supply or state in the middle pane, the bottom pane displays a legend of the analysis results and the colors used in the UPF diagram view.

You can use the split bars between the panes to increase or decrease the relative height of each pane. To improve your viewing area, you can move the Power State Table panel to different locations inside or outside the window. For details, see [Moving Panels](#).

You begin the analysis by selecting the name of a power state table. You can perform the following types of analysis:

- Always-on analysis
- Multivoltage level-shifting

Always-on analysis compares the on-off states between supplies, including both power and ground supplies. This analysis helps you to decide if an isolation strategy is required between a driver supply and a load supply. The analysis produces one of the following states:

- More AO means that for all the combinations of states, there is never a case where the reference supply is off when the comparison supply is on.
- Less AO means that for all the combinations of states, there is never a case where the reference supply is on when the comparison supply is off.
- Equally AO means that the reference supply and comparison supply are always in the same state.

If either the reference supply or comparison supply is on, the other supply is also on. If either the reference supply or comparison supply is off, the other supply is also off.

- Unrelated AO means that the analysis could not define a relative on-off relationship between the reference and comparison supplies.

For example, in one state, the reference supply is on and the comparison supply is off, but in another state, the reference supply is off and the comparison supply is on.

In always-on analysis, you can compare all the supplies against all the other supplies. You can compare power supplies with ground supplies because the combination of power and ground defines the always-on relationships between power domains.

Multivoltage level-shifter analysis compares the voltage relationships between supplies. This analysis helps you to decide if a level shifter is needed between a driver supply and a load supply. The analysis produces one of the following states:

- LH means at least one power state exists for which a low-to-high-level shifter is required between the driver supply and the load supply.
- HL means at least one power state exists for which a high-to-low-level shifter is required between the driver supply and the load supply.
- HL\_LH means a level shifter that can handle both the low-to-high and high-to-low scenarios is required between the driver supply and the load supply.
- None means the driver and load supplies operate with the same voltages for each state.

In multivoltage level-shifter analysis, you can compare only the power supplies. The only ground supply states that the tool supports are 0 volts and off.

**Note:**

The Power State Table panel compares only nominal voltage values; it ignores any minimum and maximum voltage values set in a port or power state.

**See Also**

- [Visualizing Power State Tables](#)

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## Query Panel

The Query panel displays information about objects in the active schematic or layout view. The panel opens automatically when you enable the Query Tool left mouse button tool. When you click an object, the design and timing information for the object appears on the Query panel.

You can copy the text on the object information to the session transcript in the console log view by clicking the  button on the Query panel.

You can set options on the Options menu to control whether the Query panel

- Automatically copies the object information to the session transcript
- Automatically appears, if it is hidden, when you enable the Query tool
- Wraps the text on the Query panel

You can also open the Customize Query Toolbar dialog box and change the attribute groups that control how much information appears on the Query panel for certain types of objects.

## See Also

- [Reporting Net Information](#)
- 

## View Settings Panel

Use the View Settings panel to change display properties in graphic views. You can use display properties to customize the appearance of the active schematic, layout, or UPF diagram view. You can also save the current display properties in your preferences file, and you can load display properties from the preferences file.

To display or hide the View Settings panel,

- Choose View > Toolbars > View Settings.

A check mark next to View Settings command on the menu indicates that the View Settings panel is visible.

You can set different options for each open schematic or layout view. The options you set apply to the active view. By default, after you change one or more options, you must click the Apply button to apply the changes to the active view.

When a schematic view is the active view, you can

- Change the color brightness for all objects
- Display or hide object labels or annotations, change label or annotation text colors, and change label or annotation text sizes (click the Text tab)
- Change object colors (click the Objects tab)
- Change the display style for highlighted timing paths (click the Settings tab)
- Enable or disable InfoTips (click the Settings tab)

When a layout view is the active view, you can

- Change the color brightness for all visible objects
- Expand or collapse block abstractions and physical hierarchy blocks
- Control whether the Selection tool selects only highlighted objects
- Display or hide objects or object labels
- Display or hide cell orientations
- Enable or disable object selection
- Change object style properties, such as color or fill pattern

When a UPF diagram view is the active view, you can

- Apply a predefined or user-defined color theme
- Change the color brightness for all objects
- Change object colors
- Change the background color

You can use commands on the Options menu at the top of the View Settings panel to

- Enable or disable the automatic apply mechanism by choosing Show Options > Auto Apply.

The automatic apply mechanism automatically applies settings when you change them instead of only when you click Apply. This mechanism is disabled by default.

- Reset options to their state the last time you clicked Apply by choosing Show Options > Cancel changes.

This command is available only when Auto Apply is disabled.

- Save the current display properties in your preferences file by choosing Show Options > Save to Preferences.
- Load display properties from your preferences file by choosing Show Options > Set from Preferences.
- Save the current display properties in a Tcl script by choosing Show Options > Write Settings Script and entering a file name in the dialog box that appears.

**Note:**

Design Vision tool does not automatically saves display properties when you close the GUI or exit the session.

**See Also**

- [Changing the Appearance of Schematics](#)
- [Changing Layout Display Properties](#)
- [Changing UPF Diagram Display Properties](#)
- [Adjusting the Color Brightness](#)
- [Saving and Restoring View Settings](#)

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## Visual Mode Panel

Use the Visual Mode panel to adjust visual mode display and style options for the active layout view. This panel is available only in the layout window and only when visual mode is enabled in the active layout view.

When visual mode is enabled in the layout view, you can set options on the Visual Mode panel to

- View visual mode information in the legend on the Visual Mode panel
- Display or hide individual visual mode colors (bins)
- Set visual mode options

You can display or hide the Visual Mode panel by choosing **View > Toggle Transient Toolbars**.

Each visual mode color represents a set of values called a bin. The visual legend on the Visual Mode panel displays the color, the data count, and optionally the color exaggeration level for each bin. The colored histogram bars on the right side of the legend represent the relative distribution of values in the bins. You can use the visibility options on the left side of the legend to display or hide the colors for individual bins.

To display or hide visual mode colors in the layout view,

1. Select the visibility options for the colors you want to display, and deselect the visibility options for the colors you want to hide.
2. Click **Apply**.

By default, when you change settings on the Visual Mode panel, you must click **Apply** before the changes take effect in the layout view. If you prefer, you can set the panel to apply your changes automatically as soon as you make them.

To enable or disable the automatic apply mechanism,

- Click  and choose **Auto Apply**.

A check mark appears next to the **Auto Apply** command on the Options menu when the automatic apply mechanism is enabled.

Alternatively, when the automatic apply mechanism is disabled, you can reverse changes that you have not already applied. You can also reset the visual mode options to their default settings.

To reverse unapplied changes,

- Click  and choose **Cancel Changes**.

To reset the visual mode options,

- Click  and choose Defaults.

You can customize individual bins in a visual mode by changing one or more of the following style properties:

- Color
- Fill pattern
- Exaggeration value

For details, see [Changing Style Properties in a Map Mode or Visual Mode](#).

In addition, you can display or hide columns in the legend or adjust the exaggeration range for all visual modes and map modes. For details, see [Configuring Map Modes and Visual Modes](#).

### See Also

- [Using Visual Modes](#)
- [Selecting Objects in Visual Mode Bins](#)
- [Reordering Visual Mode Bins](#)

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## Menu Commands and Dialog Boxes

The following topics provide information about Design Vision menu commands and dialog boxes:

- [Cell \(Attributes > Optimization Directives\)](#)
- [Characterize \(Attributes > Operating Environment\)](#)
- [Compile Design \(Design Menu\)](#)
- [Compile Ultra \(Design Menu\)](#)
- [Derive Constraints \(Attributes > Optimization Constraints\)](#)
- [Design \(Attributes > Optimization Directives\)](#)
- [Design Constraints \(Attributes > Optimization Constraints\)](#)
- [Drive Strength \(Attributes > Operating Environment\)](#)
- [Flip-Flop \(Attributes > Optimization Directives > Cell\)](#)

- [Flip-Flop \(Attributes > Optimization Directives > Design\)](#)
- [Input Delay \(Attributes > Operating Environment\)](#)
- [Input Port \(Attributes > Optimization Directives\)](#)
- [Latch \(Attributes > Optimization Directives > Cell\)](#)
- [Latch \(Attributes > Optimization Directives > Design\)](#)
- [Load \(Attributes > Operating Environment\)](#)
- [Net \(Attributes > Optimization Directives\)](#)
- [Operating Conditions \(Attributes > Operating Environment\)](#)
- [Output Delay \(Attributes > Operating Environment\)](#)
- [Output Port \(Attributes > Optimization Directives\)](#)
- [Pin \(Attributes > Optimization Directives\)](#)
- [Selection List \(Select Menu\)](#)
- [Set Equal \(Attributes > Optimization Directives > Input Port\)](#)
- [Set Opposite \(Attributes > Optimization Directives > Input Port\)](#)
- [Specify Clock \(Attributes Menu\)](#)
- [Timing Constraints \(Attributes > Optimization Constraints\)](#)
- [Timing Paths \(Attributes > Optimization Directives\)](#)
- [Timing Range \(Attributes > Operating Environment\)](#)
- [Understanding Filter Expressions](#)
- [Using the Visual UPF Dialog Box](#)
- [Wire Load \(Attributes > Operating Environment\)](#)

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## Cell (Attributes > Optimization Directives)

Use Cell to set instance-specific cell attributes throughout the design hierarchy.

When you select a cell and choose Attributes > Optimization Directives > Cell, the Cell Attributes dialog box appears. You can set compilation attributes that control how the cell is treated during design optimization. For sequential elements, you can also select the flip-flop and latch types which specify the maximum borrowing time, and control scan cell replacement.

**Note:**

You can also open this dialog box by selecting a cell in a schematic view or a cell name in a logic hierarchy view, right-click, and then choose Edit Attributes.

The appearance of the dialog box depends on the number and type of cells that you select.

- If you select a single cell, its name appears in the Cell name text box, and the options in the dialog box indicate the current attribute status for the cell. The name and options change automatically when you select a different cell.
- If you select more than one cell, the option Multiple selected appears in the Cell name text box, and the options in the dialog box are set to default. However, the attributes that you set apply to all of the selected cells.

Following are the options available in the Cell Attributes dialog box:

- Cell name - Displays the name of the selected cell, if only one cell is selected, or displays Multiple selected option if multiple cells are selected.
- Referencing - Displays the cell's reference name, which is either a library cell name or a subdesign name.
- Compile attributes
  - Ungroup cell's hierarchy - Controls whether the cell is a subdesign that is to be ungrouped during design optimization.  
Command cross-reference: `set_ungroup`
  - Don't touch - Controls whether the cell is to be skipped during design optimization.  
Command cross-reference: `set_dont_touch`
  - Allow boundary optimization - Controls whether to allow logic optimization across hierarchical boundaries during design optimization.  
Command cross-reference: `set_boundary_optimization`
- Sequential elements
  - [Flip-Flop \(Attributes > Optimization Directives > Cell\)](#) - Opens the Cell Default Flip-Flop Type dialog box, in which you can see and change the preferred flip-flop type used during design optimization.
  - [Latch \(Attributes > Optimization Directives > Cell\)](#) - Opens the Cell Default Latch Type dialog box, in which you can see and change the preferred latch type used during design optimization.

- Max time borrow - Specifies the amount of time borrowing permitted for sequential elements in the selected cells.

Command cross-reference: `set_max_time_borrow number`

- Scan Replacement

- Always - Controls whether not scannable cells are always replaced with their scannable equivalents.

Command cross-reference: `set_scan true`

- Never - Controls whether not scannable cells are never replaced with their scannable equivalents.

Command cross-reference: `set_scan false`

---

## Characterize (Attributes > Operating Environment)

Use Characterize to capture environment information about the selected cells and to assign it as attributes on the designs to which the cells are linked.

When you select one or more cells and choose Attributes > Operating Environment > Characterize, the Characterize dialog box appears. You can choose which types of environment information to capture from the selected cells (timing, constraint, or connection) and to apply as attributes to the designs the cells reference. By default, only timing information is captured and assigned.

The appearance of the dialog box depends on the number and type of cells that you select.

- If you select a single cell, its name appears in the Cell name text box. The name changes automatically when you select a different cell.
- If you select more than one cell, the placeholder <Multiple selected> option appears in the Cell name text box.

Following are the options available in the Characterize dialog box:

- Cell name - Displays the name of the selected cell, if only one cell is selected, or displays <Multiple selected> option if multiple cells are selected.

Command cross-reference: `characterize cell_name`

- Timing - Controls whether Design Vision tool records timing characteristics for the selected cells.

Command cross-reference: `characterize -no_timing`

- Constraints - Controls whether Design Vision tool records constraint information (area, power, connection class, and design rule constraints) for the selected cells.

Command cross-reference: `characterize -constraints`

- Connections - Controls whether Design Vision tool records logical connection (port) information for the selected cells.

Command cross-reference: `characterize -connections`

## See Also

- [Characterizing the Context of a Subdesign Instance](#)

## Compile Design (Design Menu)

Use Compile Design to perform logic and gate-level synthesis and optimization on the current design and its subdesigns. During optimization, incremental status reports are displayed in the console log view each time a transformation is applied to the design. These reports include the elapsed time, area, worst negative slack, total negative slack, design rule cost, and endpoint.

If the current design or any of its subdesigns is represented as a state table, finite state machine optimization is automatically performed on these designs.

When you choose Design > Compile Design, you see the Compile Design dialog box. You can

- Set mapping options to control the relative efforts for design mapping and area recovery
- Set compile options to control whether the compiler
  - Fixes design rule and top-level timing violations
  - Maps the circuit by using only local mapping transformations that improve the circuit
  - Removes all levels of hierarchy in the design (except for subdesigns assigned the `dont_touch` attribute)
  - Automatically removes levels of hierarchy in the design
  - Optimizes the design across all hierarchical boundaries
  - Exactly matches sequential elements with their descriptions in the HDL code (for designs that contain SEQUEM elements)

- Set design rule options that control whether the compiler maps the design, fixes design rule violations, or both
- Set background compilation options to run the compiler in the background or across the network on another machine

If you are using TestMAX DFT, you can also set a compile option that performs a test-ready compile by replacing all sequential elements with scan-equivalent cells.

Following are the options available in the Compile Design dialog box:

- Mapping options
  - Map design - Controls how the design is represented. By default, when Map design is selected, the compiler maps the design to the current technology library during design optimization. Uncheck this option if you want the compiler to use generic Boolean equations and generic flip-flops to represent the optimized design instead of mapping the design to the technology library.

Command cross-reference: `compile -no_map`

- Map effort - Sets the relative amount of CPU time spent on mapping to Medium or High. The default is Medium. These options are available only when the Map design option is selected.

Command cross-reference: `compile -map_effort`

- Area effort - Lets you select the relative effort (in terms of CPU usage) for the area recovery phase of design optimization. The options are None, Low, Medium, and High. The default is None. These options are available only when the Map design option is selected.

Command cross-reference: `compile -area_effort`

#### Compile options

- Top level - Controls whether the compiler fixes design rule and top-level timing violations but does not perform any mapping during design optimization. You cannot use this option on designs that contain unmapped logic.

Select this option when you want the compiler to fix all design rule violations and any timing violations for paths that cross hierarchical boundaries by default. If you want to fix timing violations for all paths, set the `compile_top_all_paths` variable to `true`.

Command cross-reference: `compile -top`

- Incremental mapping - Controls whether the compiler maps the circuit by using only local mapping transformations that improve the circuit.

Command cross-reference: `compile -incremental_mapping`

- Ungroup all - Controls whether the compiler removes all levels of hierarchy in the design except for subdesigns assigned the `dont_touch` attribute.

Command cross-reference: `compile -ungroup_all`

- Allow boundary condition - Controls whether the compiler optimizes across all hierarchical boundaries.

**Note:**

Selecting this option can change the function of the design. For more details, see the man page for the `compile` command.

Command cross-reference: `compile -boundary_optimization`

- Scan - Controls whether the compiler replaces all sequential elements with scan-equivalent cells during design optimization. Select this option when you want the compiler to perform a test-ready compile.

Command cross-reference: `compile -scan`

- Auto ungroup - Controls whether the compiler automatically removes levels of hierarchy in the design for all cells except those cells that
  - Have been assigned the `dont_touch` attribute
  - Have explicit constraints set on their pins
  - Have a wire load model that is different from the wire load model for the parent cell
  - Have more child cells than the value of the `compile_auto_ungroup_num_cells` variable

The compiler ungroups the cells based either on area or timing delays. When you select the Auto ungroup option, the Area and Delay options are enabled. Area is selected by default.

- Area - Ungroups all hierarchical cells except those that meet the criteria listed above.

Use the Area option when you need to ungroup small hierarchies to improve area recovery. In most cases, the Area option does not significantly affect the timing of the design.

Command cross-reference: `compile -auto_ungroup area`

- Delay - Attempts to improve the overall timing of the design by ungrouping hierarchies that are most likely to benefit from the extra boundary optimization provided by ungrouping.

When you select the Delay option, the compiler tries to find and ungroup hierarchical cells containing paths that either are critical or are likely to become critical during subsequent optimization steps. Using Auto ungroup with the Delay option is a less CPU-intensive alternative to the ungroup all option for improving design timing.

Command cross-reference: `compile -auto_ungroup delay`

- Exact map - Controls whether the sequential elements in the optimized design must exactly match the descriptions specified in the HDL code.

If your design contains SEQUEM elements, select this option when you need to force the compiler to search the target libraries for sequential elements that match only the behavior of the SEQUEM elements (without considering the surrounding logic). If an exact match is not available, another sequential element is used.

**Note:**

SEQUEM is a technology-independent representation of a sequential element that is inferred by the HDL compiler from HDL descriptions of sequential circuits. For more details, see the [compile man page](#).

Command cross-reference: `compile -exact_map`

Design rule options - Lets you control whether the compiler optimizes the design, fixes design rules, or both when you click OK or Apply.

- Fix design rules and optimize mapping - Lets the compiler attempt to fix design rules during design optimization. This is the default design rule option.
- Optimize mapping only - Prevents the compiler from fixing any design rule violations during design optimization. This option allows you to view the violations in a constraint report before fixing them. For details, see [Reporting Constraint Violations](#).

Command cross-reference: `compile -no_design_rule`

- Fix design rules only - Forces the compiler to fix design rule violations without performing design optimization.

Command cross-reference: `compile -only_design_rule`

- Fix hold time only - Forces the compiler to fix only hold time violations for clocks that have been assigned the `hold_fix` attribute (and to ignore all other design rule violations) during design optimization. When you select this option, the compiler attempts to fix `hold_fix` attribute violations if the delay (setup) cost is not increased or if hold violations have been given a higher priority than maximum delay cost.

For details about attribute priorities, see the `set_cost_priority` man page. For details about the `hold_fix` attribute, see the `set_fix_hold` man page.

Command cross-reference: `compile -only_hold_time`

#### Verification options

##### Note:

Do not use these options. The `compile` command verification options are obsolete.

#### Background compilation options

- Background - Controls whether the compiler runs in the background. To run the compiler in the background, you must specify the following options:
  - Run directory - Specifies the relative or absolute path to the directory where you want to save the optimization results. The compiler creates this directory; it must not already exist. This option is available only when the Background option is selected.

Command cross-reference: `compile -background path_name`

- Host Name - Specifies the host name of the machine where you want to run the compiler in the background. The name you specify must be a valid host name on the network, and Design Compiler must be licensed to run on the machine. This option is available only when the Background option is selected.

Command cross-reference: `compile -host host_name`

- Architecture - Specifies the hardware architecture of the machine where you want to run the compiler in the background. If you do not specify the architecture, the compiler assumes it is the same as that of the machine where you are running Design Vision tool. This option is available only when the Background option is selected.

Command cross-reference: `compile -arch architecture`

- Xterm Window - Controls whether the results of running the compiler in the background can be monitored on the X-terminal. This option is available only when the Background run option is selected and is valid only in the X11 environment.

Command cross-reference: `compile -xterm`

#### See Also

- [Optimizing the Design](#)
- [Compile Ultra \(Design Menu\)](#)

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## Compile Ultra (Design Menu)

Use Compile Ultra to obtain better quality of results (QoR) when you compile designs that have significantly tight timing constraints. This is a push-button solution for timing-critical, high performance designs that encapsulates DC Ultra strategies into a single command. It allows you to apply the best possible set of timing-centric variables for critical delay optimization and improvement in area QoR.

**Note:**

This command requires a DC-Ultra license and a DesignWare Foundation license.

When you choose Design > Compile Ultra, you see the Compile Ultra dialog box. You can select compile options, a design rule option, and a timing or area high effort option. You can also select compile options to

- Fix design rule and top-level timing violations for paths that cross hierarchical boundaries
- Prevent optimization across hierarchical boundaries
- Perform clock gate optimization (by automatically inserting or removing clock gates)
- Prevent the compiler from inverting sequential elements during mapping and optimization
- Perform incremental improvements on the gate structure without remapping the design
- Disable all automatic ungrouping operations and preserve all user hierarchies during optimization
- Enable adaptive retiming during optimization

If your design contains SEQUEM elements, you can select an option to force the compiler to search the target libraries for sequential elements that match only the behavior of the SEQUEM elements.

If you are using TestMAX DFT, you can select an option that performs a test-ready compile by replacing all sequential elements with scan-equivalent cells.

Following are the options available in the Compile Ultra dialog box:

Compile options

- Top level - Controls whether the compiler fixes design rule and top-level timing violations but does not perform any mapping during design optimization. You cannot use this option on designs that contain unmapped logic.

Select this option when you want the compiler to fix all design rule violations and any timing violations for paths that cross hierarchical boundaries by default. If you want to fix timing violations for all paths, set the `compile_top_all_paths` variable to true.

In topographical mode, if you select this option, the compiler automatically back-annotates the top-level design with virtual placement-based delays of subblocks while preserving the logic structure of the subblocks.

The Top level option is incompatible with the Incremental mapping option, the Use timing script option, and the Use area script option.

Command cross-reference: `compile -top`

- No hierarchical boundary optimization - Controls whether the compiler optimizes across all hierarchical boundaries. Select this option to prevent optimization across hierarchical boundaries.

Command cross-reference: `compile_ultra -no_boundary_optimization`

- Scan - Controls whether the compiler replaces all sequential elements with scan-equivalent cells during optimization. Select this option when you want the compiler to perform a test-ready compile.

Command cross-reference: `compile -scan`

- Gate Clock - Controls whether the compiler performs clock gating (by automatically inserting or removing clock gates) during optimization. Select this option to allow clock gate optimization. If the `power_driven_clock_gating` variable is set to true, the compiler optimizes clock gates based on the switching activity and dynamic power of the register banks.

You cannot select both the Clock gate option and the Fix design rules only option. If you select both the Clock gate option and the Exact map option, the compiler might not be able to exactly match the descriptions specified in the HDL code for registers that are involved in clock gate optimization.

Command cross-reference: `compile_ultra -gate_clock`

- No sequential output inversion - Controls whether the compiler can invert sequential elements during mapping and optimization. Select this option to prevent the compiler from inverting sequential elements. For more information about sequential output inversion, see the man page for `compile_seqmap_enable_output_inversion` variable.

Command cross-reference: `compile_ultra -no_seq_output_inversion`

- Incremental mapping - Controls whether the compiler attempts to make incremental changes in the gate structure without rerunning the mapping and implementation stages. Select this option to allow incremental changes.

**Note:**

In topographical mode, using the Incremental mapping option with a topographical netlist results in placement-based optimization only; it is not an incremental mapping.

The Incremental mapping option is incompatible with the Top level option, the Use timing script option, and the Use area script option.

Command cross-reference: `compile -incremental_mapping`

- No auto ungroup - Controls whether the compiler automatically removes levels of hierarchy in the design for all cells except those cells that
  - Have been assigned the `dont_touch` attribute
  - Have explicit constraints set on their pins
  - Have a wire load model that is different from the wire load model for the parent cell
  - Have more child cells than the value of the `compile_auto_ungroup_num_cells` variable

Select this option to disable all automatic ungrouping operations and preserves all user hierarchies.

Command cross-reference: `compile_ultra -no_autoungroup`

- Exact map - Controls whether the sequential elements in the optimized design must exactly match the descriptions specified in the HDL code.

If your design contains SEQUEM elements, select this option when you need to force the compiler to search the target libraries for sequential elements that match only the behavior of the SEQUEM elements (without considering the surrounding logic). If an exact match is not available, another sequential element is used.

**Note:**

SEQUEM is a technology-independent representation of a sequential element that is inferred by the HDL compiler from HDL descriptions of sequential circuits. For more details, see the `compile` man page.

Command cross-reference: `compile -exact_map`

- Retime - Controls whether the compiler uses adaptive retiming during optimization. Select this option to enable adaptive retiming. The compiler ignores this option if you

also select the Top level option, the Incremental mapping option, or the Fix design rules only option.

Command cross-reference: `compile_ultra -retime`

#### Design rule options

- Fix design rules and optimize mapping- Lets the compiler attempt to fix design rules during design optimization. This is the default design rule option.
- Optimize mapping only - Prevents the compiler from fixing any design rule violations during design optimization. This option allows you to view the violations in a constraint report before fixing them. For details, see [Reporting Constraint Violations](#).

Command cross-reference: `compile -no_design_rule`

- Fix design rules only - Forces the compiler to fix design rule violations without performing design optimization.

Command cross-reference: `compile -only_design_rule`

#### Timing and area high effort

- Dont use timing and Area scripts - Disables the strategic optimization processes that attempt to improve timing or area results. This is the default timing and area high effort option.
- Use timing script - Enables a strategic optimization process that attempts to improve delay optimization but might increase runtime. This process can include changes to variables or constraints that modify `compile_ultra` behavior and additional passes to achieve better timing results.

Command cross-reference: `compile_ultra -timing_high_effort_script`

- Use area script - Enables a strategic optimization process that attempts to improve area optimization but might increase runtime. This process can include changes to variables or constraints that modify `compile_ultra` behavior and additional passes to achieve better area results.

Command cross-reference: `compile_ultra -area_high_effort_script`

#### See Also

- [Optimizing the Design](#)
- [Compiling the Design](#)

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## Derive Constraints (Attributes > Optimization Constraints)

Use Derive Constraints to derive timing constraints from existing timing information for timing paths in the current design. Both sequential and combinational constraints are derived for all previously unconstrained timing paths.

When you choose Attributes > Optimization Constraints > Derive Constraints, the Derive Constraints dialog box appears. You can select or deselect options to derive maximum and minimum delay constraints for combinational paths, maximum period constraints and hold constraints for clocks, and separate rise and fall constraints for combinational timing endpoints. You can also set maximum delay, minimum delay, and maximum period scaling factors.

The following options are available in the Derive Constraints dialog box:

- Maximum period - Controls whether the compiler derives maximum period constraints for clocks in the current design.
- Fix hold - Controls whether the compiler derives hold constraints for unconstrained clocks in the design.
- Separate rise and fall - Controls whether the compiler derives separate rise and fall constraints for each combinational timing endpoint.
- Maximum delay - Controls whether the compiler derives maximum delay constraints for unconstrained combinational paths in the current design.
- Minimum delay - Controls whether the compiler derives minimum delay constraints for unconstrained combinational paths in the current design.
- Scaling factors
  - Max delay - Sets the maximum delay scaling factor.
  - Min delay - Sets the minimum delay scaling factor.
  - Max period - Sets the maximum period scaling factor.

### See Also

- [Deriving Timing Constraints](#)

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## Design (Attributes > Optimization Directives)

Use Design to set attributes that control design optimization on the current design.

When you choose Attributes > Optimization Directives > Design, the Design Attributes dialog box appears. You can select options to

- Ungroup the design
- Allow logic optimization across hierarchical boundaries
- Prevent modifications to cells, nets, designs, and references
- Permit the use of wired logic
- Attach I/O pads to ports
- Enable flattening
- Determine how the design is structured

You can also select a scan test implementation style, the CPU effort level, the minimization strategy, and the phase assignment strategy for flattening. You can control whether the compiler uses timing-driven structuring, Boolean optimization, or both to determine how the design is structured.

You can open additional dialog boxes that allow you to select the preferred flip-flop type, select the preferred latch type, and set the characteristics for I/O pads connected to ports.

Following are the options available on the Design Attributes dialog box:

- Current design - Displays the name of the current design.
- Ungroup - Sets the `ungroup` attribute on the current design. Select this option to ungroup (collapse to one design level) the design during design optimization.  
  
Command cross-reference: `set_ungroup`
- Boundary optimization - Sets the `boundary_optimization` attribute on the current design. Select this option to allow logic optimization across hierarchical boundaries during design optimization.  
  
Command cross-reference: `set_boundary_optimization`
- Don't touch - Sets the `dont_touch` attribute on the cells, nets, designs, and references in the current design. Select this option if you want to prevent modifications to these objects during design optimization.  
  
Command cross-reference: `set_dont_touch`
- Test scan style - Sets the scan test implementation style for the current design. The choices are
  - <NONE>
  - Multiplexed Flip-Flop
  - LSSD

- Clocked Scan
- Auxiliary Clock LSSD
- Combinational

**Note:**

Select Combinational if your design does not contain sequential cells (flip-flops or latches).

To verify the scan style for a design, select the Methodology option in the Test - Report Test dialog box (choose Test > Internal Scan and click the Display Reports button). For more details on these scan styles, see the *Design Compiler User Guide*.

Command cross-reference: `set_scan_style test_scan_style`

- [Flip-Flop \(Attributes > Optimization Directives > Design\)](#) - Opens the Default Flip-Flop Type dialog box, which can be used to set the preferred flip-flop type for design optimization.
- [Latch \(Attributes > Optimization Directives > Design\)](#) - Opens the Default Latch Type dialog box, which can be used to set the preferred latch type for design optimization.
- Flatten logic - Controls whether the `flatten` attribute is set on the current design. Select this option to enable flattening during design optimization.

Command cross-reference: `set_flatten`

The following options are available only when Flatten logic is selected:

- Flatten effort - Sets the CPU effort level for flattening the design. The choices are Low, Medium, or High. The default is Low.

Command cross-reference: `set_flatten -effort`

- Flatten Minimize - Sets the minimization strategy for use after a design is flattened. The choices are
  - Single output
  - Multiple output
  - None

The default is Single output, which causes the compiler to independently minimize the equations for each output in the design. Select Multiple output if you want the compiler to minimize all logic for the design. Select None if you do not want the compiler to minimize outputs.

Command cross-reference: `set_flatten -minimize`

- Flatten phase - Sets the phase assignment strategy for the current design. The choices are
  - Don't apply
  - Apply strategy

The default is Don't apply, which means the compiler does not invert the phase of outputs during flattening. Select Apply strategy if you want the compiler to invert the phase of outputs.

Command cross-reference: `set_flatten -phase`

- Structure logic - Controls whether structure attributes are set on the current design. Select this option when you want to determine how the design is structured during design optimization.

Command cross-reference: `set_structure`

The following options are available only when Structure logic is selected:

- Apply timing driven structuring - Sets the `structure_timing` attribute on the current design. Select this option to let the compiler use timing-driven structuring during design optimization.

Command cross-reference: `set_structure -timing`

- Apply Boolean optimization - Sets the `structure_boolean` attribute on the current design. Select this option to let the compiler use Boolean (nonalphabetic) optimization.

Command cross-reference: `set_structure -boolean`

## Design Constraints (Attributes > Optimization Constraints)

Use Design Constraints to set design objectives for the top level of the current design.

When you choose Attributes > Optimization Constraints > Design Constraints, the Design Constraints dialog box appears. You can enter values for optimization constraints (maximum area, maximum dynamic power, and maximum leakage power) and for design rule constraints (maximum fanout load and maximum transition time). You can also select a minimum fault coverage percentage and control whether area or timing considerations take precedence over fault coverage.

Following are the options available in the Design Constraints dialog box:

- Current design - Displays the name of the current design.
- Optimization constraints

- Max area - Specifies the value, in technology library area units, of the maximum area constraint for the design.  
 Command cross-reference: `set_max_area value`
- Max dynamic power - Specifies the value, in technology library power units, of the maximum power constraint for the design.  
 Command cross-reference: `set_max_power value`
- Max leakage power - Specifies the value, in technology library power units, of the maximum leakage power constraint for the design.  
 Command cross-reference: `set_max_leakage_power value`
- Design rules
  - Max fanout - Specifies the value, in technology library time units, of the maximum fanout load that can be driven by any port or pin in the design.  
 Command cross-reference: `set_max_fanout value`
  - Max transition - Specifies the value, in technology library time units, of the maximum transition time for any transitioning net in the design.  
 Command cross-reference: `set_max_transition value`
- Test constraints
  - Min fault coverage lets you select the minimum fault coverage for the design. The default is 80 percent.  
 You can use the Area critical and Timing critical options to control the relationship between fault coverage and area or timing considerations.  
 Command cross-reference: `set_min_fault_coverage number`
    - Area critical controls whether area considerations take precedence over fault coverage. By default, fault coverage takes precedence over area considerations. Select this option if you want area considerations to take precedence over fault coverage.  
 Command cross-reference: `set_min_fault_coverage -area_critical`
    - Timing critical controls whether timing considerations take precedence over fault coverage. By default, fault coverage takes precedence over timing considerations. Select this option if you want timing considerations to take precedence over fault coverage.  
 Command cross-reference: `set_min_fault_coverage -timing_critical`

### See Also

- [Setting Transition Time Constraints on Nets](#)
- [Setting Fanout Load Constraints on Nets](#)
- [Setting Area Constraints](#)
- [Input Port \(Attributes > Optimization Directives\)](#)
- [Output Port \(Attributes > Optimization Directives\)](#)

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## Drive Strength (Attributes > Operating Environment)

Use Drive Strength to assign or remove drive characteristics for top-level input or inout (bidirectional) ports of the current design. This option affects the port transition delay and can also place design rule requirements (such as maximum fanout or maximum transition time) on the ports.

The compiler uses drive strength to buffer nets appropriately in the case of a weak driver. Drive strength is the reciprocal of the driver resistance. The transition time delay at an input port is the product of the drive resistance and the capacitance load of the input port.

By default, the compiler assumes a drive resistance of 0, which means an infinite drive strength, for ports that have not been assigned drive characteristics.

**Note:**

For heavily loaded driving ports, such as clock lines, you should keep the drive strength at 0 to prevent the compiler from buffering the net. Each semiconductor vendor has a different way of distributing these signals within the silicon.

You set drive characteristics for a port by associating the port with a library cell or pin so that the delay calculators can accurately model the drive capability of an external driver. You can remove the drive characteristics for a port when you want it to have the default drive resistance of 0.0.

When you select one or more input or inout ports and choose Attributes > Operating Environment > Drive Strength, the Drive Strength dialog box appears. You can assign or remove drive characteristics for the selected ports.

To assign drive characteristics, you specify a technology library name, the name of a cell in the technology library, the name of the pin that you need to use as the driving pin (if the cell has more than one output pin), and the input pin (if the driving cell has more than one input pin and the arcs from those pins have different drive characteristics). You can also

- Specify a multiplication factor for the delay characteristics
- Control whether the drive capability is scaled according to the current operating environment
- Control whether design rule attributes associated with the driving cell are applied to the ports
- Control whether the drive characteristics are applied for the rising clock edge, the falling clock edge, or both
- Specify the input rise transition time for the rising case or the input fall transition time for the falling case

The appearance of the dialog box depends on the number and type of ports or pins that you select.

- If you select a single port, its name appears in the Port name text box, and the options in the dialog box indicate its current input delay status. The name and options change automatically when you select a different port or pin.
- If you select more than one port, their names appear in the Port name text box, and the options in the dialog box are set to default. However, the delays that you set apply to all of the selected ports.
- If you select a bus port, the Bus Selector dialog box appears with all the bits selected in the Port bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Name box in the Input Drive Strength dialog box changes automatically to display a bus name composed of the selected bits.
- If you select ports for a mixture of buses and individual nets, the placeholder <Multiple selected> appears in the Port name text box.

You can use the Report Ports dialog box (choose Design > Report Ports and select the Show only input port drive option) to see the drive information for input ports. For details, see [Reporting Port Information](#).

**Note:**

You can use the `set_drive` and `set_input_transition` commands to set the drive resistance and transition delay on top-level ports for which the input port drive capability cannot be characterized with a cell in the technology library. However, these commands are not as accurate for nonlinear delay models.

For more information about setting the drive characteristics for input ports, see the *Design Compiler User Guide*.

The following options appear in the Drive Strength dialog box:

- Port name - Displays the names of the selected ports.

Command cross-reference:

- `set_driving_cell port_list`
- `remove_driving_cell port_list`

- Library cell options - Controls whether driving cell attributes are applied to (when selected) or removed from (when deselected) the selected ports.

When you select the Use library cell option, the other options in the dialog box become available. You must specify the name of the library cell and, if the cell has more than one output pin, select the name of the output pin that you want to use to drive the selected ports.

Command cross-reference: `set_driving_cell`

- Library cell name - Specifies the name of the library cell to be used to drive the selected ports.

You can enter the names in the text box or use one of the buttons to select the cells.

Command cross-reference: `set_driving_cell -lib_cell cell_name`

- Cell's output pin name - Specifies the name of the output pin on the driving cell. Select the name of the pin you want to use to drive the selected ports. By default, the first timing arc found on the driving cell is used to drive the ports.

This option is required when the cell has more than one output pin.

Command cross-reference: `set_driving_cell -pin pin_name`

- Cell's input pin name - Specifies the name of the input pin on the driving cell. Select the name of the pin you want to use to drive the selected ports. By default, the first timing arc found on the driving cell is used to drive the ports.

This option is required when the driving cell has more than one input pin and the arcs from those pins have different drive characteristics.

Command cross-reference: `set_driving_cell -from_pin from_pin_name`

- Library name - Displays the name of the technology library in which the library cell is located. Enter a different name if you want to use a cell in a different technology library.

Command cross-reference: `set_driving_cell -library library_name`

- **Multiplication factor** - Specifies a factor by which the compiler multiplies the delay characteristics of the selected ports. Both the load delay and the transition times are affected. The default is 1.0.

Command cross-reference: `set_driving_cell -multiply_by factor`

- **Don't scale** - Controls whether the timing analyzer scales the drive capability of the selected ports according to the current operating conditions. Select this option when you do not want to scale the port drive capability. By default, this option is deselected and the port drive capability is scaled for operating conditions exactly to match the way the driving cell would be scaled.

Command cross-reference: `set_driving_cell -dont_scale`

- **No design rule** - Controls whether the design rule attributes associated with the driving cell are applied to the selected ports. The design rule attributes that can be derived from a driving cell are `max_fanout`, `max_capacitance`, `max_transition`, `min_fanout`, `min_capacitance`, and `min_transition`. Select this option when you do not want to derive design rule attributes from the driving cell and apply them to the ports the cell drives. By default, this option is deselected and the design rule attributes are applied to the ports.

**Note:**

Timing attributes derived from the driving cell are always applied to the ports the cell drives.

Command cross-reference: `set_driving_cell -no_design_rule`

- **Rise only** - Controls whether the drive characteristics apply only to the rising clock edge. When you select this option, the Fall only option is unavailable. By default, both the Rise only and Fall only options are deselected and the drive characteristics apply to both the rising and falling clock edges.

Command cross-reference: `set_driving_cell -rise`

- **Input rise transition time** - Specifies the input rise transition time associated with the input pin on the driving cell. The default is 0.

Command cross-reference: `set_driving_cell -input_transition_rise_time`

- **Fall only** - Controls whether the drive characteristics apply only to the falling clock edge. When you select this option, the Rise only option is unavailable. By default, both the Rise only and Fall only options are deselected and the drive characteristics apply to both the rising and falling clock edges.

Command cross-reference: `set_driving_cell -fall`

- Input fall transition time - Specifies the input fall transition time associated with the input pin on the driving cell. The default is 0.

Command cross-reference: `set_driving_cell -input_transition_fall_time`

- Remove cell attributes - Removes all drive characteristics from the selected cells, including both driving cell attributes applied by the `set_driving_cell` command and drive resistance attributes applied by the `set_drive` command.

Command cross-reference: `remove_driving_cell`

## See Also

- [Defining Drive Characteristics for Input Ports](#)
- [Load \(Attributes > Operating Environment\)](#)

## Flip-Flop (Attributes > Optimization Directives > Cell)

Use Flip-Flop to select the preferred (default) flip-flop type for the selected cells. The default flip-flop type determines which sequential cells from the target library are used to map unmapped flip-flops during design optimization.

When you click the Flip-Flop button in the [Cell \(Attributes > Optimization Directives\)](#) dialog box, the Cell Default Flip-Flop Type dialog box appears. You can select a flip-flop and control whether it is used as the default flip-flop, or as an example of the default flip-flop type, for all unmapped flip-flops in the selected cells.

If you select a single cell, its name appears in the Cell name text box, and the options in the dialog box indicate the current attribute status for the cell. If you select more than one cell, the Cell name text box is blank, and the options are set to default. However, the options that you set apply to all of the selected cells.

Flip-flop types are defined in the technology library. The names of the available flip-flops appear in the Default flip-flop type drop-down list. You can use the Exact flip-flop type option to control whether unmapped flip-flops in the selected cells must be mapped to the selected flip-flop or can be mapped to any flip-flop of the same type.

The following options appear in the Cell Default Flip-Flop Type dialog box:

- Cell name - Displays the name of the current design.
- Default flip-flop type - Sets the preferred flip-flop type (either as the exact default flip-flop or as an example of the default flip-flop type) for unmapped flip-flops in the selected cells. The names of the flip-flops defined in the technology library appear in the list.

- To set the default flip-flop type, select the name of a flip-flop of that type.
- To remove the default flip-flop type from the current design, select <NONE>.

Command cross-reference:

- `set_register_type -flip_flop example_flip_flop`
- `remove_attribute cell_names -default_flip_flop_type`

- Exact flip-flop type - Controls whether the flip-flop specified in the Default flip-flop type drop-down list is the exact default flip-flop for the selected cells. Select this option if you want to map all unmapped flip-flops to the specified flip-flop. Deselect this option if you want to map unmapped flip-flops to any flip-flop of the same type as the specified flip-flop.

Command cross-reference:

- `set_register_type -exact`
- `remove_attribute cell_names -default_flip_flop_type_exact`

## Flip-Flop (Attributes > Optimization Directives > Design)

Use Flip-Flop to select the preferred (default) flip-flop type for the current design. The default flip-flop type determines which sequential cells from the target library are used to map unmapped flip-flops during design optimization.

When you click the Flip-Flop button in the [Design \(Attributes > Optimization Directives\)](#) dialog box, the Default Flip-Flop Type dialog box appears. You can select a flip-flop and control whether it is used as the default flip-flop, or as an example of the default flip-flop type, for all unmapped flip-flops in the current design.

Flip-flop types are defined in the technology library. The names of the available flip-flops appear in the Default flip-flop type drop-down list. You can use the Exact flip-flop type option to control whether unmapped flip-flops in the current design must be mapped to the selected flip-flop or can be mapped to any flip-flop of the same type.

The following options appear in the Default Flip-Flop Type dialog box:

- Current design - Displays the name of the current design.
- Default flip-flop type - Sets the preferred flip-flop type (either as the exact default flip-flop or as an example of the default flip-flop type) for unmapped flip-flops in the current design. The names of the flip-flops defined in the technology library appear in the list.
  - To set the default flip-flop type, select the name of a flip-flop of that type.
  - To remove the default flip-flop type from the current design, select <NONE>.

Command cross-reference:

- `set_register_type -flip_flop example_flip_flop`
- `remove_attribute current_design_name -default_flip_flop_type`
- **Exact flip-flop type** - Controls whether the flip-flop specified in the Default flip-flop type drop-down list is the exact default flip-flop for the current design. Select this option if you want to map all unmapped flip-flops to the specified flip-flop. Deselect this option if you want to map unmapped flip-flops to any flip-flop of the same type as the specified flip-flop.

Command cross-reference:

- `set_register_type -exact`
- `remove_attribute current_design_name -default_flip_flop_type_exact`

## **Input Delay (Attributes > Operating Environment)**

Use Input Delay to set input path delays, relative to a clock edge, for selected input ports, inout ports, or internal pins. Input path delays define the timing requirements for input paths relative to the clock period. Specify delay values in units consistent with the technology library used during optimization.

When you select an input port, inout port, or internal pin and choose Attributes > Operating Environment > Input Delay, the Input Delay dialog box appears. You can specify single maximum and minimum values for both rising and falling edges (the default), or you can deselect the Same rise and fall option and specify separate pairs of maximum and minimum values for the rising and falling edges. You can also select the clock signal, control whether the delays are set relative to the rising edge or the falling edge of the clock, and control whether the delays are added to or overwrite any preexisting delay values.

The appearance of the dialog box depends on the number and type of ports or pins that you select.

- If you select a single port or pin, its name appears in the Name text box, and the options in the dialog box indicate its current input delay status. The name and options change automatically when you select a different port or pin.
- If you select more than one port or pin, their names appear in the Name text box, and the options in the dialog box are set to default. However, the delays that you set apply to all of the selected ports and pins.
- If you select a bus port or pin, the Bus Selector dialog box appears with all the bits selected in the Port bus name or Pin bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of

bits. The Name text box in the Input Delay dialog box changes automatically to display a bus name composed of the selected bits.

- If you select ports and pins for a mixture of buses and individual nets, the placeholder <Multiple selected> appears in the Name text box.

You can use the Report Ports dialog box (choose Design > Report Ports) to see a list of current input delays for ports, and use the Report Design dialog box (choose Design > Report Design) to see a list of current input delays for internal pins. For details, see [Reporting Port Information](#) and [Reporting Design Information](#).

The following options appear in the Input Delay dialog box:

- Name - Displays the names of the selected ports or pins.

Command cross-reference: `set_input_delay port_pin_list`

- Relative to clock - Specifies the clock signal for the relative path delay. The names of the clocks in the current design appear in the list.

- To make the delay relative to a clock signal, select the clock name in the list.

- To make the delay relative to time 0 for combinational designs, select <NONE>. For sequential designs, this delay is considered relative to a new clock with the period determined by considering the sequential cells in the transitive fanout of each port.

Command cross-reference: `set_input_delay -clock clock_name`

- Rising edge - Applies the specified delay values relative to the rising edge of the clock. This option is selected by default.

- Falling edge - Applies the specified delay values relative to the falling edge of the clock. Selecting this option deselects the Rising edge option.

Command cross-reference: `set_input_delay -clock_fall`

- Same rise and fall - Controls whether the path delay values you enter in the Max rise and Min rise text boxes also apply to the maximum and minimum fall times. Deselect this option if you want to enter different minimum and maximum input delay values for the rise time or the fall time.

- Max rise - Specifies the maximum rise time and fall time value (if Same rise and fall option is selected) or the maximum rise time value (if Same rise and fall is not selected) in technology library time units.

Command cross-reference: `set_input_delay -max -rise delay_value`

- Min rise - Specifies the minimum rise time and fall time value (if Same rise and fall option is selected) or the minimum rise time value (if Same rise and fall option is not selected) in technology library time units. This value must be less than the value in the Max rise text box.

Command cross-reference: `set_input_delay -min -rise delay_value`

- Max fall - Specifies the maximum fall time value, in technology library time units, when the Same rise and fall option is not selected.

Command cross-reference: `set_input_delay -max -fall delay_value`

- Min fall - Specifies the minimum fall time value, in technology library time units, when the Same rise and fall option is not selected. This value must be less than the value in the Max fall text box.

Command cross-reference: `set_input_delay -min -fall delay_value`

- Add delay - Controls whether the delay value is added to the input delay (when selected) or overwrites it (when deselected).

Select this option when you want to capture information about multiple paths leading to an input port and the paths are relative to different clocks or clock edges.

Command cross-reference: `set_input_delay -add_delay`

## See Also

- [Setting Input Timing Requirements](#)
- [Output Delay \(Attributes > Operating Environment\)](#)

## Input Port (Attributes > Optimization Directives)

Use Input Port to set port attributes for selected input or inout ports.

When you select an input port or input port and choose Attributes > Optimization Directives > Input Port, the Input Port Attributes dialog box appears. You can set the maximum fanout load and maximum transition time values for the port and control whether it is driven by logic 0 or logic 1.

### Note:

You can also open this dialog box by selecting an input port in a schematic view, right-clicking, and choosing Edit Attributes.

The appearance of the dialog box depends on the number and type of ports that you select.

- If you select a single port, its name appears in the Port name text box, and the options in the dialog box indicate its current attribute status. The name and options change automatically when you select a different port.
- If you select more than one port, their names appear in the Port name text box, and the options in the dialog box are set to default. However, the attributes that you set apply to all of the selected ports.
- If you select a bus port, the Bus Selector dialog box appears with all the bits selected in the Port bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Port name text box in the Input Port Attributes dialog box changes automatically to display a bus name composed of the selected bits.
- If you select ports for a mixture of buses and individual nets, the placeholder <Multiple selected> appears in the Port name text box.

The following options appear in the Input Port Attributes dialog box:

- Port name - Displays the names of the selected input or inout ports.
- Maximum fanout - Specifies the value, in technology library load units, of the maximum fanout load that can be driven by the selected ports.

Command cross-reference: `set_max_fanout number`

- Maximum transition - Specifies the value, in technology library time units, of the maximum transition time for each signal arriving at the selected ports.

Command cross-reference: `set_max_transition number`

- Maximum capacitance -Specifies the value, in technology library time units, of the maximum capacitance for each net attached to the selected ports.

Command cross-reference: `set_max_capacitance number`

- Port Pad Attributes - Opens the Port Pad Attributes dialog box, which you can use to define the pad cell type, pad cell characteristics, slew rate, and pad current and voltage levels for the selected ports.

- Port options

- Disable timing - Controls whether Design Vision tool sets (when selected) or removes (when deselected) the `disable_timing` attribute on the selected ports. This attribute disables timing arcs in the current design.

Command cross-references: `set_disable_timing`  
`remove_attributeport_names disable_timing`

- Don't touch network - Controls whether Design Vision tool sets (when selected) or removes (when deselected) the `dont_touch_network` attribute on the selected

ports. This attribute prevents cells and nets in the transitive fanout of the ports from being modified or replaced during optimization.

Command cross-reference:

- `set_dont_touch_network`
- `remove_attribute port_names dont_touch_network`

- Connected to - Determines whether the selected ports are to be driven by logic 0, logic 1, or neither. The default is Neither.
  - Logic 0 - Controls whether Design Vision tool assigns the `driven_by_logic_zero` attribute to the ports.

Command cross-references: `set_logic_zero`

- Logic 1 - Controls whether Design Vision tool assigns the `driven_by_logic_one` attribute to the ports.

Command cross-references: `set_logic_one`

- [Set Opposite \(Attributes > Optimization Directives > Input Port\)](#) - Opens the Port Opposite dialog box, in which you can set another input port as a logical opposite of the selected port.
- [Set Equal \(Attributes > Optimization Directives > Input Port\)](#) - Opens the Port Equal dialog box, in which you can set another input port as a logical equivalent of the selected port.

## See Also

- [Setting Transition Time Constraints on Nets](#)
- [Setting Fanout Load Constraints on Nets](#)
- [Setting Capacitance Constraints on Nets](#)
- [Output Port \(Attributes > Optimization Directives\)](#)
- [Design Constraints \(Attributes > Optimization Constraints\)](#)

## Latch (Attributes > Optimization Directives > Cell)

Use Latch to select the preferred (default) latch type for the selected cells. The default latch type determines which sequential cells from the target library are used to map unmapped latches during design optimization.

When you click the Latch button in the [Cell \(Attributes > Optimization Directives\)](#) dialog box, the Cell Default Latch Type dialog box appears. You can select a latch and control

whether it is used as the default latch, or as an example of the default latch type, for all unmapped latches in the selected cells.

If you select a single cell, its name appears in the Cell name text box, and the options in the dialog box indicate the current attribute status for the cell. If you select more than one cell, the Cell name text box is blank, and the options are set to default. However, the options that you set apply to all of the selected cells.

Latch types are defined in the technology library, and the names of the available latches appear in the Default latch type drop-down list. You can use the Exact latch type option to control whether unmapped latches in the selected cells must be mapped to the selected latch or can be mapped to any latch of the same type.

The following options appear in the Cell Default Latch Type dialog box:

- Cell name - Displays the name of the selected cell.
- Default latch type - Sets the preferred latch type (either as the exact default latch or as an example of the default latch type) for unmapped latches in the selected cells. The names of the latches defined in the technology library appear in the list.
  - To set the default latch type, select the name of a latch of that type.
  - To remove the default latch type from the current design, select <NONE>.

Command cross-reference:

- `set_register_type -latch example_flip_flop`
- `remove_attribute cell_names -default_latch_type`
- Exact latch type - Controls whether the latch specified in the Default latch type drop-down list is the exact default latch for the selected cells. Select this option if you want to map all unmapped latches to the specified latch. Deselect this option if you want to map unmapped latches to any latch of the same type as the specified latch.

Command cross-reference:

- `set_register_type -exact`
- `remove_attribute current_design_name -default_latch_type_exact`

## **Latch (Attributes > Optimization Directives > Design)**

Use Latch to select the preferred (default) latch type for the current design. The default latch type determines which sequential cells from the target library are used to map unmapped latches during design optimization.

When you click the Latch button in the [Design \(Attributes > Optimization Directives\)](#) dialog box, the Default Latch Type dialog box appears. You can select a latch and control

whether it is used as the default latch, or as an example of the default latch type, for all unmapped latches in the current design.

Latch types are defined in the technology library, and the names of the available latches appear in the Default latch type drop-down list. You can use the Exact latch type option to control whether unmapped latches in the current design must be mapped to the selected latch or can be mapped to any latch of the same type.

The following options appear in the Default Latch Type dialog box:

- Current design - Displays the name of the current design.
- Default latch type - Sets the preferred latch type (either as the exact default latch or as an example of the default latch type) for unmapped latches in the current design. The names of the latches defined in the technology library appear in the list.
  - To set the default latch type, select the name of a latch of that type.
  - To remove the default latch type from the current design, select <NONE>.

Command cross-references:

- `set_register_type -latchexample_flip_flop`
- `remove_attribute current_design_name -default_latch_type`
- Exact latch type - Controls whether the latch specified in the Default latch type drop-down list is the exact default latch for the current design. Select this option if you want to map all unmapped latches to the specified latch. Deselect this option if you want to map unmapped latches to any latch of the same type as the specified latch.

Command cross-reference:

- `set_register_type -exact`
- `remove_attribute current_design_name -default_latch_type_exact`

## Load (Attributes > Operating Environment)

Use Load to set the capacitive load for selected ports or nets and the maximum number of fanout loads for selected output ports. Capacitive load values help the compiler model input delays on input pads and selects the appropriate cell drive strengths of output pads. Expected fanout loads help the compiler to model the external fanout effects.

When you select a port or a net and choose Attributes > Operating Environment > Load, the Load dialog box appears. You can enter a capacitive load value for an input port or a net, or enter a capacitive load value and a maximum number of fanouts value for an output port. Specify the capacitive load value in technology library load units.

The appearance of the dialog box depends on the number and type of ports or pins that you select.

- If you select a single port or net, its object type (port or net) appears in the Type drop-down list, its name appears in the Name drop-down list, and the options in the dialog box indicate its current load status. The type, name, and options change automatically when you select a different port or net.
- If you select multiple objects of the same type (port or net), their object type appears in the Type drop-down list, their names appear in the Name drop-down list, and the options in the dialog box are set to default. By default, all the names in the Name drop-down list are selected. If you select one of the names in the Name drop-down list, the options in the dialog box change to display the current load status for that object. You can select one or more names in the list and set load options for just those objects.
- If you select a bus or a bus port, the Bus Selector dialog box appears with all the bits selected in the Net bus name or Port bus name list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Name drop-down list in the Load dialog box changes automatically to display each of the selected bits.
- If you select a mixture of ports and nets, the placeholder <All selected> appears in the Type list, and the Name drop-down list is blank. Select a type option (net or port) in the Type drop-down list to display the names of the selected nets or ports in the Name drop-down list.

The following options appear in the Load dialog box:

- Type - Controls which type of objects are listed in the Name drop-down list when both nets and ports are selected.
- Port name - Displays the names of the selected ports, the names of the selected nets, or <Multiple selected> if both ports and nets are selected.

Command cross-references:

- `set_load objects_list`
- `set_fanout_load port_list`
- Capacitive load - Sets the maximum load that can be incurred by the selected ports or nets. The default is 0.0.

Command cross-reference: `set_load capacitance_value`

- Fanout load - Sets the expected fanout load for the selected output ports. The compiler adds the fanout load value to all other loads on the pin driving each port and tries to make the total fanout load less than the pin's maximum fanout load.

Command cross-reference: `set_fanout_load fanout_load_value`

### See Also

- [Setting Capacitive Loads on Input Ports](#)
- [Setting Capacitive and Fanout Loads on Output Ports](#)
- [Drive Strength \(Attributes > Operating Environment\)](#)

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## Net (Attributes > Optimization Directives)

Use Net to set instance-specific net attributes throughout the design hierarchy.

When you select a net and choose Attributes > Optimization Directives > Net, the Net Attributes dialog box appears. You can set or remove the `dont_touch` attribute on the nets.

**Note:**

You can also open the Net Attributes dialog box by selecting a net in a schematic view, right-clicking, and choosing Edit Attributes.

The appearance of the dialog box depends on the number and type of pins that you select.

- If you select a single net, its name appears in the Net name text box, and the options in the dialog box indicate its current attribute status. The name and options change automatically when you select a different net.
- If you select a bus, the Bus Selector dialog box appears with all the bits selected in the Bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Net name text box in the Net Attributes dialog box changes automatically to display a bus name composed of the selected bits.
- If you select more than one net or bus, the placeholder <Multiple selected> appears in the Net name text box, and the options in the dialog box are set to default. However, the attributes that you set apply to all of the selected nets and buses.

**Note:**

When some of the selected nets or buses is assigned the `dont_touch` attribute and others have not, the Don't touch option is deselected. Any change you make to this option (either selecting it or selecting and then deselecting it) applies to all the selected nets and buses.

The following options appear in the Net Attributes dialog box:

- **Net name** - Displays the name of the selected net if only one net is selected, or displays <Multiple selected> option if multiple nets are selected.
- **Don't touch** - Controls whether Design Vision tool sets (when selected) or removes (when deselected) the `dont_touch` attribute on the selected nets. This attribute prevents modifications to the nets during design optimization.

Command cross-references:

- `set_dont_touch`
- `remove_attribute net_names dont_touch`

## Operating Conditions (Attributes > Operating Environment)

Use Operating Conditions to select the operating conditions you want to use for timing delay analysis. Operating conditions define the environmental characteristics of a design and are always set on the top design in the hierarchy.

When you choose Attributes > Operating Environment > Operating Conditions, the Operating Conditions dialog box appears. Operating condition characteristics are defined in a technology library. You can select the library and a set of operating conditions defined in that library. Each set of operating conditions is identified by a name and consists of a process number, a temperature value, a voltage value, and an interconnect model.

By default, you select a single set of conditions for both maximum and minimum delay analysis. Select Min/max case option if you want to select separate sets of maximum and minimum operating conditions.

**Note:**

If you do not select operating conditions for a design, the compiler searches the first link library for default operating conditions. If the defaults are not found, the compiler does not use operating conditions for timing delay analysis.

You can use Reports > Design Information > Design to see the current operating conditions for the design. To see what operating conditions are defined in a specific library, use the `report_library` command.

The following options appear in the Operating Conditions dialog box:

- **Current design** - Displays the name of the top design.
- **Analysis condition**

- Single - Applies the set of operating conditions selected under Maximum operating condition to both maximum and minimum delay analysis.
- Min/max case - Applies the set of operating conditions selected under Maximum operating condition to maximum delay analysis and the set of operating conditions selected under Minimum operating condition to minimum delay analysis.
- Maximum operating condition - Select the operating conditions, either for maximum and minimum delay analysis (if Single is selected under Analysis condition) or for maximum delay analysis (if Min/max case is selected under Analysis condition), and the library in which they are defined.
  - Library - Displays the name of the library or collection of libraries that contains the operating condition definitions. To change libraries, select a different library name in the drop-down list.

**Command cross-references:**

- `set_operating_conditions -library lib_name`
- `set_operating_conditions -max_library lib_name`
- Condition - Displays the name of the current set of operating conditions to be used during design timing or optimization. To change the operating conditions, select a different condition name in the drop-down list.

**Command cross-references:**

- `set_operating_conditions condition`
- `set_operating_conditions -max condition`
- Minimum operating condition - Selects the operating conditions for minimum delay analysis and the library in which they are defined. These options are available only when Min/max case option is selected under Analysis condition.
  - Library - Displays the name of the library or collection of libraries that contains the operating condition definitions. To change libraries, select a different library name in the drop-down list.

**Command cross-reference:** `set_operating_conditions -min_library lib_name`

- Condition - Displays the name of the current set of operating conditions to be used during design timing or optimization. To change the operating conditions, select a different condition name in the drop-down list.

**Command cross-reference:** `set_operating_conditions -min condition`

### See Also

- [Selecting Operating Conditions](#)
- [Wire Load \(Attributes > Operating Environment\)](#)
- [Timing Range \(Attributes > Operating Environment\)](#)

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## Output Delay (Attributes > Operating Environment)

Use Output Delay to set output path delays, relative to a clock edge, for selected output ports, inout ports, or internal pins. Specify delay values in units consistent with the technology library used during optimization.

When you select an output port, inout port, or internal pin and choose Attributes > Operating Environment > Output Delay, the Output Delay dialog box appears. You can specify single maximum and minimum values for both rising and falling edges (the default) or you can deselect the Same rise and fall option and specify separate pairs of maximum and minimum values for the rising and falling edges. You can also select the clock signal, control whether the delays are set relative to the rising edge or the falling edge of the clock, and control whether the delays are added to or overwrite any preexisting delay values.

The appearance of the dialog box depends on the number and type of ports or pins that you select.

- If you select a single port or pin, its name appears in the Name text box, and the options in the dialog box indicate its current input delay status. The name and options change automatically when you select a different port or pin.
- If you select more than one port or pin, their names appear in the Name text box, and the options in the dialog box are set to default. However, the delays that you set apply to all of the selected ports and pins.
- If you select a bus port or pin, the Bus Selector dialog box appears with all the bits selected in the Port bus name or Pin bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Name text box in the Output Delay dialog box changes automatically to display a bus name composed of the selected bits.
- If you select ports and pins for a mixture of buses and individual nets, the placeholder <Multiple selected> appears in the Name text box.

You can use the Report Ports dialog box (choose Design > Report Ports) to see a list of current input delays for ports, and use the Report Design dialog box (choose Design > Report Design) to see a list of current input delays for internal pins. For details, see [Reporting Port Information](#) and [Reporting Design Information](#).

The following options appear in the Output Delay dialog box:

- **Name** - Displays the names of the selected ports or pins.

**Command cross-reference:** `set_output_delay port_pin_list`

- **Relative to clock** - Specifies the clock signal for the relative path delay. The names of the clocks in the current design appear in the list.

◦ To make the delay relative to a clock signal, select the clock name in the list.

◦ To make the delay relative to time 0 for combinational designs, select <NONE>. For sequential designs, this delay is considered relative to a new clock with the period determined by considering the sequential cells in the transitive fanout of each port.

**Command cross-reference:** `set_output_delay -clock clock_name`

- **Rising edge** - Applies the specified delay values relative to the rising edge of the selected clock. This option is selected by default.

- **Falling edge** - Applies the specified delay values relative to the falling edge of the selected clock.

**Command cross-reference:** `set_output_delay -clock_fall`

- **Max rise** - Specifies the maximum rise and fall value (if Same rise and fall is selected) or the maximum rise time value (if Same rise and fall is not selected) in technology library time units.

**Command cross-reference:** `set_output_delay -max -rise delay_value`

- **Min rise** - Specifies the minimum rise and fall (if Same rise and fall option is selected) or the minimum rise time value (if Same rise and fall option is not selected) in technology library time units. This value must be less than the value in the Max rise text box.

**Command cross-reference:** `set_output_delay -min -rise delay_value`

- **Max fall** - Specifies the maximum fall time value, in technology library time units, when the Same rise and fall option is not selected.

**Command cross-reference:** `set_output_delay -max -fall delay_value`

- **Min fall** - Specifies the minimum fall time value, in technology library time units, when the Same rise and fall option is not selected. This value must be less than the value in the Max fall text box.

**Command cross-reference:** `set_output_delay -min -fall delay_value`

- **Same rise and fall** - Controls whether the path delay values entered in the Max rise and Min rise text boxes also apply to the maximum and minimum fall times. Deselect

this option if you want to enter different minimum and maximum output delay values for the rise time or the fall time.

- Add delay - Controls whether the delay value is added to the output delay (when selected) or overwrites it (when deselected).

Select this option when you want to capture information about multiple paths leading to an output port and the paths are relative to different clocks or clock edges.

Command cross-reference: `set_output_delay -add_delay`

### See Also

- [Setting Output Timing Requirements](#)
- [Input Port \(Attributes > Optimization Directives\)](#)

## Output Port (Attributes > Optimization Directives)

Use Output Port to set port attributes for selected output or inout ports.

When you select an output port or inout port and choose Attributes > Optimization Directives > Output Port, the Output Port Attributes dialog box appears.

### Note:

You can also open this dialog box by selecting an output port in a schematic view, right-clicking, and choosing Edit Attributes.

The appearance of the dialog box depends on the number and type of ports that you select.

- If you select a single port, its name appears in the Port name text box, and the options in the dialog box indicate its current attribute status. The name and options change automatically when you select a different port.
- If you select more than one port, their names appear in the Port name text box, and the options in the dialog box are set to default. However, the attributes that you set apply to all of the selected ports.
- If you select a bus port, the Bus Selector dialog box appears with all the bits selected in the Port bus name drop-down list. You can click in the list to select a single bit, or use Shift-click and Control-click to select any combination of bits. The Port name text box in the Output Port Attributes dialog box changes automatically to display a bus name composed of the selected bits.
- If you select ports for a mixture of buses and individual nets, the placeholder <Multiple selected> appears in the Port name text box.

The following options appear in the Output Port Attributes dialog box:

- `Port name` - Displays the names of the selected output or inout ports.
- `Maximum transition` - Specifies the value, in technology library time units, of the maximum transition time for the signal arriving at the selected ports.

**Command cross-reference:** `set_max_transition number`

- `Unconnected` - Controls whether Design Vision tool sets (when selected) or removes (when deselected) the `output_not_used` attribute on the selected output ports. You can use this attribute to create smaller designs by eliminating logic that drives unconnected output ports. After the design is optimized, the unconnected output ports are not driven by anything within the design.

**Command cross-references:**

- `set_unconnected`
- `remove_attribute port_names output_not_used`

## See Also

- [Setting Transition Time Constraints on Nets](#)
- [Input Port \(Attributes > Optimization Directives\)](#)
- [Design Constraints \(Attributes > Optimization Constraints\)](#)

## Pin (Attributes > Optimization Directives)

Use Pin to set instance-specific pin attributes throughout the design hierarchy.

When you select a pin and choose Attributes > Optimization Directives > Pin, the Pin Attributes dialog box appears. You can specify the maximum amount of time borrowing permitted for a pin and enable or disable timing arcs approaching a pin.

### Note:

You can also open Pin Attributes dialog box by selecting a pin in a schematic view, right-clicking, and then choosing Edit Attributes.

The appearance of the dialog box depends on the number and type of pins that you select.

- If you select a single pin, its name appears in the Pin name text box, and the options in the dialog box indicate its current attribute status. The name and options change automatically when you select a different pin.
- If you select a bus pin, the Bus Selector dialog box appears with all the bits selected in the Pin bus name drop-down list. You can click in the list to select a single bit, or use

Shift-click and Control-click to select any combination of bits. The Pin name text box in the Pin Attributes dialog box changes automatically to display a bus name composed of the selected bits.

- If you select more than one pin, the placeholder <Multiple selected> appears in the Pin name text box, and the options in the dialog box are set to default. However, the attributes that you set apply to all of the selected pins.

The following options appear in the Pin Attributes dialog box:

- `Pin name` - Displays the name of the selected pin, if only one pin is selected, or displays <Multiple selected> option if multiple pins are selected.
- `Max time borrow` - Specifies the maximum amount of time borrowing permitted for data or clock (enable) pins on level-sensitive latches.

Command cross-reference: `set_max_time_borrownumber`

- `Disable timing` - Controls whether Design Vision tool sets (when selected) or removes (when deselected) the `disable_timing` attribute on the selected pins. This attribute disables timing arcs in the current design.

Command cross-references:

- `set_disable_timing`
- `remove_attribute pin_names disable_timing`

## Selection List (Select Menu)

The Selection List dialog box displays information about the collection of selected objects in the current design. You can add objects to the collection by selecting them, or remove objects from the collection by deselecting them. When no objects are selected, the selection list is empty.

- When you select objects in a view or by using commands on the Select menu, their names automatically appear in the selection list.
- When you deselect objects in a view or by using commands on the Select menu, their names automatically disappear in the selection list.
- When you deselect all objects (no objects are selected), the selection list is empty.

The Selection List dialog box consists of a table that shows information about the selected objects. If multiple types of objects are selected, the table shows the object name, object type, and full name for each selected object. If all the selected objects are of the same type, the table shows information specific to that object type.

By default, the Selection List dialog box displays values for the attributes in the Basic attribute group.

- For selected cells, the table shows the cell instance name, the cell reference name, the hierarchical path name from the top-level design to the cell, and the status of the `dont_touch`, `is_mapped`, and `is_selected` attributes.
- For selected nets, the table shows the net name, the full name (from the top-level design to the net), and the status of the `dont_touch` attribute.
- For selected ports and pins, the table shows the port or pin name, the full name (from the top-level design to the port or pin), and the pin direction.
- For selected timing paths, the table shows the path name, the full path name, the slack value, the startpoint and endpoint names, the path group name, the design area, the design directory path, the DesignWare implementation, and the status of the `structure`, `flatten`, and `dont_touch` attributes.
- For selected designs, the table shows the design name, the object type (netlist), and the full design name.

You can control which attributes appear by selecting an attribute group in the list at the bottom-left corner of the dialog box. You can modify the contents of some predefined attribute groups and create or modify custom attribute groups by using the Attribute Group Manager dialog box. For more information, see [Creating and Editing Attribute Groups](#).

You can edit the collection in the table by selecting one or more of the object names and either removing them or removing all other object names.

To select some objects and remove all others from the collection,

- Select the names of the objects you want to retain in the collection and click the Select button.

To deselect objects and remove them from the collection,

- Select the names of the objects you want to remove and click the Deselect button.

## See Also

- [Viewing the Selection List](#)

---

## Set Equal (Attributes > Optimization Directives > Input Port)

Use Set Equal to set two input ports in the current design as logical equivalents. Setting ports as logical equivalents improves optimization quality by eliminating redundant ports.

When you click the Set Equal button in the [Input Port \(Attributes > Optimization Directives\)](#) dialog box, the Port Equal dialog box appears. Enter the name of the input port that you want to set as logically equivalent to the selected input port.

The following options appear in the Port Equal dialog box:

- Port name 1 - Displays the name of the selected input port.

Command cross-reference: `set_equal port_1`

- Port name 2 - Specifies the name of the port that you want to set as a logical equivalent of the port named in Port 1.

Command cross-reference: `set_equal port_2`

---

## **Set Opposite (Attributes > Optimization Directives > Input Port)**

Use Set Opposite to set two input ports in the current design as logical opposites. Setting ports as logical opposites improves optimization quality by eliminating redundant ports.

When you click Set Opposite button in the [Input Port \(Attributes > Optimization Directives\)](#) dialog box the Port Opposite dialog box appears. Enter the name of the input port that you want to set as logically opposite to the selected input port.

The following options appear in the Port Opposite dialog box:

- Port name 1 - Displays the name of the selected input port.

Command cross-reference: `set_opposite port_1`

- Port name 2 - Specifies the name of the port that you want to set as a logical opposite of the port named in Port 1.

Command cross-reference: `set_opposite port_2`

---

## **Specify Clock (Attributes Menu)**

Use Specify Clock to define or change the period and waveform for a clock in the current design. You can also set `dont_touch` and `fix_hold` attributes on the clock. You can create a clock on an input port or pin by specifying its name and defining its waveform and period. You can also define virtual clocks that are not associated with a port or pin.

A clock period constrains all register-to-register paths in a synchronous design. If you define multiple clocks, the minimum base period for the design is the least common multiple of all the clock periods. You can create virtual clocks for modeling clock signals in blocks that do not contain system clocks. By creating a virtual clock for a block, you can represent delays that are relative to a clock outside the block.

When you choose Attributes > Specify Clock, the Specify Clock dialog box appears. If you have selected a pin, net, or input port, its name appears in the Port name text box, and the name of the associated clock appears in the Clock name text box. If you select more than one object (port, pin, or net), the Clock name text box displays the clock name for the last object selected.

To create a virtual clock, choose Attributes > Specify Clock without selecting an object. The Port name text box appears blank, and you can enter a name for the virtual clock in the Clock name text box.

You define the clock period and waveform by entering a period value and the times for each rising and falling edge within a clock period.

The following options appear in the Specify Clock dialog box:

- **Clock name** - Specifies the name of the clock you want to create or change.  
If you selected an object (port, pin, or net) on a clock network, the name of the clock associated with the selected object appears in this box. If you did not select an object, you must enter a name in this box. This creates a virtual clock that is not associated with a port or pin.

You can edit the name in the Clock name text box to create a new clock. If you specify a new clock name for a port or pin that already has a clock, the new clock replaces the existing one.

Command cross-reference: `create_clock -name clock_name`

- **Port name** - Displays the name of the selected object (port, pin, or net) on the clock network.

Command cross-reference: `create_clock port_pin_name`

- **Remove clock** - Removes the clock specified in the Clock name text box from the current design. If the clock is the only member of a path group, the path group is also removed. You can view a clocks report (choose Report > Clocks) to see a list of clock sources in the current design.

Command cross-reference: `remove_clock clock_name`

- **Clock creation** - Defines the clock period and waveform. To specify the clock period, enter a value in the Period text box. You can define the waveform by entering one or more edge pairs of rising and falling values in the table below the Period text box. Each rising or falling value represents the transition time for a clock edge.

The waveform must consist of an even number of monotonically increasing time values over an entire clock period. The compiler assumes that these time values are alternating rise and fall times. You must enter at least one pair of rising and falling edge values.

You can use the following options to add or remove edge pairs or to invert the waveform (by reversing the order of edge pairs in the table).

- Period - Specifies the clock period in technology library time units.  
Command cross-reference: `create_clock -period`
- Rising - Specifies a rising transition time in technology library time units.  
Command cross-reference: `create_clock -waveform edge_list`
- Falling - Specifies a falling transition time in technology library time units.  
Command cross-reference: `create_clock -waveform edge_list`
- Add edge pair - Adds a new Rising row and a new Falling row to the table.
- Remove edge pair - Removes the selected pair of Rising and Falling rows from the table. Shift-click the rows to select them. You must select adjacent rows.
- Invert wave form - Reverses the order of edge pair (Rising and Falling) rows in the table.
- Don't touch network - Controls whether the clock fanout network is preserved during design optimization.  
Command cross-reference: `set_dont_touch_network`
- Fix hold - Controls whether the compiler creates hold constraints for the clocks in the current design during design optimization.  
Command cross-reference: `set_fix_hold`

### See Also

- [Creating Clocks](#)
- [Fixing Hold Time Violations](#)

## Timing Constraints (Attributes > Optimization Constraints)

Use Timing Constraints to set maximum and minimum delay constraints for one or more timing paths in the current design. These constraints provide point-to-point timing exceptions for combinational circuits and override the default single-cycle timing relationships for asynchronous paths or paths that do not follow the default single-cycle behavior.

When you choose Attributes > Optimization Constraints > Timing Constraints, the Timing Constraints dialog box appears. Use this dialog box to specify maximum and minimum

path delays for one or more paths. You can specify single rising and falling values for both the maximum and minimum delay times (the default), or you can deselect the Same rise and fall option and specify separate pairs of rising and falling values for the maximum delay and the minimum delay. You can also specify a path group to which you want to add the paths.

You specify a path by identifying its startpoint, endpoint, or both.

- Valid startpoints are the primary input ports of a design and the clock pins of sequential cells.
- Valid endpoints are the primary output ports of a design and the data pins of sequential cells.

Only paths that begin at valid startpoints or end at valid endpoints are constrained by the rise and fall delays you specify. For a clock, all startpoints or endpoints related to the clock are affected. For a cell, only one path startpoint or endpoint on the cell is affected.

When you select an object (pin, port, clock, or cell) that represents a valid startpoint or endpoint, its name appears in either the From list (startpoints) or the To list (endpoints) at the top of the dialog box. You can select names in these lists and use the arrow buttons to move them from one list to the other, or use the X button to remove them from the dialog box.

- To move an object name from the From list to the To list, select the name and click the down arrow button.
- To move an object name from the To list to the From list, select the name and click the up arrow button.
- To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)

The delay values you specify apply to all paths from the startpoints in the From list to the endpoints in the To list. If you do not select any startpoints (the From list is blank), all paths that end at the endpoints in the To list are constrained. If you do not select any endpoints (the To list is blank), all paths that start at the startpoints in the From list are constrained.

To meet path delay constraints, the path length for any path must be less than the maximum delay values and greater than the minimum delay values that you specify. The individual delays are automatically derived from clock waveforms and from input and output port delays.

The following options appear in the Timing Constraints dialog box:

- **From** - Displays the names of the valid startpoints (selected ports, pins, clocks, or cells) for timing paths you want to constrain. This list should not contain the names of output ports or hierarchical cells.

Command cross-reference: `set_max_delay -from from_list`

- **To** - Displays the names of the endpoints (selected ports, pins, clocks, and cells) for the timing paths you want to constrain. This list should not contain the names of input ports or hierarchical cells.

Command cross-reference: `set_max_delay -to to_list`

- **Delays**

- **Same rise and fall** - Controls whether the maximum and minimum values entered in the Max rise and Min rise text boxes also apply to the maximum and minimum fall times. Deselect this option if you want to enter different rise and fall time values for the minimum and maximum path delays.

- **Max rise** - Specifies the maximum rise time value for the endpoints of the timing paths.

Command cross-reference: `set_max_delay number -rise`

- **Min rise** - Specifies the minimum rise time value for the endpoints of the timing paths.

Command cross-reference: `set_min_delay number -rise`

- **Max fall** - Specifies the maximum fall time value for the endpoints of the timing paths.

Command cross-reference: `set_max_delay number -fall`

- **Min fall** - Specifies the minimum fall time value for the endpoints of the timing paths.

Command cross-reference: `set_min_delay number -fall`

- **Group name** - Specifies the name of the path group to which you want to add the timing paths. If the group does not exist, Design Vision tool creates the group. If you do not specify a group name, the path's group is not changed.

Command cross-references:

- `set_max_delay -group_path group_name`
- `set_min_delay -group_path group_name`

- **Reset path** - Controls whether Design Vision tool resets the timing paths to the default single-cycle timing behavior.

When this option is selected, Design Vision tool resets the path timing by removing point-to-point exception attributes on the paths. If you enter values for one or more of the delay options, Design Vision tool removes only the exception information for those types of delays. By default, when you do not enter any delay values, all exception information is removed.

Command cross-references:

- `set_max_delay -reset_path`
- `set_min_delay -reset_path`
- `reset_path`

### See Also

- [Setting Combinational Path Delay Requirements](#)
- [Setting Maximum and Minimum Delay Requirement](#)
- [Creating Path Groups](#)
- [Timing Paths \(Attributes > Optimization Directives\)](#)

## Timing Paths (Attributes > Optimization Directives)

Use Timing Paths to define timing exceptions to constrain or disable asynchronous paths or paths that do not follow the default single-cycle behavior. Timing exceptions are timing relationships that override the single-cycle setup and hold relationship for one or more paths.

When you choose Attributes > Optimization Directives > Timing Paths, the Timing Paths dialog box appears. Use this dialog box to set single-cycle, multicycle, or false timing path setup and hold timing exceptions for one or more paths.

You specify a path by identifying its startpoint, endpoint, or both.

- Valid startpoints are the primary input ports of a design and the clock pins of sequential cells.
- Valid endpoints are the primary output ports of a design and the data pins of sequential cells.

Only paths that begin at valid startpoints or end at valid endpoints are affected by the timing exceptions you specify. For a clock, all startpoints or endpoints related to the clock are affected. For a cell, only one path startpoint or endpoint on the cell is affected.

When you select an object (pin, port, clock, or cell) that represents a valid startpoint or endpoint, its name appears in either the From list (startpoints) or the To list (endpoints) at the top of the dialog box. You can select names in these lists and use the arrow buttons to move them from one list to the other, or use the X button to remove them from the dialog box.

- To move an object name from the From list to the To list, select the name and click the down arrow button.
- To move an object name from the To list to the From list, select the name and click the up arrow button.
- To remove an object name from the To list, select the name and click the X button. (If no object name is selected, this button removes the name at the bottom of the list.)

If you do not select any startpoints (the From list is blank), all paths that end at the endpoints in the To list are constrained. If you do not select any endpoints (the To list is blank), all paths that start at the startpoints in the From list are constrained.

The Setup and Hold options you select apply to all paths from the startpoints in the From list to the endpoints in the To list. If you do not select any startpoints (the From list is blank), the Setup and Hold options apply to all paths that end at the endpoints in the To list. If you do not select any endpoints (the To list is blank), the Setup and Hold options apply to all paths that start at the startpoints in the From list.

The following options appear in the Timing Paths dialog box:

- From - Displays the names of the startpoints (selected ports, pins, clocks, and cells) for the timing paths. This list should not contain the names of output ports or hierarchical cells.

#### Command cross-references:

- `set_false_path -from source_list`
- `reset_path -from source_list`
- `set_multicycle_path -from source_list`

- To - Displays the names of the endpoints (selected ports, pins, clocks, and cells) for the timing paths. This list should not contain the names of input ports or hierarchical cells.

#### Command cross-references:

- `set_false_path -to destination_list`
- `reset_path -to destination_list`
- `set_multicycle_path -to destination_list`

- **Setup** - Lets you select the setup (maximum delay) relationship for timing checks on the paths identified by the startpoints and endpoints in the From and To lists. The False path option is selected by default. You can select any one of the following option:

- **False path** - Removes maximum rise and fall delay constraints. Select this option to disable setup constraints on paths that you know do not affect circuit operation.

Command cross-reference: `set_false_path -setup`

- **Single cycle path** - Sets maximum rise and fall delay checking to single-cycle timing. Select this option to reset delay checking for paths previously assigned a multicycle path, false path, or maximum delay attribute.

Command cross-reference: `reset_path -setup`

- **Multi cycle path** - Sets the maximum rise and fall delay checking to multicycle timing. Select this option for timing paths that can satisfy multiple timing constraints based on the number of cycles you specify in the Cycles box.

Command cross-reference: `set_multicycle_path -setup`

- **Cycles** - Specifies the path multiplier for multicycle timing paths. This value is the number of cycles that a datapath must have for setup, relative to the startpoint or endpoint clock, before data is required at the endpoint. This option is available only when the Multi cycle path option is selected.

Command cross-reference: `set_multicycle_path path_multiplier`

- **Hold** - Lets you select the hold (minimum delay) relationship for timing checks on the paths identified by the startpoints and endpoints in the From and To lists. The False path option is selected by default. You can select one of the following:

- **False path** - Removes minimum rise and fall delay constraints. Select this option to disable hold constraints on paths that you know do not affect circuit operation.

Command cross-reference: `set_false_path -hold`

- **Single cycle path** - Sets minimum rise and fall delay checking to single-cycle timing. Select this option to reset delay checking for paths previously assigned a multicycle path, false path, or minimum delay attribute.

Command cross-reference: `reset_path -hold`

- **Multi cycle path** - Sets the minimum rise and fall delay checking to multicycle timing. Select this option for timing paths that can satisfy multiple timing constraints based on the number of cycles you specify in the Cycles box.

Command cross-reference: `set_multicycle_path -hold`

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- **Cycles** - Specifies the path multiplier for multicycle timing paths. This value is the number of cycles that a datapath must have for hold, relative to the startpoint or endpoint clock, before data is required at the endpoint. This option is available only when the Multi cycle path option is selected.

Command cross-reference: `set_multicycle_path path_multiplier`

### See Also

- [Setting False Paths](#)
- [Setting Multicycle Paths](#)
- [Restoring Single-Cycle Timing](#)
- [Timing Constraints \(Attributes > Optimization Constraints\)](#)

## Timing Range (Attributes > Operating Environment)

Use Timing Range to set or remove timing range scaling factors for modeling operating condition variations in the current design. Timing ranges are scaling factors used to scale timing path totals. The slowest factor is the largest value of any specified timing range, and the fastest factor is the smallest value.

Changing timing ranges affects the path delays in the timing and constraints reports and also affects the delay cost computation during design optimization. Maximum path delays are scaled by the slowest factor, and minimum delays are scaled by the fastest factor. You can use the `report_lib` command with the `-timing_arcs` option to see which timing ranges are defined in your technology library.

When you choose Attributes > Operating Environment > Timing Range, the Timing Ranges dialog box appears. You can use the timing range values displayed in the Timing ranges text boxes or select a different set of values from the list of available timing ranges.

The following options appear in the Timing Ranges dialog box:

- Current design - Displays the name of the current design.
- Timing ranges - Displays the current timing range scaling factors. Available timing ranges appear in the list below the Timing ranges text boxes. To change timing ranges, select a different set of scaling factors from the list.

Select <NONE> if you want to clear the Timing ranges text box and remove the assigned timing range scaling factors from the current design.

Command cross-reference: `set_timing_ranges timing_ranges -lib library_name`

## See Also

- [Selecting Timing Ranges](#)
- [Operating Conditions \(Attributes > Operating Environment\)](#)
- [Wire Load \(Attributes > Operating Environment\)](#)

## Understanding Filter Expressions

A filter expression is a set of logical expressions that describe the constraints you want to place on a collection.

Each logical expression uses a relational operator to contrast an attribute name (such as area or direction) with a value. The syntax for a logical expression is as follows:

`attributeoperatorvalue`

For a list of frequently-used attributes, see [Filter Expression Attributes](#). The value can be a number (such as 43 or 3.45) or a keyword string (such as input or output).

The following table shows the relational operators that you can use in logical expressions:

Syntax	Value	Description
a<b	numeric, string	1 if a is less than b, 0 otherwise
a>b	numeric, string	1 if a is greater than b, 0 otherwise
a<=b	numeric, string	1 if a is less than or equal to b, 0 otherwise
a>=b	numeric, string	1 if a is greater than or equal to b, 0 otherwise
a==b	numeric, string, Boolean	1 if a is equal to b, 0 otherwise
a!=b	numeric, string, Boolean	1 if a is not equal to b, 0 otherwise

You can combine logical expressions using logical AND (AND or `&&`) or logical OR (OR or `||`). You can group logical expressions with parentheses to enforce order; otherwise, the order is left to right.

When you use a string value as an argument in a logical expression, you do not need to enclose the string in quotation marks. This is useful because when you use a filter expression as an argument, you must enclose the entire filter expression in quotation marks or curly braces.

For example, the following filter expression selects all hierarchical cells whose area attribute is less than 12 units:

```
"is_hierarchical==true && area<12"
```

Design Vision tool can fail to parse a filter expression because of the following reasons:

- Invalid syntax
- Invalid attribute name
- Type mismatch between an attribute and its compare value

You can use the `-filter` option of the `get*` commands or the `filter_collection` command to select specific objects from a collection. Both the `-filter` option and the `filter_collection` command use filter expressions to restrict the resulting collection.

### Using the `-filter` option

Many commands that create collections accept a `-filter` option that specifies a filter expression. For example, the following command gets the hierarchical cells in U1 that have an area less than 12:

```
prompt> set regs \
    [get_instances U1/* \ -filter "is_hierarchical==true && area<12"]
```

The command then assigns the collection to the `regs` variable.

### Using the `filter_collection` command

It is usually more efficient to filter out objects during the collection process, as shown above. However, sometimes it is useful to filter an existing collection by using the `filter_collection` command, which takes a collection and a filter expression as arguments. The result is a new collection (or an empty string if no objects match the criteria).

The following two commands return the same collection:

```
prompt> get_cells * -filter "reference == FD1"
prompt> filter_collection [get_cells *] \ "reference == FD1"
```

## Filter Expression Attributes

The following table shows the names of attributes that are frequently used in filter expressions, the types of objects to which they can be applied, and the types of values that they accept. The table is organized alphabetically by object type. To see a complete list of attributes, use the `list_attributes` command.

Attribute Name	Object Value
<code>dont_touch</code>	Cell Boolean

<b>Attribute Name</b>	<b>Object Value</b>
full_name	Cell String
is_hierarchical	Cell Boolean
object_class	Cell String
ref_name	Cell String
scan_chain	Cell Integer
dont_touch	Net Boolean
full_name	Net String
ideal_net	Net Boolean
object_class	Net String
full_name	Pin String
ideal_network	Pin Integer
object_class	Pin String
pin_direction	Pin String
pin_name	Pin String
pin_properties	Pin String
scan_chain	Pin Integer
clock	Port Boolean
clock_pin	Port Boolean
direction	Port Integer
dont_touch_network	Port Boolean
full_name	Port String
ideal_network	Port Integer
object_class	Port String
port_direction	Port String
scan_chain	Port Integer
signal_type	Port String

---

## Using the Visual UPF Dialog Box

You can use the Visual UPF dialog box to create IEEE 1801 power domains and define their supply networks, connections with other power domains, and relationships with elements in the design hierarchy. You can also review and edit an existing power architecture. IEEE 1801 is also known as Unified Power Format (UPF).

The Visual UPF dialog box contains the work environment for power domain generation. It displays the design hierarchy and provides the tools you use to define the power domains and supply sets for the top-level design and its subdesigns (hierarchical cells).

For more information, see [Using the Visual UPF Dialog Box](#).

---

## Wire Load (Attributes > Operating Environment)

Use Wire Load to assign or remove a wire load model for the current design. The wire load must be defined in one of the libraries in the link library (including the local link library).

When you choose Attributes > Operating Environment > Wire Load, the Wire Load dialog box appears. You can use the wire load model named in the Wire load model dialog box or select a different model from the list of available models.

You can use the Report Wire Load dialog box (choose Timing > Report Wire Load) to view the wire load information for the current design. For details, see [Reporting Wire Load Information](#).

The following options appear in the Wire Load dialog box:

- Current design - Displays the name of the current design.
- Wire load model - Displays the name of the current wire load model and, in parentheses, the name of the library in which it is defined. The available model names appear in the list below the Wire load model dialog box. To change models, select a different model name from the list.
- Select NONE - to clear the Wire load model dialog box options and remove the assigned wire load model from the current design.

Command cross-reference:

- `set_wire_load_model -name model_name -library lib_name`
- `remove_wire_load_model`

**See Also**

- [Selecting a Wire Load Model](#)
  - [Operating Conditions \(Attributes > Operating Environment\)](#)
  - [Timing Range \(Attributes > Operating Environment\)](#)
- 

## Tcl Commands and Variables

The following topics provide information about Tcl commands that are used frequently in Design Vision tool:

- [get\\_selection](#)
  - [change\\_selection](#)
- 

### **get\_selection**

You can use the `get_selection` command to create a heterogeneous collection of selected objects. This command returns a collection handle that can be assigned to a variable or passed to another command. If you have not selected any objects, the command returns an empty collection.

The syntax is

```
get_selection  
[-type object_type | -design design_name]  
-type object_type
```

Choose within design, port, net, cell, or pin.

```
-design design_name
```

Specifies the design selected.

For example, to return a handle to the collection of selected objects, enter the following command:

```
prompt> get_selection
```

**See Also**

- [change\\_selection](#)

---

## change\_selection

You can use the `change_selection` command to change your current selection. Depending on which option you choose, you can replace the current selection with the object list, add the current list to the current selection, or remove the object list from the current selection.

The syntax is

```
change_selection  
[-type object_type]  
[-replace | -add | -remove]  
object_list
```

`-type object_type`

Choose among design, port, net, cell, or pin.

`-replace`

Replaces the current selection with the object list. This is the default.

`-add`

Adds the object list to the current selection.

`-remove`

Removes the object list from the current selection.

`object_list`

Returns the collection handle for the list of objects to add, replace, or remove.

For example, to query the CP pins of instances that begin with “o” and set them as the current selection, enter the following command:

```
prompt> change_selection [get_pins o*/CP]
```

To show the addition of all nets to the current selection, enter the following command:

```
prompt> set allnets [get_nets *]  
prompt> change_selection -add $allnets
```

### See Also

- [get\\_selection](#)