VLSI HW4 Report

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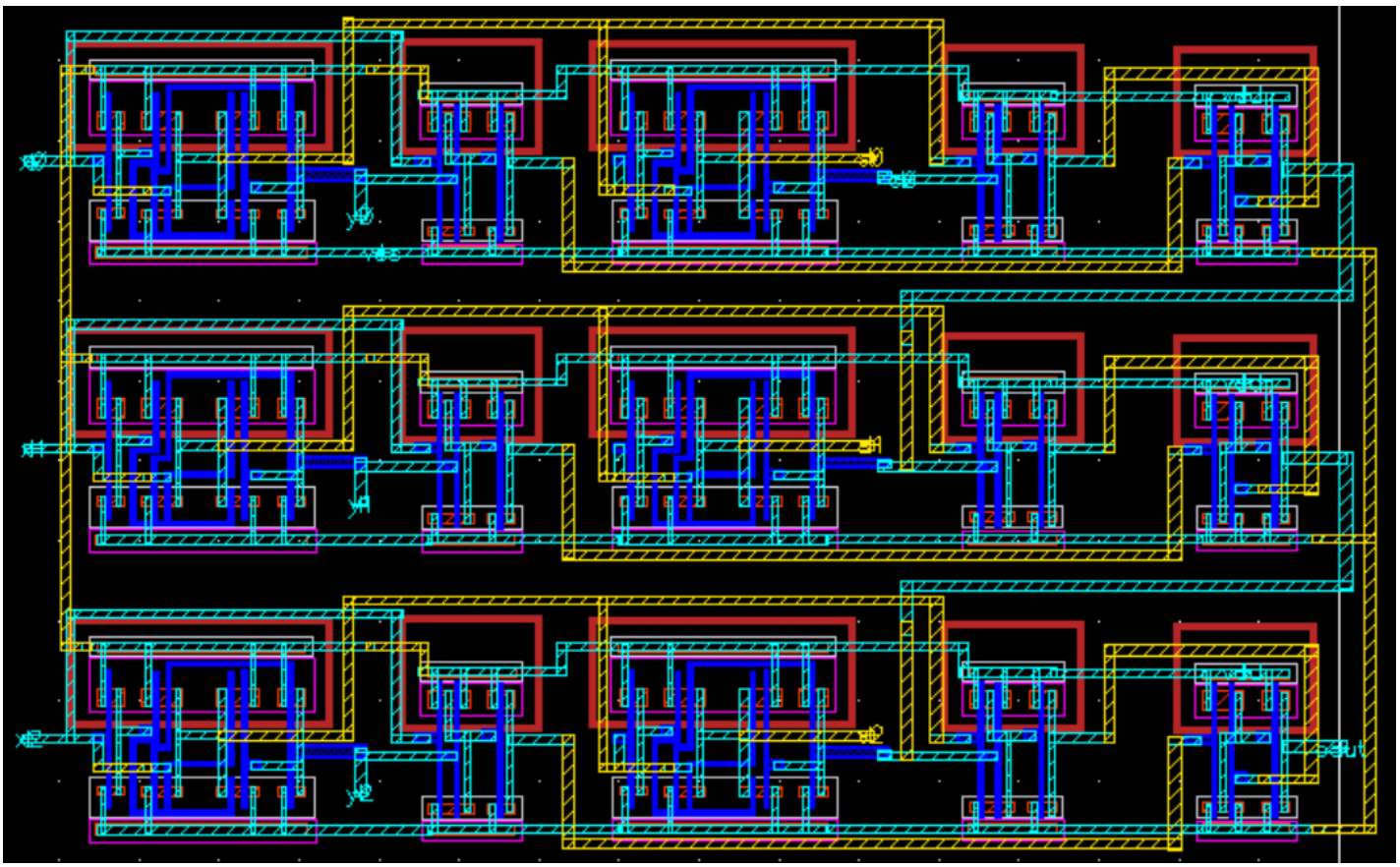
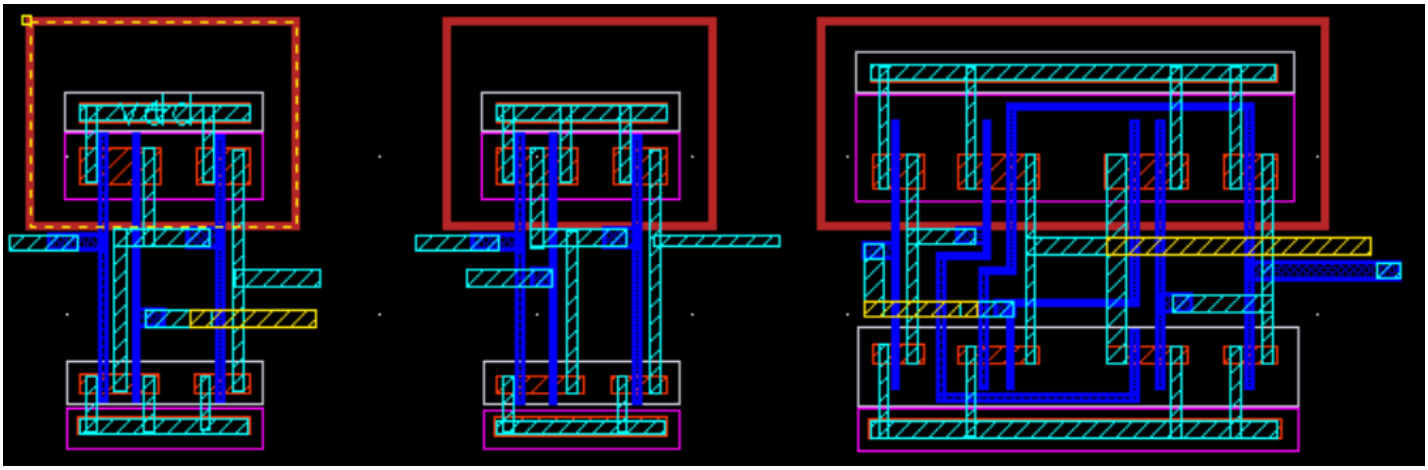
1. Layout 的圖、DRC 及 LVS 成功的截圖

3 Bit full adder Layout cell view:



由以下 gate 組成:

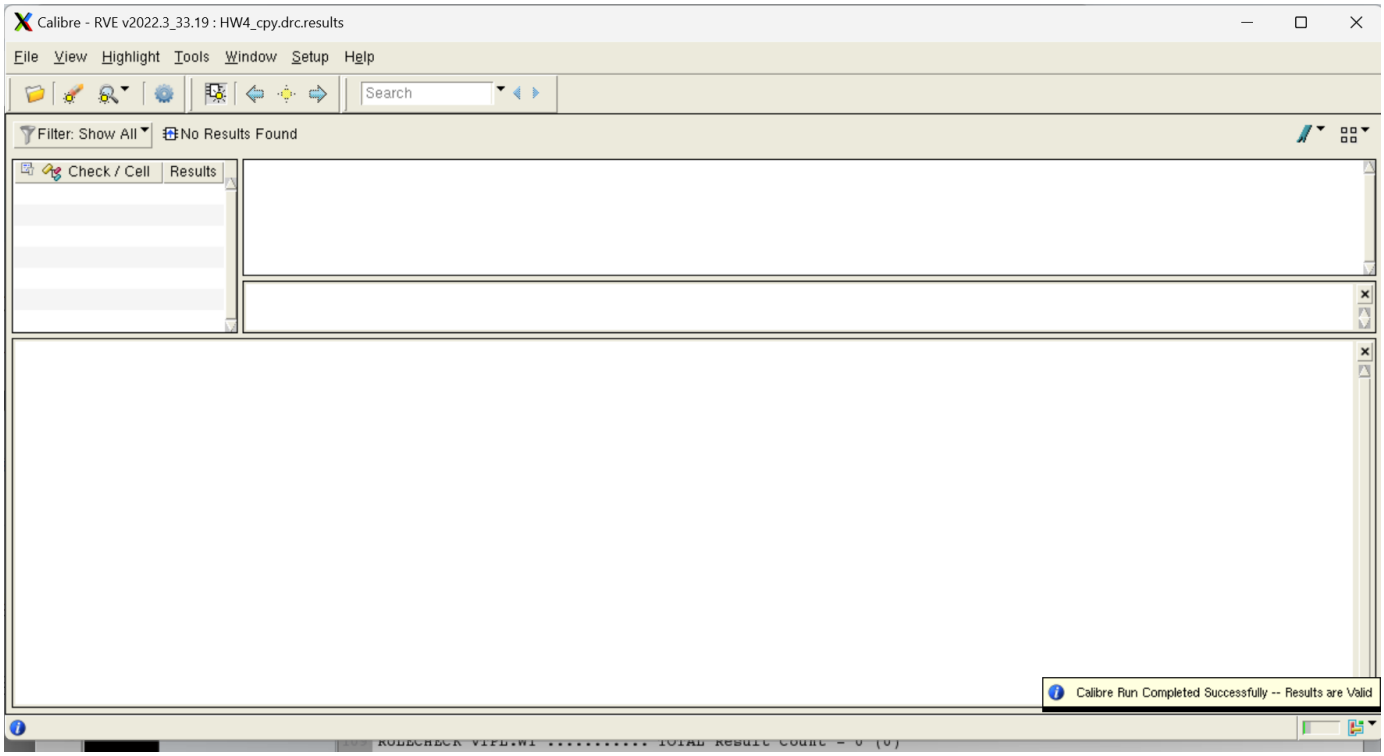


OR gate

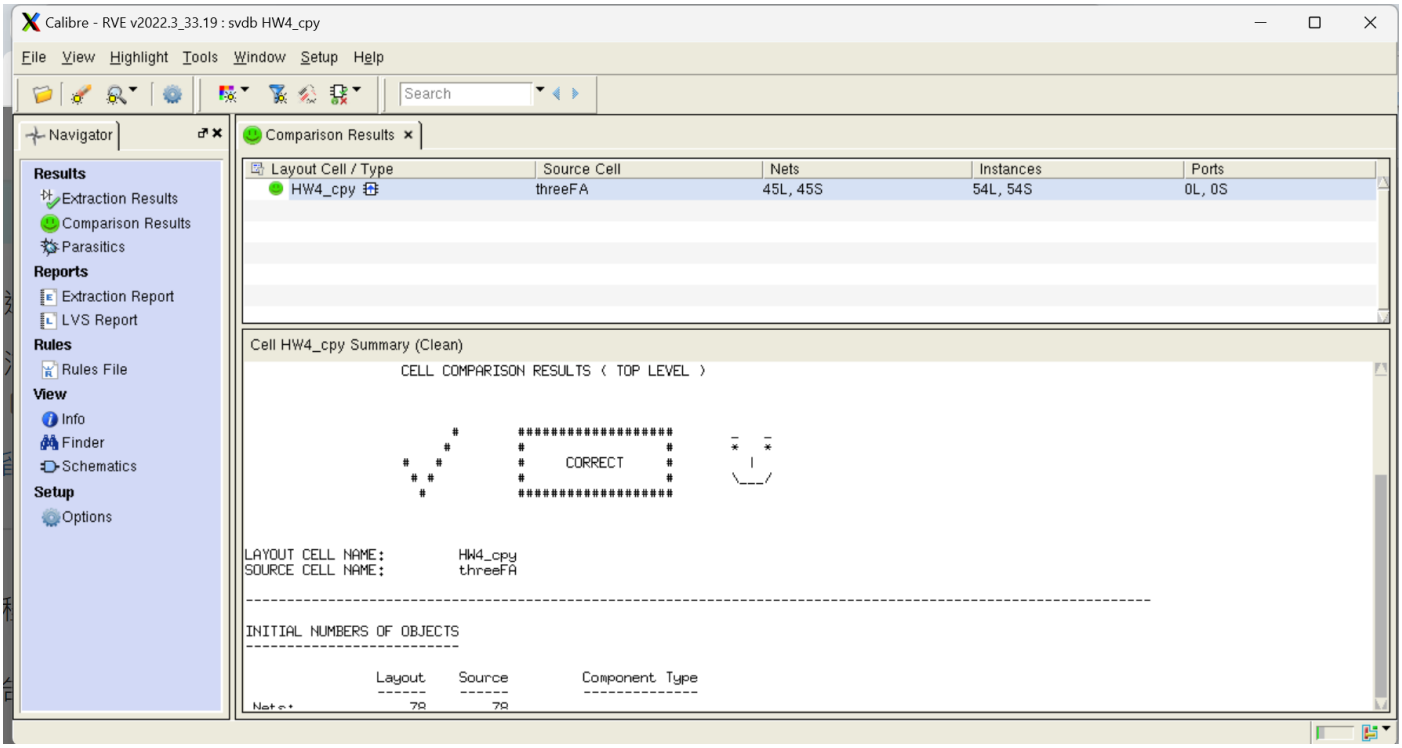
AND gate

XOR gate

DRC 成功畫面截圖:



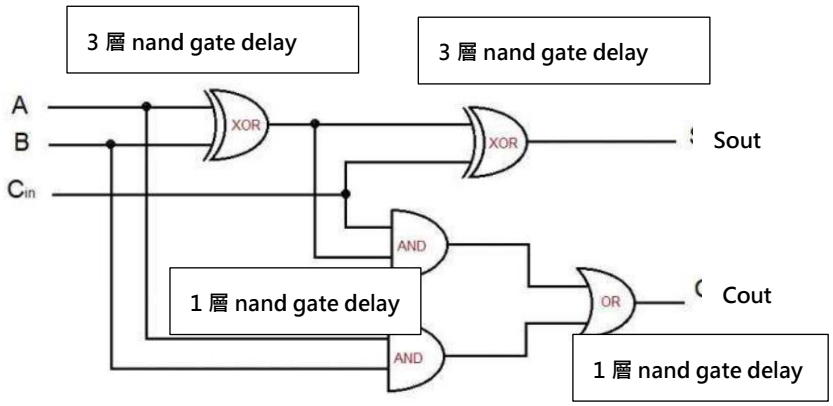
LVS 成功畫面截圖



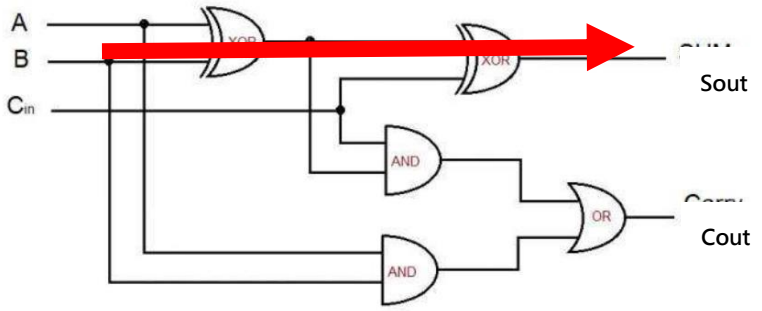
2. post-sim 量測 worst-case propagation delay(用 layout 後的.sp 檔)

測試結果: input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) ，y0 到 s2 的 delay= 1.653ns

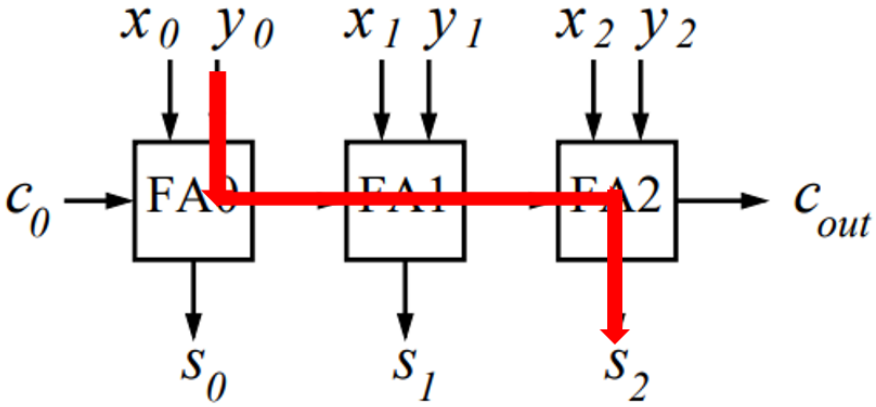
這次測量的過程中，測到最大的 delay 是出現在 y0 到 s2 的 delay，出現在當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)時, worst case delay 為 1.653ns，原因應該是當 input pattern 為 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)時，S2 和 Cout 的電位都是 0，當 input pattern 為 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)時，S2 和 Cout 的電位都是 1，故兩者都有充放電的現象，且由上圖可知，當 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)時，C1 和 C2 都為 1，故在這樣的 pattern change 下，Cout 和 S2 的 delay 會等於 FA0、FA1、FA2 的 delay 相加，會是 worst case delay. 而 critical path 會出現在 y0 到 s2 而非 y0 到 cout 的原因和我們的電路有關，原因如下:



故一個 full adder 的 critical path 如下:



整個 3-bit ripple carry full adder 的 critical path 如下:



我們的 post-sim 總共有五組測資，每組測資都分別測量 y0 to s2 與 y0 to cout 的 delay，整理如下，可知當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)時, worst case delay 為 1.653ns:

起始input pattern	切換後input pattern	y0 t0 s2 delay	y0 to cout delay
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,1,1)	720.6ps	349.2ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,0,1)	1.653ns	349.2ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,1,1)	720.5ps	349.3ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,0,1)	1.237ns	349.1ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,1,1)	720.6ps	349.3ps

Worst case dely

五次測試的內容詳細整過程如下:

A. C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0) -> C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,1,1)
說明:當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,1,1)時，y0 至 s2 的 delay 為 720.6ps，y0 至 cout 的 delay 為 349.2ps。

a. Test pattern for y0 to s2 delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(s2) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

b. y0 to s2 delay

```
 .title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  48.4342u  from=   0.             to=  50.0000n
tdealy= 720.6176p  targ=   5.6706n   trig=   4.9500n

          ***** job concluded
```

c. Test pattern for y0 to cout delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(cout) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

d. y0 to cout delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  48.6421u  from=   0.            to=  50.0000n
tdealy= 349.2278p  targ=   5.2992n   trig=   4.9500n

         ***** job concluded
```

B. C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0) -> C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)

說明:當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0)=(1,0,1)時，y0 至 s2 的 delay 為 1.653ns，y0 至 cout 的 delay 為 349.2ps。

a. Test pattern for y0 to s2 delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(s2) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

b. y0 to s2 delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  53.5926u  from=   0.            to=  50.0000n
tdealy=   1.6539n  targ=   6.6039n   trig=   4.9500n

         ***** job concluded
```

c. Test pattern for y0 to cout delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(cout) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

d. y0 to cout delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  53.7185u  from=   0.             to=  50.0000n
tdealy= 349.1852p  targ=   5.2992n   trig=   4.9500n
```

C. C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0) -> C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) =(1,1,1)

說明:當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) =(1,1,1)時，y0 至 s2 的 delay 為 720.5ps，y0 至 cout 的 delay 為 349.3ps。

a. Test pattern for y0 to s2 delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(s2) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

b. y0 to s2 delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  51.3483u  from=   0.             to=  50.0000n
tdealy= 720.5750p  targ=   5.6706n   trig=   4.9500n
```

c. Test pattern for y0 to cout delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(cout) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

d. y0 to cout delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  51.5034u  from=   0.             to=  50.0000n
tdealy= 349.2619p  targ=   5.2993n   trig=   4.9500n
```

D. C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0) -> C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) =(1,0,1)

說明:當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) =(1,0,1)時，y0 至 s2 的 delay 為 1.237ns，y0 至 cout 的 delay 為 349.1ps。

a. Test pattern for y0 to s2 delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(s2) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

b. y0 to s2 delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  49.9195u  from=   0.             to=  50.0000n
tdealy=   1.2375n  targ=   6.1875n   trig=   4.9500n
```

c. Test pattern for y0 to cout delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(cout) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

d. y0 to cout delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  50.0626u  from=   0.             to=  50.0000n
tdealy= 349.1635p  targ=   5.2992n   trig=   4.9500n
```

E. C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0) -> C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) =(1,1,1)

說明:當 input pattern 由 C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)切換至 C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) =(1,1,1)時，y0 至 s2 的 delay 為 720.6ps，y0 至 cout 的 delay 為 349.3ps。

a. Test pattern for y0 to s2 delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(s2) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

b. y0 to s2 delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  52.4978u  from=   0.             to=  50.0000n
tdealy= 720.5750p  targ=   5.6706n   trig=   4.9500n
```

c. Test pattern for y0 to cout delay

```
.meas tran Tdealy
+trig v(y0) val=1.3*0.5 rise=1
+targ v(cout) val=1.3*0.5 rise=1

Vx0 x0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx1 x1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx2 x2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy0 y0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 20ns)
Vy2 y2 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vc0 c0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY
```

d. Test pattern for y0 to s2 delay

```
.title ripplecarryadder

****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  52.6427u  from=   0.             to=  50.0000n
tdealy= 349.2619p  targ=   5.2993n   trig=   4.9500n
```

3. post-sim 量測所消耗的 average power consumption(用 layout 後的.sp 檔)

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

Vx1 x1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)

Vx2 x2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)

Vy0 y0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)

Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)

Vy2 y2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)

Vc0 c0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)

當 Input pattern 如上時，我們測量到 post sim 的 average power consumption 如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  33.0555u  from=   0.             to=  50.0000n

          ***** job concluded
```

4. HW3(pre-sim)跟 post-sim 的 worst case delay 與 average power consumption 的比較

A. worst case delay 比較:

HW3 的 delay 量測:

測試序號	Input Pattern 切換說明	y0至s2 的 Delay (ps)	y0至cout 的 Delay (ps)
1	C0=0, (X2,X1,X0)=(0,0,0), (y2,y1,y0)=(0,0,0) -> C0=1, (X2,X1,X0)=(1,1,1), (y2,y1,y0)=(1,1,1)	398.5	216.9
2	C0=0, (X2,X1,X0)=(0,0,0), (y2,y1,y0)=(0,0,0) -> C0=1, (X2,X1,X0)=(1,1,0), (y2,y1,y0)=(1,0,1)	856.5	217.9
3	C0=0, (X2,X1,X0)=(0,0,0), (y2,y1,y0)=(0,0,0) -> C0=1, (X2,X1,X0)=(1,1,0), (y2,y1,y0)=(1,1,1)	398.5	216.9
4	C0=0, (X2,X1,X0)=(0,0,0), (y2,y1,y0)=(0,0,0) -> C0=1, (X2,X1,X0)=(1,1,1), (y2,y1,y0)=(1,0,1)	677.6	216.9
5	C0=0, (X2,X1,X0)=(0,0,0), (y2,y1,y0)=(0,0,0) -> C0=1, (X2,X1,X0)=(1,1,0), (y2,y1,y0)=(1,1,1)	677.6	216.9

Pre-sim Worst case delay=856.5ps

起始input pattern	切換後input pattern	y0 t0 s2 delay	y0 to cout delay
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,1,1)	720.6ps	349.2ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,0,1)	1.653ns	349.2ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,1,1)	720.5ps	349.3ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,1), (y2, y1, y0) = (1,0,1)	1.237ns	349.1ps
C0=0, (X2, X1, X0) = (0,0,0), (y2, y1, y0) = (0,0,0)	C0=1, (X2, X1, X0) = (1,1,0), (y2, y1, y0) = (1,1,1)	720.6ps	349.3ps

Pos-sim Worst case delay=1.653ns

解釋與說明:我們 pre-sim 和 pos-sim 的測資是一樣的，從測試結果可以看出我們 pos-sim 的 time delay 都比 pre-sim 大，可能的原因如下:

1. 因為在 HW4(pos-sim)中，我們都不考慮寄生電容，所以這邊的 gate delay 估計的方式我們無法用 simple 或是 elmore model 解釋。

- Simple RC modeling
  - Lumped RCs
  - $t_{df} = \sum R_{pulldown} \times \sum C_{pulldown-path}$
- Elmore RC modeling
  - Distributed RCs
  - $t_d = \sum_i R_i C_i$

2. Rise time 與 fall time 的差異:我們這邊的測試統一都是測試 rise time，rise time 的 formula:

$$t_r = -RC \cdot \ln(1 - 0.9),\ t_r \approx 0.693 \times RC$$

我們 pre-sim 時的 Pmos W/L=2um/0.18um, Nmos W/L=1um/0.18um，但 HW4(pos-sim)因為繪製 layout 需要，所以改成 Pmos W/L=1.13um/0.19um, Nmos W/L=0.58um/0.19um
由以上的計算可知，R 和 W/L 成反比，故 rise time，也就是 worst case delay 必定會比較大。

B. average power consumption 比較:

Pre-sim average power consumption:

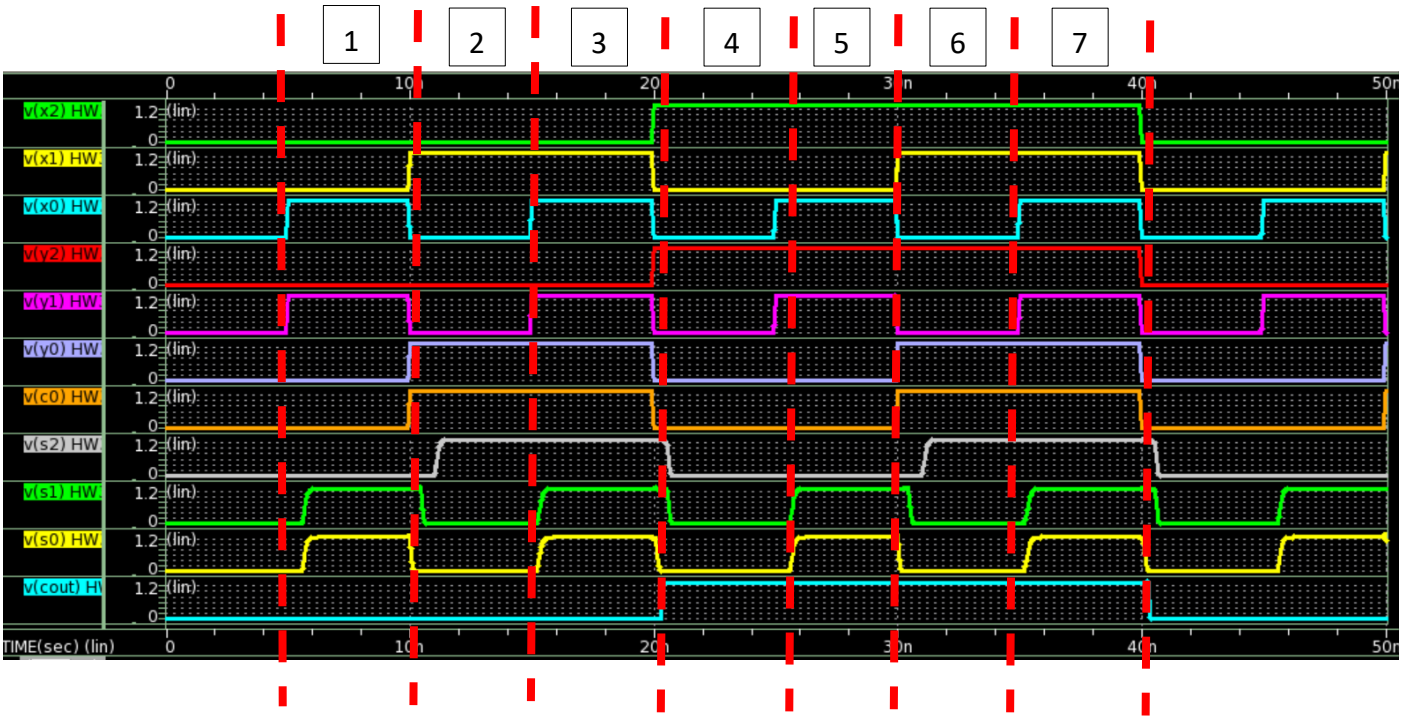
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  44.1412u  from=   0.             to=  50.0000n
```

Pos-sim average power consumption:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  33.0555u  from=   0.             to=  50.0000n
```

解釋與說明:我們 pre-sim 和 pos-sim 的測資是一樣的，從測試結果可以看出我們 pos-sim 的 average power consumption 都比 pre-sim 小，我認為最有可能的原因是，pos-sim 我們沒有考慮寄生電容，所以整體功號相對小。

5. Post-sim 的波型(共七組測資)



(x2,x1,x0)= X, (y2,y1,y0)=Y, Ci= c0

波形說明與 function 驗證

序號	c0	x2×1×0	y2y1y0	s2s1s0	Cout	Function
1	1	001	001	011	0	正確
2	0	010	010	100	0	正確
3	1	011	011	111	0	正確
4	0	100	100	000	1	正確
5	1	101	101	011	1	正確
6	0	110	110	100	1	正確
7	1	111	111	111	1	正確

說明:由以上七組測試資料可知我們 3 bit full adder function 正確。

6. 跑 LVS 的.sp

```
.subckt xor vin1 vin2 vout vdd vss
mp0 inv1 vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 c inv1 vdd vdd P_18 W=1.13u l=0.19u
mp2 vout vin2 c vdd P_18 W=1.13u l=0.19u
mp3 vout vin1 d vdd P_18 W=1.13u l=0.19u
mp4 d inv2 vdd vdd P_18 W=1.13u l=0.19u
mp5 inv2 vin2 vdd vdd P_18 W=1.13u l=0.19u
mn0 inv1 vin1 vss vss N_18 W=0.58u l=0.19u
mn1 e vin2 vss vss N_18 W=0.58u l=0.19u
mn2 vout vin1 e vss N_18 W=0.58u l=0.19u
mn3 vout inv1 f vss N_18 W=0.58u l=0.19u
mn4 f inv2 vss vss N_18 W=0.58u l=0.19u
mn5 inv2 vin2 vss vss N_18 W=0.58u l=0.19u
.ends
.subckt and vin1 vin2 vout vdd vss
mp0 v1 vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 v1 vin2 vdd vdd P_18 W=1.13u l=0.19u
mp2 vout v1 vdd vdd P_18 W=1.13u l=0.19u
mn0 c vin1 vss vss N_18 W=0.58u l=0.19u
mn1 v1 vin2 c vss N_18 W=0.58u l=0.19u
mn2 vout v1 vss vss N_18 W=0.58u l=0.19u
.ends
```

```
.subckt or vin1 vin2 vout vdd vss
mp0 c vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 v1 vin2 c vdd P_18 W=1.13u l=0.19u
mp2 vout v1 vdd vdd P_18 W=1.13u l=0.19u
mn0 v1 vin1 vss vss N_18 W=0.58u l=0.19u
mn1 v1 vin2 vss vss N_18 W=0.58u l=0.19u
mn2 vout v1 vss vss N_18 W=0.58u l=0.19u
.ends

.subckt FA A B cin cout sout vdd vss
Xxor1 A B out1 vdd vss xor
Xxor3 out1 cin sout vdd vss xor
Xand2 A B out2 vdd vss and
Xand4 out1 cin out3 vdd vss and
Xor5 out2 out3 cout vdd vss or
.ends

.subckt 3BFA c0 x0 y0 x1 y1 x2 y2 s0 s1 s2 cout vdd vss
XFA1 x0 y0 c0 cout1 s0 vdd vss FA
XFA2 x1 y1 cout1 cout2 s1 vdd vss FA
XFA3 x2 y2 cout2 cout s2 vdd vss FA
.ends
```

7. Pre-sim 的.sp(即 HW3 的.sp)

```
.title ripplecarryadder
.protect
.lib '/cad/cell_lib/cic018.l'tt
.unprotect
.option post captab accurate
.temp 25
.meas tran pwr avg power

.global vdd vss
vdd vdd 0 dc 1.3
vss vss 0 dc 0
```

```
.subckt xor vin1 vin2 vout vdd vss
mp0 inv1 vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 c inv1 vdd vdd P_18 W=1.13u l=0.19u
mp2 vout vin2 c vdd P_18 W=1.13u l=0.19u
mp3 vout vin1 d vdd P_18 W=1.13u l=0.19u
mp4 d inv2 vdd vdd P_18 W=1.13u l=0.19u
mp5 inv2 vin2 vdd vdd P_18 W=1.13u l=0.19u

mn0 inv1 vin1 vss vss N_18 W=0.58u l=0.19u
mn1 e vin2 vss vss N_18 W=0.58u l=0.19u
mn2 vout vin1 e vss N_18 W=0.58u l=0.19u
mn3 vout inv1 f vss N_18 W=0.58u l=0.19u
mn4 f inv2 vss vss N_18 W=0.58u l=0.19u
mn5 inv2 vin2 vss vss N_18 W=0.58u l=0.19u
.ends

.subckt and vin1 vin2 vout vdd vss
mp0 v1 vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 v1 vin2 vdd vdd P_18 W=1.13u l=0.19u
mp2 vout v1 vdd vdd P_18 W=1.13u l=0.19u

mn0 c vin1 vss vss N_18 W=0.58u l=0.19u
mn1 v1 vin2 c vss N_18 W=0.58u l=0.19u
mn2 vout v1 vss vss N_18 W=0.58u l=0.19u
.ends

.subckt or vin1 vin2 vout vdd vss
mp0 c vin1 vdd vdd P_18 W=1.13u l=0.19u
mp1 v1 vin2 c vdd P_18 W=1.13u l=0.19u
mp2 vout v1 vdd vdd P_18 W=1.13u l=0.19u

mn0 v1 vin1 vss vss N_18 W=0.58u l=0.19u
mn1 v1 vin2 vss vss N_18 W=0.58u l=0.19u
mn2 vout v1 vss vss N_18 W=0.58u l=0.19u
.ends

.subckt FA A B cin cout sout vdd vss
```

```
Xxor1 A B out1 vdd vss xor
Xxor3 out1 cin sout vdd vss xor
Xand2 A B out2 vdd vss and
Xand4 out1 cin out3 vdd vss and
Xor5 out2 out3 cout vdd vss or
.ends

.subckt threeBFA c0 x0 y0 x1 y1 x2 y2 s0 s1 s2 cout vdd vss
XFA1 x0 y0 c0 cout1 s0 vdd vss FA
XFA2 x1 y1 cout1 cout2 s1 vdd vss FA
XFA3 x2 y2 cout2 cout s2 vdd vss FA
.ends

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx2 x2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)
Vy0 y0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)
Vc0 c0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)

XFA1 x0 y0 c0 cout1 s0 vdd vss FA
XFA2 x1 y1 cout1 cout2 s1 vdd vss FA
XFA3 x2 y2 cout2 cout s2 vdd vss FA

Cload1 cout1 vss 1f
Cload2 cout2 vss 1f
Cload3 cout vss 1f
Cload4 s0 vss 1f
Cload5 s1 vss 1f
Cload6 s2 vss 1f

.tran 0.01n 50n
.option post
.end
```

8. Pos-sim 的.sp 檔

(因為 Pos-sim 直接 include PEX 的 netlist 所以整個 3-bit full adder 的 module 就叫做 HW4_cpy)

```
.title ripplecarryadder
.protect
.lib '/cad/cell_lib/cic018.l'tt
.inc HW4_cpy.pex.netlist
.unprotect
.option post captab accurate
.temp 25
.meas tran pwr avg power

.global vdd vss
vdd vdd 0 dc 1.3
vss vss 0 dc 0

Vx0 x0 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vx1 x1 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vx2 x2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)
Vy0 y0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)
Vy1 y1 0 pulse (0v 1.3v 4.9ns 0.1ns 0.1ns 4.9ns 10ns)
Vy2 y2 0 pulse (0v 1.3v 19.9ns 0.1ns 0.1ns 19.9ns 40ns)
Vc0 c0 0 pulse (0v 1.3v 9.9ns 0.1ns 0.1ns 9.9ns 20ns)

XHW4_CPY vdd x2 x1 x0 s2 s1 s0 vss y2 y1 y0 c0 cout HW4_CPY

.tran 0.01n 50n
.option post
.end
```