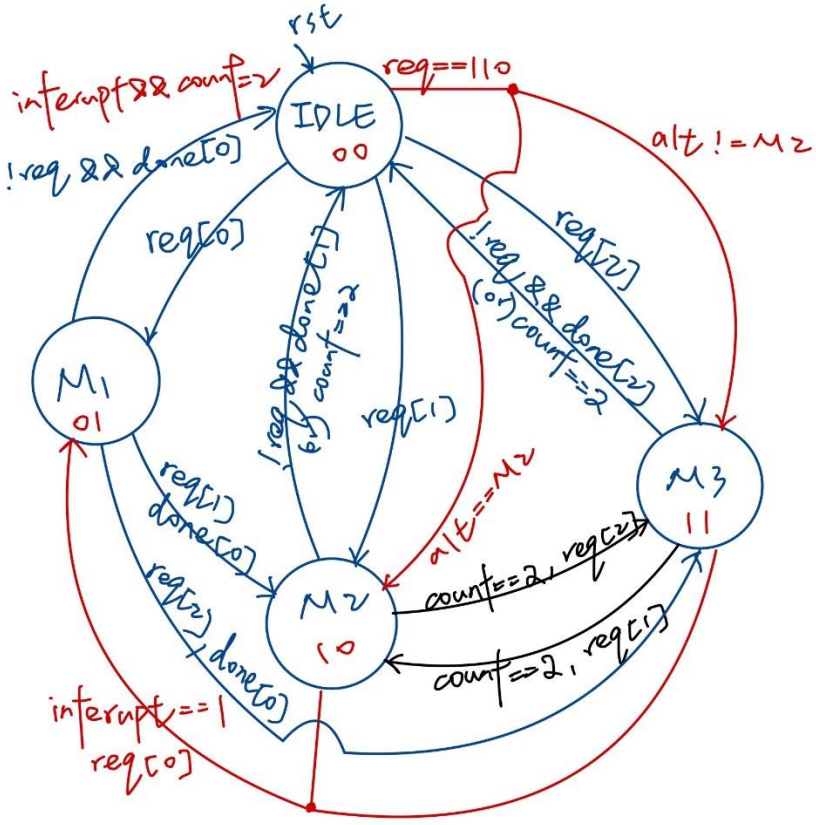
Lab: Memory controller

Name: Hsuan-Chih Hsu (Kevin)

- A clearly marked diagram of the finite state machine



Note:

counter for M1 & M2 is at most 2 cycles.

if M1 interupts others, counter for M1 activates and is also at most 2 cycles in this situation.

- a walkthrough of your machine's operation

1. M2 requests first
2. Next cycle, M2 accesses the memory; however, M1 also requests
3. Next cycle, “M1 interrupts” M2 successfully; therefore, M1 accesses the memory
4. Next cycle, M1 is done with the machine; therefore, state is back to “IDLE”