Computer System Architecture

Fifth week’s Report

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Laptop Lenovo P52

- Processor
  - Intel® Core™ i7-8850H @ 2.60GHz
- Power Saving Functions
  - C-States power saving modes
  - P-States power saving modes (Speed Step)
  - Intel Turbo Boost

Smart phone iPhone SE

- Processor
  - Apple A9
- Power saving functions
  - Run/Standby/Shutdown/Dormant modes
  - Processor speed reduction

Impact on power and energy consumption by reducing clock speed

- Let original power, voltage, energy, delay and frequency denote as: $P_0, V_{DD_0}, E_0, D_0, F_0$ and the new power, voltage energy, delay and frequency denote as: P, V_{DD}, E, D, F
- For the same instruction set we have:

$$D = IC \times CPI \times CCT \times 1/(1 - 15\%) = IC \times CPI \times CCT \times 1/0.85$$

Impact on power and energy consumption by reducing clock speed

- The original power is:

$$P_0 = C_L \cdot {V_{DD_0}}^2 \cdot S_{0\to1} \cdot F_0 + t_{SC} \cdot V_{DD_0} \cdot I_{SC} \cdot S_{0\to1} \cdot F_0 + V_{DD_0} \cdot I_{leakage}$$

$$P_0 = V_{DD_0}(C_L \cdot V_{DD_0} \cdot S_{0\to1} \cdot F_0 + t_{SC} \cdot I_{SC} \cdot S_{0\to1} \cdot F_0 + I_{leakage})$$

- Therefore, the new power is:

$$P = V_{DD}(C_L \cdot V_{DD} \cdot S_{0\to1} \cdot F + t_{SC} \cdot I_{SC} \cdot S_{0\to1} \cdot F + I_{leakage})$$

$$P = 0.85V_{DD_0}(C_L \cdot 0.85V_{DD_0} \cdot S_{0\to1} \cdot 0.85F_0 + t_{SC} \cdot I_{SC} \cdot S_{0\to1} \cdot 0.85F_0 + I_{leakage})$$

Impact on power and energy consumption by reducing clock speed

- The new power:

$$P = 0.85V_{DD_0}(0.7225C_L \cdot V_{DD_0} \cdot f_{0\to1} + 0.85t_{SC} \cdot I_{SC} \cdot f_{0\to1} + I_{leakage})$$

$$\frac{P}{P_0} = \frac{0.85\,(0.7225C_L \cdot V_{DD_0} \cdot f_{0\to1} + 0.85t_{SC} \cdot I_{SC} \cdot f_{0\to1} + I_{leakage})}{C_L \cdot V_{DD_0} \cdot f_{0\to1} + t_{SC} \cdot I_{SC} \cdot f_{0\to1} + I_{leakage}}$$

As a result above, we have a power reduction greater than 15% depending on the actual processor configuration

Impact on power and energy consumption by reducing clock speed

- The original energy consumption:

$$E_0 = P_0 \cdot D_0 = (1/0.85)P_0 \cdot D$$

- The new energy consumption:

$$E = P \cdot D$$

Impact on power and energy consumption by reducing clock speed

- Therefore, the ratio is:

$$\frac{E}{E_0} = \frac{P \cdot D}{(1/0.85)P_0 \cdot D} = \frac{P}{P_0} \cdot 0.85$$

- As from previous result, this equation become:

$$\frac{E}{E_0} = \frac{0.7225C_L \cdot V_{DD_0} \cdot f_{0\to1} + 0.85t_{SC} \cdot I_{SC} \cdot f_{0\to1} + I_{leakage}}{C_L \cdot V_{DD_0} \cdot f_{0\to1} + t_{SC} \cdot I_{SC} \cdot f_{0\to1} + I_{leakage}}$$

This equation shows that the reduction in total energy consumption is not so significant as the power consumption, which might be the main reason for CPU manufacturers choose C-steps or P-steps to save energy in idle state