Hardware Software Platforms Project Presentation

G4-DE1-Serial-RS232

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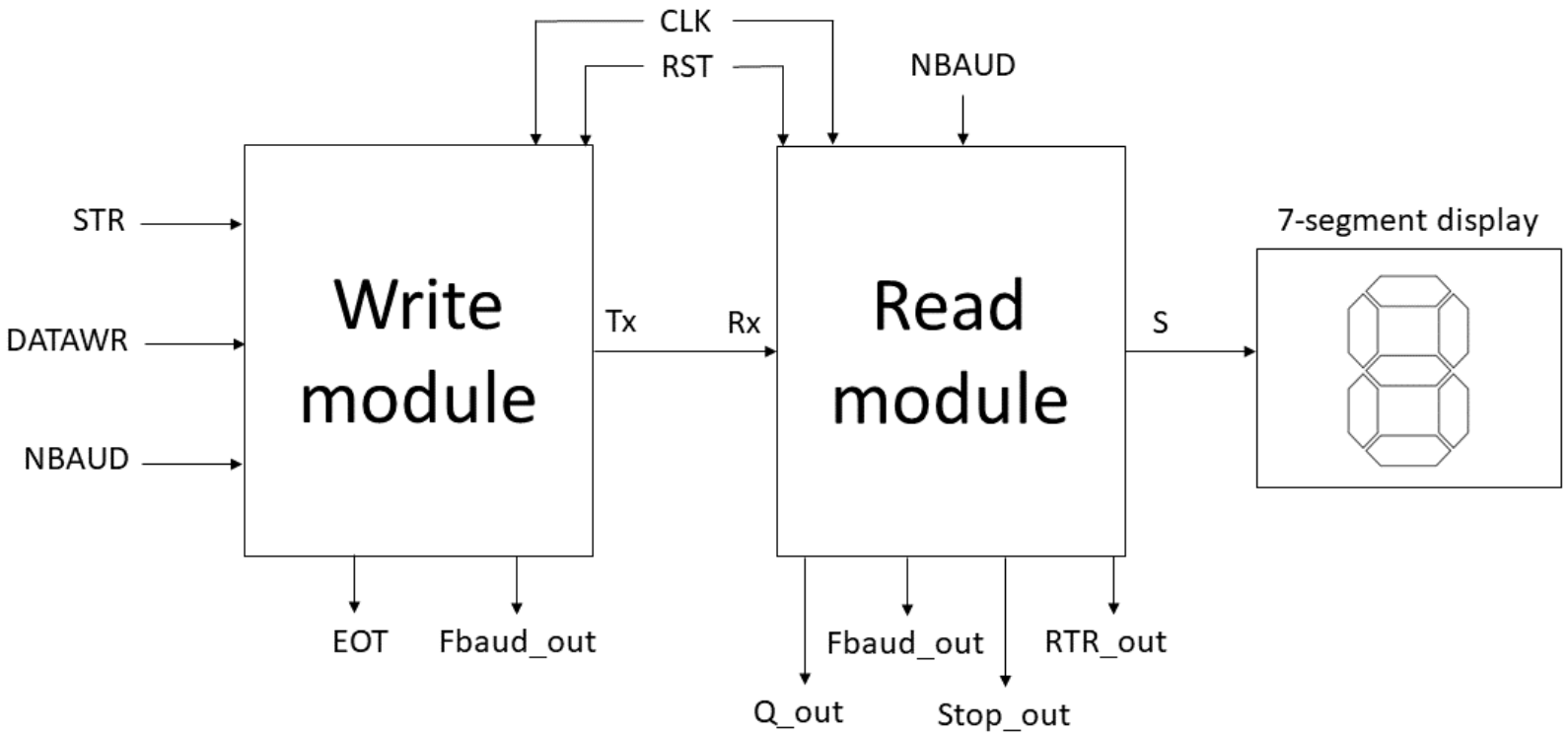
Structure


CLK
RST
NBAUD
STR
DATAWR
NBAUD
Write module
Tx
Rx
Read module
S
7-segment display
EOT
Fbaud_out
Fbaud_out
RTR_out
Q_out
Stop_out

Structure

- Write module
  - Source codes
  - Test bench
  - Simulation
- Read module
  - Source codes
  - Test bench
  - Simulation

Write module

- Source codes

3 codes manage the baudrate, the FSM and the shift of the buffer.

1 top level code links the 3 components.

Write module

- Test bench

Setting of the inputs:

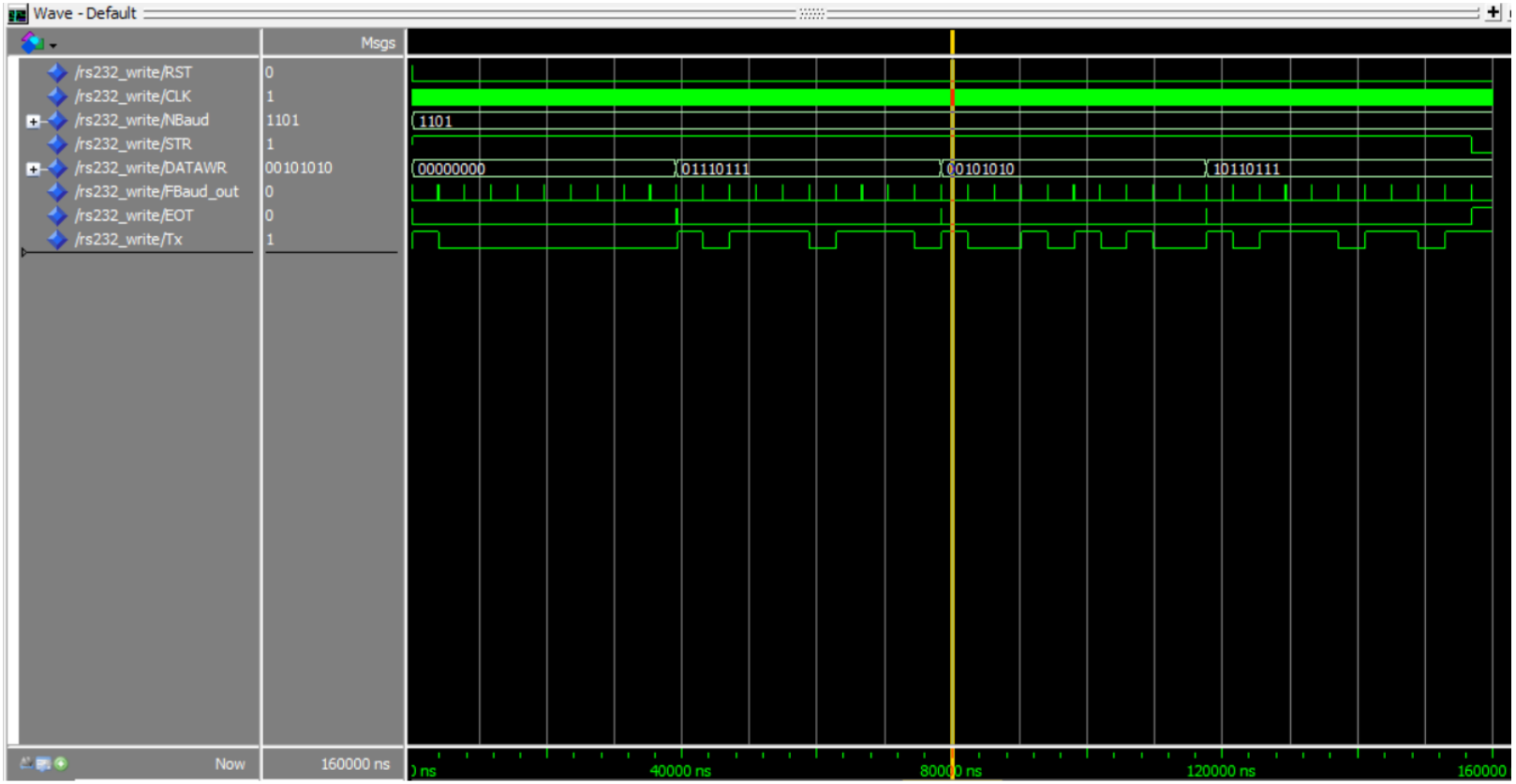
- Clock
- Reset
- Start
- Baudrate
- Data to send

Write module

- Simulation
  - RST (after 20 ns), CLK, Nbaud constant
  - DATAWR: the current byte that is written
  - FBaud_out: a wire that allows to see the value of internal signal Fbaud
  - EOT is ’1’ when a byte is fully written
  - Tx is the channel of transmission

Write module

❑ Simulation



Read module

- Source codes

4 codes manage the baudrate, the FSM, the buffer and the 7-segment application.

1 top level code links the 4 components.

Read module

- Test bench

Setting of the inputs:

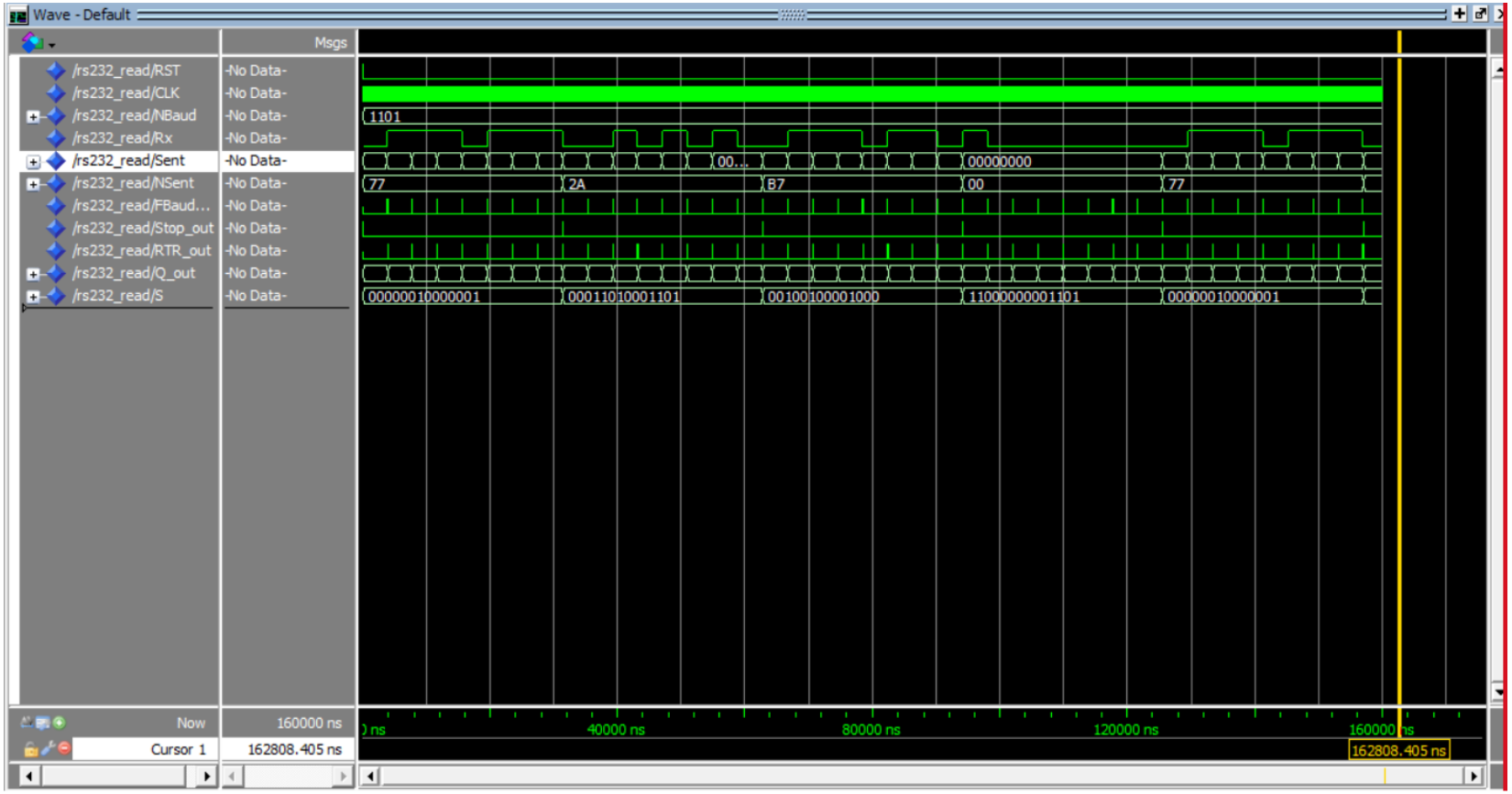
- Clock
- Reset
- Baudrate
- Rx

Read module

- Simulation
  - RST (after 20 ns), CLK, NBaud constant
  - Rx: the current bit received
  - Sent: the buffer containing the next bits to put in the channel
  - Nsent: the 8-bit value we want to read at the end of the byte transmission
  - FBaud_out (idem as write module, as well as for RTR_out, Stop_out and Q_out)
  - S is the 7-bit representation of what the 7-segments displays

Read module

- Simulation



Read module

- Simulation (zoom on a byte)