

Yangjia Hu

University of Science and Technology of China, 96 Jinzhai Road - 230026 Hefei - P.R.China
☎ (+86) 13688355505 | ✉ huyangjia@mail.ustc.edu.cn |

EDUCATION

University of Science and Technology of China	HeFei, AnHui, China
Junior Year, Major in Computer Science and Technology	Sep. 2022 – Present
<ul style="list-style-type: none">• GPA: 3.89/4.3• Arithmetic mean score: 90.55/100• Rank: 9/164	

RESEARCH EXPERIENCE

Optimization of FPGA-Based Control and Data Transmission for Piezoresistive Array Devices	
Supervisor: Prof. Xiaohui Cai, USTC	Nov 2023 - Dec 2024
<ul style="list-style-type: none">• Description: Optimized FPGA-based control systems and data transmission for piezoresistive array devices, focusing on improving data throughput, reducing latency, and enhancing real-time signal processing capabilities.• Contribution: Analyzed system performance to identify bottlenecks, optimizing resource utilization and efficiency. Including increasing data acquisition frequency from 40Hz to 80Hz and implementing a command frame control system.• Tech stack: SystemVerilog	
8th National College Students Computer System Ability Competition, CPU Track	
	May 2024 - Aug 2024
<ul style="list-style-type: none">• Description: Designed and implemented a sequential dual-issue 8-stage pipeline CPU, utilizing the AXI-4 bus protocol. Integrated components included ICache, DCache, a pre-decoder, and a branch predictor.• Contribution: Led the implementation of CPU architecture and performance optimization for stages prior to the Execute stage, focusing on critical components like FIFO and the pre-decoder. Contributed to the overall CPU design and verified functionality using SystemVerilog.• Tech stack: SystemVerilog	

ADDITIONAL EXPERIENCE

Rewriting Linux Kernel bpf_trace Module with Rust	
	Apr 2024 - Jul 2024
<ul style="list-style-type: none">• Led the translation and debugging of the Linux kernel's bpf_trace module from C to Rust, enhancing safety and performance by refactoring data structures and optimizing code, leveraging Rust and Make.	
Implemented a 2-issue out-of-order CPU(ongoing)	
Supervisor: Prof. Weng, KAUST	Dec 2024 - Present
<ul style="list-style-type: none">• Utilized a newly developed language from the lab to design and implement a high-performance CPU, exploring the potential and practical application value of this language in hardware design.	

SKILLS

<ul style="list-style-type: none">• Programming Languages: C/C++, Verilog, SystemVerilog, Java, Python• Tools: Git, Maven, Make, Verilator• Software: Vivado, Wireshark	
---	--

Awards and Honors

Excellent Student Scholarship Silver Award	2022
National Encouragement Scholarship	2023
3rd Prize in the National Finals of the 8th National College Students Computer System Ability Competition (CPU Track) - Team Award	2024
National Scholarship(Top 10%)	2024