Lab2: Exercises

EE332: Digital System Design

Objectives

The objectives of this laboratory are the following:

1. To understand delay in VHDL codes.
2. To understand the differences between the signal assignment and variable assignment.
3. To practice on the developing of test bench for both combinational and sequential circuits.
4. To become familiar with the structural coding style.
5. To investigate how the design affects the critical path of a circuit.
6. To practice on the sequential circuits, FSM, and FSMD design.
7. To understand and practice on pipeline design and parameterized design.

This lab includes 6 exercises.

Exercise 3: Design a tree 16-to-4 priority encoder
(Week 4, report due by noon, i.e., 12:00 noon, on 1 day before the week 6 class)

A priority encoder is a circuit that returns the codes for the highest-priority request. By using a conditional signal assignment or if statements to naturally describe this function, the shape of the specified priority network is a single cascading chain.

Prelab exercise:
Refer to the 4-to-2 priority encoder on Page 81, develop a VHDL code to realize a 16-to-4 priority encoder using a conditional signal assignment. The outputs of the encoder are a 4-bit code and a 1-bit activity flag. Sketch the conceptual implementation of the design.

During the lab:
To shape the layout of the circuit to a tree form so that to reduce the critical path of the designed 16-to-4 priority encoder.

Develop the block diagram of the design.
Based on the block diagram, develop the VHDL code of the design using component instantiation.
Do the simulation of the design.
Compare the layout and performance of the tree design with that of the cascading design.

A simple report is required for this exercise.
In the report, you may investigate your design from, but **NOT** limited to, the following aspects:
a. block diagrams and codes showing your design
b. Theoretical analysis of the critical paths of the two designs.
c. Simulated critical delays of the two designs, at different simulation modes.
d. The comparison, and if the comparison is consistent with your expectations? If not, what's the reasons?

Lab Report

The full report should include the following for each exercise:

1. Title
2. Introduction, including the objective of the laboratory. 10%
3. Pre-lab preparation results. 10%
4. Complete VHDL code and test bench code, and remarks for your codes. 20%
5. Results, including conceptual diagram (if not given elsewhere yet), waveform images, and data, tables if any, and remarks for the results. 10%
6. Your thinking and analysis to the results. 20%
7. Conclusions. 10%

If a report contains only a title, a VHDL code with resultant waveform images, the report will have not than 60 marks over 100 marks. Pre-lab preparation results and analysis to your results take heavy weight for high marks.

encoder