Chapter 3

Terminology and knowledge

3.1 Integrated semiconductor companies
Companies that design and fabricate integrated circuits

Fabless
With no fabrication/processing facility

Foundries
Companies that specialize in processing wafers to produce silicon devices

Wafer fab
Fabrication facility where wafers are processed to produce silicon devices

Integrated circuits
System of transistors manufactured on silicon wafers

CPU
Central processor unit that is an active part of computer containing the datapath and control

DRAM
Dynamic random access memory

Flat-panel displays
Display panels with flat screens

MEMS
Micro-electro-mechanical-system

DNA chips
Silicon chips used for DNA screening

Dry oxidation
Growth of SiO_2 using oxygen gas

Wet oxidation
Growth of SiO_2 using water vapor

Horizontal furnace
Horizontally oriented oxidation furnace

Vertical furnace
Vertically oriented oxidation furnace

Photolithography/Optical lithography
Process in which the resist is optically patterned and selectively removed from designated areas on a wafer

Wafer stepper
Equipment used in lithography process

Photoresist
Ultraviolet-light sensitive material

Photomask
Quartz photo-plate containing a copy of pattern to be transferred to Si or SiO_2 surface

Negative resist
Photoresist that becomes polymerized and resistant to a developer when exposed to an UV light

Positive resist
Photoresist whose stabilizer breaks down when exposed to an UV light, leading to the preferential removal of exposed regions in a developer

Strip
Removal of photoresist

Asher
System that removes the resist on a wafer by oxidizing it in oxygen plasma or UV ozone system

Lithography field
Small area exposed to an UV light during the exposure through a photomask and an optical reduction system

Stepper
Another name for lithography equipment

Step-and-repeat action
The process of exposing different parts of a wafer until the whole wafer has been exposed

Phase-shift photomask
Photomask that produces 180 degree phase difference in neighboring clear features so that their diffraction fringes cancel each other

Optical Proximity Correction (OPC)
Printing a slightly different shape on the photomask to correct distortions resulting from an exposure process

Overlay
Alignment between 2 separate lithography steps

Extreme UV lithography (EUVL)
Lithography that uses 13nm wavelength and is expected to result in much higher resolution

Soft-x-ray lithography
Old name of EUVL

Electron-beam lithography (EBL)
Lithography using a focused stream of electrons

Electron projection lithography (EPL)
EBL that exposes a complex pattern simultaneously using a mask and a reduction electron lens system

Wet etching
Removal of SiO_2 using hydrofluoric acid

Isotropic
Without preference in direction

Dry etching (also known as plasma etching or reactive-ion etching (RIE))
Removal of SiO_2 using plasma and reactive ions

Anisotropic
With preference in direction

Selectivity
The extent in which an etching process distinguishes between different materials

End-point detector
Detector that monitors the emission of characteristic light from the etching products so as to signal when etching should end

Plasma process induced damage / Wafer charging damage
Damage to devices on wafers due to the use of plasma

Antenna Effect
Sensitivity of the damage to the size of the conductor

Ion implantation
Method of doping in which ions of impurity are accelerated and shot into the semiconductor surface

Gas-source doping
Method of doping in which a gas reacts with silicon and liberates phosphorus so that phosphorous diffuses into the silicon substrate

Solid-source diffusion
Method of doping in which the dopants from the thin film coated on the silicon surface diffuse into silicon

Anneal
Heating of wafers for dopant activation and damage removal

Dopant activation
Making dopants behave as donors and acceptors by heating the wafers

Implantation dose
Total number of implanted ions/cm^2

Depth/ Range
The location of peak concentration below the surface of silicon

Straddle
Spread of dopant concentration profile

3.2 Diffusion
The movement of molecules from an area of high concentration to an area of low concentration

Junction depth
Thickness of diffusion layer

Diffusivity
Constant that describes how quickly a given impurity diffuses in silicon for a given furnace temperature

Predeposition
Portion of diffusion process step with the source present

Drive-in
Portion of diffusion process step without the source

Furnace annealing
Heating of wafers in a furnace for dopant activation and damage removal

Rapid thermal annealing (RTA)
Annealing process in which a wafer is rapidly heated to high temperature and cooled quickly down to the room temperature

Rapid thermal oxidation
Oxidation process in which a wafer is heated to the designated temperature quickly, oxidized, and then cooled rapidly down to the room temperature

Rapid thermal chemical vapor deposition (CVD)
Chemical vapor deposition process in which a wafer is heated to the designated temperature quickly, the material is deposited on the wafer, and the wafer is cooled rapidly down to the room temperature

Laser annealing
Annealing process in which a silicon wafer is heated with a pulsed laser

Transient enhanced diffusion (TED)
Diffusion phenomena in which diffusion rate is increased by crystal damage due to ion implantation

Interconnect
Metal connection between devices in integrated circuits

Inter-metal dielectrics
Materials used for electrical isolation between metal layers

Crystalline
Molecular structure with nearly perfect periodicity

Polycrystalline
Molecular structure composed of densely packed crystallites or grains of single-crystals

Amorphous
Structure with no atomic or molecular ordering

Grain boundary
Interface between crystal grains

Thin-film transistors (TFT)
Transistors made of amorphous or polycrystalline silicon, widely used in flat-panel displays

Sputtering target
The source material for sputtering

Reactive sputtering
Sputtering accompanied by chemical reaction of sputtered ions. For example, Ti sputtered in nitrogen gas forms TiN film on the Si wafer

Physical vapor deposition (PVD)
Another name for sputtering

Step coverage problem
The inability of sputtering to deposit uniform films in small holes or vertical features on wafer

High-temperature oxide (HTO)
Very conformal oxide formed by a CVD process at a high temperature

Low-pressure chemical vapor deposition (LPCVD)
CVD process at low pressure, which yields good thickness uniformity and low gas consumption

Plasma-enhanced chemical vapor deposition (PECVD)
CVD using plasma; low deposition temperatures

In-situ doping
Doping process in which dopant species are introduced during the CVD deposition of polycrystalline silicon

Spin-on
Process in which liquid materials are spun onto the wafer

Epitaxy
Special type of thin-film deposition technology that produces a crystalline layer on silicon surfaces that is an extension of the underlying semiconductor crystal arrangement

Metallization
Interconnection of individual devices by metal lines

Via/ Plug
Electrical connection between adjacent metal layers

Electromigration
Migration of metal along the crystal-grain boundaries in a quasi-random manner, causing voids to occur in metal interconnects

Damascene process
Process used to form copper interconnect lines

Chemical-mechanical polishing (CMP)
Process in which a polishing pad and slurry are used to polish away material and leave a very flat surface

Back-end process
Metallization; last step of IC fabrication

Front-end processes
Oxidation, diffusion

Planarization
Process to obtain a flat surface to improve lithography and etching

Multi-chip modules
Multiple chips put into one package

Solder bumps
Electrical connection between chip and package

Flip-chip bonding
Melting pre-formed solder bumps on IC pads to make all connections simultaneously

Burn-in
Subjecting IC packages to higher than normal voltage and temperatures; identify potential failures

Qualification
Routine used to verify the quality of manufacturing and reliability

Operation life test
Part of qualification process; to find out if the devices last over one thousand operating hours

3.3 (a) Lithography field
A small area having the best optical resolution (The beam intensity is uniform within a lithography field.)
(b) Misalignment
Layer to layer mismatch (Each new mask level should be aligned to one of the previous levels)
(c) Selectivity

The ratio of etching rate of the film to be etched to that of the substrate film below

(d) End-point detection
Detecting the exposed substrate film after the removal of the desired film.

(e) Step coverage
The ratio of film thickness deposited on the flat surface to that deposited on the non-flat surface.

(f) Electromigration
The movement of atoms in a metal film due to momentum transfer from the electrons carrying the current.

3.4 (a) Wet. Otherwise, it would take too long to grow the thick oxide.

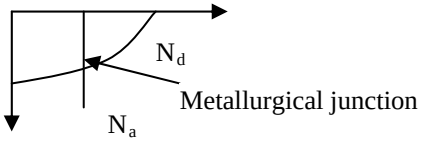
(b) Dry because it provides better control of the gate (channel) length and vertical wall profile.

(c) Arsenic because
- it is a donor ion (group V),
- it reduces R_p and ΔR_p, and
- it reduces diffusivity.

(d) PECVD

(e) Sputtering, dry etching, plasmas containing chlorine.

(f)



Oxidation

3.5 Wet oxidation is faster than dry oxidation because the solid solubility of H_2O steam into SiO_2 is higher than that of O_2 gas into SiO_2. This creates a very sharp concentration profile that causes H_2O to diffuse towards the SiO_2-Si interface much more effectively than O_2 under the same conditions.

3.6 (a) $\tau = \dfrac{0.2um * 0.2um + 0.165um * 0.2um}{0.0117um^2 / hr} = 6.239hr$

Solving the given equation for t_{ox} and using quadratic formula,

$$T_{ox} = \frac{-A + \sqrt{A^2 + 4B(t+\tau)}}{2} = 0.256um\,.$$

(b) Linear approximation: $T_{ox} \approx \dfrac{B}{A}(t+\tau)$ => 0.655um (156% error).

Quadratic approximation: $T_{ox}^2 \approx B(t+\tau)$ => 0.320um (25% error).

In this case $A \approx T_{ox}$, neither linear nor quadratic approximations would be valid.

Deposition

3.7 Poly Silicon:

$SiH_4 \rightarrow Si(s) + 2H_2$

Silicon Nitride:

$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$

LTO:

$SiH_4 + O_2 \rightarrow SiO_2 + 2HCl + 2H_2$

HTO:

$SiH_2Cl_2 + 2H_2O \rightarrow SiO_2 + 2HCl + 2H_2$

Diffusion

3.8 (a) $x_j = \sqrt{Dt} \Rightarrow x_j + \Delta x_j = \sqrt{Dt + \Delta(Dt)}$

$x_j^2 + 2x_j\Delta x_j + (\Delta x_j) = Dt + \Delta(Dt) = x_j^2 + \Delta(Dt)$

$2x_j\Delta x_j + (\Delta x_j) = \Delta(Dt)$

Since $x_j >> \Delta x_j$,

$2x_j\Delta x_j \approx \Delta(Dt) \quad \Rightarrow \quad \Delta x_j \approx \dfrac{\Delta(Dt)}{2x_j}$.

(b) For boron,

D(500K) = 10.5×Exp[-3.69/(8.614×10-5×773)]cm2/sec = 9.0×10^{-24} cm^2/sec, and 500 years = 1.58×10^{10} sec.

Hence,

$\Delta x_j = 1.42\times10^{-13} cm = 1.42\times10^{-9} \mu m$.

Our assumption ($x_j >> \Delta x_j$) in part (a) is correct.

3.9 (a) Junction depth is distance from surface where the dopant concentration equals the substrate concentration.

$N_{sub} = N_d = N_{junction} = 10^{15} cm^{-3}$ (Required junction dopant concentration)

From Eq. (3.6.1),

$N_{junction} = \dfrac{N_0}{\sqrt{\pi Dt}} e^{-x_j^2/4Dt} = 10^{15} cm^{-3}$

Using

$D = D_0 e^{-E_a/kT}$, $D_0 = 10.5 cm^2/\sec$, $N_0 = 10^{15} cm^{-2}$, *and* $E_a = 3.7eV$,
$X_j = 1.97 \times 10^{-4} cm$.

(b) X_j has the form

$$X_j = 2\sqrt{Dt}\left[\ln\left(\frac{k}{\sqrt{Dt}}\right)\right]^{1/2}.$$

Taking the derivative,

$$\frac{dX_j}{dDt} = \frac{1}{\sqrt{Dt}}\left\{\left[\ln\left(\frac{k}{\sqrt{Dt}}\right)\right]^{1/2} - \frac{1}{2\left[\ln\left(\frac{k}{\sqrt{Dt}}\right)\right]^{1/2}}\right\} = \frac{X_j}{2Dt} - \frac{1}{X_j}.$$

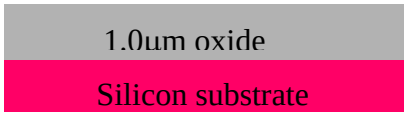
$$\frac{dX_j}{dDt} = \frac{1.98 \times 10^{-4}}{2 \times 10^{-9}} - \frac{1}{1.98 \times 10^{-4}} = 9.39 \times 10^4 cm^{-1}$$

$$\Delta Dt = 10.5 e^{\frac{-3.70}{373}} . (10^6)(3600) = 3.996 \times 10^{-40} cm^2$$

Hence, $\Delta X_j = \frac{\partial X_j}{\partial Dt} . \Delta Dt = 3.75 \times 10^{-35} cm \approx 0.$

Visualization

3.10 (a)



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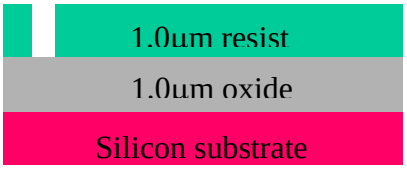

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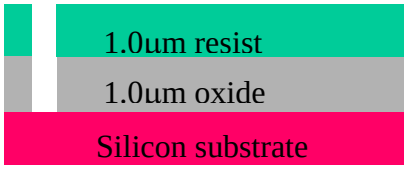

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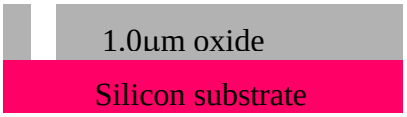

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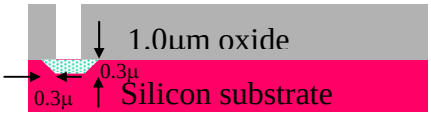

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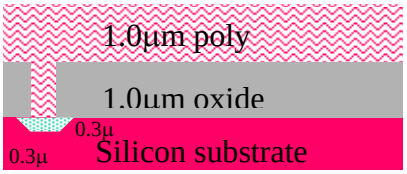
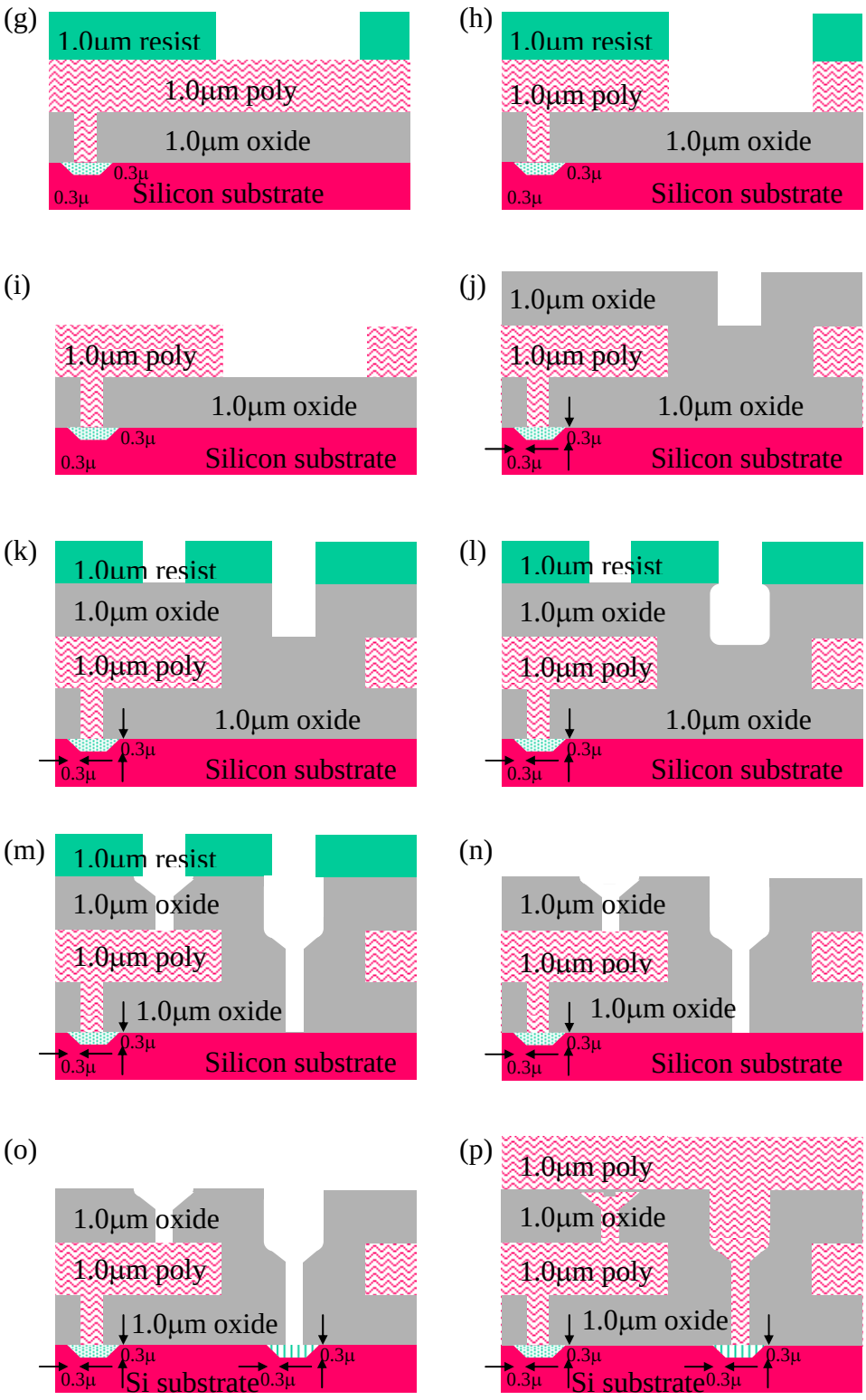
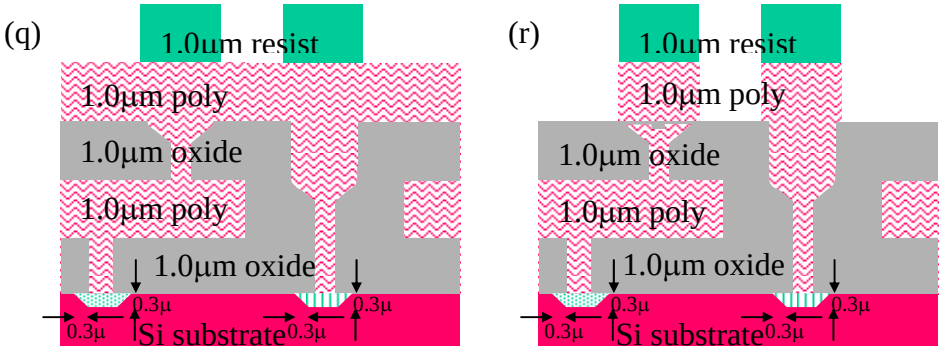
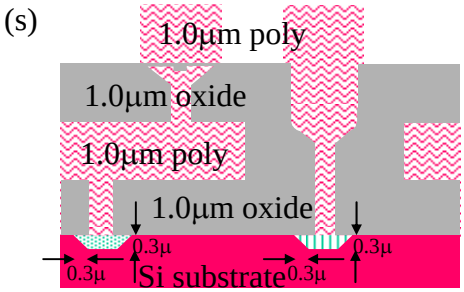
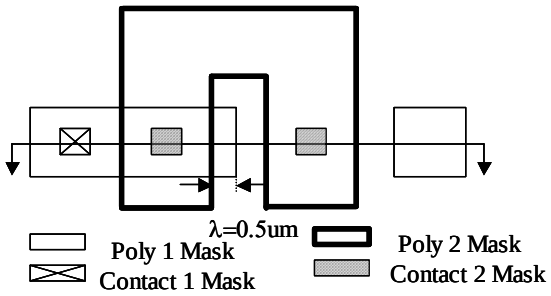


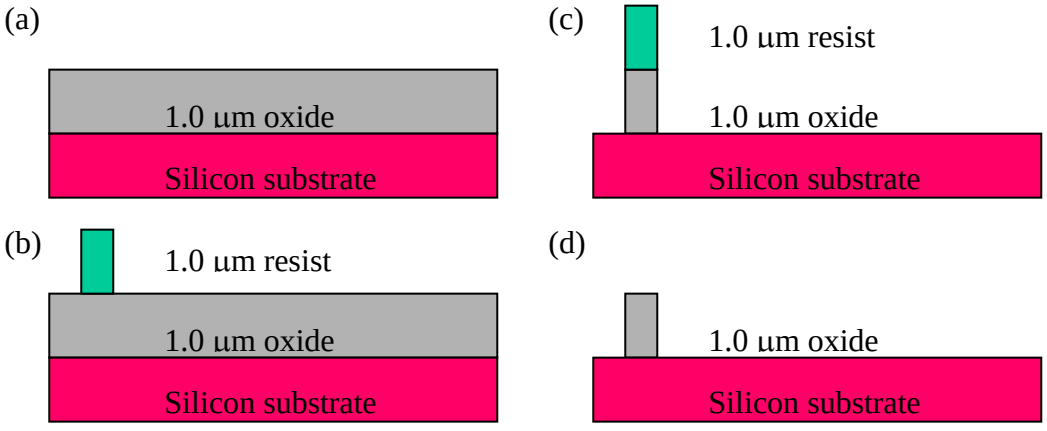






3.11





Changing the polarity of the contact 1 mask results in the same cross section as problem **3.10** (d). The same cross-section is obtained by using a negative resist and the reversed mask of contact 1, which is opaque in the inside of contact 1 area.