Chapter 7

Subthreshold Leakage Current

7.1 a) Cox=3.45E-13/11E-8 = 3.138uF/cm^2
Vt = -1.04 + 0.95 + Qdep/Cox = -1.04 + 0.95 + 0.180 = 0.109V

b) S = 60(1+Cdep/Cox) = 60(1+2.953E-7/3.138E-6) = 65.64mV/dec

c) 1/S = [log(W/L*100nA) – log($I_{leakage}$)]/Vt
$I_{leakage}$ = 121nA

Field Oxide Leakage

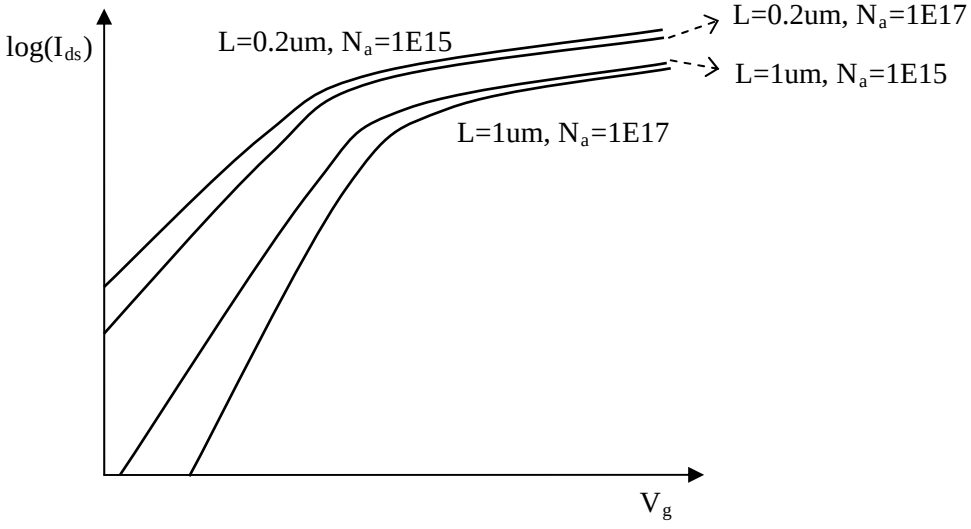
7.2 a) Cox=3.45E-13/0.3E-4 = 1.151E-8F/cm^2
Vt = -1.01 + 0.92 + Qdep/Cox = -1.01 + 0.92 + 33.96 = 33.87V

b) S = 60(1+Cdep/Cox) = 60(1+2.119E-7/1.151E-8) = 1164.6mV/dec

c) 1/S = [log(W/L*100nA) – log($I_{leakage}$)]/Vt
$I_{leakage}$ = 2.81E-26nA

Vt Roll-off

7.3



Trade-off between I_{off} and I_{on}.

7.4 i) Larger V_t : Decrease I_{off} and decrease I_{on}
ii) Larger L : Decrease I_{off} and decrease I_{on}
iii) Shallower junction : Decrease I_{off} and somewhat decrease I_{on}
iv) Smaller V_{dd} : Decrease I_{off} and decrease I_{on}
v) Smaller T_{ox} : Decrease I_{off} and increase I_{on}
A smaller T_{ox} contributes to leakage reduction and increases the precious I_{on}.

7.5
There is a lot of concern that we will soon be unable to extend Moore's Law. In your own words explain this concern and the concerns for high I_{on} and low I_{off}.

(a) Answer this question using 1 paragraph of less then 50 words. : Methods of manufacturing very small objects such as photolithography will run into limitations. Transistors may not be able to provide circuit functions with high speed and low power. Specifically, means of increasing speed (I_{on}) tend to worsen leakage (I_{off}). Other relevant comments include the following. V_t must not be too low because of subthreshold current but small L reduces V_t. Since I_{on} (speed) is roughly proportional to V_{gs}-V_t (V_{dd}-V_t), I_{on} and speed can not be raised by lowering V_t especially because V_{dd} needs to be reduced to reduce the power consumption.

(b) Support your description in (a) with 3 hand drawn sketches of your choice. : Possible choices are Log(I_{ds}) vs. V_{gs} , Vt vs. L and Vds, Ion vs. Ioff, gate leakage vs. Tox, etc.

(c) Why is it not possible to achieve high I_{on} and small I_{off} by picking optimal T_{ox}, X_j, W_{dep} etc? Please explain in your own words.: Decreasing T_{ox} is good for Ion but bad for I_{off}. So is increasing X_j. W_{dep} is basically fixed by the choice of T_{ox} and V_t.

(d) Provide three equations that help to quantify the issues discussed in part (c). : Some relevant equations include Eq. (6.9.14), Eq.(6..10.1), (7.2.8), Eq.(7.3.3), Eq.(7.5.2).

7.6 (a) Final equation:

$$l_d \propto \sqrt[3]{\frac{\varepsilon_{ox}\left(V_t - V_{fb} - 2\phi_B\right)}{qN_a} X_j} = \sqrt[3]{\frac{X_j T_{ox} T_{oxe} 2\varepsilon_s 2\phi_B}{\varepsilon_{ox}\left(V_t - V_{fb} - 2\phi_B\right)}}$$

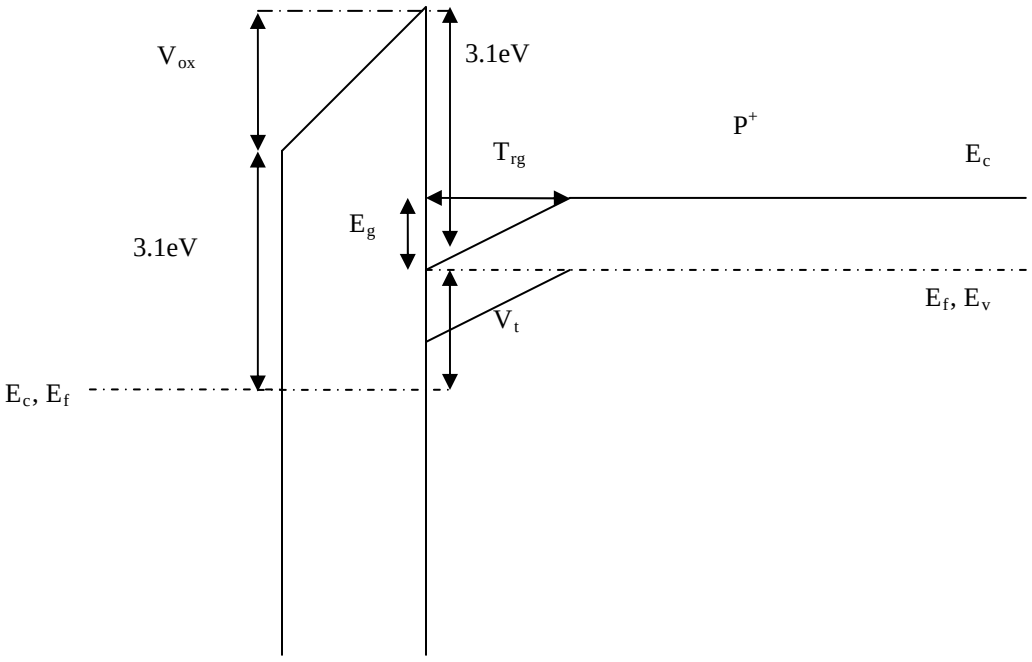
(b) The minimum acceptable L is several times of *ld***.** In order to support the reduction of L at each new technology node, ld must be reduced in proportion to L. According to the derived equation, in order to reduce the minimum acceptable channel length, $\left(V_t - V_{fb} - 2\phi_B\right)$ should be increased by gate workfunction engineering, Xj can be decreased, and the oxide permittivity can be increased .

7.7 (a) A smaller W_{dep}
Reduces DIBL (V_t is not as low) → decreases I_{off}

(b) $I_{dsat} = \dfrac{W}{2mL} C_{oxe} \mu_{ns} \left(V_{gs} - V_t\right)^2$ where $m \equiv 1 + \alpha = 1 + 3T_{oxe} / W_{dmax}$
Reducing W_{dep} increases m which decreases I_{dsat}.

MOSFET with Ideal Retrograde Doping Profile

7.8 (a)



(b) The figure above assumes that the gate is N+ polysislicon and the substrate (below the undoped layer) is P+ silison. In that case , it can be seen that $V_t = V_{ox}$. In general, V_t is determined by Eq. (5.2.2) and

$$V_t = V_{fb} + \varphi_{st} + V_{ox}$$

Note – You need to apply a positive gate bias to reach inversion. Thus the Fermi level of the poly gate is below the Fermi level of the substrate and the difference is V_t.

(c) $\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_{si}\mathcal{E}_{si}$

$$\varepsilon_{ox} \frac{V_{ox}}{T_{ox}} = \varepsilon_{si} \frac{\phi_{st}}{T_{rg}} \approx \varepsilon_{si} \frac{E_g / q}{T_{rg}}$$

The last equality is the result of a further approximation for ϕ_{st}. Using the result of part (b),

$$\therefore\ V_t = V_{fb} + \phi_{st} + \phi_{st} \frac{\varepsilon_{si} T_{ox}}{\varepsilon_{ox} T_{rg}}$$

(d) First derive Eq. (7.5.2) using Eq. (7.5.1) and eq. (5.5.1). By comparing Eq. (7.5.2) and Eq. (7.5.3) one concludes that, for the same Vt, the depletion region width of the "ideal retrograde doping" MOSFET (Trg) is half of that of a MOSFET with uniformly doped substrate.

(e) A small W_{dep} reduces the V_t roll-off caused by DIBL which in effect decreases I_{off}.

(f) $I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_{ns} \left(V_{gs} - V_t\right)^2$ where $m \equiv 1 + \alpha = 1 + 3T_{oxe} / W_{dmax}$

Reducing W_{dep} increases *m* which decreases I_{dsat}.
A smaller I_{dsat} causes a longer inverter delay. However, it is important to reduce W_{dmax} so that L can be reduced to increase the device integration density and to reduce chip cost. I_{dsat} and speed still get improved due to the reduction in L.