Imperial College
London

MSc Project Interim Report

Sikan Sun (01099224)

Real-time Face Super-Resolution *Supervisor* Dr. Christos Bouganis

March 30, 2016

Contents

1 Introduction

1.1 Project Specification

The technique of face super-resolution (SR, aka face hallucination) is convert the noisy or low-resolution facial images into high-resolution images using knowledge about typical facial features. This technique can be applied in facial recognition systems (e.g. smart surveillance cameras) for identifying faces faster and more effectively. Currently, the existing image hallucination methods are mainly fall into two categories: reconstruction-based techniques and learning-based techniques. In this project, it focus on learning-based method as it can generate batter performance and higher magnification factor. The learning-based method investigated in this project is a simple and effective scheme called Locality-constrained Representation (LcR) proposed by J. Jiang. For a real-time application, it requires to design an embedded system with the implementation of this advanced algorithm, and the embedded system is designed with FPGA in this project.

1.2 Aims and Objectives

As the development of smart surveillance system rapidly, it requires high-resolution (HR) facial images for comparing with the images in the database to identify the suspects. Modern embedded systems are often based on microcontrollers (with on-chip memory and peripherals) and ordinary microprocessors (with external chips for memory and peripherals interface), but in recent years, FPGAs are used in microprocessor-based embedded systems for glue logic or for off-loading the processor from tasks that require fast updates. The advantages of using FPGA rather than using single-chip microcontroller (MCU) in an embedded system are FPGA can provides approximately 1000 times of logic gates and bits of memory (RAM) more than a single-chip MCU. The aims of this project are design an embedded system using FPGA and implement the existing SR algorithm (LcR) in the designed embedded system. The objectives of this projects are set an database, investigate the SR algorithm of LcR, implement it in Matlab and determine the design parameters (i.e. regularisation parameter τ, patch width, overlap), optimise the efficiency of the existing algorithm, implement it in ARM processors (C/C++) on ZedBoard (Zynq SoC) and FPGA mapping for acceleration.

2 Project Background

2.1 Super-Resolution Algorithm

Recently, the approaches based on *position-patch* have been proposed to replace the probabilistic graph based or manifold learning based models for face SR techniques. There are three *position-patch* based schemes have been proposed, the Least Square Representation (LSR), the Sparse Representation (SR) and the Locality-constrained Representation (LcR), and this project is focus and investigate the last approach.

The approach of position patch based face hallucination is create a database includes a set of training face images denoted as Y^m, $m = 1, 2, ..., M$, and M is the number of samples. Each face image is divided into N small overlapping patch sets $\{Y^m(i,j)|1 \leq i \leq U, 1 \leq j \leq V\}$, $N = UV$, U is the patch number in every column and V is the patch number in every row, and the coordinate (i,j) indicates the position of the patch as shown in Figure 1. For the patch at (i,j), it can be represented by M training samples located at the same position with a weight vector, $w(i,j) = [w_1(i,j), w_2(i,j), ..., w_M(i,j)]$.

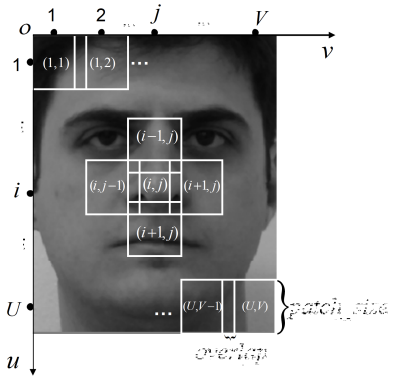

Figure 1: Position patch based approach

The Euclidean distance between the LR test image $X_L(i,j)$ and the LR training image Y_L^m is

$$d_m(i,j) = \|X_L(i,j) - Y_L^m(i,j)\|_2,\ 1 \le m \le M \tag{1}$$

The objective of this scheme is to minimise the reconstruction and locality error

$$\min \|d(i,j) \circ w(i,j)\|_2^2,\ s.t. \|X(i,j) - \sum_{m=1}^{M} Y^m(i,j) w_m(i,j)\|_2^2 \le \varepsilon,\ \sum_{m=1}^{M} w_m(i,j) = 1 \tag{2}$$

The Lagrangian for equation (2) can be written as:

$$w^*(i,j) = \arg\min_{w(i,j)} \left\{ \left\| X(i,j) - \sum_{m=1}^{M} Y^m(i,j) w_m(i,j) \right\|_2^2 + \tau \sum_{m=1}^{M} [d_m(i,j) w_m(i,j)]^2 \right\} \tag{3}$$

2.2 FPGA Implementation

In this project, the FPGA development kit specified is the ZedBoard for the Xilinx Zynq-7000 All Programmable SoC, which running on the ARM dual-core Cortex-A9 MPCore Processing System (PS) and interacting with the tightly coupled 7 series 85K Programmable Logic (PL) cells.

3 Project Schedule

Table 1: Project plan

Project Tasks / Milestones	Time Frame
Understand the algorithm of LcR	Spring Term
Setting database	Spring Term
Implement LcR in Matlab	Spring Term
Determine design parameters	Spring Term
Optimise LcR algorithm	Spring Term/Easter Break
Implement in ARM processor (C/C++)	Easter Break
Exams in May	
Implement in FPGA platform	Summer Term
Optimise and acceleration in FPGA	Summer Term
Testing and performance evaluation	Summer Term