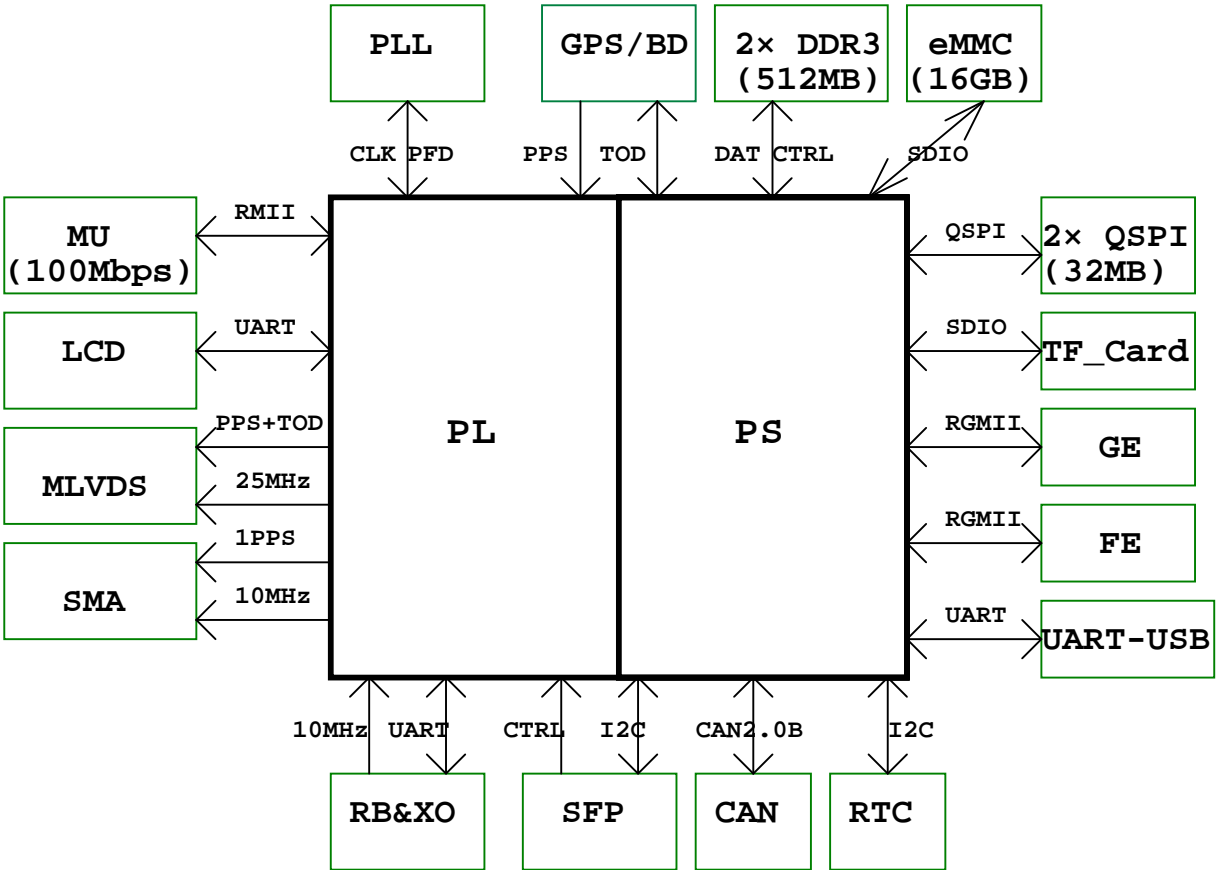


Schematics of TFSE

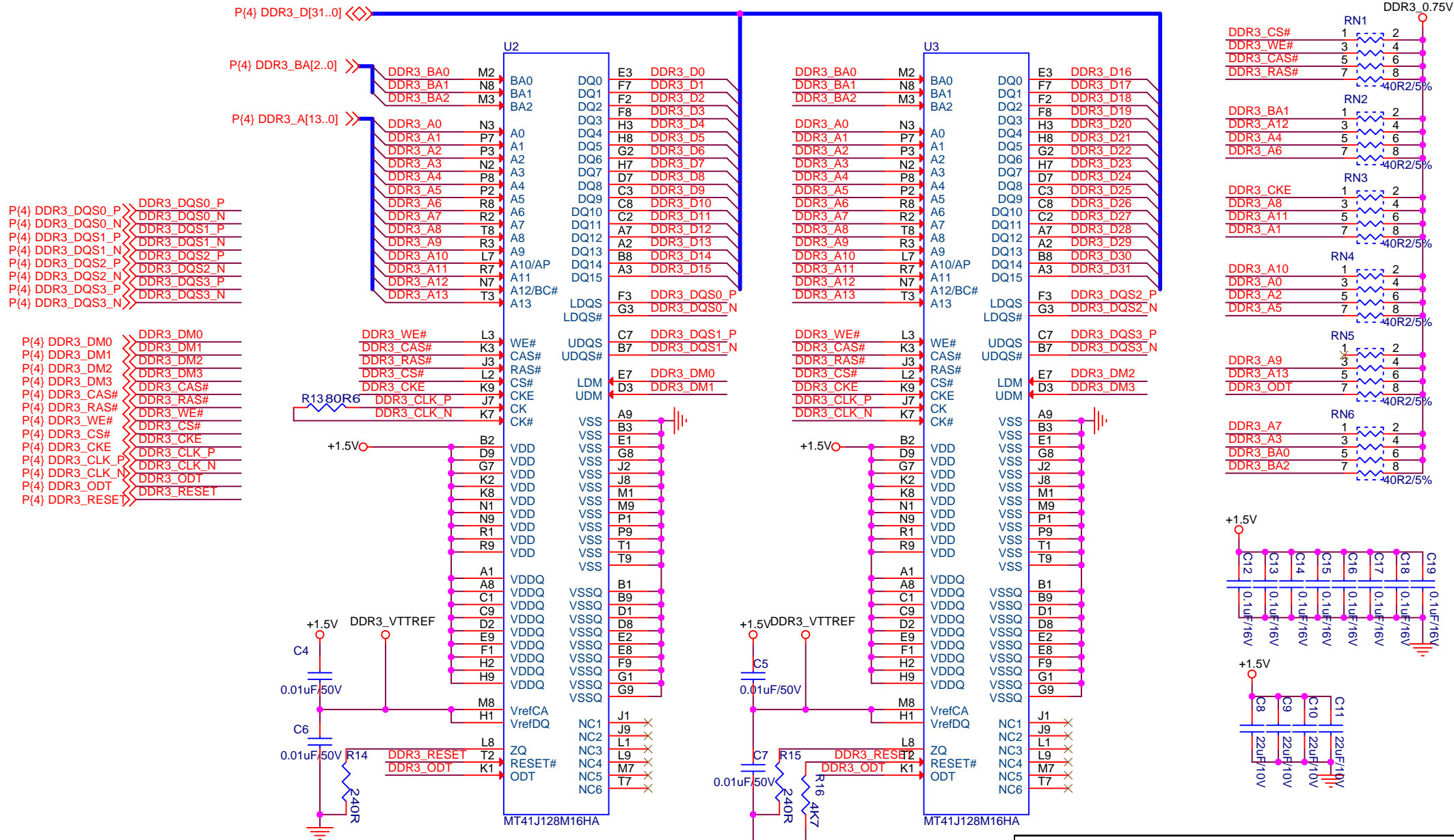
REV	Description	DATE	BY
V0.1	First Draft	2017-4-8	HCX



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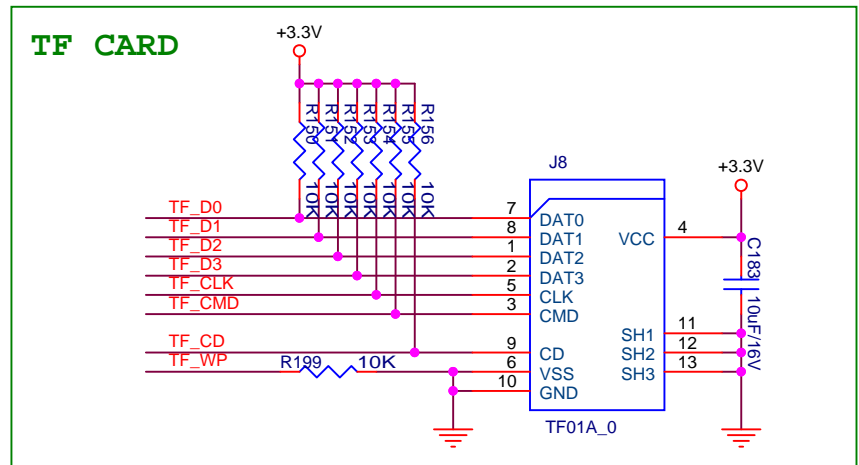
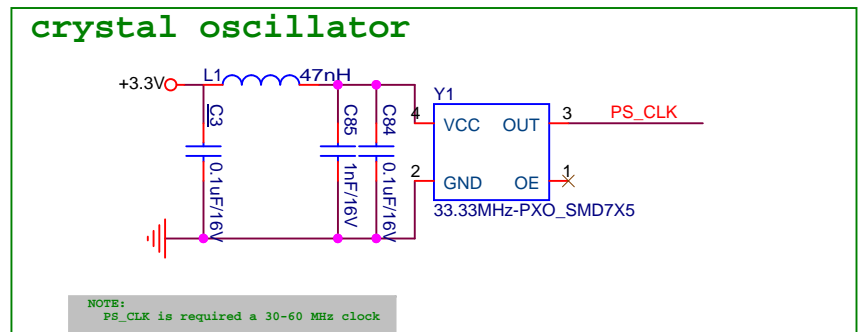
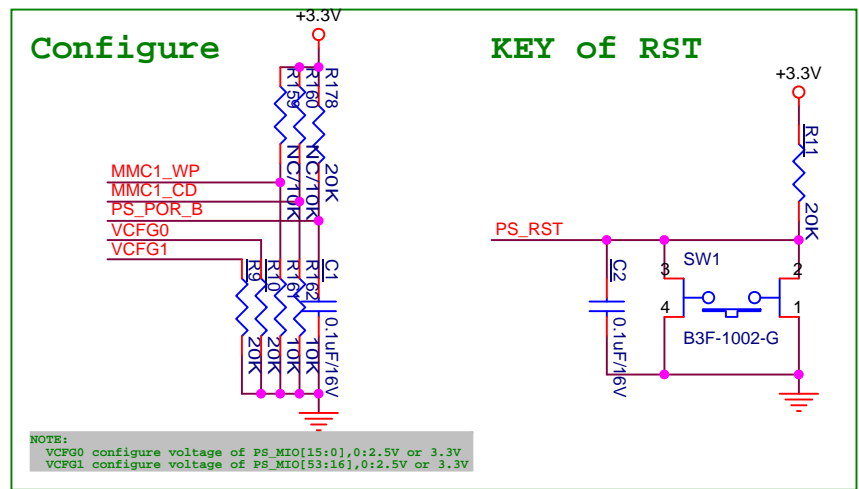
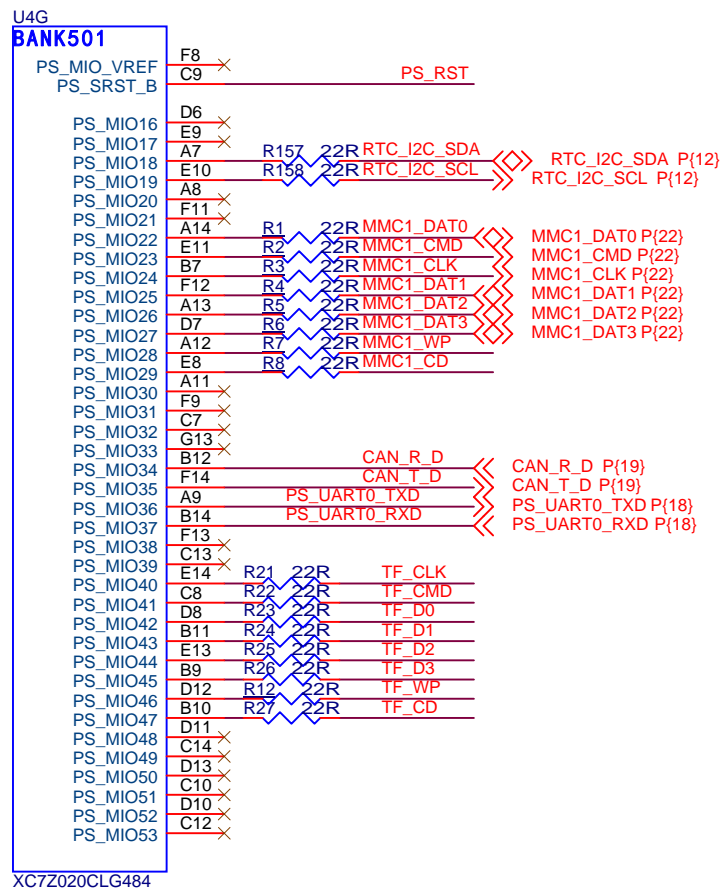
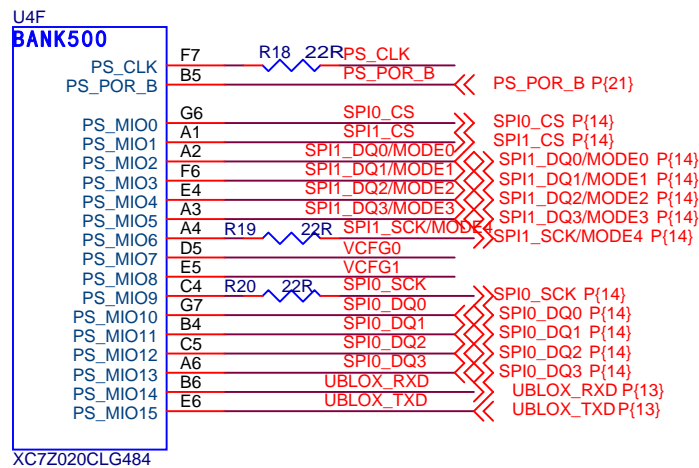
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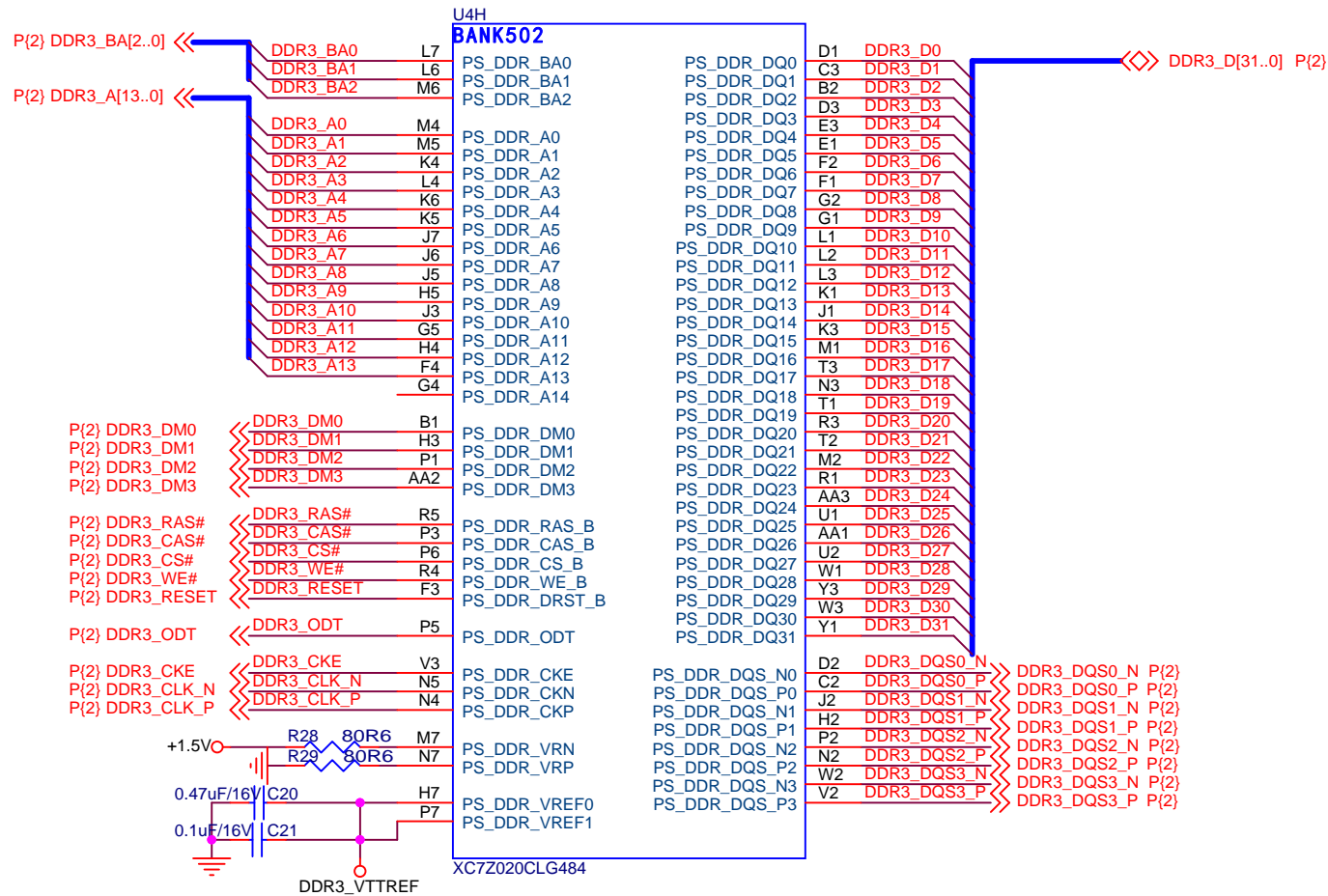


Note1:DDR3-RESET is pulled up to VTT in PTG,but pulled down to GND in Datasheet

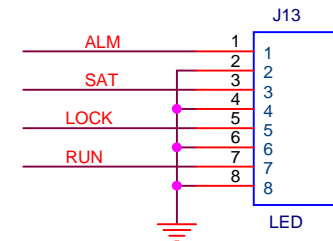
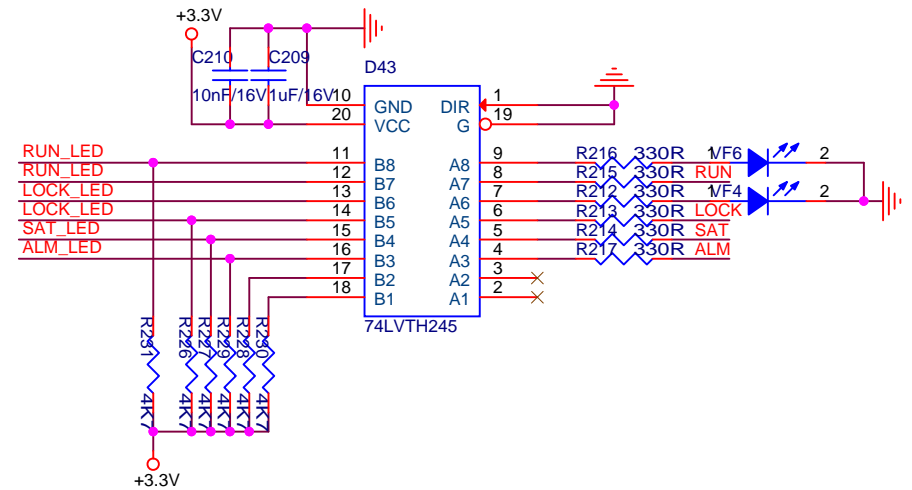
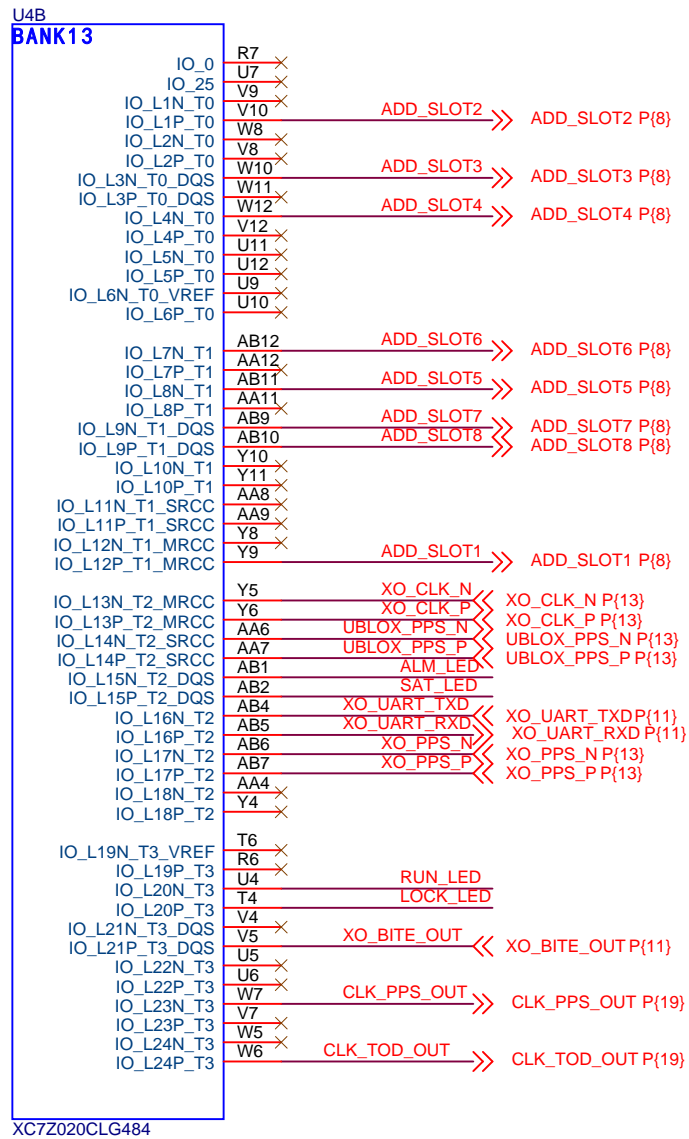
Note2:VrefCA don't need to pulled up to +1.5V by C2 in new Demo-Board, but it does in PTG

TFSE			
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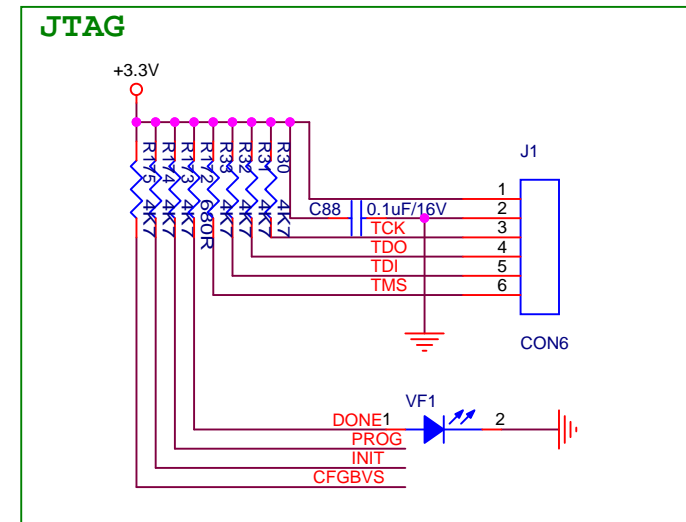
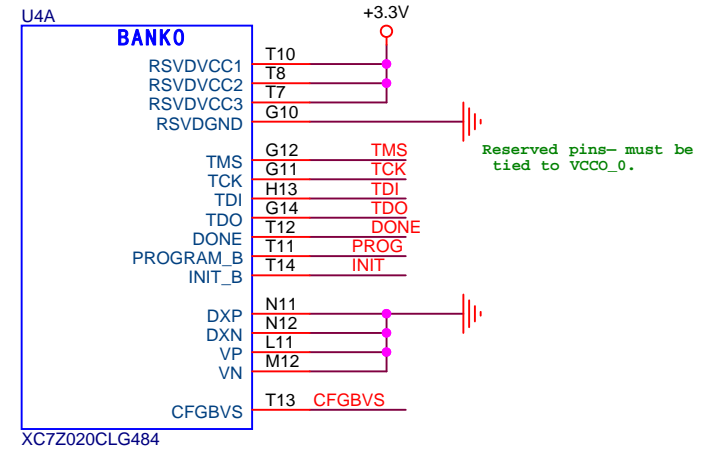
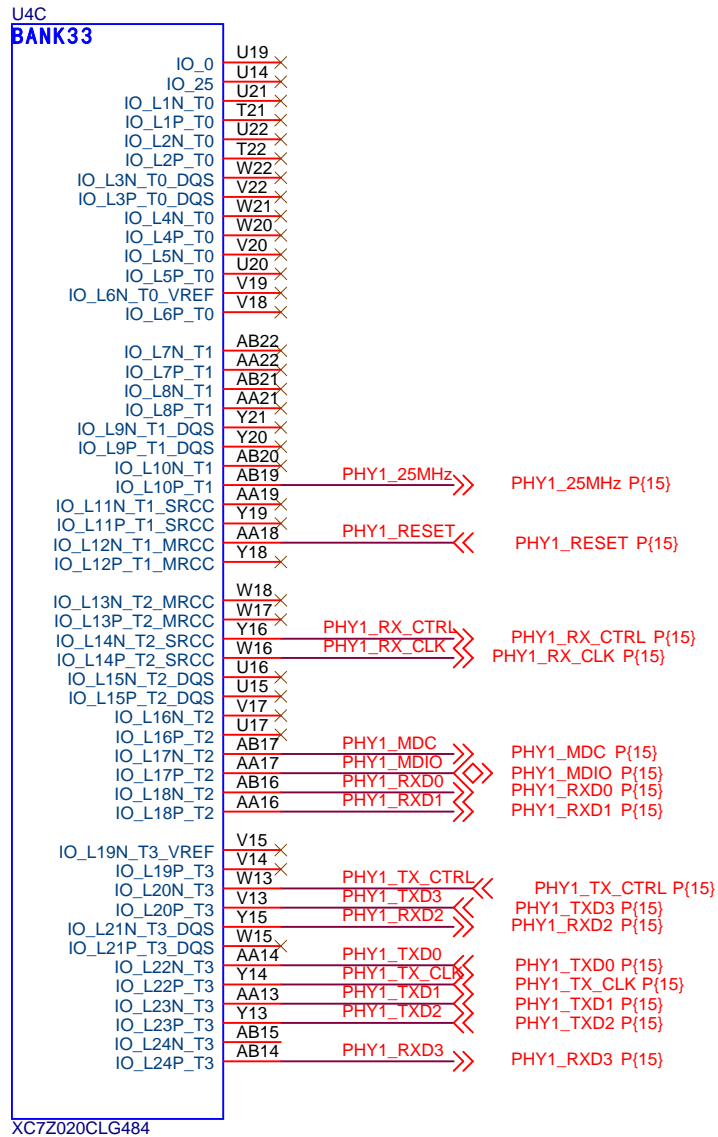




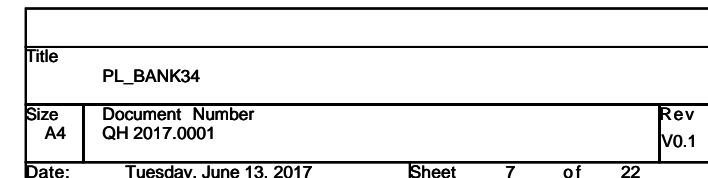
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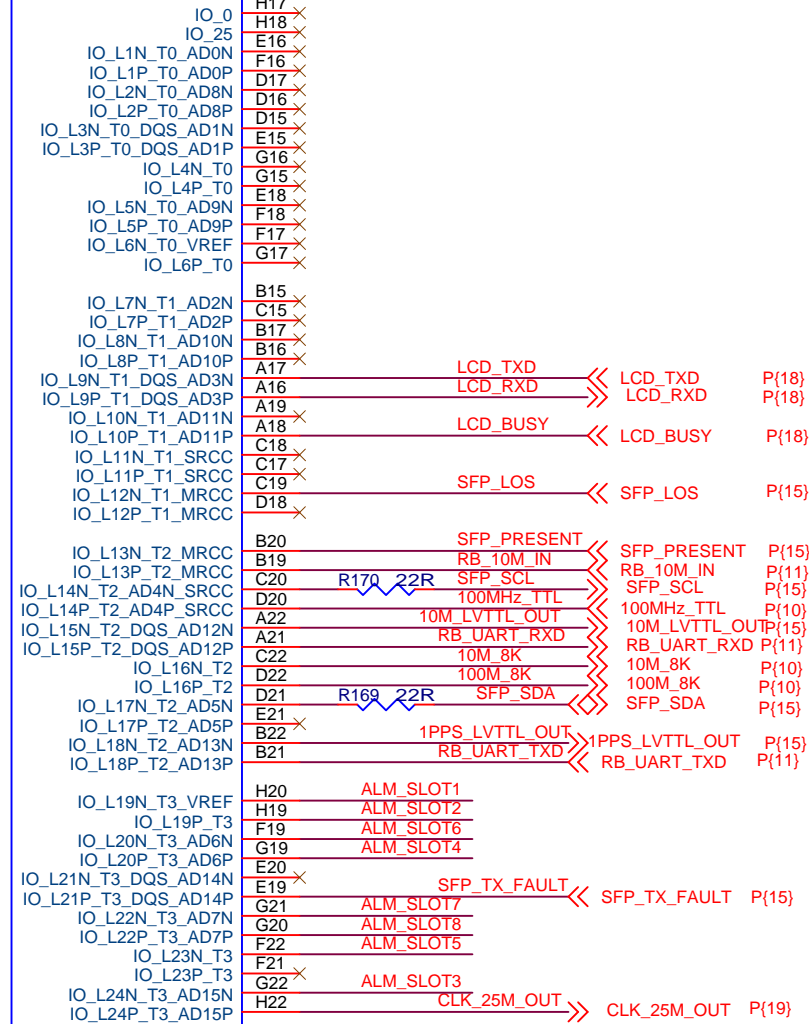
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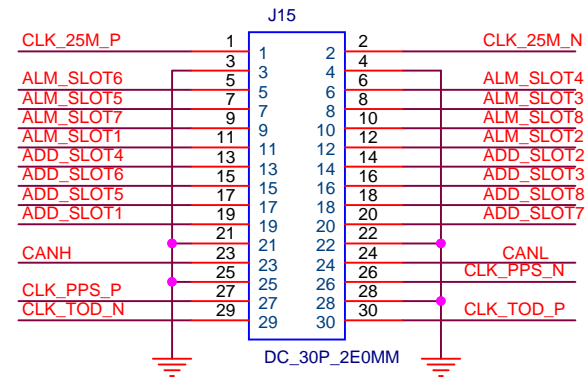
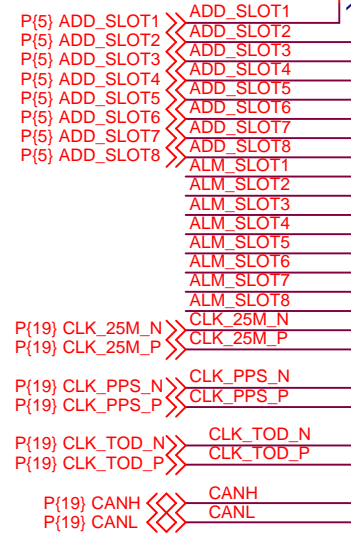
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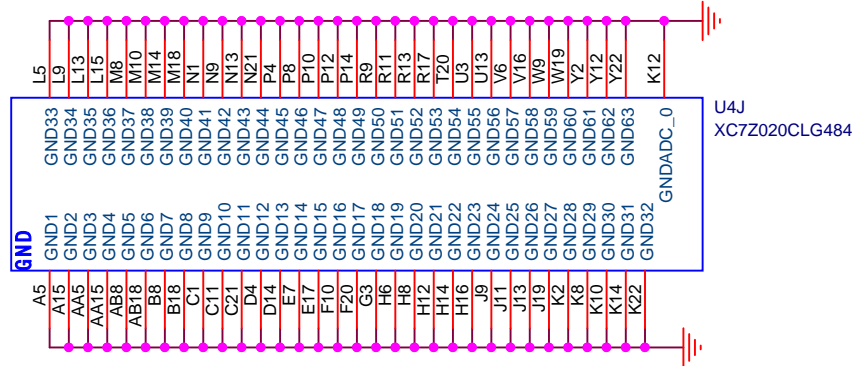
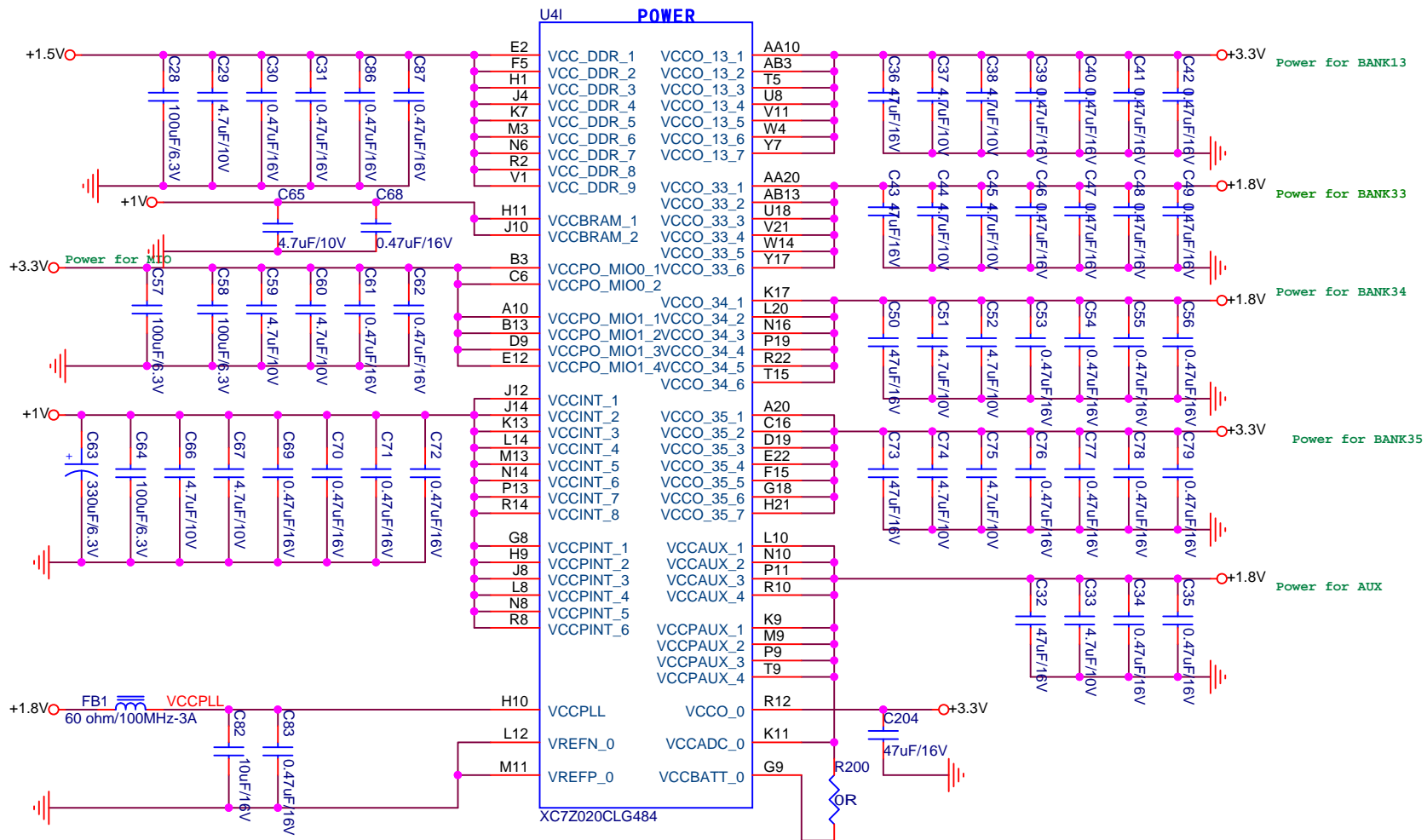
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BANK35

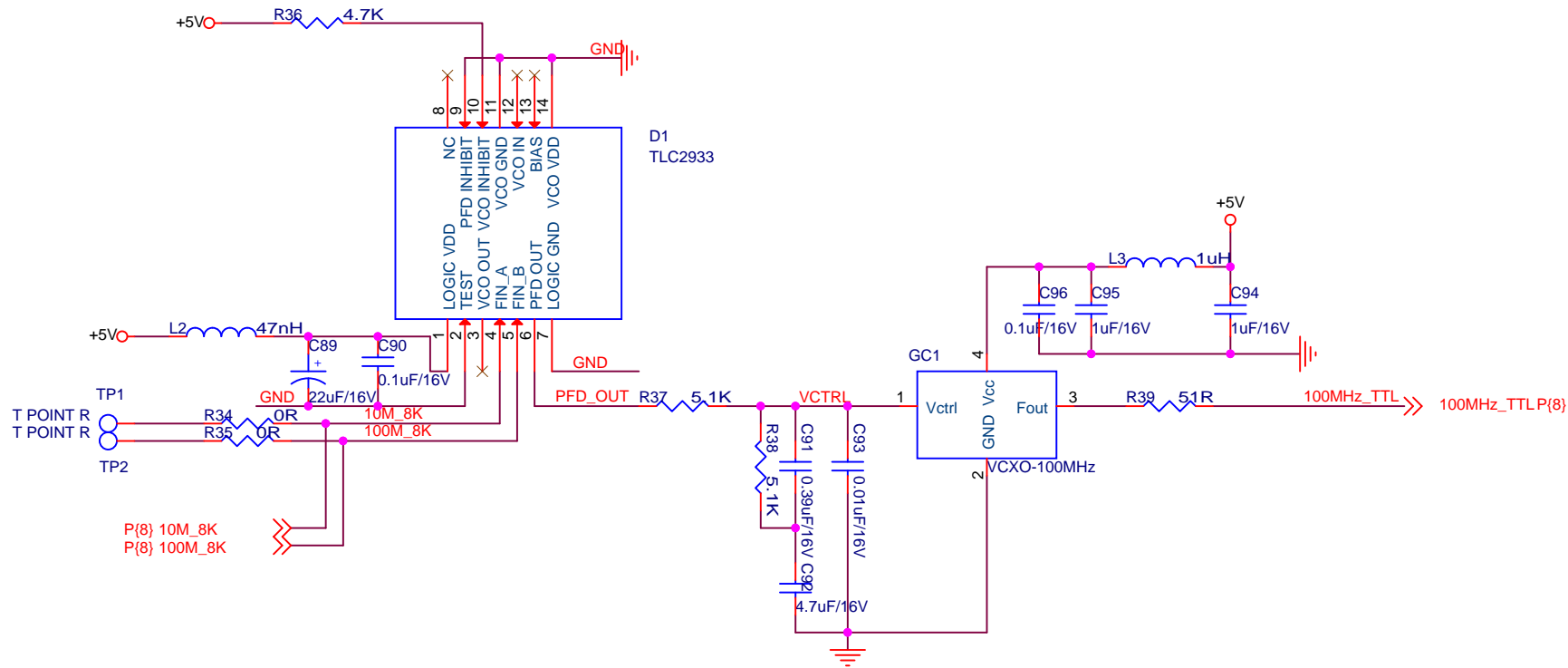


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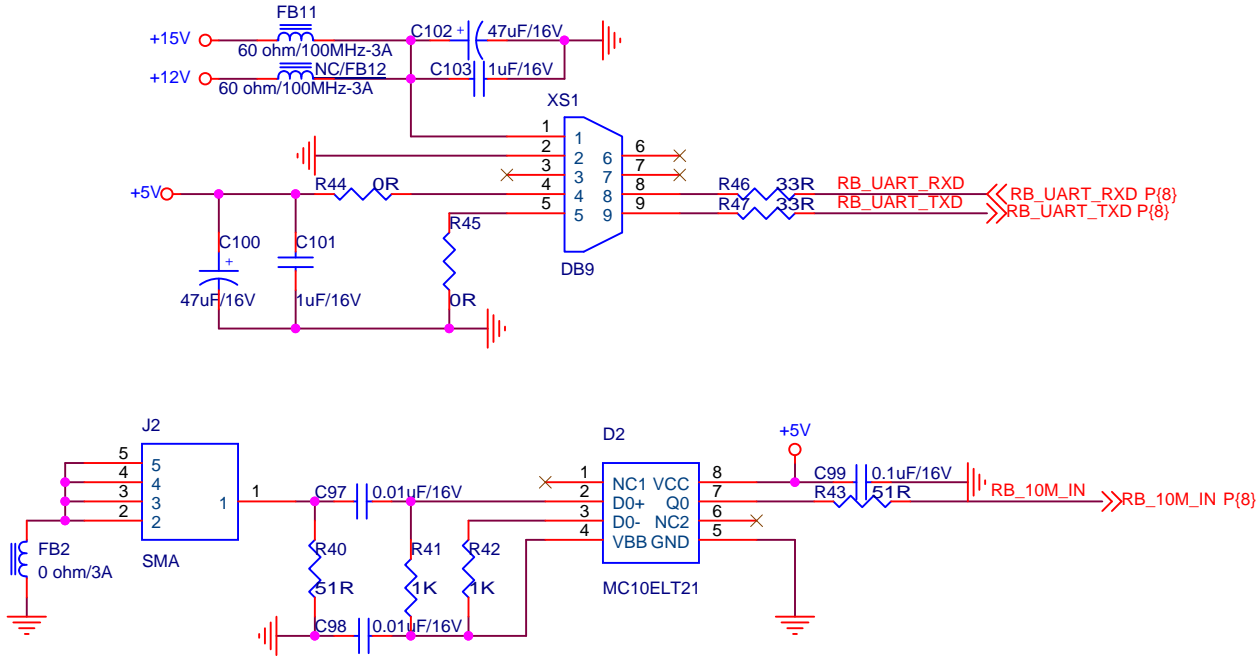
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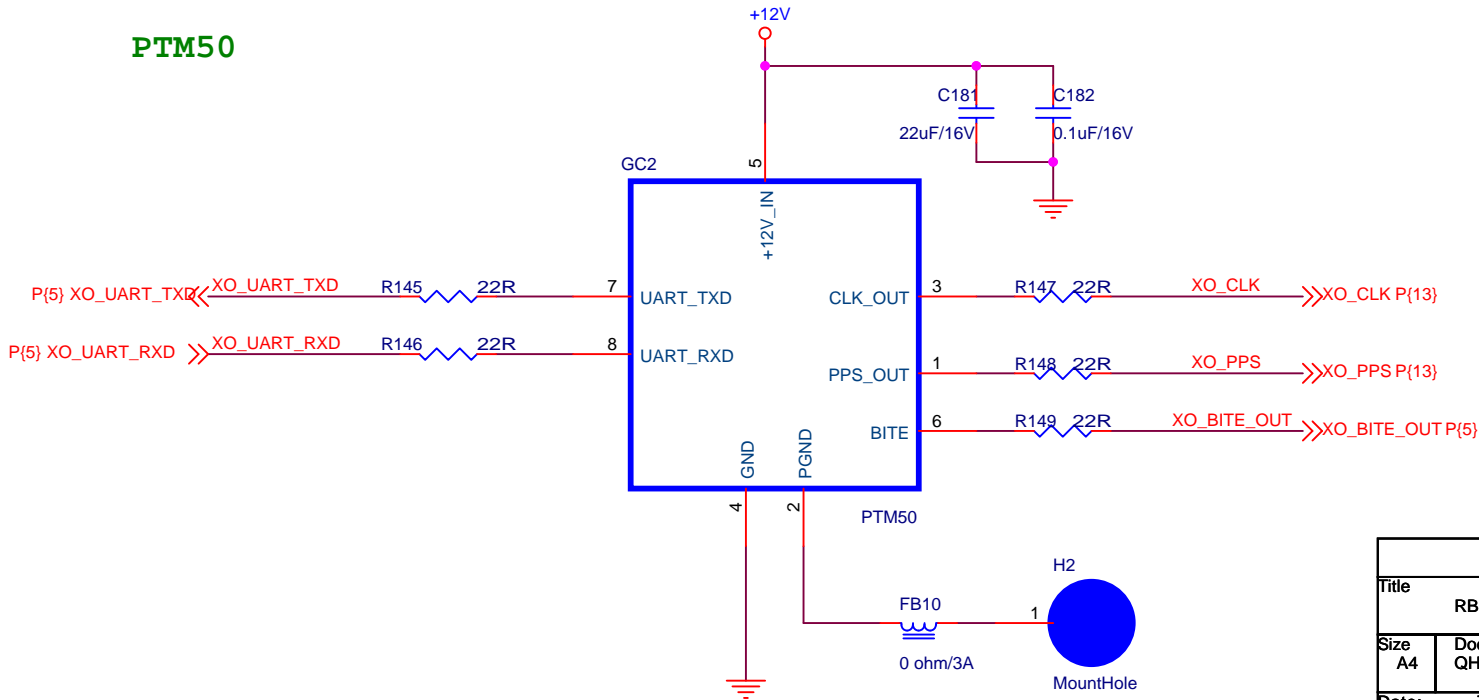


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RB

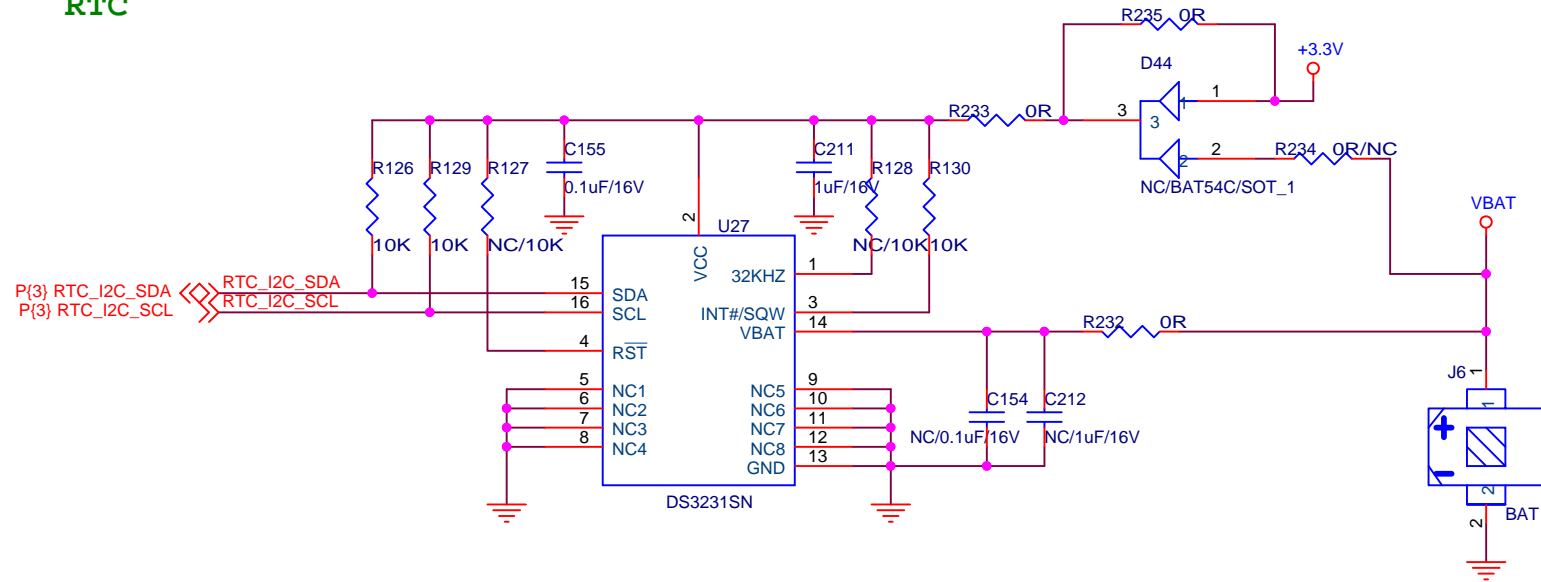


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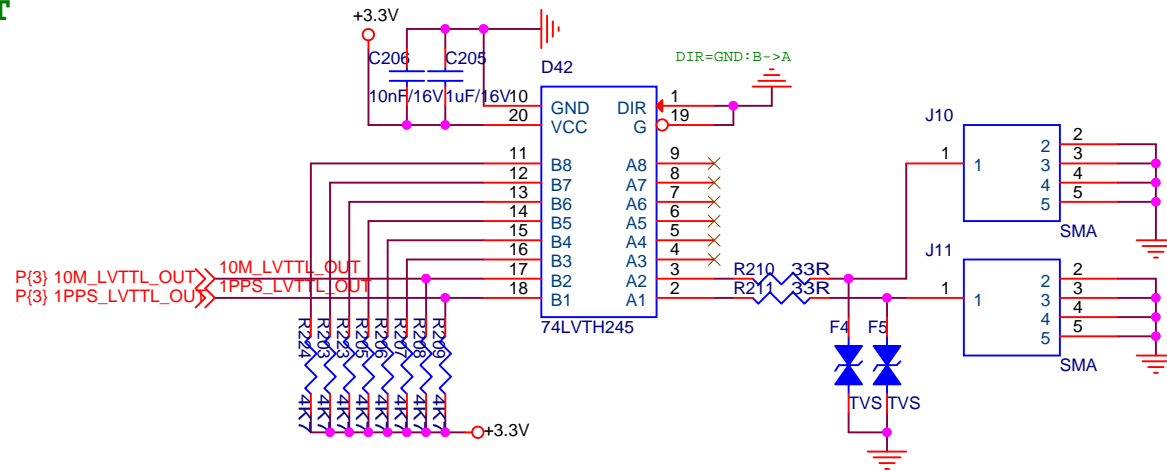


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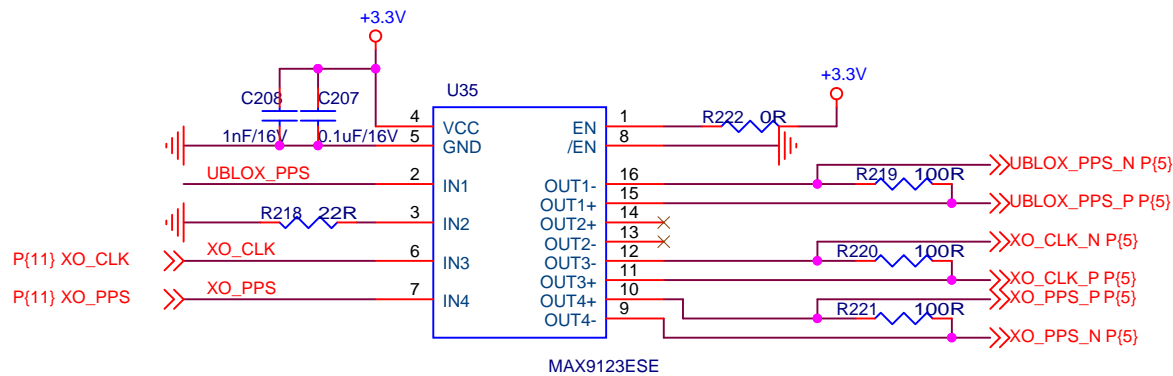
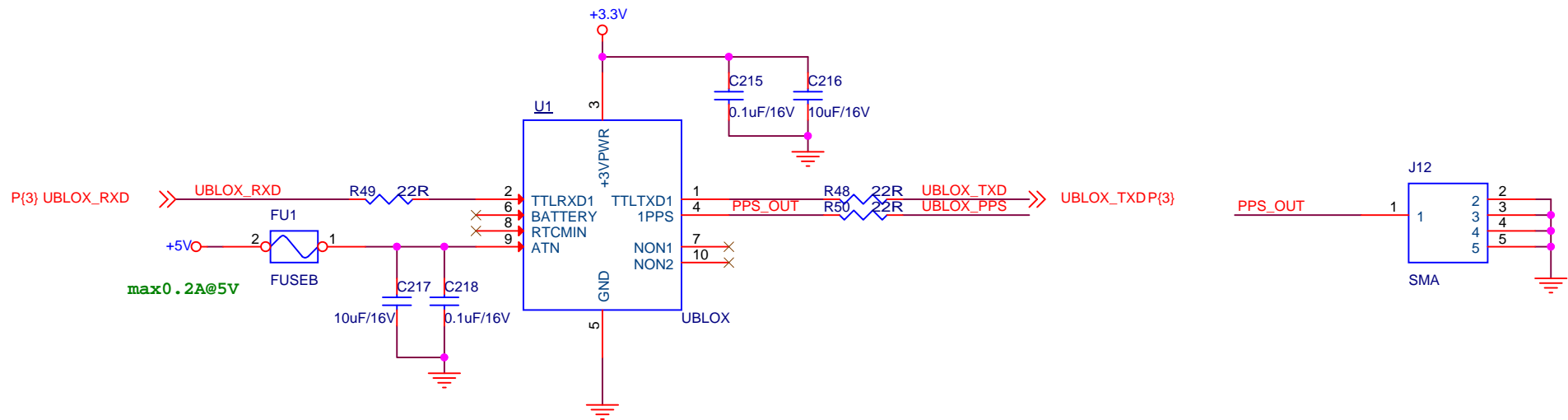
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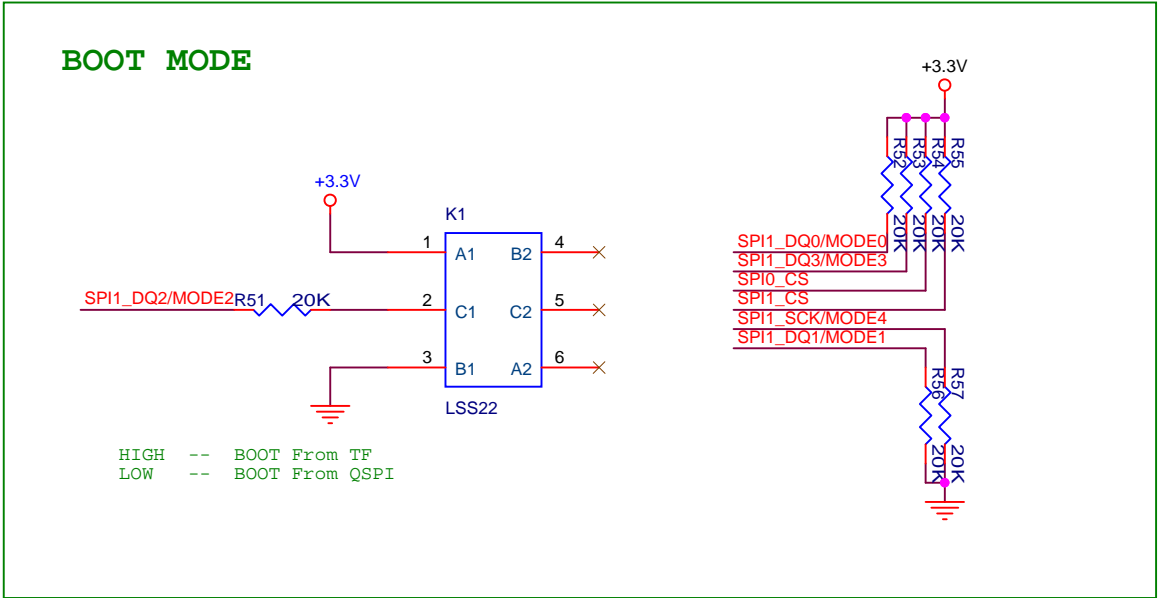
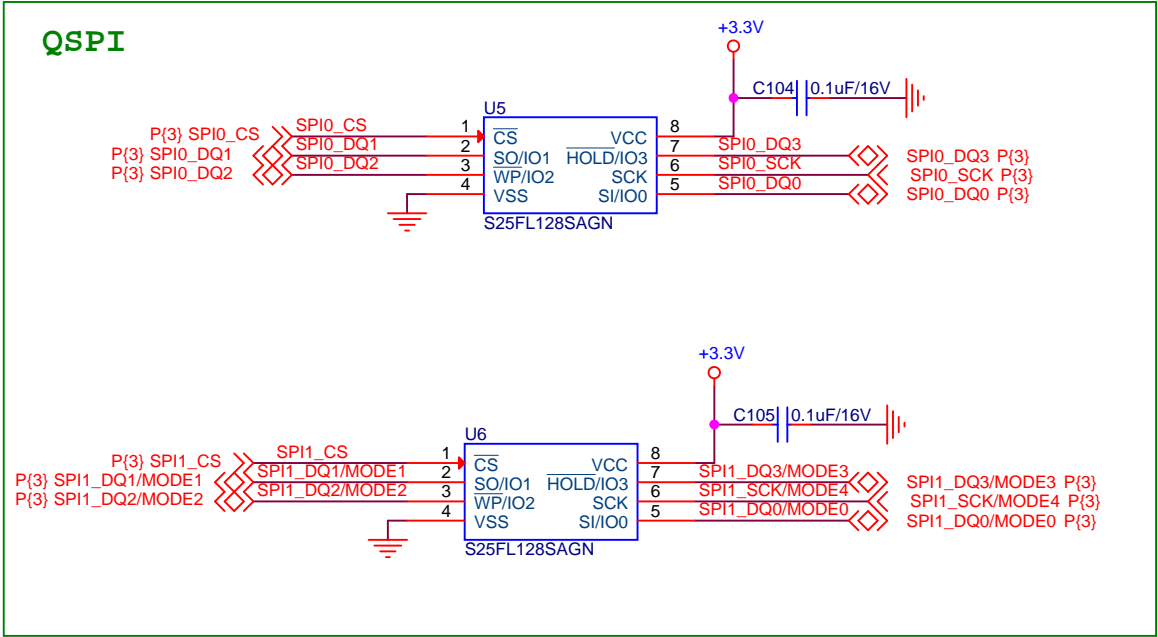
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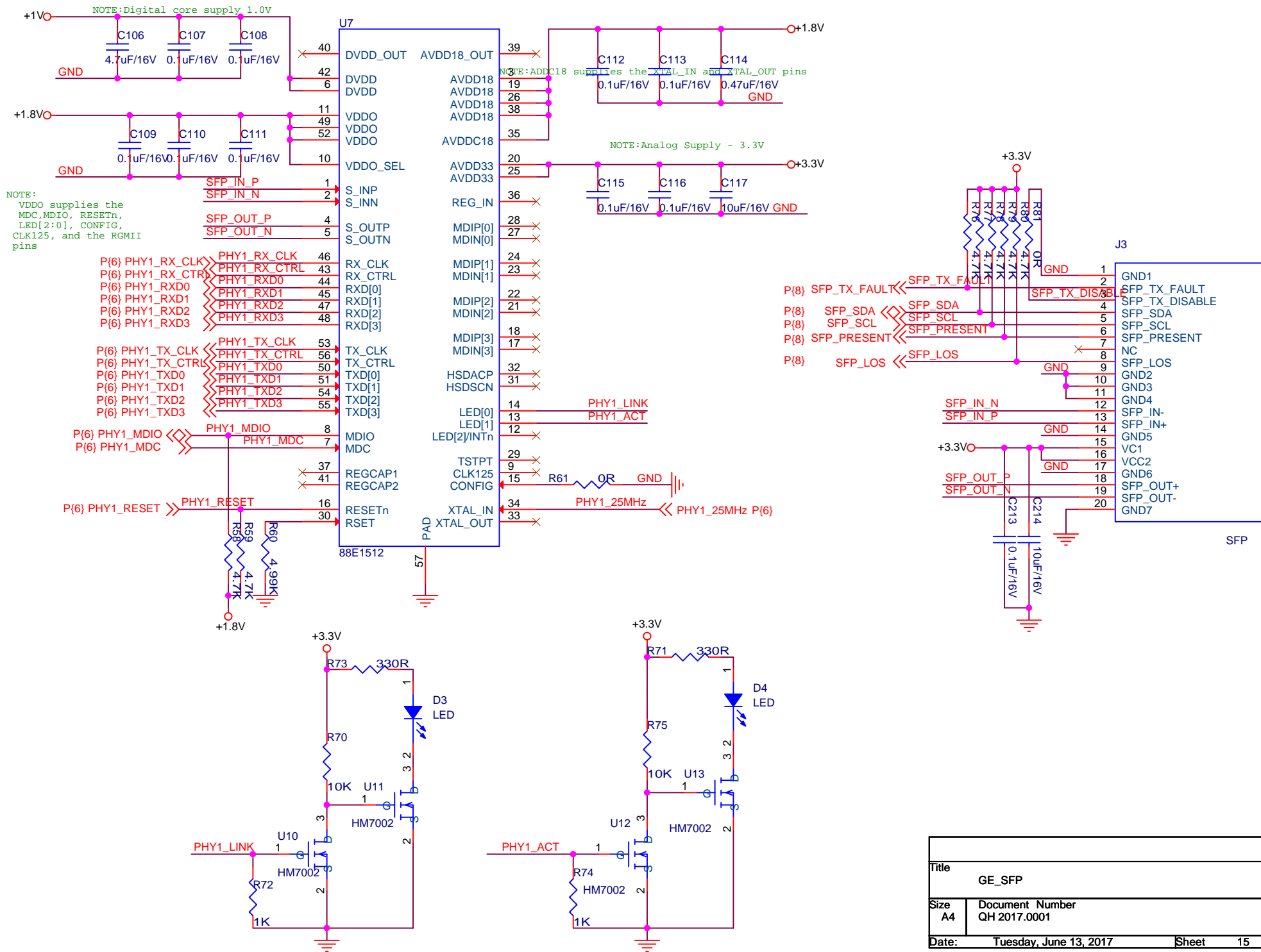
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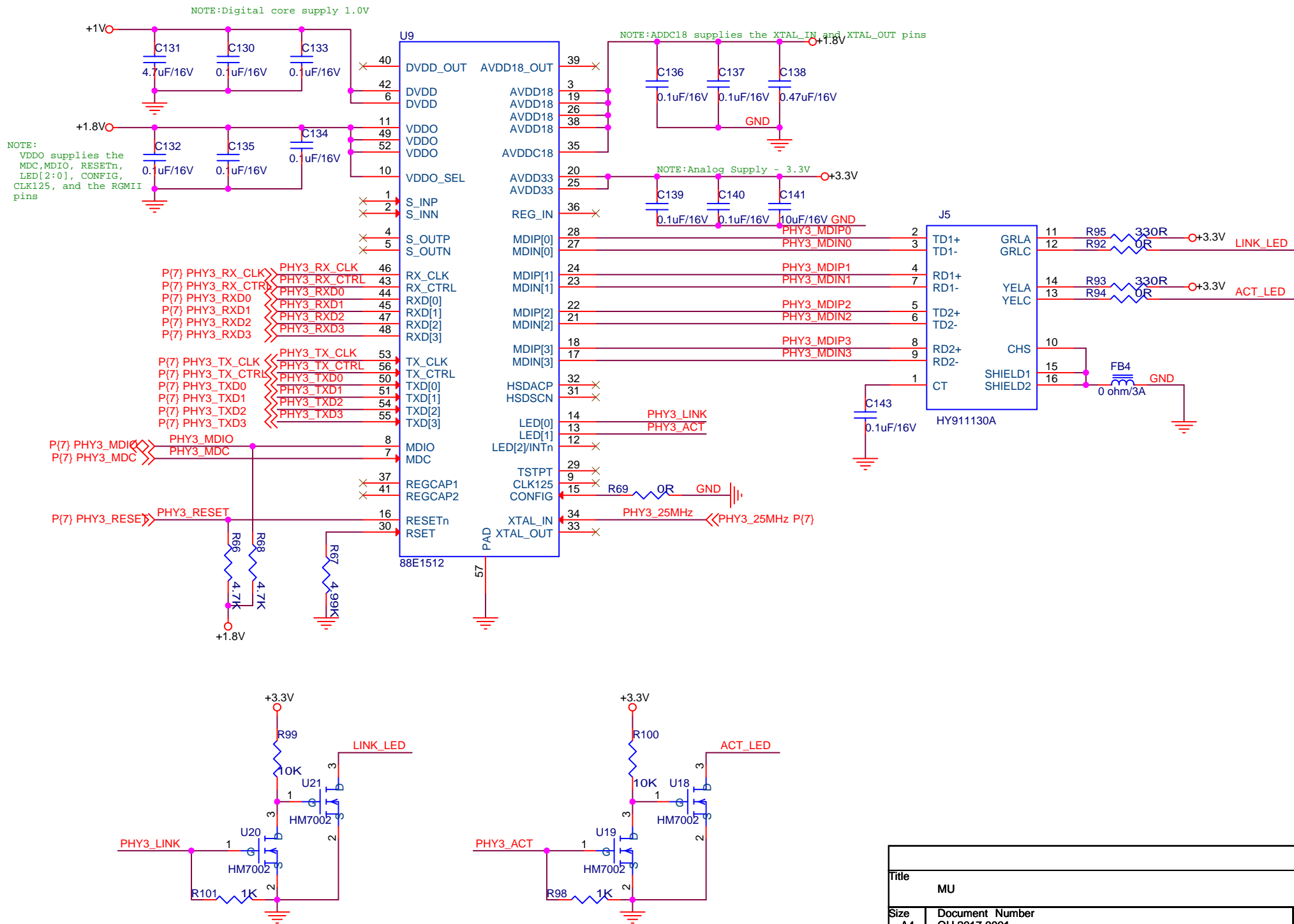
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Mode3	Mode2	Mode1	Mode0	BOOT MODE
H	L	L	L	JTAG BOOT
H	L	H	L	NOR BOOT
H	H	L	L	NAND BOOT
H	L	L	H	QSPI BOOT
H	H	L	H	SD BOOT

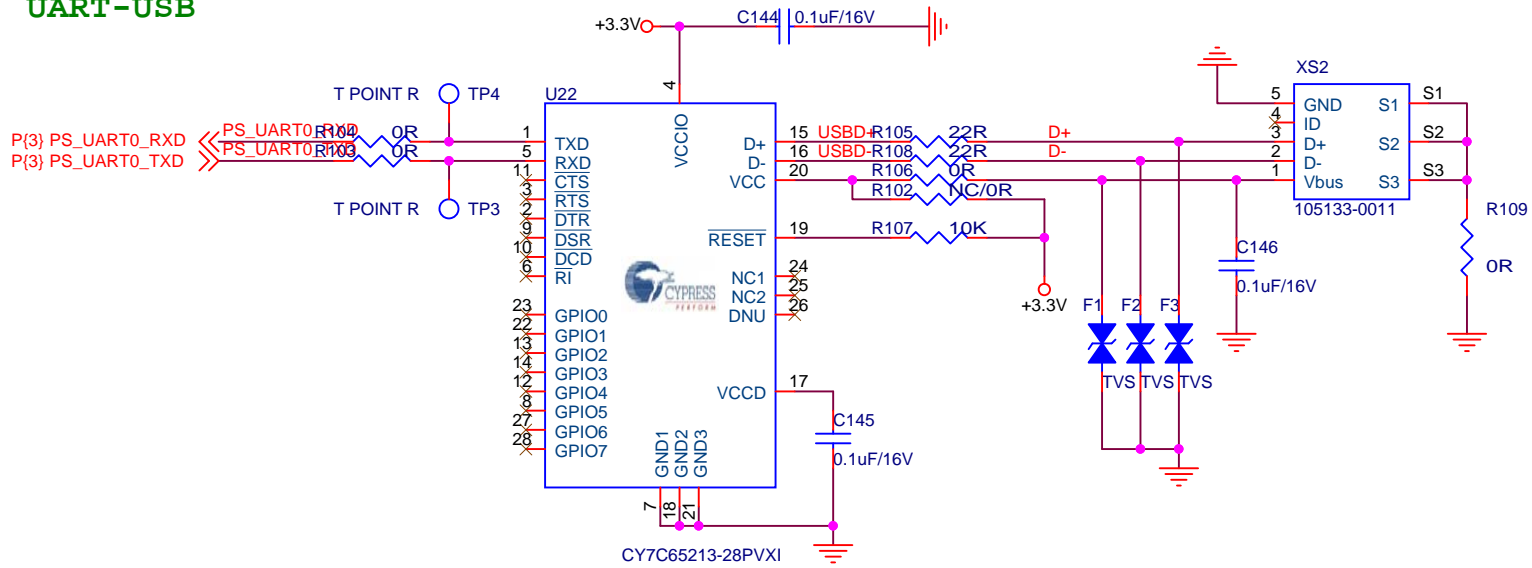


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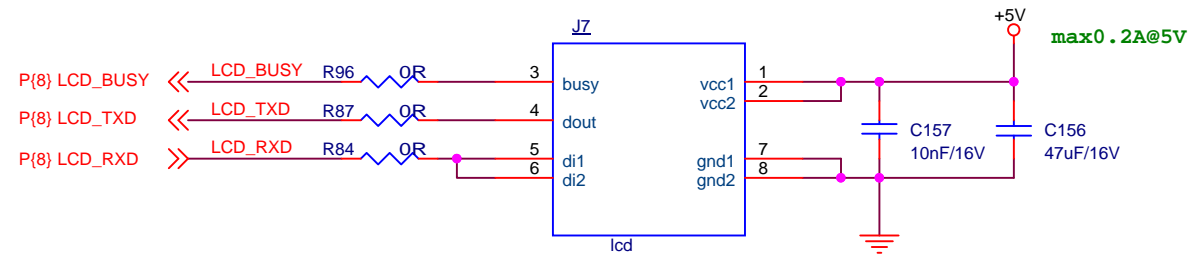


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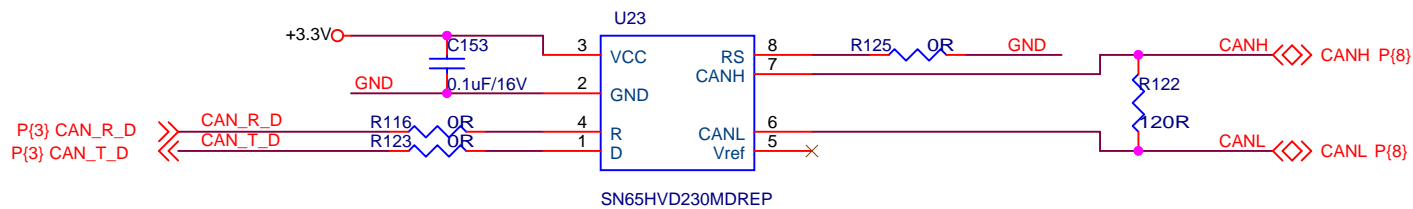
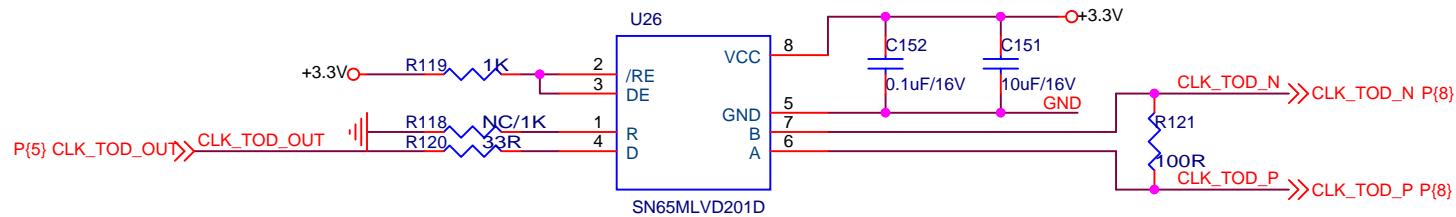
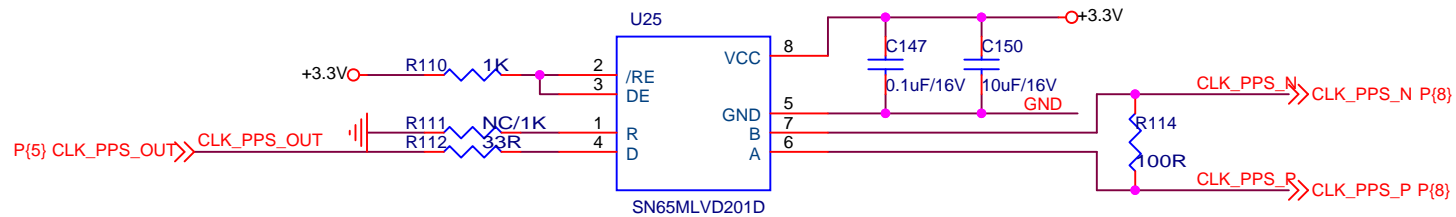
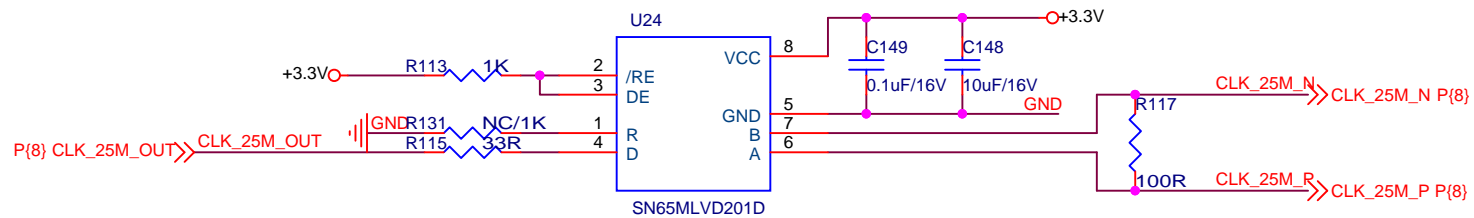
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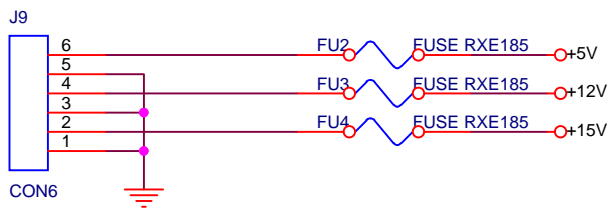
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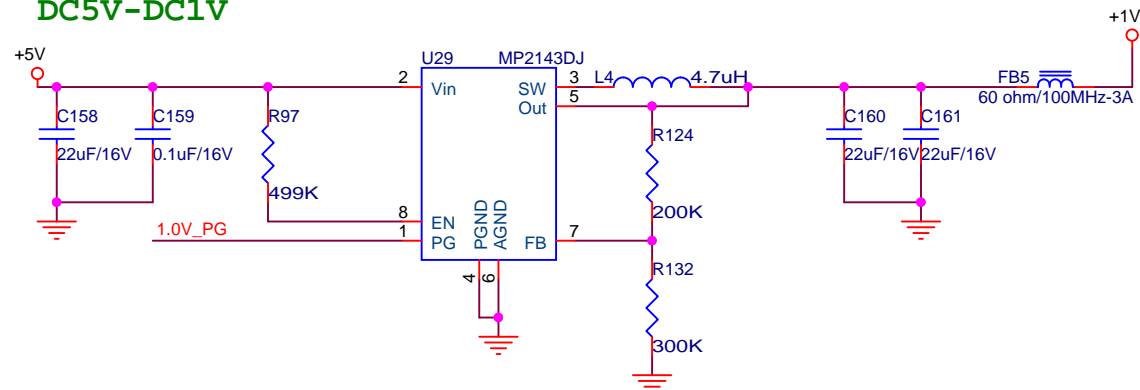
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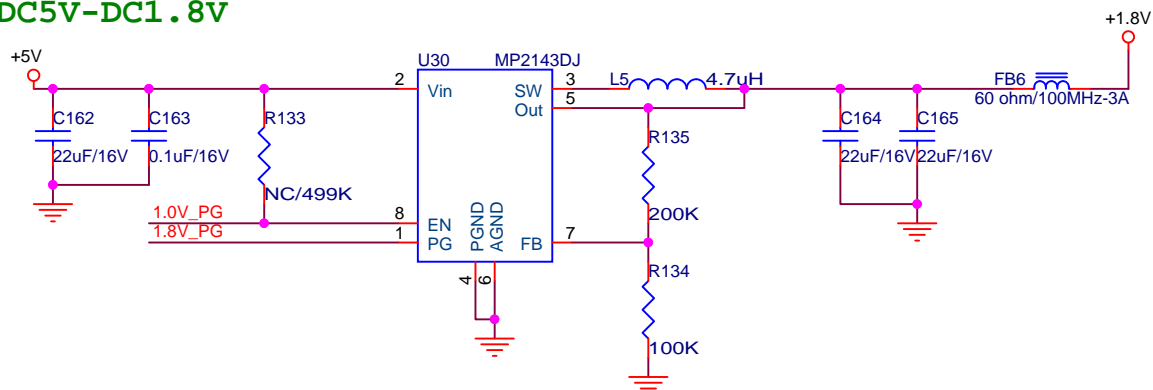
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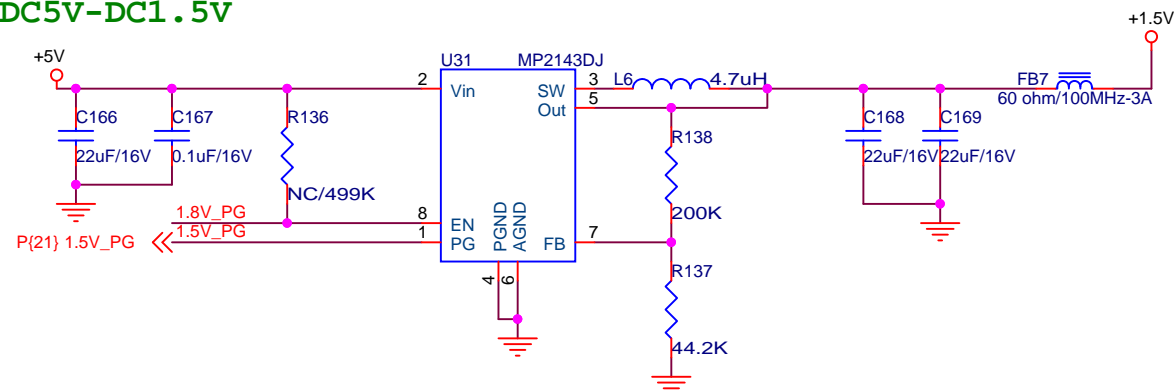
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DC5V-DC1.8V

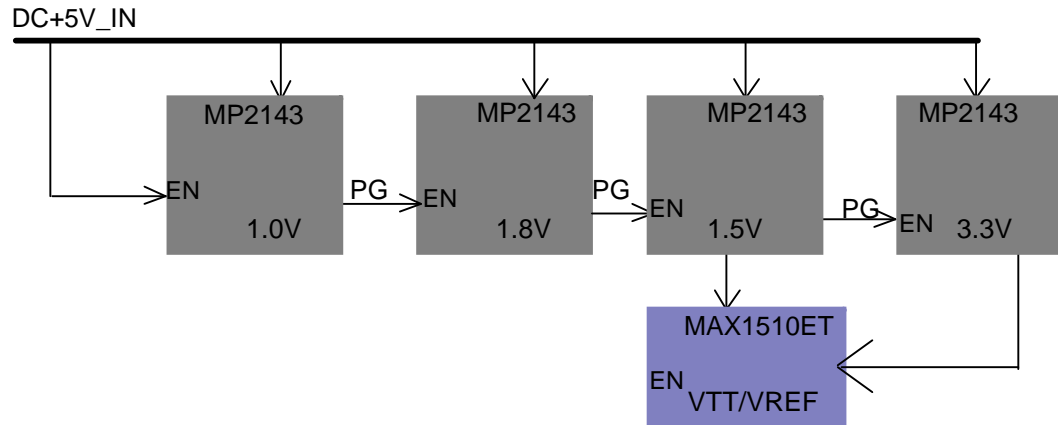


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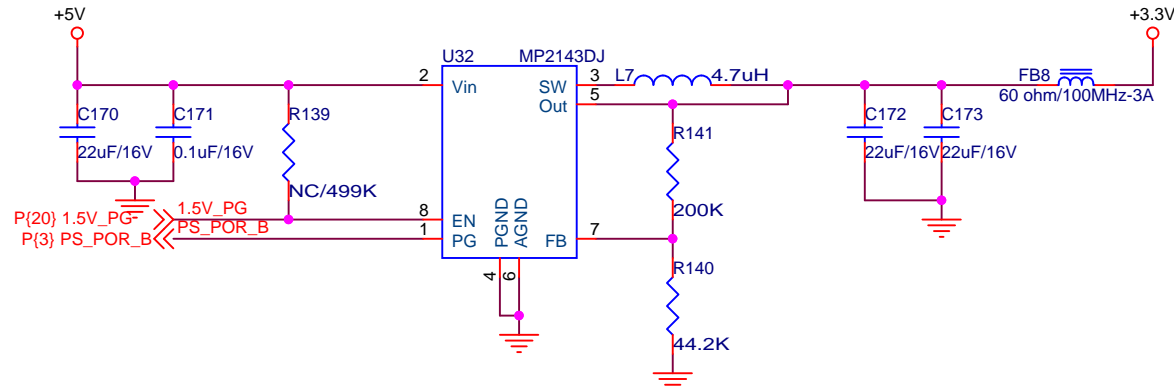


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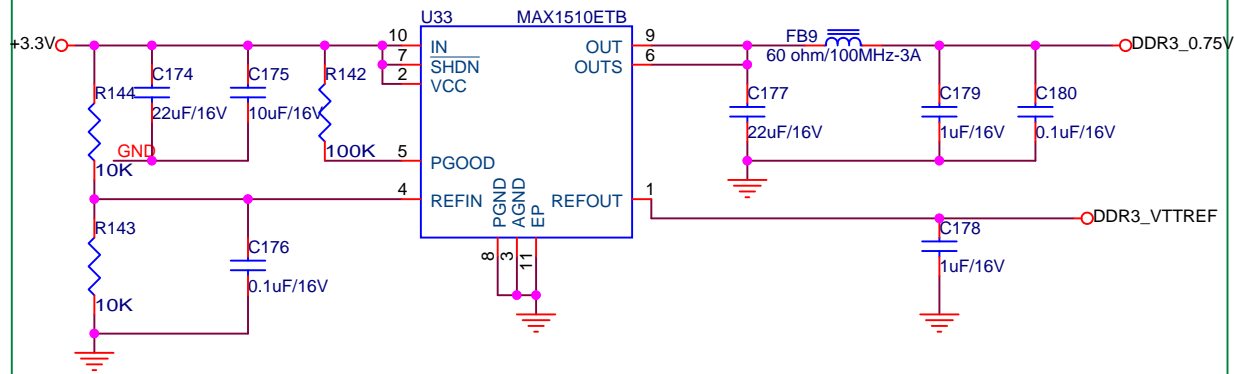
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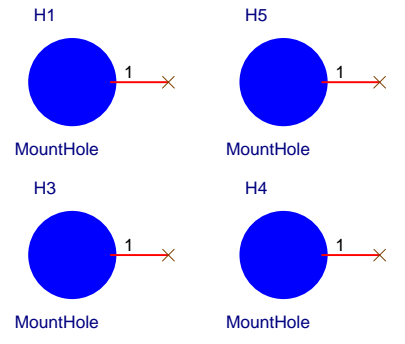
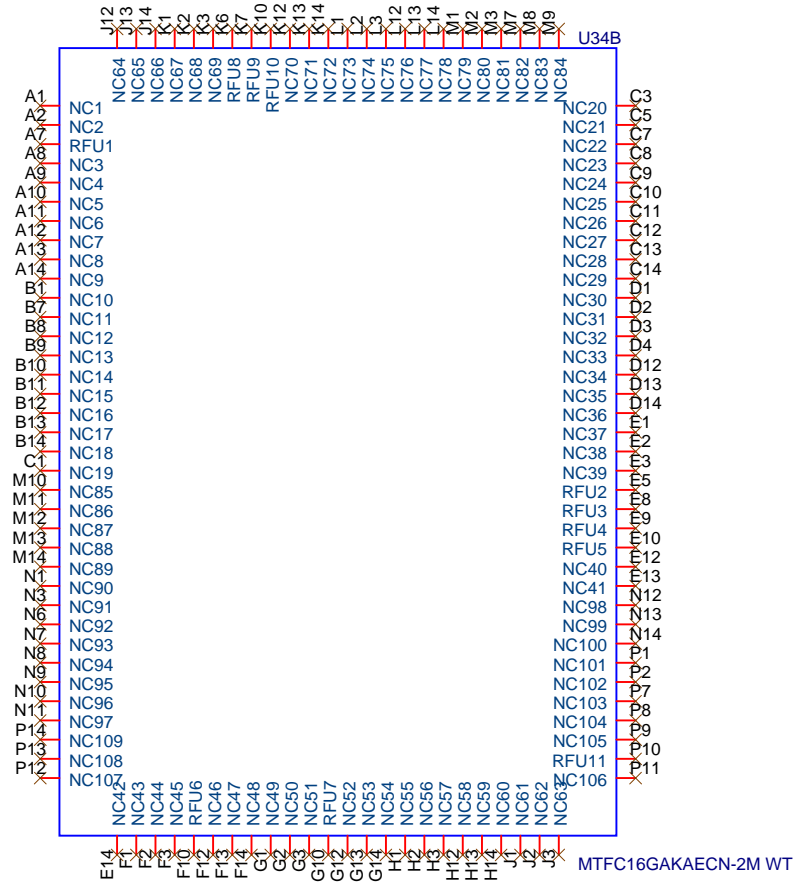
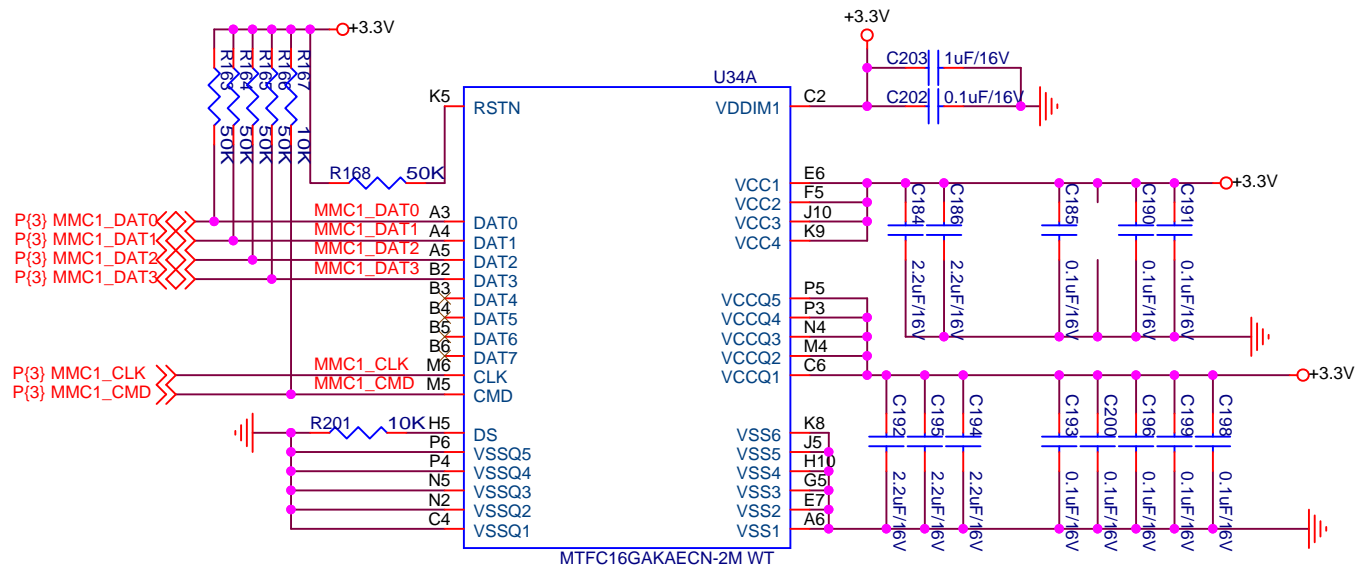
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VDD_DDR3



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