EtherSynch™ - *Synchronization Perfected*

Reducing the cost of implementing IEEE1588v2 Time Synchronized Ethernet Networks

A WHITE PAPER

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Introduction

Next-generation Industrial Automation Systems are increasingly being architected around distributed, high-performance networks that blend low-messaging latencies, flexible topologies, and integrated timing. Several so-called Industrial Ethernet frameworks are emerging based on standard Ethernet communications tightly coupled with IEEE 1588v2 (also known as IEEE 1588-2008) distributed synchronization. IEEE 1588v2 offers sub-microsecond performance, flexible timing modes, and widespread acceptance among a growing ecosystem of vendors. Increasingly, they are replacing industry-specific interconnects, delivering performance and cost efficiencies. Industrial Ethernet standards such as Ethernet/IP, Profinet, and PowerLink seeking to capitalize upon the benefits of Commercial Off-The-Shelf (COTS) technologies, are aggressively deploying Ethernet integrated with IEEE 1588. Similarly, the power systems automation industry has specified an important standard to guide Power Substation Automation. IEC 61850 breaks new ground in adopting Ethernet, IEEE 1588, and responsive fault tolerance schemes for a comprehensive communications framework for Substation Automation Systems (SAS). There are also many lower-end applications with synchronization needs far less stringent than sub-microsecond jitter, but potential cost barriers have prevented the implementation of the IEEE 1588v2 standard.

At the other end of the spectrum of synchronization a select set of applications may require synchronization performance far better than specified in the IEEE 1588v2 standard. In the Industrial Automation arena, defacto standards such as EtherCAT, and Profinet IRT have emerged to fill the need for the most critical real-time applications with synchronization accuracies are measured in 10"s of ns. EtherCAT and Profinet IRT use proprietary approaches that preclude the use of standard Ethernet MACs (even though both adopted the Ethernet 10/100/1000 Mbps PHY layer).

The key to driving such markets, whatever the synchronization needs may be, is to realize cost benefits with the availability of off-the-shelf, highly integrated, low cost silicon. Micrel's recent EtherSynch™ product family introduction provides systems designers with the most highly integrated IEEE 1588v2 network attachment device available, significantly reducing the physical form factor, power consumption, as well as overall BOM costs. This paper examines the implications of integrating Ethernet and IEEE 1588v2 for Industrial Automation, the Micrel's EtherSynch™ product architecture and benefits for Industrial Ethernet networks.

Time Synchronized Network Needs

As with most successful technologies, the availability of low-cost, standardized building blocks spawn a diverse and broad set of applications, even where synchronization precision is relatively relaxed. The convergence of Ethernet and IEEE 1588 has paved the way for precision timing to catalyze development of such systems; by capitalizing upon the benefits of COTS, proven communications and synchronization technologies, and of course, reduction of life-cycle costs. The key to enabling such applications is availability of highly integrated silicon that simplifies node designs, adapting to the widely varying interface requirements, including:

- Comprehensive support for standards including IEEE 802.3 (Ethernet) and IEEE 1588/PTPv2 distributed timing and synchronization
- Standardized copper and fibre media options to accommodate varying cable reaches
- Flexible topologies:
    - Centralized, star-wired topologies to exploit the benefits of structured wiring
    - Distributed, daisy-chained topologies (i.e., rings and linear buses) to simplify wiring installation and facilitate dynamically changing network configurations
    - Hybrid topologies, exploiting the benefits of both Centralized and Distributed topologies
- Optional, network fault tolerance mechanisms to maintain communications availability
- Support for distributed synchronization, which may be extended to locally connected devices
- Hardware assist for communications and synchronization to minimize the processing demands on the embedded processors
- Rich set of I/O capabilities to accommodate a range of devices with varying operating characteristics

Systems performance is driven by a complex combination of these factors, making it difficult to apply generic rules of thumb for network configuration. Communications latency, synchronization jitter, ring recovery delays, etc. are all inter-related. For instance, increasing ring recovery times may degrade synchronization performance. Neither increasing network bandwidth nor increasing the processing speed will necessarily overcome the issue. For higher-end applications, IEEE 1588v2 over Ethernet implementations may be enhanced by proactively addressing the error sources that deteriorate synchronization performance. Higher accuracy oscillators, enhanced power filtering, etc. are likely to result in synchronization performance well-below 100ns.

The challenge to driving such a broad spectrum of applications is architecting a network sufficiently broad to encompass their needs at a very low cost. Systems designers may then exploit standardized building blocks that attain the best of both worlds; the high-performance, only achievable by silicon, at a cost-effective price.

Reducing Cost with Integration

IEEE 1588v2 implementations are far less common, and are typically implemented in FPGAs, Physical Layer (PHY) transceivers, or Micro-Controllers. Integrating Ethernet switching along with IEEE 1588v2 (and the associated logic) is not a trivial exercise, and requires additional communications and synchronization processing (in the host CPU).

Migrating from relatively simple serial interconnects and buses to an integrated Ethernet/IEEE 1588v2 network in a cost-effective manner can be challenging. Considering the cost difference between an RS-485 interface and Ethernet port, it remains cost-prohibitive to directly connect low-end devices to Ethernet networks. Ethernet/IEEE 1588 attachments will multiplex multiple devices (through I/O pins) in order to achieve cost parity with point-to-point systems. Migrating to a network offers greater flexibility and a compelling range of benefits.

The costs for an Ethernet/1588v2 attachment (assuming a distributed topology), include:

- IEEE 1588v2 Support
  - IEEE 1588v2 Precision Clock
  - 2 x Time Stamp Units (TSUs) for PTP packets
  - PTP hardware support
- 3-port 10/100 Ethernet switch
- 2 x integrated Media Access Control (MAC)
- 2 x 10/100BaseTX PHY Transceivers
- Precision I/O (synchronized to the Precision Clock)
- PTP Software (typically running in the Host CPU)

Presently, an Ethernet/1588v2 attachment implemented in an FPGA, with a pair of external Ethernet PHY Transceivers, with an estimated cost measured in $20-30 USD or more. Assuming four to eight devices share a single Ethernet/1588 attachment, the per-device costs are on the order of $3–$5; multiples of the sub $1 USD cost for an RS-485 interface transceiver. In order to reduce

the Ethernet/IEEE 1588 attachment costs so as to be on par with serial interconnects, further integration is necessary. This is primarily achievable through an ASIC. As a result, Micrel Semiconductor recently introduced the KSZ84xx EtherSynch™ family of IEEE 1588v2-enabled Ethernet 3-port 10/100 switches, for real-time applications, as shown in Figure 1.

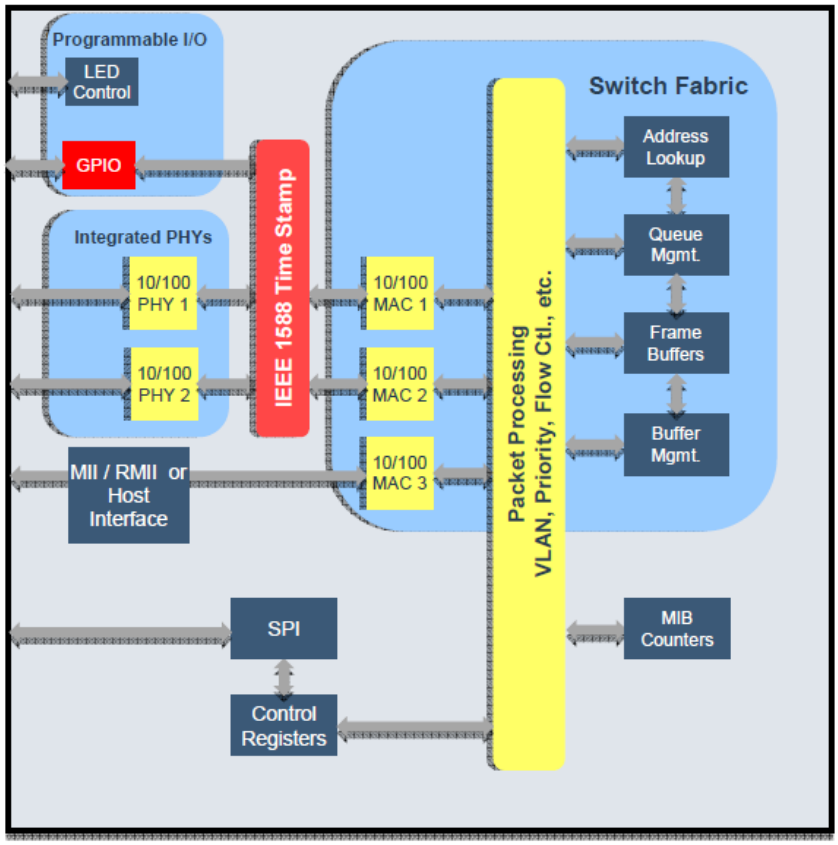

Figure 1: KSZ84xx EtherSynch™ IEEE 1588-Enabled 3-Port Switch Architecture.

This Industrial-grade platform represents a single chip, highly integrated 1588/Ethernet attachment, offering numerous benefits:

- Wire-speed, fully managed 3-port 10/100 Mbps switch
- Dual IEEE 1588v2 time stamp units, Precision Clock, and distributed synchronization facility
    - Synchronization performance is improved as TSUs reside between the MAC and PHY
    - Grand Master, Master, Slave, and Transparent Clock modes are supported

- Dual, low-power 10BaseT / 100BaseTX PHYs
    - Lowest power 100BaseTX PHY Transceiver (< 150 mW per port)
    - 100Base-FX optical transceiver support
- Hardware support for communications and precision clock synchronization, which reduces the overall processing load on the host CPU
- Integrated I/O that can be synchronized to the overall system synchronization hierarchy
- Advanced power management including IEEE 802.3az Energy Efficient Ethernet (EEE)
- Compact size through a single-chip design (64-pin package, 10 mm x 10 mm)

Host CPU overhead processing is reduced with the realisation of 1-Step Transparent Clock mechanism 100 percent hardware implementation. 1-Step synchronization method, as shown in Figure 2, reduces network traffic as well as CPU burden. Switching delays are measured and corrected in the outgoing network PTP packet on-the-fly. 2-Step synchronization is also supported by the KSZ84xx with the timestamp switch latency correction added to the follow up message, under the control of the host CPU.

End-to-End and Peer-to-Peer synchronization delay mechanisms are both supported by the KSZ84xx EtherSynch™ family.

The KSZ84xx is available with standard (MII or RMII) and generic host bus interfaces to support CPUs with and without embedded Ethernet MACs. Most available 1588 implementations partition the high pin count (30+) MAC-to-PHY interface on two distinct devices, compromising synchronization performance. Multi-chip implementations also prove more costly, consume higher power, require additional board space, and are typically less reliable than an ASIC.

The Precision GPIO facility enables multiple devices to share a single Ethernet/IEEE 1588 attachment. Precision GPIO is highly flexible and configurable to support a diverse set of devices with wide ranging operational and performance characteristics.

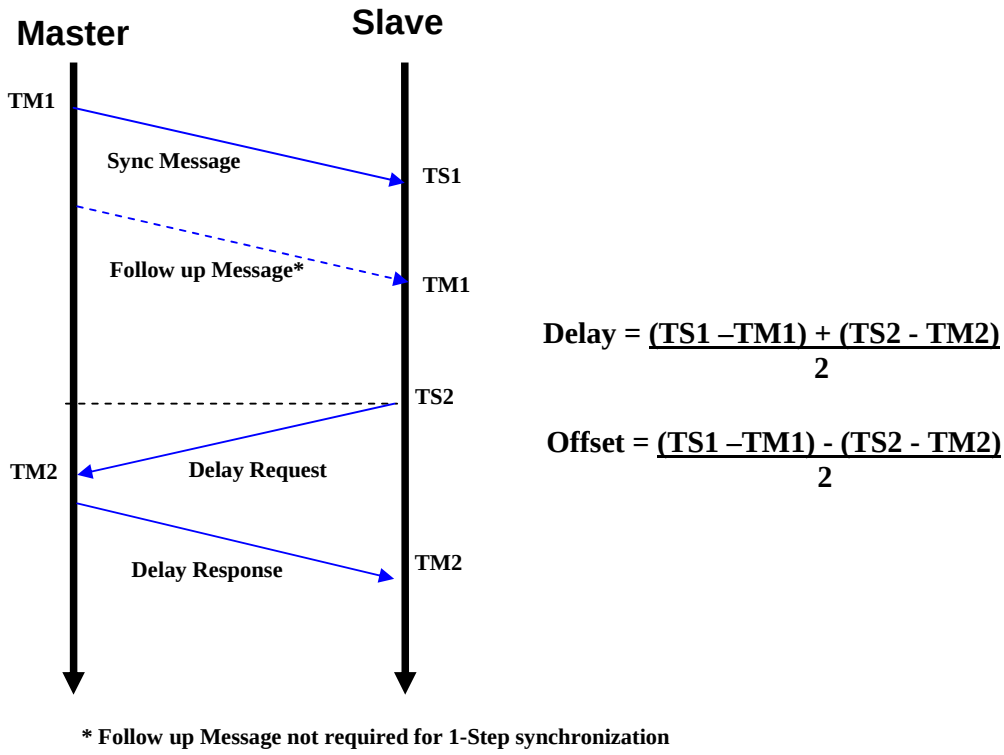

Figure 2: 1-Step and 2-Step Synchronization Methods.

Precision and Local Synchronization

Devices connected to the network through the Precision GPIO facility must be synchronized to the node, and hence system reference timing. Figure 3 illustrates the system timing hierarchy implied by IEEE 1588v2, where a global, real-time reference (i.e., GPS) synchronizes a Grand Master Clock (GMC) for the system reference

Multiple Master Clocks (MCs), each corresponding to a distinct synchronization domain. Each MC synchronizes the set of Slave Clocks (SCs) comprising a particular synchronization domain. For Industrial Ethernet, SCs are typically daisy-chained together into a distributed topology. Locally connected nodes can source or sink data and/or control information through a Precision I/O interface that is synchronized with the local precision clock

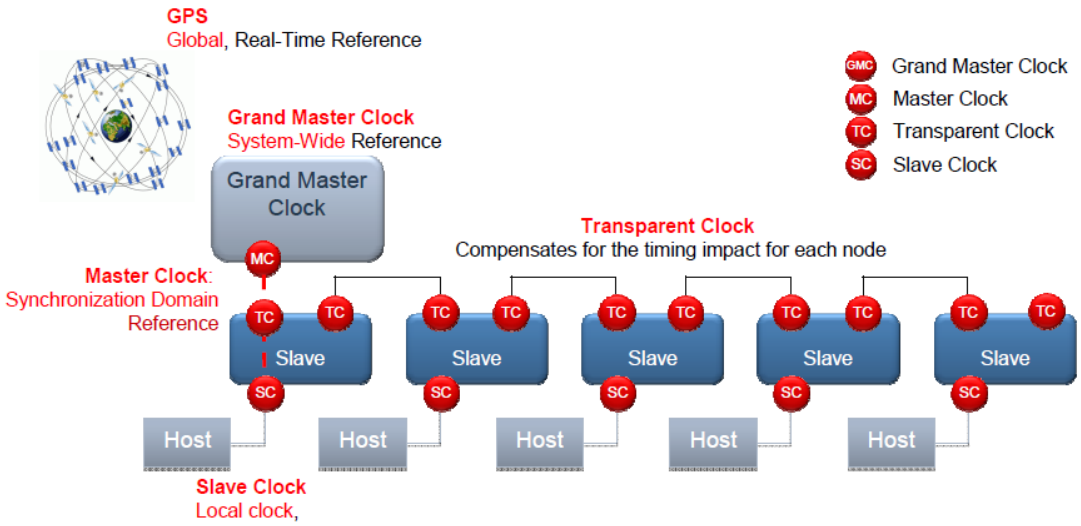

Figure 3: IEEE 1588v2 Distributed Timing Network Example.

Local synchronization may be provided through standardized timing interfaces:

- 1 PPS reference for time distribution
- 10 MHz reference for synchronized clock distribution

Because timing and synchronization is application-specific, versatility is required to tailor the timing interfaces to the needs for specific designs. Additional reference signals (such as 100 PPS timing output, 1 MHz and 5 MHz, etc.) may be necessary and also signal characteristics may also vary (e.g., pulse width, voltage level, etc.).

Micrel's KSZ84xx Industrial Ethernet switch platform is an ASIC specifically designed to enable synchronized networks. Precision I/O pins are synchronized with the local precision clock, which in turn is synchronized to the system timing hierarchy. In-house testing yields synchronization jitters on the order of 100 ns or less (see Figure 4), even under 99 percent+ network loads and the use of standard 50ppm local crystal oscillators. Such performance is attained through positioning the time stamp units, directly between the PHY and the MAC (on-chip). As a result, measurement and time stamp errors are significantly reduced at the node-level. The result is that higher-end real-time network needs can be addressed with a low cost, off-the-shelf, IEEE1588v2 device, where typically today only expensive ASIC solutions exist.

Another factor yielding improved synchronization performance is the tightly coupled Precision Timing Protocol (PTP) stack, developed by OnTime Networks, Oslo, Norway. Hardware-assisted PTP operations (especially periodic Transparent Clock corrections) are not only more efficient, but more importantly, conserve scarce Host CPU resources which can otherwise be dedicated to applications processing. That said, any IEEE 1588v2 PTP stack software can be utilized (and optimised) to work with the KSZ84xx platform.

Figure 4: Sub 100ns Synchronization Jitter with KSZ84xx EtherSynch™ Family.

In order to support diverse interface needs anticipated for real-time systems, a broad set of I/O capabilities has been provided. The I/O implementation is based on a set of logical I/O Event Units that may be assigned to any of the available I/O pins (up to 12 in total). By decoupling Event Units from physical pins, more sophisticated I/O operations are possible.

Input Event Units provide an efficient means of monitoring external events and conditions on I/O input pins. For each Input Event, a time stamp is generated whether for an Edge or Pulse sensed on that pin. Input Event Units may be cascaded together to monitor more compound events i.e. sequences of multiple pulses, edges, and in essence bit patterns, offloading the Host CPU from low-level I/O manipulation.

Once detected, the time stamp corresponding to each received event will be queued up for the host CPU to retrieve. Such an approach decouples host processing from the I/O acquisition, further offloading the Host CPU.

For Output Events, a flexible range of I/O Output Units and associated operations are supported. Each Output Event will be initiated (i.e., triggered) when the local precision clock reaches a pre-configured value corresponding to the event. Thus, all Output Events are timed in concert with the local clock, and in turn the overall systems timing hierarchy. Similar to the Input Event Units, Output Event Units may be cascaded to enable more complex operations. For example, if a Logic Controller is required to send a 32-bit control word to request a Sensor reading, 2 Register Mode Output Events may be cascaded together and shift out the 16-bit contents of user-data (contained in an internal register) onto a single I/O Output pin.

In addition, a programmable Waveform Generator Output Unit may be configured to provide; N x PPS Output Interval (where N = 1 for 1 PPS). The waveform can be configured with start time, pulse width, time period as well as the number of pulses (if not continuous).

High-frequency reference signals may also be generated, using the Frequency Generator Output Unit. Frequency Outputs may be configured from 1Hz to 12.5MHz, on one or more I/O output pins, synchronized to the network clock.

Conclusions

Real-Time network cost of ownership can be reduced through the availability of highly integrated, IEEE1588v2 silicon implementations. By dramatically reducing the cost of the distributed network node, IEEE1588v2 standard based solutions can be utilised not only for sub micro-second synchronization needs, but also migrate into many other emerging, relatively mid to low-end, applications.

By offering sub 100 nano-second IEEE1588v2 synchronization performances with low cost, off-the-shelf devices, high-end real-time network needs can also be addressed, where typically today only expensive ASIC solutions exist.

While network performance remains closely coupled with the applications, high-performance silicon such as Micrel's KSZ84xx EtherSynch™ family renders IEEE 1588 over Ethernet as a viable option for a range of diverse applications that were previously cost-prohibitive.

The KSZ84xx product family consists of 3-port, 10/100 Mbps Ethernet switches, with integrated PHY Transceivers, IEEE 1588v2 synchronization, along with a powerful I/O facility synchronized to the local precision clock.

KSZ8463MLI	**3-Port 10/100Mbps Ethernet Switch with MII**
KSZ8463RLI	**3-Port 10/100Mbps Ethernet Switch with RMII**
KSZ8462HLI	**2-Port 10/100Mbps Ethernet Switch with Host interface**
KSZ8441HLI	**Single-Port 10/100Mbps Ethernet MAC/PHY Controller with Host interface**

The KSZ8463/8462 family includes a fully featured, wire-speed switch, based Micrel's proven Industrial Ethernet product family. Switches provide comprehensive QoS, Packet Filtering, Congestion Control, and Layer 2+ features to carry and process IPv4 and IPv6 packets.

The two integrated PHY transceivers are draw less than 150 mW per port. Overall power consumption is reduced by adoption of the recently ratified IEEE 802.3az Energy Efficient Ethernet (EEE) standard, Energy Detect Power Down (EDPD), and Wake on LAN (WoL).

PCB real estate is minimised by the single-chip integration into a 10 mm x 10 mm 64-pin LQFP package. Powered by a single 3.3VDC supply, an optional integrated LDO controller enables a range of I/O voltages across the industrial temperature range (-40^{o}C - +85^{o}C). Such integration elevates Industrial Ethernet to the next level as a viable technology for Industrial Automation, down to the Field bus layer.

For further details, contact your Micrel representative or visit: www.ethersynch.com/.