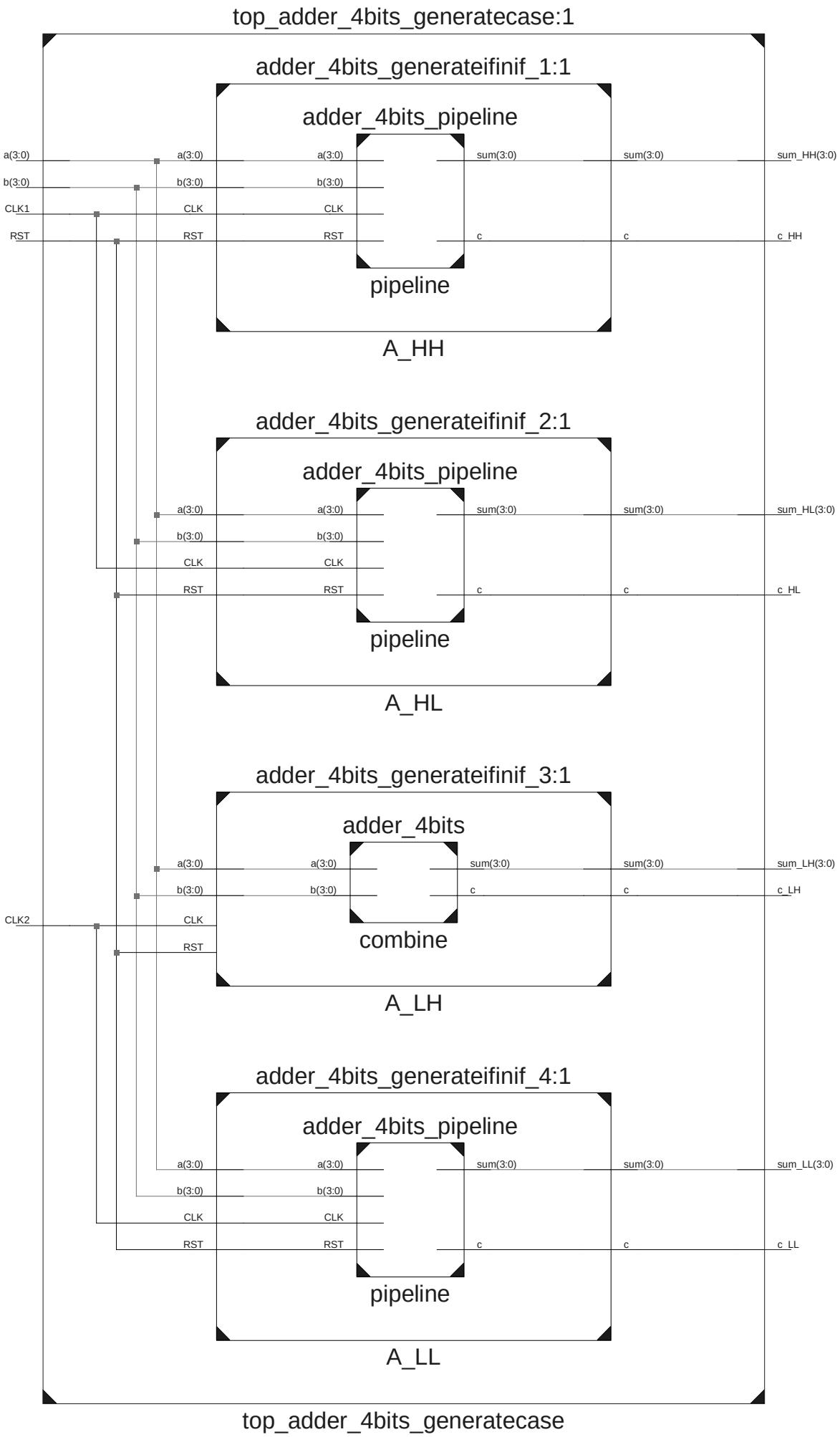
top_adder_4bits_generatecase:1
adder_4bits_generateifinif_1:1
adder_4bits_pipeline
a(3:0)
b(3:0)
CLK1
RST
a(3:0)
b(3:0)
CLK
RST
a(3:0)
b(3:0)
CLK
RST
sum(3:0)
c
sum(3:0)
c
sum_HH(3:0)
c_HH
pipeline
A_HH
adder_4bits_generateifinif_2:1
adder_4bits_pipeline
a(3:0)
b(3:0)
CLK
RST
a(3:0)
b(3:0)
CLK
RST
sum(3:0)
c
sum(3:0)
c
sum_HL(3:0)
c_HL
pipeline
A_HL
adder_4bits_generateifinif_3:1
adder_4bits
CLK2
a(3:0)
b(3:0)
CLK
RST
a(3:0)
b(3:0)
sum(3:0)
c
sum(3:0)
c
sum_LH(3:0)
c_LH
combine
A_LH
adder_4bits_generateifinif_4:1
adder_4bits_pipeline
a(3:0)
b(3:0)
CLK
RST
a(3:0)
b(3:0)
CLK
RST
sum(3:0)
c
sum(3:0)
c
sum_LL(3:0)
c_LL
pipeline
A_LL
top_adder_4bits_generatecase