Report of Multiplexer and feed-forward equalization capable line driver

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Abstract—

The objective of this report is to introduce the design of the system created to multiplex four square waves, to equalize their leveling and their peaks and periodic spacing, to amplify the resulting signal, and to eliminate as much noise as possible.

This report will analyze the connection between a 4-to-1 multiplexer, a feed-forward equalizer, a transmission line, and a CTLE/line driver, while also using CML design to implement each part in order to prove the methods usefulness and reliability.

Testing signal data rate: 10Gb/s

I. Introduction

THIS report is to give readers the insight of the project (Multiplex and feed forward equalizer on transmission line with 10Gb/s data rate), meanwhile, the continuous time linear equalizer is also added at the end of transmission line to test the whole performance. This project is divided by four parts: 4-1 multiplexer, feed forward equalizer, transmission line and continuous time linear equalizer. First, the multiplexer's function is essentially to create a single line of data taken from two or more inputs by triggering a specific selection of inputs using a switch. The multiplexer logic is configured with the selection bit as the first two output results take after the x1 selection and the final two takes after the x2 selection. The inputs in the above example are 0 and 1 where the selection of which bit is used is determined by switches x1 and x2. The multiplexer circuit is implemented as a type of CML diagram implication using six MOSFETs [Figure 1]. Second, the fee forward equalizer is using 4 taps of CML equalizer structure with 4 sets of DFF, 4 sets of Amp, and one main driver and 3 equalizers [Figure 2]. DFF is composed by two level sensitive latches, and each has one conventional differential pair and one cross couple differential pair. For this type of DFF, each DFF's output signal will be delayed by one clock cycle, when clock cycle represents the data period, every output of the DFF could be regarded as sending one UI delayed signal to the tap. [Reference 1]. The buffer amplifier and main CML driver is connecting to the first output of DFF, while 3 other buffer Amp and taps are connecting to the rest of DFF reversely so as to make subtraction from the main signal. By adjusting the transistor's width and subtraction taps' bias current, the ISI from random 10Gb/s data signal could be eliminated to a large extend. The detail explanation of each components in FEE will be introduced in next block. Third, it is transmission line. Third, the transmission line, from a general standpoint, is a long chord or a set of wires connecting structures that alter the wave nature of an incoming electric signal in order to conduct electromagnetic waves. In this simulation, we use five set parts to construct the line, while each set is composed by inductor, capacitor, resister and trans-conductor. The abundance of 5 RLC loads (RL in series and RC in parallel) was tested and works the in a more realistic way for providing the input signal with a realistic distortion as well as eye-closed output. Forth, we use conventional negative impedance CTLE to cancel the ISI due to the signal distortion from transmission line so that the eye could be reopened at the end stage of output. This negative impedance CTLE is composed by a CML amplifier and a cross couple CML impedance.

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II. Implementation

Multiplexer:

The building of the multiplexer circuits consisted of three CML amplifiers with six MOSFETs each where the outputs of two would lead into the inputs of the third one and multiplex a total of 4 inputs. A 4 to 1 multiplexer was chosen to be analyzed as it is the best for showing the convention for building a MUX with more than 2 inputs and also simpler to analyze [Reference 2].

The MOSFETs used for the three parts of the multiplexer were programmed with values of L=50 nm and W=2 μm. As stated before, the convention of the multiplexer is two CMLs that are supplied by a bias current such that the product of bias current and a 500 ohm-resistor is 0.5 V. Therefore, the suitable bias current supplying or opposing the amplifiers is 1mA.

The schematic provides the layout of the multiplexer and the wireless connections [Figure 3].

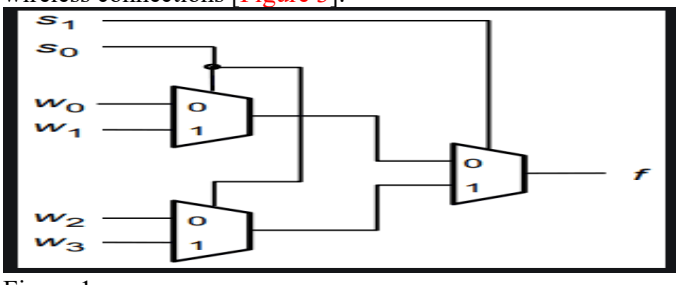


Figure 1

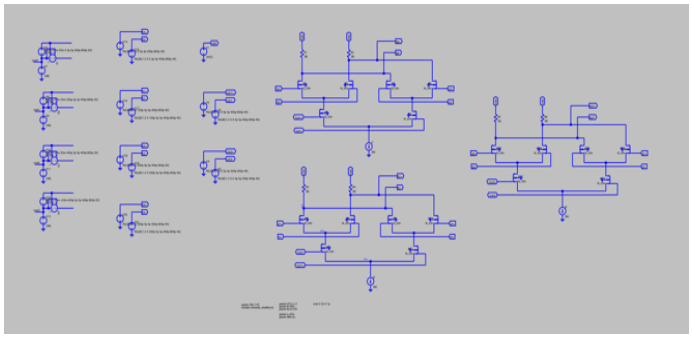


Figure 3

The inputs (D0+, D0-, D1+, D1-, D2+, D2-, D3+, D3-) are shown as rectangular pulses that connect to the first two CMLs. The first stage CML amplifiers and second stage amplifier are clocked by different clock signals as seen in [Figure 4]. The 2 clock inputs are used to apply the periodic cycle to the specific parts of the multiplexer. The first clock input is applied to the first two MUXs that take the inputs D0-D2 and D1-D3 with opposing polarities between MUXs. The output of the 4 to 1 multiplexer is determined in the third 2 to 1 multiplexer to allow a higher frequency (more bandwidth and less time needed to transfer information). The peaks of the clock and inputs range from -1.2 to 1.2 V and while the first input is identical to the first clock, the second third and fourth signals each vary by a phase of 45 degrees. The reason D0 and D2 are multiplexed together first is such that they are separated by 90 degrees, making it easier to analyze the circuit with varying inputs at different times.

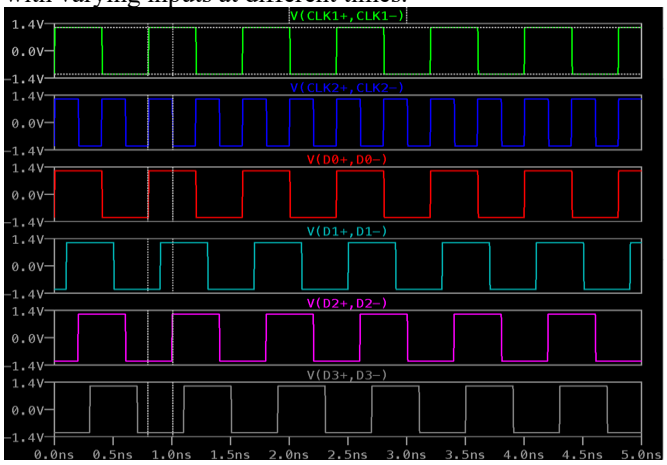


Figure 4

In [Figure 5], D0 and D2 generate a lower output of -600 mV only when D2 has a high value while the D0 input is low. Otherwise, the output is higher. It can be concluded that for this portion of the MUX, while D0 is replicates a 0 pulse, the output selects values equal to the opposite of D2, while D0 has a 1 pulse, the output selects values of D0.

As for the D1 and D3 input MUX, the [Figure 6] explains this particular behavior. While D1 emits a low input, the output selects D1 values as output, and when D1 emits high voltage, it then selects the opposite of the D3 input as output.

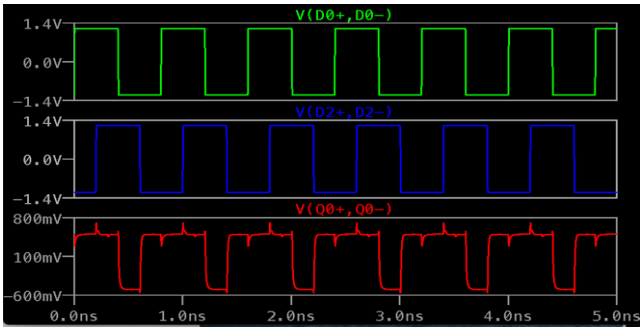


Figure 5

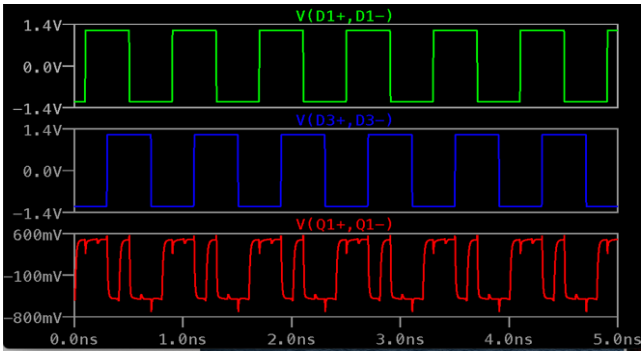


Figure6

In [Figure 7], the modified multiplexed signals are placed in the last 2 to 1 MUX to complete the selection of the four inputs. When the D1D3 signal experiences an abrupt drop (D1=1, D3=1), then this signal becomes selected as the output. Otherwise, the D0D2 input will be selected as the output. Although, this convention is determined for the output of the 4 to 1 multiplexer, the values of amplitude are decreases such that the signal varies from -400 mV to +400 mV and the hold of the high voltage when the D0D2 is selected is not as long due to the last part of the MUX being clocked with a higher frequency clock signal.

The amplitude of the MUX output is significantly lower than that of the inputs, and while this does not allow for as much information to be transferred at those instances, the benefit of having a smaller amplitude voltage is that it is filtered to transfer compressed data that will not be cut or experience any interference. The logic of this MUX can be explained by

Y = S0D0 + S1D2' + S2D1 + S3D3', where Sn (n=0,1,2,3), represents the switch selection

inputs activated when Sn = 1.

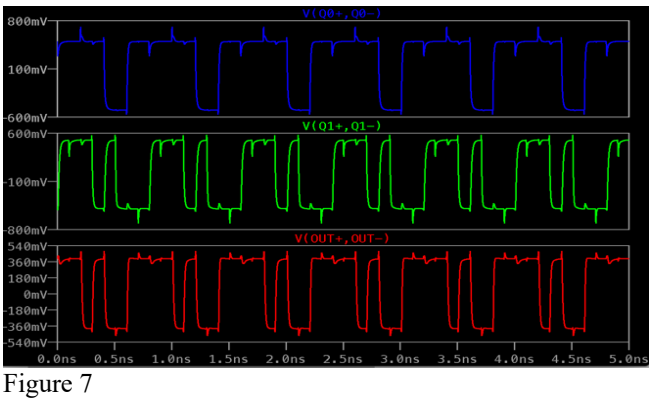


Figure 7

With the 10Gb/s signal from 4-1 multiplexer, we need test these signals in decision circuit and cancel ISI if there are too much noise inside.

Feed Forward Equalizer:

This FEE transceiver is built on conventional structure. 4 taps of DFF connect 4 taps of driver and equalizers [Reference 1]. The general structure layout is showed below:

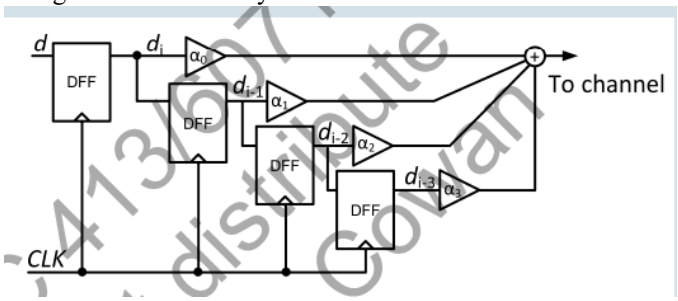


Figure 2.

Based on above structure, we built a taps FEE. Each DFF has 2um MOSFET CML and 4um MOSFET cross couple CML, transistor length is set as 50nm for all the components [Figure 8]. The biased current is chosen for full signal swing from 0.3v to – 0.3v. The main CML buffer and main CML driver has transistor of width 4um and 8um, of which the size is chosen based on that we need some relatively larger analog output signals. Main buffer has RL 750Ω with 1mA biased current, which makes this buffer works at the edge of triode region. (Vth≈0.22V, Vgd≈0.23V). The main driver uses inductive peaking, choosing resistor, capacitor and inductor values so that the damping factor is 0.707. In this case the bandwidth is able to be extended to accept the faster data rate. The other three buffer and taps are using transistor of 4um width, load resistor of 500Ω. To make transmitter side ISI eliminated, the taps biased current is scaled by a factor of 0.39.

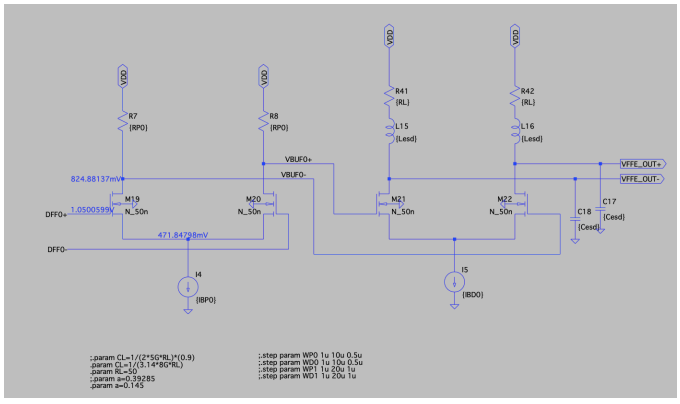


Figure 9, CML driver with inductive peaking

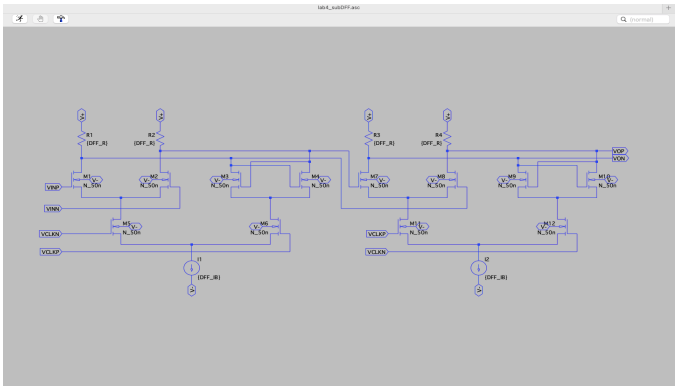


Figure 8, DFF

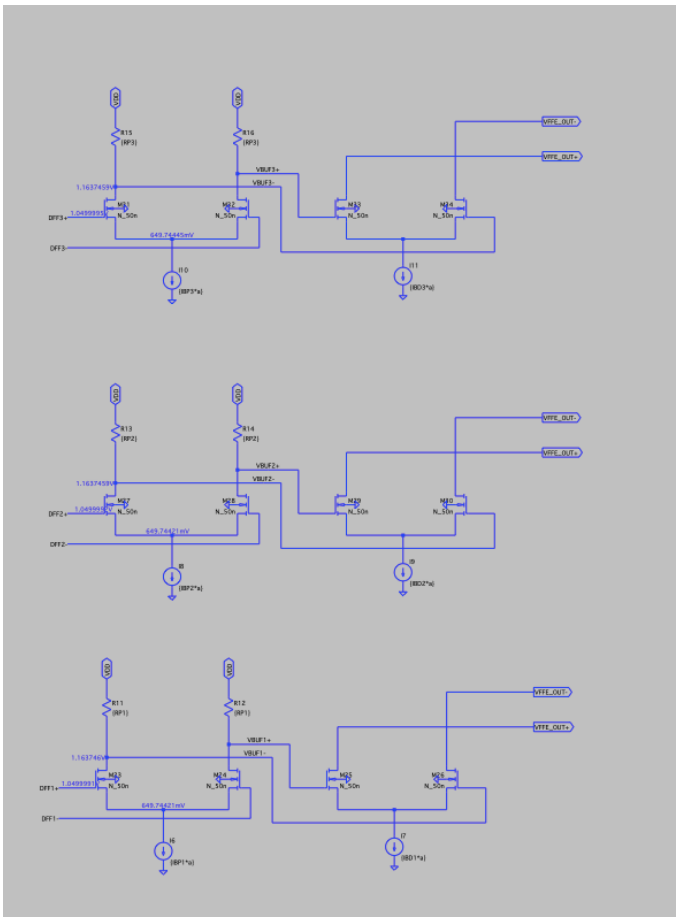
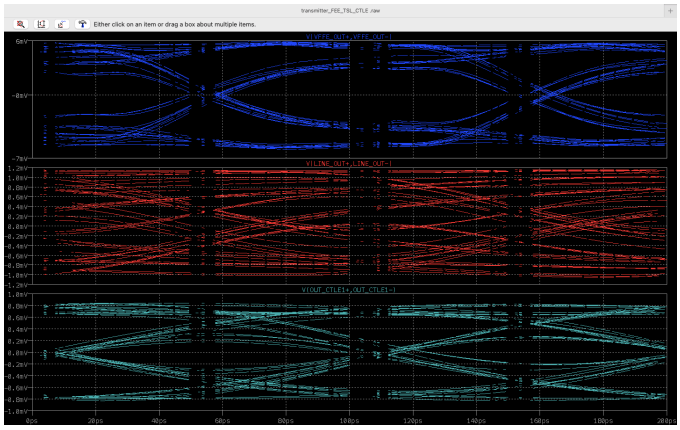


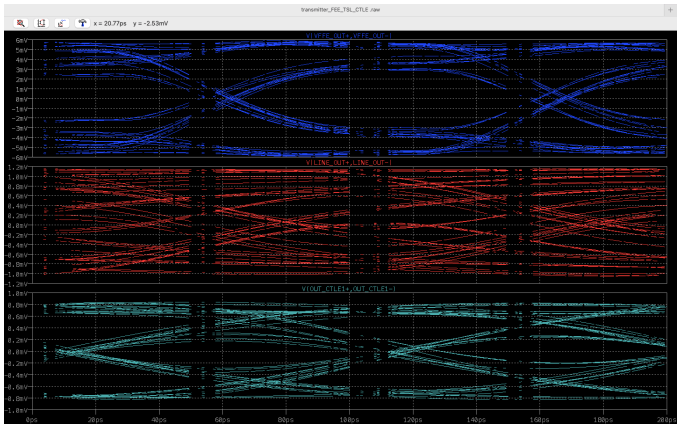
Figure 10, FEE taps

[Figure 9] shows the FEE schematic of main CML driver and buffer. [Figure 10] shows three equalizer taps attached with buffer, biased current is scaled by factor å.

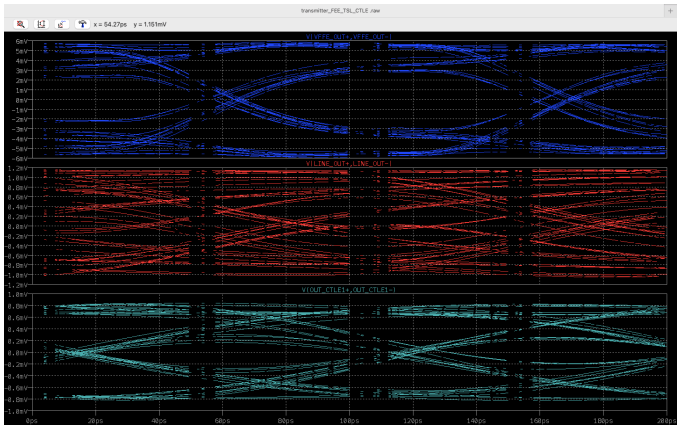
The Inductive peaking is used on the main CML driver. 50Ω RL and 400fF Capacitor and 500pH inductor is chosen to make damping factor at 0.707. Comparison is made by changing damping factor to 0.99. The plot shows the difference regarding eye opening.



inductive peaking Damping factor = 0.707



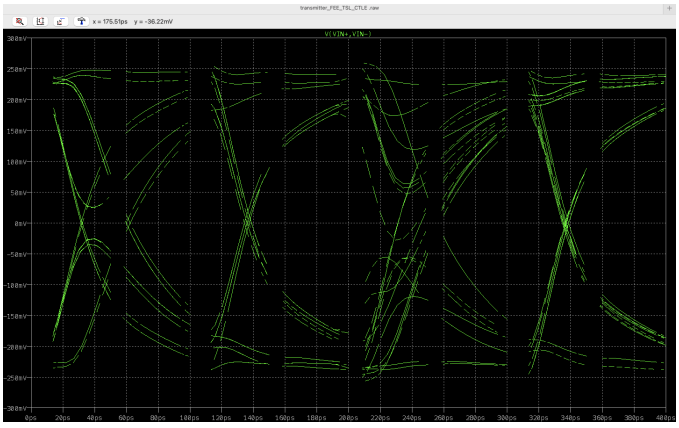
Inductive peaking damping = 0.99



RC load

From the above three plots we can see, there is less ISI (blue one is FEE output signal) at transmitter side when inductive peaking of 0.707 damping is applied compared to using damping at 0.99 or using RC load .

At the stage of FEE output, the voltage swing is about ||6 mv||, the VEO is about 0.6mv, and the ISI is around 0.5 at the normalized signal swing. Compared to the direct input signal from multiplexer, which is showed in below, the ISI is indeed improved after being passed through decision circuit and FEE.



Signal at mux output

Using CML driver is better choice than using SST driver at transmitter side. This has been simulated by replacing CML driver by SST driver [Figure 11]. SST driver has off chip two 50Ω RL, two PMOS and two NMOS have resistance around 50Ω at width 256um. This is only to simulate transistor behaving as resistor, in the real situation, all the transistors are cascaded each other. The signal at output of transmitter side shows very large ISI as plot below [Figure 12].

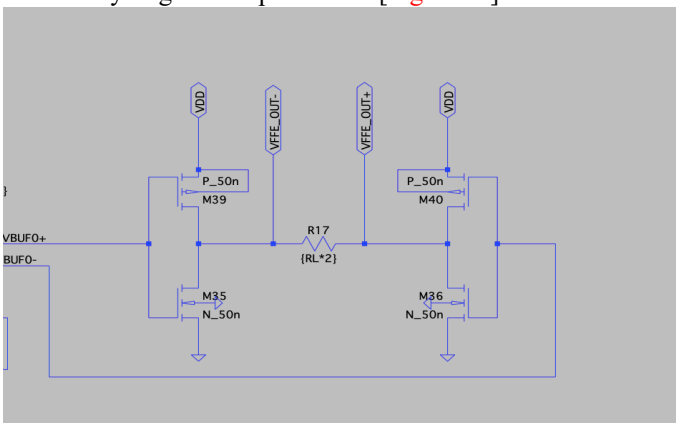


Figure 11, SST driver

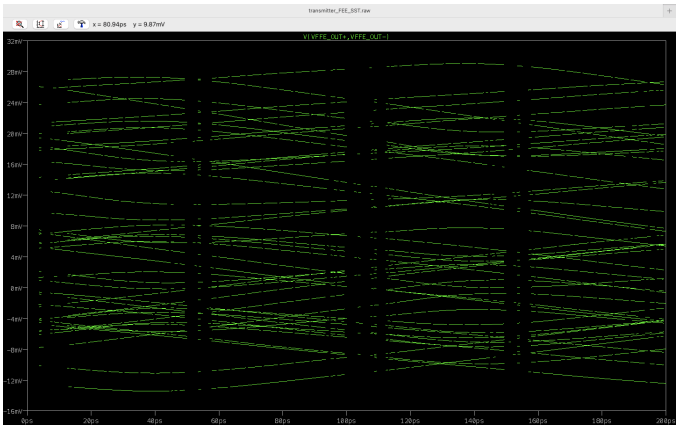


Figure 12

When adjust the SST transistor width to 4um, ISI could be reduced [Figure 13], but it is done at the cost of enlarging transistor resistance value to about 900Ω, meanwhile, signal current is reduced to a very large extend, the voltage swing is around [-8mv, +8mv] compared to CML driver voltage swing [-60mv, +60mv], also the VEO from SST is not better than that of using CML driver [Figure 14]. Generally speaking, using SST driver is for the sake of power perspectives while the output swing and ISI performance are still good enough. To achieve this effect, we need transistor resistance reaching the value closed to on chip resistance so that the current flowing into the driver could be reduced compared to using CML driver. However, this simulation using 10Gb/s signal could not be achieving the expected effect while keeping lower ISI and moderate output signal swing. Therefore, this simulation test adopted CML driver in transmitter side and the achieved signal [Figure14] is accepted to be further tested on wire line.

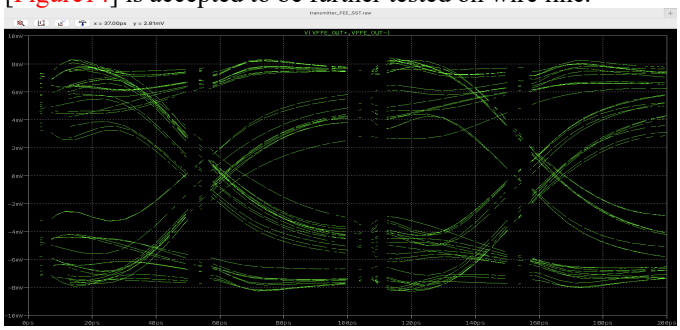


Figure 13, SST driver with MOSFET width at 4um

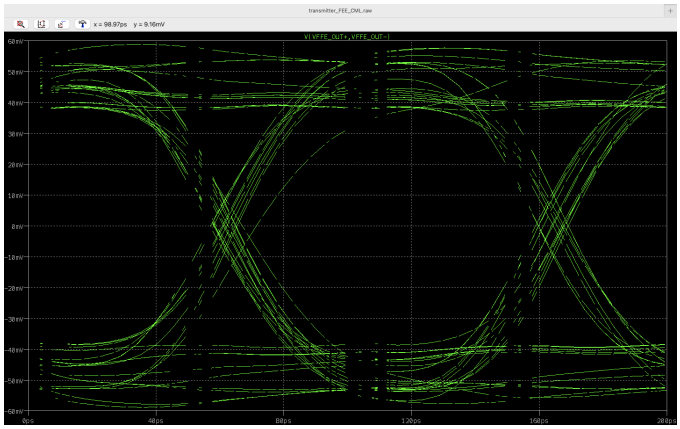
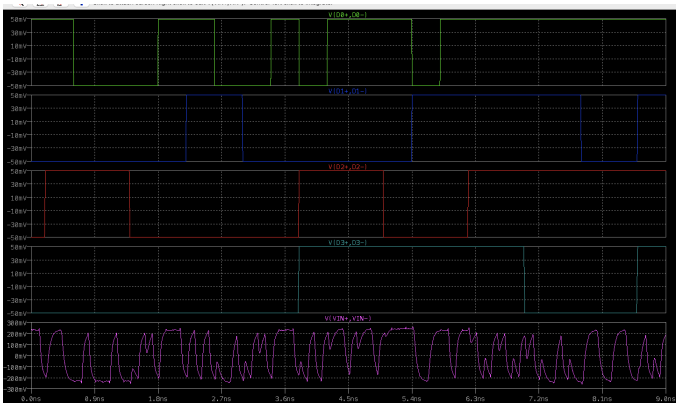


Figure 14, CML driver with MOSFET width at 4um

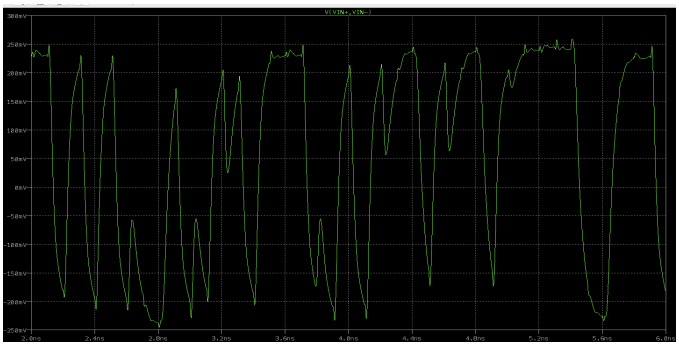
Transient signal of Feed Forward Equalizer explanation:

There are more transient responses between the signal input at 2.5Gb/s and FEE output at 10Gb/s, these signal plot in time domain could be able to explain how random 2.5Gb/s signal is transmitted through the multiplexer and CML driver and final combined to the desirable signal.

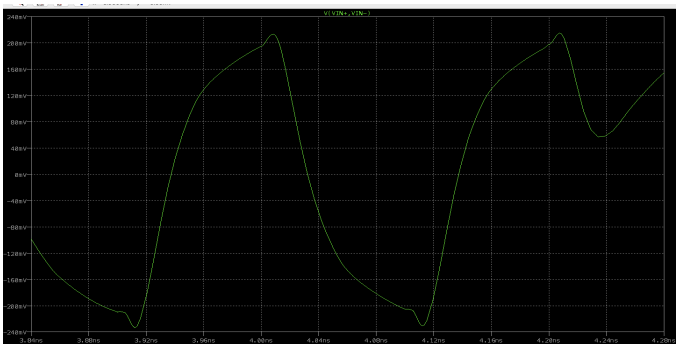
Multiple plots as following.



4 random signals with 2.5Gb/s at input and 10Gb/s signal at MUX output

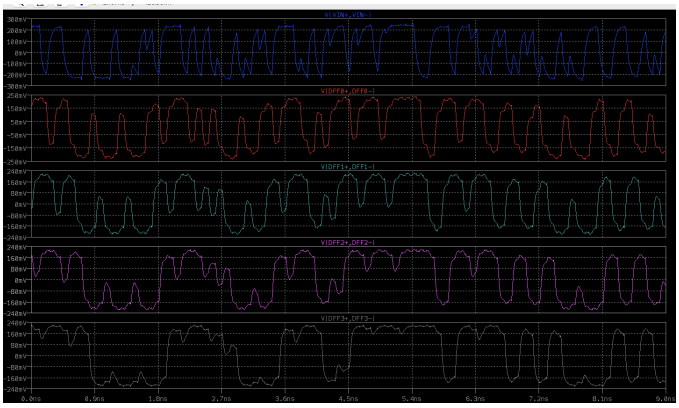


MUX output signal at 10Gb/s



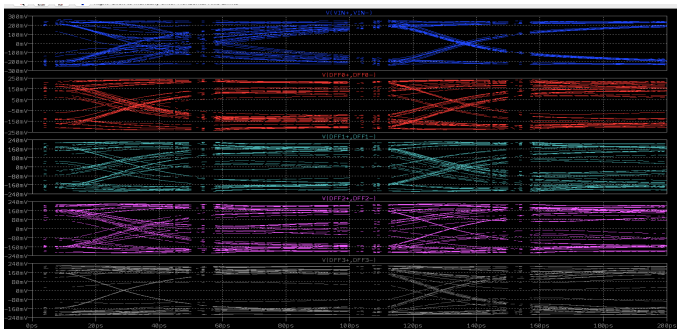
MUX output pulse response at 10Gb/s

Mux output signal as the data signal has large ISI, so it need three equalizer taps to cancel the interferences.



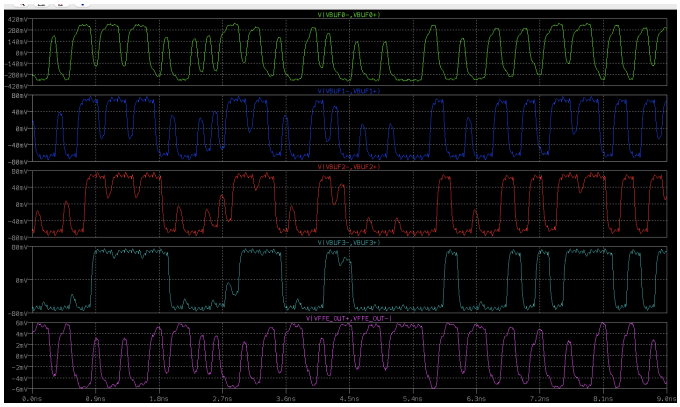
Time Pulse signal for MUX output and each DFF output

Each DFF is to delay the transmission signal by one UI period, so as to make the subsequent signal equaled to i(d-1), i(d-2) and i(d-3), which are to be subtracted by main signal id.



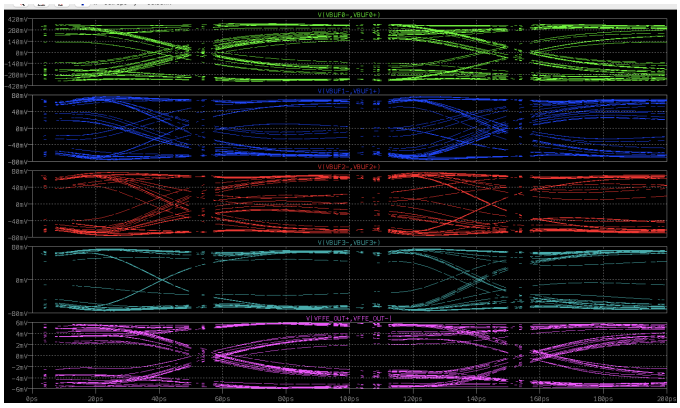
Eye diagram for Mux output and DFF output

From the above plot, we can find out the MUX signal has larger ISI. (the top blue one)



Time pulse of FEE output and each buffer Amp output.

Each buffer output before the tap could be treated as the delayed and scaled version of the previous buffer signal. After main signal subtracts these delayed and scaled signals, the FEE output shows at the bottom.



Eye diagram for FEE output and each buffer output

Transmission Line:

[Figure 15] shows the transmission line model used in the amplifier. This circuit requires the use of series RL loads and parallel RC loads. The output of the circuit coming from the line driver was analyzed using an frequency response and time pulse response view and the result was the diagram shown in [Figure 16,17].

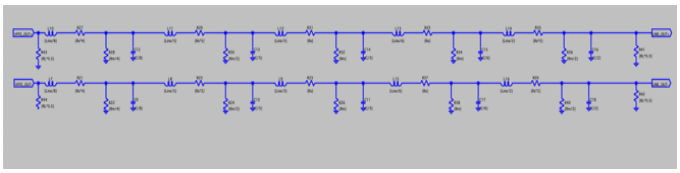


Figure 15

This transmission line used non-uniform 5 section of combined components. The parameter is each component is set at: L=5nH, C=1pF, Rs=4Ω, Gm=3mS. Each set of components are scaled by different value, but is keeping the characteristic impedance equaled to 50Ω. Two sides of the line are added with resistor value 25Ω and 15Ω, which models the unmatching transmission in reality. The time pulse response shows that this unmatching transmission line has ISI around 0.43 with normalized signal [Figure 16], while the frequency response gives the -3dB bandwidth around 1.49GHz at 10Gb/s data rate [Figure 17].

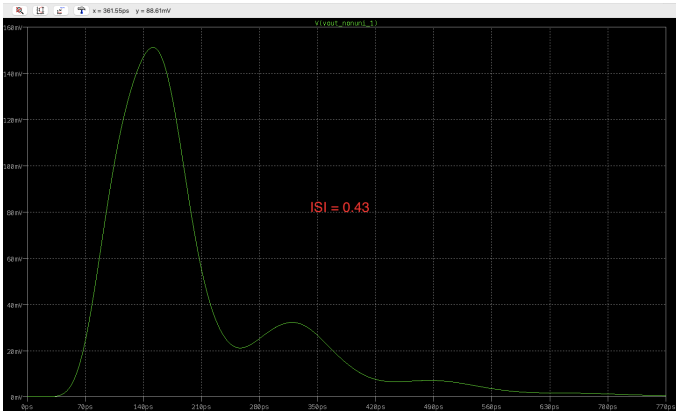


Figure 16

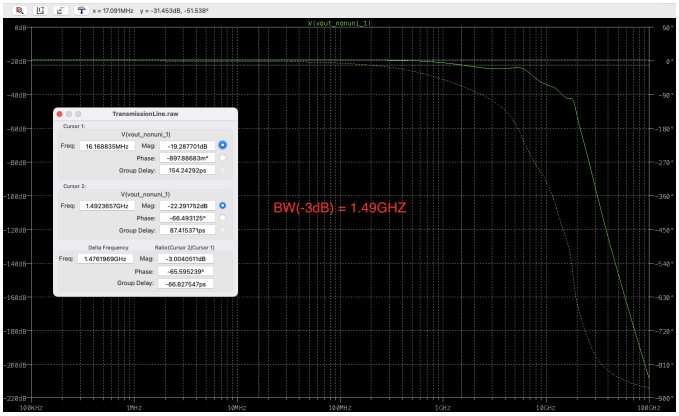


Figure 17

At the bandwidth of only 15% of data rate, the input signal is expected to be attenuated with large distortion as showed in [Figure 18].

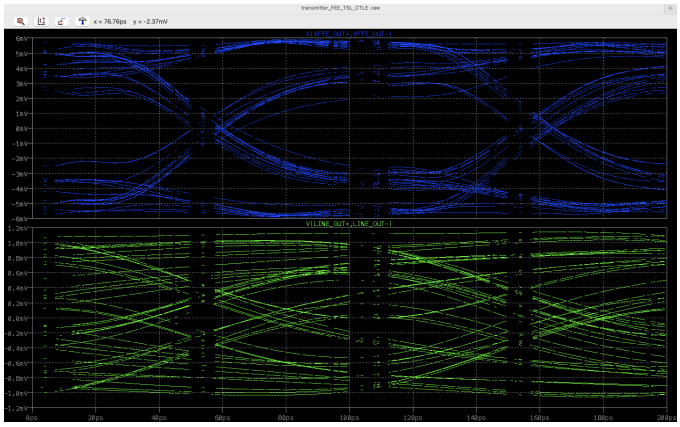


Figure 18

The blue one is the input signal at Transmission Line and the green one is the output signal at the other side of line. With this transmission line model, we are now moving to receiver side equalizer, which is expected to recover the distorted signal from the wireline.

Continuous Time Linear Equalizer:

The receiver side is composed by a continuous time linear equalizer. The CLTE is composed by 3 stages, stage one is conventional current biased (1mA) CML amplifier with 8um width and load of 750Ω NMOS, this is to gives amp gain equaled to 4. Stage two is inductive peaking CML amplifier with 2 um NMOS and stage three is a negative impedance convertor with 20um NMOS. The inductive peaking damping factor is 0.707. Stage two and three are voltage biased by using transistors behaving as switches at virtual ground source [Reference 3]. One Ac coupling capacitor is set with value of 2pF, which is to address the high frequency disturbing issue. [Figure 19]

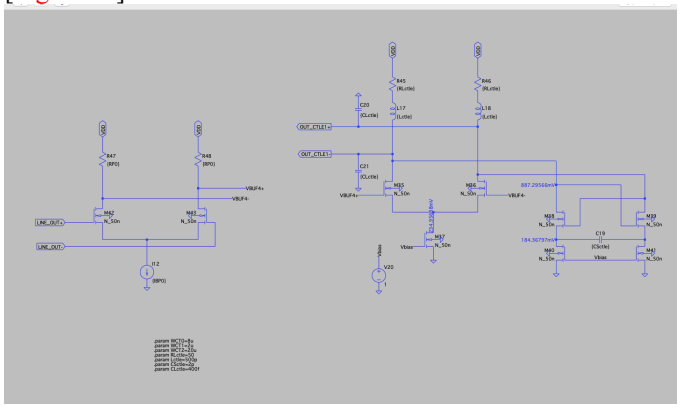


Figure 19

The first stage CML amp is to catch the signal from transmission line, the stage two inductive peak CML is to enlarge the signal at higher frequency and the stage three negative impedance is to amplifier the signal at lower frequency [Reference 3]. One Ac coupling capacitor make negative impedance working at lower frequency. The time pulse response and eye diagram are plotted as following [Figure 20, 21]:

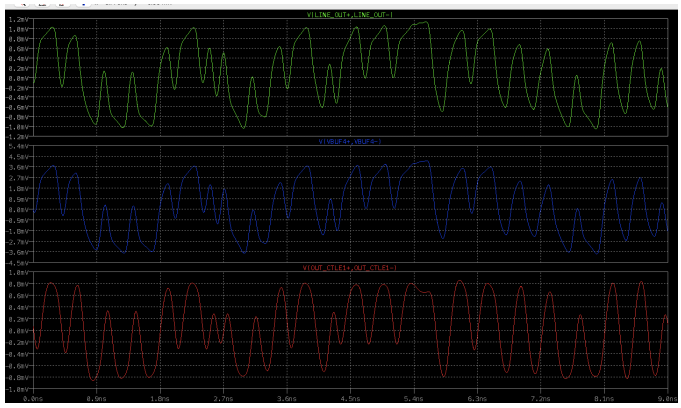


Figure 20, TSline_output VS buffer output VS CTLE output

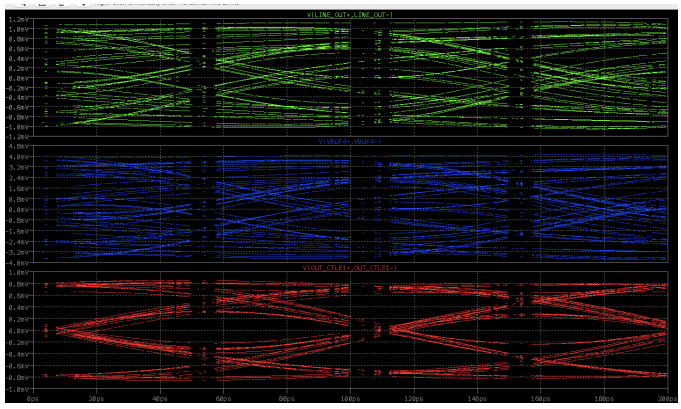


Figure 21, Eye diagram for TSLine_out, Buffer out and CTLE out

As the above plot, we can find the transmission line output (top green one) has very large ISI, and its signal swing is around ||1.2 mv|| only, which is not big enough to let decision circuit to catch the signal. After the first stage CML amp, the signal (middle blue one) swing is enlarged to around ||4.8 mv||, but eye is still closed at this point. The signal passes through CTLE equalizer, and the voltage swing (bottom red one) is reduced to around ||0.8 mv||, but the eye is opened. The VEO is about 0.6mv, and the ISI is about 0.625 with the normalized signal swing.

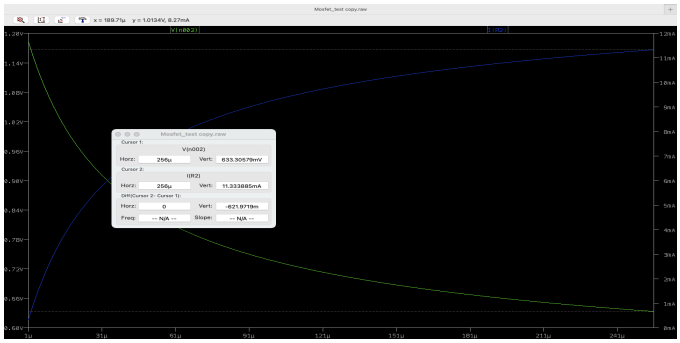
III. Conclusion

In conclusion, the CML implementation is used for multiple different types to circuits. It is proven that it works well to multiplex two square waves while showing the impact of selection that the system has on the output by relation to the input signals by parts. Three 2-to-1 MUXs are able to produce the same selective behavior as a 4-to-1 MUX while smoothing out the edges regardless of some signal noise. *The FFE* portions of the circuit (made from CML design) take the output supplied by the MUX and order the used signal into a

slightly less distorted function with constant high and low peaks per cycle. The transmission line, designed using RLC loads instead, amplified the signal such that it becomes less cluttered and loses noise. The. Placed into the CTLE, the wave forms that took similar pattern from the multiplexer output are now less noisy although there were some dissolution issues faced in developing the driver model. The basic functions defined by what the circuits are supposed to be are present in the design of this system, and although these issues did exist and may have resulted in an odd output shape, it does not completely detract from the general functions of each part. There are still something which need to be improved. The CTLE output has ISI about 0.625, which is larger than ISI of FEE output at around 0.5, in order to reduce ISI furthermore, some receiver side equalizers are need to release the designing burden from CTLE and FEE, the potential option could be using Decision Feedback Equalizer, but this is being presented in this report.

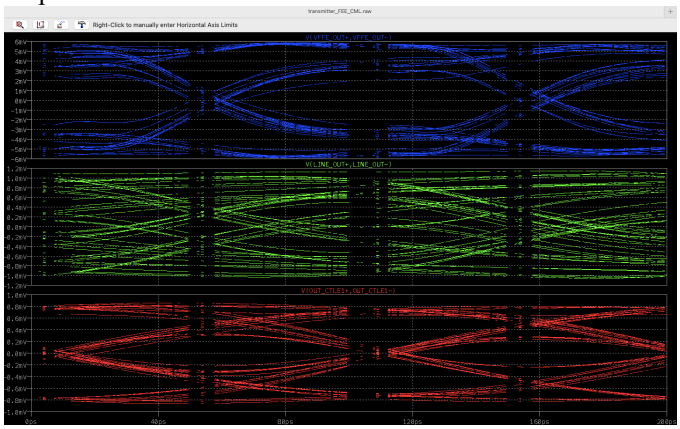
APPENDIX

The following plot shows PMOS resistance is expected to reach around 53Ω when width at 256um and length at 50nm.

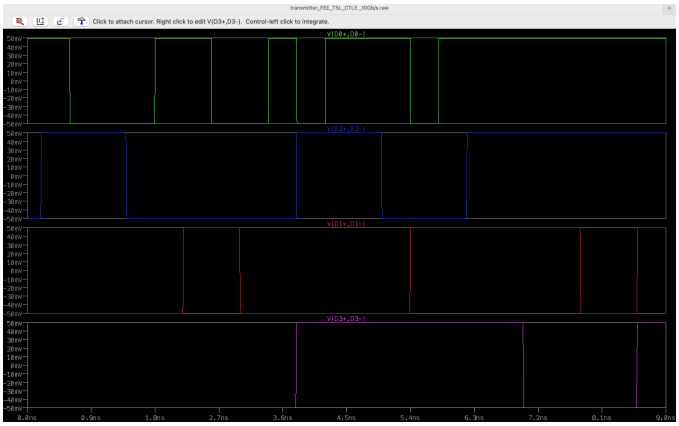


MOSFET resistance value swept by Width

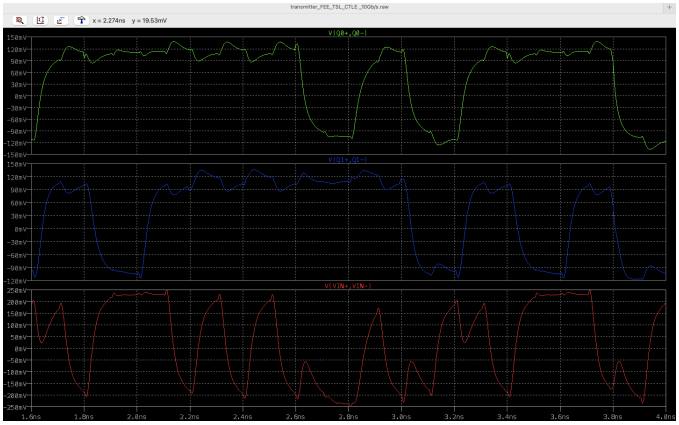
General eye diagram for FEE output, TS line output and CTLE output. Showed below:



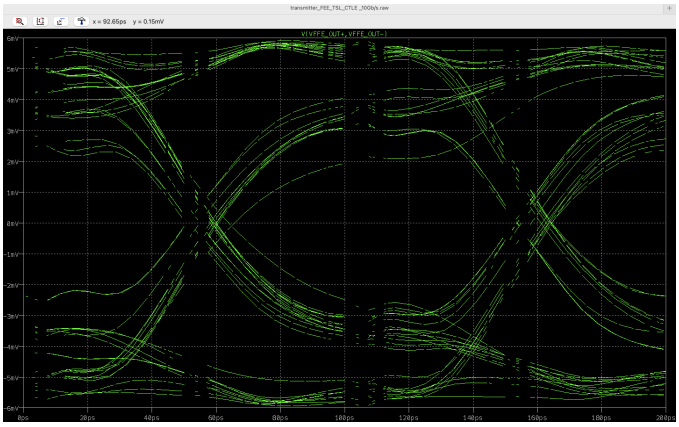
Fee Output (blue one), Line output (green one), CTLE output (red one)



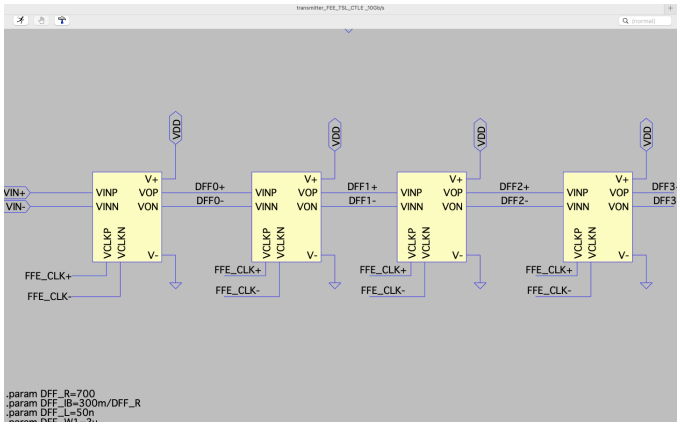
4 random signals at 2.5Gb/s



2-1 multiplexer 1 output (green one), 5Gb/s
2-1 multiplexer 2 output (blue one), 5Gb/s
2-1 multiplexer 3 output (red one), 10Gb/s



FEE output Eye diagram using single RC load on CML driver.



4 DFF pairs used to connect 4 equalizer taps

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A 40Gb/s 860_W Single-Phase 4:1 Multiplexer in 45nm CMOS, Elkim Roa and Byunghoo Jung School of Electrical and Computer Engineering - Purdue University, elkim,jungb@purdue.edu, 2013

Reference 3.

A 10-Gb/s Low-Power Low-Voltage CTLE Using Gate and Bulk Driven Transistors, Amin Aghighi*, Abdul Hafiz Alameh**, Mohammad Taherzadeh-Sani*, and Frederic Nabki, Ferdowsi University of Mashhad, Mashhad, Iran**,** École de technologie supérieure (ETS), Montréal, Canada, 2016.

Reference 4.

Figure 6 and Logic Function Implementation with a 4:1 Multiplexer. Oreilly (2021). Retrieved from: "*https://www.oreilly.com/library/view/introduction-to-digital/9780470900550/chap7-sec006.html"*