

# NM6007 Report

Fully Differential Wideband Amplifier

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# Contents

<b>1</b>	<b>Introduction</b>	<b>4</b>
<b>2</b>	<b>Theoretical Calculation</b>	<b>4</b>
2.1	Basing part . . . . .	4
2.2	Amplifier part . . . . .	6
2.3	Feedback part . . . . .	6
<b>3</b>	<b>Pre-simulation</b>	<b>7</b>
3.1	Transistor Characterization . . . . .	7
3.2	Parameter of transistor and resistor . . . . .	7
3.2.1	Biassing part . . . . .	8
3.2.2	Amplifier part . . . . .	9
3.2.3	Feedback part . . . . .	10
<b>4</b>	<b>Post-simulation</b>	<b>10</b>
4.1	Layout . . . . .	10
4.2	DRC - Design Rule Check . . . . .	11
4.3	LVS - Layout Vs Schematic . . . . .	12
4.4	PEX - Parasitic Extraction . . . . .	12
<b>5</b>	<b>Result</b>	<b>13</b>
5.1	AC Differential Gain and Unity Gain Bandwidth in Different Corners . . . . .	13
5.1.1	Normal conditions . . . . .	14
5.1.2	-40°C . . . . .	15
5.1.3	100°C . . . . .	15
5.1.4	$V_{DD} = 1.5v$ . . . . .	16
5.1.5	$V_{DD} = 1.8v$ . . . . .	16
5.1.6	Slow-Slow . . . . .	17

5.1.7	Slow-Fast . . . . .	17
5.1.8	Fast-Slow . . . . .	18
5.1.9	Fast-Fast . . . . .	18
5.2	Common Mode Gain . . . . .	19
5.3	Output Voltage Swing . . . . .	20
5.4	Current Consumption . . . . .	21
5.5	Total Harmonic Distortion . . . . .	21
5.6	Settling Time . . . . .	22
5.7	Slew Rate . . . . .	24
5.8	CMFB Loop Unity Gain Bandwidth and Phase Margin . . . . .	25
5.9	Chip Area . . . . .	26
5.10	DO's and DON'Ts . . . . .	26
<b>6</b>	<b>Conclusion</b>	<b>28</b>
<b>7</b>	<b>Personal Score Sheet</b>	<b>29</b>
<b>8</b>	<b>Reference</b>	<b>30</b>

# 1 Introduction

In this NM 6007 lab project, we are asked to build a closed-loop fully differential amplifier with unity gain = 4. Professor Siek provided us schematic of basing, amplifier and feedback. What we need to do is analysing the usage of each component, generating theory parameters then testing it in pre-simulation. During simulation, parameters could be changed based on practical situation to fit our amplifier's standards which will mentioned in later section.

When passing the pre-simulation, we need to draw the layout based on schematic. There are two principles, keeping the area as small as possible and keep matching and symmetry without making. There will be two test during post-simulation DRC and LVS to check if our layout structure is correct. Then PEX will help us generate a parasitic capacitance configuration file to run post-simulation. The results of post-simulation are also need to fit our standards.

## 2 Theoretical Calculation

### 2.1 Basing part

The function of basing circuit is generating constant voltage which is not affected by environmental factors such as temperature as much as possible.

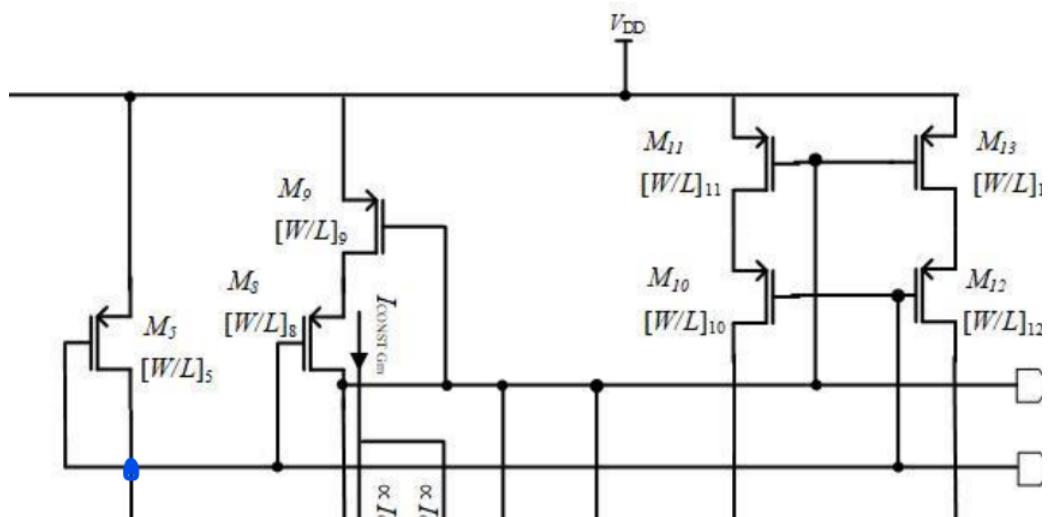


Figure 1: Wide swing cascode

The structure above is a wide swing cascode. The M5 here pull down the gate voltage M8 to  $V_{DD} - V_{tp} - \Delta v$ , then  $V_{DS}$  of M9, M11, M13 keep to  $\Delta v$  working on saturation region. According to instruction, the current go through M3 is half of M9, Thus

$$\sqrt{I_D} = \Delta v \text{ for M8 to M13}$$

$$\sqrt{\frac{1}{2}I_D} = 2\Delta v \text{ for M5}$$

So the  $\frac{W}{L}$  of M5 should around 8 times bigger than M8 to M13.

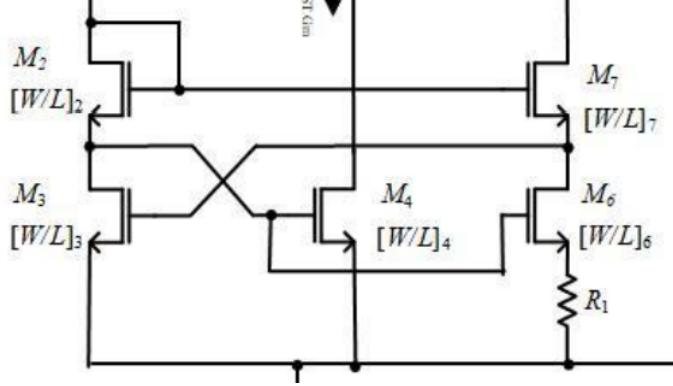


Figure 2: Constant gm

There are two constant gm bias circuit structure in biasing, I show one of them above. With the help of this structure, the gm can only depends on R1, ignoring influence from temperature and voltage variation. So the  $\frac{W}{L}$  of M6 should be four times  $\frac{W}{L}$  of M2,M3,M4 and M7. Same reason, the  $\frac{W}{L}$  of M17 should be four times  $\frac{W}{L}$  of M15,M16 and M18. At the same time, the current go through M15 is twice the current go through M7, so the  $\frac{W}{L}$  of them are also twice as related to each other.

The function of M14 is negative feedback. If  $V_{DD}$  increases, the current go through M15 will increase faster than M18's, because  $\frac{W}{L}$  of M17 is bigger. Then the gate voltage of M14 will go down, which will make current of M14 smaller. Later  $V_{DS}$  of M14 will increase,  $V_{GS}$  of M11 and M13 will decrease. Finally, the current go through M15 and M18 will decrease.

## 2.2 Amplifier part

Here we use a typical folded cascode structure, which can give us high bandwidth and output swing. The current go through M40,M41,M25 and M26 should be same to keep the circuit matching. Thus,  $\frac{W}{L}$  and multiplier of all P-Mos in amplifier part should be same. We set the current go through M21,M22,M25,M26 to I, then the current go through M29 and M30 should be 2I. M29, M30, M27 and M28 forms a current mirror with the P-Mos in basing part, so  $\frac{W}{L}$  of M29, M30 should be two times bigger than M27, M28. The transistors here, except input transistor M23 and M22, control the overall current, which is around 5 8 times the current of basing part. We need to increase the  $\frac{W}{L}$  of transistors 5 8 as needed based on the  $\frac{W}{L}$  in basing.

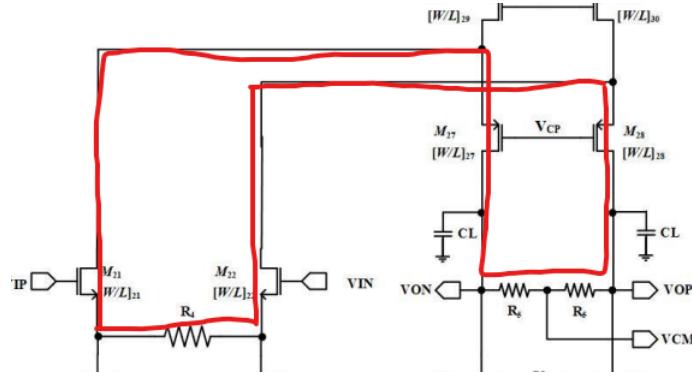


Figure 3: Loop circuit for small signal

R4, M21, M22, M27, M28, R5, R6 form a loop circuit for small signals like the figure above to amplify signals. After calculation, the gain is

$$\text{Gain} = \frac{2R_5}{gm+R_4}$$

The band width is

$$\text{Bandwidth} = \frac{1}{2\pi R_5 C_L}$$

Meanwhile, R4 is closely related to settling time and slew rate, so the value shouldn't be too small.

## 2.3 Feedback part

Feedback part is used to keep amplifier working in a stable level. M31, M32, M33, M34 should match to M23,M24,M25,M26, so keeping the parameters same. M35, M36 are the input transistor of feedback circuit,

whose  $\frac{W}{L}$  have relationship with CMFB gain, just making them big enough. The P-Mos M39 and M38 are used to generate stable voltage  $0.5V_{DD}$  called  $V_{REF}$ .  $V_{REF}$  works as a reference voltage for  $V_{CM}$  to keep it around  $0.5V_{DD}$ .

### 3 Pre-simulation

Pre-simulation is a simulation process without considering the layout which can generate various types of parasitic capacitors. In pre-simulation, we built our schematic, adjusted parameters for transistors, resistors and capacitors. The final simulation results should meet standards, which will show in later section.

#### 3.1 Transistor Characterization

The transistors we used in schematic is given by professor, so we need to  $K'_n$ ,  $K'_p$  and  $V_{tn}$  and  $V_{tp}$  at first. Since we have equation:

$$I_D = 0.5K_n \frac{W}{L} (V_{GS} - V_{tn})^2$$

$$\sqrt{I_D} = \sqrt{0.5K_n \frac{W}{L} (V_{GS} - V_{tn})}$$

we can find linear between relationship between  $\sqrt{I_D}$  and  $V_{GS}$ . Thus we can generate K and  $V_t$  through slope and intercept easily. After calculation, I got

$K'_n$	$K'_p$	$V_{tn}$	$V_{tp}$
0.0006042	7.7214	0.35449	0.39016

Table 1: Transistor Characterization

#### 3.2 Parameter of transistor and resistor

Based on theoretical analysis above, here is my parameters of element in circuit.  $\frac{360n}{180n}$ .

### 3.2.1 Biasing part

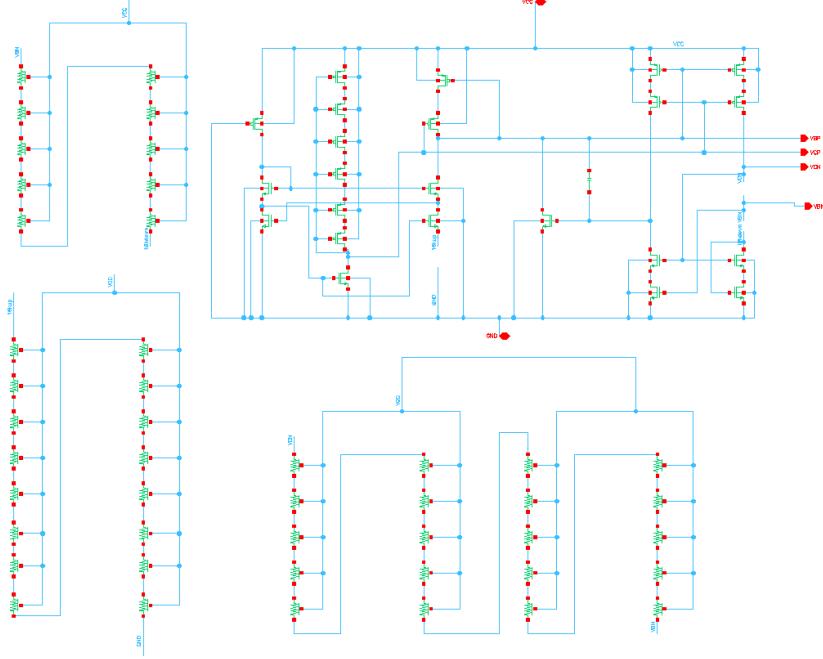


Figure 4: Biasing circuit

P-Mos		N-Mos	
M8,M9,M10,M11,M12,M13	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 4	M15,M16,M18	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 2
M1	$\frac{W}{L} = \frac{0.22u}{0.66u}$ M = 1	M2,M3,M4,M7	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 1
M5	$\frac{W}{L} = \frac{0.22u}{0.66u}$ M = 2, 6 series connecting	M6	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 4
		M14	$\frac{W}{L} = \frac{0.36u}{1.44u}$ M = 1

Table 2: Parameters table of Basing circuit

There are also 1 capacitor  $C_{c1}$  and 3 resistors  $R_1, R_2, R_3$ . I set  $\frac{W}{L}$  of  $C_{c1}$  to  $\frac{12u}{12u}$ , whose capacitance is equal to 0.463 pF. As for 3 resistors, each of their  $\frac{W}{L}$  is  $\frac{0.8u}{2u}$ , whose resistance is equal to 1.0297K Ohm. Here I put 16 resistors in series to build  $R1 = 16.4752$ K Ohm, put 20 resistors in series to build  $R3 = 20.594$ K Ohm, put 10 resistors in series to build  $R2 = 10.297$ K Ohm

### 3.2.2 Amplifier part

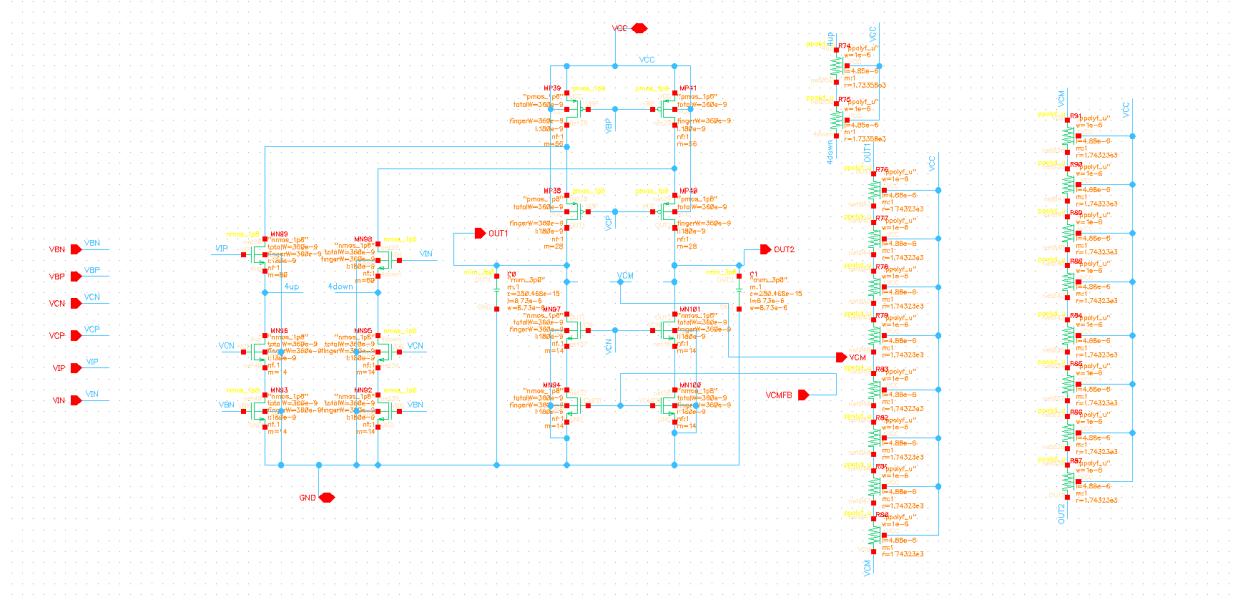


Figure 5: Amplifier circuit

P-Mos		M-Mos	
M27,M28	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 28	M23,M24,M25,M26,M19,M20,M40,M41	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 14
M29,M30	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 56	M21,M22	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 80

Table 3: Parameters table of Amplifier circuit

1 capacitor  $C_{cl}$  here, set  $\frac{W}{L} = \frac{8.73u}{8.73u}$ , C = 0.25 pF. 3 resistors  $R_4, R_5, R_6$  here. R4 is consist of 2 resistor in series, each of their  $\frac{W}{L} = \frac{1u}{4.85u}$  R = 1.7336K Ohm, the total resistance of R4 = 3.4672K Ohm. Both of R5 and R6 is consist of 8 resistors in series, each of their  $\frac{W}{L} = \frac{1u}{4.88u}$  R = 1.74323K Ohm, the total resistance of R5 = 13.94584K Ohm.

### 3.2.3 Feedback part

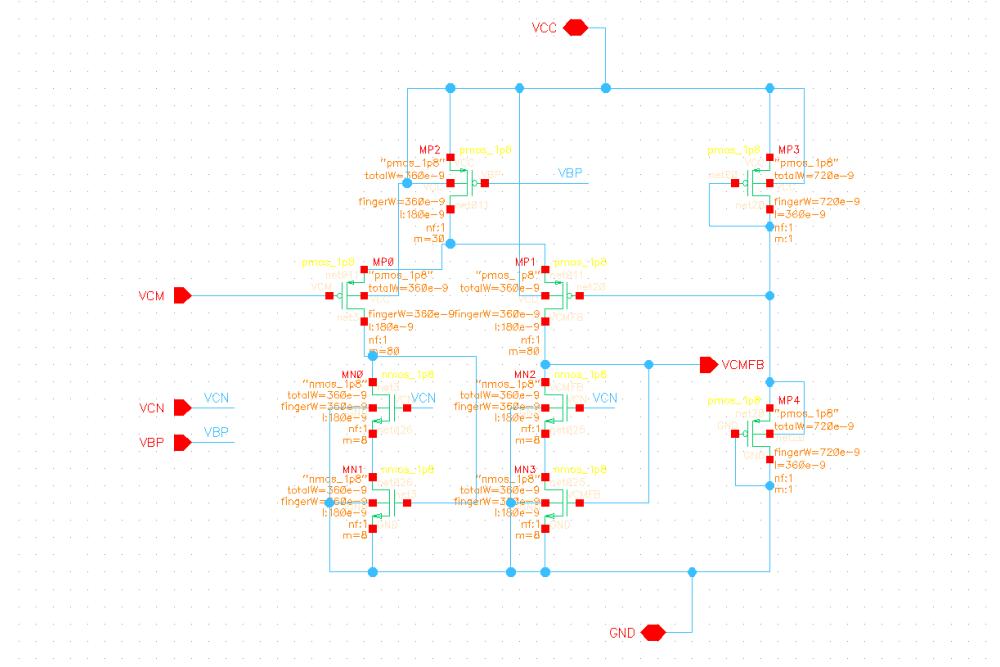


Figure 6: Feedback circuit

P-Mos		N-Mos
M35,M36	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 80	M31,M32,M33,M34
M38,M39	$\frac{W}{L} = \frac{0.72u}{0.36u}$ M = 1	$\frac{W}{L} = \frac{0.36u}{0.18u}$ M = 8

Table 4: Parameters table of Feedback circuit

## 4 Post-simulation

Post-simulation is a simulation process that depending not only on your schematic but also your layout. A good matching layout structure can mitigating the effects of parasitic capacitance on the layout. circuit.

### 4.1 Layout

The layout needs to meeting the following requirements.

1. Maintain the specified distance between materials.

2. Add guard ring every two transistor rows.
3. The structure needs to be as symmetrical as possible. Matching the most important thing in analog circuit design.

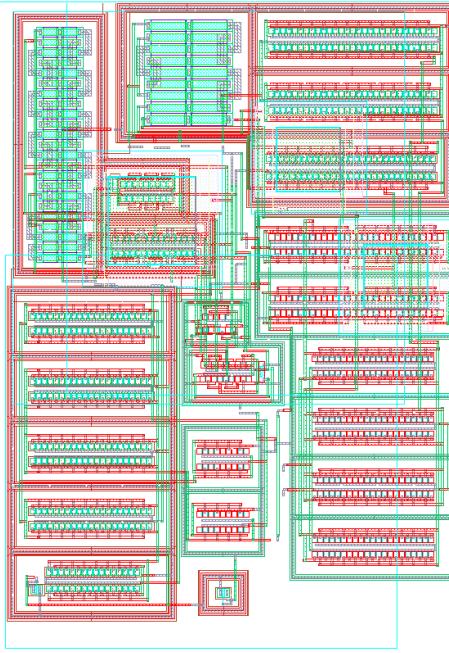


Figure 7: Layout

## 4.2 DRC - Design Rule Check

DRC is a process to check if the distance between each material is bigger than minimum distance.

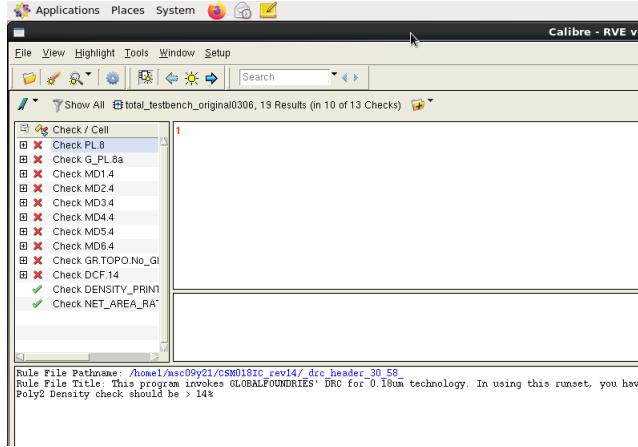


Figure 8: Design Rule Check

### 4.3 LVS - Layout Vs Schematic

LVS is used to check whether the connection of the layout is consistent with the schematic.

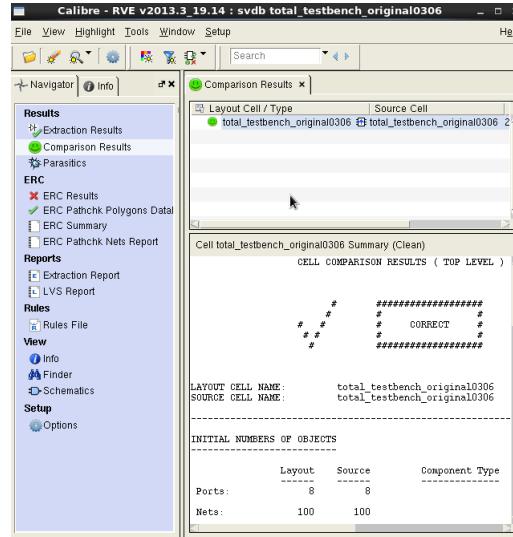


Figure 9: Layout vs Schematic

### 4.4 PEX - Parasitic Extraction

After running the DRC and LVS without error, we can run PEX to generate a parasitic capacitance configuration file which can replace schematic file to run simulation.

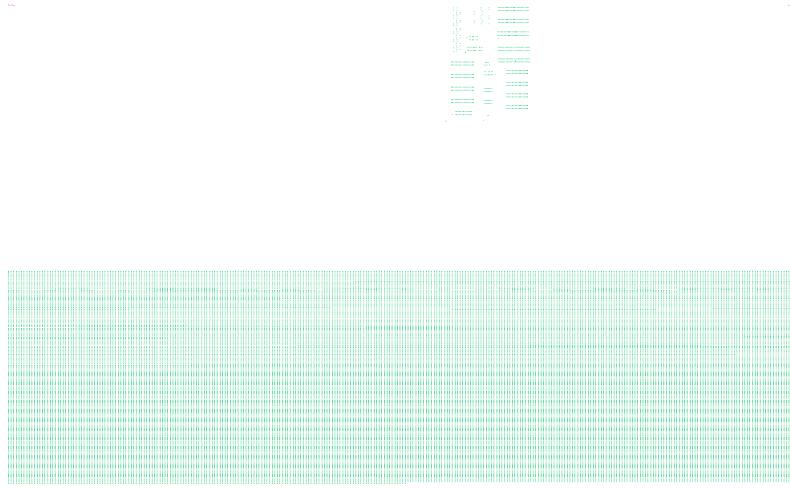


Figure 10: Configuration file after Pex

## 5 Result

In our project, there are several standard we should follow as the figure below.

I'll explain them one by one and give my results got from pre-simulation and post-simulation.

### 5.1 AC Differential Gain and Unity Gain Bandwidth in Different Corners

Gain is the basic parameter to describe any differential amplifier. In the ideal case, it equal to the ratio of output and input amplitude of small signal. The equation is  $A_d = \frac{V_{out}}{V_{in}^+ - V_{in}^-}$ . According to our requirements, our differential mode gain needs to be  $4\pm5\%$  (3.8~4.2), or in dB 11.6dB~12.46dB.

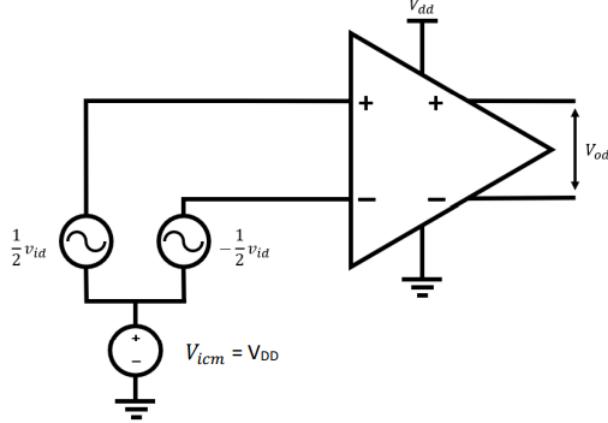


Figure 11: AC Differential Gain and Unity Gain Bandwidth Testing

Unity gain bandwidth is the standard for evaluating the operating frequency of the amplifier. In general, we should increase it as much as possible. From theory, the gain will decrease if we increase the working frequency. Thus, when the differential gain reducing to 1 or 0dB, the frequency at this point is unity gain bandwidth. In this project, our standard is greater than 90 MHz.

At the same time, we have added some requirements to the amplifier's ability to cope with environmental changes. The amplifier should work stably when temperature changes from -40°C to 100 °C, supply voltage changes  $V_{DD}$  from 1.5v to 1.8v, as well as different corners.

### 5.1.1 Normal conditions

The amplifier working at 60°C, and  $V_{DD} = 1.6v$ . From the figure below, we can find, in pre-simulation, the differential gain is 12.3034dB, with unity gain bandwidth equaling to 169.192MHz. In post-simulation, the differential gain is 12.0355dB, with unity gain bandwidth equaling to 147.301MHz.

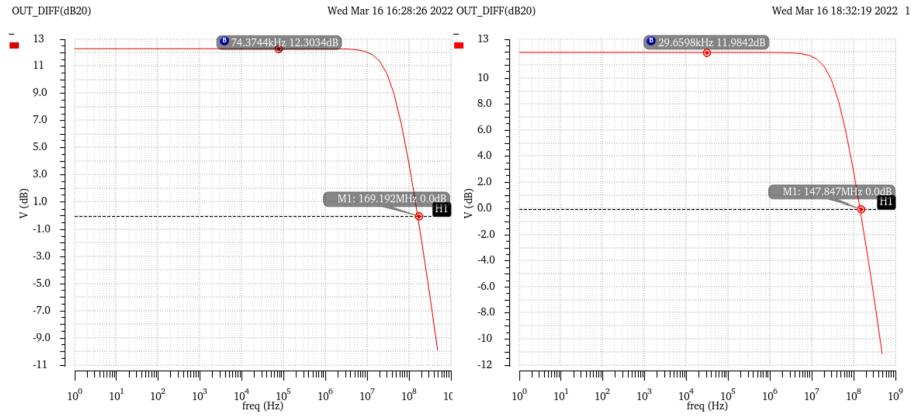


Figure 12: Pre-simulation vs Post-simulation in normal conditions

### 5.1.2 -40°C

From the figure below, we can find, in pre-simulation, the differential gain is 12.4438dB, with unity gain bandwidth equaling to 170.253MHz. In post-simulation, the differential gain is 12.1412dB, with unity gain bandwidth equaling to 147.175MHz.

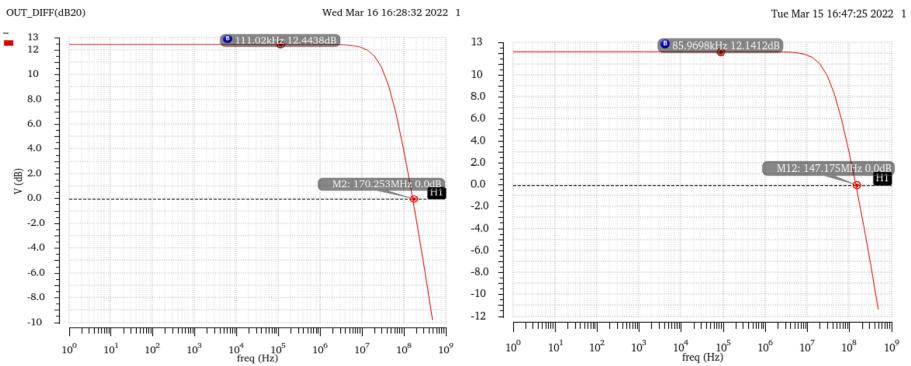


Figure 13: Pre-simulation vs Post-simulation in -40 degree

### 5.1.3 100°C

From the figure below, we can find, in pre-simulation, the differential gain is 12.19dB, with unity gain bandwidth equaling to 167.448MHz. In post-simulation, the differential gain is 11.9431dB, with unity gain bandwidth equaling to 146.377MHz.

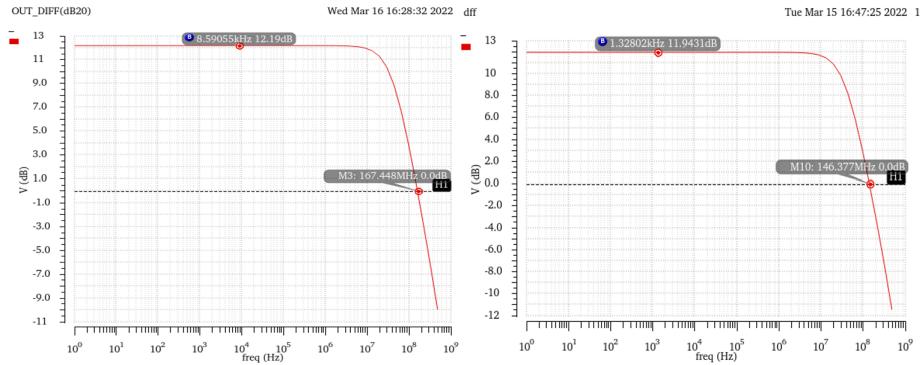


Figure 14: Pre-simulation vs Post-simulation in 100 degree

#### 5.1.4 $V_{DD} = 1.5v$

From the figure below, we can find, in pre-simulation, the differential gain is 12.1615dB, with unity gain bandwidth equaling to 166.639MHz. In post-simulation, the differential gain is 11.9081dB, with unity gain bandwidth equaling to 145.626MHz.

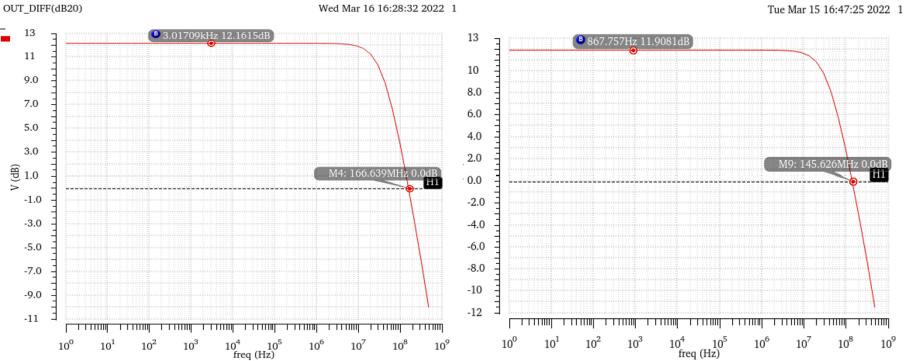


Figure 15: Pre-simulation vs Post-simulation when  $V_{DD} = 1.5v$

#### 5.1.5 $V_{DD} = 1.8v$

From the figure below, we can find, in pre-simulation, the differential gain is 12.4904dB, with unity gain bandwidth equaling to 172.699MHz. In post-simulation, the differential gain is 12.1648dB, with unity gain bandwidth equaling to 150.196MHz.

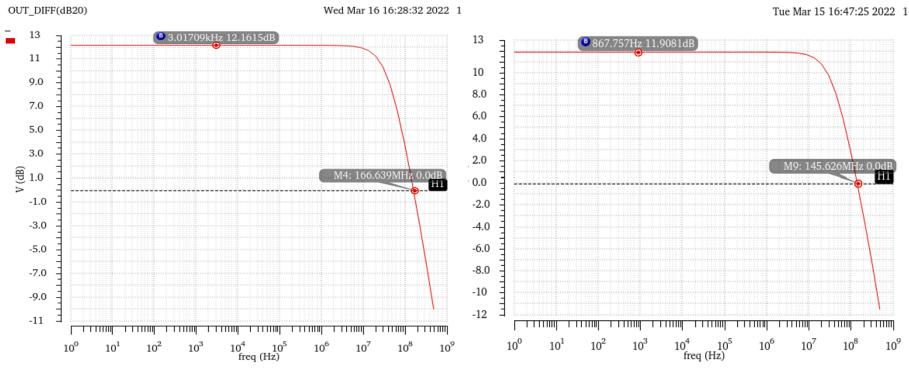


Figure 16: Pre-simulation vs Post-simulation when  $V_{DD} = 1.8v$

### 5.1.6 Slow-Slow

From the figure below, we can find, in pre-simulation, the differential gain is 12.2438dB, with unity gain bandwidth equaling to 166.544MHz. In post-simulation, the differential gain is 11.9397dB, with unity gain bandwidth equaling to 146.713MHz.

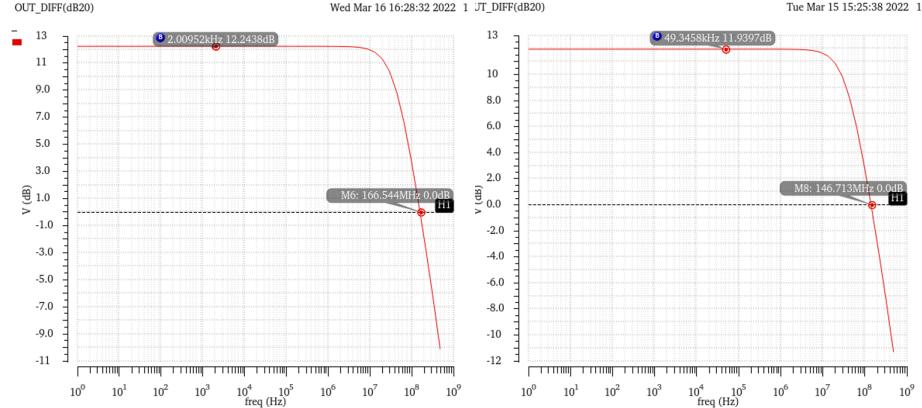


Figure 17: Pre-simulation vs Post-simulation Slow-Slow

### 5.1.7 Slow-Fast

From the figure below, we can find, in pre-simulation, the differential gain is 12.1856dB, with unity gain bandwidth equaling to 170.154MHz. In post-simulation, the differential gain is 11.8836dB, with unity gain bandwidth equaling to 148.225MHz.

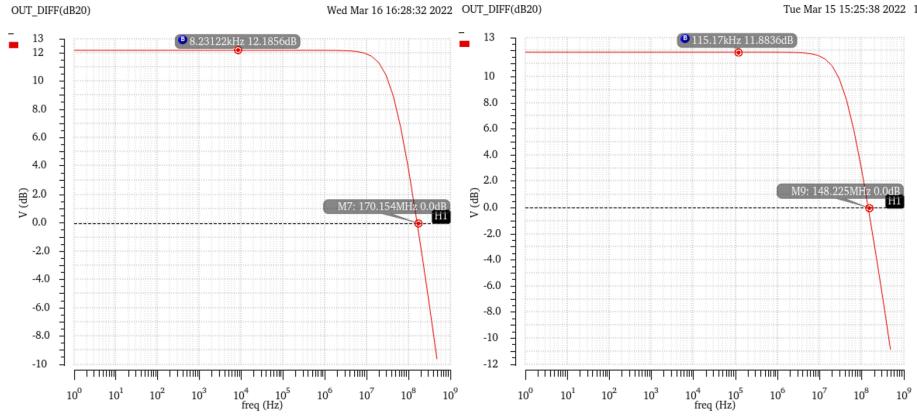


Figure 18: Pre-simulation vs Post-simulation Slow-Fast

### 5.1.8 Fast-Slow

From the figure below, we can find, in pre-simulation, the differential gain is 12.2832dB, with unity gain bandwidth equaling to 166.321MHz. In post-simulation, the differential gain is 11.9553dB, with unity gain bandwidth equaling to 146.134MHz.

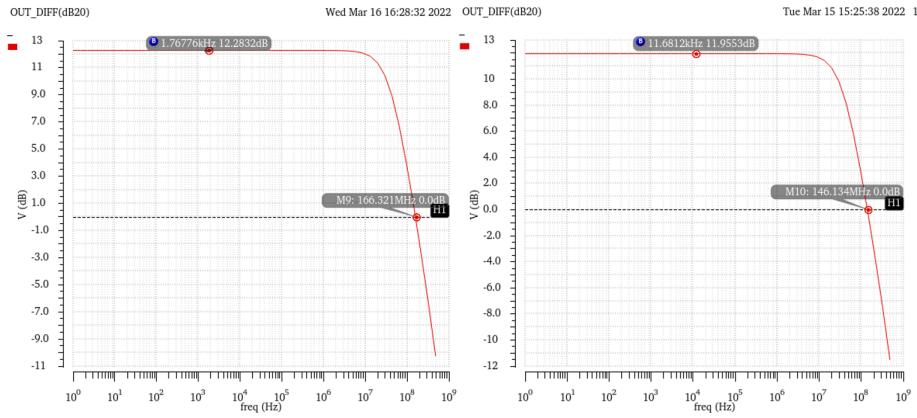


Figure 19: Pre-simulation vs Post-simulation Fast-Slow

### 5.1.9 Fast-Fast

From the figure below, we can find, in pre-simulation, the differential gain is 12.2775dB, with unity gain bandwidth equaling to 170.742MHz. In post-simulation, the differential gain is 11.9486dB, with unity gain

bandwidth equaling to 148.221MHz.

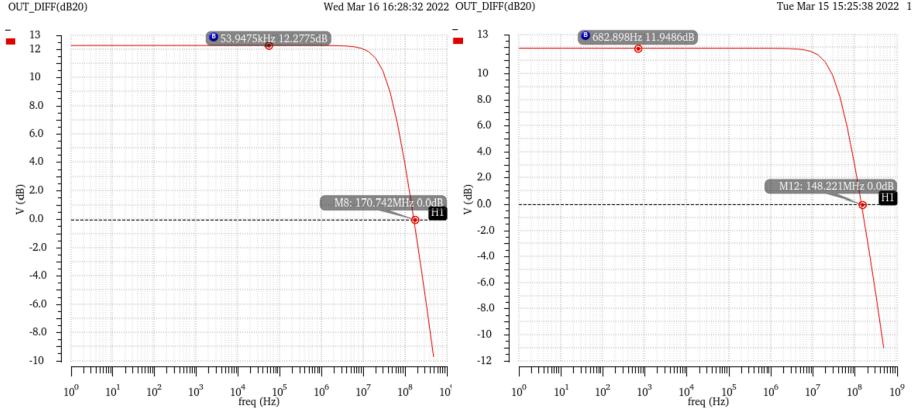


Figure 20: Pre-simulation vs Post-simulation Fast-Fast

## 5.2 Common Mode Gain

As we mentioned above, we can roughly estimate the amplitude of the output voltage using differential gain in ideal case. However, in practical, another parameter called common mode gain also effect our output. The equation of output voltage in the real world case is

$$V_{out} = A_d(V_{in}^+ - V_{in}^-) + A_{cm} \frac{V_{in}^+ + V_{in}^-}{2}$$

Thus we need to minimize the common mode gain  $A_{cm}$ . From the standard of this project, our common-mode gain should less than -30 dB in pre-simulation and less than -24 in post-simulation in different corners and environment variation.

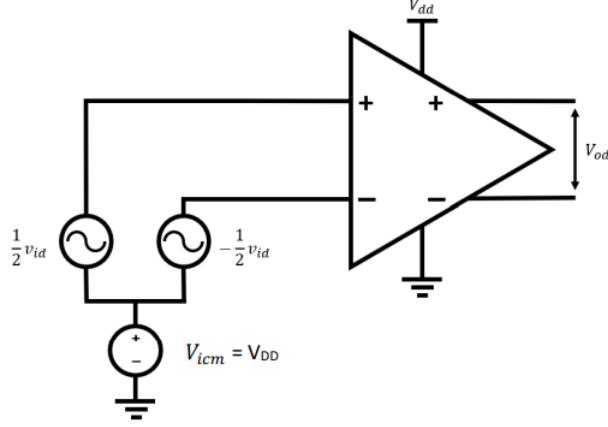


Figure 21: Common Mode Gain Testing

From the figure below, we can find, in pre-simulation, the common mode gain of  $V_{op}$  is -54.953dB,  $V_{on}$  is -54.953dB. In post-simulation, the common mode gain of  $V_{op}$  is -54.219dB,  $V_{on}$  is -55.993dB.

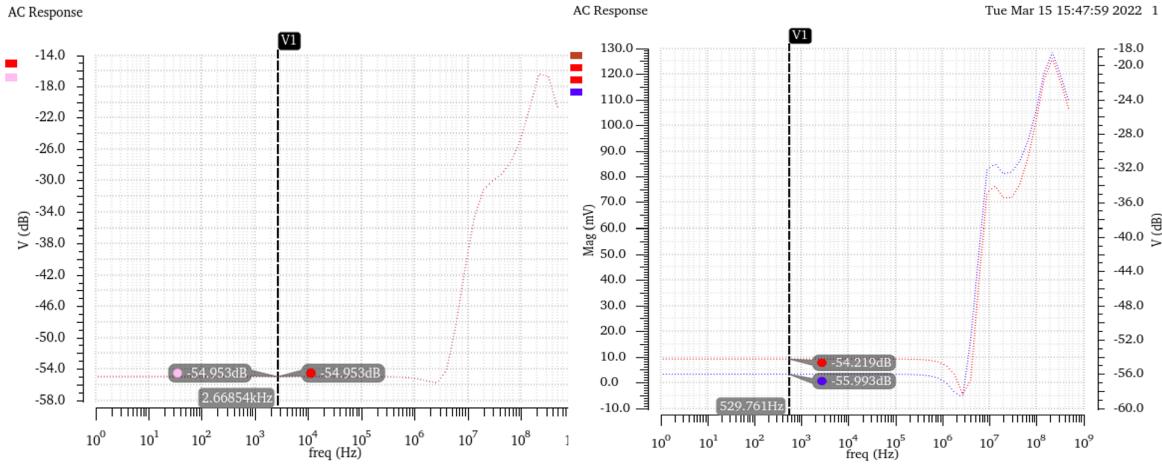


Figure 22: Pre-simulation vs Post-simulation Common-mode Gain

### 5.3 Output Voltage Swing

Output swing is used to describe the range between highest output voltage and lowest output voltage. This, of course, has the prerequisite that the voltage waveform needs to be a distortion-free sine signal (since our input signal is sine signal), at the same time, we need to ensure that all mos tubes are working in the saturation area. Because the process and requirements of the measurement are too complex, we only require

the output voltage swing in pre-simulation. With the help of TA, my output voltage swing is 0.45v 1.15v, meeting the requirement.

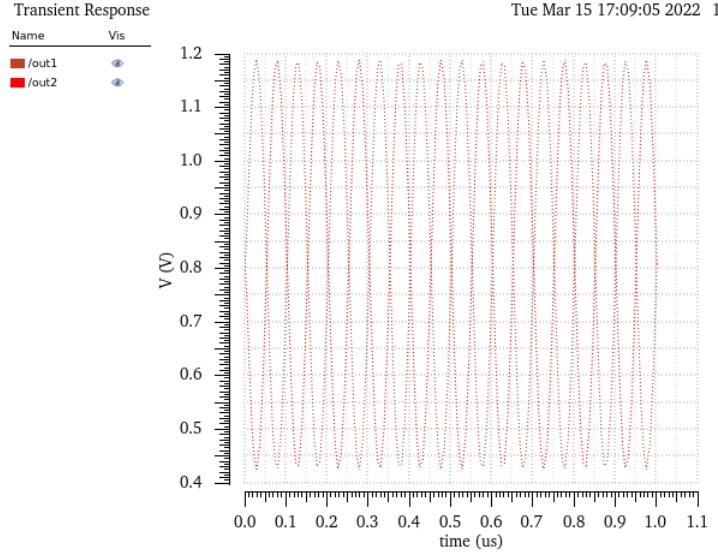


Figure 23: Output Voltage Swing

#### 5.4 Current Consumption

The current goes through supply voltage  $V_{DD}$ . In pre-simulation, my current consumption is 392.815uA. In post-simulation, it's 368.397uA like the figure below.

#### 5.5 Total Harmonic Distortion

Total harmonic distortion is an indicator that describes the degree of distortion of the output signal. A linear amplifier system is of course the best result, however, in the real world, most system are non-linear, which means the output can be written as a Taylor expansion.

$$V_o(t) = a_1 V_{in}(t) + a_2 V_{in}^2(t) + a_3 V_{in}^3(t) + \dots$$

The  $a_1 V_{in}(t)$  part is the essential part, while others are distortion parts. After some processes, we can transfer every  $a_n A \sin^n(\omega t)$  to  $H_{Dn} \sin(n\omega t)$ . Then we can write THD formulation here.

$$THD = 10 \log \left( \frac{H_{D2}^2 + H_{D3}^2 + H_{D4}^2 + \dots}{H_{D1}^2} \right)$$

From the equation above, smaller THD means the ratio between distortion parts and essential part are smaller, which means less distortion. In our project, the THD should less than -50 dB in pre-simulation, and less than -46 dB in post-simulation part.

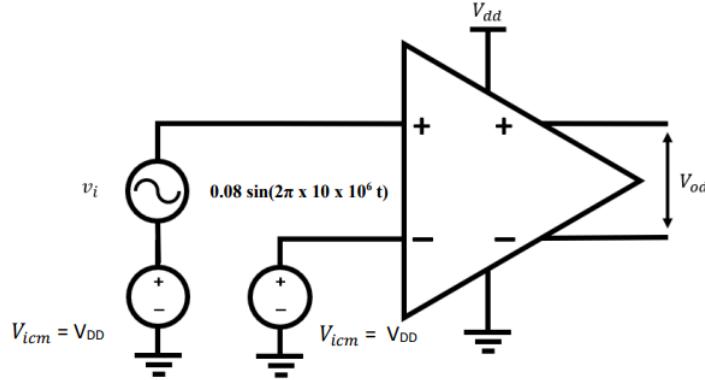


Figure 24: THD Testing

In my test, I got THD = -57.21 dB in pre-simulation part, and THD = -56.62 dB in post-simulation part. Working pretty well.

## 5.6 Settling Time

Settling time is an indicator time that takes for the output voltage to reach stability, or in other words, output voltage stays within a error band.

For example, from the figure below, we can find, because of parasitic capacitance, the voltage fluctuates up and down before stabilizing. Thus, The difference between the time point that finally enters and stabilizes in the error band (0.2% in our project) and the point of time when the input signal starts is the settling time. We need to minimize settling time to reduce setup time, to make the whole circuit system more stable.

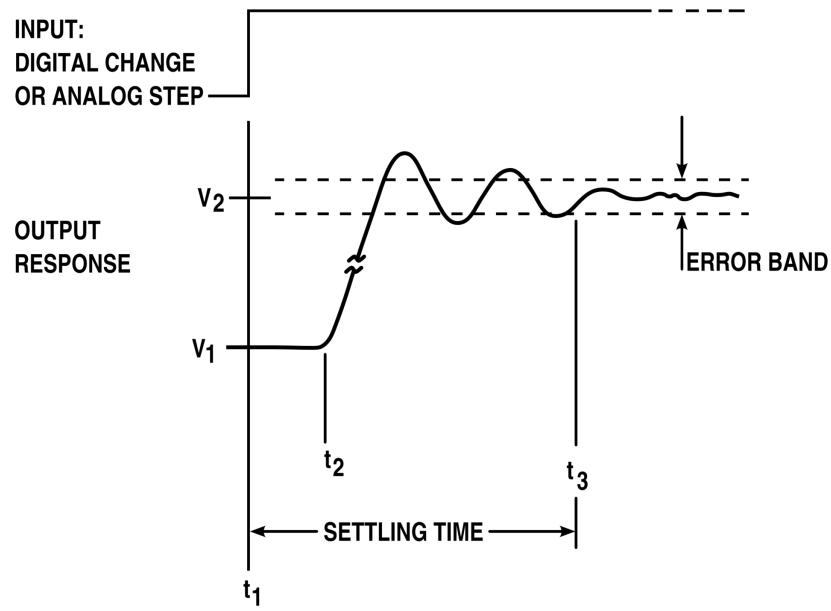


Figure 25: Settling Time Principle from Wiki

After measurement, in pre-simulation, raising settling time is 23.9 ns, falling settling time is 25.0 ns (standard:  $\leq 30\text{ns}$ ). In post-simulation, my raising settling time is 23.7 ns, while the falling settling time is 29.9 ns. (standard:  $\leq 40\text{ns}$ ).

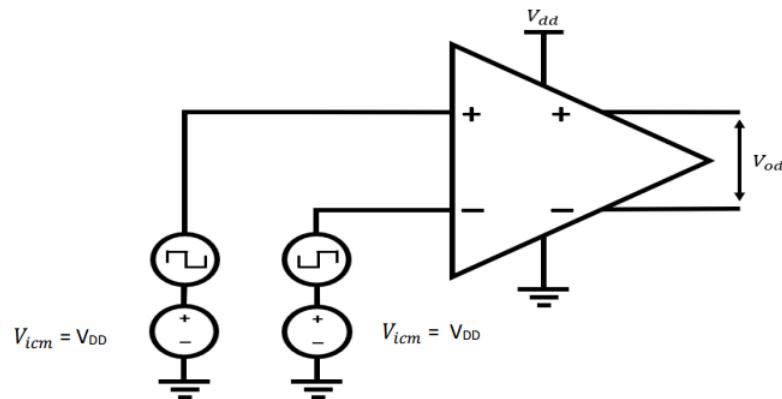


Figure 26: Settling Time and Slew Rate Testing

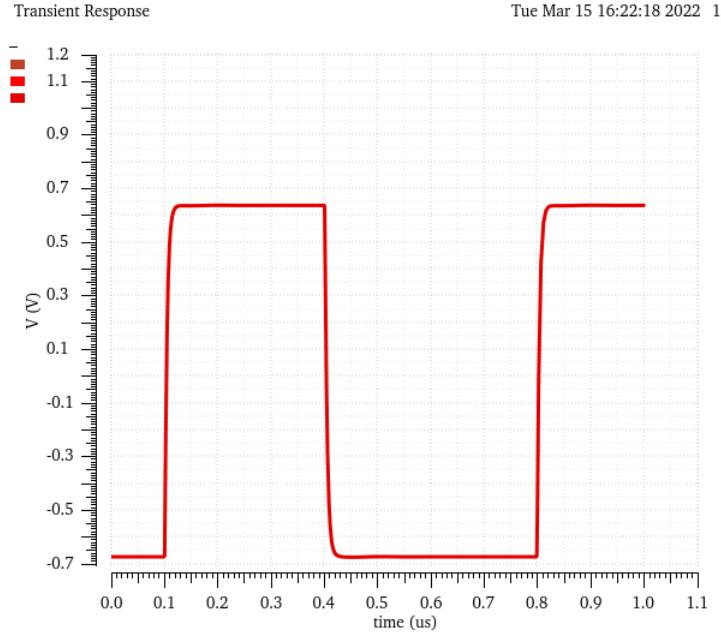


Figure 27: Settling Time and Slew Rate Wave

## 5.7 Slew Rate

Slew rate is the maximum slope of output voltage over time like the figure below. Bigger slew rate means circuit works faster.

I got 133.6 v/us in raising slew rate and -133.6 v/us in falling slew rate in pre-simulation, and got 118.8 v/us in raising slew rate and -117.3 v/us in falling slew rate in post-simulation.

## 5.8 CMFB Loop Unity Gain Bandwidth and Phase Margin

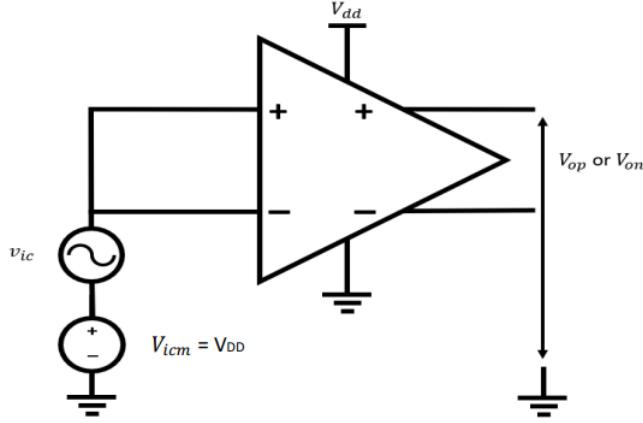


Figure 28: CMFB Loop Unity Gain Bandwidth and Phase Margin Testing

Since our circuit is a closed-loop, to test our feedback circuit, we added a new input circuit between amplifier and feedback like the figure below. The 1 PH large inductor helps us to isolate the small signal of two circuits, because of its large impedance. The 1 PF capacitor work as a high pass filter. According to the theory, a high bandwidth feedback network is more important than a high bandwidth amplifier to achieve a closed-loop amplifier. Normally, the bandwidth of feedback circuit should higher than amplifier. Here we set CMFB loop unity gain bandwidth is 20 MHz bigger than unity gain bandwidth of amplifier.

The phase margin is a parameter to describe how close a given feedback system is to instability. A small phase margin will lead to some unstable dynamic behavior. In our project, the phase margin should bigger than 60 degree in both pre-simulation and post-simulation.

After testing, the bandwidth and phase margin of pre-simulation is 210.692MHz (amplifier's bandwidth is 169.192MHz ) and  $62.4^\circ$ . As for post-simulation, I got 181.5 MHz for CMFB's bandwidth (amplifier's bandwidth is 147.8 MHz) and  $61^\circ$  for CMFB's phase margin.

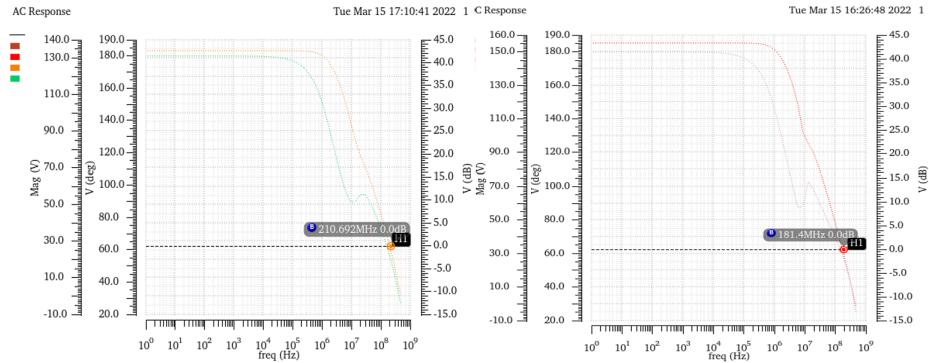


Figure 29: Pre-simulation vs Post-simulation in -40 degree

## 5.9 Chip Area

The total area of my layout design. After measuring, my chip area is 62.075 um x 84.6 um.

## 5.10 DO's and DON'Ts

During the interview with professor, he gave me some suggestions listed below.

1. These kind of resistor layout is pretty well, good matching.
2. But do not cross the metal above the resistor, because the current going through the metal will generate small magnetic field, which will have an effect on the flow of electrons in the resistor.

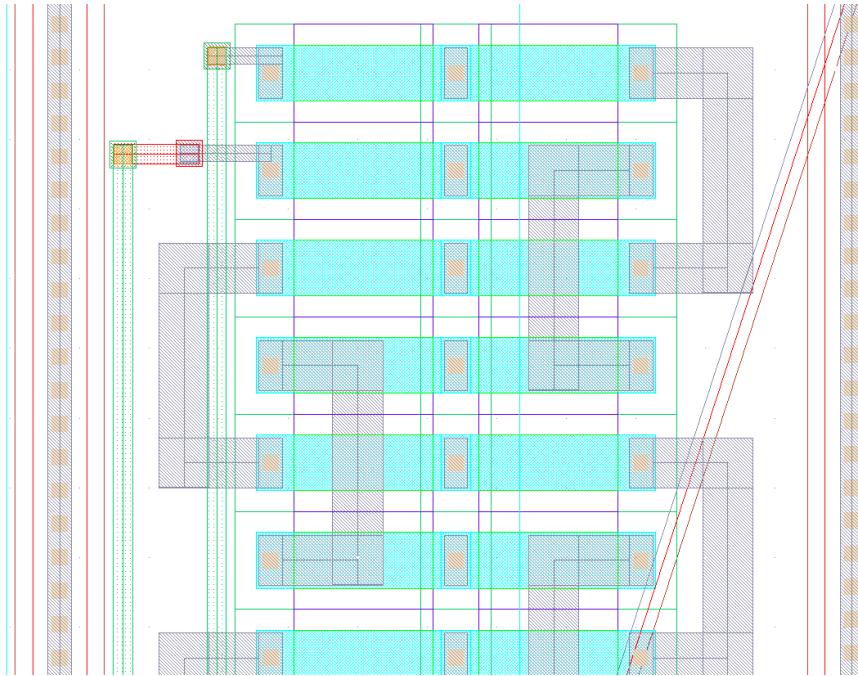


Figure 30: Resistor Layout Structure

3. Matching is the most important thing in analog circuit design. M39 and M38 should also be matching, so do not put M39 in a huge guard ring with other transistor, while putting M38 outside independently.

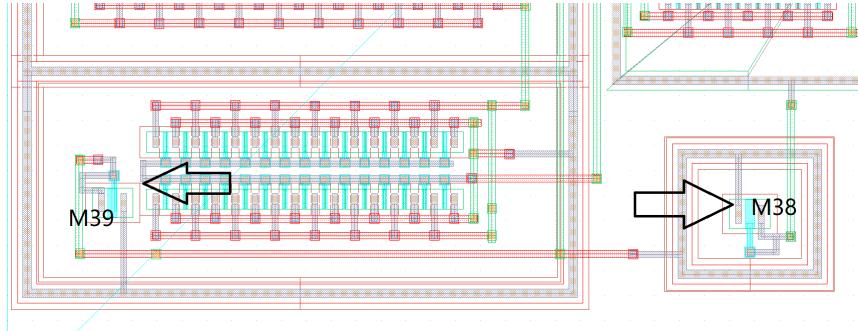


Figure 31: Matching Problem

4. N-Mos has high speed, P-Mos has low noise. For faster speeds, use N-Mos whenever possible.

## 6 Conclusion

This is my first time drawing such a mos level amplifier circuit. Comparing to the learning of theoretical knowledge, a practical lab project can help us apply our theoretical knowledge to a visible, testable object. This process helps us to understand the theory more deeply in our own way. It also helps me learn how to draw layout, and figure out some drawing tips by myself, which can make layout drawing more convenient.

## 7 Personal Score Sheet

<u>Personal Score Sheet</u>		
Name: <u>Zin Huangja</u>		Date: <u>7/3/2022</u>
Specification	Signature	
<b>AC Differential Gain*</b>  $40^\circ C : 12.1 dB$ $SS : 11.9 dB$ $f_{yp} : 11.9 dB$ $SF : 11.9 dB$ $100^\circ C : 11.9 dB$ $ff : 12.0 dB$ $V_{DD-1.8V} : 11.8 dB$ $f_z : 11.9 dB$ $V_{DD-1.8V} : 12.2 dB$	<u>AB</u>	
<b>Common Mode Gain</b>  $VOP : -54.2 dB$ $VON : -55.99 dB$	<u>AB</u>	
<b>Output Voltage Swing</b>  $0.45V \leq V_{out} \leq 1.15V$	<u>AB</u>	
<b>Unity Gain Bandwidth*</b>  $-40^\circ C : 147.9 MHz$ $SS : 146.7 MHz$ $fyp : 147.8 MHz$ $CF : 148.2 MHz$ $100^\circ C : 146.8 MHz$ $ff : 146.1 MHz$ $V_{DD-1.8V} : 146.1 MHz$ $f_z : 148.2 MHz$ $V_{DD-1.8V} : 150.2 MHz$	<u>AB</u>	
<b>Current Consumption</b>  $348.9 \mu A$	<u>AB</u>	
<b>Total Harmonic Distortion</b>  $-56.62 dB$	<u>AB</u>	
<b>Settling Time</b>  $+ve : 23.7 ns$ $-ve : 29.9 ns$	<u>AB</u>	
<b>Slew Rate</b>  $+ve : 118.8 V/us$ $-ve : -117.3 V/us$	<u>AB</u>	
<b>CMFB Loop Unity Gain Bandwidth</b>  $181.5 MHz$	<u>AB</u>	
<b>CMFB Loop Phase Margin</b>  $61^\circ$	<u>AB</u>	
<b>Chip Area</b>  $62.075 \mu m \times 84.6 \mu m$	<u>AB</u>	

\*Only AC Differential Gain & Unity Gain Bandwidth have to fulfill all PVT corners for this assignment

Please scanned a copy of this page which must be included in the appendix of the final report.

Figure 32: Personal Score Sheet

## 8 Reference

- 1 Ogata, K. (2010). Modern Control Engineering. Prentice Hall.
- 2 Carusone, T. C., Johns, D., & Martin, K. (2011). Analog Integrated Circuit Design (2nd ed.) [E-book]. Wiley.