ECE451Lab7

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Contents

1 Objective

During this lab, we are asked to improve the design of Subway Signal Control which we did in Lab3. Here is the objective list on Canvas.

The objective of this lab is to expand the subway signal control logic by adding a sequential logic to it.

2 Introduction

The subway signal control is the continuation of Lab3. In Lab 3, the direction signal D is given as a primary input signal. Now, we should design a finite state machine to generate signal D. And the train should follow the rule: when two consecutive left-to-right trains passed by, the next train must go from right-to-left. After that, there will be two more left-to-right trains

3 Procedure and analysis

3.1 State transition diagrams

Before designing FSM, we need to figure out the state transition diagram, the diagram below is mine state transition diagram to describe subway signal control system. Here, state A,B describe the first train goes from left to right, and state C,D is the second. State E,F are used to show the train goes from right to left. After state F, it will back to state A, which means there will be two more left-to-right train.

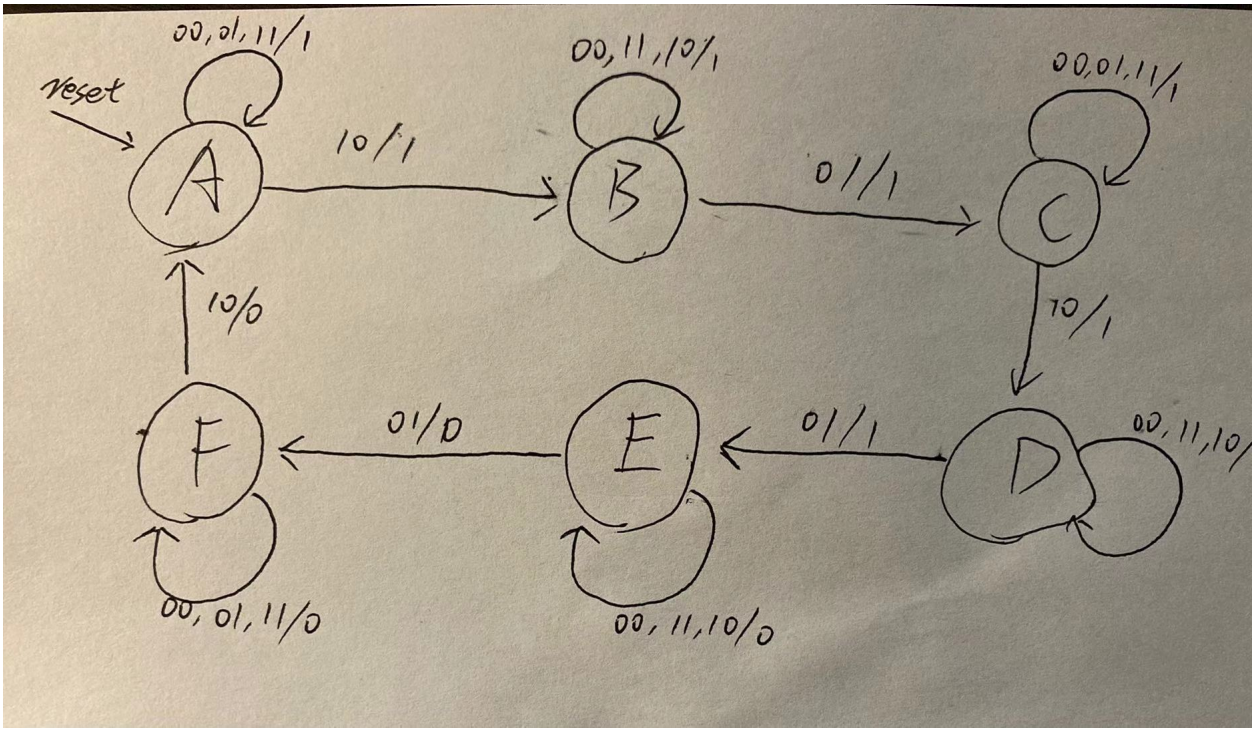

Figure 1: State transition diagrams

3.2 State transition tables

According to the diagram above, we can encode it and generate the state transition tables. We assigned state A F to the binary number 000 101.

Current State		P(left)	P(right)	Next State		D
A	000	0	0	A	000	1
		0	1	A	000	1
		1	0	B	001	1
		1	1	A	000	1
B	001	0	0	B	001	1
		0	1	C	010	1
		1	0	B	001	1
		1	1	B	001	1
C	010	0	0	C	010	1
		0	1	C	010	1
		1	0	D	011	1
		1	1	C	010	1
D	011	0	0	D	011	1
		0	1	E	011	1
		1	0	D	100	1
		1	1	D	011	1
E	100	0	0	E	100	0
		0	1	F	101	0
		1	0	E	100	0
		1	1	E	100	0
F	101	0	0	F	101	0
		0	1	F	101	0
		1	0	A	000	0
		1	1	F	101	0

Figure 2: State transition table

From the table above we can generate the equations for next state and output. Here we use the D flip flop, setting Q2,Q1,Q0 for current state and D2,D1,D0 for next state. D is the output direction.

$$D_2 = Q_2Q_0' + Q_2P_L' + Q_2P_R + Q_1Q_0P_L'P_R$$

$$D_1 = Q_1Q_0' + Q_1P_R' + Q_1P_L + Q_2'Q_0P_LP_R' + Q_2'Q_1'Q_0P_L'P_R$$

$$D_0 = Q_0P_L'P_R' + Q_0P_LP_R + Q_2P_L'P_R + Q_1P_LP_R' + Q_2'Q_0'P_LP_R'$$

$$D = Q_2'$$

3.3 Schematic of D-bit equations

Now we can generate the schematic according to the equations above. Here are my schematic.

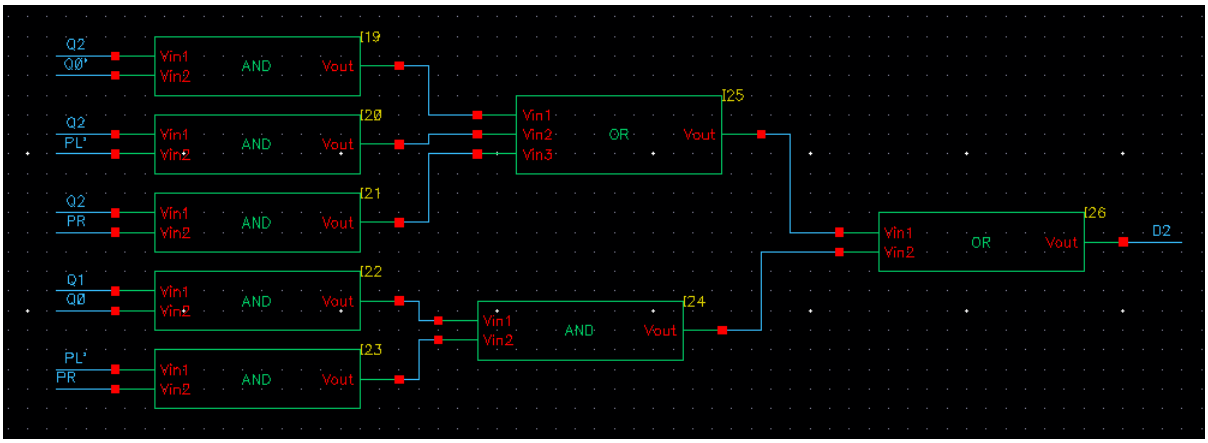

Figure 3: D_2 schematic

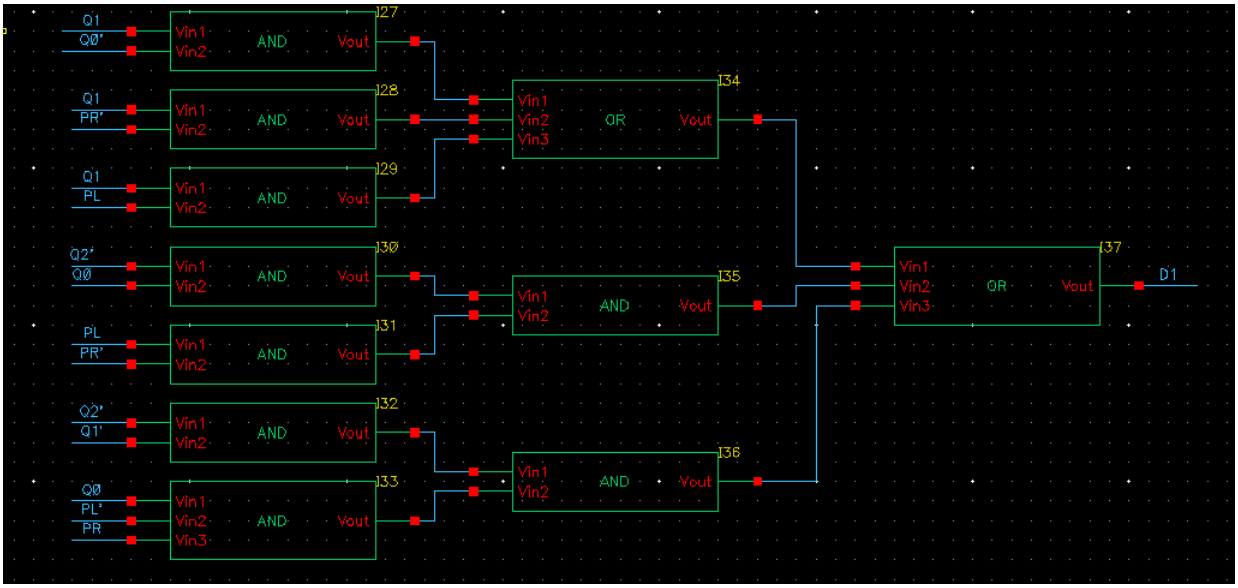

Figure 4: D_1 schematic

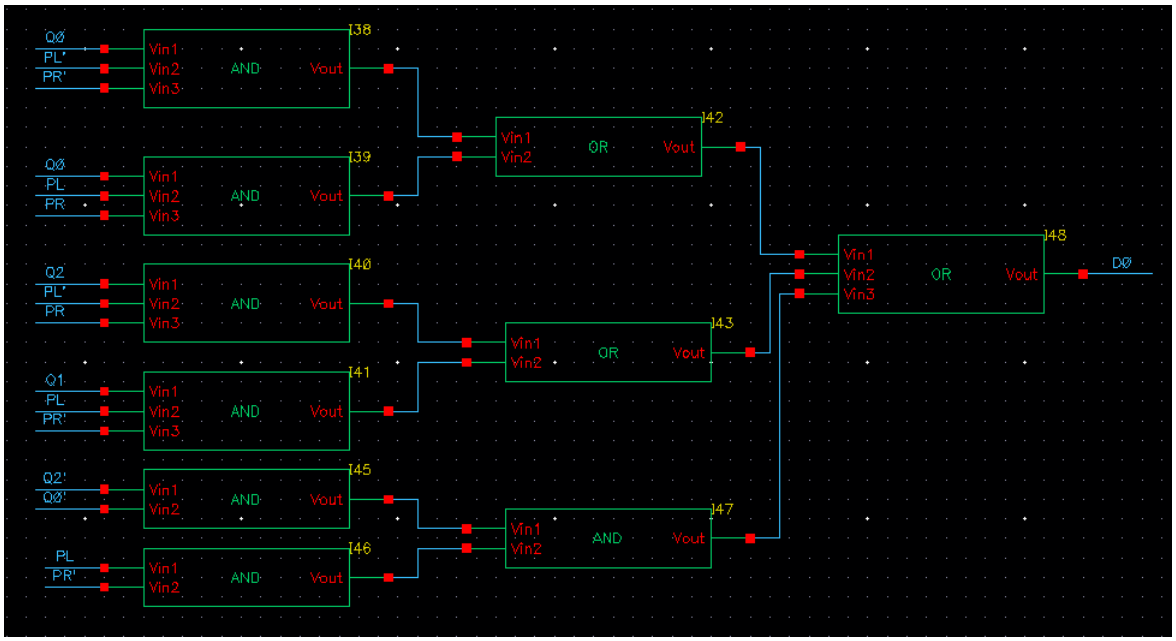

Figure 5: D_0 schematic

Combining them together, here is my DFF main schematic.

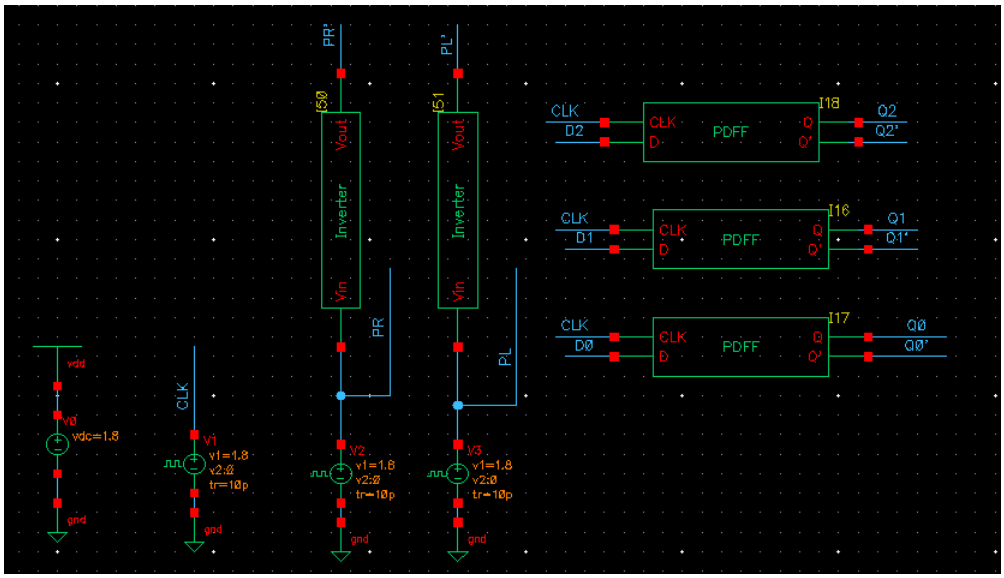

Figure 6: Combining DFF schematic

3.4 Final output waveforms

After running the simulation. we got the figure below. Let's check from the state 000. when the input is 10, state move to 001. Then when the input is 01 sate move to 010. The next changes occurred following the input sequence {10, 01, 01}. Finally, when input is 10, the state 101 change back to 000. We can find the state changes and change conditions follow our state transition tables.

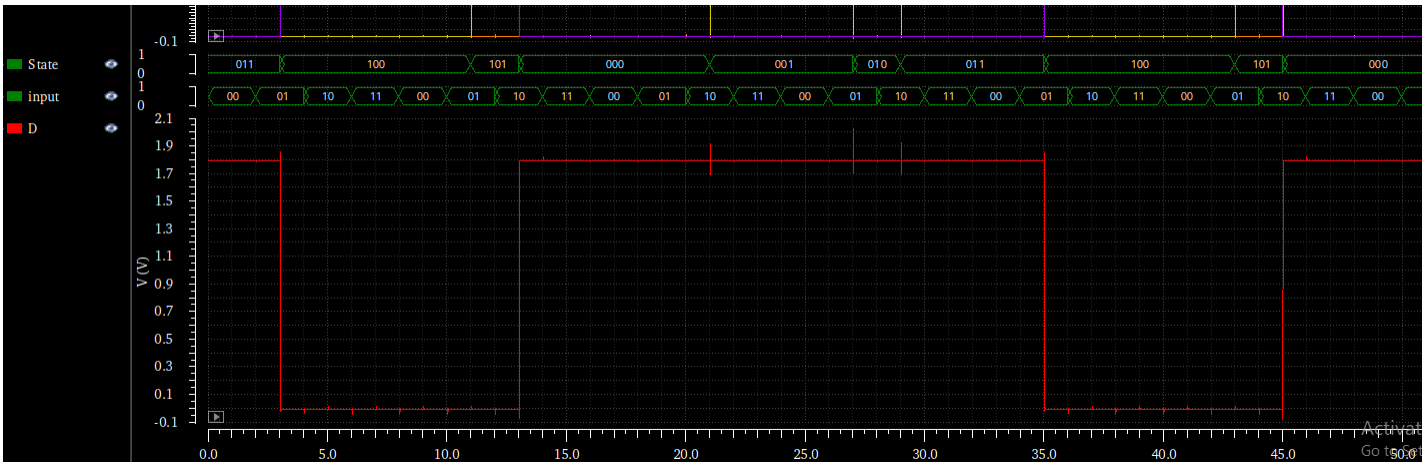

Figure 7: Final output waveforms

4 Questions

4.1 Compare and contrast a Moore Finite State Machine (FSM) with a Mealy FSM.

4.1.1 Moore

1 Output depends only upon present state.

2 If input changes, output does change.

3 More number of states are required.

4 There is less hardware requirement for circuit implementation.

5 They react slower to inputs(One clock cycle later).

4.1.2 Mealy

1 Output depends on present state as well as present input.

2 If input changes, output also changes.

3 Less number of states are required.

4 There is more hardware requirement for circuit implementation.

5 They react faster to inputs.

5 Conclusion

Now we can get the conclusion, I finish this lab successfully, and achieve all the objective. I have learned that encoding and minimization is a good way to improve efficiency and improve accuracy.