ECE451Lab5

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Contents

1 Objective

During this lab, we are asked to achieve a grey code counter, in Cadence using D flip flop. Here is the objective list on Canvas.

The objective of this lab is to learn simple sequential logic circuit design and verification using schematic capture and digital simulation tools.

2 Introduction

We are asked to design a 3 bit grey code counter. The counting sequence for grey code is 000, 001, 011, 010, 110, 111, 101, 100. Use D-FFs to implement the counter. There is only one input: clock signal, and a 3 bits output.

3 Procedure and analysis

3.1 D flip flop

In order to implement grey code counter, we need to design a D flip flop at first, here is truth table of D flip flop.

Clk	D	Q		Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Figure 1: D flip flop truth table

Here is my circuit of master slave D flip flop.

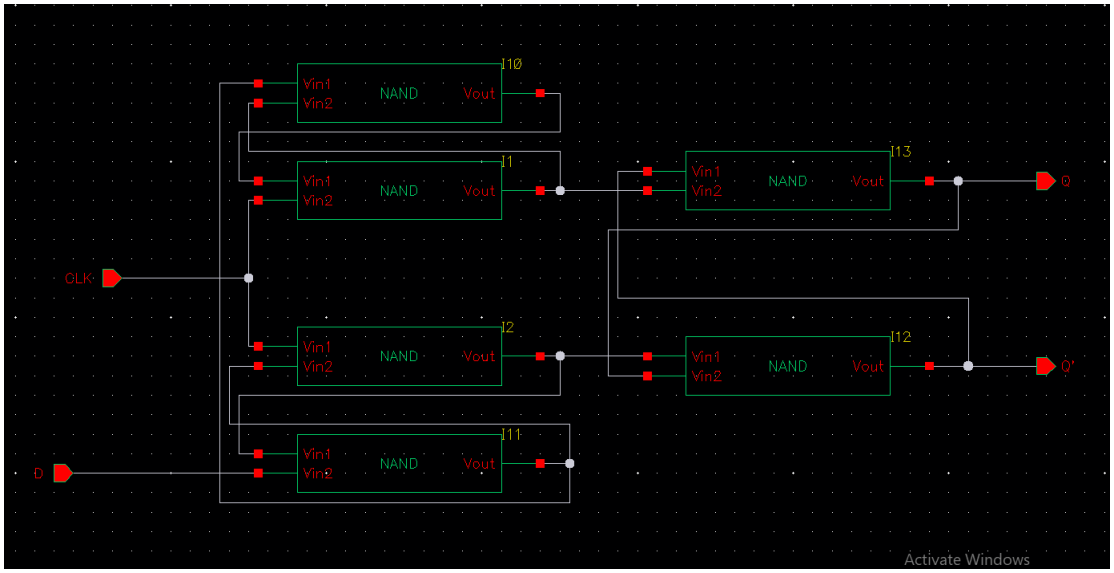

Figure 2: Master slave D flip flop

Here is simulation waveform of D flip flop.

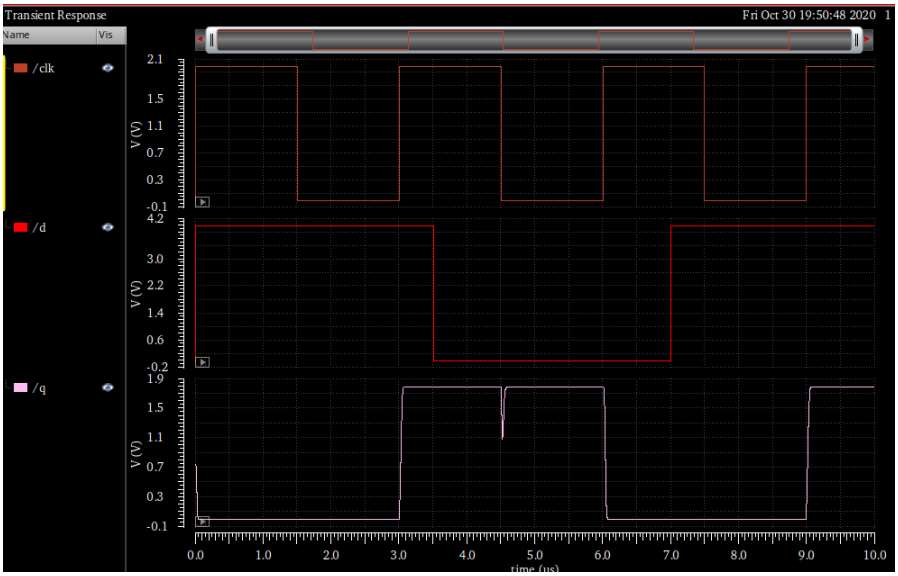

Figure 3: D flip flop wave form

3.2 Grey code counter

We need to write down the state transition table and truth table at first.

Q2	Q1	Q0	Q2n	Q1n	Q0n	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	1
0	1	0	1	1	0	1	1	0
0	1	1	0	1	0	0	1	0
1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	0	1

$$D2 = Q1*Q0' + Q2*Q0$$

$$D1 = Q1*Q0' + Q2'*Q0$$

$$D0 = Q2*Q1 + Q2'*Q1'$$

Then we can achieve our grey code counter circuit.

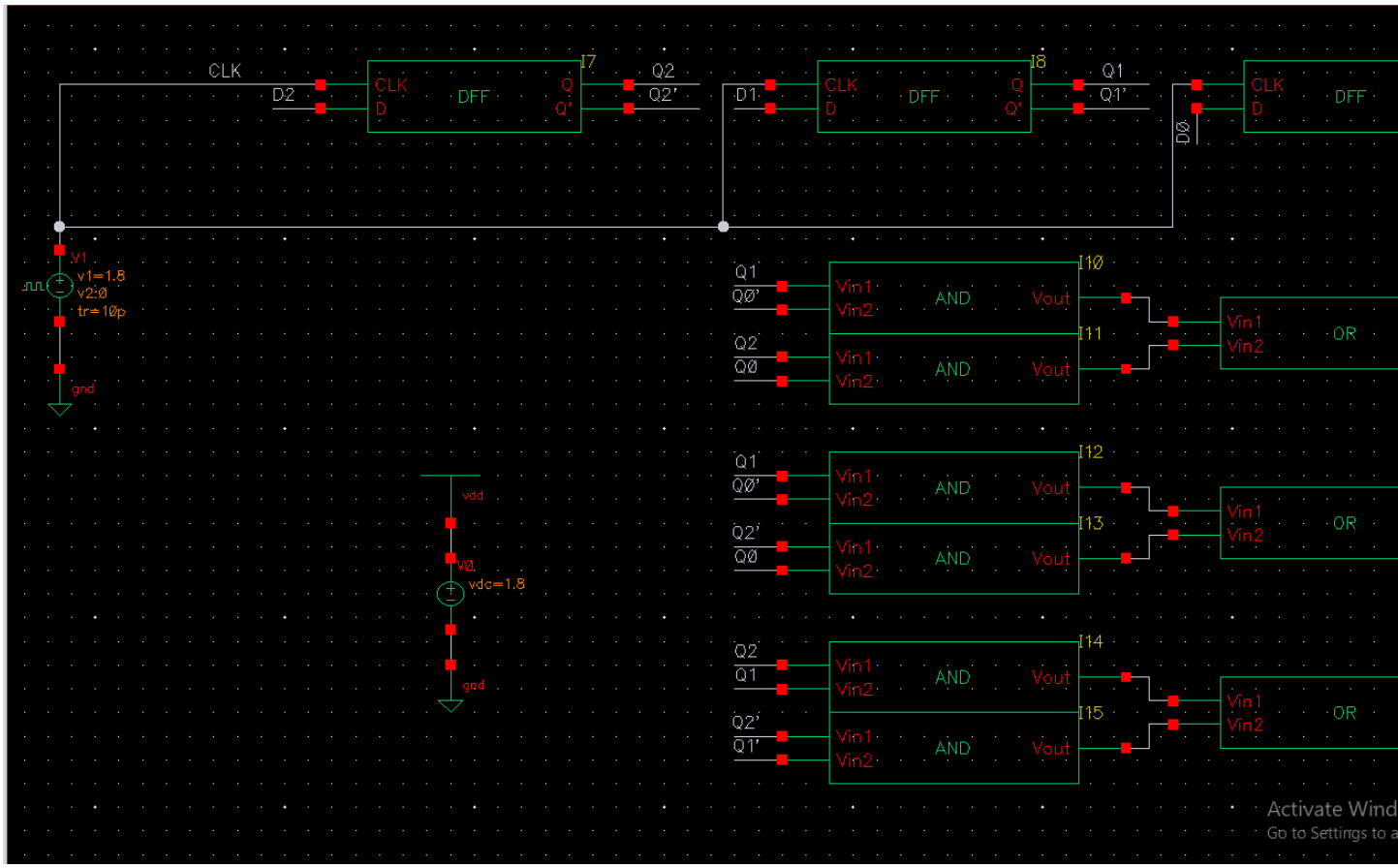

Figure 4: Grey code counter circuit

Here is my simulation waveform of grey code counter.

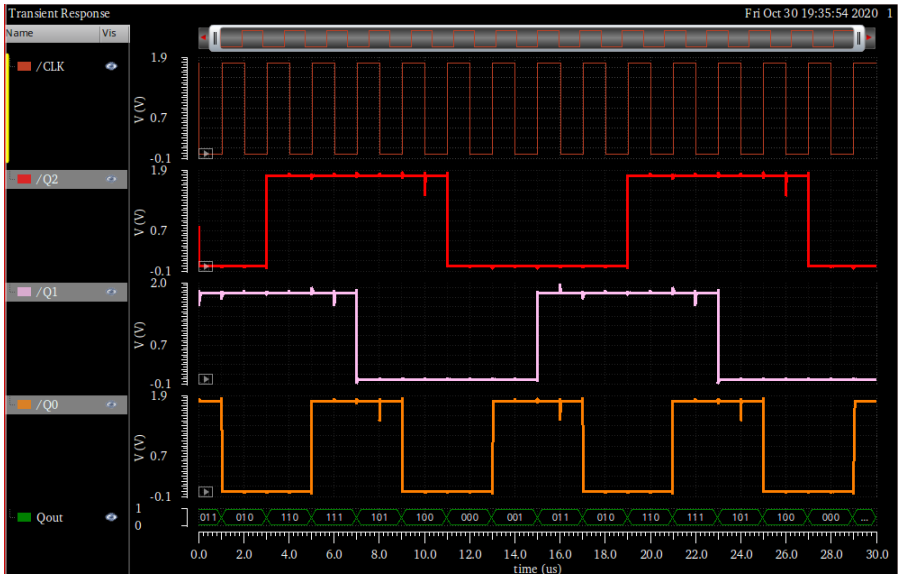

Figure 5: Grey code counter waveform

4 Questions

4.1 What is Moore Finite State Machine (FSM)?

Moore machine is an FSM whose outputs depend on only the present state.

4.2 What is Mealy FSM?

A Mealy Machine is an FSM whose output depends on the present state as well as the present input.

5 Conclusion

Now we can get the conclusion, I finish this lab successfully, and achieve all the objective. I have learned that the master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output.