- Programmable Look-Ahead Up/Down Binary Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- · Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

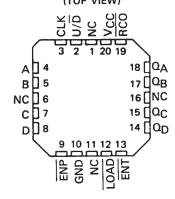
description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high speed counting applications. The 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

SN54LS169B, SN54S169 . . . J OR W PACKAGE SN74LS169B, SN74S169 . . . D OR N PACKAGE (TOP VIEW) U₁6∐Vcc U/D∏1 15 RCO CLK 2 A □ 3 14 □ QA В 🛛 4 13 🛮 QB 12 QC C∐5 D [] € 11 🗌 QD 10 ENT ENP 7 9 LOAD GND ∐8

SN54LS169B, SN54S169 . . . FK PACKAGE (TOP VIEW)



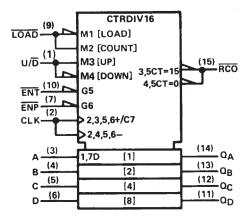
NC-No internal connection

TYPE		TYPICAL MAXIMUM CLOCK FREQUENCY				
	COUNTING	COUNTING DOWN	DISSIPATION			
'LS169B	35MHz	35MHz	100mW			
'S169	70MHz	55MHz	500mW			

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (ENP, ENT) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input ENT is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the QA output when counting up and approximately equal to the low portion of the QA output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$, $\overline{\text{LOAD}}$, $\overline{\text{U/D}}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

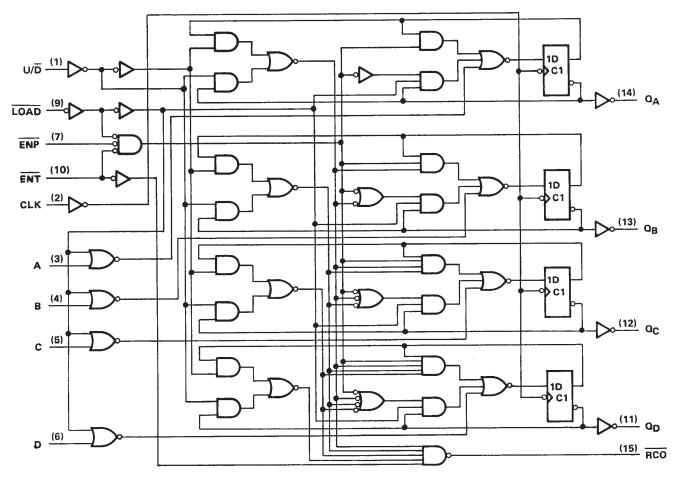
logic symbol[†]



 † This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

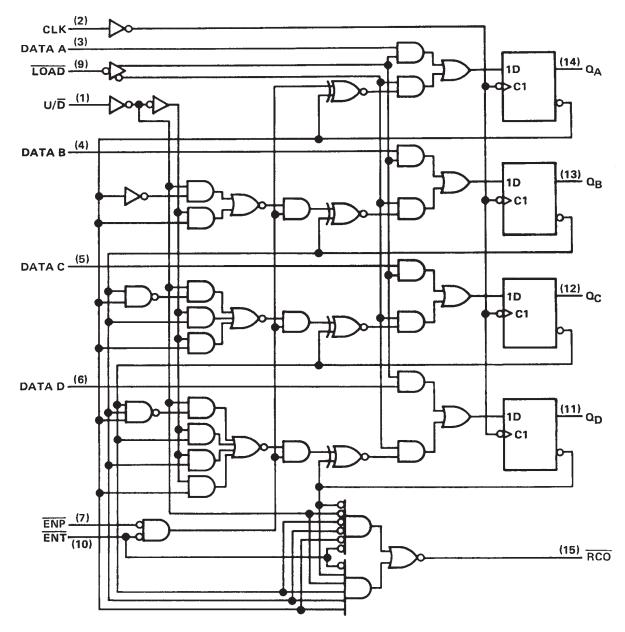


logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



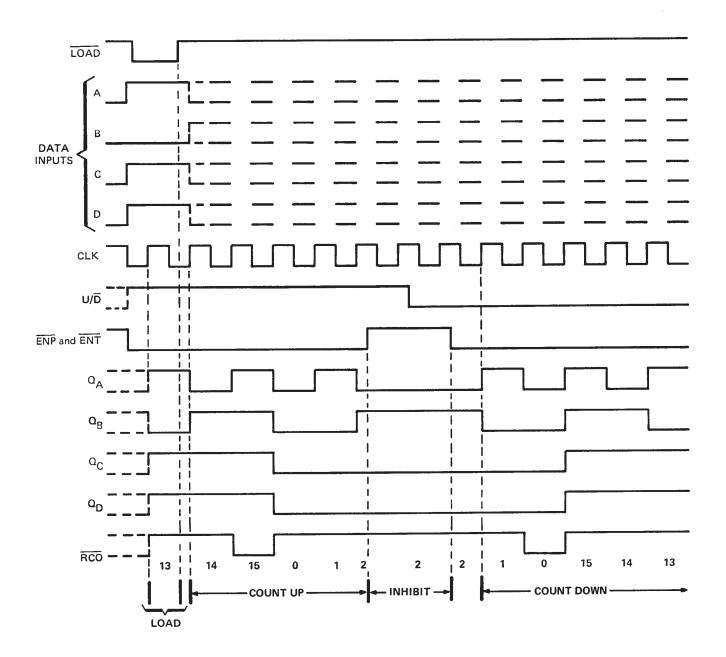
Pin numbers shown are for D, J, N, and W packages.



typical load, count, and inhibit sequences

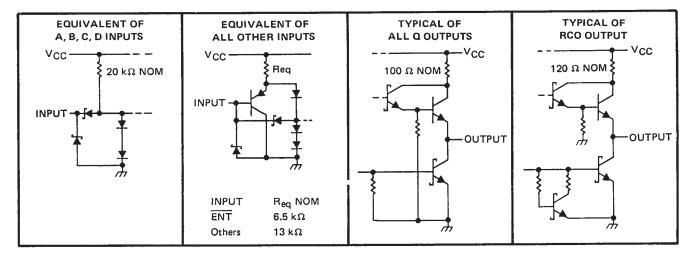
Illustrated below is the following sequence:

- 1. Load (preset) to binary thirteen.
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two.
- 3. Inhibit
- 4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen





schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		7 V
Input voltage		7 V
Operating free-air temperature range	: SN54LS169B	$ 55^{\circ}$ C to 125° C
	SN74LS169B	0°C to 70°C
Storage temperature range		65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SI	154LS1	69B	SN	SN74LS169B		UNIT	
				MIN	NOM	MAX	MIN	NOM	MAX	ONT	
Vcc	Supply voltage			4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level-input voltage			2			2			V	
VIL	Low-level input voltage					0.7			8.0	V	
IOH High-level output current			RCO			- 0.4			- 0.4	mA	
			Any Q			- 1.2			- 1.2	mA	
IOL Low-level output current		RCO			4			8	mA		
			Any Q			12			24	mA	
fclock	Clock frequency			0		20	0		20	MHz	
tw(clock)	Width of clock pulse (high or low) (see Figure 1)		25			25			ns	
		Data inputs	A, B, C, D	30			30]	
		ENP or ENT		30			30			ns	
IOL Low-leve fclock Clock fre tw(clock) Width of tsu Setup tir	Setup time, (see Figure 1)	Load		35			35] '''	
		U/D		35			35		0.8 - 0.4 - 1.2 8 24		
th	Hold time at any input with respe	ct to clock (see Figu	re 1)	0			0			ns	
TA	Operating free-air temperature			- 55		125	0		70	°c	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER					SN54LS169B			SN	UNIT		
		TEST CONDITIONS†				TYP‡	MAX	MIN	TYP‡	MAX	ONT
VIK	V _{CC} = MIN,	I ₁ = - 18 mA					– 1.5			– 1. 5	V
	V _{CC} = MIN,	V _{IH} = 2 V,	RCO	I _{OH} = - 0.4 mA	2.5	3.4		2.7	3.4		V
Vон	VIL = MAX		Any Q	I _{OH} = - 1.2 mA	2.4	3.2		2.4	3.2		
			RCO	IOH = 4 mA		0.25	0.4		0.25	0.4	1.4
	V _{CC} = MIN,	i, V _{IH} = 2 V,	RCO	I _{OL} = 8 mA					0.35	0.5] _v
VoL	VIL = MAX		1 0	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
		Any Q I _{OL} = 24 mA							0.35	0.5]
Iį	V _{CC} = MAX,	V _I = 7 V	-				0.1			0.1	mA
Iн	V _{CC} = MAX,	V ₁ = 2.7 V	······································				20			20	μΑ
	., .,,,		U/D, LC	AD, ENP, CLK			- 0.2			- 0.2	mA
¹ 1L	V _{CC} = MAX,		All othe				0.4			- 0.4	mA
			RCO		- 20		- 100	- 20		- 100	
los§	$V_{CC} = MAX$, $V_O = 0 V$		Any Q		- 30		- 130	- 30		- 130	mA
lcc	V _{CC} = MAX,	See Note 2	1			28	45		28	45	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see note 3)

	FROM	то	TO TEST CONDITIONS				TO TOTAL CONTRACTOR				'LS169B		
PARAMETER¶	(INPUT)	(OUTPUT)	TEST CON	MIN	TYP	MAX	UNIT						
fmax					20	35		MHz					
^t PLH	01.14	RCO				26	40	ns					
tPHL tPHL	CLK	HCO HCO				17	25	115					
^t PLH	ENT	RCO	D - 010	045 -5		15	25	ns					
tPHL	ENI	HCO	$R_L = 2 k\Omega$,	C _L = 15 pF		11	20	'''					
^t PLH	U/D		500				23	35					
^t PHL		RCO				15	25	ns					
^t PLH						16	25						
tPHL	CLK	Any Q	$R_L = 667 \Omega$, C_L	C _L = 45 pF		17	25	ns					

[¶] Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transistion will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



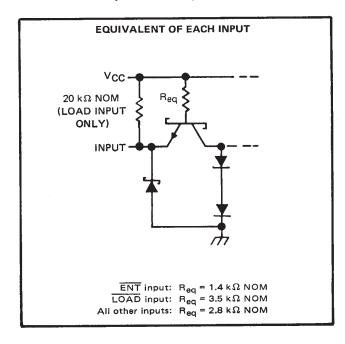
 $[\]ddagger$ All typical values are at V_{CC} = 5 V, T_A = 25°C. § Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

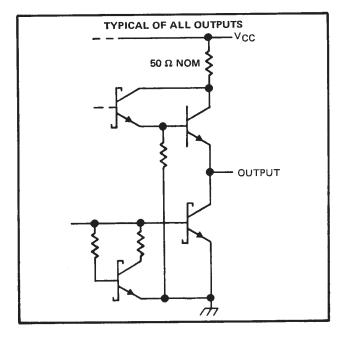
NOTE 2: ICC is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 - OCTOBER 1976 - REVISED MARCH 1988

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (See Note 4)
Input voltage 5.5 V
Interemitter voltage (see Note 5)
Operating free-air temperature range: SN54S169 (see Note 6)55°C to 125°C
SN74S169 0°C to 70°C
Storage temperature range

recommended operating conditions

		S	4.5 5 5. - 2		SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				- 1			- 1	mA
Low-level output current, IQL				20			20	mA
Clock frequency, f _{clock}		0		40	0		40	MHz
Width of clock pulse, tw(clock) (high or low) (see Figure 1)		10			10			ns
Vidth of clock pulse, t _W (clock) (high o	Data inputs A, B, C, D	4			4			1
·	ENP or ENT	14			14			ns
Setup time,t _{SU} (see Figure 1)		9			6] ""
	U/D	20			20			
Hold time at any input with respect to clock, tw (see Figure 1)		1			1			ns
Operating free-air temperature, TA (se		- 55		125	0		70	°C

NOTES: 4. Voltage values, except interemitter voltage, are with respect to network ground terminal.

- 5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$.
- 6. A SN54S169 in the W package operating at free-air temperatures above 91 °C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26 °C/W.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TTOT CONDITIONS!			SN54S169			SN74S169										
PARAMETER		TEST CONDITIONS [†]		MIN	TYP‡	MAX	MIN	TYP [‡]	MAX	UNIT								
V _{IH} High-level input voltage				2			2			V								
V _{IL} Low-level input voltage						0.8			0.8	٧								
VIK Input clamp voltage		V _{CC} = MIN,	$I_{J} = -18 \text{ mA}$			-1.2			-1.2	V								
V _{OH} High-level output voltage		$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	$V_{IH} = 2 V$, $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		٧								
V _{OL} Low-level output voltage		$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	٧								
I Input current at maximum inpu	ıt voltage	V _{CC} = MAX,	V ₁ = 5.5 V			1			1	mA								
	ENT					100			100									
IH High-level input current	Load	V _{CC} = MAX,	$V_i = 2.7 V$	-10		- 200	- 10		- 200	μΑ								
	Other inputs					50		-1.2 3.4 0.5 1 100										
	ENT	.,,	0.5.1/			-4			-4	mA								
I _{IL} Low-level input current	Other inputs	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	VCC = MAX,	$V_{CC} = MAX$, $V_I = 0.5 V$			- 2			- 2	
IOS Short-circuit output current§		V _{CC} = MAX,		- 40		- 100	- 40		- 100	mΑ								
ICC Supply current		V _{CC} = MAX,	See Note 2		100	160		100	160	mA								

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: ICC is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, VCC = 5 V, TA = 25°C

a	FROM	FROM TO U/D				IGH	U/	D = L(w	UNIT
PARAMETER¶	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	ONT
f _{max}				40	70		40	55		MHz
tPLH	01.14	500			14	21		14	21	ns
tPHL t	CLK	RCO	0 15-5		20	28		20	28	113
tPLH	01.14		$C_L = 15 \mathrm{pF},$ $R_L = 280 \Omega,$		8	15		8	15	ns
tPHL	CLK	Any Q	See Figures 2 and 3		11	15		11	15] '''
tPLH		===	and Note 3		7.5	11		6	12	ns
tPHL	ENT	RCO			15	22		15	25] ""
tPLH♦			1		9	15		8	15	
tpHL♦	U/ <u>D</u>	RCO	RCO		10	15		16	22	ns

 $¹_{t_{max}} = maximum clock frequency$

Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15 for 'S169), the ripple carry output will be out of phase.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



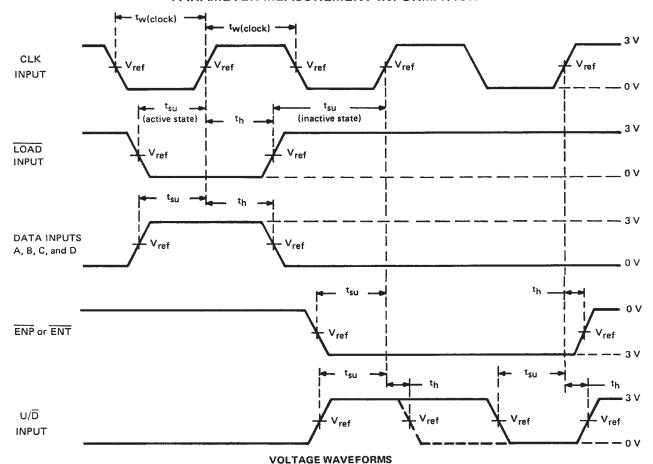
 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

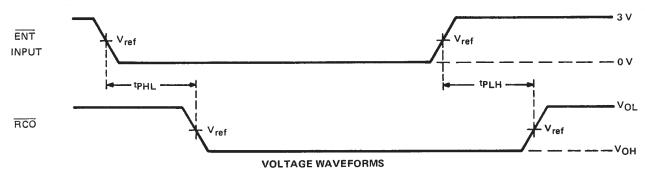
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx$ 50 Ω ; for 'LS169B, $t_r \leq$ 15 ns; $t_f \leq$ 6 ns, and for 'S169, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

B. For 'LS169B, V_{ref} = 1.3 V; for 'S168 and 'S169, V_{ref} = 1.5 V.

FIGURE 1-PULSE WIDTHS, SETUP TIMES, HOLD TIMES



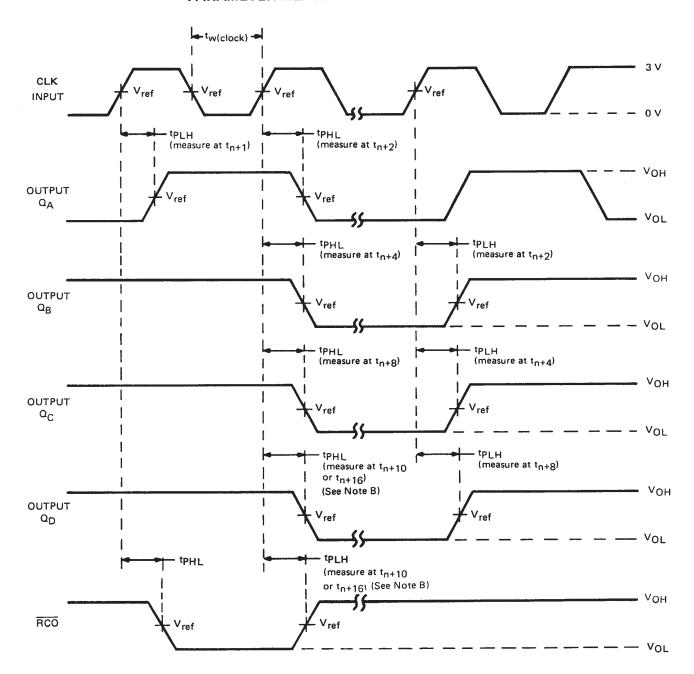
NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq MHz, duty cycle \leq 50%, Z_{out} \approx 50 Ω ; for 'LS169B, t_r \leq 15 ns, t_f \leq 5 ns; and for 'S169, t_r \leq 2.5 ns.

- B. tpLH and tpHL from enable T input to ripple carry output assume that the counter is at the maximum count, all Q outputs high.
- C. For 'LS169B, $V_{ref} = 1.3 \text{ V}$; for 'S169, $V_{ref} = 1.5 \text{ V}$.
- D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

FIGURE 2-PROPAGATION DELAY TIMES TO CARRY OUTPUT



PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤50%, $Z_{out} \approx 50~\Omega$; for 'LS169B, $t_r \leq 15$ ns; $t_f \leq 6$ ns, and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max} .

- B. Outputs Q_D and carry are tested at t_{n+16} , where t_n is the bit-time when all outputs are low. C. For 'LS169B, $V_{ref}=1.3$ V; for 'S169, $V_{ref}=1.5$ V.

FIGURE 3-PROPAGATION DELAY TIMES FROM CLOCK



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