

Lógica Digital (1001351)

Circuitos Sequenciais: Análise de Tempo



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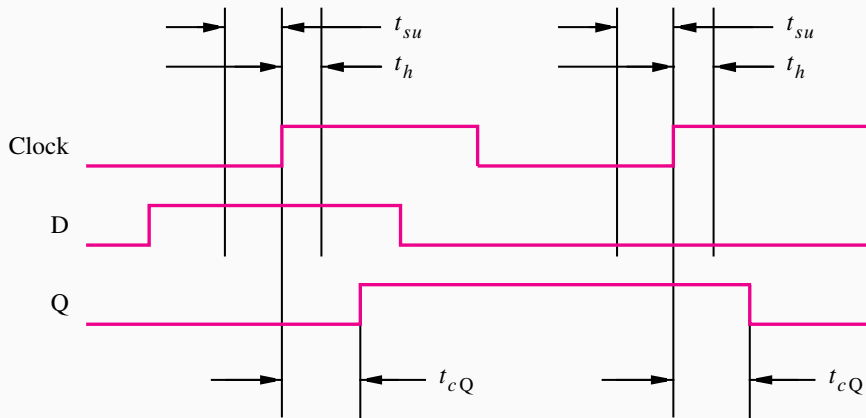
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Departamento de Computação

Centro de Ciências Exatas e de Tecnologia

Universidade Federal de São Carlos

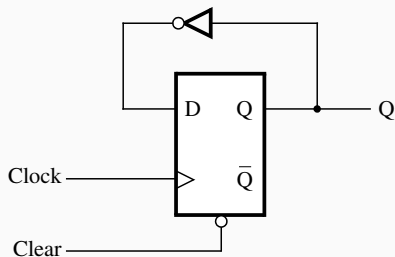
Temporização de um flip-flop



(b) Timing diagram

Figure 5.14 Flip-flop timing parameters.

Análise de tempo (*timing analysis*)



- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$

Figure 5.66 A simple flip-flop circuit.

Análise de tempo (*timing analysis*)

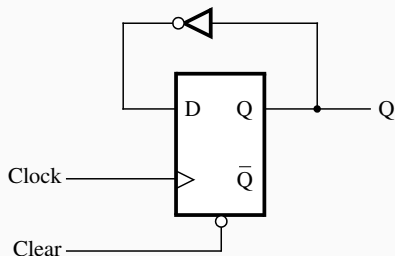


Figure 5.66 A simple flip-flop circuit.

- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$
- $T_{min} = 1/F_{max}$
- $T_{min} = t_{cQ} + t_{NOT} + t_{su}$
- $T_{min} = 1,0 + 1,1 + 0,6 = 2,7 \text{ ns}$
- $F_{max} = 1/2,7 \text{ ns} = 370,37 \text{ MHz}$

Análise de tempo (*timing analysis*)

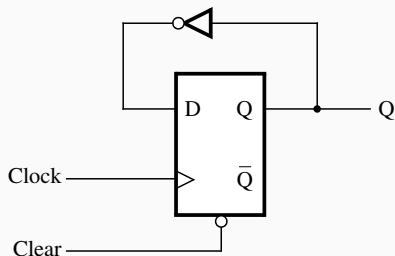
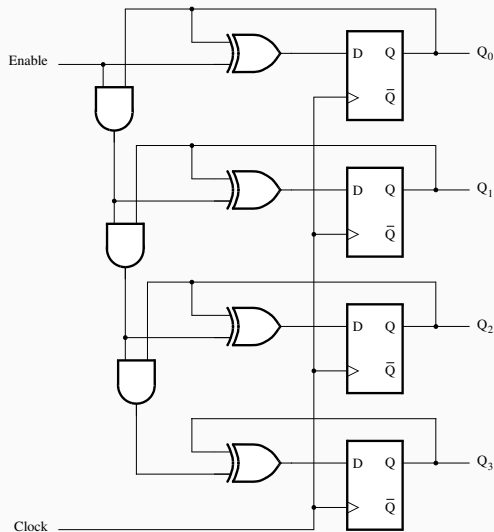


Figure 5.66 A simple flip-flop circuit.

- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$
- $T_{min} = 1/F_{max}$
- $T_{min} = t_{cQ} + t_{NOT} + t_{su}$
- $T_{min} = 1,0 + 1,1 + 0,6 = 2,7 \text{ ns}$
- $F_{max} = 1/2,7 \text{ ns} = 370,37 \text{ MHz}$
- $t_{cQ} + t_{NOT} = 0,8 + 1,1 = 1,9 \text{ ns} > t_h = 0,4 \text{ ns}$

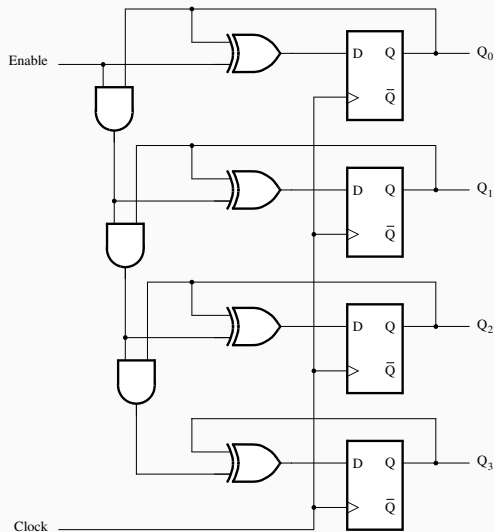
Análise de tempo (*timing analysis*)



- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$

Figure 5.67 A 4-bit counter.

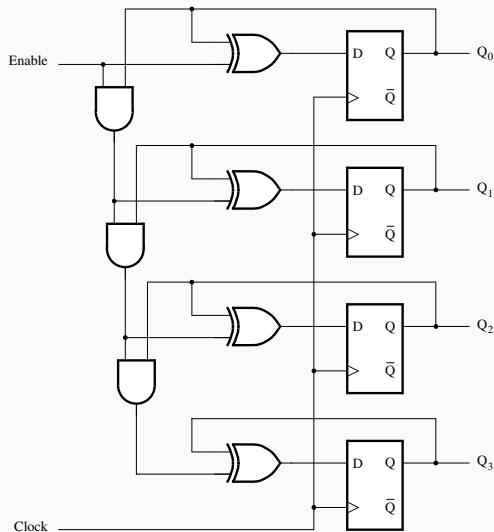
Análise de tempo (*timing analysis*)



- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$
- $T_{min} = 1/F_{max}$
- $T_{min} = t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su}$
- $T_{min} = 1,0 + 3(1,2) + 1,2 + 0,6 = 6,4 \text{ ns}$
- $F_{max} = 1/6,4 \text{ ns} = 156,25 \text{ MHz}$

Figure 5.67 A 4-bit counter.

Análise de tempo (*timing analysis*)



- $t_{su} = 0,6 \text{ ns}$
- $t_h = 0,4 \text{ ns}$
- $0,8 \text{ ns} \leq t_{cQ} \leq 1,0 \text{ ns}$
- $T_{min} = 1/F_{max}$
- $T_{min} = t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su}$
- $T_{min} = 1,0 + 3(1,2) + 1,2 + 0,6 = 6,4 \text{ ns}$
- $F_{max} = 1/6,4 \text{ ns} = 156,25 \text{ MHz}$
- $t_{cQ} + t_{XOR} = 0,8 + 1,2 = 2,0 \text{ ns} > t_h = 0,4 \text{ ns}$

Figure 5.67 A 4-bit counter.

Conceito geral de *clock skew*

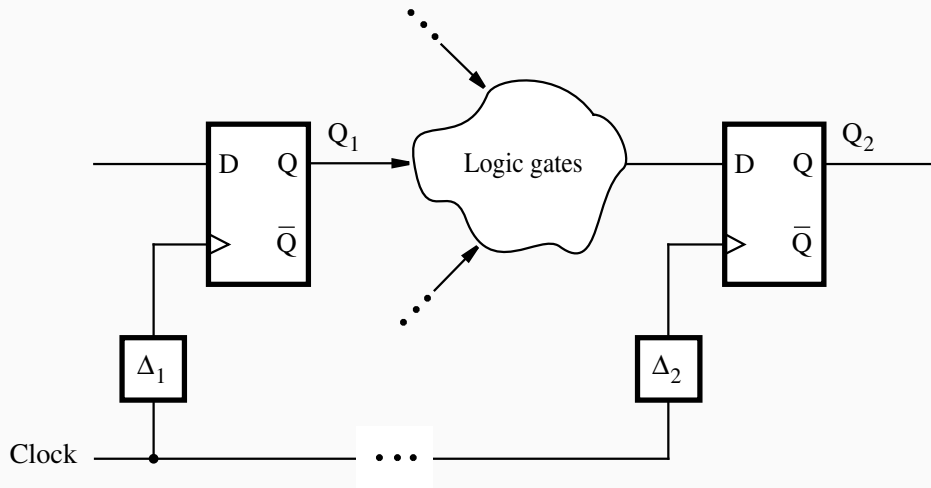


Figure 5.68 A general example of clock skew.

Relógio “distorcido” (*clock skew*)

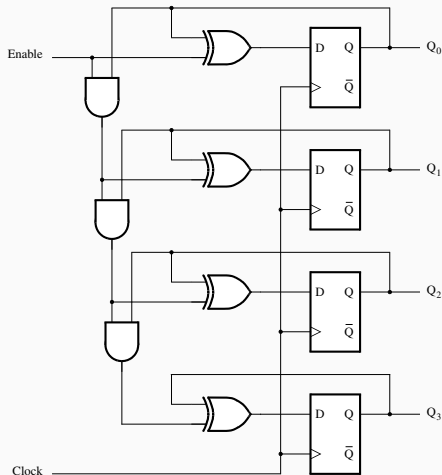


Figure 5.67 A 4-bit counter.

- $t_{skew} = 1,5 \text{ ns}$
- $T_{min} = t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su} - t_{skew}$
- $T_{min} = 1,0 + 3(1,2) + 1,2 + 0,6 - 1,5 = 4,9 \text{ ns}$
- $T_{min} = t_{cQ} + 2(t_{AND}) + t_{XOR} + t_{su}$
- $T_{min} = 1,0 + 2(1,2) + 1,2 + 0,6 = 5,2 \text{ ns}$
- $F_{max} = 1/5,2 \text{ ns} = 192,31 \text{ MHz}$

Relógio “distorcido” (*clock skew*)

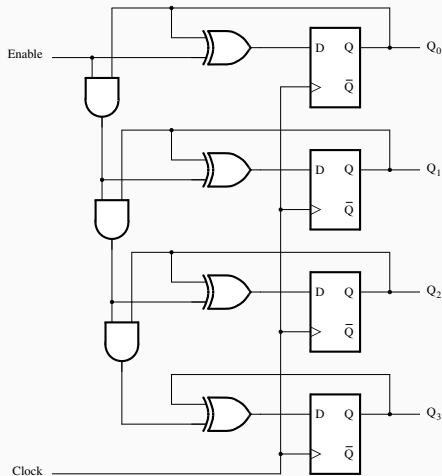
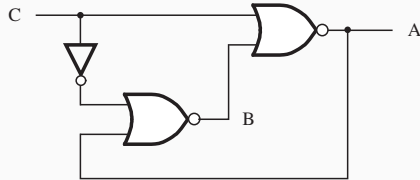


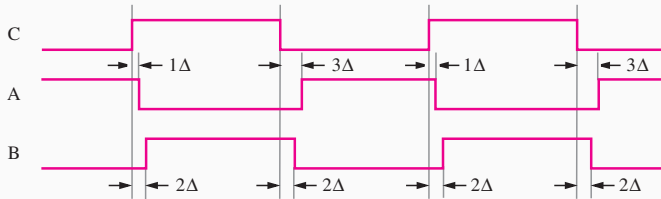
Figure 5.67 A 4-bit counter.

- $t_{skew} = 1,5 \text{ ns}$
- $T_{min} = t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su} - t_{skew}$
- $T_{min} = 1,0 + 3(1,2) + 1,2 + 0,6 - 1,5 = 4,9 \text{ ns}$
- $T_{min} = t_{cQ} + 2(t_{AND}) + t_{XOR} + t_{su}$
- $T_{min} = 1,0 + 2(1,2) + 1,2 + 0,6 = 5,2 \text{ ns}$
- $F_{max} = 1/5,2 \text{ ns} = 192,31 \text{ MHz}$
- $t_{cQ} + t_{AND} + t_{XOR} = 0,8 + 1,2 + 1,2 = 3,2 \text{ ns}$
 $> t_h + t_{skew} = 0,4 + 1,5 = 1,9 \text{ ns}$
- $t_{skew} \geq 2,8 \text{ ns}$

Exemplo de análise de tempo



(a) Circuit



(b) Timing diagram

Figure 5.70 Circuit for Example 5.18.

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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