

# MIPS32<sup>®</sup> Instruction Set

## Quick Reference

- R<sub>D</sub>  
R<sub>S</sub>, R<sub>T</sub>  
R<sub>A</sub>  
PC  
ACC  
Lo, Hi  
±  
∅  
::  
R2  
DOTTED
- DESTINATION REGISTER  
— SOURCE OPERAND REGISTERS  
— RETURN ADDRESS REGISTER (R31)  
— PROGRAM COUNTER  
— 64-BIT ACCUMULATOR  
— ACCUMULATOR LOW (ACC<sub>31:0</sub>) AND HIGH (ACC<sub>63:32</sub>) PARTS  
— SIGNED OPERAND OR SIGN EXTENSION  
— UNSIGNED OPERAND OR ZERO EXTENSION  
— CONCATENATION OF BIT FIELDS  
— MIPS32 RELEASE 2 INSTRUCTION  
— ASSEMBLER PSEUDO-INSTRUCTION

PLEASE REFER TO “*MIPS32 ARCHITECTURE FOR PROGRAMMERS VOLUME II: THE MIPS32 INSTRUCTION SET*” FOR COMPLETE INSTRUCTION SET INFORMATION.

ARITHMETIC OPERATIONS		
ADD	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> + R <sub>T</sub> (OVERFLOW TRAP)
ADDI	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = R <sub>S</sub> + CONST16 <sup>±</sup> (OVERFLOW TRAP)
ADDIU	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = R <sub>S</sub> + CONST16 <sup>±</sup>
ADDU	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> + R <sub>T</sub>
CLO	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = COUNTLEADINGONES(R <sub>S</sub> )
CLZ	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = COUNTLEADINGZEROS(R <sub>S</sub> )
LA	R <sub>D</sub> , LABEL	R <sub>D</sub> = ADDRESS(LABEL)
LI	R <sub>D</sub> , IMM32	R <sub>D</sub> = IMM32
LUI	R <sub>D</sub> , CONST16	R <sub>D</sub> = CONST16 << 16
MOVE	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = R <sub>S</sub>
NEGU	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = −R <sub>S</sub>
SEB <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = R <sub>S</sub> <sub>7:0</sub> <sup>±</sup>
SEH <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = R <sub>S</sub> <sub>15:0</sub> <sup>±</sup>
SUB	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> − R <sub>T</sub> (OVERFLOW TRAP)
SUBU	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> − R <sub>T</sub>

SHIFT AND ROTATE OPERATIONS		
ROTR <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub> , BITS5	R <sub>D</sub> = R <sub>S</sub> <sub>BIT55−1:0</sub> :: R <sub>S</sub> <sub>31:BIT55</sub>
ROTRV <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> <sub>RT40−1:0</sub> :: R <sub>S</sub> <sub>31:RT40</sub>
SLL	R <sub>D</sub> , R <sub>S</sub> , SHIFT5	R <sub>D</sub> = R <sub>S</sub> << SHIFT5
SLLV	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> << R <sub>T</sub> <sub>4:0</sub>
SRA	R <sub>D</sub> , R <sub>S</sub> , SHIFT5	R <sub>D</sub> = R <sub>S</sub> <sup>±</sup> >> SHIFT5
SRAV	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> <sup>±</sup> >> R <sub>T</sub> <sub>4:0</sub>
SRL	R <sub>D</sub> , R <sub>S</sub> , SHIFT5	R <sub>D</sub> = R <sub>S</sub> <sup>∅</sup> >> SHIFT5
SRLV	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> <sup>∅</sup> >> R <sub>T</sub> <sub>4:0</sub>

LOGICAL AND BIT-FIELD OPERATIONS		
AND	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> & R <sub>T</sub>
ANDI	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = R <sub>S</sub> & CONST16 <sup>∅</sup>
EXT <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub> , P, S	R <sub>S</sub> = R <sub>S</sub> <sub>P+5−1:P</sub> <sup>∅</sup>
INS <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub> , P, S	R <sub>D</sub> <sub>P+S−1:P</sub> = R <sub>S</sub> <sub>S−1:0</sub>
NOP		No-OP
NOR	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = ~(R <sub>S</sub>   R <sub>T</sub> )
NOT	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = ~R <sub>S</sub>
OR	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub>   R <sub>T</sub>
ORI	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = R <sub>S</sub>   CONST16 <sup>∅</sup>
WSBH <sup>R2</sup>	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = R <sub>S</sub> <sub>23:16</sub> :: R <sub>S</sub> <sub>31:24</sub> :: R <sub>S</sub> <sub>7:0</sub> :: R <sub>S</sub> <sub>15:8</sub>
XOR	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> ⊕ R <sub>T</sub>
XORI	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = R <sub>S</sub> ⊕ CONST16 <sup>∅</sup>

CONDITION TESTING AND CONDITIONAL MOVE OPERATIONS		
MOVN	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	IF R <sub>T</sub> ≠ 0, R <sub>D</sub> = R <sub>S</sub>
MOVZ	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	IF R <sub>T</sub> = 0, R <sub>D</sub> = R <sub>S</sub>
SLT	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = (R <sub>S</sub> <sup>±</sup> < R <sub>T</sub> <sup>±</sup> ) ? 1 : 0
SLTI	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = (R <sub>S</sub> <sup>±</sup> < CONST16 <sup>±</sup> ) ? 1 : 0
SLTIU	R <sub>D</sub> , R <sub>S</sub> , CONST16	R <sub>D</sub> = (R <sub>S</sub> <sup>∅</sup> < CONST16 <sup>∅</sup> ) ? 1 : 0
SLTU	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = (R <sub>S</sub> <sup>∅</sup> < R <sub>T</sub> <sup>∅</sup> ) ? 1 : 0

MULTIPLY AND DIVIDE OPERATIONS		
DIV	R <sub>S</sub> , R <sub>T</sub>	Lo = R <sub>S</sub> <sup>±</sup> / R <sub>T</sub> <sup>±</sup> ; Hi = R <sub>S</sub> <sup>±</sup> MOD R <sub>T</sub> <sup>±</sup>
DIVU	R <sub>S</sub> , R <sub>T</sub>	Lo = R <sub>S</sub> <sup>∅</sup> / R <sub>T</sub> <sup>∅</sup> ; Hi = R <sub>S</sub> <sup>∅</sup> MOD R <sub>T</sub> <sup>∅</sup>
MADD	R <sub>S</sub> , R <sub>T</sub>	ACC += R <sub>S</sub> <sup>±</sup> × R <sub>T</sub> <sup>±</sup>
MADDU	R <sub>S</sub> , R <sub>T</sub>	ACC += R <sub>S</sub> <sup>∅</sup> × R <sub>T</sub> <sup>∅</sup>
MSUB	R <sub>S</sub> , R <sub>T</sub>	ACC −= R <sub>S</sub> <sup>±</sup> × R <sub>T</sub> <sup>±</sup>
MSUBU	R <sub>S</sub> , R <sub>T</sub>	ACC −= R <sub>S</sub> <sup>∅</sup> × R <sub>T</sub> <sup>∅</sup>
MUL	R <sub>D</sub> , R <sub>S</sub> , R <sub>T</sub>	R <sub>D</sub> = R <sub>S</sub> <sup>±</sup> × R <sub>T</sub> <sup>±</sup>
MULT	R <sub>S</sub> , R <sub>T</sub>	ACC = R <sub>S</sub> <sup>±</sup> × R <sub>T</sub> <sup>±</sup>
MULTU	R <sub>S</sub> , R <sub>T</sub>	ACC = R <sub>S</sub> <sup>∅</sup> × R <sub>T</sub> <sup>∅</sup>

ACCUMULATOR ACCESS OPERATIONS		
MFHI	R <sub>D</sub>	R <sub>D</sub> = Hi
MFLO	R <sub>D</sub>	R <sub>D</sub> = Lo
MTHI	R <sub>S</sub>	Hi = R <sub>S</sub>
MTLO	R <sub>S</sub>	Lo = R <sub>S</sub>

JUMPS AND BRANCHES (NOTE: ONE DELAY SLOT)		
B	OFF18	PC += OFF18 <sup>±</sup>
BAL	OFF18	RA = PC + 8, PC += OFF18 <sup>±</sup>
BEQ	R <sub>S</sub> , R <sub>T</sub> , OFF18	IF R <sub>S</sub> = R <sub>T</sub> , PC += OFF18 <sup>±</sup>
BEQZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> = 0, PC += OFF18 <sup>±</sup>
BGEZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> ≥ 0, PC += OFF18 <sup>±</sup>
BGEZAL	R <sub>S</sub> , OFF18	RA = PC + 8; IF R <sub>S</sub> ≥ 0, PC += OFF18 <sup>±</sup>
BGTZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> > 0, PC += OFF18 <sup>±</sup>
BLEZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> ≤ 0, PC += OFF18 <sup>±</sup>
BLTZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> < 0, PC += OFF18 <sup>±</sup>
BLTZAL	R <sub>S</sub> , OFF18	RA = PC + 8; IF R <sub>S</sub> < 0, PC += OFF18 <sup>±</sup>
BNE	R <sub>S</sub> , R <sub>T</sub> , OFF18	IF R <sub>S</sub> ≠ R <sub>T</sub> , PC += OFF18 <sup>±</sup>
BNEZ	R <sub>S</sub> , OFF18	IF R <sub>S</sub> ≠ 0, PC += OFF18 <sup>±</sup>
J	ADDR28	PC = PC <sub>31:28</sub> :: ADDR28 <sup>∅</sup>
JAL	ADDR28	RA = PC + 8; PC = PC <sub>31:28</sub> :: ADDR28 <sup>∅</sup>
JALR	R <sub>D</sub> , R <sub>S</sub>	R <sub>D</sub> = PC + 8; PC = R <sub>S</sub>
JR	R <sub>S</sub>	PC = R <sub>S</sub>

LOAD AND STORE OPERATIONS		
LB	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM8(R <sub>S</sub> + OFF16 <sup>±</sup> ) <sup>±</sup>
LBU	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM8(R <sub>S</sub> + OFF16 <sup>±</sup> ) <sup>∅</sup>
LH	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM16(R <sub>S</sub> + OFF16 <sup>±</sup> ) <sup>±</sup>
LHU	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM16(R <sub>S</sub> + OFF16 <sup>±</sup> ) <sup>∅</sup>
LW	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM32(R <sub>S</sub> + OFF16 <sup>±</sup> )
LWL	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = LOADWORDLEFT(R <sub>S</sub> + OFF16 <sup>±</sup> )
LWR	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = LOADWORDRIGHT(R <sub>S</sub> + OFF16 <sup>±</sup> )
SB	R <sub>S</sub> , OFF16(R <sub>T</sub> )	MEM8(R <sub>T</sub> + OFF16 <sup>±</sup> ) = R <sub>S</sub> <sub>7:0</sub>
SH	R <sub>S</sub> , OFF16(R <sub>T</sub> )	MEM16(R <sub>T</sub> + OFF16 <sup>±</sup> ) = R <sub>S</sub> <sub>15:0</sub>
SW	R <sub>S</sub> , OFF16(R <sub>T</sub> )	MEM32(R <sub>T</sub> + OFF16 <sup>±</sup> ) = R <sub>S</sub>
SWL	R <sub>S</sub> , OFF16(R <sub>T</sub> )	STOREWORDLEFT(R <sub>T</sub> + OFF16 <sup>±</sup> , R <sub>S</sub> )
SWR	R <sub>S</sub> , OFF16(R <sub>T</sub> )	STOREWORDRIGHT(R <sub>T</sub> + OFF16 <sup>±</sup> , R <sub>S</sub> )
ULW	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = UNALIGNED_MEM32(R <sub>S</sub> + OFF16 <sup>±</sup> )
USW	R <sub>S</sub> , OFF16(R <sub>T</sub> )	UNALIGNED_MEM32(R <sub>T</sub> + OFF16 <sup>±</sup> ) = R <sub>S</sub>

ATOMIC READ-MODIFY-WRITE OPERATIONS		
LL	R <sub>D</sub> , OFF16(R <sub>S</sub> )	R <sub>D</sub> = MEM32(R <sub>S</sub> + OFF16 <sup>±</sup> ); LINK
SC	R <sub>D</sub> , OFF16(R <sub>S</sub> )	IF ATOMIC, MEM32(R <sub>S</sub> + OFF16 <sup>±</sup> ) = R <sub>D</sub> ; R <sub>D</sub> = ATOMIC ? 1 : 0

REGISTERS		
0	zero	Always equal to zero
1	at	Assembler temporary; used by the assembler
2-3	v0-v1	Return value from a function call
4-7	a0-a3	First four parameters for a function call
8-15	t0-t7	Temporary variables; need not be preserved
16-23	s0-s7	Function variables; must be preserved
24-25	t8-t9	Two more temporary variables
26-27	k0-k1	Kernel use registers; may change unexpectedly
28	gp	Global pointer
29	sp	Stack pointer
30	fp/s8	Stack frame pointer or subroutine variable
31	ra	Return address of the last subroutine call

DEFAULT C CALLING CONVENTION (O32)	
<p><b>Stack Management</b></p> <ul style="list-style-type: none"> <li>The stack grows down. <ul style="list-style-type: none"> <li>Subtract from \$sp to allocate local storage space.</li> <li>Restore \$sp by adding the same amount at function exit.</li> </ul> </li> <li>The stack must be 8-byte aligned. <ul style="list-style-type: none"> <li>Modify \$sp only in multiples of eight.</li> </ul> </li> </ul>	
<p><b>Function Parameters</b></p> <ul style="list-style-type: none"> <li>Every parameter smaller than 32 bits is promoted to 32 bits.</li> <li>First four parameters are passed in registers \$a0–\$a3. <ul style="list-style-type: none"> <li>64-bit parameters are passed in register pairs: <ul style="list-style-type: none"> <li>Little-endian mode: \$a1:\$a0 or \$a3:\$a2.</li> <li>Big-endian mode: \$a0:\$a1 or \$a2:\$a3.</li> </ul> </li> </ul> </li> <li>Every subsequent parameter is passed through the stack. <ul style="list-style-type: none"> <li>First 16 bytes on the stack are not used.</li> <li>Assuming \$sp was not modified at function entry: <ul style="list-style-type: none"> <li>The 1<sup>st</sup> stack parameter is located at 16(\$sp).</li> <li>The 2<sup>nd</sup> stack parameter is located at 20(\$sp), etc.</li> </ul> </li> <li>64-bit parameters are 8-byte aligned.</li> </ul> </li> </ul>	
<p><b>Return Values</b></p> <ul style="list-style-type: none"> <li>32-bit and smaller values are returned in register \$v0.</li> <li>64-bit values are returned in registers \$v0 and \$v1: <ul style="list-style-type: none"> <li>Little-endian mode: \$v1:\$v0.</li> <li>Big-endian mode: \$v0:\$v1.</li> </ul> </li> </ul>	

MIPS32 VIRTUAL ADDRESS SPACE				
kseg3	0xE000.0000	0xFFFF.FFFF	Mapped	Cached
ksseg	0xC000.0000	0xDFFF.FFFF	Mapped	Cached
kseg1	0xA000.0000	0xBFFF.FFFF	Unmapped	Uncached
kseg0	0x8000.0000	0x9FFF.FFFF	Unmapped	Cached
useg	0x0000.0000	0x7FFF.FFFF	Mapped	Cached

READING THE CYCLE COUNT REGISTER FROM C
<pre> unsigned mips_cycle_counter_read() {     unsigned cc;     asm volatile("mfc0 %0, \$9" : "=r" (cc));     return (cc &lt;&lt; 1); } </pre>

ASSEMBLY-LANGUAGE FUNCTION EXAMPLE
<pre> # int asm_max(int a, int b) # { #   int r = (a &lt; b) ? b : a; #   return r; # }          .text         .set      nomacro         .set      noreorder          .global   asm_max         .ent       asm_max  asm_max:     move    \$v0, \$a0        # r = a     slt     \$t0, \$a0, \$a1    # a &lt; b ?     jr      \$ra              # return     movn    \$v0, \$a1, \$t0    # if yes, r = b          .end       asm_max </pre>

C / ASSEMBLY-LANGUAGE FUNCTION INTERFACE
<pre> #include &lt;stdio.h&gt;  int asm_max(int a, int b);  int main() {     int x = asm_max(10, 100);     int y = asm_max(200, 20);     printf("%d %d\n", x, y); } </pre>

INVOKING MULT AND MADD INSTRUCTIONS FROM C
<pre> int dp(int a[], int b[], int n) {     int i;     long long acc = (long long) a[0] * b[0];     for (i = 1; i &lt; n; i++)         acc += (long long) a[i] * b[i];     return (acc &gt;&gt; 31); } </pre>

ATOMIC READ-MODIFY-WRITE EXAMPLE
<pre> atomic_inc:     ll      \$t0, 0(\$a0)      # load linked     addiu   \$t1, \$t0, 1      # increment     sc      \$t1, 0(\$a0)      # store cond'1     beqz    \$t1, atomic_inc  # loop if failed     nop </pre>

ACCESSING UNALIGNED DATA			
NOTE: ULW AND USW AUTOMATICALLY GENERATE APPROPRIATE CODE			
LITTLE-ENDIAN MODE		BIG-ENDIAN MODE	
LWR	RD, OFF16(Rs)	LWL	RD, OFF16(Rs)
LWL	RD, OFF16+3(Rs)	LWR	RD, OFF16+3(Rs)
SWR	RD, OFF16(Rs)	SWL	RD, OFF16(Rs)
SWL	RD, OFF16+3(Rs)	SWR	RD, OFF16+3(Rs)

ACCESSING UNALIGNED DATA FROM C
<pre> typedef struct {     int u; } __attribute__((packed)) unaligned;  int unaligned_load(void *ptr) {     unaligned *uptr = (unaligned *)ptr;     return uptr-&gt;u; } </pre>

MIPS SDE-GCC COMPILER DEFINES	
__mips	MIPS ISA (= 32 for MIPS32)
__mips_isa_rev	MIPS ISA Revision (= 2 for MIPS32 R2)
__mips_dsp	DSP ASE extensions enabled
_MIPSEB	Big-endian target CPU
_MIPSEL	Little-endian target CPU
_MIPS_ARCH_CPU	Target CPU specified by -march=CPU
_MIPS_TUNE_CPU	Pipeline tuning selected by -mtune=CPU

NOTES
<ul style="list-style-type: none"> <li>Many assembler pseudo-instructions and some rarely used machine instructions are omitted.</li> <li>The C calling convention is simplified. Additional rules apply when passing complex data structures as function parameters.</li> <li>The examples illustrate syntax used by GCC compilers.</li> <li>Most MIPS processors increment the cycle counter every other cycle. Please check your processor documentation.</li> </ul>

Arithmetic operations = 2 cycles

Shift and rotate operations = 1 cycle

Logical and bit-field operations = 1 cycle

Conditional testing and conditional move operations = 2 cycles

Multiply and divide operations = 5 cycles

Accumulator access operations = 1 cycle

Jumps and branches = 2 cycles

Load and stores operations = 4 cycles