ECE 385

Fall 2021

Experiment # 1

Introductory Experiment

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LA4/Thursday & 18:00-20:50 Huang Tianhao

I. Introduction

This is the first experiment of course **ECE 385 2021Fa** semester and it is designed to help us get familiar with fundamental equipment for future use, including both software (i.e. Quartus Prime) and hardware (i.e. Lab Kit). More specifically, in this lab, I design a **2-to-1 multiplexor** to avoid static hazards. I build two circuits for analysis, namely A and B. I find that the circuit for Part A has a glitch (called static-1 hazard) caused by gate delay of the **NAND gate**. And the glitch disappears when I add redundant terms into the circuit to get B. In addition, I also use the circuit to further explore (i.e. de-bouncer).

II. Written description of the circuit

In this experiment, I build two circuits for analysis, namely **Part A** and **B**. They are both 2-to-1 multiplexor and the only difference between them is that the circuit for Part A has a static hazard while Part B doesn't have any.

1) K-Map

A \ BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Figure 1

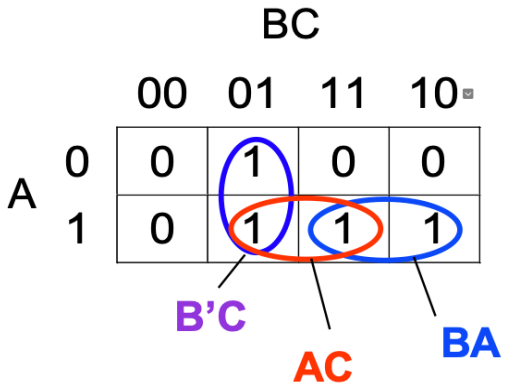

Figure 2

2) Circuit A

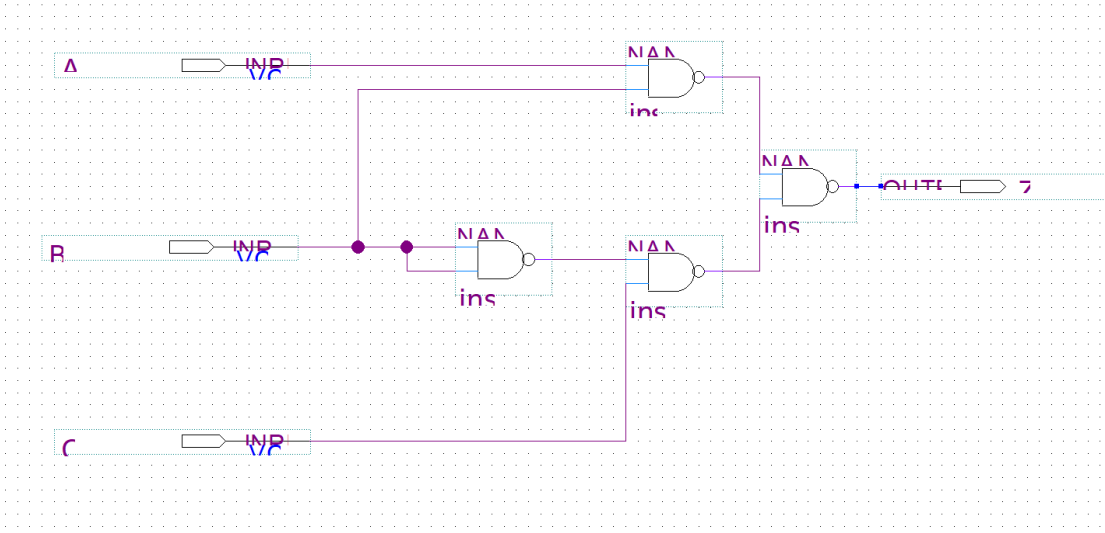

Figure 3

For Part A, the circuit has 3 inputs and 1 output, namely A, B, C and Z respectively shown as the Figure 3 above (if build with NAND gate). (The K-map is also shown as Figure 1 & 2 above). With previous knowledge, it is clear that the SOP (sum of product) is B'C+BA, shown as the following Figure 4 copied from the lecture notes (if build with AND, OR and NOT gates). It is clear that due to the existence of the NOT gate (or inverter), one gate delay will happen shown as the following Figure 5 and thus a static hazard will happen.

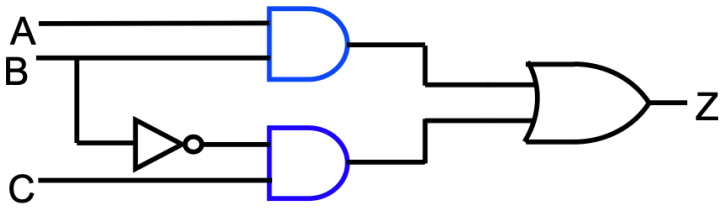

Figure 4

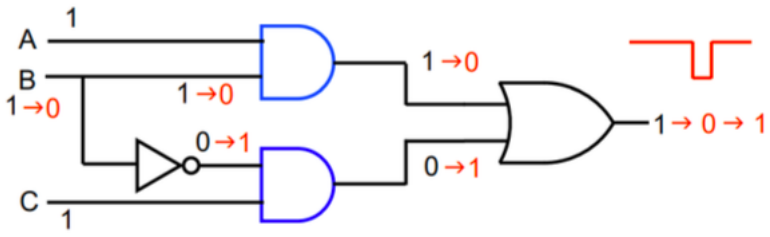

Figure 5

3) Circuit B

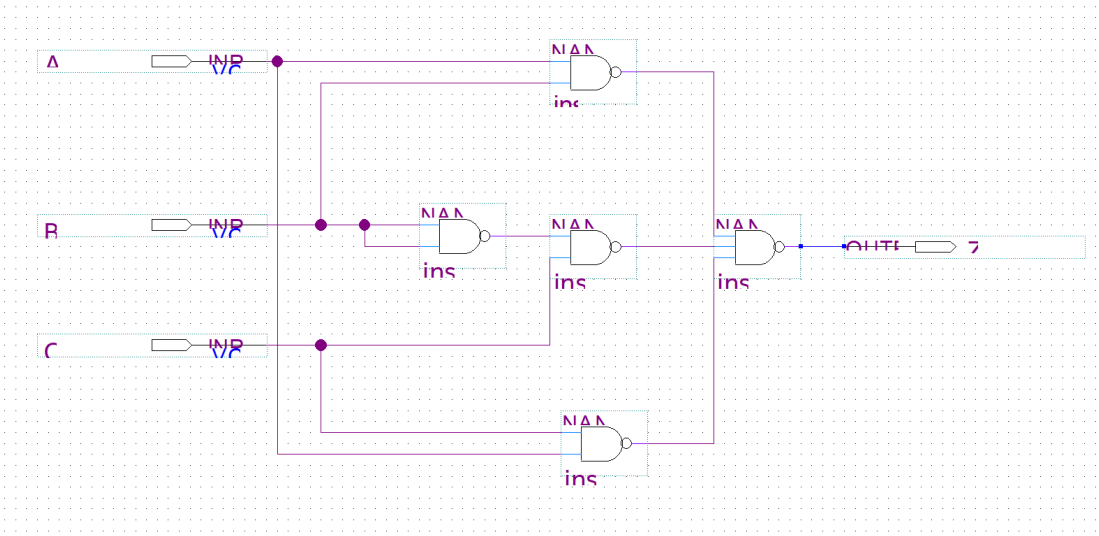

Figure 6

For Part B, the circuit also has 3 inputs and 1 output, namely A, B, C and Z respectively shown as Figure 6 above (if build with NAND gate). In order to avoid static-1 hazard in an SOP (sum of product) circuit, I decide to cover all adjacent min-terms in the K-map, in this case, add the term AC shown as Figure 2 above. Thus, the final Boolean function for glitch-free circuit is Z = B'C + BA + **AC**.

III. Documentations of the lab

1) Truth Table

a. Truth table of prelab part A

A	B	C	(AB)’	B’	(B’C)’	Z
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	0
0	1	1	1	0	1	0
1	0	0	1	1	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	1	0	0	1	1

b. Truth table of prelab part B

A	B	C	(AB)’	(AC)’	B’	(B’C)’	Z
0	0	0	1	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	1	1	0	1	0
0	1	1	1	1	0	1	0
1	0	0	1	1	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	1	1
1	1	1	0	0	0	1	1

2) Answers to Pre-Lab Questions

a. **Question**: Why don’t all groups may observe static hazards?

Answer: Because some chips might have less gate-delay time, resulting in less significant static hazards that can hardly be observed.

b. **Question**: Why does the hazard appear when you add more inverters or capacitors?

Answer: Because when I add more inverters or capacitors, the time signals need to pass through gates will increase due to the gate-delay, causing glitches, and thus hazard will appear.

3) Circuit Diagram

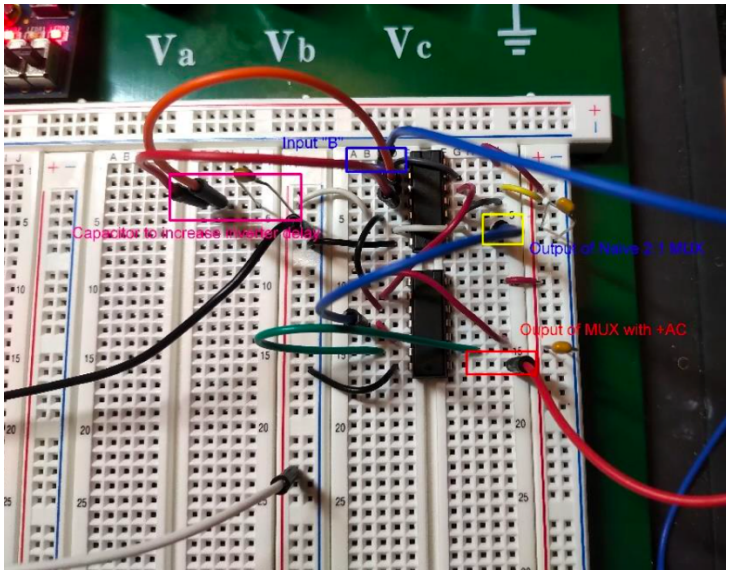

Figure 7

4) The Result of Circuit Part A

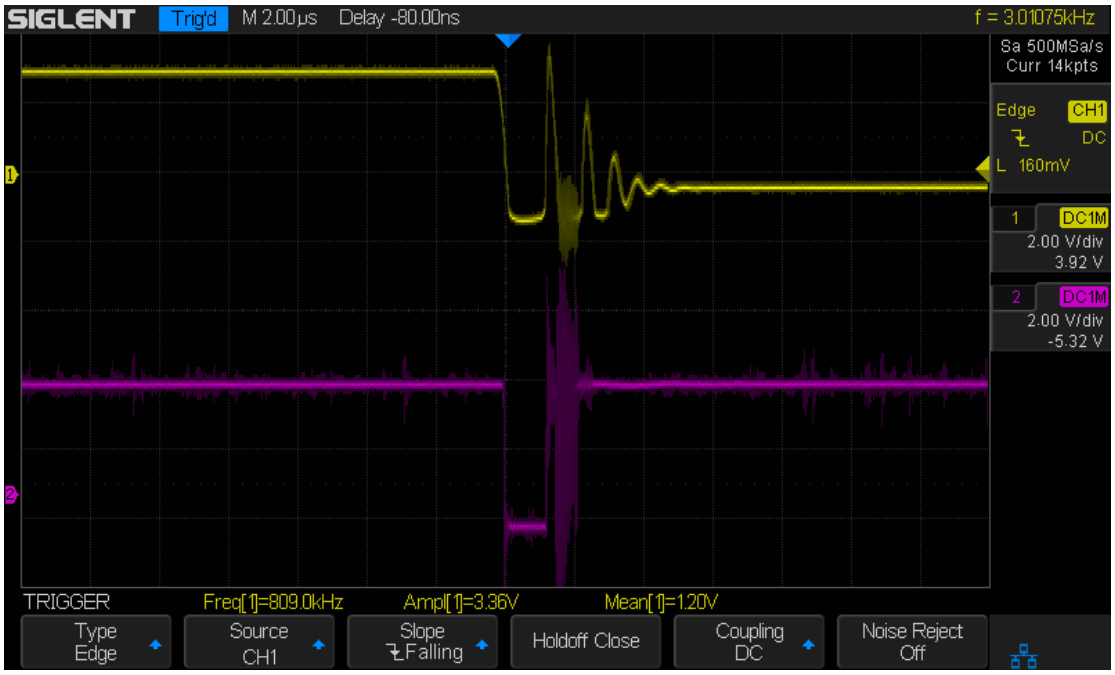

Figure 8

5) The Result of Circuit Part B

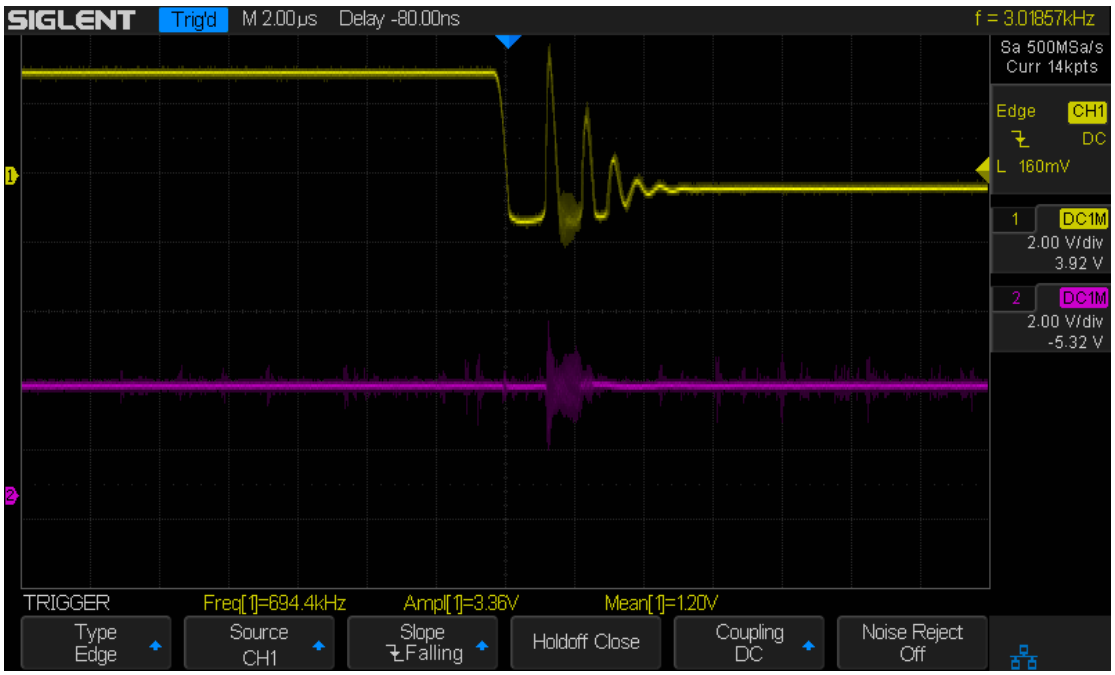

Figure 9

IV. Answers to Lab Questions Part 4

1) **Question**: Does the circuit in part B respond like the circuit of part A?

Answer: The circuit in part B does not respond like the circuit of A. Even though both of circuits from part A and part B have the same logic function, resulting in the

same truth table. However, since there is a redundant term in the circuit B and it could help eliminate the effect of gate-delay, thus avoiding the static-1 hazards.

2) **Question**: Describe and save the output and explain any differences between it and the results obtained in part 2.

Answer: From the demo during the lecture, it is clear that the output of part B circuit remains in 1 without glitch while the output of part A circuit falls at some time with glitch. The reason of this phenomenon is the redundant term (AC)', with which when C switches from 1 to 0, (AC)' and (AB)' will have the same gate delay, thus eliminating the delay of (B'C)'.

3) **Question**: For the circuit of part A of the prelab, at which edge of the input B are we more likely to observe a glitch at the output?

Answer: We are more likely to observe a glitch at the falling edge. That is because with an inverter, the input C will pass through much more gate-delay than input A. Suppose there is a condition that A and C are both 1 and B is switched from 1 to 0, the output Z in this case should remain 1. However, due to the inverter, the output from A side will change faster than the C side, and thus the output of OR gate will fall to 0 for a short period of time. While for rising edge, as the gate delay from A side is smaller, it will change to 1 faster, thus causing no obvious problem. Please see the diagram in the next page for more detailed explanation.

V. Answers to Post-Lab Questions

1) **Question**: How long does it take the output Z to stabilize on the falling edge of B (in ns)?

Answer: Output Z takes about 60ns to stabilize on falling edges of B.

2) **Question**: How long does it take on the rising edge (in ns)?

Answer: Output Z takes about 60ns to stabilize on rising edges of B.

3) **Question**: Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

Answer: Yes, there are some potential glitches in the output Z. Because (AB)' has 20ns time-delay, (B'C)' has 40ns time-delay and Z has 60ns time-delay. Thus, for the time period starting from 0ns to 20ns, (AB)' would change from 0 to 1 and become 1 after this period. And for the time period starting from 20ns to 40ns, (B'C)' would change from 1 to 0. It is clear that at t = 40ns, Z = ((B'C)' (AB)')' = 0 while (B'C)'=1, (AB)'=1, which is caused by the 1 gate-delay. And after the gate-delay, (B'C)' would turn into 0, Z turn back to 1 again. Thus a glitch occurs.

TIMING DIAGRAM

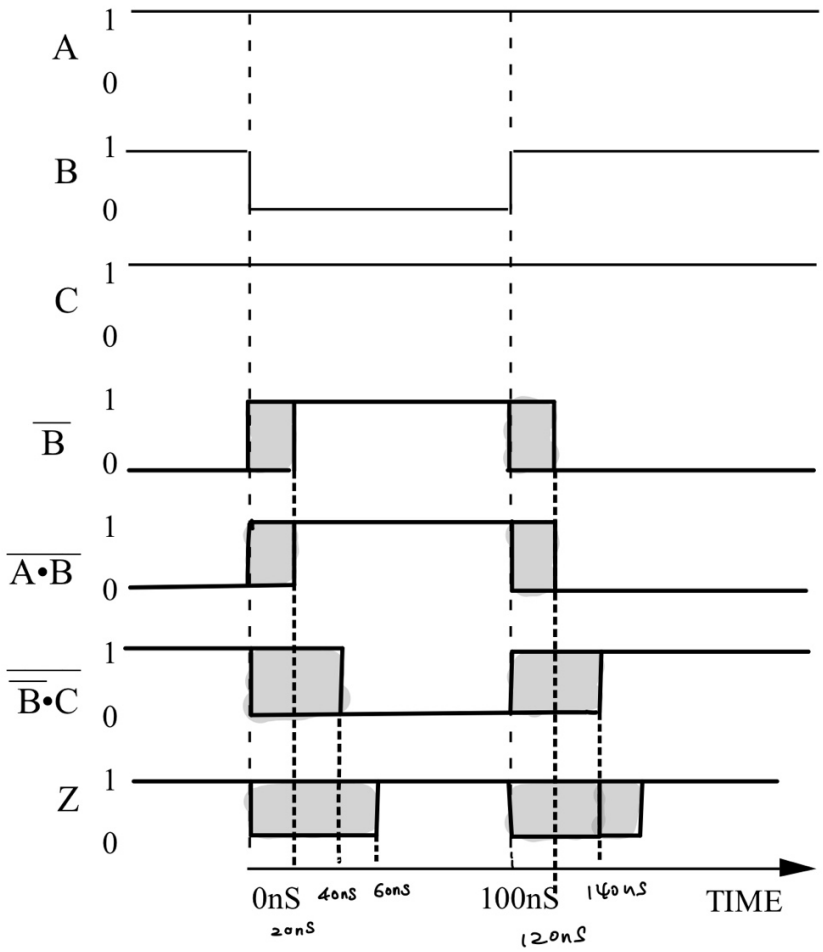

Figure 10

VI. Answers to General Guide Questions

1) GG.6: a. **Question**: What is the advantage of a larger noise immunity?

Answer: In order to keep its output stable the elements with larger noise immunity will have larger tolerance to noise, thus the circuit can be more noise-free.

b. **Question**: Why is the last inverter observed rather than simply the first?

Answer: Because the noise in the input voltage would make it hard for observation while by passing through several inverters, the signal could be rectified to simplify observation. Besides, the gate-delay could help extend time to get better observation.

c. **Question**: How could you calculate the noise immunity for the inverter?

Answer: I could firstly judge the output (i.e. high or low) by using the input voltage range and high or low limitations. And then we could just use upper voltage to subtract the lower one to get the noise immunity, shown as the Figure 11 below.

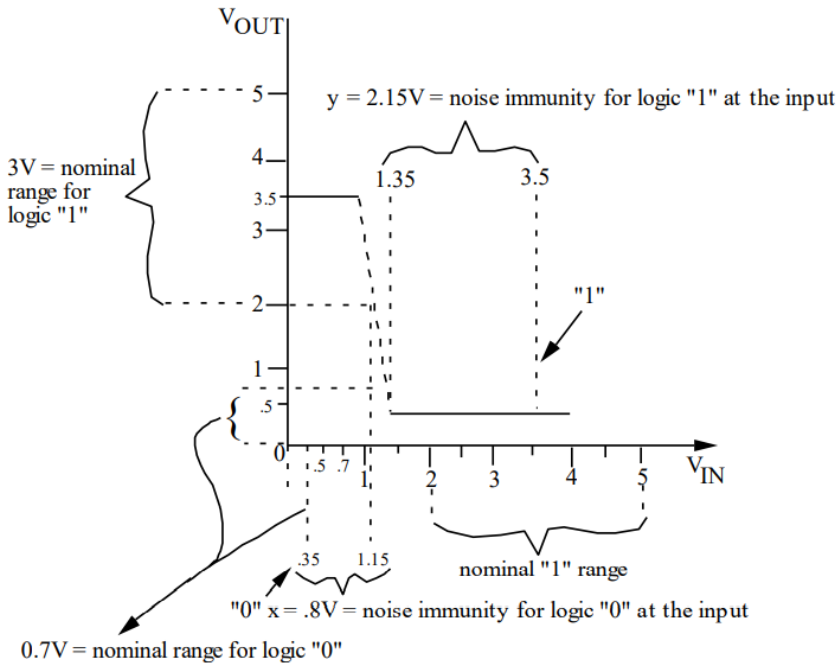

Figure 11

2) GG.29

Question: If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors.

Answer: If many LEDs share only one resistor and both of them work normally, the general current in the circuit may exceed threshold easily, and thus burning down the IC. Also, different type of LEDs may need different resistors to better assign current distribution. By the way, in this case, once a LED break (i.e. gets shorted), the whole circuit including all other LEDs will not work.

VII. Conclusion

In conclusion, in this experiment, I learn how to build a 2-to-1 multiplexor with only NAND gates, which helps me get familiar with Quartus Prime software and have better understanding about static hazards caused by the gate delay in this case. Besides, I get the idea about how to avoid static hazards (i.e. adding redundant term) and better understand about the glitch. Also, I learn about contact bounce and de-bouncer as well as noisy immunity, which turns out to be very important for future study.