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Modeling Statistical Dopant Fluctuations Effect on Threshold Voltage of Scaled JFET Devices

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ABSTRACT This paper presents a simple mathematical expression to model the effect of statistical dopant fluctuations on threshold voltage (V_{th}) of junction field-effect transistors (JFETs). The random discrete doping (RDD) in the active device area is used to derive an analytical model to compute the standard deviation, $\sigma V_{th,RDD}$ of the V_{th}-distribution for any arbitrary channel doping profiles. The model shows that the V_{th}-variability in JFETs depends on the active device area, channel doping concentration, and the depth of the channel depletion region of the gate/channel *pn*-junction. The model is applied to compute $\sigma V_{th,RDD}$ for symmetric and asymmetric source/drain double-gate n-channel JFETs. The simulation results show that the model can be used for predicting V_{th}-variability in JFETs.

INDEX TERMS Junction field-effect transistor (JFET), JFET threshold voltage variability, modeling threshold voltage variability, process variability in JFETs, random discrete doping, statistical dopant fluctuations.

I. INTRODUCTION

Recently, the junction field-ffect transistors (JFETs) have been the subject of numerous investigations for their possible applications in the ultra-low power very large scale integrated (VLSI) circuits [1]–[16]. The major advantage of JFETs is their low threshold voltage, $V_{th} \leq 0.25$ V to achieve the desired on-state current (I_{on}) at a supply voltage, $V_{dd} = 0.5$ V which leads to larger input common mode ranges [2], [5], [8], [17]. Another important advantage of JFETs is the channel modulation by applied gate voltage, V_{gs}. Since the gate can totally shut-off the channel, the on/off current ratio of the gate-modulated channel-JFETs is very large [5], [8], [17].

Recently, it has, also been reported that similar to metal-oxide-semiconductor field-ffect transistors (MOSFETs), the JFETs can, also, be scaled down to sub-10 nm regime [10], [11]. In order to understand the performance of these nanometer scale JFETs, device theory appropriate to these advanced devices has been developed [16]. However, as the devices are scaled down [10], [11], the process variability due to statistical dopant fluctuations must be modeled to optimize the circuit performance and mitigate the risk of process variability in the performance of VLSI chips [18]–[22]. Though, the compact models for computer-aided design (CAD) of VLSI JFET-circuits have been developed [16], [23], there is no reported study on modeling the impact of process variability on the performance of JFETs. Since with the scaling of devices, the process variability poses a severe challenge on the performance of VLSI devices, circuits, and systems [18]–[22], it is critical to model process variability in scaled JFET devices. It is well established that the major source of process variability is the random discrete doping (RDD) in the active region of the scaled VLSI devices [18], [21], [22]. RDD causes random variation in V_{th} which in turn causes device and circuit performance variability. Therefore, it is critical to model the impact of statistical dopant fluctuations on V_{th} of scaled JFET devices.

The objective of this paper is to develop an analytical model to study the effect of statistical dopant fluctuations on V_{th} of JFETs. In order to achieve this objective, first of all, a brief overview of the operating principles of JFETs is presented. Then a simplified mathematical expression for V_{th}-variance, $\sigma V_{th,RDD}$ is derived using dopant fluctuations in the active channel region of JFETs. The model is then used to compute the values of mismatch coefficients and $\sigma V_{th,RDD}$ for JFETs with two different types of device structures and results are discussed. Finally, conclusion on the usage of the model for estimating the V_{th}-variability on scaled JFETs is presented.

II. MODEL FORMULATION

In this section, an expression for $\sigma V_{th,RDD}$ for JFET devices is derived considering the stochastic distribution of dopants for any arbitrary one-dimensional (1D) channel doping profiles. In order to derive the model, first of all, the basic operation of JFETs is overviewed.

A. BASIC OPERATION OF JFET DEVICES

The detailed report on JFET device architecture and basic principle of device operation is available in the literature [5], [8] and is briefly described below. In order to describe the basic operation of JFETs, let us consider an ideal two-dimensional (2D) cross-section of a double-gate (DG) n-channel JFET (DG-nJFET) device structure with p+ gate as shown in Fig. 1 [8]. The idealized device structure shown in Fig. 1 consists of a p-type well region as the bottom gate and an n-type region where the n-channel, heavily doped p+ top-gate, shallow n-type source-drain extensions (n-SDE), and the heavily doped n+ deep source-drain (DSD) regions are formed [8].

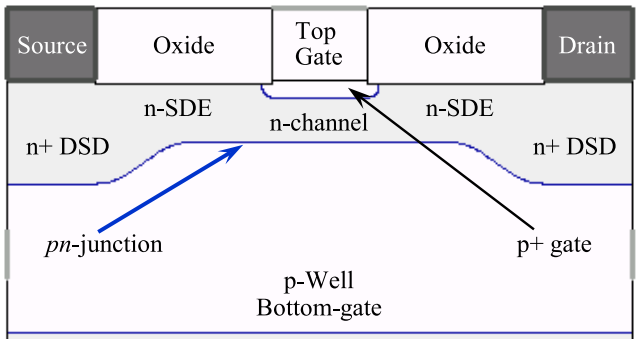

FIGURE 1. 2D cross-section of an ideal n-channel JFET device structure used for ultra-low power operation with n+ deep source-drains (DSDs), n-source-drain extensions (n-SDEs), a p+ top-gate, and a p-Well as the bottom-gate. The top and bottom gates are tied together to operate the device as a DG- nJFET. The *pn*-junction separates the n-region consisting of n+ DSD, n-SDE, and n-channel from the p-Well bottom gate region [8].

The channel of this device shown in Fig. 1 is modulated by an appropriate value of V_{gs} as shown in Fig. 2 for current flow under any target drain bias, V_{ds}. At $V_{gs} = 0$, the n-channel region under the gate is completely depleted by p+ gates and n-channel *pn*-junction depletion region, and the device shown in Fig. 1 is in the off-state. Fig. 2(a) shows the off-state of the device with a completely depleted channel under the biasing condition, $V_{gs} = 0 = V_{ds}$ whereas, Fig. 2(b) shows the same device with a conducting channel at the biasing condition, $V_{gs} = 0.5$ V and $V_{ds} = 0.05$ V. Thus, a conducting channel is modulated in a JFET by applying V_{gs} to facilitate the current flow from the source to drain of the device at any target applied V_{ds} similar to a MOSFET.

B. DERIVATION OF $\sigma V_{th,RDD}$

In order to develop an analytical model for V_{th}-variability due to RDD, let us consider an ideal single-gate nJFET device structure on a silicon layer of thickness t_{si} on a buried oxide (BoX) substrate as shown in Fig. 3. At $V_{gs} = 0 = V_{ds}$, the p+ gate/n-channel *pn*-junction depletion region in the channel region reaches the silicon/BoX interface to completely turning off the device. When $V_{gs} > 0$ at $V_{ds} = 0$, the gate/channel *pn*-junction is forward biased and the channel depletion region under the gate shrinks to open a conducting channel from the source to drain similar to Fig. 2(b). For a

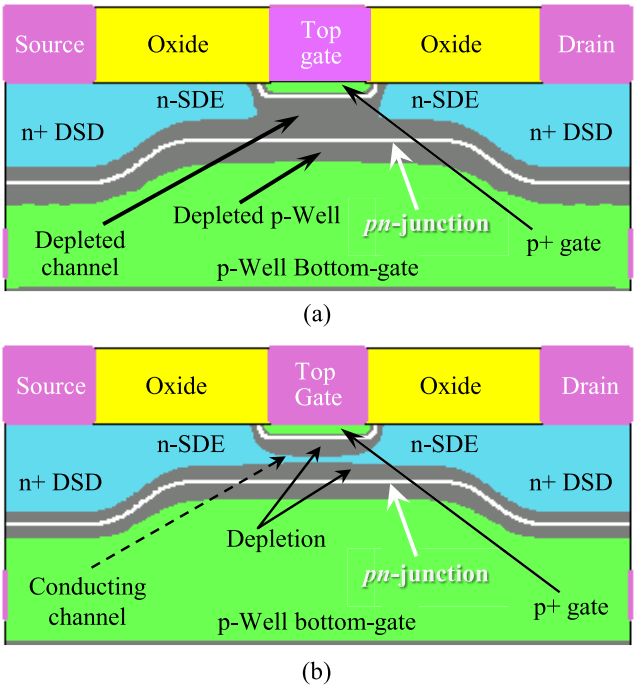

FIGURE 2. DG-nJFET device operations: (a) off-sate at $V_{gs} = V_{ds} = 0$ due to the completely depleted channel region; (b) gate-modulated conducting channel at $V_{gs} = 0.5$ V and $V_{ds} = 0.05$ V. The *pn*-junction separates the n-region consisting of n+ DSD, n-SDE, and n-channel from the p-Well bottom gate region [8].

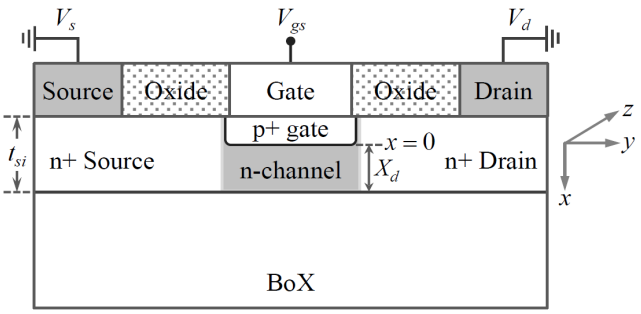

FIGURE 3. 2D cross-section of an ideal single gate nJFET device structure on silicon on a buried oxide (BoX) substrate with a p+ gate, an n-channel, and n+ source/drain regions; t_{si} is the thickness of the silicon body; (x, y, z) is the coordinate system with x along the depth, y along the channel length L, and z along the width W of the device; $x = 0$ at the p+ gate/n-channel metallurgical junction.

sufficiently strong forward bias V_{gs}, the channel depletion depth below the p+ gate region approaches to zero. Under this condition, the region below the gate is completely opened for conduction so that with any $V_{ds} > 0$, a drain current I_{ds} flows from the source to drain of the device.

In Fig. 3, x, y, and z represent the space along the depth, length L, and width W of the device, respectively with $x = 0$ at the gate/channel metallurgical junction. In the off-state of the device, $x = X_d$ is the depth of the gate/channel depletion reaching the channel/BoX interface similar to that in Fig. 2(a). For the simplicity of modeling, let us make the following simplifying assumptions:

1) The gate/channel is a one-sided step junction with channel doping concentration, N_b significantly lower than the heavily doped gate doping concentration; that is, X_d is the total depth of the gate/channel *pn*-junction depletion.
2) Channel doping can be represented by any arbitrary one-dimensional (1D) profiles along the x direction.
3) The channel region consists of a number of thin sheets of dopants of thickness dx and area WL stacked consecutively from the gate/channel metallurgical junction to channel/BoX interface.
4) For any fluctuations in N_b, the conducting channel depth is maintained the same by corresponding change in V_{gs}; this implies that the depth x of a sheet of dopants is maintained the same by corresponding change in V_{gs}.
5) V_{th} of a JFET is equal to the forward bias V_{gs} with $V_{ds} \cong 0$ at which the channel depletion layer shrinks from the BoX/channel interface to channel/gate metallurgical junction; that is, the depth of the conducting channel is equal to X_d at $V_{gs} = V_{th}$.
6) Dopant fluctuations in a sheet of dopants imply that the probability of finding the number of dopants in the sheet is '1' or '0.' In other words, the variance of dopant fluctuations in a sheet is the total number of dopants in the sheet.

Let us consider $V_{ds} \cong 0$. Then using *assumption* 2 for 1D channel doping profile along x direction only, the number of dopants per unit depth of a sheet of dopants (*assumption* 3) is $N_{sh} = N_b WL$. Where $N_b = N_d$ is the donor concentration in the channel region of an nJFET device and N_a is the acceptor concentration of the p+ gate.

If $dN_{sh}(x)$ is the fluctuations per unit depth of N_{sh} at a depth x, then by *assumption* 4 to maintain the depth of a sheet of dopants the same, the corresponding change in the vertical electric field $dE(x)$ due to V_{gs} (from Gauss's law) is

$$dE(x) = -\frac{q}{K_{si}\varepsilon_0}\frac{dN_{sh}(x)}{WL} \tag{1}$$

Since $dE(x) = -dV_{gs}/x$, then using *assumptions* 4 and 5, the corresponding change in V_{gs} and therefore, V_{th} is given by

$$dV_{gs}(x) = dV_{th}(x) = \frac{q}{K_{si}\varepsilon_0}\frac{dN_{sh}(x)}{WL}x \tag{2}$$

Since $dN_{sh}(x)$ is a random variable in the area WL at a depth x, therefore, $dV_{th}(x)$ is a random variable in this thin sheet of thickness dx of channel dopants. Then the total variation in V_{th} is a linear combination of random variables over the entire channel depth, X_d. Therefore, we can write from (2)

$$dV_{th}(X_d) = \int_0^{dV_{th}} dV_{th}(x) = \frac{q}{K_{si}\varepsilon_0}\frac{1}{WL}\int_0^{X_d} x dN_{sh} \tag{3}$$

where dV_{th} is the total fluctuations in V_{th} corresponding to the total dopant fluctuations in the entire channel region under the gate. Then the variance of V_{th} is given by

$$\begin{aligned} Var\left(dV_{th}(X_d)\right) &= \sigma^2_{V_{th}} \\ &= \left(\frac{q}{K_{si}\varepsilon_0}\frac{1}{WL}\right)^2 Var\left(\int_0^{X_d} x dN_{sh}\right) \end{aligned} \tag{4}$$

Now, we know that the variance of a sum is the sum of variances. Therefore, from (4), we get:

$$\begin{aligned} \sigma^2_{V_{th}} &= \left(\frac{q}{K_{si}\varepsilon_0}\frac{1}{WL}\right)^2 \int_0^{X_d} Var\left(dN_{sh}x\right) \\ &= \left(\frac{q}{K_{si}\varepsilon_0}\frac{1}{WL}\right)^2 \int_0^{X_d} \sigma^2_{N_{sh}}x^2 \end{aligned} \tag{5}$$

Since $\sigma^2_{N_{sh}} = Var(dN_{sh}) = N_b WL$ is the variance in a sheet of channel dopants per unit depth (*assumption* 6). Therefore, for a sheet of thickness dx, we can express (5) as,

$$\begin{aligned} \sigma^2_{V_{th}} &= \left(\frac{q}{K_{si}\varepsilon_0}\frac{1}{WL}\right)^2 \int_0^{X_d} \left(N_b WL dx\right)x^2 \\ &= \left(\frac{q}{K_{si}\varepsilon_0}\right)^2 \frac{N_b}{WL}\int_0^{X_d} x^2 dx \\ &= \left(\frac{q}{K_{si}\varepsilon_0}\right)^2 \frac{N_b}{WL}\frac{1}{3}X_d^3 \end{aligned} \tag{6}$$

From (6), the variance of V_{th} due to RDD in the channel region of a JFET device is given by

$$\begin{aligned} \sigma_{V_{th,RDD}} &= \frac{1}{\sqrt{3}}\frac{q}{K_{si}\varepsilon_0}\frac{N_b^{1/2}}{\sqrt{WL}}X_d^{3/2} \\ &= \frac{1}{\sqrt{3}}\frac{X_d}{K_{si}\varepsilon_0}q\frac{\sqrt{N_b}}{\sqrt{WL}}\sqrt{X_d} \end{aligned} \tag{7}$$

Now, for the one-sided gate/channel *pn*-junction (*assumption* 1), the depth of the zero-bias depletion region is given by [22]

$$X_d = \sqrt{\frac{2K_{si}\varepsilon_0}{qN_b}\cdot\phi_{bi}}, \tag{8}$$

where ϕ_{bi} is the built-in potential of the junction with N_a number of p+ gate doping concentration and $N_d = N_b$ number of channel doping concentration and is given by [22]

$$\phi_{bi} = \frac{kT}{q}\ln\left(\frac{N_a N_b}{n_i^2}\right) \tag{9}$$

Again, from *assumption* 5, the depth of the conducting channel in the on-state of the device is equal to the width

of the depletion region, X_d at $V_{gs} = 0$. Therefore, we can express (7) as

$$\begin{aligned}\sigma_{V_{th,RDD}} &= \frac{1}{\sqrt{3}}\frac{X_d}{K_{si}\varepsilon_0}q\frac{N_b^{1/2}}{\sqrt{WL}}\left(\sqrt{\frac{2K_{si}\varepsilon_0}{qN_b}\phi_{bi}}\right)^{1/2} \\ &= \frac{1}{\sqrt{3}}\frac{X_d}{K_{si}\varepsilon_0}q\frac{N_b^{1/2}}{\sqrt{WL}}\left(\frac{2K_{si}\varepsilon_0}{qN_b}\phi_{bi}\right)^{1/4} \\ &= \frac{\sqrt[4]{2}}{\sqrt{3}}\frac{X_d}{K_{si}\varepsilon_0}\sqrt[4]{q^3K_{si}\varepsilon_0\phi_{bi}}\cdot\frac{\sqrt[4]{N_b}}{\sqrt{WL}} \qquad (10)\end{aligned}$$

Now, we know that $K_{si}\varepsilon_0 = \varepsilon_{si}$ is the dielectric constant of silicon channel, therefore, we can write the expression for the V_{th}-variance in JFET devices from (10) as:

$$\sigma_{V_{th,RDD}} = C'\cdot\left(\sqrt[4]{q^3\varepsilon_{si}\phi_{bi}}\right)\frac{X_d}{\varepsilon_{si}}\cdot\left(\frac{\sqrt[4]{N_b}}{\sqrt{WL}}\right). \qquad (11)$$

Where C' is a number and its value depends on operating JFETs as a single gate or DG configuration in VLSI circuits. For a single gate JFET, the value of C' from (10) is 0.6866. For a symmetric DG-JFET with the top-gate and bottom-gate tied together, the depletion from each gate into the channel is $X_d/2$. Therefore, for DG-JFETs, the value of C' is 0.3433.

We know that the V_{th}-variance due to statistical dopant fluctuations in MOSFETs is given by [19]–[22]

$$\sigma^{MOSFETs}_{V_{th,RDD}} = C\cdot\left(\sqrt[4]{q^3\varepsilon_{si}\phi_B}\right)\frac{T_{ox}}{\varepsilon_{ox}}\cdot\left(\frac{\sqrt[4]{N_{CH}}}{\sqrt{WL}}\right) \qquad (12)$$

Where C is a number, T_{ox}, ε_{ox}, and N_{CH} are the gate oxide thickness, dielectric constant of oxide, and the channel doping concentration, respectively. It is to be noted that the value of C is 0.8165 [20] or 0.7071 [19] with or without the dopant fluctuations along the entire depth of the channel region [21], [22]. Comparing (11) and (12), we find that the expression for $\sigma\Delta V_{th,RDD}$ in JFETs with parameters C', ϕ_{bi}, X_d/ε_{si} $(=1/C_d)$, N_b, and X_d, is similar to that in MOSFETs with corresponding parameters C, ϕ_B, T_{ox}/ε_{ox} $(=1/C_{ox})$, N_{CH}, and T_{ox}; where C_d and C_{ox} are the gate/channel *pn*-junction capacitance for JFETs and gate oxide capacitance for MOSFETs, respectively. Thus, we find that X_d in JFETs is analogous to T_{ox} in MOSFETs. Intuitively, this can be understood from the gate formation of each type of device. In MOSFETs, the gate consists of a dielectric grown on the top of the channel region and T_{ox} controls the channel modulation and long channel V_{th}. Whereas in JFETs, the gate is a heavily doped extrinsic semiconductor forming a *pn*-junction with the channel and X_d modulates the channel as described in Fig. 2 and 4 and controls the electrostatics of the devices. Therefore, the V_{th} variation due to RDD in JFETs is expected to be similar to that in MOSFETs with appropriate set of device parameters given in (11).

For a particular complementary JFET (CJFET) technology [2], the thickness of the channel region is the same. Therefore, X_d is a constant for an optimized CJFET manufacturing technology similar to T_{ox} for a CMOS technology. Therefore, in (11), we can define a technology dependent parameter, C_{vt} as

$$C_{vt} = C'\cdot\left(\sqrt[4]{q^3\varepsilon_{si}\phi_{bi}N_b}\right)\cdot\frac{X_d}{\varepsilon_{si}}. \qquad (13)$$

Thus, for any particular CJFET technology, (11) can be expressed as

$$\sigma_{V_{th,RDD}} = C_{vt}\frac{1}{\sqrt{WL}}, \qquad (14)$$

Equation (14) shows that V_{th}-variability in JFETs due to statistical dopant fluctuations is inversely proportional to the square root of active device area similar to that in MOSFETs [19]–[22] and Eq. (13) and (14) show that it is directly proportional to X_d and $(N_b)^{1/4}$. Thus, we can estimate $\sigma\Delta V_{th,RDD}$ in JFETs using (14). From (13) and (14), it is obvious that $\sigma\Delta V_{th,RDD}$ due to RDD in JFETs can be minimized by reducing X_d and N_b. It is to be noted that for lower N_b, the depletion depth of the gate/channel *pn*-junction into the channel region increases. Since X_d depends on the thickness of the channel region, therefore, shallower channel implant with lower N_b can be used to reduce X_d as well as $\sigma\Delta V_{th,RDD}$ in JFET devices.

III. MODEL APPLICATION

The model derived in section IIB is applied to predict the effect of stochastic dopant fluctuations on V_{th} of DG-nJFETs. In order to model V_{th}-variability in JFETs, first of all, devices are selected from the published report to obtain N_b and calculate X_d and ϕ_{bi} from (8) and (9), respectively. Then C_{vt} is calculated from (13) to compute $\sigma\Delta V_{th,RDD}$ from (14).

A. DEVICE CONSIDERATION

The devices used to show the usage of the derived V_{th}-variability model are symmetric and asymmetric source/drain (S/D) 65 nm DG-nJFETs [8]. The detailed device architecture is described in [8] and is briefly described below. A symmetric S/D device structure, hereafter referred to as the "symmetric" device, includes symmetric source and drain regions as shown in Fig. 1 and 2. Whereas, an asymmetric S/D device structure, hereafter called the "asymmetric" device, shown in Fig. 4(a) includes a drain underlap region to reduce the off-state leakage current (I_{off}) of the device and improve the device performance [8]. In symmetric devices, the SDE-offset spacers on each side of the gate are used to reduce the high field effects at the n-SDE/p+ gate sidewall *pn*-junctions and therefore, reduce I_{off} [5], [8]. Whereas, in asymmetric devices, a wide offset spacer is used only at the drain-end of the p+ gate to create a drain underlap region as shown in Fig. 4(a) [8], [24]. Both the structures include a p-type well region with peak doping concentration of 5.5×10^{18} cm^{-3} as the bottom gate and an n-type region in which the n-channel, heavily doped p+ top-gate, shallow n-SDEs, and the heavily doped n+ DSD regions are formed. The peak doping concentration of the p+ gate, n-SDE regions,

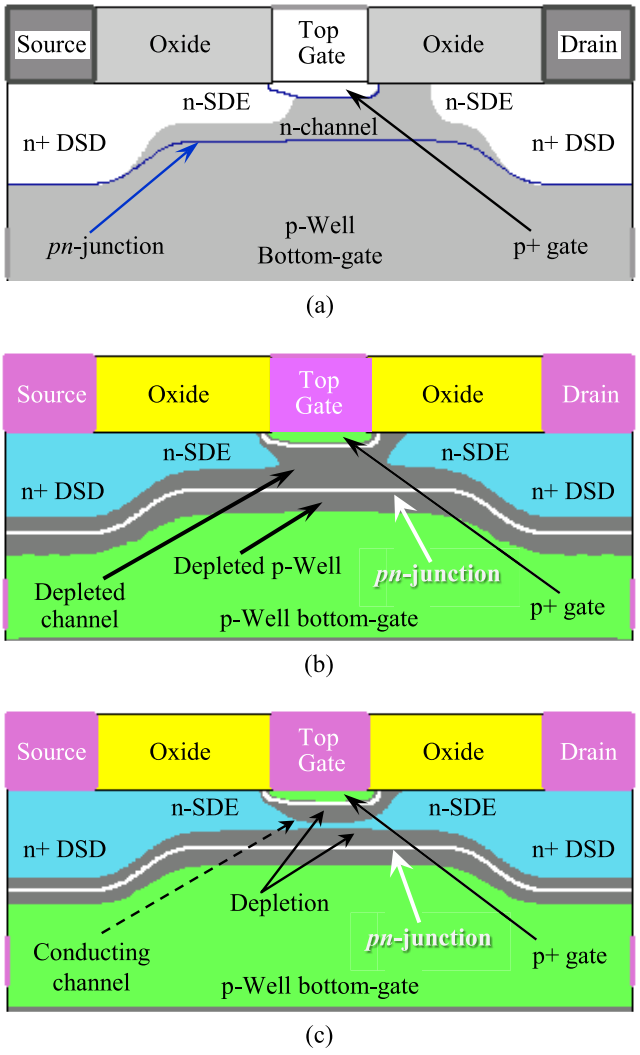

FIGURE 4. Asymmetric S/D DG-nJFET device operations: (a) device structure; (b) off-sate at $V_{gs} = V_{ds} = 0$ due to completely depleted channel region; (c) on-state with gate-modulated conducting channel at $V_{gs} = 0.5$ V and $V_{ds} = 0.05$ V. The *pn*-junction separates the n-region consisting of n+ DSD, n-SDE, and n-channel from the p-Well bottom gate region [8].

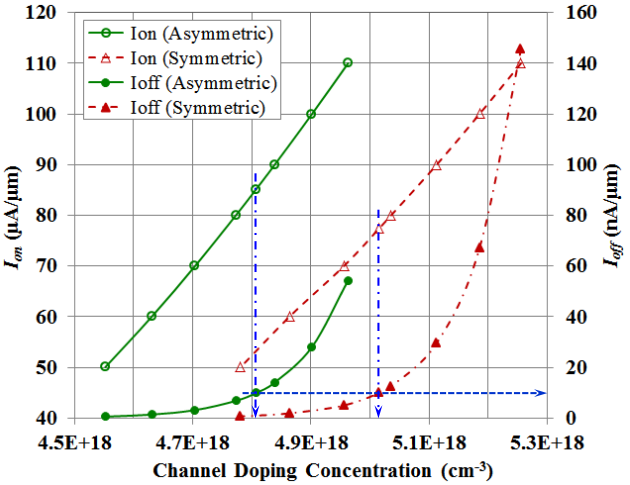

FIGURE 5. I_{on} and I_{off} versus N_b characteristics of 65 nm symmetric and asymmetric DG-nJFETs; plots show the optimized values of N_b for $I_{off} \cong 9.4$ nA/μm are 5.02×10^{18}cm^{-3} and 4.81×10^{18}cm^{-3} for the symmetric and asymmetric devices, respectively [8].

and n+ DSD regions is about 1×10^{20} cm^{-3} each and the n-channel doping concentration is varied to generate I–V characteristics and extract the device parameters as a function of N_b [8].

The $I_{ds} - V_{gs}$ characteristics of the symmetric and asymmetric devices are generated by numerical device simulation using MEDICI [25]. For device simulation, both the top and bottom gates are tied together to analyze the DG-nJFET device performance. Again, the detailed simulation methodology, models, and calibration of device models for accurate device simulation are described in [8] and [26] and outlined below. The DC device characteristics are generated using the drift-diffusion carrier transport model, Fermi-Dirac carrier distribution function with incomplete ionization, Philips universal carrier mobility model accounting for the distinct acceptor and donor scattering, carrier-carrier scattering, and screening, concentration-dependent Shockley-Reed-Hall and Auger generation-recombination models, band-to-band tunneling, and an effective field dependent impact ionization model [8], [26]. The simulated off-state and on-state of the 65 nm asymmetric DG-nJFET device are shown in Fig. 4(b) and (c), respectively [8].

From the simulation data the value of I_{off} is extracted at $V_{gs} = 0$ and $V_{ds} = 0.5$ V and that for I_{on} is extracted at $V_{gs} = 0.5$ V $= V_{ds}$. The simulated I_{on} and I_{off} versus N_b data for both the symmetric and asymmetric DG-nJFETs are shown in Fig. 5. From Fig. 5, the values of N_b for the symmetric and asymmetric devices are selected at the fixed value of $I_{off} \cong 9.4$ nA/μm. At this value of I_{off}, Fig. 5 shows that the values of N_b are 5.02×10^{18} cm^{-3} and 4.81×10^{18} cm^{-3} for the symmetric and asymmetric devices, respectively. It is, also, observed from Fig. 5 that I_{on} is higher for asymmetric devices ($\cong 85.2$ μA/μm) than the symmetric devices ($\cong 77.2$ μA/μm). Thus, asymmetric devices offer superior device performance at the same value of I_{off} as reported in [8].

B. COMPUTATION OF $\sigma V_{th,RDD}$

The optimized values of N_b for the symmetric and asymmetric DG-nJFETs obtained from Fig. 5, are used to compute the values $\sigma\Delta V_{th,RDD}$ for each type of devices. First of all, the values of N_b for symmetric and asymmetric devices are used to calculate the respective values of X_d and ϕ_{bi} from (8) and (9), respectively. Then using the calculated values of X_d and ϕ_{bi}, the values of C_{vt} for each device-type are computed from (13) using $C' = 0.3433$ for DG-JFETs. The computed values of C_{vt} for the symmetric and asymmetric devices are 2.0858 mV $\cdot$ μm and 1.9903 mV $\cdot$ μm, respectively. These values of C_{vt} for the symmetric and asymmetric devices are then used to calculate the values of $\sigma V_{th,RDD}$ of

the respective type of devices as a function of the device area. In order to calculate a set of device area, two sets of device dimensions are selected: one with a fixed L and varying W and the other with a fixed W and varying L. Thus, the $\{W, L\}$ sets considered are:

i) $\{5000\text{ nm} \leq W \leq 100, \text{nm } L = 200\text{ nm}\}$;
ii) $\{W = 500\text{ nm}, 20\text{ nm} \leq L \leq 500\text{ nm}\}$.

Also, each selected W and L pair of the sets is such that each value of WL of the sets is different, that is, no two WL values of the first and second sets are the same. Then for each type of devices, $\sigma V_{th,RDD}$ is calculated as a function of $(WL)^{-1/2}$ using (14) for the selected set of $\{W, L\}$ and plotted in Fig. 6 and for a selected set of $\{L\}$for different W as shown in Fig. 7.

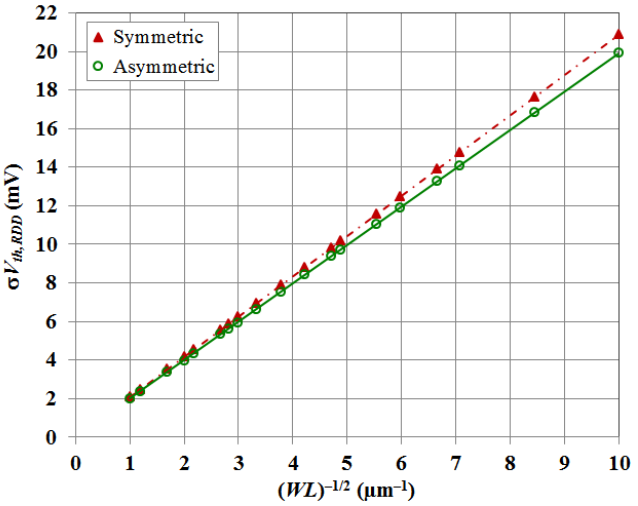

FIGURE 6. Plot of $\sigma V_{th,RDD}$ versus $\left(\sqrt{WL}\right)^{-1}$ of the symmetric and asymmetric DG-nJFETs; C_{vt} is the slope of the plot; the values of C_{vt} used in (14) to calculate $\sigma \Delta V_{th,RDD}$ are 2.0858 mV $\cdot \mu$m and 1.9903 mV $\cdot \mu$m for the symmetric and asymmetric devices, respectively.

IV. RESULTS AND DISCUSSIONS

Figure 6 shows $\sigma V_{th,RDD}$ versus $1/\sqrt{WL}$ plots for both the symmetric and asymmetric devices. Fig. 6 is known as the Pelgrom plot which is used to extract the mismatch coefficient, A_{vt} (defined as the slope of $\sigma \Delta V_{th}$ versus $(WL)^{-1/2}$ plot) from the measured V_{th}-distribution of two closely apart transistor pair [27]. From Fig. 6, the calculated values of $A_{vt}(\equiv \sqrt{2}C_{vt}$ [21], [22]) are 2.9497 mV $\cdot \mu$m and 2.8147 mV $\cdot \mu$m for the symmetric and asymmetric devices, respectively. Thus, we find from Fig. 6 that the mismatch coefficient for the asymmetric devices is lower than the symmetric devices. As a result, the value $\sigma V_{th,RDD}$ for the asymmetric devices is lower than the symmetric devices as shown in Fig. 6. The lower value of $\sigma V_{th,RDD}$ for the asymmetric devices is due to the lower value of N_b compared to that in symmetric devices.

Figure 7 shows the simulated $\sigma V_{th,RDD}$ versus L plots for DG-nJFETs with 10 nm $\leq L \leq$ 100 nm and $W = 30$ and 200 nm of a typical 65 nm CJFET technology. Fig. 7 shows

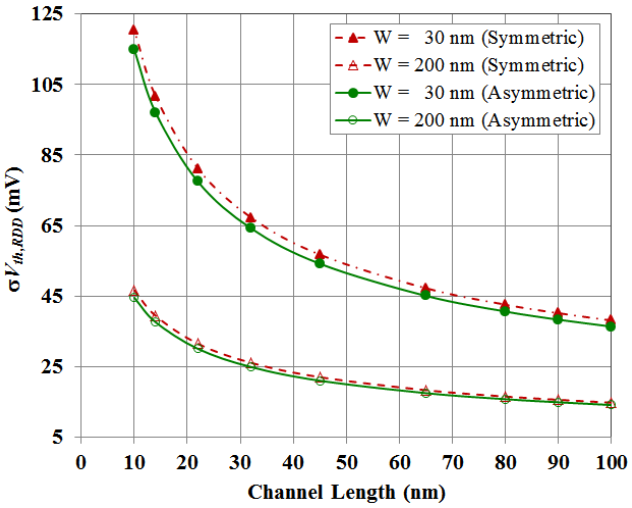

FIGURE 7. Simulated $\sigma V_{th,RDD}$ versus L for the symmetric and asymmetric DG-nJFETs of a typical 65 nm CJFET technology [8]; the values of C_{vt} used in (14) to calculate $\sigma \Delta V_{th,RDD}$ are 2.0858 mV $\cdot \mu$m and 1.9903 mV $\cdot \mu$m for the symmetric and asymmetric devices, respectively.

that $\sigma \Delta V_{th,RDD}$ for JFETs increases as the device dimensions are scaled down similar to MOSFETs. It is observed from Fig. 7 that for short and narrow DG-nJFETs with $L = 10$ nm and $W = 30$ nm, the V_{th}-variance is about 120 mV for the symmetric and 115 mV for asymmetric devices. On the other hand, for wider, $W = 200$ nm symmetric and asymmetric devices the V_{th}-variance is significantly low (about 45 mV for 10 nm devices) and is almost the same for both type of devices. Thus, Fig. 7 shows that the model for statistical variability of V_{th} predicts the similar behavior as the MOSFETs [21], [22] and therefore, can be used for statistical modeling of CJFET devices in circuit CAD and variability-aware circuit design.

In addition, the expression (14) shows that $\sigma \Delta V_{th,RDD}$ depends directly on X_d and therefore, can be optimized to reduce V_{th}-variability in JFETs. Since a thinner channel thickness, t_{si} ensures complete channel depletion in the off-state with lighter N_b, therefore, N_b can be optimized to reduce X_d and minimize $\sigma \Delta V_{th,RDD}$ in JFETs. Thus, the model can be used for device optimization and mitigate the risk of process variability on CJFET circuit performance. It is to be noted that reduced X_d and hence, thinner t_{si} will reduce the drive current. Therefore, appropriate trade-off between the device performance and V_{th} variability is required for device optimization.

It is seen from Fig. 7 that value of $\sigma \Delta V_{th,RDD}$ in DG-nJFETs can be reduced using an asymmetric device with drain underlap region and a heavily doped source region to scale down N_b as shown in Fig. 5. Fig. 5, also, shows that the asymmetric devices, offer higher I_{on} compared to the symmetric devices for the same value of I_{off} [8]. Therefore, the reported data [8] show that the asymmetric devices offer improved device performance and tend to offer lower V_{th} variability.

V. CONCLUSION

For the first time, an analytical V_{th}-variability model for JFET devices is presented in this paper to simulate the effect of statistical dopant fluctuations on V_{th} of the devices. The model shows that the V_{th}-variance, $\sigma V_{th,RDD}$ due to RDD in JFETs depends on the channel doping concentration N_b, active area of the device WL, and the depth of the gate/channel pn-junction depletion region X_d into the channel region. The model is validated by applying to symmetric and asymmetric DG-nJFET devices of a typical 65 nm CJFET technology to simulate $\sigma V_{th,RDD}$ as a function of $1/\sqrt{WL}$ to calculate the mismatch coefficient for each technology and $\sigma V_{th,RDD}$ as a function of L to show the effect of RDD on scaled devices. The simulation results show that the asymmetric DG-nJFETs offer lower $\sigma V_{th,RDD}$ compared to the symmetric devices. Since N_b for the asymmetric devices is lighter than the symmetric devices with lower expected RDD, therefore, the simulation data predict the expected results and validate the usefulness of the model for statistical analysis of CJFET VLSI circuits in circuit CAD tools.

The model, also, shows that $\sigma V_{th,RDD}$ in JFETs can be reduced by reducing X_d. Since X_d can be reduced by shallow channel region (pinning X_d at the bottom gate metallurgical junction), therefore, by keeping gate doping the same, N_b can be scaled down to completely deplete the channel in the off-state of JFET devices. Thus, the present analytical model can, also, be used for CJFET device optimization to reduce the effect of process variability on device and circuit performance. Therefore, the present analytical model can be used for statistical modeling of CJFET VLSI circuits for variability-aware circuit design as well as optimization of device performance to mitigate the risk of process variability in CJFET VLSI circuits.

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