



R818

Thermal Design Manual

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Contents

Revision History	i
Contents	ii
Figures	iii
1 About This Document	1
1.1 Purpose and Scope	1
1.2 Intended Audience	1
2 What Causes the High Temperature	2
3 Basics of the Thermal Design	3
3.1 Thermal Conduction	3
3.2 Thermal Convection	4
3.3 Thermal Radiation	5
3.4 Thermal Resistance	6
3.5 Thermal Resistance and Thermal Characterization Parameters of IC Package in JEDEC	6
3.6 Differences Among Thermal Resistance and Thermal Characterization Parameters	7
4 Thermal dissipation Path	9
4.1 Thermal dissipation on the Package	9
4.2 Thermal dissipation on the Board	11
4.2.1 Component Layout	11
4.2.2 Thermal Vias	12
4.2.3 Traces and Shapes	14
4.3 Thermal dissipation on the System	16
4.3.1 Ambient Temperature	16
4.3.2 Device Temperature	16
4.3.3 System Temperature Rise	16

Figures

Figure 3-1 Heat Transfer Modes	3
Figure 3-2 Methods for Optimizing Thermal Conduction	4
Figure 3-3 Thermal Convection Categories	4
Figure 3-4 Methods for Optimizing Thermal Convection	5
Figure 3-5 Methods for Optimizing Thermal Radiation	6
Figure 3-5 Thermal Resistance and Thermal Characterization Parameters	7
Figure 3-5 Relative Thermal Performance of Common Packages	8
Figure 3-5 Thermal dissipation Paths	9
Figure 3-5 Thermal dissipation on the Different Packages	9
Figure 3-5 Cavity-Up Package	9
Figure 4-1 Cavity-Down Package	10
Figure 4-1 R818 Package (Cavity-Down)	10
Figure 4-3 Layout for Heat-Generating Components	11
Figure 4-4 Drill Enough GND Vias under the Chip	12
Figure 4-3 Fully Connect the Cooling Pad and GND	12
Figure 4-4 Pastemask Openings on the EPAD	13
Figure 4-4 Evenly Drill GND Vias on the Thermal Pad	13
Figure 4-4 Traces and Shapes for the Important Power Supplies	14
Figure 4-4 Processing the Component Pads	14
Figure 4-4 Layout for Thermal-Sensitive Components	15
Figure 4-4 Soldermask Openings on Both Sides of the PMU	15

1 About This Document

1.1 Purpose and Scope

This document introduces the thermal design points and notes when designing application solutions with R818 chip.

As electronic products are becoming thinner and with higher performance, more components need to be placed on a smaller board, which requires the products to have a powerful cooling performance. To reduce the losses caused by thermal faults and improve the stability of the circuit, read this document carefully before you start your PCB design.

1.2 Intended Audience

This document is intended for:

- Thermal design engineers
- PCB layout engineers
- Hardware development engineers
- Technical support engineers

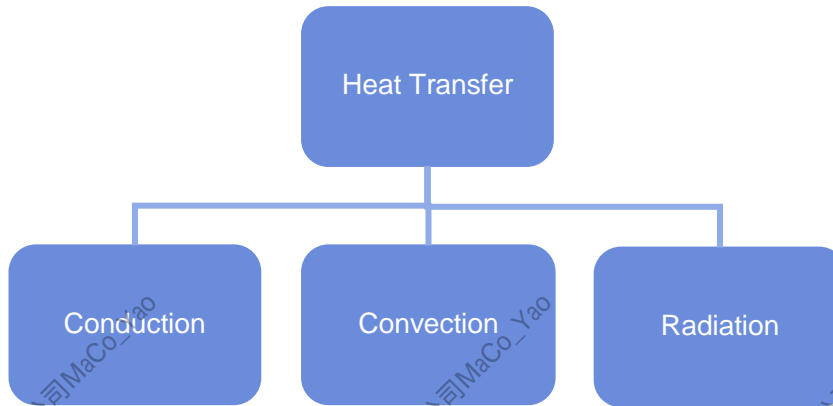
2 What Causes the High Temperature

When the IC is in operation, only a small part of the input power translates to the effective power, and the other part is translated into heat. The great majority of the heat is transmitted to the PCB and causes the temperature to rise. The overheating environment will affect the IC performance, lead to the failure of some components or even the whole IC.

3 Basics of the Thermal Design

There are three heat transfer modes: conduction, convection, and radiation, as the following figure shows.

Figure 3-1 Heat Transfer Modes



3.1 Thermal Conduction

Thermal conduction is the transfer of thermal energy within an object or between two objects in contact without the involvement of mass flow and mixing. It is the direct microscopic exchange of kinetic energy. The higher temperature object has molecules with more kinetic energy; collisions between molecules distribute this kinetic energy until an object (or objects in contact) has the same thermal energy throughout.

Thermal conduction is the primary path for heat leaving from the chips to the IC package.

The thermal conduction rate (Q) can be calculated by Fourier's law of thermal conduction:

$$Q = \lambda \cdot A \cdot (T_h - T_c) / \delta$$

Where,

λ is the thermal conductivity of the material (units: W/(m·°C)).

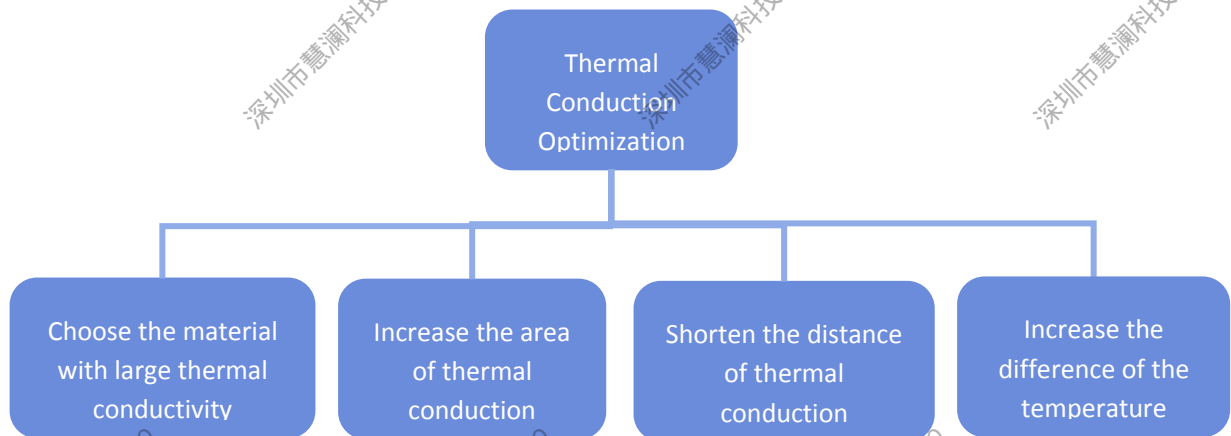
A is the area perpendicular to the thermal energy flow direction (units: m²).

T_h and T_c are the higher and lower temperature, respectively (units: °C).

δ is the distance through which heat conduction is taking place (units: m).

According to Fourier's law of thermal conduction, the heat conduction rate (Q) is proportional to the thermal conductivity of the material (λ), the section area (A), and the temperature difference (ΔT), and inversely proportional to the thermal conduction distance (δ). So, to optimize the thermal conduction, there are four methods as shown in the following figure.

Figure 3-2 Methods for Optimizing Thermal Conduction

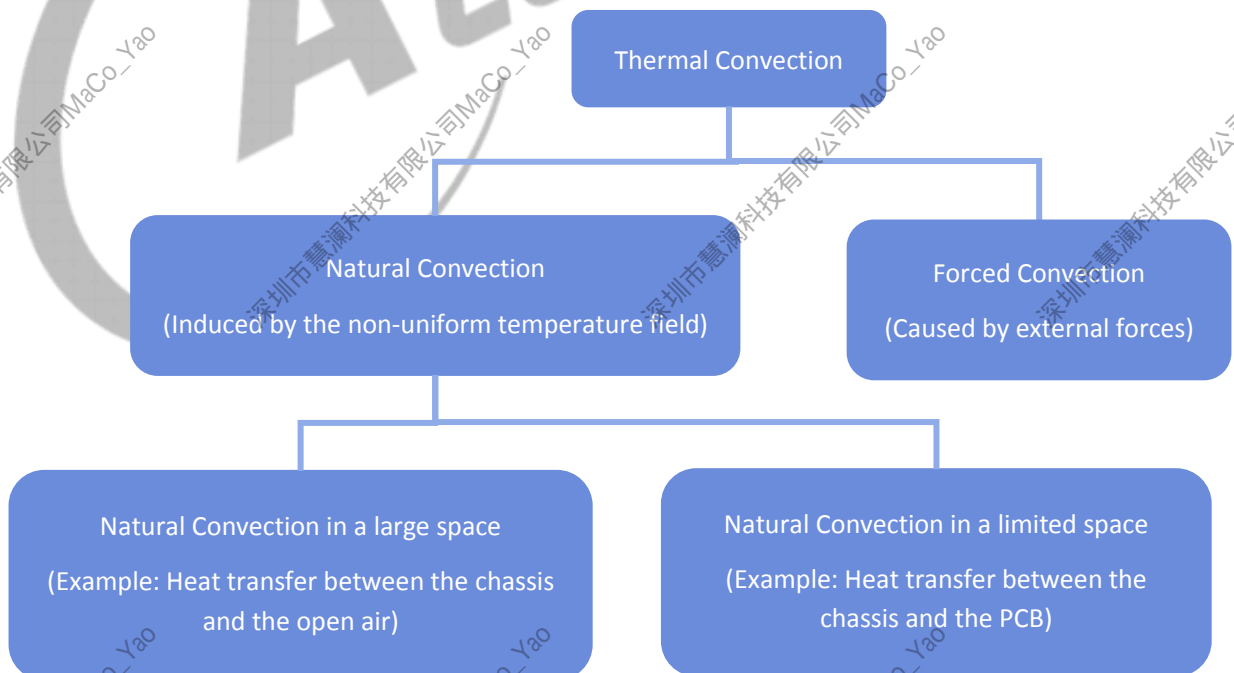


3.2 Thermal Convection

Thermal convection is a mode of heat transfer by the mass motion of a fluid such as water and air. It occurs on the surface of an object where the surrounding fluid of the object is heated and moved energy away from the source of heat.

According to the nature of the fluid flow, the convection heat transfer can be classified into the forced convection and natural convection. Forced convection occurs when the flow is caused by external means, such as a pump, a fan, and similar. In contrast, the flow of natural convection is induced by buoyancy forces, which arise from density differences caused by temperature variations in the fluid.

Figure 3-3 Thermal Convection Categories



The thermal convection rate (Q) can be calculated by Newton's Law of Cooling. Newton's Law of Cooling is used for both natural convection and forced convection. The following is the normal form of Newton's Law of Cooling:

$$Q = h \cdot A \cdot (T_2 - T_1)$$

Where,

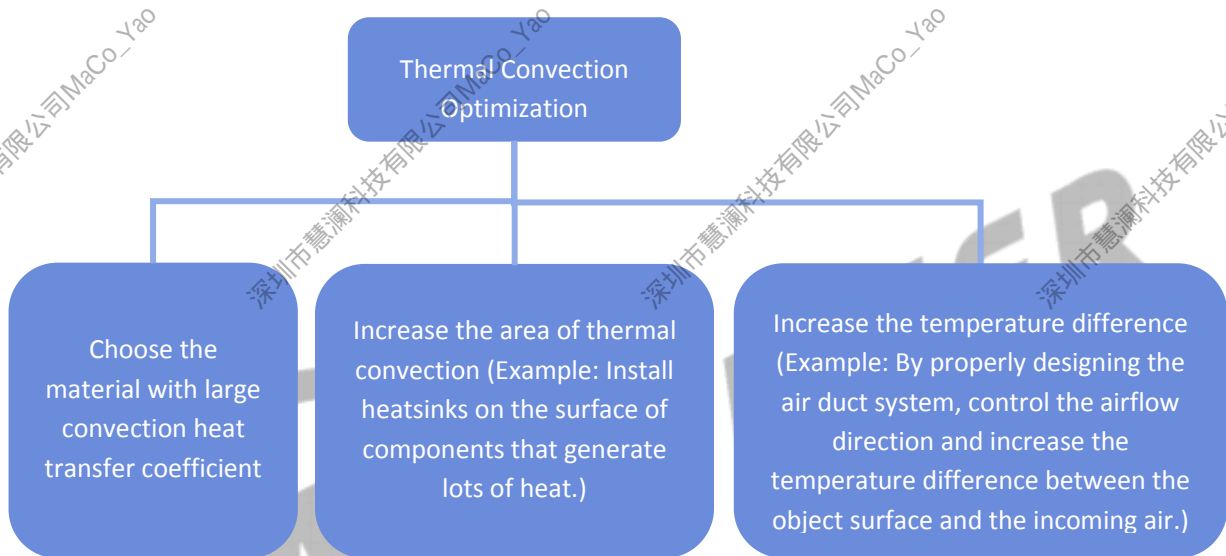
h is the convection heat transfer coefficient (units: $W/m^2 \cdot ^\circ C$).

A is the area perpendicular to the thermal energy flow direction (units: m^2).

T_2 and T_1 are the temperature of the heated object surface and the fluid, respectively. (units: $^\circ C$)

According to Newton's Law of Cooling, the heat convection rate (Q) is proportional to the convection heat transfer coefficient of the material (h), the section area (A), and the temperature difference ($T_2 - T_1$). So, to optimize the thermal convection, there are three methods as shown in the following figure.

Figure 3-4 Methods for Optimizing Thermal Convection



3.3 Thermal Radiation

Radiation is the process that objects deliver energy in the form of electromagnetic waves. All objects whose temperature is higher than absolute zero emit electromagnetic waves, and the process is called thermal radiation. Thermal radiation is a mode of heat transfer, and it is the only way for heat to transfer in a vacuum.

The total radiant flux emitted from the surface of an object at temperature T is expressed by the Stefan–Boltzmann law, in the form

$$Q = \varepsilon \cdot \sigma \cdot T^4$$

Where,

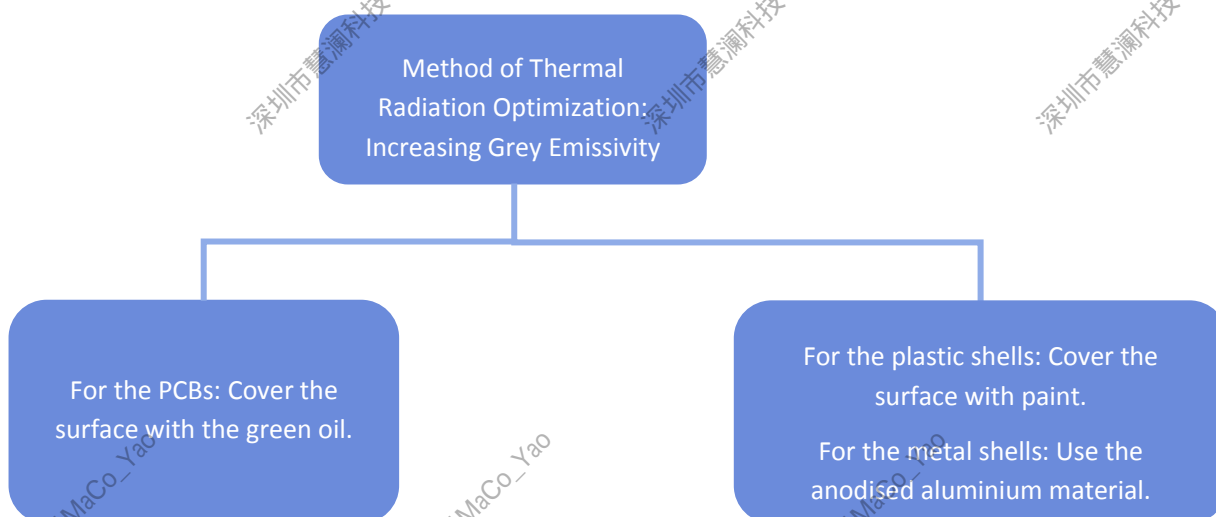
ε is the grey emissivity of the material (units: $W/m^2 \cdot ^\circ C$).

σ is the Stefan–Boltzmann constant ($5.67 \times 10^{-8} W \cdot / (m^2 \cdot K^4)$).

T is the absolute temperature of the object (units: K).

According to Stefan–Boltzmann law, increasing the grey emissivity of the material is the main method for enhancing the thermal radiation. The following figure shows how to increase the grey emissivity of the PCBs, plastic shells, and metal shells.

Figure 3-5 Methods for Optimizing Thermal Radiation



3.4 Thermal Resistance

Thermal resistance is a measurement of the temperature difference by which an object or material resists a heat flow. Just as electrical resistance is associated with the conduction of electricity, thermal resistance is associated with the conduction of heat.

Fourier's Law of Conduction can be rearranged into the form:

$$Q = \lambda \cdot A \cdot \frac{T_h - T_c}{\delta} = \frac{T_h - T_c}{\delta / (\lambda \cdot A)}$$

Newton's Law of Cooling can be rearranged into the form:

$$Q = h \cdot A \cdot (T_2 - T_1) = \frac{T_2 - T_1}{1 / (h \cdot A)}$$

The above two equations for heat flow are analogous to the relation for electric current flow I , expressed as:

$$I = \frac{V_2 - V_1}{R_e}$$

That is, the resistance to conductive heat transfer $R_{\text{cond}} = \delta / (\lambda \cdot A)$, and the resistance to convective heat transfer $R_{\text{conv}} = 1 / (h \cdot A)$.

3.5 Thermal Resistance and Thermal Characterization Parameters of IC Package in JEDEC

The following table shows the thermal resistance and thermal performance parameters of the IC package defined in JEDEC.

Table 3-1 Thermal Resistance and Thermal Characterization Parameters

Parameter	Description	Calculation
Thermal Resistance		
θ_{ja}	Thermal resistance from the silicon junction (chip) to ambient air temperature.	$\theta_{ja} = (T_j - T_a) / P$
θ_{jc}	Thermal resistance from the silicon junction (chip) to device case temperature.	$\theta_{jc} = (T_j - T_c) / P$
θ_{jb}	Thermal resistance from the silicon junction (chip) to board temperature.	$\theta_{jb} = (T_j - T_b) / P$

Parameter	Description	Calculation
Thermal Performance		
Ψ_{jt}	Thermal characterization parameter from the silicon junction (chip) to the package top.	$\Psi_{jt} = (T_j - T_t)/P$
Ψ_{jb}	Thermal characterization parameter from the silicon junction (chip) to the board.	$\Psi_{jt} = (T_j - T_b)/P$

Note:

T_j is the junction temperature of the chip (°C).

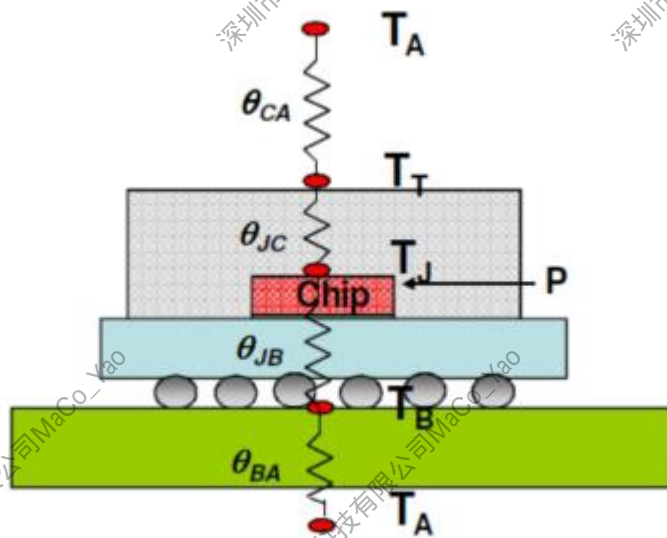
T_a is the ambient air temperature (°C).

T_b is the board temperature measured from the root of the chip (°C).

T_t is the temperature of the package top (°C).

The following figure shows the thermal resistance and thermal characterization parameters.

Figure 3-6 Thermal Resistance and Thermal Characterization Parameters



3.6 Differences Among Thermal Resistance and Thermal Characterization Parameters

Thermal resistance parameters, such as θ_{jc} and θ_{jb} , are the most common thermal metrics. Thermal resistance assumes that all heat flows from the junction to the destination location which remains isothermal.

Thermal characterization parameters are different from thermal resistances. Thermal characterization parameters measure heat flowing through multiple thermal paths rather than a single direct path, as in thermal resistances. Thermal characterization parameters are not true thermal resistances for this reason.

- **θ_{jc} and Ψ_{jt}**

θ_{jc} is the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area. When measuring θ_{jc} , it requires that all of the heat flows from the chip to the case and there is no heat transfer in any other path.

ψ_{jt} is the thermal characterization parameter from the junction to the package top. The measurement condition allows only a fraction of the heat flows from the junction to the package top. In practice, ψ_{jt} provides limited value for estimating the junction temperature by measuring the temperature of the package top.

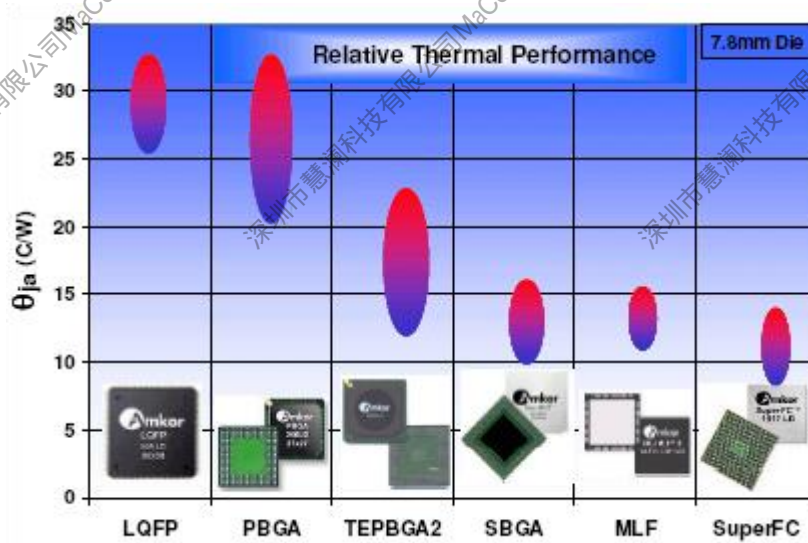
- θ_{jb} and ψ_{jb}

θ_{jb} is used to compare the figure of merits of the IC package thermal performance for chips mounted on the board. It is suitable for 2S2P PCB, not for IC packages with non-isothermal chips on the board.

ψ_{jb} is the thermal characterization parameter from the junction to the board. As mentioned above, it is different from θ_{jb} . $\theta_{jb} > \psi_{jb}$.

The following figure shows the relative thermal performance of common packages.

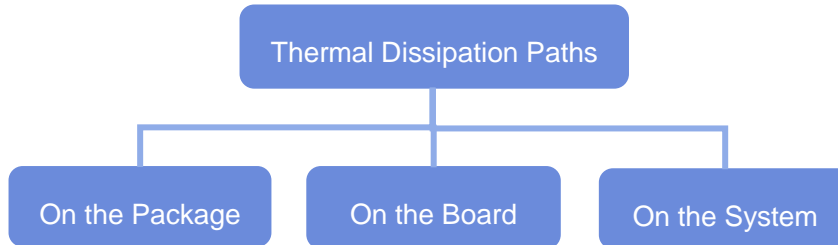
Figure 3-7 Relative Thermal Performance of Common Packages



4 Thermal dissipation Path

There are three major paths for thermal dissipation: thermal dissipation on the package, board, and system, as the following figure shows.

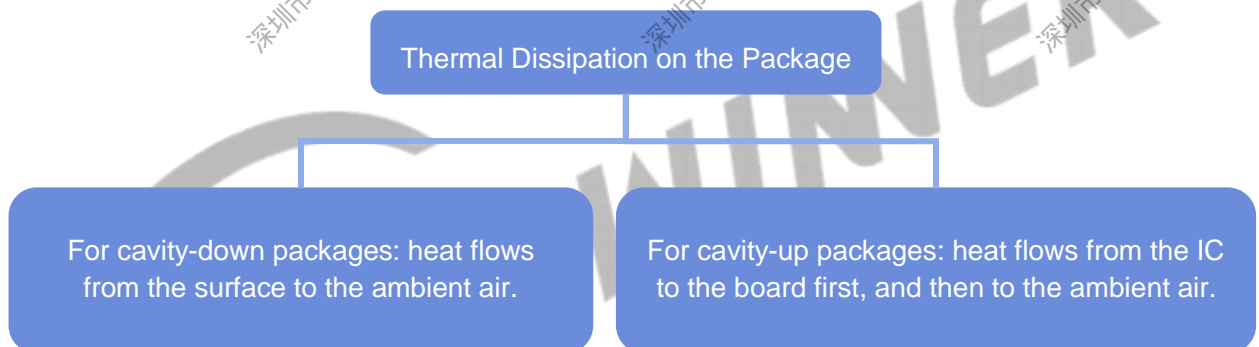
Figure 4-1 Thermal dissipation Paths



4.1 Thermal dissipation on the Package

For the package, the thermal dissipation path depends on the packaging structure. The following figure shows thermal dissipation paths for cavity-down and cavity-up packages.

Figure 4-2 Thermal dissipation on the Different Packages



The following figures show the cavity-down and cavity-up packages.

Figure 4-3 Cavity-Up Package

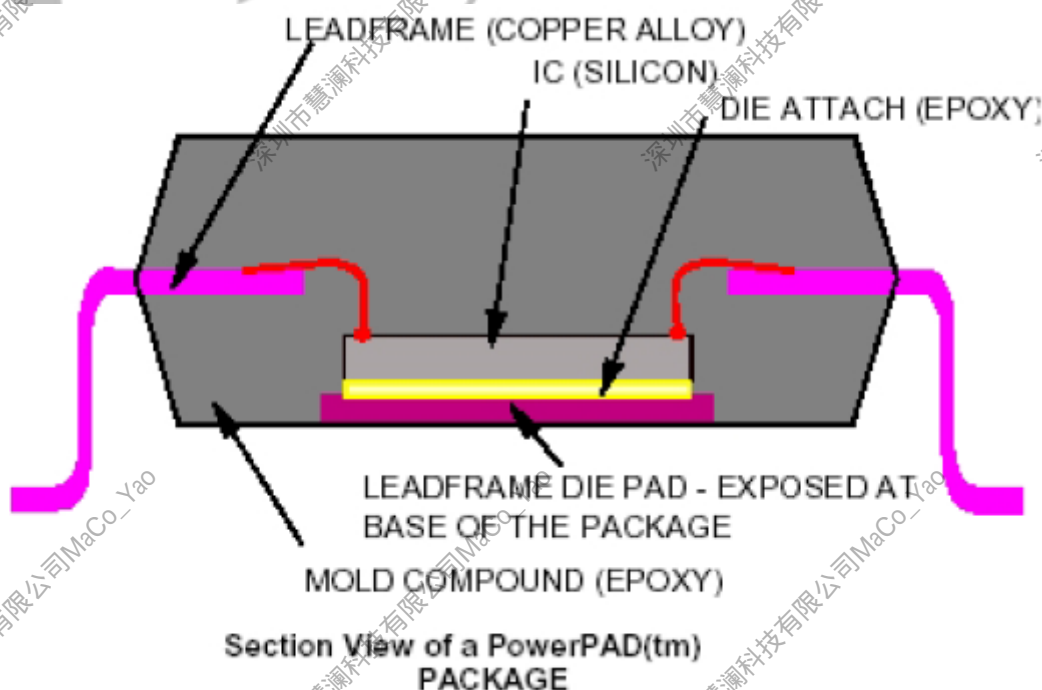
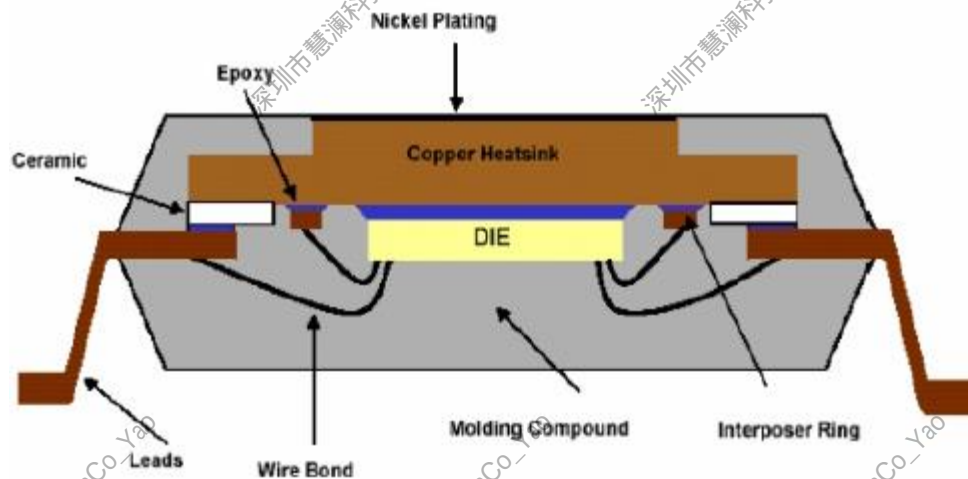
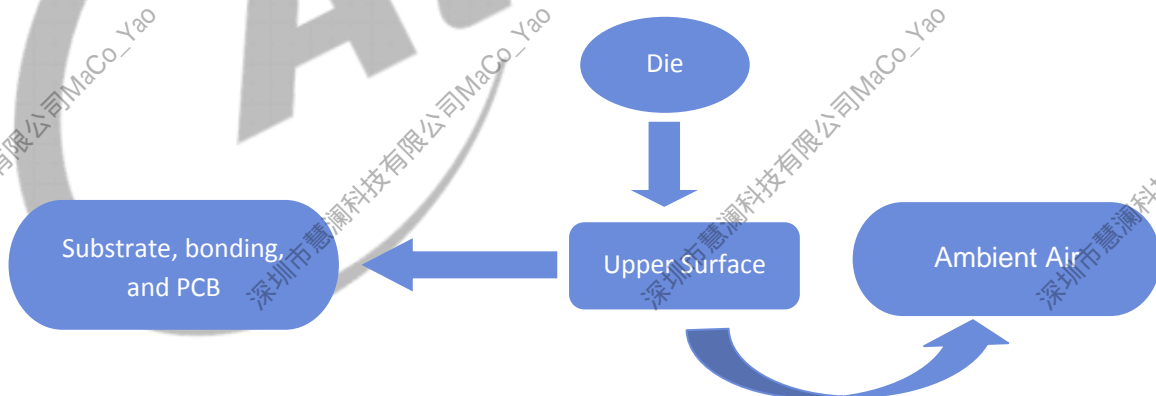
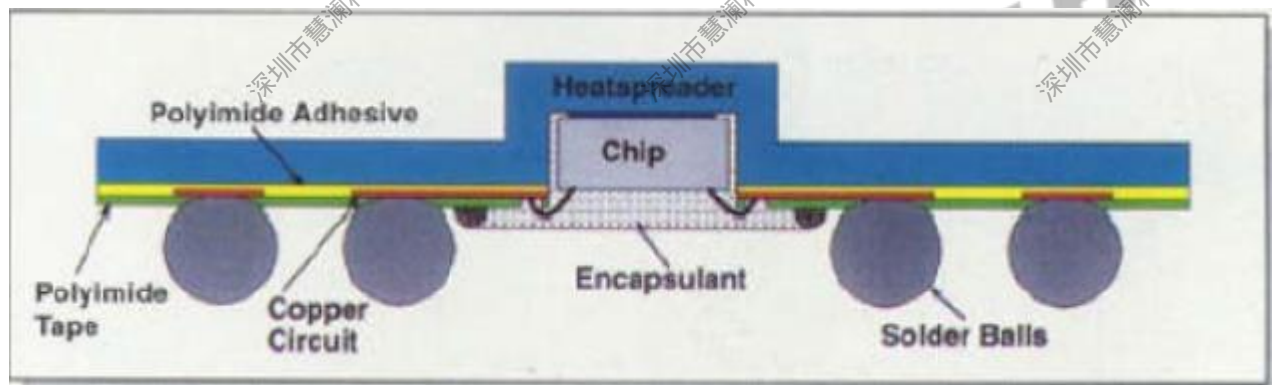


Figure 4-4 Cavity-Down Package



R818 adopts the cavity-down package, as the following figure shows.

Figure 4-5 R818 Package (Cavity-Down)



TIP

When implementing thermal design for a single-board chip, make sure the thermal dissipation method you choose is based on the package structure.

4.2 Thermal dissipation on the Board

4.2.1 Component Layout

1. When the natural convection is implemented, consider placing the PCB vertically first. When placed vertically, the air can flow through the surface of components effectively, while when placed horizontally, the airflows upward and away from the surface of the components. When the forced convection is implemented, you can place the PCB either vertically or horizontally because the components are mainly cooled by the wind caused by the external force like a fan.
2. If possible, place the heat-generating components like the CPU and PMU on the top layer (near the LCD) of the board. It allows you to easily mount the heatsink and make it contact with the metal rim for better thermal dissipation. Also, it facilitates the shield casing to be better grounded.
3. For components that generate little heat or have poor thermal resistance, place them to the upstream of the cooling airflow. For components that generate much heat or has good thermal resistance, place them to the downstream of the cooling airflow.
4. Evenly place the heat-generating components to keep the thermal characterization on the board surface uniform, which can avoid local overheating on the area with high power density.
5. Place components that generate the most heat and consume the largest amount of power to the position with the best thermal dissipation. Do not place components like the CPU and PMU to the corner or edge of the board. Also, choose a large package for the power resistors.
6. Place thermal-sensitive components to the low-temperature area and keep them as far away as possible from heat sources or isolate them from heat sources with other components.

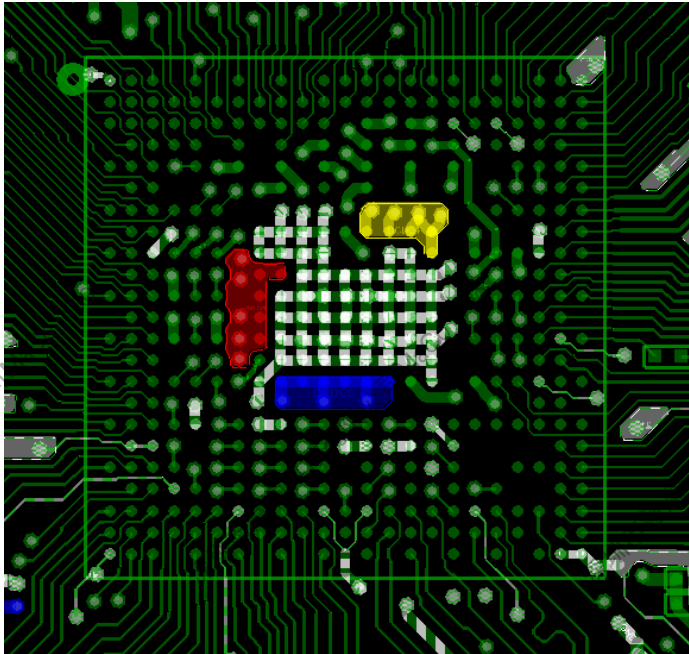
Figure 4-6 Layout for Heat-Generating Components



7. Place the main ground plane as close to the components as possible so that the components can dissipate heat through the shape. For R818, the GND bonding in the center of the BGA is for thermal dissipation, make sure it is connected to the ground plane.

- When mounting components, try to reduce the thermal resistance between the heatsink surface and the shell (the contact resistance). For multi-layer boards, drill as many GND vias as possible to reduce the conduction thermal resistance. The GND vias act as the thermal dissipation path here.

Figure 4-7 Drill Enough GND Vias under the Chip

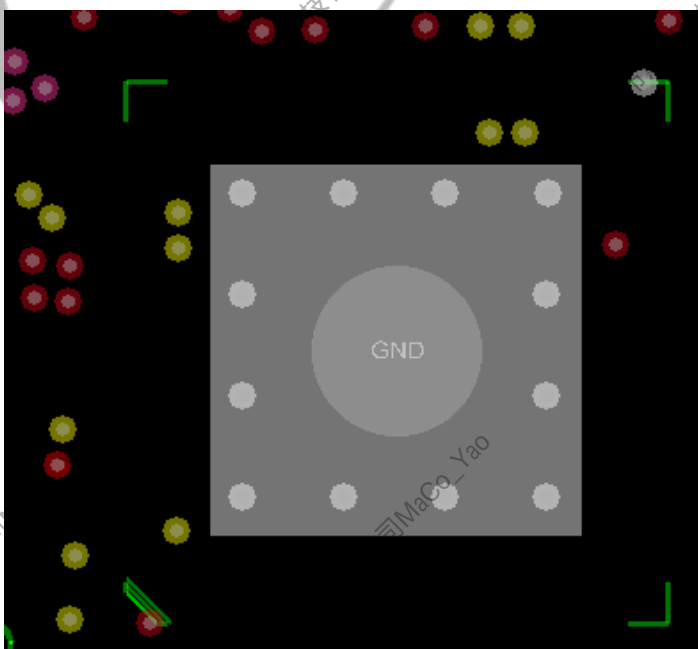


4.2.2 Thermal Vias

- For ICs with QFP or QFN packages, the cooling pad area should not be smaller than the EPAD area. The EPAD acts as the main thermal dissipation path because the thermal resistance from the junction to the EPAD is far smaller than that to the plastic shell, and heat tends to flow along the path with the smallest thermal resistance. If you choose to dissipate thermal through vias, fully connect the cooling pads with the ground plane at each layer. Do not connect them with the thermal relief pad.

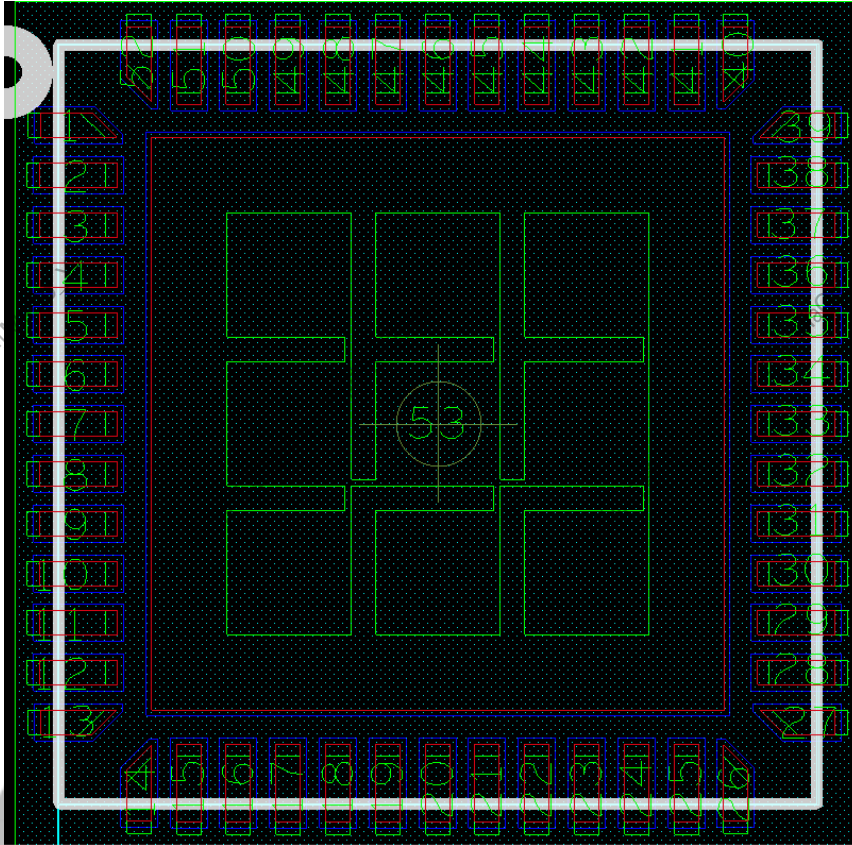
The following figure shows the cooling pad connection of the PMU in R818 platform.

Figure 4-8 Fully Connect the Cooling Pad and GND



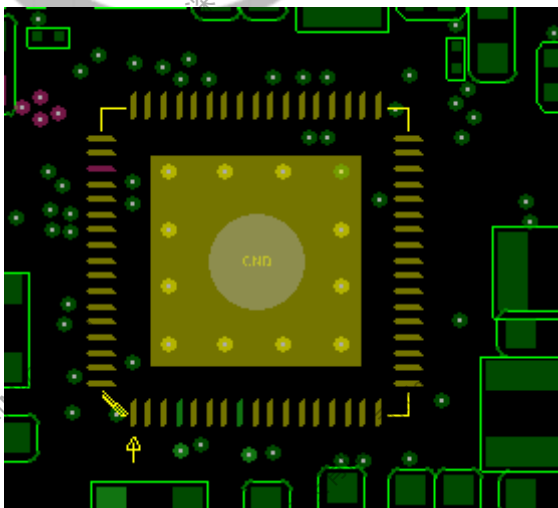
- When mounting the EPAD in single layer mode, to minimize the contact thermal resistance, make sure the pastemask opening area is 50% to 80% of the pad area so that the EPAD can be fully connected to the cooling pad through the solder. To avoid solder balls occur, design the pastemask openings as 3x3 or 2x4 rectangles.

Figure 4-9 Pastemask Openings on the EPAD



- Drill an appropriate number of vias on the cooling pad. The thermal conductivity at the normal direction of the PCB is quite low and it can be significantly improved by adding thermal vias on the cooling pad. However, the improvement reaches the limit when thermal vias reach a certain number and too many vias will consume the trace space. The recommended thermal via design is to keep the via diameter 10–12 mils and the via spacing 30–40 mils.

Figure 4-10 Evenly Drill GND Vias on the Thermal Pad

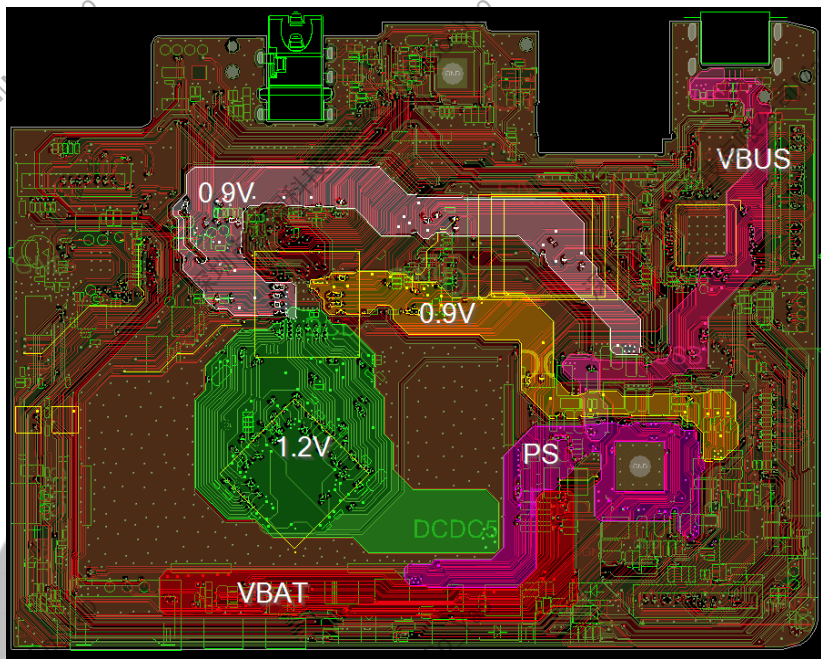


4. Ground the unused pins if it will not affect any features.
5. When drilling vias for the components with a thermal pad, try to drill the vias as close to the center of the components as possible. The die of the component which generates heat is normally at the center of the components.

4.2.3 Traces and Shapes

1. Decide the width of traces and shapes according to the current-carrying capacity in R818 schematic diagram. For the important power supplies, like the 0.9 V, 1.2 V, and 3.3 V DC-DC power supply, and the 4.2 V VBAT power supply, the width of the traces and shapes should meet the over-current protecting requirements, otherwise, the temperature may rise above the acceptable level.

Figure 4-11 Traces and Shapes for the Important Power Supplies



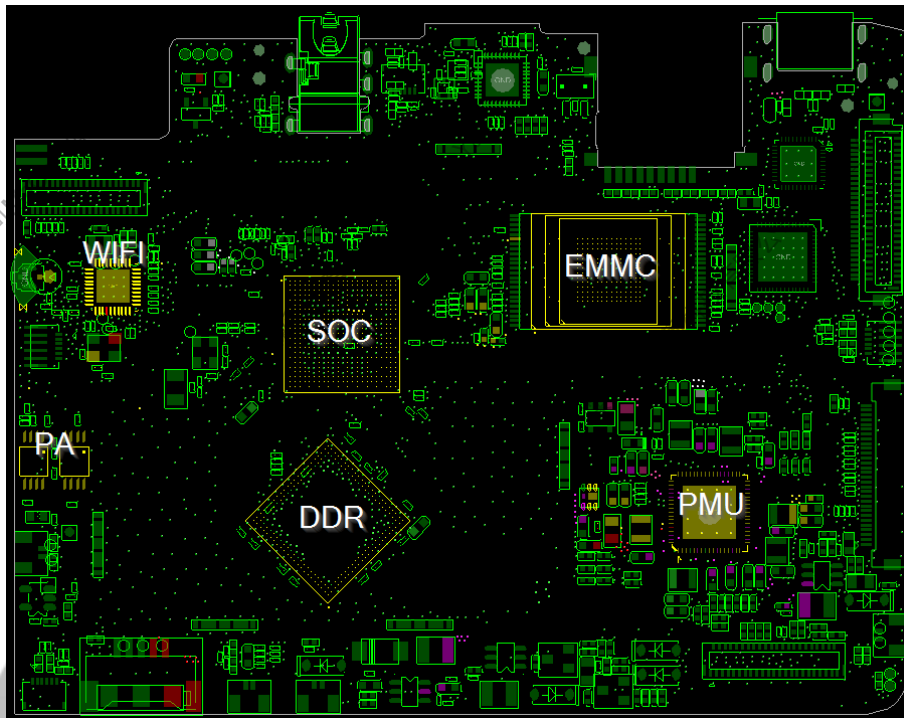
1. Use a large shape to connect the pins because it is beneficial for thermal dissipation and over-current protection. However, during the wave soldering or reflow soldering, remember to take some heat insulation measures like using the thermal relief pad for connection to avoid the void-welding caused by dissipating heat too fast. The SMD pads that smaller than 0402 must be connected by the thermal relief pad and should not be fully connected (the ESD components are exceptions).

Figure 4-12 Processing the Component Pads



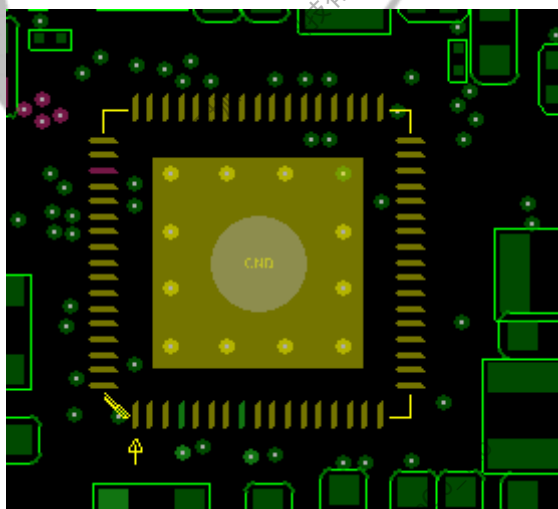
2. Keep the GND and power planes continuous and complete if possible.
3. If space allows, lay a large-area shape on the GND at the bottom layer to facilitate thermal dissipation.
4. Evenly place the components that consume a large amount of power and avoid placing heat sources together. Place the SoC in the center of the board, and keep the PMU at least 2 cm away from the SoC.
5. Keep thermal-sensitive components (like Wi-Fi/BT chips and sensors)at least 1 cm away from components that generate much heat (like the SoC and PMU).

Figure 4-13 Layout for Thermal-Sensitive Components



6. When there are components with EPAD and the thermal pads are through-hole pads, you can add soldermask openings on both sides of the EPAD to facilitate thermal dissipation.

Figure 4-14 Soldermask Openings on Both Sides of the PMU



7. Choose the appropriate substrate and base material. For the substrate, choose a multi-layer metal substrate if possible. For the base material, consider balancing the electrical and thermal performance.

4.3 Thermal dissipation on the System

4.3.1 Ambient Temperature

The following table shows the temperature requirements for R818.

Table 4-1 R818 Temperature Requirements

Items		Values
Storage Temperature		-20°C to 70°C
Operating Temperature	Indoors	-5°C to 55°C
	Outdoors	-10°C to 60°C

4.3.2 Device Temperature

To obtain a good performance, control the junction temperature to be not higher than 90% of the maximum value.

The junction temperature (T_j) is hard to measure. You can measure the case temperature and then calculate the T_j according to the following formula:

$$T_j = T_c + R_{jc} * P_{jc}$$

Where,

T_j is the junction (die) temperature;

T_c is the package case temperature;

R_{jc} is the thermal resistance from the junction to the package case;

P_{jc} is the power consumption of the chip.

4.3.3 System Temperature Rise

The system temperature rise indicates the difference between the average temperature of the air inside the device and the ambient air. For R818, the value should be controlled between 10°C to 15°C. For the heatsink inside the device, the acceptable maximum temperature rise is 45°C.

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