VERSION HISTORY

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Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	20200528			
Ver 1.1	Release version	20200714			
Ver 1.2	Release version	20201203			
Ver 1.3	Release version	20210126			
Ver 1.4	Release version	20210913			
Ver 1.5	Release version	20220209			
Ver 1.6	Release version	20220719			
Ver 1.7	Release version	20220729			

AllWinner Technology Co.,Ltd
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Size: A3 | Page Name: VERSION HISTORY | Rev
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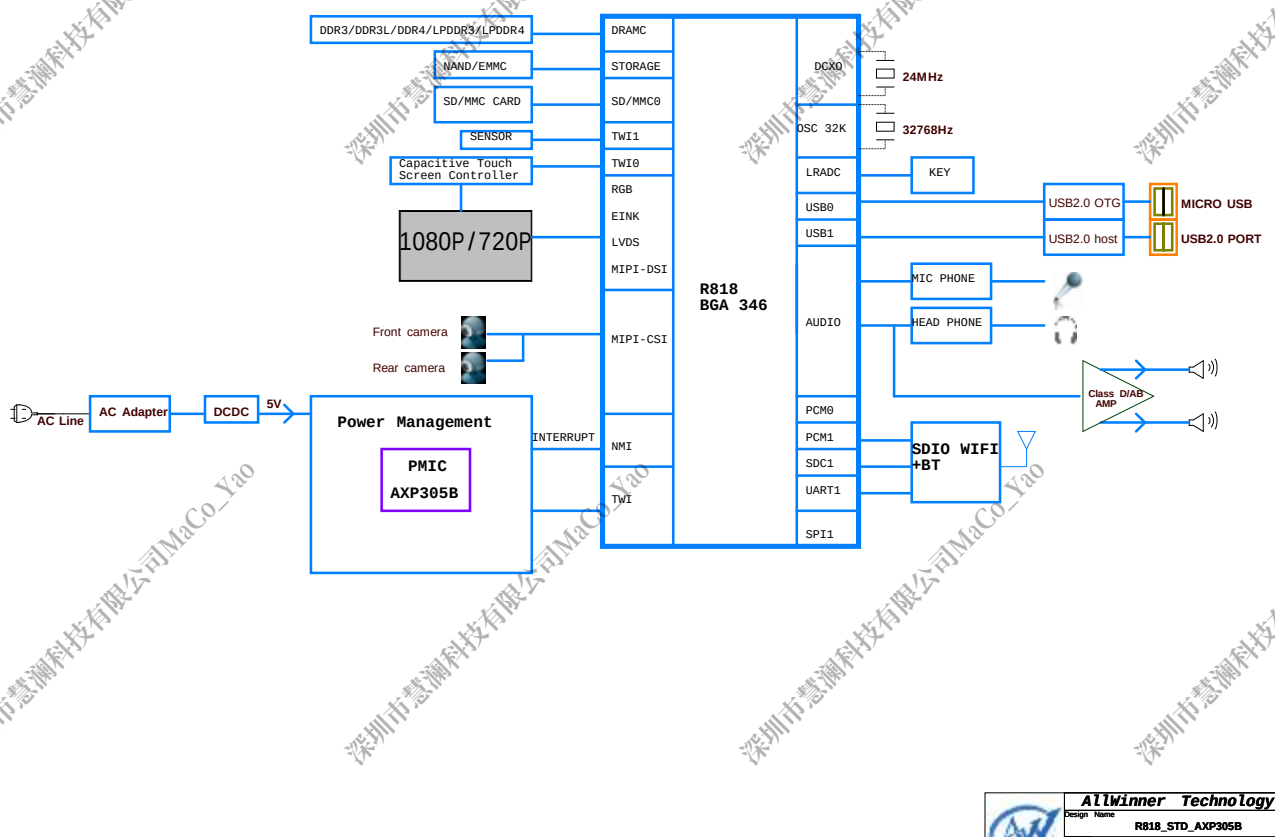
BLOCK



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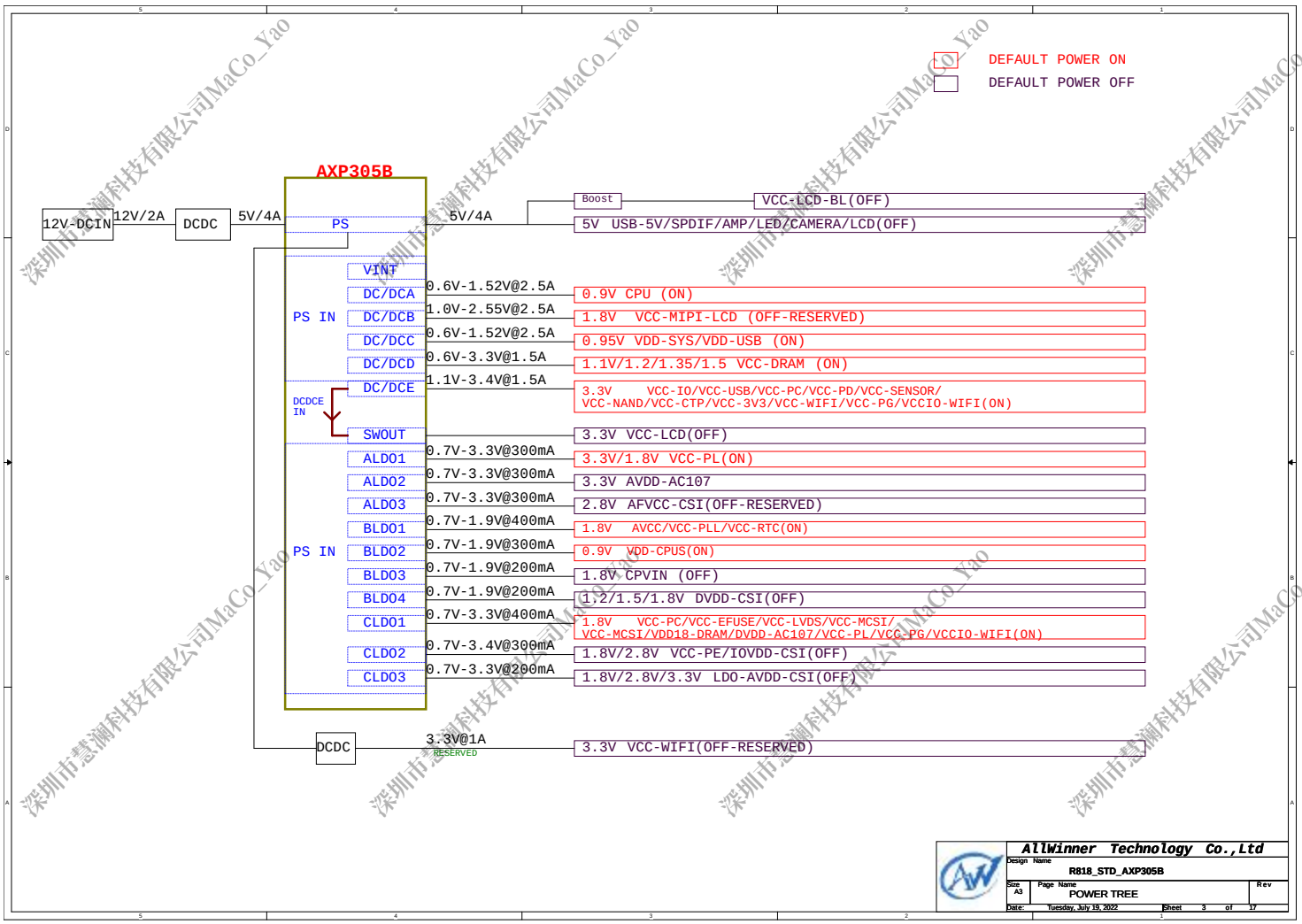

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	UART2-TX	2	UART
PB1	UART2-RX	2	
PB2	CPUX_TDO	2	
PB3	CPUX_TDI	2	
PB4	I2S0_MCLK	3	I2S
PB5	I2S0_BCLK	3	
PB6	I2S0_LRCK	3	
PB7	I2S0_DOUT	3	
PB8	I2S0_DIN	3	
PB9	CPUX_TX	2	DEBUG
PB10	CPUX_RX	2	

PIN	Define	CFG	Function
PE0	MCSI_MCLK0	2	CSI
PE1	MCSI_SCK0	2	
PE2	MCSI_SDA0	2	
PE3	MCSI_SCK1	2	
PE4	MCSI_SDA1	2	
PE5	MCSI_MCLK1	2	
PE6	MCSIB_STBY_F	1	
PE7	MCSIB_RST_F	1	
PE8	MCSIA_STBY_R	1	
PE9	MCSIA_RST_R	1	

PIN	Define	CFG	Function
PH0	TWI0_SCK	2	TWI
PH1	TWI0_SDA	2	
PH2	TWI1_SCK	2	
PH3	TWI1_SDA	2	
PH4	UART3-TX	2	UART
PH5	UART3-RX	2	
PH6	UART3-RTX	2	
PH7	UART3-CTX	2	
PH8	DMIC-CLK	2	DMIC
PH9	DMIC-DATA0	2	
PH10	DMIC-DATA1	2	
PH11	DMIC-DATA2	2	
PH12	DMIC-DATA3/USB0-DRVVBUS	2	
PH13	I2S3-MCLK	4	I2S
PH14	I2S3-BCLK	4	
PH15	I2S3-LRCK	4	
PH16	I2S3-DOUT0	3	
PH17	I2S3-DIN0	4	
PH18	IR-OUT	2	CIR
PH19	LEDC	5	LEDC

PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

PIN	Define	CFG	Function
PF0	USB0-ID	0	GPIO
PF1	CTP-RST	1	
PF2	PA-CTR	1	
PF3	GS-INT	6	
PF4	USB1-DRVVBUS	1	
PF5	LS-INT	6	
PF6	CTP-INT	6	

PIN	Define	CFG	Function
PL0	PMU_SCK	2	CPUS
PL1	PMU_SDA	2	
PL2	BT_RST_N	1	
PL3	BT_WAKE_AP	0	
PL4	AP_WAKE_BT	1	
PL5	WL_PMU_EN	1	
PL6	WL_WAKE_AP	0	
PL7	LCD-BL-EN	1	
PL8	S_TWI_SCK	2	
PL9	S_TWI_SDA	2	
PL10	S_PWM	2	
PL11	IR_IN	3	

PIN	Define	CFG	Function
PD0	LCD_D2	2	LCD
PD1	LCD_D3	2	
PD2	LCD_D4	2	
PD3	LCD_D5	2	
PD4	LCD_D6	2	
PD5	LCD_D7	2	
PD6	LCD_D10	2	
PD7	LCD_D11	2	
PD8	LCD_D12	2	
PD9	LCD_D13	2	
PD10	LCD_D14	2	
PD11	LCD_D15	2	
PD12	LCD_D18	2	
PD13	LCD_D19	2	
PD14	LCD_D20	2	
PD15	LCD_D21	2	
PD16	LCD_D22	2	
PD17	LCD_D23	2	
PD18	LCD_CLK	2	
PD19	LCD_DE	2	
PD20	LCD_HSYNC	2	
PD21	LCD_VSYNC	2	
PD22	LCD_RST	1	
PD23	LCD_PWM	3	

PIN	Define	CFG	Function
PG0	WL_SDIO_CLK	2	WIFI/BT
PG1	WL_SDIO_CMD	2	
PG2	WL_SDIO_D0	2	
PG3	WL_SDIO_D1	2	
PG4	WL_SDIO_D2	2	
PG5	WL_SDIO_D3	2	
PG6	BT_UART_RX	2	
PG7	BT_UART_TX	2	
PG8	BT_UART_CTS	2	
PG9	BT_UART_RTS	2	
PG10	BT_PCM_CLK	3	
PG11	BT_PCM_SYNC	3	
PG12	BT_PCM_DIN	3	
PG13	BT_PCM_DOUT	3	

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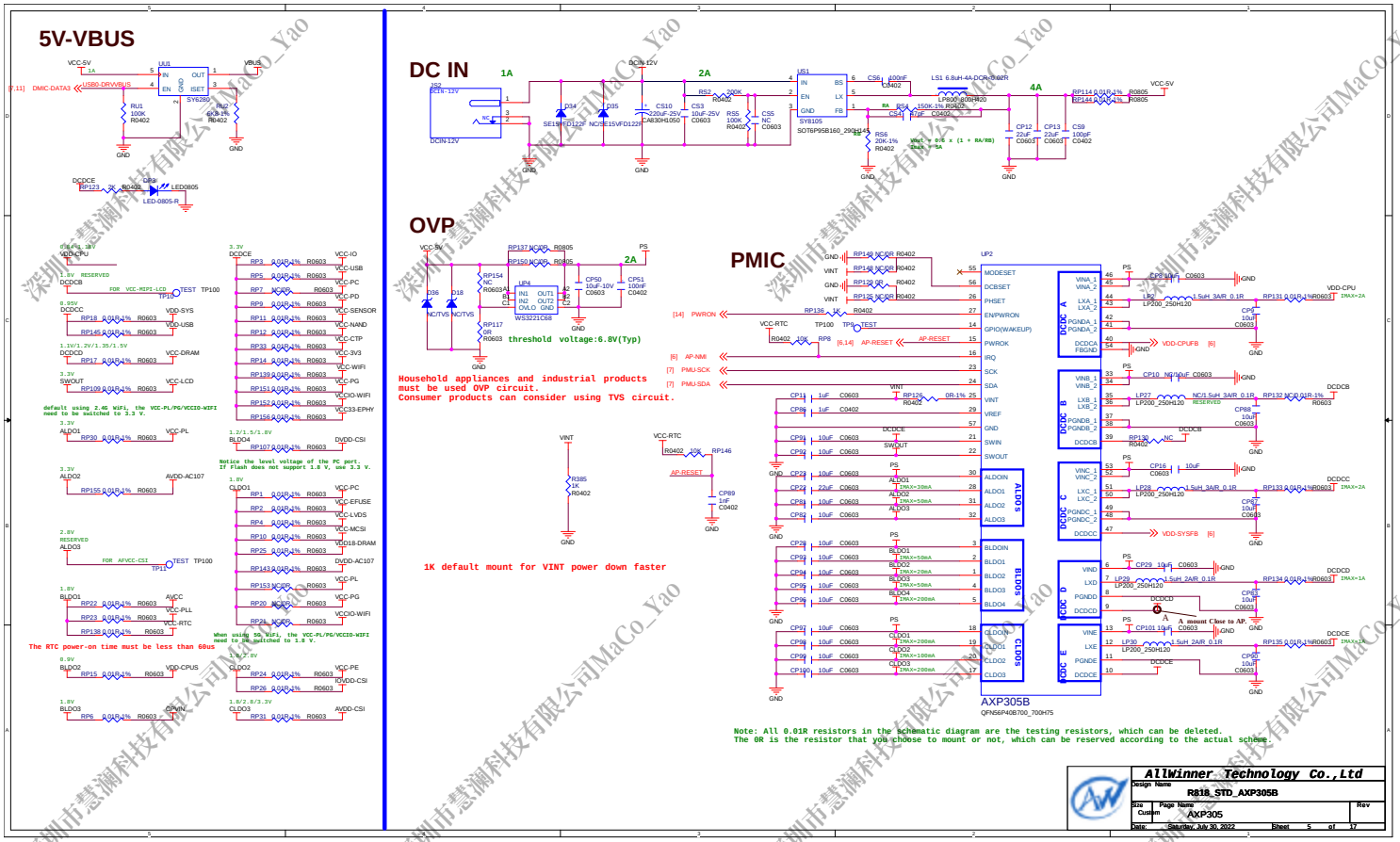
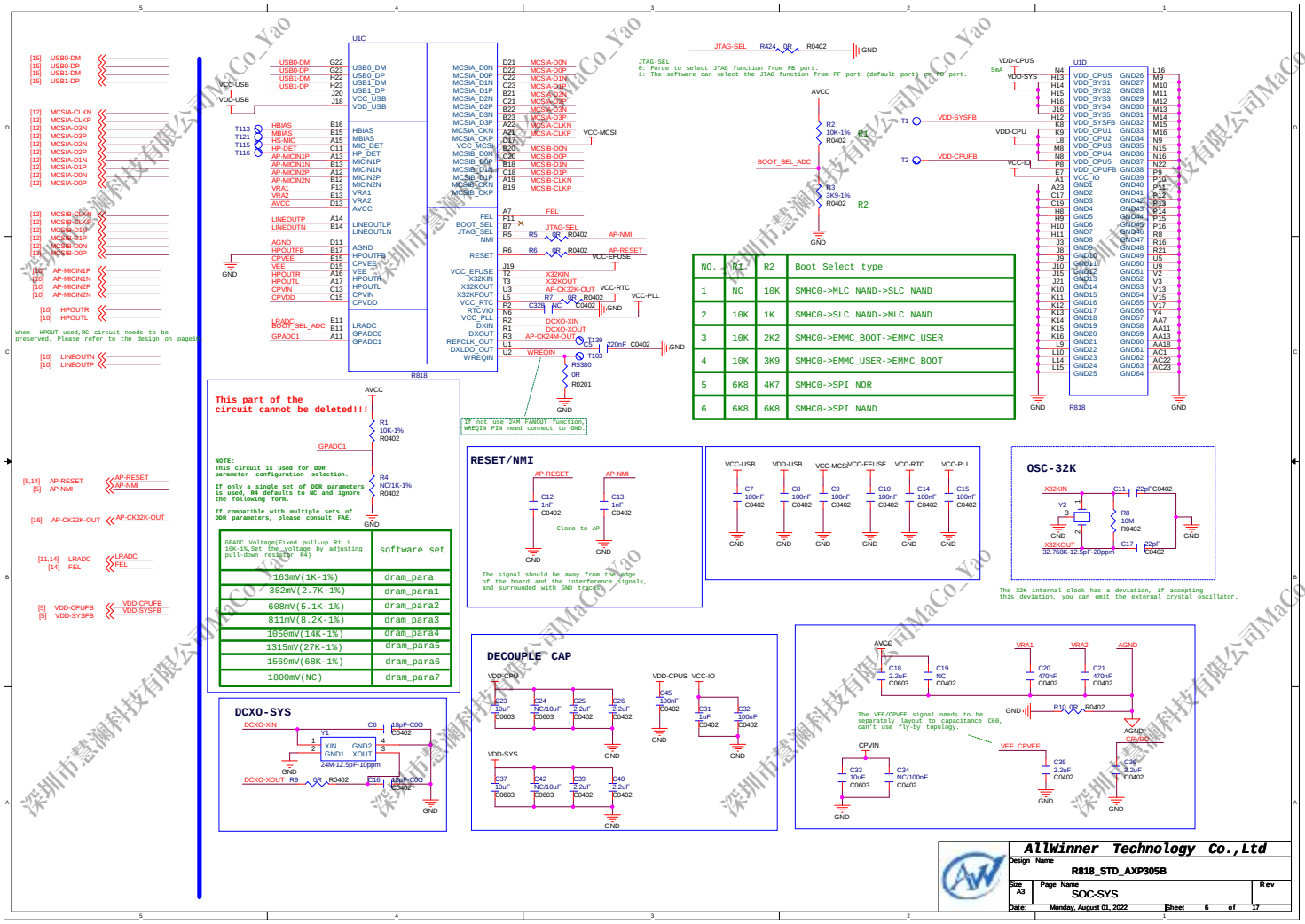
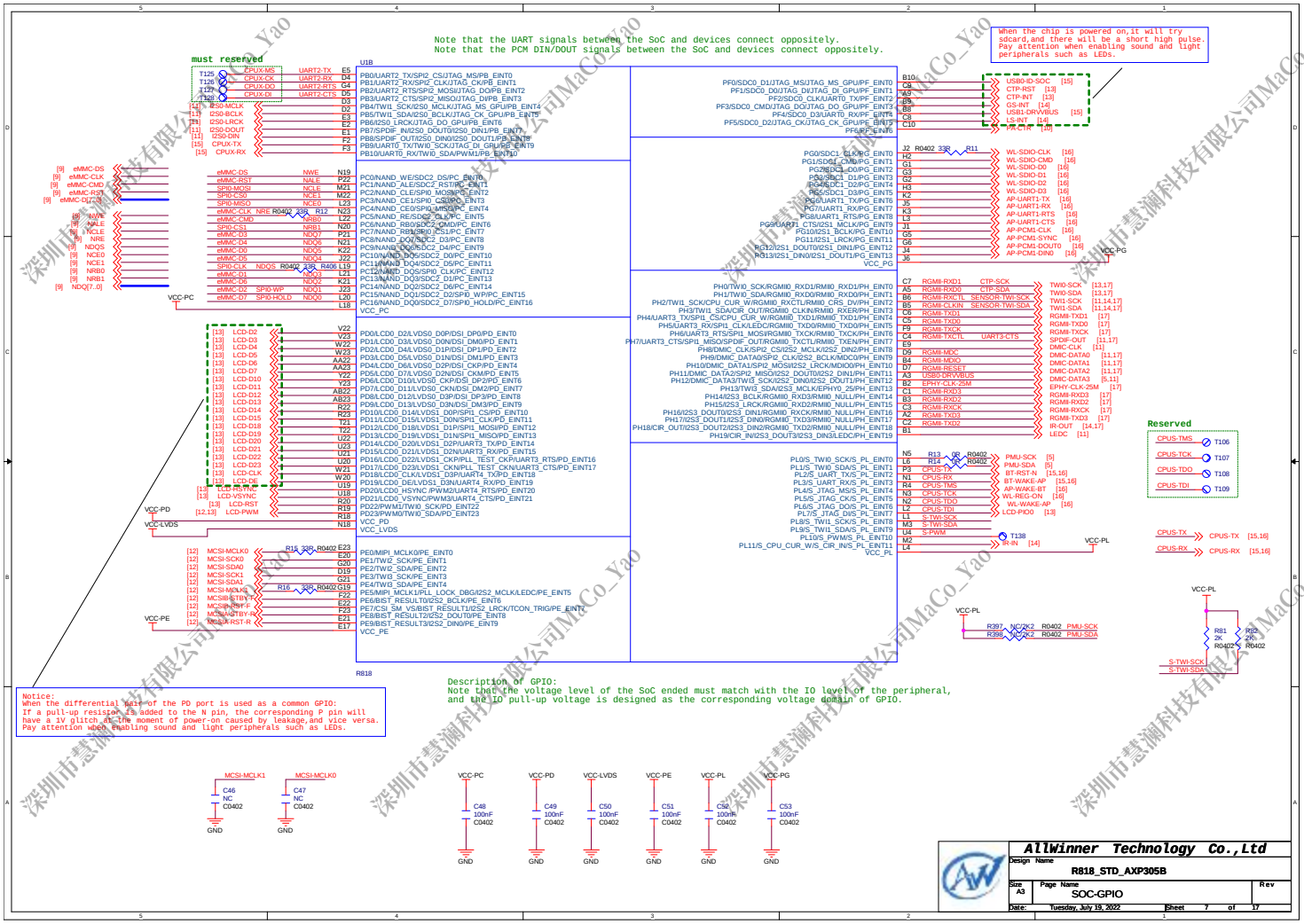
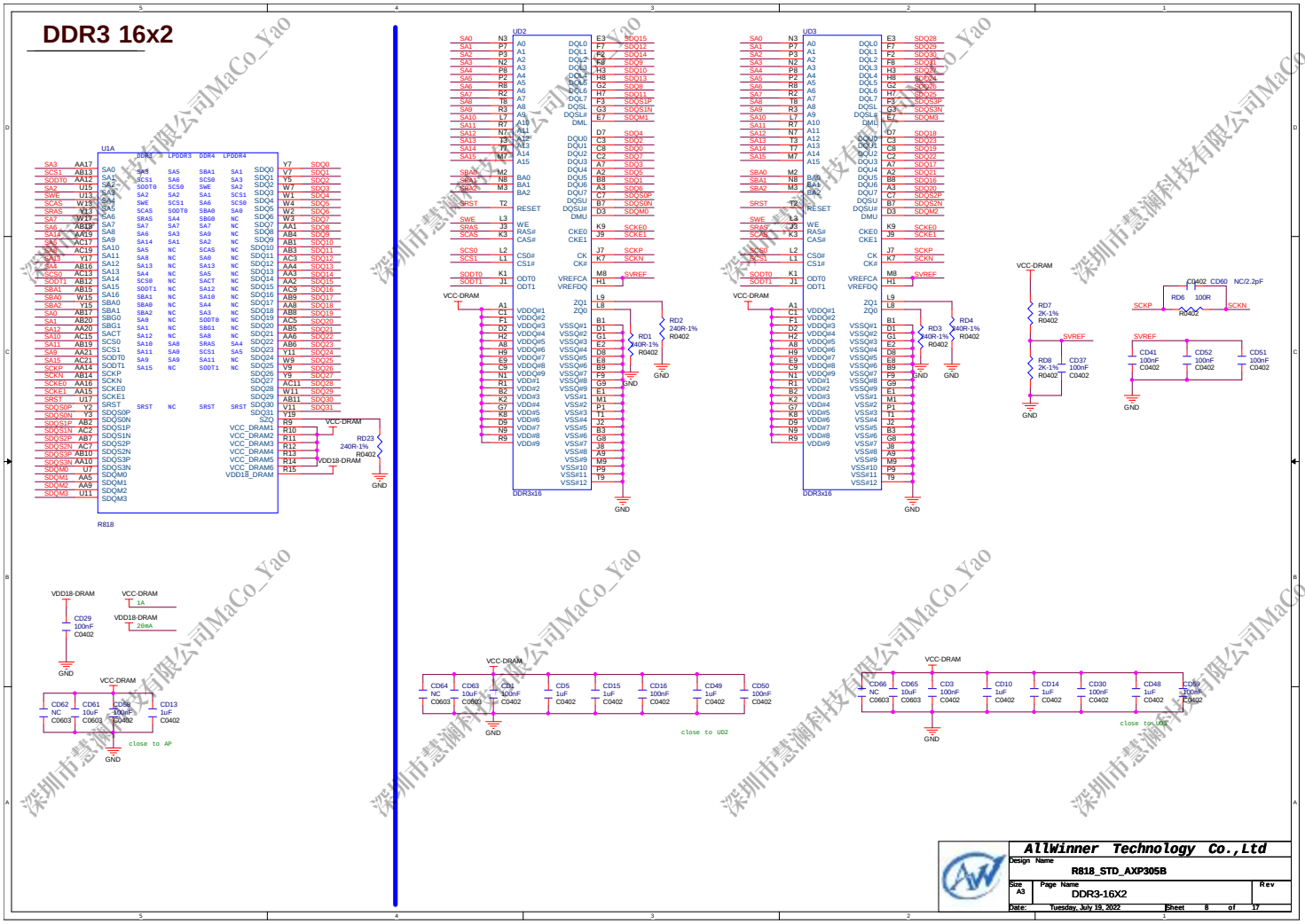




NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND
2	10K	1K	SMHC0->SLC NAND->MLC NAND
3	10K	2K2	SMHC0->EMMC_BOOT->EMMC_USER
4	10K	3K9	SMHC0->EMMC_USER->EMMC_BOOT
5	6K8	4K7	SMHC0->SPI NOR
6	6K8	6K8	SMHC0->SPI NAND


must reserved
Note that the UART signals between the SoC and devices connect oppositely.
Note that the PCM DIN/DOUT signals between the SoC and devices connect oppositely.
When the chip is powered on,it will try sdcard,and there will be a short high pulse. Pay attention when enabling sound and light peripherals such as LEDs.
U1B
Reserved
Notice:
When the differential bit of the PD port is used as a common GPIO:
If a pull-up resistor is added to the N pin, the corresponding P pin will have a 1V glitch at the moment of power-on caused by leakage,and vice versa. Pay attention when enabling sound and light peripherals such as LEDs.
Description of GPIO:
Note that the voltage level of the SoC ended must match with the IO level of the peripheral, and the IO pull-up voltage is designed as the corresponding voltage domain of GPIO.
AllWinner Technology Co.,Ltd
R818_STD_AXP305B
SOC-GPIO
Tuesday, July 19, 2022

DDR3 16x2



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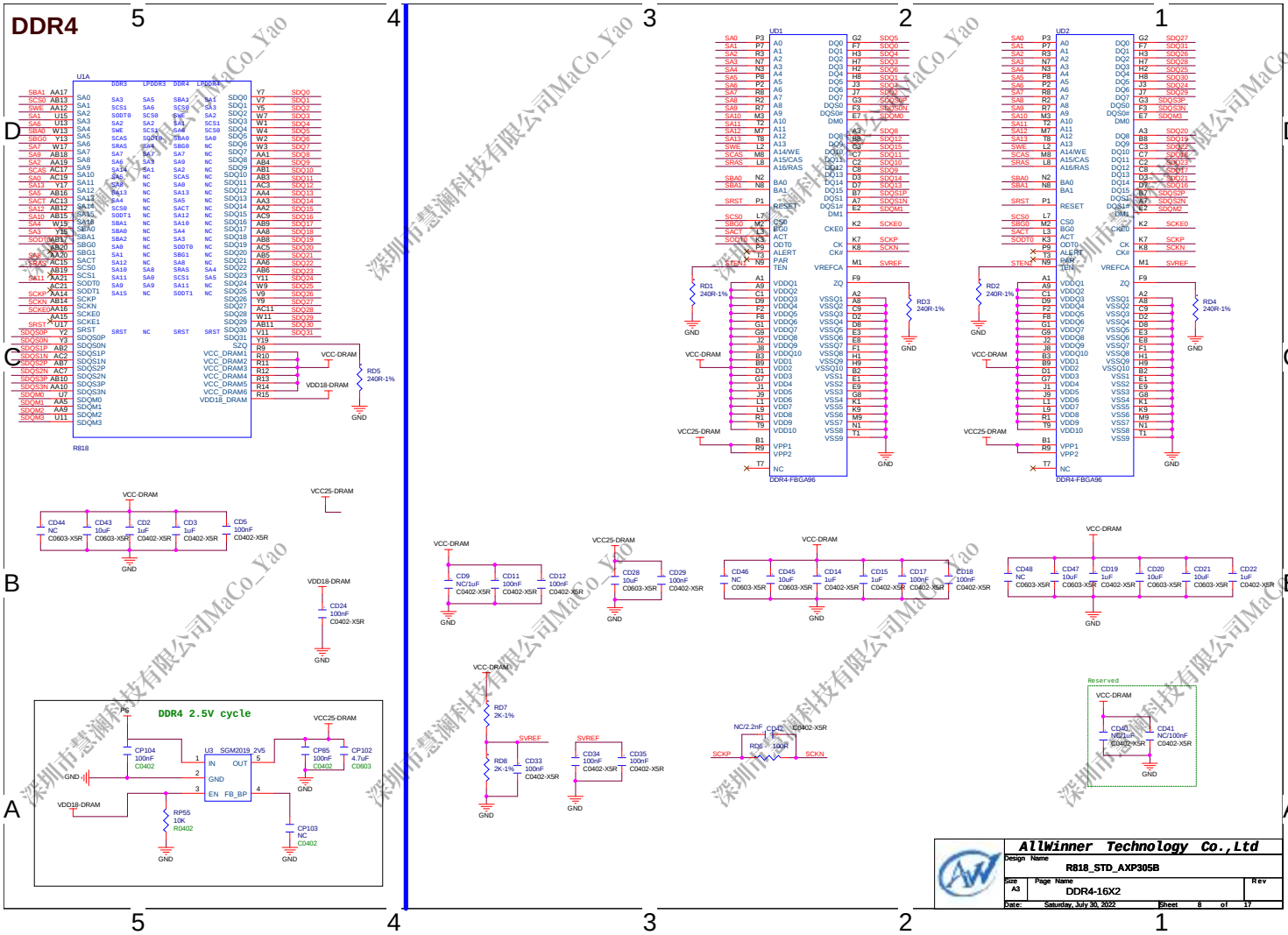

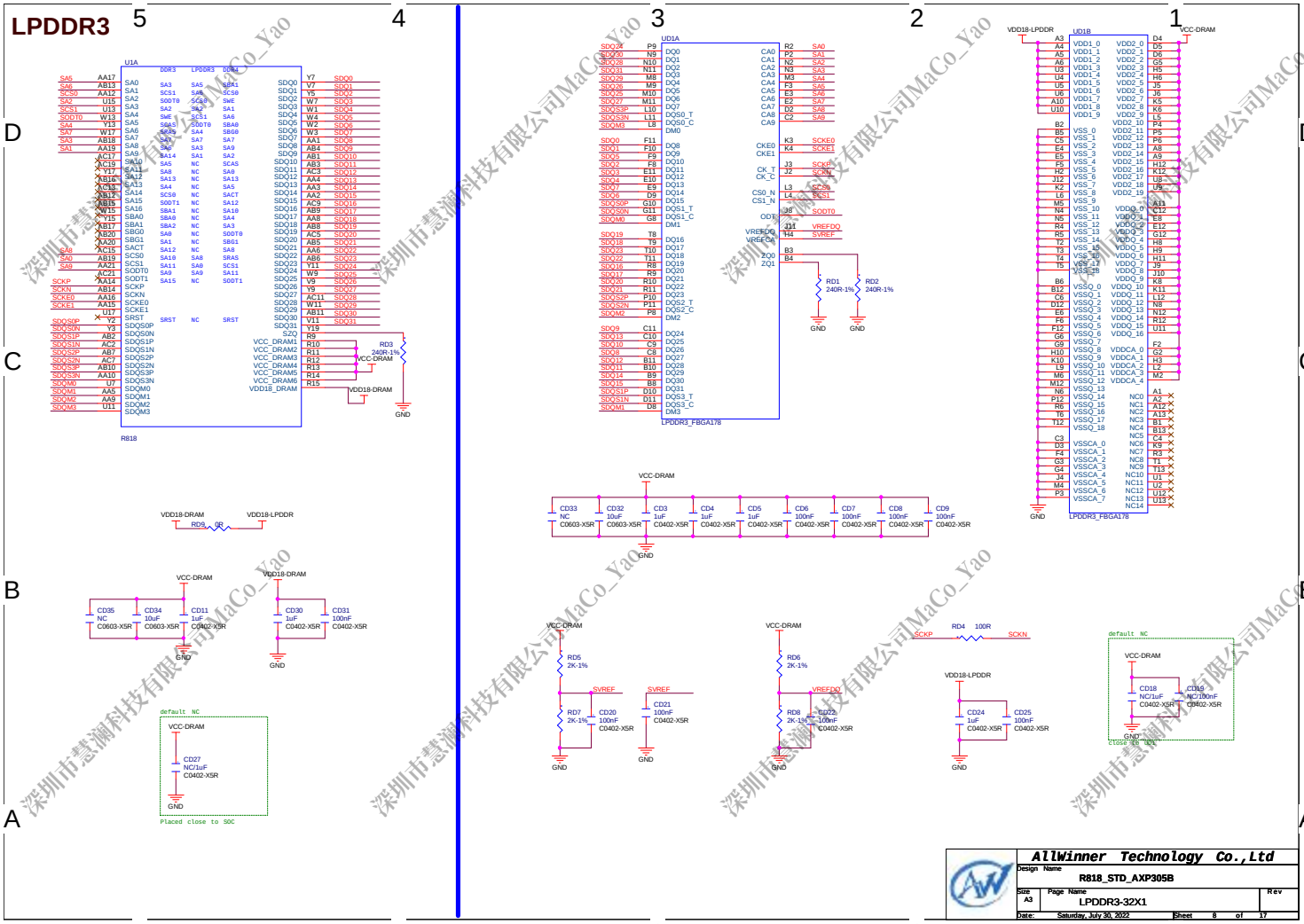
LPDDR3
U1A
R818
UD1A
LPDDR3_FBGA178
UD1B
LPDDR3_FBGA178
RD1 240R-1%
RD2 240R-1%
RD3 240R-1%
RD4 100R
RD5 2K-1%
RD6 2K-1%
RD7 2K-1%
RD8 2K-1%
RD9 0R
VCC-DRAM
VDD18-DRAM
VDD18-LPDDR
GND
SVREF
VREFDQ
SCKP
SCKN
default NC
Placed close to SOC
close to U01
AllWinner Technology Co.,Ltd
R818_STD_AXP305B
LPDDR3-32X1
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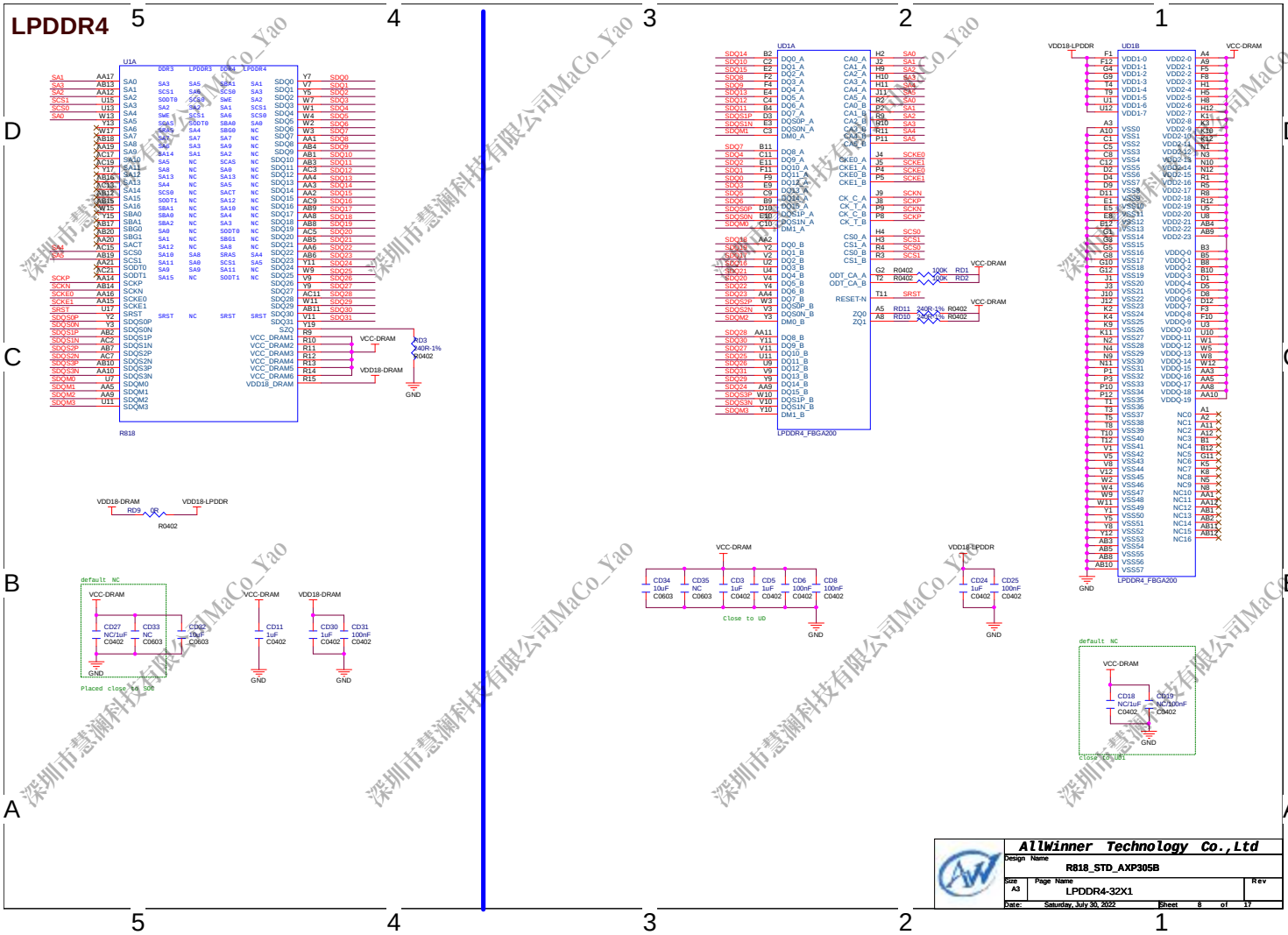
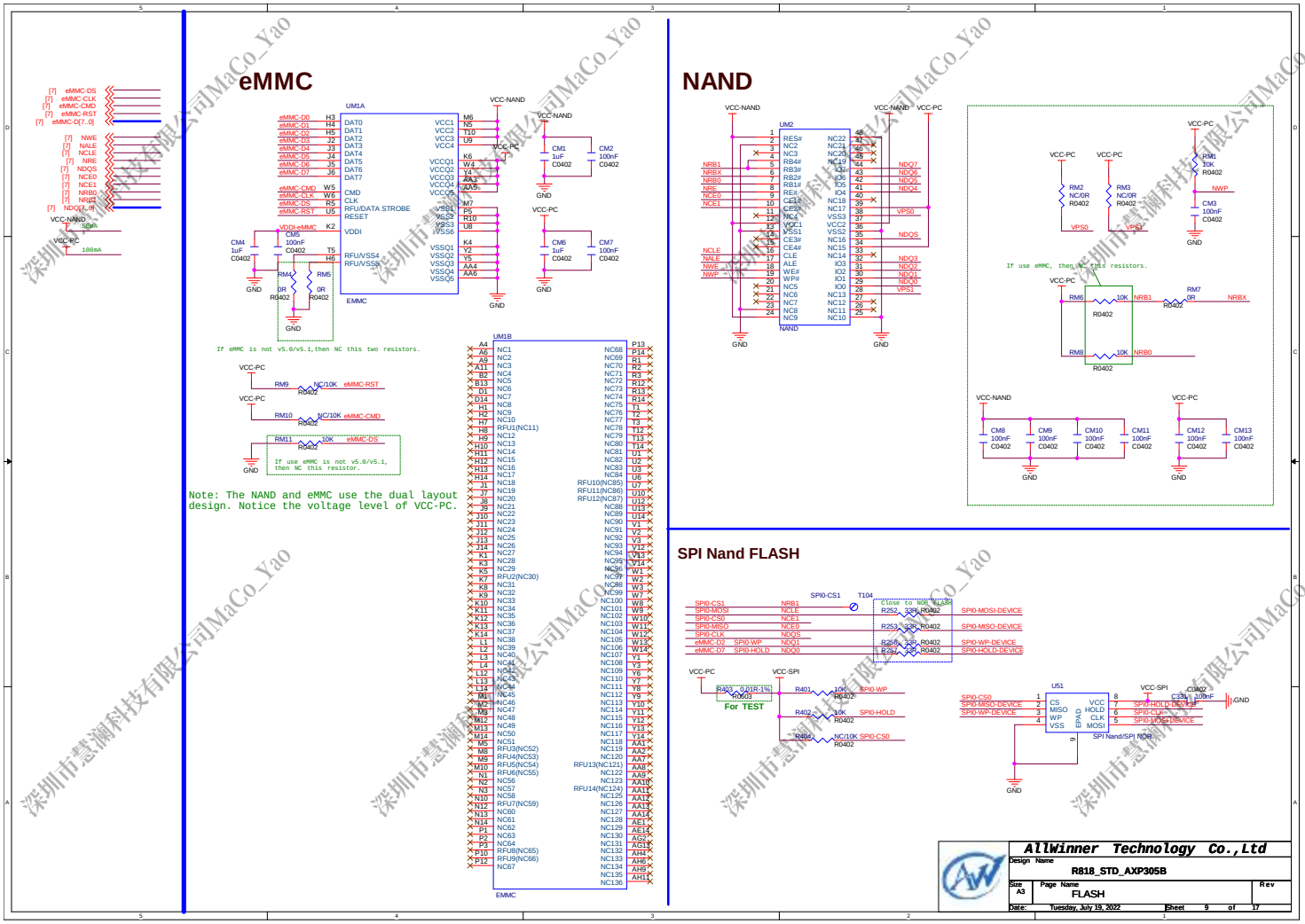
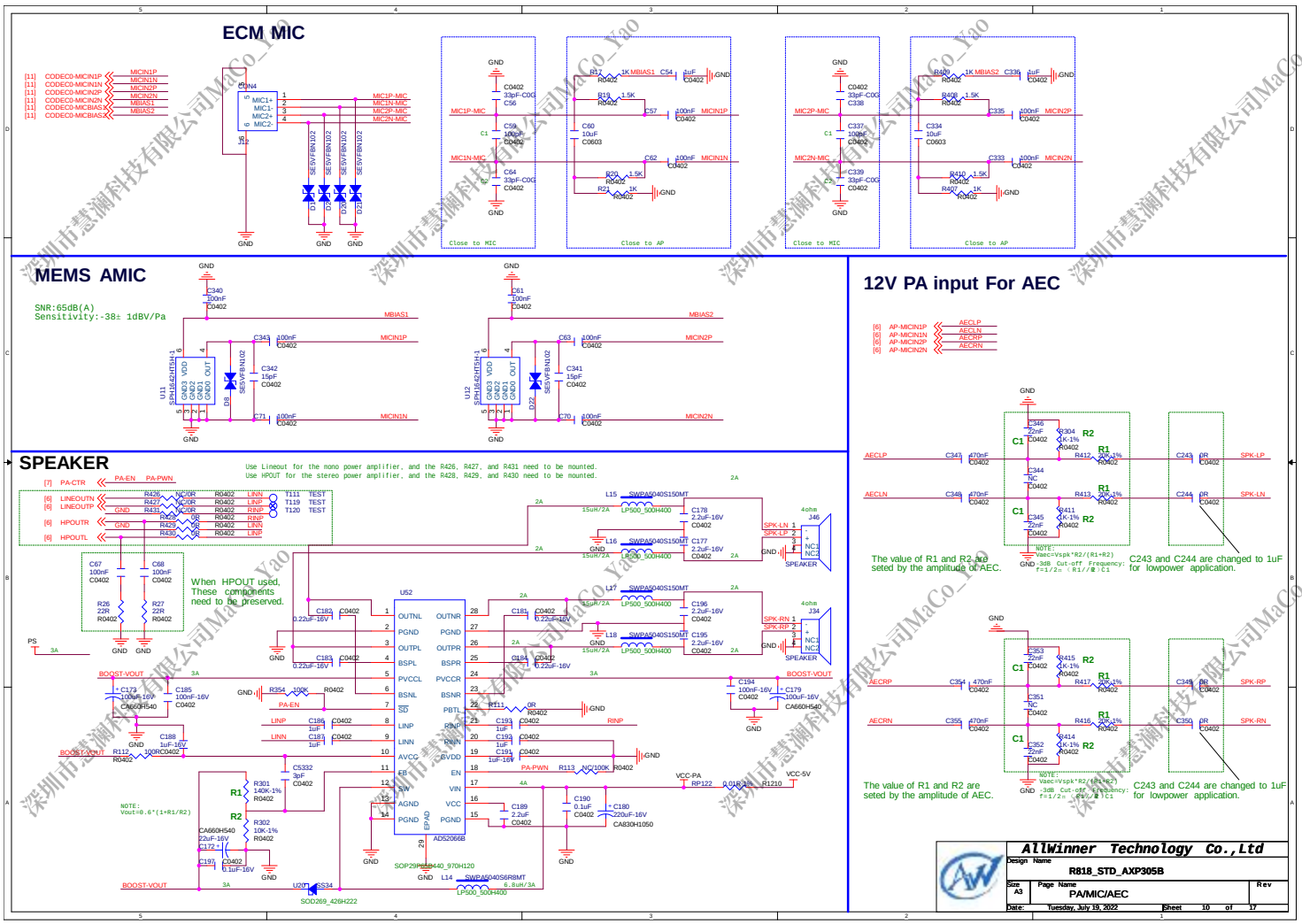
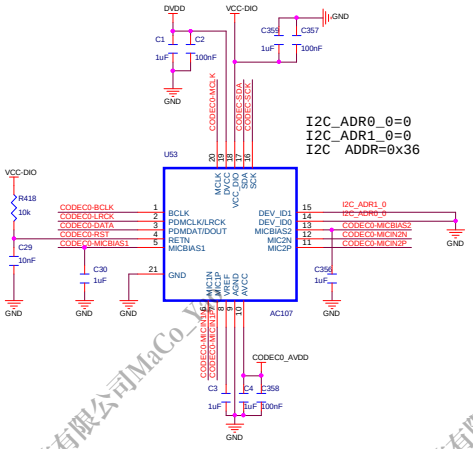




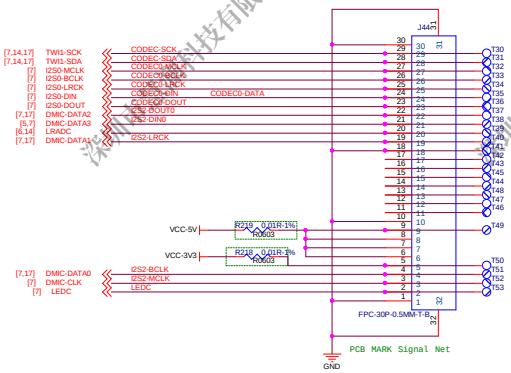


AUDIO2

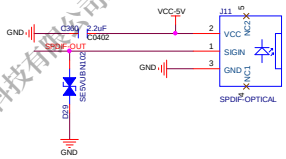
AEC



MIC ARRAY



SPDIF



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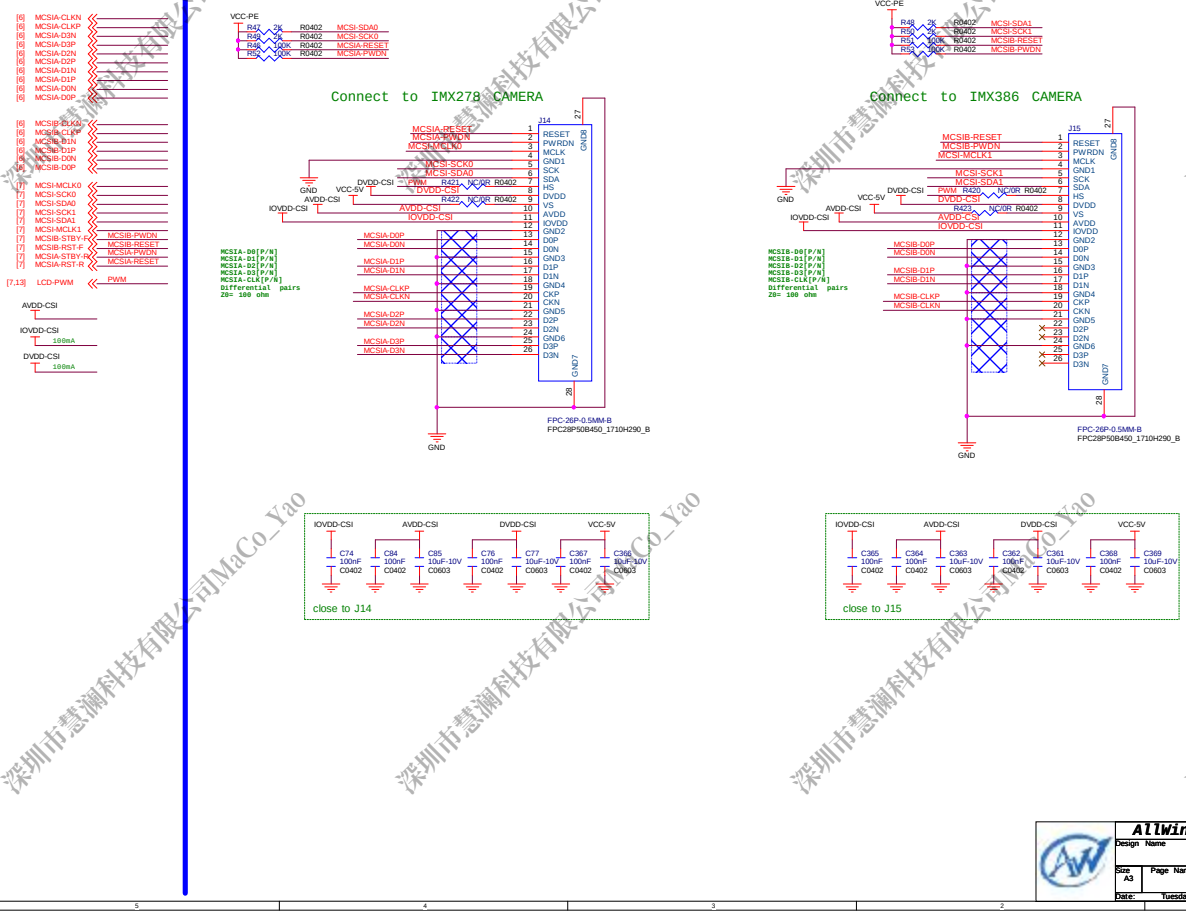
MIPI-CSI



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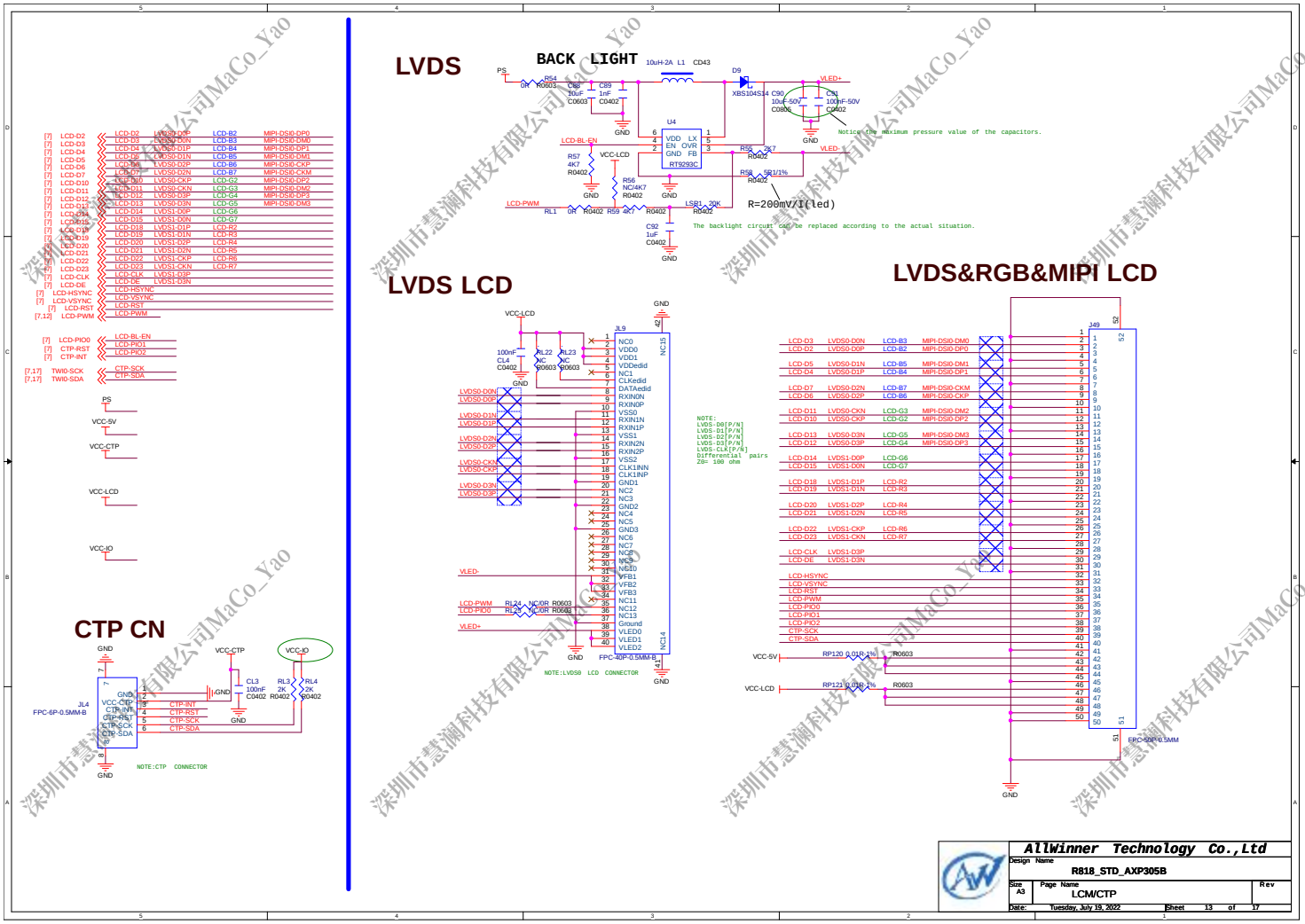
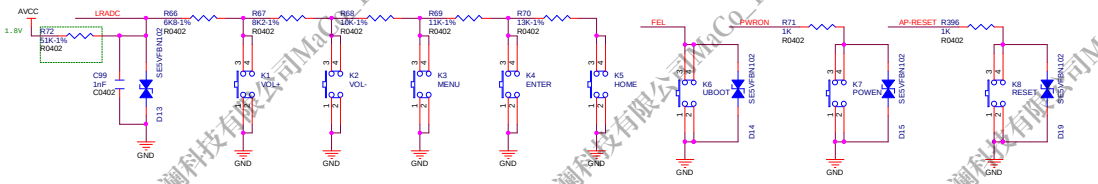
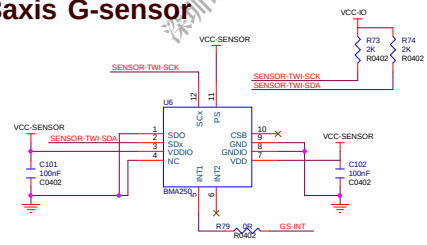


KEY

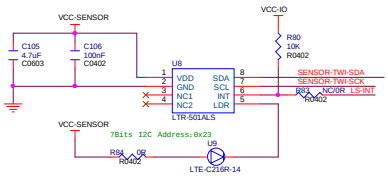


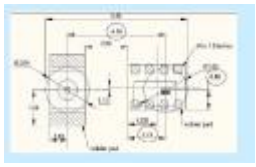
3axis G-sensor



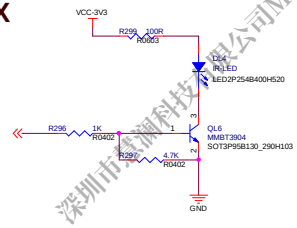
7Bits I2C Address:0x18
place PIN1 in the top right,parallel to the screen,
and put on the top left of the screen.

LIGHT SENSOR

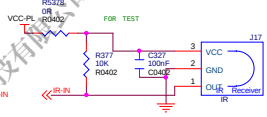




IR-TX



IR-RX



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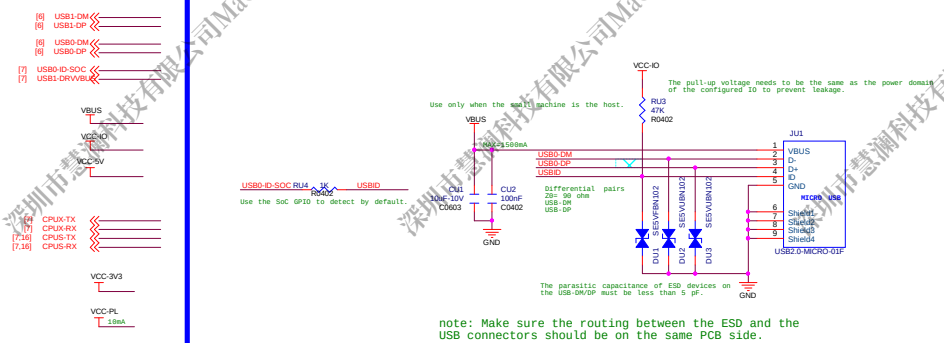
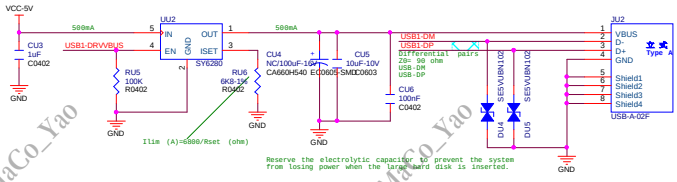
USB

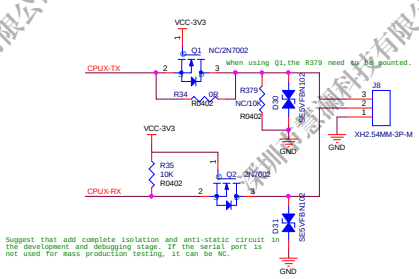


note: Make sure the routing between the ESD and the USB connectors should be on the same PCB side.

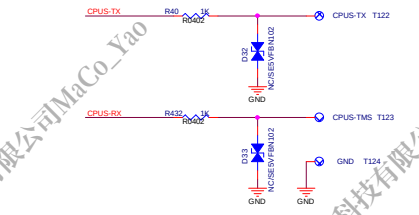
portAUSB



CPUX DEBUG



CPUS DEBUG



The UART of the CPUS domain needs to be connected to resistors in series or added ESD for anti-static design.

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