# R818 Hardware Design Guide

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# About This Document

## Purpose

This document introduces the key rules of schematic design for R818 chip, which can guide customers to design, help customers shorten the product mass production cycle, improve the reliability of product design, reduce the design cost of the product, and ensure the design quality.

## Related Chip Type

The chip type related to this document：**R818**

## Intended Audience

The document is intended for：

- Hardware development engineers
- Technical support engineers
- Product testing engineers
- PCB layout engineers

## Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

| Version | Change History | Date | Author | Note |
|---|---|---|---|---|
| Ver 1.0 | Initial Version | 2020-03-10 | | |

# Contents

# Figures

# Tables

# 1. R818 Overview

## 1.1. R818 Solution Introduction

R818 is a new generation of high-performance low-cost solution launched by Allwinner for the smart speaker market. It adopts 4-core 64-bit A53 CPU and PowerVR GE8300 GPU.

R818 integrates the new-generation DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 DRAM controller and 13M Camera ISP. R818 supports 4k@30Hz video decoding and rich LCD interfaces such as MIPI, RGB, LVDS. With the improvement of technology, R818 has lower power consumption and higher performance. The new Android Q system provides a better product experience for the next generation of smart speakers.

Figure 1-1 shows the block diagram of R818.

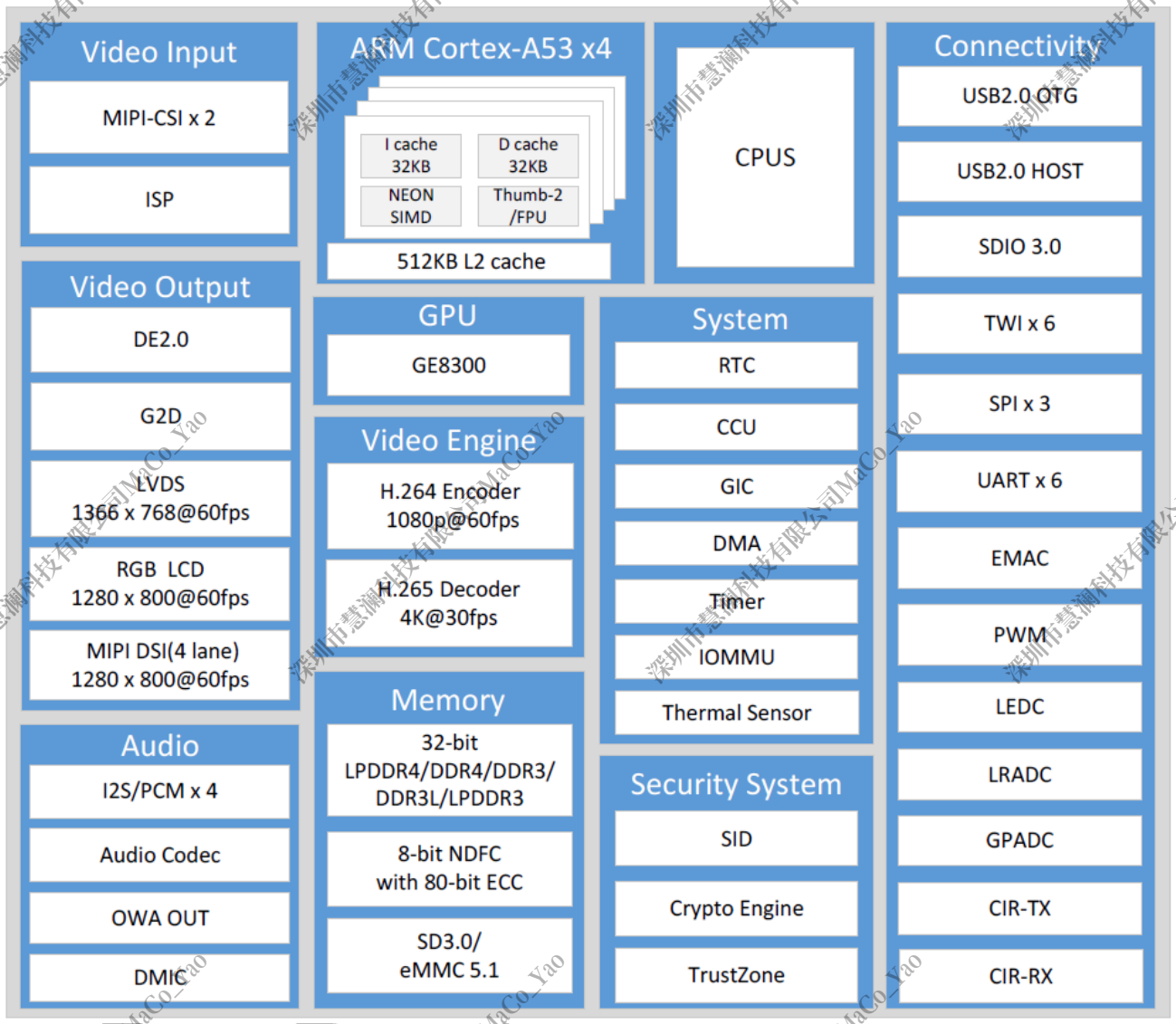



Figure 1-1 R818 System Block Diagram

## 1.2. Application Diagram

Figure 1-2 shows the typical application diagram of R818.

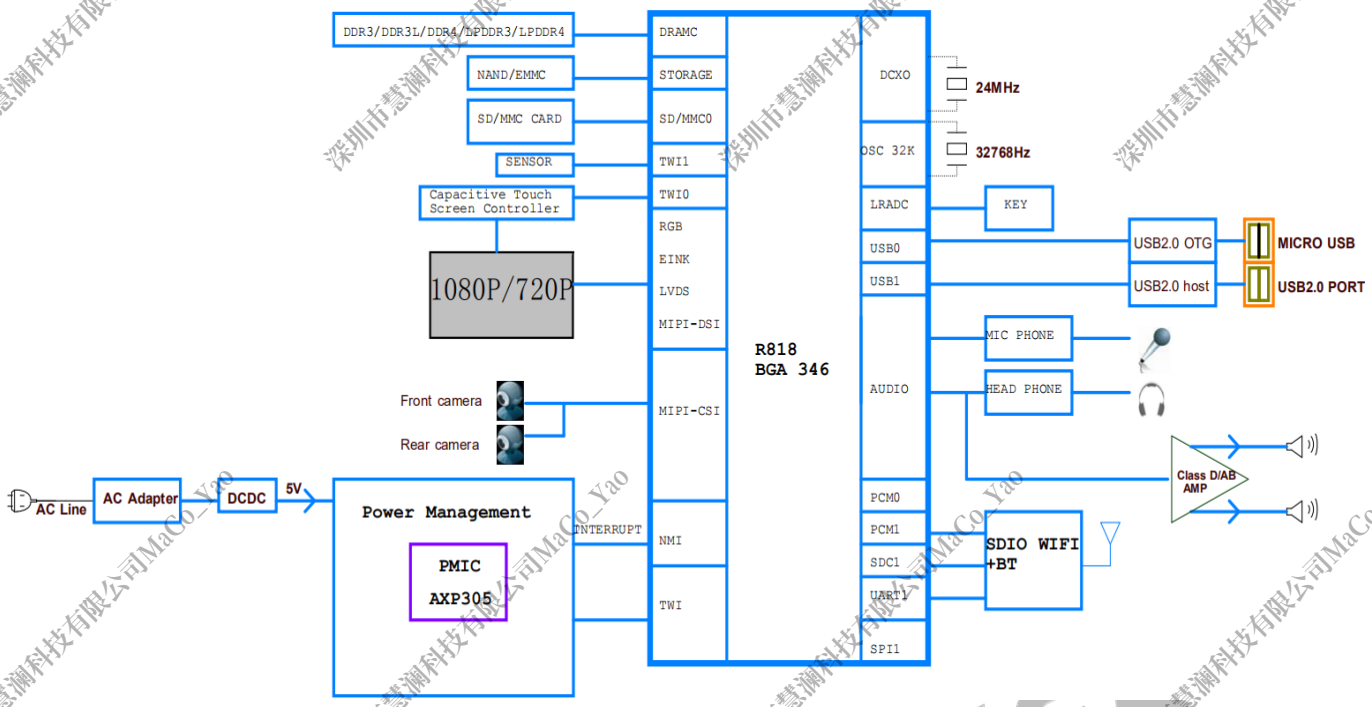



Figure 1-2 R818 Application Diagram

# 2. Schematic Design

## 2.1. Power System Design

### 2.1.1. Introducing R818 Power System Architecture

The R818 platform comes with a companion power management chip: AXP305.
AXP305 can provide 5 channels of adjustable output step-down DCDC, 10 channels of adjustable output LDO, a Switch, which meet the usage of R818 solution.

### 2.1.2. R818 Power-on Sequence

The power-on sequence of R818 is as follows.

- **Step1** The VCC-RTC, AVCC&VCC-PLL, VCC-PL must be powered-on in step 1 to ensure PMU communication.
- **Step2** The VDD-CPU, VCC-DRAM, VDD-CPUS, VDD-SYS, VDD18_DRAM, VDD18_LPDDR, VCC_PC, VCC_PD, VCC_PG, VCC_USB, VCC_IO, VCC_EFUSE, VPP-DRAM must be powered-on in step 2. Note that VPP-DRAM (2.5 V, provided for DDR4) needs to connect to the external LDO.
- During the entire power-on sequence, the Reset signal must always be low level, and the Reset signal can be pulled high until all power supplies are stable.
- The 24M crystal starts oscillation after the reset signal releases.

Figure 2-1 shows the power-on sequence of R818.

CAUTION

The power-on sequence of some peripheral IO power is limited by the load time of the driver, such as VCC-PG/VCC-PE, the SoC design requires that these powers start to power on later than the T2 and are not within the SoC power-on sequence limit.

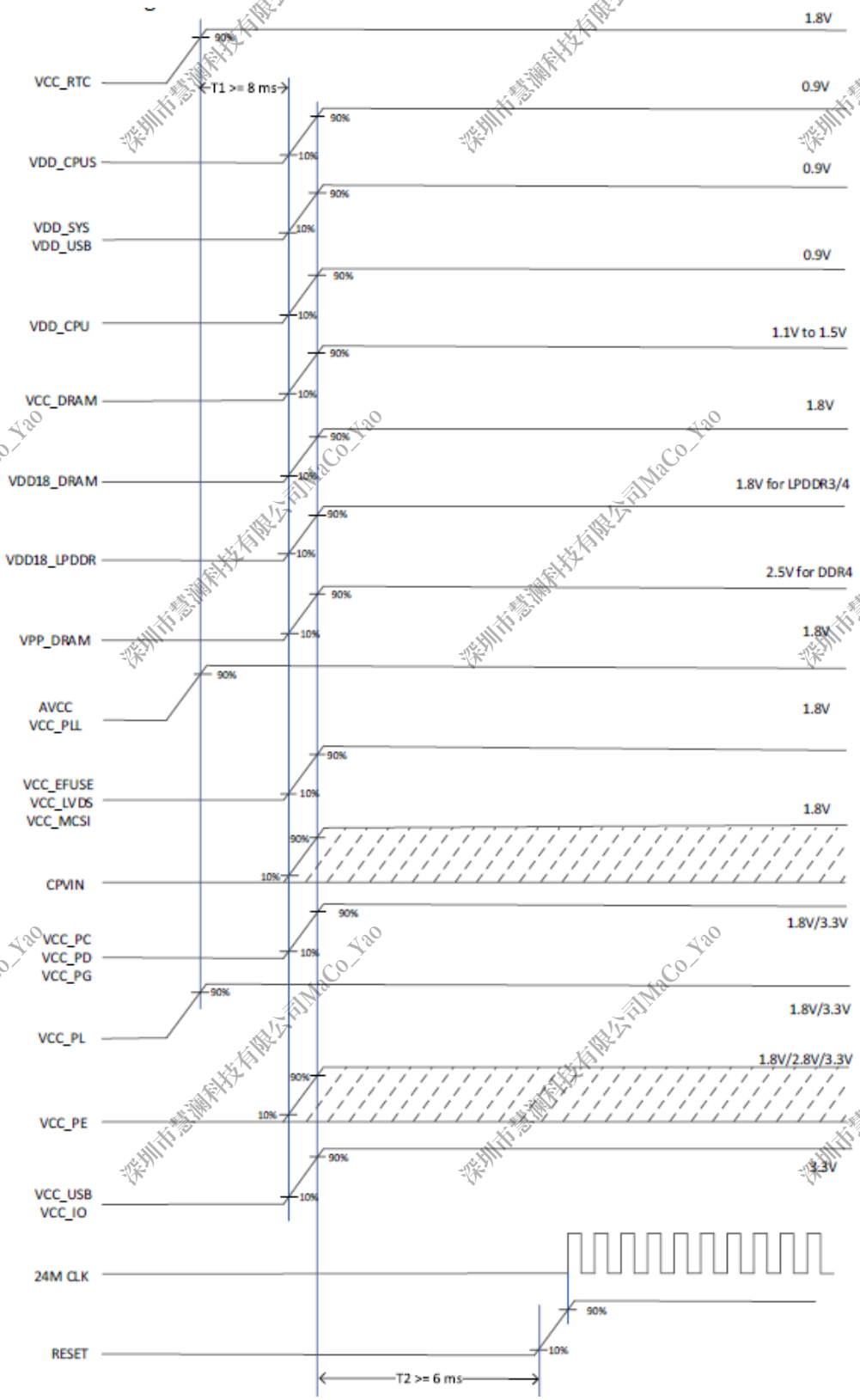



Figure 2-1 R818 Power-on Sequence

## 2.1.3. R818 Power-off Sequence

The power-off sequence of R818 is as follows.

- VCC-RTC holds high.
- After PMU receives the power-off demand, pulls down the Reset signal, and delays T1.
- VDD-SYS is not powered-off earlier than other circuits.

Figure 2-2 shows the power-off sequence of R818.

CAUTION

The power-off sequence only applies to the software shutdown process, does not apply to the forced hardware shutdown process by long-pressing the power button for 6 s or unplugging the battery.

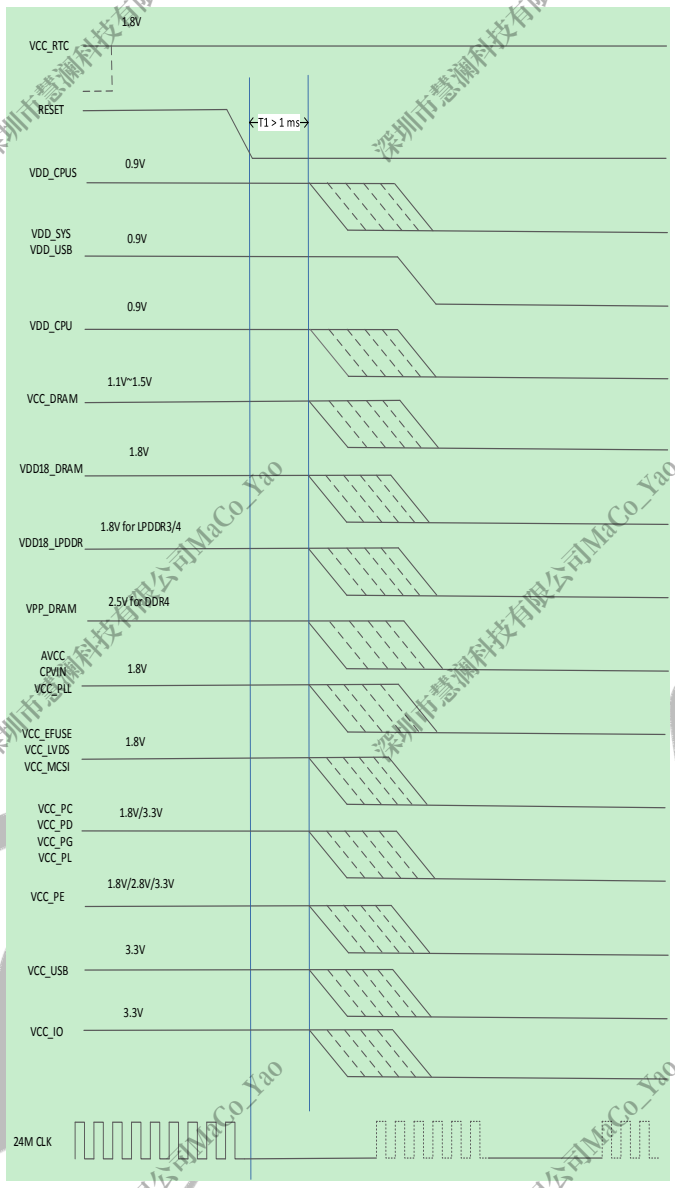



Figure 2-2 R818 Power-off Sequence

## 2.1.4. R818 POWER TREE

The design requirement of the R818 power tree is as follows.

- The power supply with the red mark needs to be turned on by default and has a fixed power-on sequence requirement, which is determined by the internal burning of the PMU. Therefore, this part of the power supply must be the same as the standard case and cannot be changed.
- The R818 platform optimizes power consumption for typical speaker scenarios. It is recommended that the POWER TREE should be designed by following the default power distribution of the standard case, to avoid the increase in power consumption of some product scenarios and software adaptation workload due to power changes.
- For the module power supplied by the same power domain, it has been verified and tested, and cannot be changed and matched casually to avoid system instability, such as AVCC/VCC-PLL.

Figure 2-3 shows the POWER TREE reference design of R818 plus AXP305.

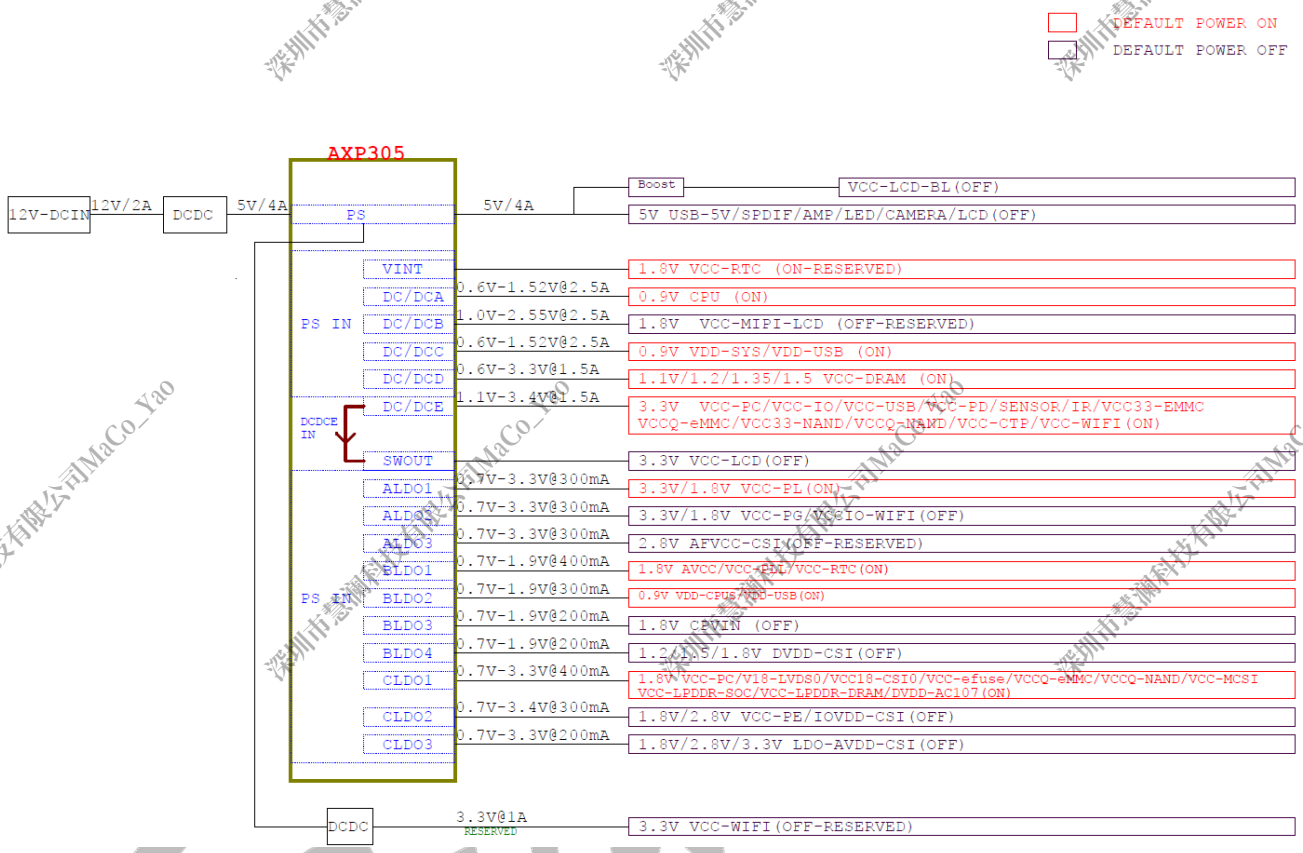



Figure 2-3 R818+AXP305 POWER TREE

## 2.1.5. PMIC AXP305 Circuit Design

- Do not modify the power supply circuits of the SoC functional module, and design by strictly following the standard case.
- The inductor reference value of DCDCA/DCDCB/DCDCC/DCDCD/DCDCE: the inductance is 1.5 uH, the maximum current of this path cannot exceed 80% of the inductor saturation current, and the DC resistance is less than 100 mΩ.
- DCDCD supplies power to DDR by default. The default output voltage of PMU downloading is 1.1 V. After the system starts up, the software automatically adjusts the output voltage of DCDCD according to DRAM configuration parameters: 1.1 V/1.2 V/1.35 V/1.5 V.
- The input and output filter capacitors of each DCDC and LDO that are not used by the PMU can be deleted in the actual solution application, but the input power supply must be maintained, such as DCDCB shown in Figure 2-4.

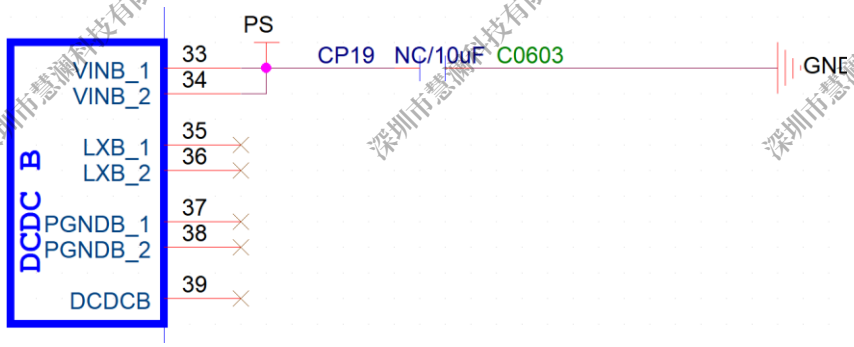



Figure 2-4 AXP305 DCDCB

- VCC-PC has two voltages of 1.8 V and 3.3 V. The design needs to configure the voltage by following the specifications of NAND/EMMC. Please check the datasheet of the NAND/EMMC chip for the specific design.
- BLDO3 is provided power to CPVIN. If the audio function is required, the software must turn on the power.
- Different modules may have a different power consumption of WiFi. When the average power consumption is less than 1000 mA, the WiFi can be provided through DCDCE. If large than 1000 mA, suggest that use an external DCDC to supply power. When WiFi supports SDIO3.0, the VCC-PG and VCC-WIFI-IO can use 1.8 V power (change the value of ALDO2 by software); when WiFi supports SDIO2.0, the VCC-PG and VCC-WIFI-IO can use 3.3 V power.
- The DCDCB-FB of PMU must connect to the VDD-CPUFB pin of R818, and the DCDCC-FB must connect to the VDD-SYSFB pin of R818. These pins cannot close to the sensitive signals and must be surrounded with GND traces.
- Evaluate the operating voltage and maximum operating current of each power supply and mark in the schematic diagram to facilitate the traces of the PCB layout.

## 2.2. DRAM

- R818 supports DDR3/3L, DDR4, LPDDR3, and LPDDR4, you need to determine firstly the DRAM type, chip selection, and bit-width, and then choose the corresponding schematic diagram template and PCB template of DRAM. The DRAM is designed by strictly following the schematic design of the standard case and using the companion DDR PCB template. Do not suggest modifying the design.
- The VPP-DRAM (2.5 V) of DDR4 needs the extra LDO to supply power.
- Do not modify or rearrange the bit number of the component for the schematic diagram of DRAM, or the companion PCB template can not match.
- Except for the ZQ pin of LPDDR4, each ZQ pin of SoC and DRAM devices must connect to a 240R-1% pull-down resistor to GND.
- The quantity, value, and precision of DRAM external discrete devices cannot be changed randomly. Strictly follow the schematic design of the standard case.
- All filter capacitors of DRAM cannot be deleted. Recommend to reserve the reserved filter capacitors for debugging during the development stage, but they do not need to be mounted. After the development testing is stable, these filter capacitors can be deleted according to the actual situation in mass production. As shown in Figure 2-5.

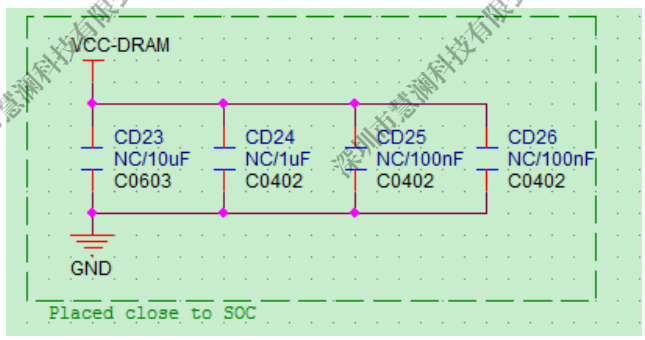



Figure 2-5 R818 DRAM Filter Capacitor

- If the DDR template is designed by yourselves, SDQ0-SDQ7, SDQ8-SDQ15, SDQ16-SDQ23, and SDQ24-SDQ31 are four groups of data lines respectively. The memory ended can be exchanged intra-group or inter-group. If the exchange is conducted inter-group, the corresponding SDQM and SDQS differential pairs must also be exchanged so that the intra-group or inter-group exchange can be conducted according to the trace difficulty of PCB.

CAUTION

The template design of LPDDR4 is different from that of other DDR types. When LPDDR4 is used for intra-group data exchange, the 8 bits within the group can be exchanged arbitrarily. However, when exchanging data inter-group, the data must be exchanged within the high and low 16-bit channels, for example, DX0 only can exchange with DX1, not exchange with DX2/DX3. If the high and low 16 bits need to be exchanged, the high and low 16 bits must be exchanged together and cannot be exchanged independently, for example, if DX1 wants to swap with DX3, it must be swapped between DX1 and DX3, between DX0 and DX2. DX1 and DX3 cannot be swapped separately, while DX0 and DX2 remain no swapped.

- See 《Allwinner AXX SDRAM Support List-Vxx》 for the DDR model supported by R818. During product design, strictly select the material model listed in the support list of Allwinner. If there are unsupported new DDR materials, please apply for debugging support through our business channels.

## 2.3. SOC

### 2.3.1. System Function Configuration Pin Design

#### 2.3.1.1. System Function Configuration Pin Design

Table 2-1 describes the system function configuration pins of the R818.

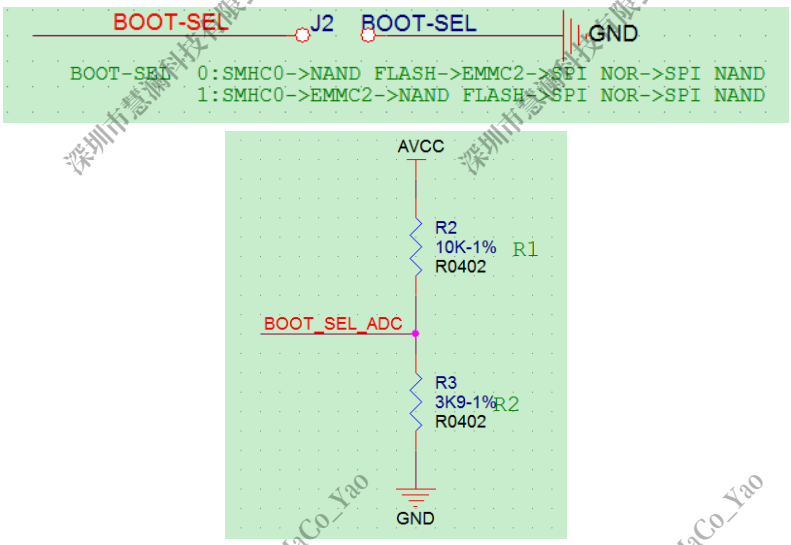
| Signal | Signal Description | Application Description |
|---|---|---|

| Signal | Signal Description | Application Description |
|---|---|---|
| BOOT-SEL-ADC | Boot sequence select.<br>External connect to voltage-division resistor. | Select the boot sequence based on the voltage-division resistor, refer to the schematic diagram of the standard case. |
| BOOT-SEL | Boot sequence select.<br>The internal is pulled up by default. The BOOT-SEL has the same function with BOOT-SEL-ADC. R818 identifies the boot sequence by BOOT-SEL-ADC by default. | 0:SMHC0->NAND FLASH->EMMC2->SPI NOR->SPI NAND<br>1:SMHC0->EMMC2->NAND FLASH->SPI NOR->SPI NAND |
| JTAG-SEL | JTAG Configuration.<br>The internal is pulled up by default. | 1: The software can select the JTAG function from PF or PB port.<br>0: Force to select JTAG function from PB port. |
| FEL | Upgrade PIN | The low level of power triggers the machine to enter the burning mode, which is used in mass production burning firmware. |
| RESET | Reset PIN | 1. CPU reset pin<br>2. Watchdog output pin |
| NMI | Non-maskable interrupt | 1. Receive the interrupt of the power system<br>2. Send an alarm signal to wake up the power system |
| TEST | IC test | Float |

Table 2-1 R818 System Function Configuration Pin

The key designing points of system function configuration pin are as follows:

- The Boot-SEL/JTAG-SEL is high level and floated by default; If it is configured to the low level, it can directly connect to GND. The Boot-SEL/JTAG-SEL is a sensitive signal and susceptible to interference from ESD. Forbid to lead out a floating trace in the actual product.
- The TEST is an internal testing pin, which should float it and forbid leading out a section of the floated traces in actual application.
- The FEL/GPADC needs to connect to 1 nF debounce capacitors when connecting keys. Do not delete or change to other capacitance.
- The BOOT-SEL /BOOT_SEL_ADC are the configuration pins for the BOOT sequence of storage media, which can adjust the BOOT sequence of NAND and eMMC. The BOOT-SEL /BOOT_SEL_ADC can be configured according to the requirements of the product. R818 turns on the BOOT_SEL_ADC pin to recognize the BOOT sequence and floats the BOOT-SEL pin by default. As shown in Figure 2-6.




| NO. | R1 | R2 | Boot Select type |
|---|---|---|---|
| 1 | NC | 10K | SMHC0->MLC NAND->SLC NAND |
| 2 | 10K | 1K | SMHC0->SLC NAND->MLC NAND |
| 3 | 10K | 2K2 | SMHC0->EMMC_BOOT->EMMC_USER |
| 4 | 10K | 3K9 | SMHC0->EMMC_USER->EMMC_BOOT |
| 5 | 6K8 | 4K7 | SMHC0->SPI NOR |
| 6 | 6K8 | 6K8 | SMHC0->SPI NAND |

Figure 2-6 BOOT-SEL Signal Design

### 2.3.1.2. Reset and Interrupt Circuit

- The AP-RESET and AP-NMI need to connect to 1 nF grounded capacitors. Do not delete or change to other capacitance, or else it will affect the normal startup of the system. The reset and interrupt signals need to be far away from board edge and interference signals and surrounded with GND traces, as shown in Figure 2-7.

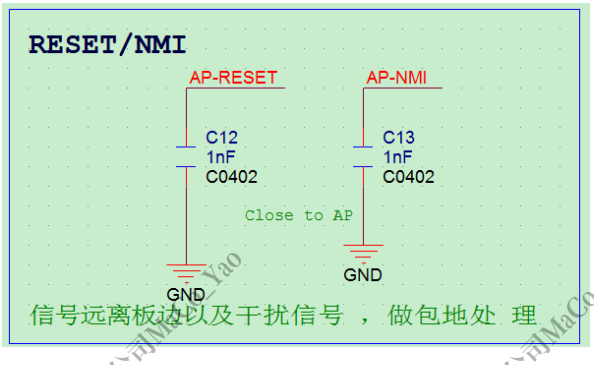



Figure 2-7 Reset and Interrupt Circuit Design

- The AP-NMI network is OD output structure and must pull up to VCC-RTC, as shown in Figure 2-8.

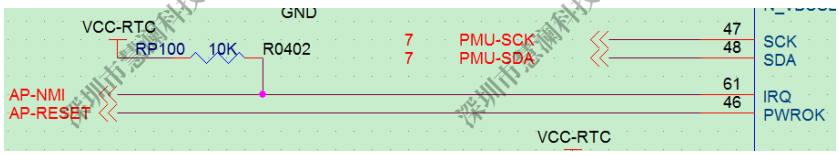



Figure 2-8 AP-NMI Pull-up Circuit Design

## 2.3.2. System Clock Circuit

- The DCXO module has the 24M CLK fanout function, which is used for the Allwinner XR819/XR829 WiFi chip. The DCXO module can save a 24M crystal of WiFi part and reduce the BOM cost of products. The WREQIN pin needs to connect to the interrupt response pin of the XR819/XR829 WIFI module, and the function cannot be used with the WiFi chip of other manufactures. If using the WiFi chip of other manufactures, the WREQIN signal needs to connect to GND, the REFCLK-OUT needs to be floated. See the schematic design of the standard case for the usage method of DCXO.
- The reference of crystal selection is as follows:
  1） If the DXCO fanout clock needs to be used for XR819/XR829 WIFI, the frequency tolerance of the crystal is less than or equal to 10 ppm;
  2） If the DXCO fanout clock needs not to be used for XR819/XR829 WIFI, the frequency tolerance of the crystal is less than or equal to 20 ppm;
- The series resistors on the high-frequency crystal oscillator network X24MO must be retained to facilitate the debugging of the oscillation amplitude. The matching capacitance needs to be matched according to the load capacitance of the crystal. As shown in Figure 2-9.

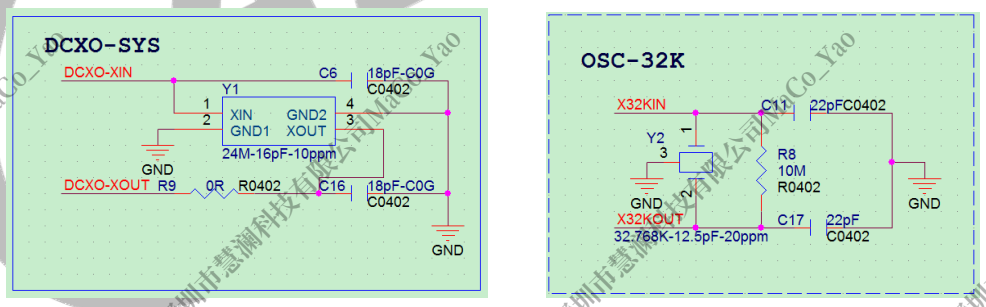



Figure 2-9 External Crystal

- The frequency precision of external 32.768 kHz crystal is less than or equal to +/-20 ppm and can work stably in high temperature 70°C and low temperature -20°C; Must reserve the 10 M parallel resistor between X32KI and X32KO and do not change; the matching capacitance needs to be matched according to the load capacitance of the crystal. As shown in Figure 2-9.
- The 32KFOUT pin is an OD output structure pin and must connect to the external pull-up resistor, the pull-up voltage and the working voltage of the external peripheral must be consistent. As shown in Figure 2-10.

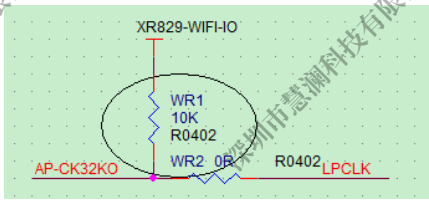



Figure 2-10 32KFOUT Circuit Design

- R818 contains an RC oscillation circuit that generates a 32K clock, the DCXO module will calibrate the RC oscillation circuit regularly, with an accuracy of about +/ -7s per day (the accuracy deviation is related to the IC process, and the deviation for the different IC are different). If the customer does not have a high requirement for the accuracy of the system clock, the external 32K crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.
- When the 32K clock needs to be fanout for the WiFi module using the 32KFOUT pin, the 32K crystal oscillator needs to be connected.

**CAUTION**

The crystal parameters shall not be changed randomly. The load capacitor of the crystal shall be mat ched with the external matching capacitor and the load capacitor of the PCB routing.

## 2.3.3.SoC Power

- The filter capacitor of SoC cannot delete and must design by strictly following the schematic design of the standard case, or else it will affect the stability of the system. As shown in Figure 2-11.

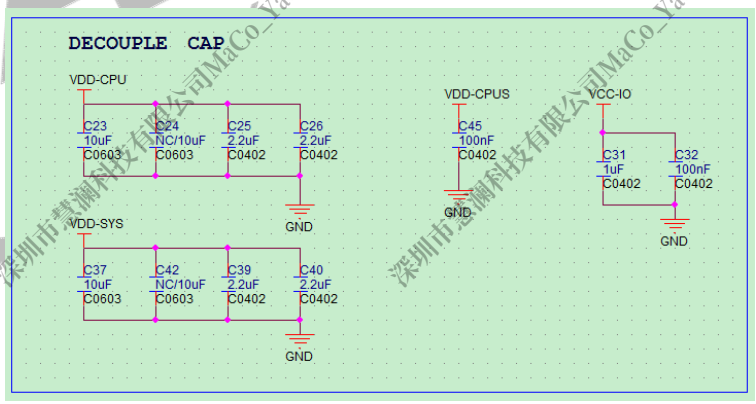



Figure 2-11 SoC Filter Capacitors

- Suggest that VDD-CPUFB and VDD-SYSFB are retained the testing point and are placed close to the SoC pin to facilitate the voltage testing of the load side. As shown in Figure 2-12.

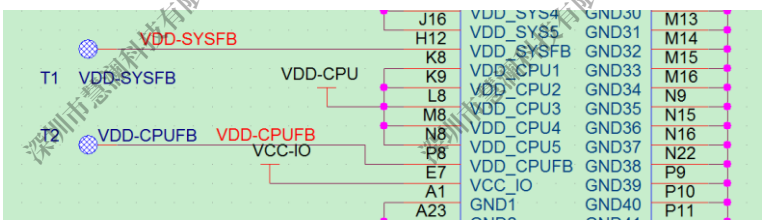



Figure 2-12 SoC Power Feedback Pin

- The rest of the SoC power pins must be connected to the external filter capacitors by following the standard case, and these capacitors need be placed close to the power pins during PCB design and cannot be deleted, such as PLL, EFUSE, RTC, GPIO, and so on. As shown in Figure 2-13.

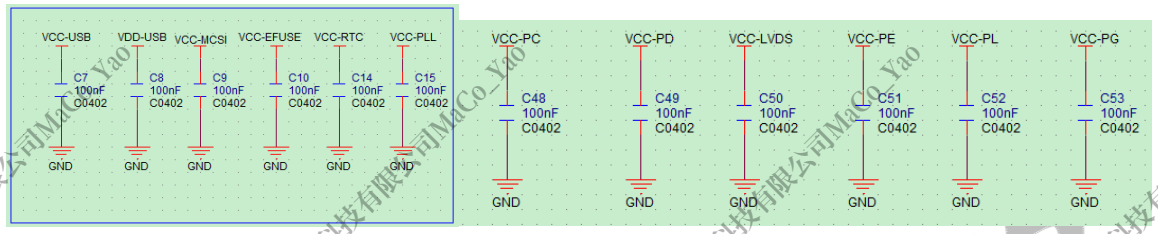



Figure 2-13 SoC Power Pin

## 2.3.4.GPIO

- The UART0 is used for system debugging and printing by default. It is recommended to reserve test points for system debugging and printing. As shown in Figure 2-14.

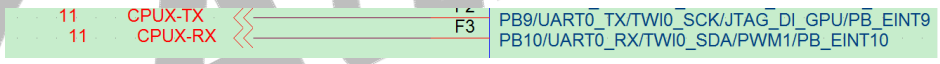



Figure 2-14 UART0 Debugging Serial Port

- Suggest that design the GPIO division is suggested by following the schematic diagram of the standard case. Do not adjust it randomly to reduce the workload of software adaptation.
- The PL0/PL1 is the TWI communication port between SoC and PMIC and has 4.7 kΩ internal pull-up resistors, so it is not recommended to share the PL0/PL1 port with other I2C devices. As shown in Figure 2-15.

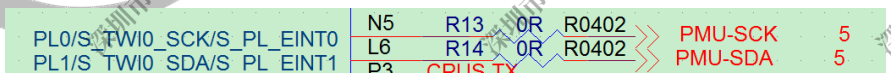



Figure 2-15 TWI Communication Bus

- The PL port in the CPUS domain holds power and maintains normal working conditions during standby mode. If the wake-up function is needed, please connect the interrupt wake-up source to the PL port and pay attention to match the voltage level.
- The GPIO ports with independent power supply can be adjusted according to the requirements of peripherals, such as PC, PD, PE, PF, PG and PL ports; The PB and PH ports have not the independent power supply and are powered by the VCC-IO power with the default voltage value of 3.3 V. When using GPIO, it is necessary to pay attention to the level matching problem with peripherals.
- When the GPIO port needs to increase the pull-up resistor, the corresponding pull-up power supply should be designed as the corresponding voltage domain to avoid the leakage of the system power supply and the increase of the system power consumption. For example, the pull-up resistors of the PE

port must be connected to the VCC-PE power.

## 2.4. FLASH

- The FLASH part of the standard case provides the schematic diagram reference design of NAND TSOP48, BGA152, and eMMC BGA169 packages. Customers can add or remove the related design based on the product specification requirements.
- In the PCB layout, the Flash should be placed close to the SoC, and the traces should be separated from the high-frequency signals.
- Suggest that the footprint of Flash uses the PCB library provided by Allwinner, and the Flash is compatible with the dual Layout design of TSOP48 NAND/eMMC FLASH.
- If using eMMC 5.0 and above wafers, the T5 and H6 pin of eMMC must be connected to 0R pull-down resistors to GND. Because the eMMC-DS signal of R818 integrates the pull-down resistors, the 10K resistor connected with R5 pins can be NC. For other non-eMMC5.0 chips, the T5, H6, and R5 must be NC. As shown in Figure 2-16.

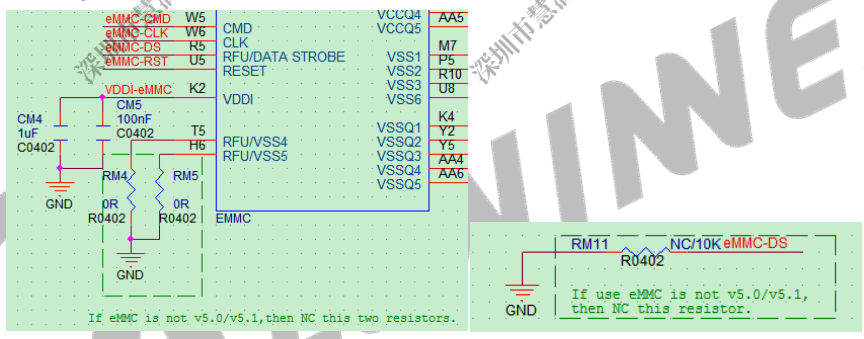



Figure 2-16 eMMC 5.0/5.1 Mounting Circuit

- If the eMMC device uses HS200 and HS400 high-speed bus mode, the voltage of the eMMC VCCQ and the GPIO PC port needs to be configured to 1.8 V. In application, please configure the VCC-PC power according to the actual requirements. As shown in Figure 2-17.

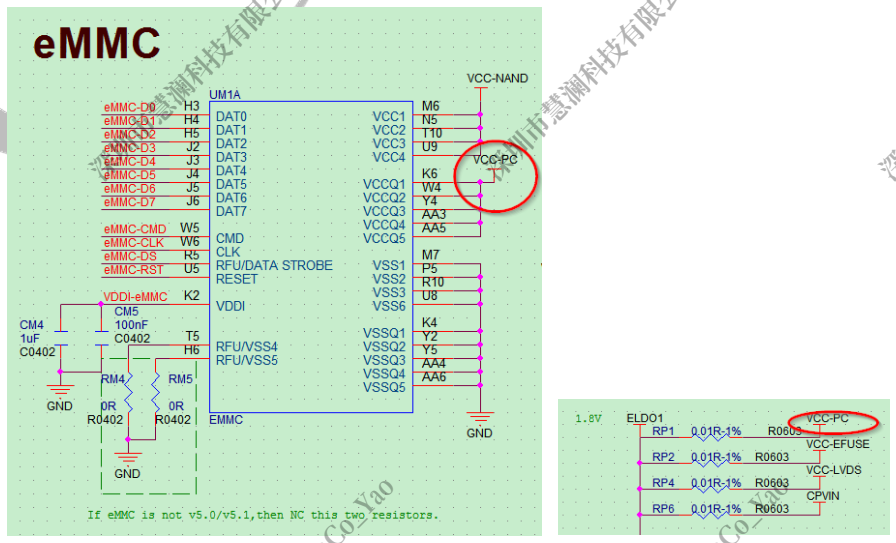



Figure 2-17 VCC-PC Power Design

- One piece of NAND can be 1 CE or 2 CEs. Two pieces of NAND can only be 1 CE.

- Some NAND Flash has VPS power pins, and the circuit design of VPS0 and VPS1 for NAND Flash needs to be matched with the corresponding datasheet.
- Note that the IO voltage of NAND Flash has 1.8 V and 3.3 V, and please see the corresponding datasheet and match the voltage of VCC-PC based on the actual requirement.

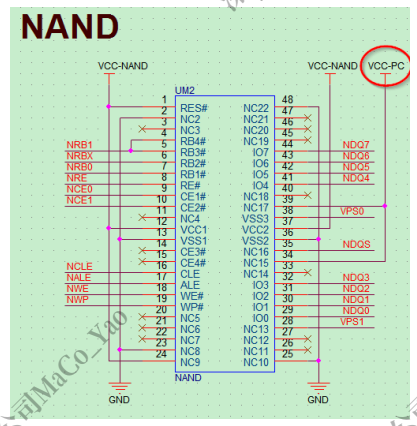



Figure 2-18 IO Power of NAND Flash

- Add the impedance requirement descriptions of NAND/eMMC signal traces in the schematic diagram, as shown in Figure 2-19.

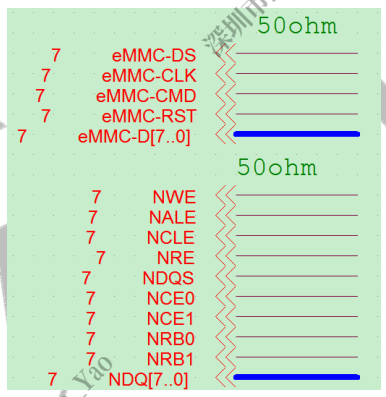



Figure 2-19 NAND/eMMC Signal Line Impedance Label

- Must mark the operating voltage and the maximum operating current about NAND/eMMC in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-20.

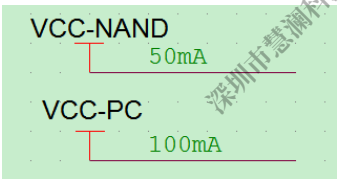



Figure 2-20 The Operating Current and Voltage Label of Flash Power

- The material selection of NAND/eMMC must use the model in 《Allwinner XXX eMMC Support List_Vxx》 and 《Allwinner XXX NAND Flash Support List_Vxx》, and select the model supported by R818 in the support list.

## 2.5. CARD (option)

The CLOCK pin does not need a pull-up resistor and needs to connect to a 33 Ω resistor in series near the SoC end,

as shown in Figure 2-21. If the capacitors are connected in parallel, the capacitance should not exceed 15 pF.

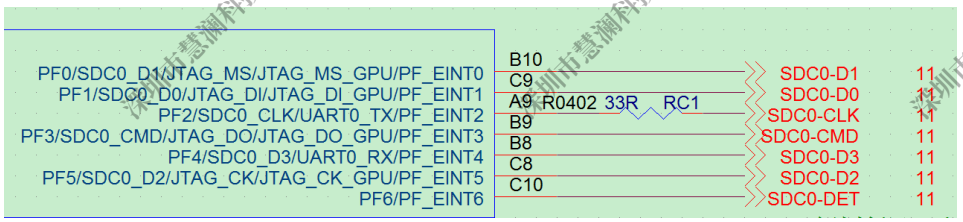



Figure 2-21 SDC0-CLK Series Resistor

- The CMD and DET signals must be pulled up to VCC-PF, see the schematic diagram of the standard case for details.
- R818 supports SD3.0 protocol and automatically identifies the type of CARD, then adjusts the IO voltage. If the TF card is an SD3.0 storage card, R818 works in SD3.0 mode, and the IO voltage will be switched from 3.3 V to 1.8 V, and the power supply of the PF port will be switched inside the SOC without the need for external independent power.
- The SD interface signal line is a high-speed signal line. If in SD3.0 mode, the parasitic capacitance of TVS tube by parallel connecting to the signal line is required to be less than or equal to 5 pF; if only in SD2.0 mode, the parasitic capacitance of TVS tube is required to be less than 35 pF, or else the quality of data transmission will be affected.
- Suggest that reserve the series resistors in the DET signal line. This is to avoid the signal undershoot when SD CARD is inserted to affect the signal quality and to improve the ESD performance of IO signals. As shown in Figure 2-22.

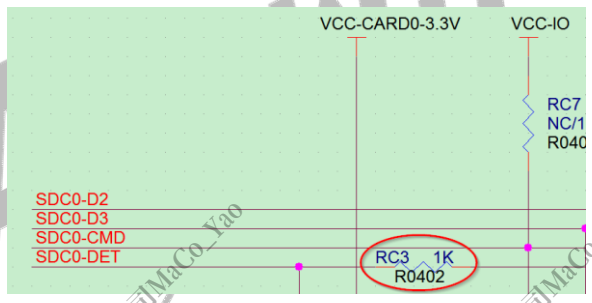



Figure 2-22 SDC0-DET Series Resistors

- For VCC-CARD, it is recommended to use a power switch protection circuit to avoid damaging the system when a bad card is inserted and to improve the power quality of the SD CARD when it is powered on. To reduce the product cost, you can delete this circuit. As shown in Figure 2-23.

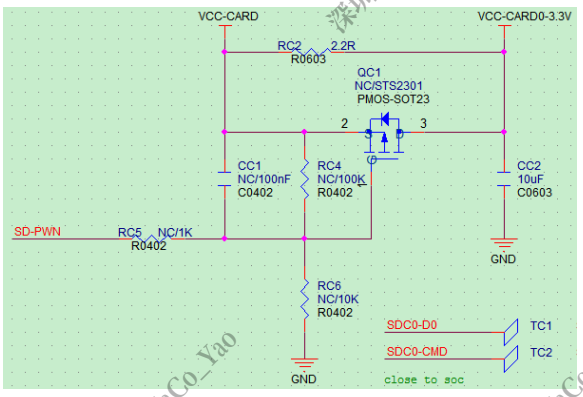



Figure 2-23 The Protect Circuit of VCC-CARD

- The TF interface of some products is shrunk inside the structure shell, which has a lower risk of ESD

interference. To reduce the product cost, the ESD device of the TF card interface can be cut-down according to the product structure and test result.

- Must mark the trace impedance requirement of the TF card signal in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-24.

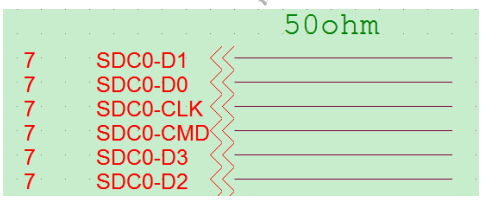



Figure 2-24 The Trace Impedance Requirement of TF Card Signal

- Must mark the operating voltage and the maximum operating current of TF Card power to facilitate PCB layout design. As shown in Figure 2-25.

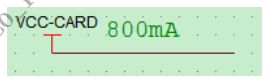



Figure 2-25 The Operating Voltage and Current Label of TF Card

## 2.6. USB

- The USB0 has the OTG function, and the USB1 only has the HOST function. The downloading function only can use the USB0 port, please note the differences in product function definitions.
- The ID pin on the USB0 socket is used for external device detection. It is connected to the GPIO pin and pulled up to the VCC-IO voltage through a resistor. If the ID detection is low, the SoC recognizes that the USB peripheral is inserted, then the USB0 works in Host mode. Otherwise, the USB0 works in Device mode.
- Suggest that reserve the series resistors in the ID signal line. This is to avoid the signal undershoot when a USB device is inserted to affect the signal quality and to improve the ESD performance of IO signals. As shown in Figure 2-26.

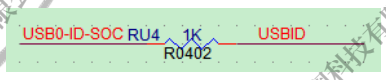



Figure 2-26 USB-ID Series Resistors

- The DP/DM signal is a high-speed signal line, and the parasitic capacitance of the TVS tube connected to the ground is required to be less than 5 pF, otherwise, it will affect the data transmission.
- It is recommended to reserve the common mode inductor on USB D+/D-, which can layout together with 0R resistors to facilitate EMI testing and changing. As shown in Figure 2-27.

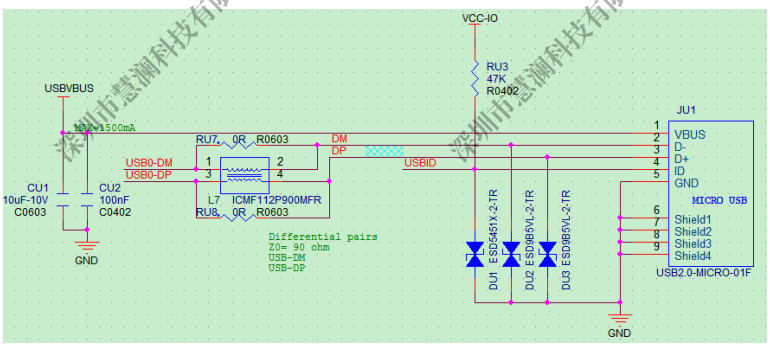



Figure 2-27 USB0 Circuit Design

- For USB0 and USB1, the design of the power supply should be consistent with the corresponding power supply solution.

  1、The power design of USB0:

  Because PMIC does not have a 5 V boost and current-limiting output functions, the USB0 needs an external current limiting switch, and its power supply comes from the system VCC-5V. As shown in Figure 2-28.

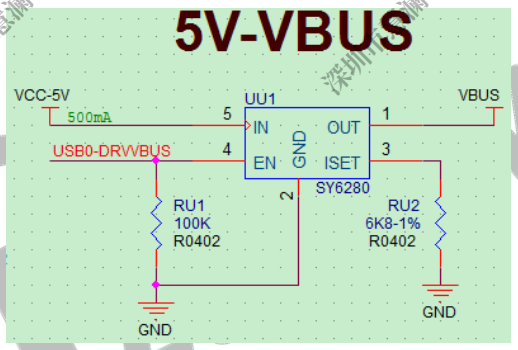



Figure 2-28 USB0 Power Design

2、The power supply of USB1:

a) Because the front end contains a 5 V boost IC, the power supply of USB1 comes from the system VCC-5V, and only one current-limiting switch needs to be added. As shown in Figure 2-29.

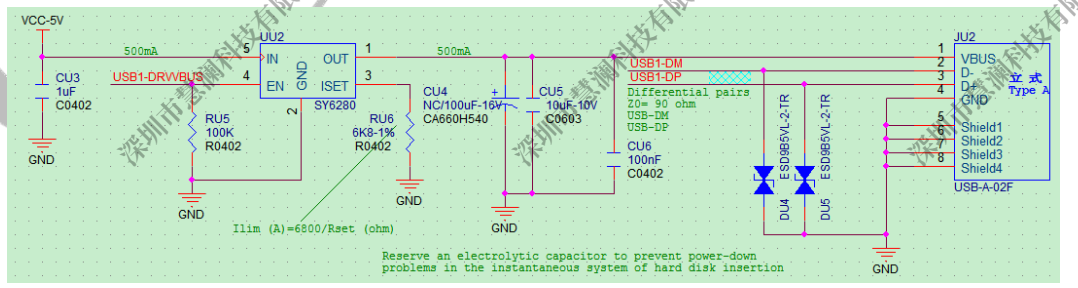



Figure 2-29 USB1 Power Design

- Mark the trace impedance requirement of the USB signal in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-30.

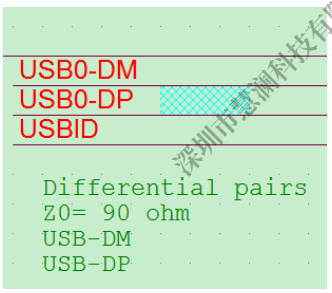



Figure 2-30 The Trace Impedance Requirement of USB Signal

- Mark the operating voltage and the maximum operating current of USB power in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-31.

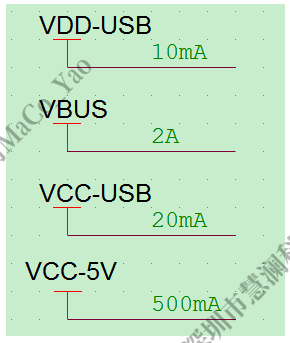



Figure 2-31 The Operating Voltage and Current Label of USB

## 2.7. WIFI-BT

- Ensure that the voltage of VCC-WIFI must be the same as the working voltage of the WiFi chip.
- The SDIO interface of the WiFi must be the same as the voltage of the PG port, and the voltage of the interrupt port must be the same as the voltage of the PL port.
- Table 2-2 shows the connection mode of the PCM. Please do not connect oppositely.

| SoC end | WiFi end |
|---|---|
| PCM-CLK | PCM-CLK |
| PCM-SYNC | PCM-SYNC |
| PCM-DOUT | PCM-DIN |
| PCM-DIN | PCM-DOUT |

Table 2-2 PCM Connection Mode

- Table 2-3 shows the connection mode of the UART. Please do not connect oppositely.

| SoC end | BT end |
|---|---|
| UART-RX | UART-TX |
| UART-TX | UART-RX |
| UART-RTS | UART-CTS |
| UART-CTS | UART-RTS |

Table 2-3 UART Connection Mode

- The 32KFOUT of R818 is the output pin of the internal 32.768 kHz. When used in combination with the WiFi module, the external pull-up resistors must be added, and note that the pull-up power supply is VCCIO-WIFI. As shown in Figure 2-32.

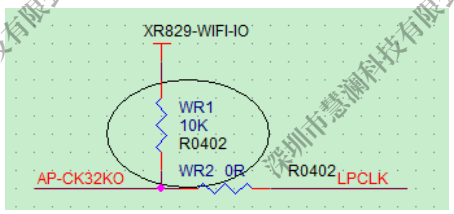



Figure 2-32 AP-CK32KO Pull-up Circuit

- The XR829 can be used in combination with the 24M FANOUT of R818 DCXO to achieve the purpose of saving crystal. If the XR829 uses the 24M FANOUT of DCXO, the CLKREQOUT pin needs to connect to the WREQIN pin of the SoC, the XTAL2 pin needs to connect to the AP-CK24M-OUT pin of the R818, and the XTAL1 pin needs to connect to GND, as shown in Figure 2-33. If the XR829 does not use the 24M FANOUT of DCXO, the CLKREQOUT pin of the XR829 needs to be floated, the WREQIN of the XR829 needs to connect to GND, and the XTAL1 and XTAL2 need to connect to the external crystal.

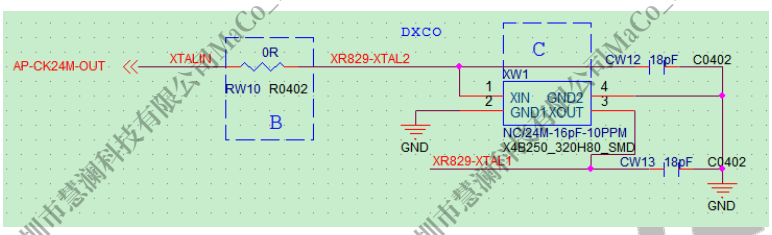



Figure 2-33 The XR829 Circuit Design Without 24M Crystal

- If using the XR829 chip of Allwinner, please use the companion crystal (Model: E3SB24E004304E) by Allwinner to ensure the RF performance of WiFi.
- If using the XR829 chip and the companion crystal E3SB24E004304E, if you want to use the DCXO module of R818 to save the crystal, you can mount this crystal to the DCXO part of R818, and at the same time, ensure that change the corresponding matching capacitor from 18 pF to 20 pF.
- The VDD14_XX power output of XR829 has LDO and DCDC modes. If using LDO output mode, please pull up the LDO_SEL pin to VCCIO-WIFI, and at the same time no connect the inductor LP14, and the power is output from the SENSE pin. If using DCDC output mode, please pull down the LDO_SEL pin to GND, and mount the inductor LP14 at the same time, and the power is output from the VLX pin. As shown in Figure 2-34.

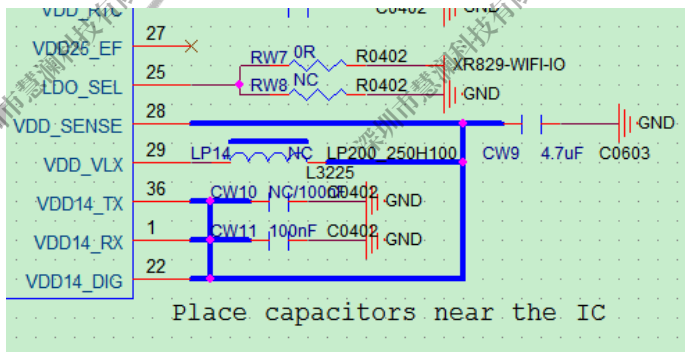



Figure 2-34 XR829 VDD14 Power Design

- The antenna of WiFi needs to reserve aπ-type circuit for antenna debugging. As shown in Figure 2-35.

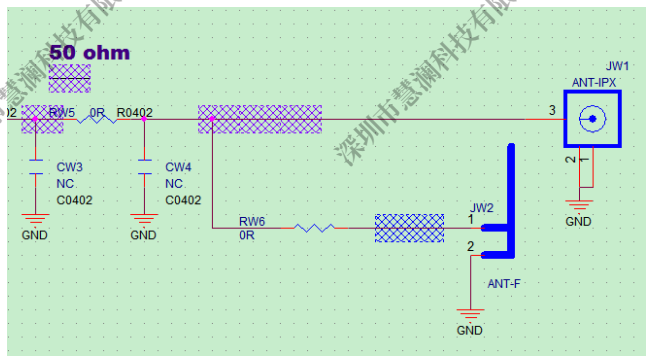



Figure 2-35 WiFi Antenna Matching Circuit

- Each new PCB using Onboard WiFi requires an impedance matching and conduction testing.
- For other WiFi modules of different manufacturers, see the design guidance document of the WiFi original factory for specific schematic design.
- Mark the trace impedance requirement of the WiFi SDIO signal in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-36.

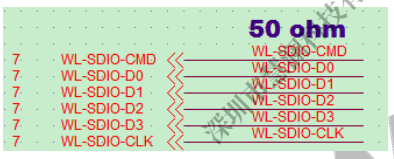



Figure 2-36 The Trace Impedance Requirement of SDIO Signal

- Mark the operating voltage and the maximum operating current of the WiFi power supply in the schematic diagram to facilitate PCB layout design. As shown in Figure 2-37.

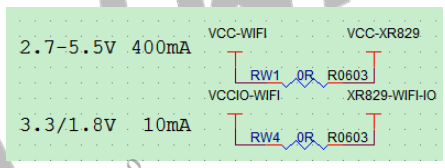



Figure 2-37 The Operating Voltage and Circuit of WiFi

## 2.8. AUDIO

- The ground points of AVCC, VRA1, VRA2, and AGND are gathered to a point and must connect to a 0R resistance to GND. The parameters of the resistor and capacitor on the external network of the Audio CODEC module cannot be modified. As shown in Figure 2-38.

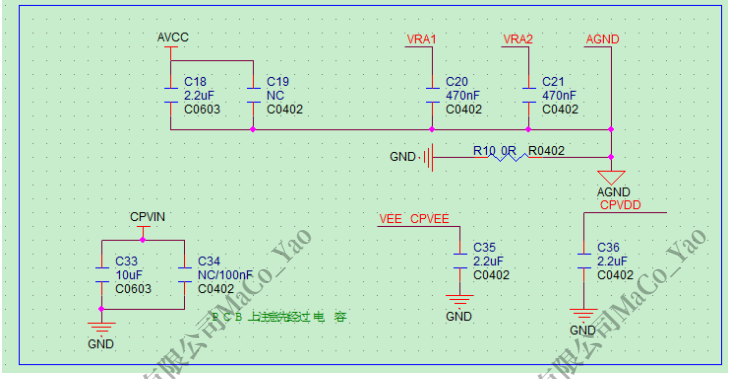



Figure 2-38 Audio Codec External Circuit

- The CPVEE and VEE share the filter capacitor. In the design of PCB, they need to separately route to connect to the filter capacitor C35, and cannot connect together on the PAD under IC.
- Must reserve the RC circuit of headphone output, such as C67/R26, C68/R27 shown in Figure 2-43. The grounded resistor of HPOUTFB is close to the headphone socket, and the trace between the headphone socket and the grounded resistor R28 must be at least 15 mil. Refer to the ground of the headphone socket for the MIC2N-N network. As shown in Figure 2-39.

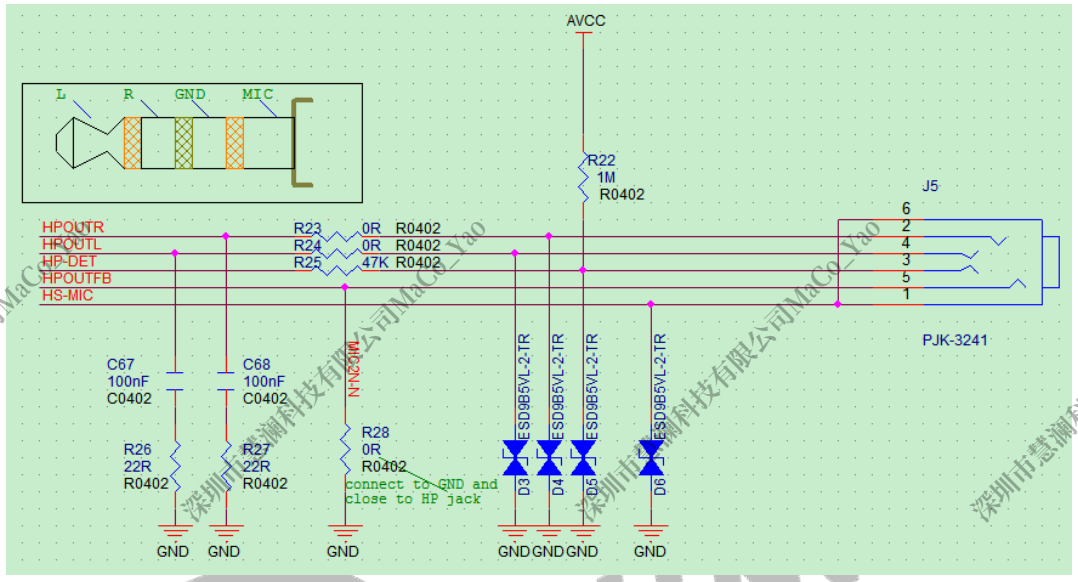



Figure 2-39 Headphone Interface Circuit Design

- The headphone detection is to detect the high and low state of HP-DET level. If the headphone is inserted, and the 3 and 4 pins are shorted, the resistance R84 NC is not mounted; If the headphone is removed, and the 3 and 4 pins are disconnected, the resistor R84 is mounted at 100K, as shown in Figure 2-39. The effective levels detected by different headphones need to be modified in the sys_config configuration file.
- If the product does not have a headphone interface but need to connect the audio amplifier via HPOUTL/HPOUTR signal, the HPOUTFB signal must be grounded nearby on the CPU end.
- The headphone output HPOUTR/L channel does not allow connecting in series to EMI beads, otherwise, the audio transmission quality will be affected.
- Different headphone sockets have different structures. The headphone connection method must consider the actual structure of the headphone socket. For details, please refer to the corresponding specifications of the headphone socket, and consider the connecting sequence of four-segment headphones in the European standard (OMTP) or American standard (CTIA). The standard case defaults to the American standard four-segment headphone connection. Figure 2-40 shows the interface difference between CTIA and OMTP.

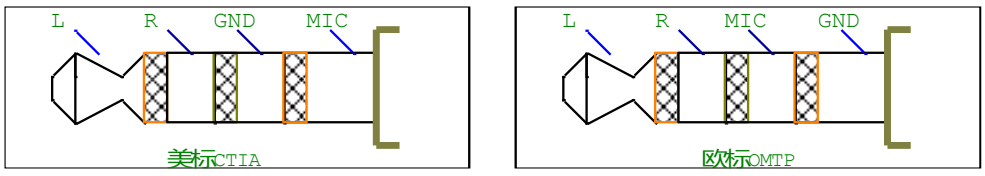



Figure 2-40 The Headphone Interface Difference between CTIA and OMTP

- The AVCC power is the power supply of the internal analog module, which requires high power quality. Please do not change the existing power supply relationship.
- The HS-MIC signal is MIC detection and signal reception pin, which is generally located outside the

headphone interface and susceptible to interference from ESD. So the HS-MIC needs to connect to a 1 nF grounded capacitor (such as C66) nearby the headphone socket to improve the ESD performance of the system and cannot delete this capacitor.

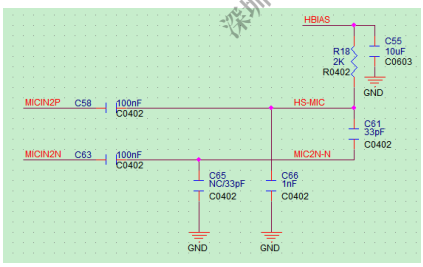



Figure 2-41 HS-MIC Signal Circuit Design

- R818 supports the stereo dual speaker outputs. If the product is mono speaker output, please connect the power amplifier to the HPOUTR signal by default. Meanwhile, the power amplifier enabling signal needs to be connected to the pull-down resistors to GND by default to avoid the abnormal sound of the upper and downer speakers. During designing a power amplifier, pay attention to the selection of the feedback resistors. The selection of the feedback resistor should refer to the specification of the power amplifier to avoid the excessive amplification factor, which may cause sound distortion. As shown in Figure 2-42.

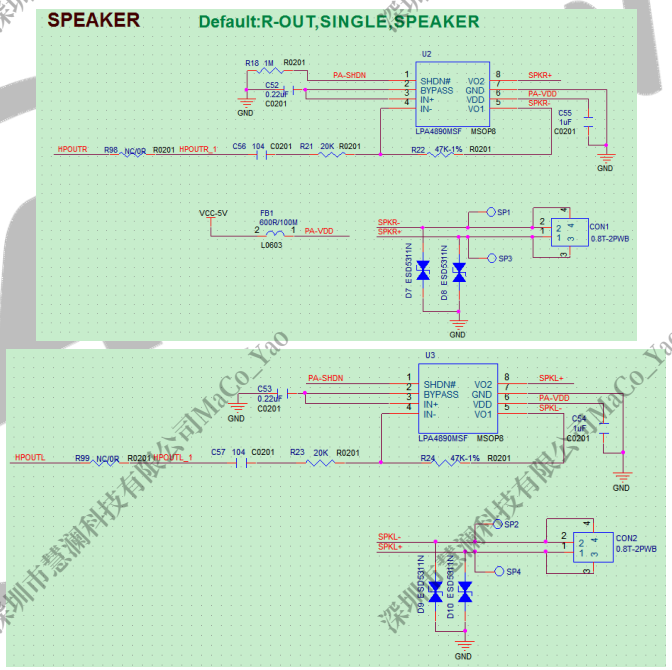
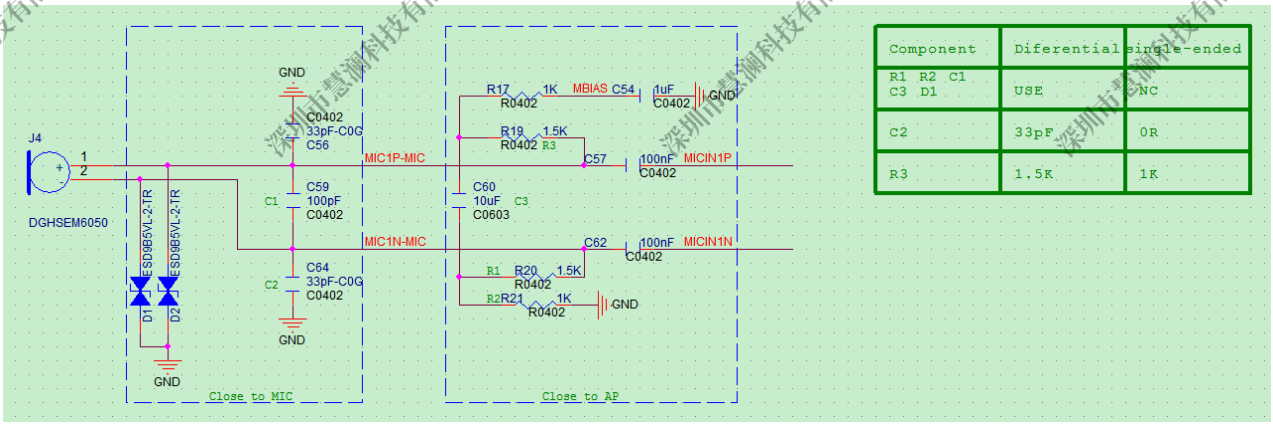



Figure 2-42 SPEAKER Circuit Design

- The HPOUT signal of R818 only supports single-ended signal output and does not support differential signal output. When connecting to a differential class D power amplifier, the IN-pin must be grounded.
- The circuit design of the local MIC recommends single-ended design and class-differential design. If the product needs cost down, it is recommended to use a single-ended design, which can save an ESD device. If the product needs to improve the mic sound quality and anti-interference, it is recommended to adopt a differential design, and the voice recognition products must use a differential design. As shown in Figure 2-43.




| Component | Diferential | single-ended |
|---|---|---|
| R1 R2 C1 C3 D1 | USE | NC |
| C2 | 33pF | 0R |
| R3 | 1.5K | 1K |

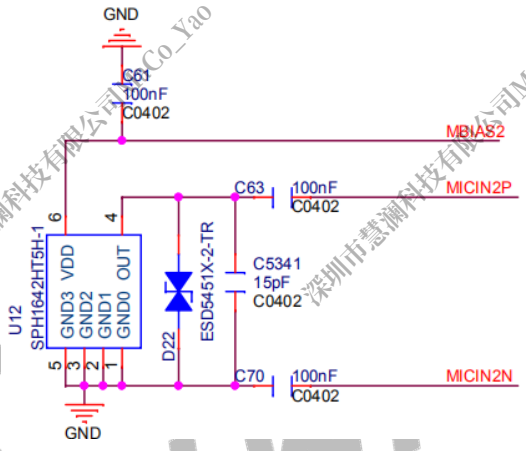
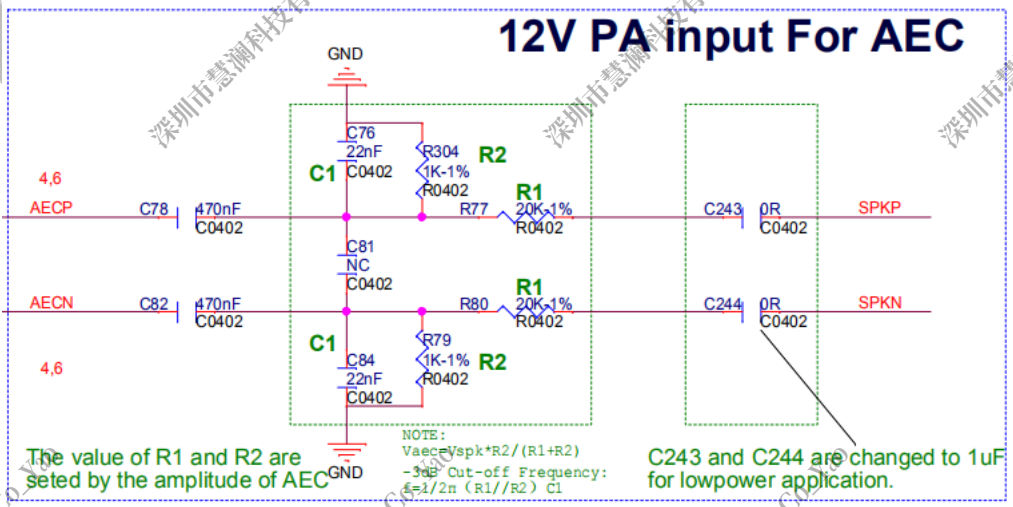



Figure 2-43 ECM&MEMS MIC Circuit Design

- The offset resistors of headphone MIC and local MIC need to be matched based on differential or single-ended, such as R17/R19/R20/R21 resistors shown in Figure 2-43.
- The AEC circuit refers to the following connection mode: when the power voltage of the power amplifier is 12 V, use the reference design circuit of 12 V PA; when the power voltage of the power amplifier is 5 V, use the reference design circuit of 5V PA. The division-voltage value of the circuit can be adjusted according to the actual scene.



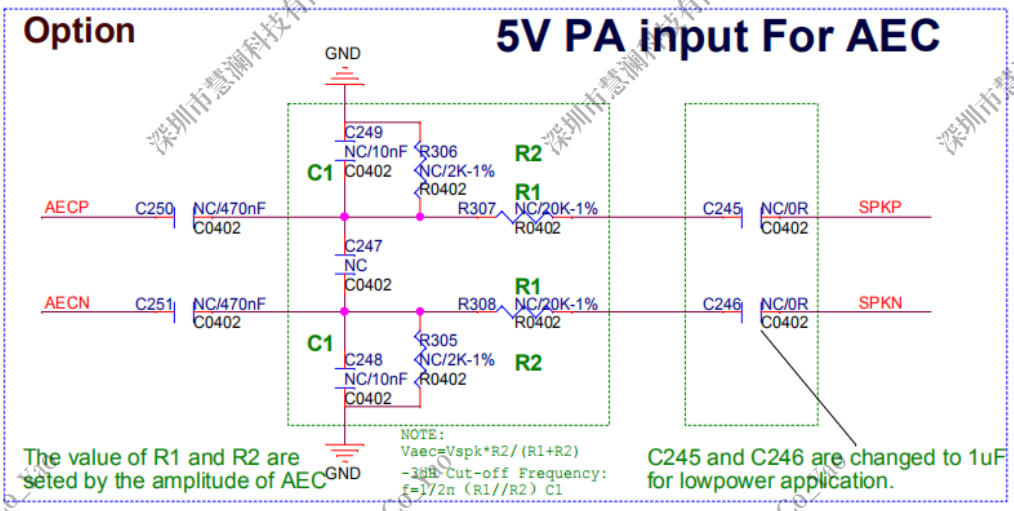



Figure 2-44 AEC Loop Reference Design

- Mark the operating voltage and the maximum operating current of AUDIO power in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-45.

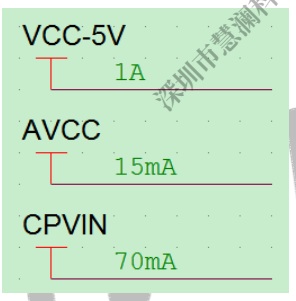



Figure 2-45 The Operating Voltage and Circuit of Audio Power

CAUTION

The HS-MIC signal needs to connect to a 1 nF grounded capacitor to improve the ESD performance.

## 2.9. Debug

- The JTAG debugging interface and UART interface of CPUX can come out from the PB and PF ports of the SoC respectively. At least one of the interfaces must be reserved for both development debugging and the analysis of the mass production problem. For the products with TF card function, suggest that the PB port also reserves test points as much as possible to increase problem analysis and debugging channels, the mass production does not need to mount components. The UART interface is suggested that add an anti-leakage circuit to avoid leakage between the prototype and the computer during the long-term aging test, which may cause the machine to work abnormally or the computer to hang up. As shown in Figure 2-46.

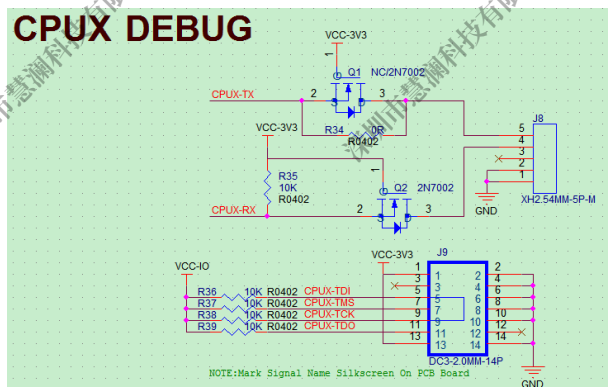



Figure 2-46 CPUX Debugging Interface

## 2.10. KEY

- Select the number of LRADC keys and increase or decrease them according to the requirement of the product. The voltage acquisition range of LRADC is 0 to 1.266 V. In the design, please ensure that the voltage interval between each key value is greater than 0.2 V. The precision of the division-voltage resistor must be 1%. As shown in Figure 2-47.

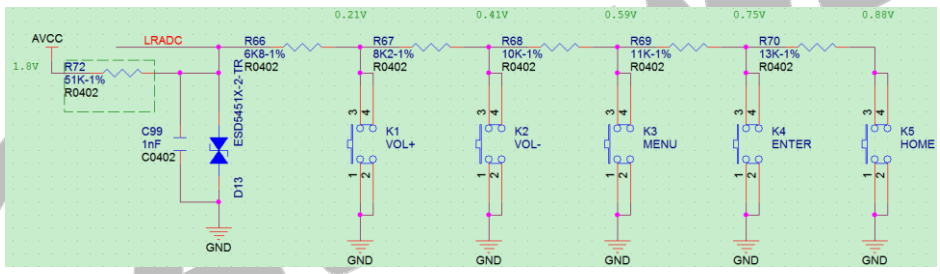



Figure 2-47 Key Circuit Design

- If no key is required, and the SDK compatibility is considered, the LRADC must add a 100 kΩ pull-up resistor to AVCC; otherwise, the LRADC can be floated.
- The UBOOT button is used for the hardware trigger to download software. Please decide whether to reserve it according to the product requirements. As shown in Figure 2-48.

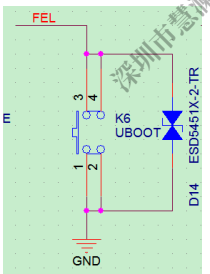



Figure 2-48 UBOOT Key

- Please decide whether to delete RESET and POWER keys according to the product requirements.
- There are two key combinations for the machine hardware to trigger the firmware burning. Please reserve one of the keys to avoid the software fails to burn after the machine program is damaged.
  1) UBOOT key;
  2) Volume up or down + POWER key.

## 2.11. DISPLAY

- R818 supports three LCD panels：RGB, LVDS, MIPI DSI. In product design, please select the relevant reference circuit according to the specific LCD specifications.
- The RGB, LVDS, and DSI interfaces corresponding to the PD port should be designed by following the standard case and cannot be modified. As shown in Figure 2-49.

| | | |
|---|---|---|
| LCD0_D2 | LVDS0_D0P | DSI_DP0 |
| LCD0_D3 | LVDS0_D0N | DSI_DM0 |
| LCD0_D4 | LVDS0_D1P | DSI_DP1 |
| LCD0_D5 | LVDS0_D1N | DSI_DM1 |
| LCD0_D6 | LVDS0_D2P | DSI_CKP |
| LCD0_D7 | LVDS0_D2N | DSI_CKM |
| LCD0_D10 | LVDS0_CKP | DSI_DP2 |
| LCD0_D11 | LVDS0_CKN | DSI_DM2 |
| LCD0_D12 | LVDS0_D3P | DSI_DP3 |
| LCD0_D13 | LVDS0_D3N | DSI_DM3 |
| LCD0_D14 | LVDS1_D0P | |
| LCD0_D15 | LVDS1_D0N | |
| LCD0_D18 | LVDS1_D1P | |
| LCD0_D19 | LVDS1_D1N | |
| LCD0_D20 | LVDS1_D2P | |
| LCD0_D21 | LVDS1_D2N | |
| LCD0_D22 | LVDS1_CKP | |
| LCD0_D23 | LVDS1_CKN | |
| LCD0_CLK | LVDS1_D3P | |
| LCD0_DE | LVDS1_D3N | |
| LCD0_HSYNC | | |
| LCD0_VSYNC | | |

Figure 2-49 RGB/LVDS/DSI Interface Definition

- Make sure that the MIPI or LVDS interface signals between the AP end and LCD end are connected correctly. The positive and negative signals cannot be reversed.
- The positive and negative power supply of LCD shall be designed by following the LCD specifications. The design of the standard case is for reference only.
- The backlight IC of the LCD needs to be designed by following the specific LCD specifications and adopts PWM dimming by default. When using PWM dimming, please note that the PWM frequency needs to be greater than 20 kHz, otherwise there will be inductance noise. Suggest that adjust the PWM frequency to 30-50 kHz according to the specification parameters of backlight IC.
- The grounded current-limiting resistors of FB end for the backlight IC need be 1% precision, and the selected package needs to meet the power demand of the circuit. As shown in Figure 2-50.

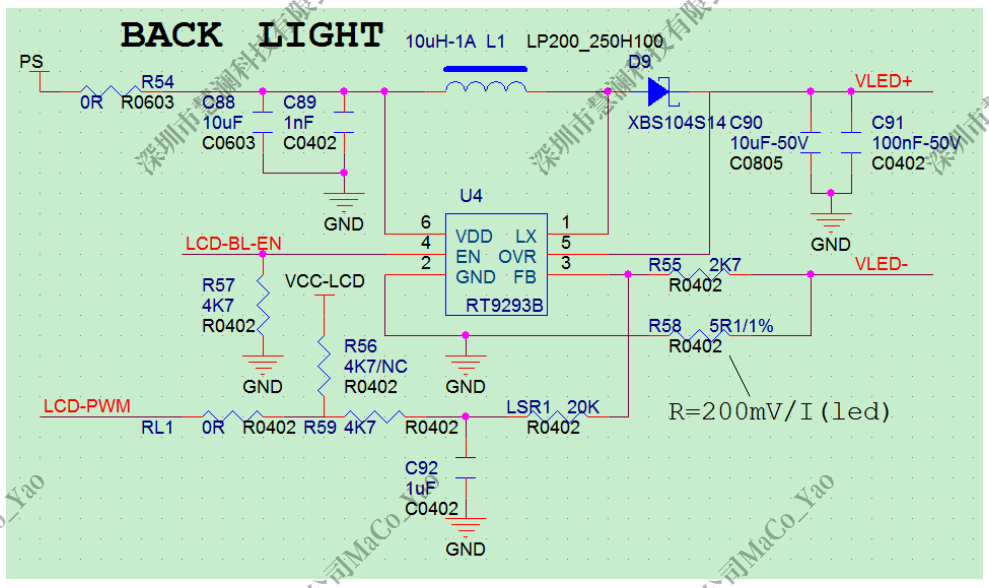



Figure 2-50 LCD Backlight Circuit Design

- Please confirm whether the IO voltage of LCD is consistent with the control IO voltage of the AP end. If not, pay attention to do level matching, such as LCD-RST signal.
- Mark the trace impedance requirements of LVDS/MIPI DSI signal lines in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-51.

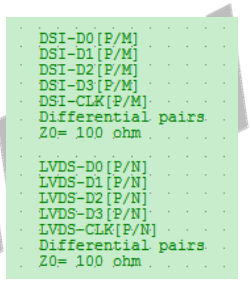



Figure 2-51 The Trace Impedance Requirement of LVDS/MIPI-DSI

- Mark the operating voltage and the maximum operating current of LCD power in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-52.

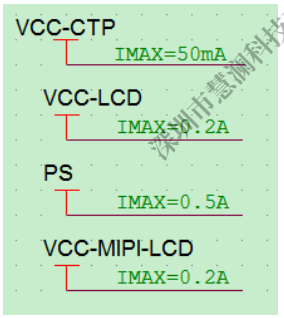



Figure 2-52 The Operating Voltage and Current of LCD Power

## 2.12. SENSOR

- The VCC and IOVCC voltages of the SENSOR may be inconsistent. Make sure that the voltage domain of the master I2C bus is consistent with the IOVCC of the SENSOR; otherwise, the level conversion is needed.

- The I2C of the SENSOR needs to connect to pull-up resistors and cannot delete them, as shown in Figure 2-53.

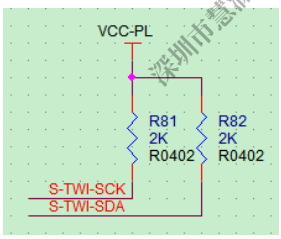



Figure 2-53 I2C Circuit Design

- The interrupt signal of the SENSOR is connected to the PH port of R818 by default, if a SENSOR needs to be worked in standby mode, please keep the power supply of the SENSOR working normally in standby mode, and connect the interrupt port to PL port. Such as the circuit design of the LIGNT sensor shown in Figure 2-54.

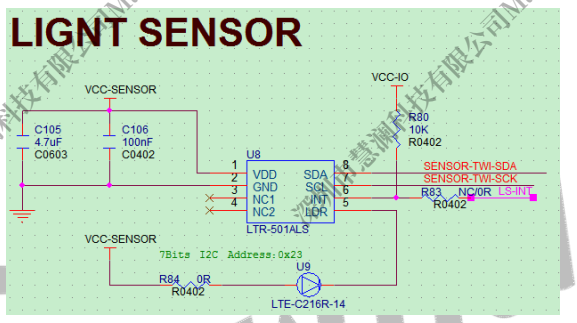



Figure 2-54 The Circuit Design of LIGNT Sensor

- When the same I2C connects to multi-sensor devices, the I2C address cannot repeat.
- Mark the operating voltage and the maximum operating current of SENSOR power in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-55.

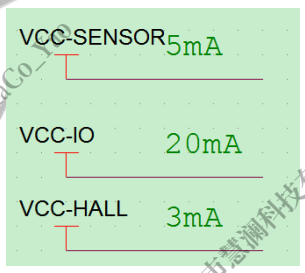



Figure 2-55 The Operating Voltage and Current of SENSOR Power

## 2.13. CAMERA

- R818 supports two MIPI-CSI interfaces, channel A and B are switched by internal analog switches for time-sharing multiplexing. In hardware design, the correspondence between A/B channels and front/rear cameras can be exchanged to facilitate PCB layout design. However, if it is different from the standard case, perform related software adaptations at the same time.
- The power supply of the camera (AVDD-CSI, DVDD-CSI, IOVDD-CSI, AFVCC-CSI) must be connected to filter capacitors. Refer to the camera sensor specification for the capacitance. As shown in Figure 2-56.

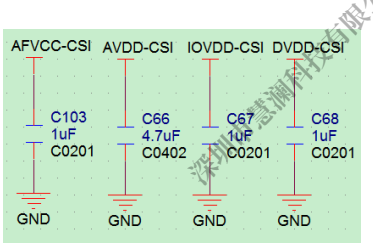



Figure 2-56 Camera Power

- For the MCLK, suggest that reserve the NC capacitor near the socket and connect to the 33R resistor in series near the SOC end. As shown in Figure 2-57.

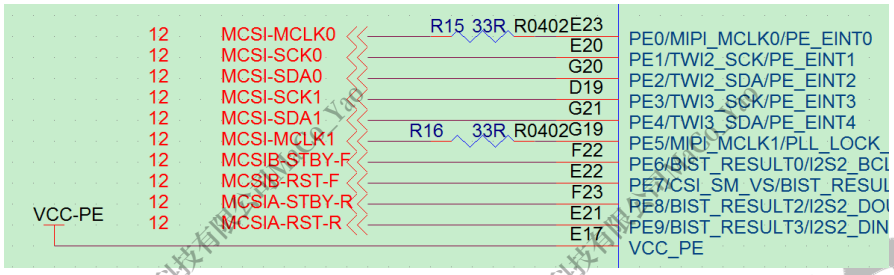



Figure 2-57 MCLK Circuit Design

- AVDD-CSI supplies power to the analog circuit inside the sensor, which has a high requirement for the ripple noise of power supply, so it must be supplied separately from other power sources to ensure the power quality of AVDD-CSI.
- If the module includes the autofocus function, the module needs to be supplied power by AFVCC-CSI. If the AFVCC-CSI power has no timing requirement, AFVCC-CSI and IOVDD need to be combined to supply power; if the AFVCC-CSI power supply has a timing requirement, it needs to be supplied independently.
- If the digital power DVDD-CSI of the front camera and rear camera have the same supply voltage, then the front camera and the rear camera can use the same power network. If the supply voltage of the digital power DVDD-CSI is different, it is recommended that supply separately power to the front camera and rear camera or do DCDC step-down compatible design for CAMERA modules.
- The definition of the camera module pin: Check whether the PIN definition of the camera module is consistent with the socket. Note that the general 24PIN socket has the upper contact or the downer contact. Check whether the direction of the gold-finger contact surface for the module matches.
- The CAMERA I2C must be connected to pull-up resistors and cannot be shared with other devices. The I2C address of the front and rear cameras should be different to avoid communication conflict. As shown in Figure 2-58.

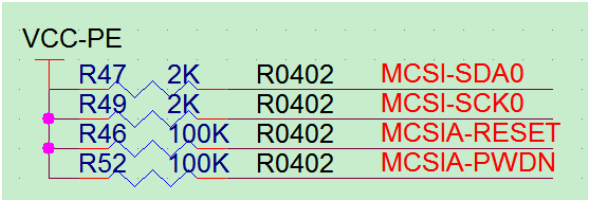



Figure 2-58 I2C Design of Camera

- Mark the trace impedance requirement of the MIPI-CSI signal in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-59.

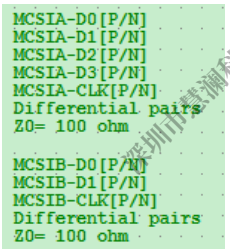



Figure 2-59 The Trace Impedance Requirement of MIPI-CSI Signal

- Mark the operating voltage and the maximum operating current of the camera power in the schematic diagram to facilitate PCB layout design, as shown in Figure 2-60.

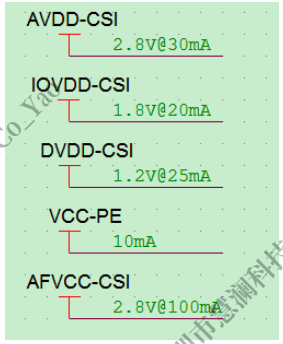



Figure 2-60 The Operating Voltage and Current of Camera Power

## 2.14. TP

- The I2C of the TP must connect to pull-up resistors.
- Note that the voltage of the PH port and the IO voltage of the TP driver chip must be consistent.
- Mark the operating voltage and the maximum operating current of the CTP power in the schematic diagram to facilitate PCB layout design.

# 3. ESD Design

The smart speaker products are close to the test platform during testing, besides, they have a large LCD metal shell, which leads to a large coupling of the GND plane to bring great challenges to the ESD test. Therefore during the ESD test, there appears some abnormal problems such as LCD blur, freeze, TP touch failure, system crash, and so on. The ESD design of the product is inseparable from the structural process design, electronic system design, software design, component selection, and so on. Therefore, if the customer has high requirements for the ESD performance of the product, sufficient technology evaluation and product planning must be carried out before the product design. During the product design, it is necessary to do well not only in the selection of electronic accessories, but also in the protection design of schematic, PCB, structural process, software, and so on.

## 3.1. Schematic Diagram ESD Design

The main considerations in the schematic ESD design of R818 are as follows:

- The system function configuration pin TEST of R818 are sensitive signals, which are susceptible to interference and have the weak anti-ESD ability. Do not lead out the wiring during solution applications. If you want to lead the wiring, suggest that increase a 1-100 nF grounded capacitor.
- The freeze of the system is related to the ESD resistance of the IO. Improving the ESD ability of the input PIN at each interface will help improve the system ESD, such as HP-DET/USB-ID/CARD-DET/MIC-DET detection pin, and so on, and connecting them to the series resistors of the SoC end is beneficial to improve the ESD performance.
- The HS-MIC signal is the PIN exposed at the interface. Except for adding ESD protection devices, it is also necessary to connect to a 1-1.5 k resistors in series between HS-MIC and SoC, or a 1 nF grounded capacitor. The existing scheme directly changes the grounded capacitor of HS-MIC to 1 nF.
- When the reset signal is near the AP end, a grounded filter capacitor must be reserved and its capacitance is fixed as 1 nF. The traces should be surrounded with GND traces and kept away from interference signals.
- For the reset signal on the module, if the ESD testing fails, the module needs to be considered to add 1-100 nF grounded capacitors near the chip pin to improve the performance of ESD.
- The DP and DM signals of USB can connect to the EMI beads or 0R resistors in series to improve the performance of ESD.
- Suggest that reserve metal shields for the ESD-sensitive devices such as CPU, DRAM, and crystal.
- Suggest that add the LC filter design for the main sensitive powers.
- These interfaces directly connected to or exposed to the outside (such as the speaker, microphone, headphone, USB, TF, DCIN, and so on) must be added to the proper ESD components.

## 3.2. PCB ESD Design

NOTE

See the ESD design part of《R818_Tablet_PCB_Design Layout Guide_Vxx》for the ESD design of PCB.

## 3.3. Software ESD Design

The main considerations in the software ESD design are as follows:

- Suggest that set the unused IO port to a low level.
- The software adds a watchdog to detect and monitor the protected target status bit.
- In the case of an abnormal problem such as LCD blur, buffering, freeze, if the hardware rectification is invalid, you can consider adding the strategy of LCD soft reset.

- When TP is out of order and cannot be restored to normal, if the hardware rectification is invalid, the soft reset strategy of TP can be considered.

## 3.4. Structure Process ESD Design

The main considerations in the structure ESD design are as follows:

- For the design of the entire machine structure and assembly process, increase the effective contact area between the GND plane of the PCBA and the external metal plane, such as the LCD metal protective shell, to increase the ESD discharge plane and improve the ESD level.
- If the entire machine has an interface of the sub-board design which is connected to the mother-board through an FPC cable, it is recommended to place the interface ESD device on the sub-board, and effectively connect the sub-board and the LCD metal plane through conductive cotton to make it close to GND. Reduce ESD into the mother-board to interfere with the SOC system.
- Suggest that set aside evenly multiple more than 25 $mm^2$ GND bare copper (the copper is directly connected to the GND plane through vias) around both sides of PCB to connect to the metal plane through conductive cotton.
- The plastic inner layer is sprayed with conductive paint which is effectively connected to the GND plane to achieve the shielding effect.
- If the FPC cable of the LCD is too long and susceptible to interference, the FPC cable can be shielded with conductive cloth, or a shielded FPC cable can be used.
- The interference with the TCOM panel circuit of LCD may cause an exception for the ESD testing of LCD, you can stick the conductive cloth to shield.
- For the structure process design, the entire machine needs to be as far as possible away from the ESD-sensitive parts (such as LCD, TP) exposed outside the metal interface to reduce the risk of ESD interference.
- When the entire machine is assembled, it is necessary to ensure the effective contact between the PCBA and LCD plane to increase the discharge path of ESD.

# 4. EMI Design

At the beginning of product design, it is necessary to fully understand the clock signals in the hardware system and protect these signals to improve the EMI performance of the product and reduce the time and cost of subsequent debugging.

Table 4-1 shows the main clock frequency of each module for R818.

| Interface | Clock | Clock Frequency | Whether support spread spectrum |
|---|---|---|---|
| DDR | SCKP/SCKN | The frequency point of DDR | Support |
| TWI | TWI-SCK | 400 kHz | Support |

| Interface | Clock | Clock Frequency | Whether support spread spectrum |
|---|---|---|---|
| IIS | IIS-MCLK | 24.576 MHz、22.5792 MHz、 | Support |
| SDIO | SDC-CLK | 50 MHz、100 MHz、150 MHz | Support |
| LCD | LCD-CLK | 33 MHz、49.5 MHz、74.25 MHz | Support |
| CSI | MCLK | 24 MHz、27 MHz、37.25 MHz、74.5 MHz | Support |

Table 4-1 The Module Clock of R818

The suggestions for EMI design are as follows.

- Each interface should be designed by following the requirements of the schematic diagram and PCB design for each module.
- Suggest that the high-speed clock line on the hardware system should be in the inner layer, and the high-speed single-end clock line should be reserved the RC filter circuit to restrain the high-frequency component, and the clock line of each module should be surrounded with GND traces.
- The differential signals need to route by following the requirements of the differential pairs. If no spacing, the traces need to meet the 3W rule.
- The cable sockets must layout reasonable. No components and PCB traces under the cables as far as possible.
- If limited by the structure, the cable must be stretched very long, it is recommended that the sub-signal line of the cable seat adopts a method of two-by-two surrounding with GND traces, and the sub-board should reserve a grounding position with the metal plane of the display screen, and the cable should use the shielded cable.
- Reserve some space on the back of the PCB, and use conductive foam to contact the display panel to improve the ground loop.
- The USB and BMU share the same USB-DM/DP interface, and the resistors connected in series on the USB-DM/DP signal at the BMU end are placed near the branching point.
- Suggest that use twisted-pair lines for the speaker traces.