AXP707 PMIC Optimized For Multi-Core High-Performance System

1. Features

- 6 DCDCs
  DCDC1: 1.6-3.4V, 100mV/step, IMAX=1.5A
  DCDC2: 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM
  DCDC3: 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM
  DCDC4: 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM
  DCDC5: 0.8-1.12V, 10mV/step, 1.14-1.84V, 20mV/step, IMAX=2.5A, DVM, default set by DC5SET
  DCDC6: 0.6-1.10V, 10mV/step,1.12-1.52V, 20mV/step, IMAX=2.5A, DVM
  DCDC2 &DCDC3 can be set as dual-phase;
  DCDC5 & DCDC6 can be set as dual-phase.
  DVM(Dynamic Voltage scaling Management) ramp rate: 2.5mV/us at DCDC frequency 3MHz.
- 15 LDOs, 1 Switch
  RTCLDO: 3.0V/1.8V,IMAX=60mA
  ALDO1: 0.7~3.3V, 100mV/step, IMAX=500mA
  ALDO2: 0.7~3.3V, 100mV/step, IMAX=300mA
  ALDO3: 0.7~3.3V, 100mV/step, IMAX=200mA
  DLDO1: 0.7~3.3V, 100mV/step, IMAX=500mA
  DLDO2: 0.7~3.4V, 100mV/step; 3.4~4.2V, 200mV/step; IMAX=400mA
  DLDO3: 0.7~3.3V, 100mV/step, IMAX=300mA
  DLDO4: 0.7~3.3V, 100mV/step, IMAX=500mA
  ELDO1: 0.7~1.9V, 50mV/step, IMAX=400mA
  ELDO2: 0.7~1.9V, 50mV/step, IMAX=200mA
  ELDO3: 0.7~1.9V, 50mV/step, IMAX=200mA
  FLDO1: 0.7~1.45V, 50mV/step, IMAX=300mA
  FLDO2: 0.7~1.45V, 50mV/step, IMAX=100mA
  GPIO0LDO: 0.7~3.3V, 100mV/step, IMAX=100mA
  GPIO1LDO: 0.7~3.3V, 100mV/step, IMAX=150mA
  CHGLED: GND switch for motor or LED, IMAX=100mA
- TWSI(Two wire serial interface) supporting standard and quick slave mode, slave Address is 0x68/0x69 or 0x6A/6B by customer
- RSB(Reduced Serial Bus) supporting for Allwinner platform, slave Address is 0x01D1 or 0x0273 by customer
- Intelligent Power Select (IPS), VBUS-IPSOUT is 125mΩ typically, and ACIN-IPSOUT is 80mΩ typically.
- Adaptive Li battery PWM charger with current total up to 2.8A
- Battery Fuel Gauge and coulomb counter
- Power on/off press key
- Internal Temperature sensor and protection
- Safe and Soft start up

2. Applications

- Tablet, Smart phone, DVR, Desktop, Dongle
- UMPC-like, Student Computer

3. Description

AXP707 is customized PMIC for multi-power rails required SOC platform.

AXP707 is a highly integrated PMIC targeting at Li-battery (Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for processors to meet the increasingly complex and accurate requirements on power control.

AXP707 comes with an adaptive USB3.0 compatible Flash Charger that supports up to 2.8A charge current. It also supports 22 channels power outputs (including 6-CH DCDCs). To ensure the security and stability of the power system, AXP707 provides multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as OVP, UVP, OTP, and OCP. Moreover, AXP707 features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

In addition, AXP707 embraces a fast interface for the system to dynamically adjust output voltage and enable power outputs so that the battery life can be extended to the largest extent.

Besides, AXP707 features an IPS™ (Intelligent Power Select) circuit to transparently select power path among ACIN/USB and Li-battery to system load.

Device Information

Part Number	Package	Body Size
AXP707	QFN-68	8mm * 8mm

4. Revision History

Revision	Date	Description
V 1.0	Mar.4, 2020	Initial version
V 1.1	Aug.28, 2020	Update I_{TOLER} in Section 6.4
V 1.2	Nov.13, 2020	Update Electrical Characteristics in Section 6.4 and Baking Conditions in Section 9.5

Contents

5. Pin Configuration and Functions

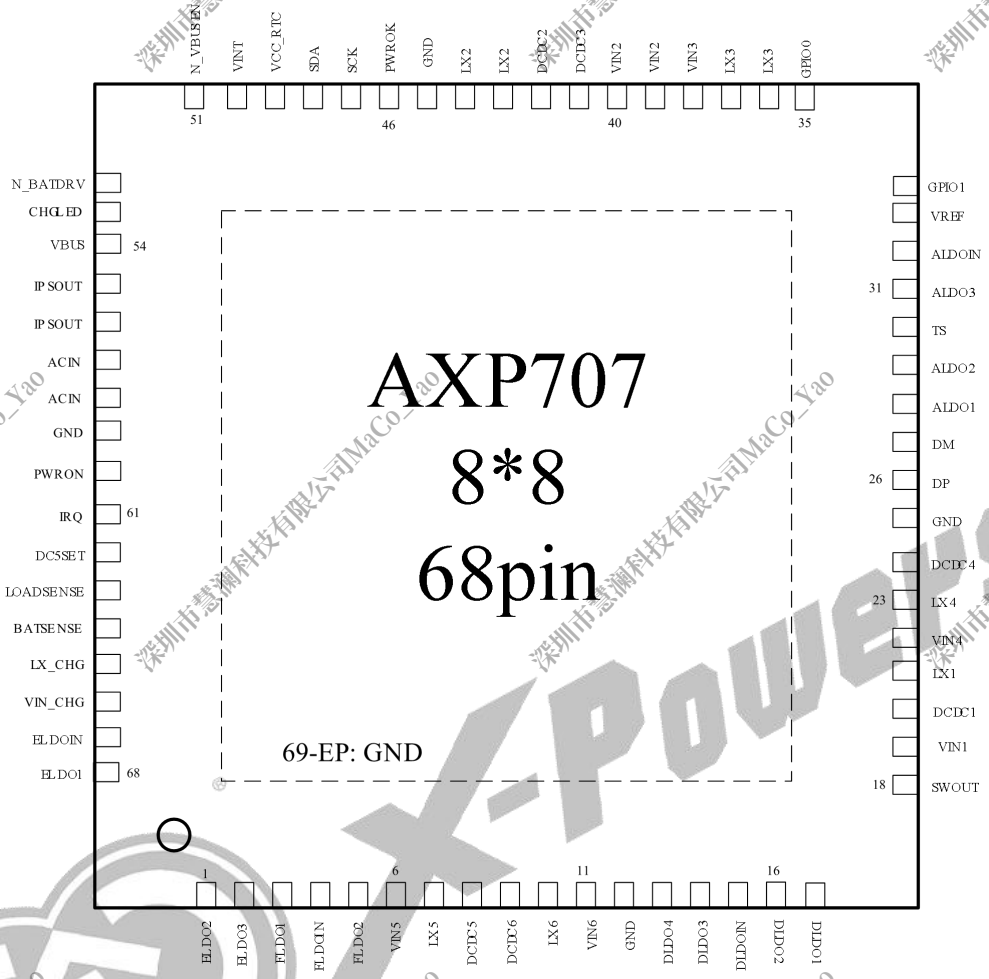


Figure 5-1 Pin Map

Table 5-1 Pin Description

No.	Name	I/O(1)	Description
1	ELDO2	O	Output pin of ELDO2
2	ELDO3	O	Output pin of ELDO3
3	FLDO1	O	Output Pin of FLDO1
4	FLDOIN	PI	FLDOs input source
5	FLDO2	O	Output Pin of FLDO2
6	VIN5	PI	DCDC5 input source
7	LX5	IO	Inductor Pin for DCDC5
8	DCDC5	I	DCDC5 feedback pin
9	DCDC6	I	DCDC6 feedback pin
10	LX6	IO	Inductor Pin for DCDC6
11	VIN6	PI	DCDC6 input source
12	GND	G	GND for internal analog circuit
13	DLDO4	O	Output Pin of DLDO4

No.	Name	I/O(1)	Description
14	DLDO3	O	Output Pin of DLDO3
15	DLDOIN	PI	DLDOs input source
16	DLDO2	O	Output Pin of DLDO2
17	DLDO1	O	Output Pin of DLDO1
18	SWOUT	O	Output pin of switch form DCDC1
19	VIN1	PI	DCDC1 input source
20	DCDC1	I	DCDC1 feedback and Switch(from DCDC1 to SWOUT) input pin
21	LX1	IO	Inductor Pin for DCDC1
22	VIN4	PI	DCDC4 input source
23	LX4	IO	Inductor Pin for DCDC4
24	DCDC4	I	DCDC4 feedback pin
25	GND	G	GND for internal analog circuit
26	DP	I	Charger detection, USB D+
27	DM	I	Charger detection, USB D-
28	ALDO1	O	Output pin of ALDO1
29	ALDO2	O	Output pin of ALDO2
30	TS	I	Battery Temperature Sensor Input or an External ADC Input
31	ALDO3	O	Output pin of ALDO3
32	ALDOIN	PI	ALDOs and internal module input source
33	VREF	O	Internal reference voltage, connect a 1uF capacitor to ground
34	GPIO1	IO	General purpose I/O or LDO by REG92H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG93H.
35	GPIO0	IO	General purpose I/O/ADC input or LDO by REG90H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG91H.
36	LX3	IO	Inductor Pin for DCDC3
37	LX3	IO	Inductor Pin for DCDC3
38	VIN3	PI	DCDC3 input source
39	VIN2	PI	DCDC2/3 input source
40	VIN2	PI	DCDC2 input source
41	DCDC3	I	DCDC3 feedback pin
42	DCDC2	I	DCDC2 feedback pin
43	LX2	IO	Inductor Pin for DCDC2
44	LX2	IO	Inductor Pin for DCDC2

No.	Name	I/O(1)	Description
45	GND	G	GND for internal analog circuit
46	PWROK	O	Power Good pin, push-pull output , and pull to VCC_RTC internal
47	SCK	I	Clock pin for serial interface, need a 2.2kΩ Pull High.
48	SDA	IO	Data pin for serial interface, need a 2.2kΩ Pull High.
49	VCC_RTC	O	Output pin of RTCLDO
50	VINT	PO	Internal logic power, 1.8V
51	N_VBUSEN	IO	VBUS select or not setting pin
52	N_BATDRV	O	BAT to PS extern PMOS driver
53	CHGLED	O	Charger status indication
54	VBUS	PI	VBUS input
55	IPSOUT	PO	System power source
56	IPSOUT	PO	System power source
57	ACIN	PI	ACIN input
58	ACIN	PI	ACIN input
59	GND	G	GND for internal analog circuit
60	PWRON	I	Power On-Off key input，Internal 100k pull high to VINT pin
61	IRQ	O	Interrupt output, open drain output, need a 10kΩ Pull High
62	DC5SET	I	Setting DCDC5 default Output Voltage, this pin must tied to GND/VINT or floating.
63	LOADSENSE	I	PWM Charger Current Sense Resistance Positive Input
64	BATSENSE	I	PWM Charger Current Sense Resistance Negative Input
65	LX_CHG	IO	Inductor Pin for PWM Charger
66	VIN_CHG	I	Charger input source
67	ELDOIN	PI	ELDOs input source
68	ELDO1	O	Output pin of ELDO1
69	EP	G	Exposed pad, connected to PCB ground

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

6. Specifications

6.1 Absolute Maximum Ratings(1)

SYMBOL	DESCRIPTION	VALUE	UNITS
VBUS/ACIN	Input Voltage Range	-0.3 to 11	V
V_{RIO1}	Voltage Range on pins IRQ, PWROK	-0.3 to 5.5	V
V_{RIO2}	Voltage Range on pins SCK, SDA, GPIO0, GPIO1, N_VBUSEN	-0.3 to IPSOUT+0.3	V
V_{RIO3}	Voltage Range on pin PWRON	-0.3 to 2.1	V
T_j	Operating Junction Temperature Range	125	℃
T_A	Operating Temperature Range	-20 to 85	℃
Ts	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads， 10sec)	260	℃

(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Maximum ESD stress voltage， Human body model(HBM)	>2000	V

6.3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS/ACIN	Input voltage	3.5	7	V

6.4 Electrical Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
ACIN						
V_{ACIN}	ACIN input voltage		3.5	**5**	7	V
I_{ACLIM}	ACIN input current limit		1500	1500	4000	mA
R_{ACIN}	Internal Ideal Diode On Resistance	ACIN to IPSOUT		80		mΩ
VBUS						
V_{VBUSIN}	VBUS Input Voltage		3.5	5	7	V
I_{BUSLIM}	VBUS input current limit		100	500	4000	mA
V_{UVLO}	VBUS Under Voltage Lockout			3.5		V
V_{OUT}	IPSOUT Output Voltage		2.9		5.0	V
R_{VBUS}	Internal Ideal Diode On Resistance	VBUS to IPSOUT		125		mΩ

Battery Charger						
V_{TRGT}	BAT Charge Target Voltage		4.1	4.2	4.35	V
I_{CHRG}	Charge Current		200	1200	2800	mA
I_{TRKL}	Trickle Charge Current			10%*I_{CHRG}		mA
V_{TRKL}	Trickle Charge Threshold Voltage			3.0		V
ΔV_{RECHG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{TARGET}		-100		mV
T_{TIMER1}	Charger Safety Timer Termination Time	Trickle Mode	40	50	70	min
T_{TIMER2}	Charger Safety Timer Termination Time	CC Mode	360	480	720	min
I_{END}	End of Charge Indication Current	CV Mode		10%*I_{CHRG} or 20%*I_{CHRG}		mA
I_{TOLER}	The tolerance of charge current	ACIN=5V, VBAT=3.4V, I_{CHRG} =1.2A	-20%		+25%	
NTC						
$V_{LTF-work}$	Cold Temperature Fault Threshold Voltage For Battery Work	Set by REG3CH	0	3.226	3.264	V
$V_{HTF-work}$	Hot Temperature Fault Threshold Voltage For Battery Work	Set by REG3DH	0	0.282	3.264	V
$V_{LTF-charge}$	Cold Temperature Fault Threshold Voltage For Battery Charge	Set by REG38H	0	2.112	3.264	V
$V_{HTF-charge}$	Hot Temperature Fault Threshold Voltage For Battery Charge	Set by REG39H	0	0.397	3.264	V
Off Mode Current						
I_{BATOFF}	OFF Mode Current	BAT=3.7V		40		μA
DCDC						
f_{OSC}	Oscillator Frequency	Default		3		MHz
L	Inductor value			1.0		μH
DCDC1						
I_{VIN1}	Input Current	PFM Mode I_{DCDC1} =0		50		μA
I_{LimDC1}	Switch Current Limit of PMOS	PWM Mode		2000		mA
I_{DCDC1}	Available Output Current	PWM Mode		1500		mA

V_{DCDC1}	Output Voltage		1.6		3.4	V
C_{OUT1}	Output capacitor value		10	10*2	66	μF
DCDC2						
I_{VIN2}	Input Current	PFM Mode I_{DCDC2} =0		50		μA
I_{LimDC2}	Switch Current Limit Per PMOS	PWM Mode		3900		mA
I_{DCDC2}	Available Output Current	PWM Mode		3000		mA
V_{DCDC2}	Output Voltage		0.5		1.3	V
C_{OUT2}	Output capacitor value		10	10*2	66	μF
DCDC3						
I_{VIN3}	Input Current	PFM Mode I_{DCDC3} =0		50		μA
I_{LimDC3}	Switch Current Limit Per PMOS	PWM Mode		3900		mA
I_{DCDC3}	Available Output Current	PWM Mode		3000		mA
V_{DCDC3}	Output Voltage		0.5		1.3	V
C_{OUT3}	Output capacitor value		10	10*2	66	μF
DCDC4						
I_{VIN4}	Input Current	PFM Mode I_{DCDC4} =0		50		μA
I_{LimDC4}	Switch Current Limit of PMOS	PWM Mode		3900		mA
I_{DCDC4}	Available Output Current	PWM Mode		3000		mA
V_{DCDC4}	Output Voltage		0.5		1.3	V
C_{OUT4}	Output capacitor value		10	10*2	66	μF
DCDC5						
I_{VIN4}	Input Current	PFM Mode I_{DCDC5} =0		50		μA
I_{LimDC5}	Switch Current Limit of PMOS	PWM Mode		3000		mA
I_{DCDC5}	Available Output Current	PWM Mode		2500		mA
V_{DCDC5}	Output Voltage	DC5SET is tied to GND	0.8		1.84	V
C_{OUT4}	Output capacitor value		10	10*2	66	μF
DCDC6						
I_{VIN6}	Input Current	PFM Mode I_{DCDC6} =0		50		μA
I_{LimDC6}	Switch Current Limit of PMOS	PWM Mode		3000		mA

I_{DCDC6}	Available Output Current	PWM Mode		2500		mA
V_{DCDC6}	Output Voltage		0.6		1.52	V
C_{OUT6}	Output capacitor value		10	10*2	66	μF
RTCLDO (always on)						
V_{RTCLDO}	Output Voltage	I_{RTCLDO}=1mA	1.8 or 3.0			V
I_{RTCLDO}	Output Current			60		mA
ALDO1						
V_{ALDO1}	Output Voltage	I_{ALDO1}=1mA	0.7		3.3	V
I_{ALDO1}	Output Current			500		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{ALDO1}=3V,f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{ALDO1}=1.8V, I_{ALDO1}=10mA		40		μVRMS
ALDO2						
V_{ALDO2}	Output Voltage	I_{ALDO2}=1mA	0.7		3.3	V
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{ALDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{ALDO2}=1.8V, I_{ALDO2}=10mA		40		μVRMS
ALDO3						
V_{ALDO3}	Output Voltage	I_{ALDO1}=1mA	0.7		3.3	V
I_{ALDO3}	Output Current			200		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{ALDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{ALDO3}=1.8V, I_{ALDO3}=10mA		40		μVRMS
DLDO1						
V_{DLDO1}	Output Voltage	I_{DLDO1}=1mA	0.7		3.3	V
I_{DLDO1}	Output Current			500		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO1}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{DLDO1}=1.8V, I_{DLDO1}=10mA		40		μVRMS
DLDO2						
V_{DLDO2}	Output Voltage	I_{DLDO2}=1mA	0.7		4.2	V

I_{DLDO2}	Output Current			400		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{DLDO2}=1.8V, I_{DLDO2}=10mA		40		μVRMS
DLDO3						
V_{DLDO3}	Output Voltage	I_{DLDO3}=1mA	0.7		3.3	V
I_{DLDO3}	Output Current			300		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{DLDO3}=1.8V, I_{DLDO3}=10mA		40		μVRMS
DLDO4						
V_{DLDO4}	Output Voltage	I_{DLDO4}=1mA	0.7		3.3	V
I_{DLDO4}	Output Current			500		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO4}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80kHz	V_{DLDO4}=1.8V, I_{DLDO4}=10mA		40		μVRMS
ELDO1						
V_{ELDO1}	Output Voltage	I_{ELDO1}=1mA	0.7		1.9	V
I_{ELDO1}	Output Current			400		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO1}=1.2V, f=1kHz		65		dB
ELDO2						
V_{ELDO2}	Output Voltage	I_{ELDO2}=1mA	0.7		1.9	V
I_{ELDO2}	Output Current			200		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO2}=1.2V, f=1kHz		65		dB
ELDO3						
V_{ELDO3}	Output Voltage	I_{ELDO3}=1mA	0.7		1.9	V
I_{ELDO3}	Output Current			200		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO3}=1.2V, f=1kHz		65		dB
FLDO1						

V_{FLDO1}	Output Voltage	I_{FLDO1}=1mA	0.7		1.45	V
I_{FLDO1}	Output Current			300		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{FLDO1}=1.2V, f=1kHz		65		dB
FLDO2						
V_{FLDO2}	Output Voltage	I_{FLDO2}=1mA	0.7		1.45	V
I_{FLDO2}	Output Current			100		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{FLDO2}=1.2V, f=1kHz		65		dB
GPIO0LDO						
$V_{GPIO0LDO}$	Output Voltage	REG90H[2:0]=011, $I_{GPIO0LDO}$=1mA	0.7		3.3	V
$I_{GPIO0LDO}$	Output Current	REG90H[2:0]=011		100		mA
I_Q	Quiescent Current	REG90H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG90H[2:0]=011 V_{GPIO0}=3V, f=1kHz		65		dB
GPIO1LDO						
$V_{GPIO1LDO}$	Output Voltage	REG92H[2:0]=011, $I_{GPIO1LDO}$=1mA	0.7		3.3	V
$I_{GPIO1LDO}$	Output Current	REG92H[2:0]=011		150		mA
I_Q	Quiescent Current	REG92H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG92H[2:0]=011 V_{GPIO1}=3V, f=1kHz		65		dB
CHGLED						
R_{CHGLED}	Internal Ideal Resistance	Supply Voltage is 0.3V		2		Ω
TWSI						
V_{CC}	Input Supply Voltage		1.8	3.3		V
Addr	TWSI Slave Address (7 bits)			0x34	0x35	
f_{SCK}	Clock Operating Frequency			400		kHz
V_{IL}	SCK/SDA Logic Low Voltage	SDA is Open drain pin			0.3*V_{CC}	V
V_{IH}	SCK/SDA Logic Low Voltage		0.7*V_{CC}			V
t_f	Clock Data Fall Time	2.2kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2kohm Pull High		100		ns
RSB						
Addr	TWSI Slave Address			0x01D1	0x0273	

VINT						
V_{INT}	Internal power supply for logic circuit			1.8		V
Related IO: PWRON						
$R_{pull-up}$	Internal resister to VINT		50	100		kΩ
V_{IL}	Logic Low Voltage			0.5		V
V_{IH}	Logic High Voltage			1.3	2.1	V
Related IO: IRQ						
V_{IL}	Logic Low Voltage	IRQ is open drain output pin, pull up to IO power (V_{IO}) by 10kΩ			0.3	V
V_{IH}	Logic High Voltage		0.7*V_{IO}		V_{IO}	V
Related IO: PWROK						
V_{IL}	Logic Low Voltage	PWROK is push-pull output pin, pull up to V_{RTCLDO} internal			0.3	V
V_{IH}	Logic High Voltage		0.7* V_{RTCLDO}		V_{RTCLDO}	V
Related IO: GPIO0						
V_{IL}	Logic Low Voltage	REG90H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG90H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG90H[2:0]=001, drive high (high level set by REG91H)	0.7	3.3	3.3	V
Related IO: GPIO1						
V_{IL}	Logic Low Voltage	REG92H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG92H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG92H[2:0]=001, drive high (high level set by REG93H)	0.7	3.3	3.3	V

7. Detail Description

7.1 Overview

AXP707 is customized PMIC for multi-power rails required SOC platform.

AXP707 is a highly integrated PMIC targeting at Li-battery (Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for processors to meet the increasingly complex and accurate requirements on power control.

AXP707 comes with an adaptive USB3.0-compatible Flash Charger that supports up to 2.8A charge current. It also supports 22 channels power outputs (including 6-CH DCDCs). To ensure the security and stability of the power system, AXP707 provides multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as OVP, UVP, OTP, and OCP. Moreover, AXP707 features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

In addition, AXP707 embraces a fast interface for the system to dynamically adjust output voltage and enable power outputs so that the battery life can be extended to the largest extent.

Besides, AXP707 features an IPS™ (Intelligent Power Select) circuit to transparently select power path among ACIN/USB and Li-battery to system load.

AXP707 is available in 8mm x 8mm 68-pin QFN package, and the package is Pb free.

7.2 Function Block Diagram

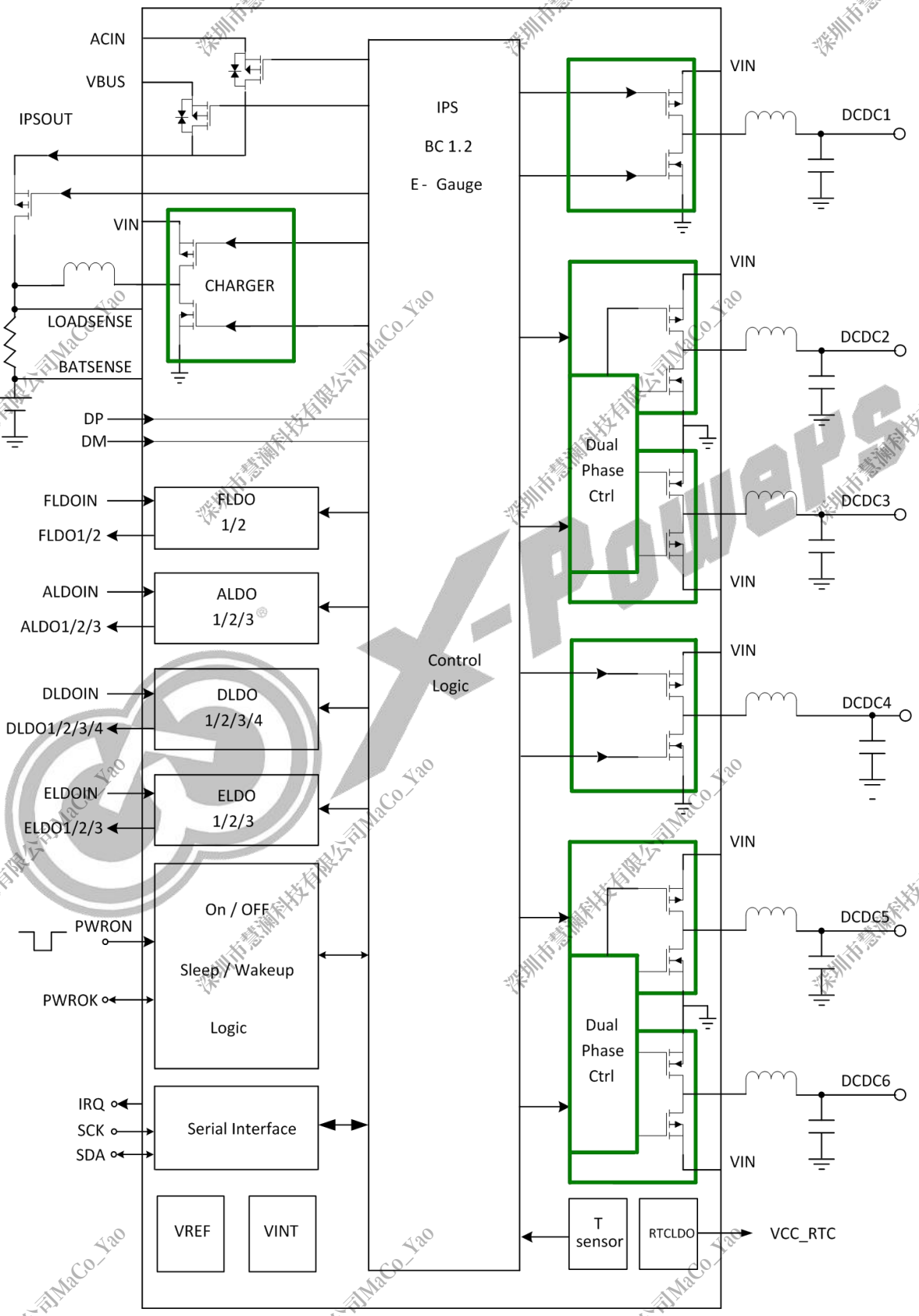


Figure 7-1 Function Block Diagram

7.3 Serial Interface Communication

When AXP707 works, the TWSI (two wire serial interface) SCK/SDA pin is pulled up to system IO power, and this interface can be used by HOST to access and adjust AXP707's working status. The RSB interface is fixed for Allwinner SOC platform.

Note that the external power hereinafter is ACIN or VBUS input.

7.4 Power on/off and Power sequences

PMIC has power off and power on status. When at off state, all voltage outputs are turned off except VCC_RTC, IPS, VINT and charger. At this time if powered by battery, the total power consumption is typically 40uA.

7.4.1 Power on/off sources

Power on source

Below are the 2 power up sources supported by AXP707 in mechanical off state:

1. Charger insertion (including ACIN and VBUS insertion); or
2. Power on key pressed

Power off source

Below are the few sources that can trigger power down of PMIC:

1. ALDOIN < V_{OFF} (indicating IPSOUT too low); or
2. Faulty condition; or
3. Power on key pressed; or
4. write 1 to REG32H[7]

Power on from charger insertion

The PMIC will start the power on sequence by a charger insertion. A charger insertion is detected from a rising voltage on the ACIN/VBUS node. If 4.1V< ACIN/VBUS < 7.0V, the charger will start charging immediately and autonomously. The existence of ACIN/VBUS is stored in REG00H[7/5].

Power on from power key pressed

The Power On Key(POK) can be connected between PWRON pin and GND of AXP707. AXP707 can automatically identify the status and then correspond respectively.

The PMIC should be able to start the power on sequence from a power on key pressed. The PMIC has a configurable timer to detect the power on key hold time. Power on key signal in AXP707 is referred as POK. Once falling edge is detected on POK, PMIC timer will start counting the hold time. POK signal has to be low for at least 32ms for it to be considered a valid signal. If the power on key hold time exceeds the timer threshold (ONLEVEL determined by REG36H [7:6]), the PMIC will start the power on sequence. Otherwise the PMIC will remain off.

Power off from ALDOIN< V_{OFF}

PMIC will constantly monitor voltage level of ALDOIN which is connected to IPSOUT. When VALDOIN < VOFF (default is 2.9V, set in REG31H[2:0]), PMIC will force shutdown. There will be 500us de-bounce circuit for ALDOIN detection and adjusted hysteresis voltage to prevent false trigger. After force shutdown occurred, PMIC will remain off and wait for power on event to boot up.

VOFF and the compensated hysteresis voltage as below:

Table 7-1 VOFF and hysteresis

V_{OFF} condition	VX condition (Hysteresis)
V_{OFF} <= 3.0V	0.3V
V_{OFF} = 3.1V	0.2V
V_{OFF} = 3.2V or 3.3V	0.1V

Power off due to faulty condition

PMIC will force shutdown once faulty event happened. Faulty event includes ACIN/VBUS>7V, PMIC internal temperature exceeds warning level3 (set in REG8FH [2]) and DCDC output drop more than 15% than the targeted output voltage (set in REG81H).

Power off by power on key pressed

Once power on key pressed, POK signal assert low and need to remain low for 32ms to be considered valid. PMIC has configurable timer to detect power on key hold time. If POK remain low for less than IRQLEVEL (set in REG36H [5:4]), POKSIRQ will be set. For POK hold time > IRQLEVEL, POKLIRQ will be set. Typically, the system uses POKLIRQ to allow user to express their demands for Host shutdown.

If POK remain low for more than OFFLEVEL (set in REG36H[1:0]), POKOIRQ will be issued. After IRQ issued, PMIC will wait for a period of time before it force shutdown (set in REG36H[3]). The PMIC can be turned on automatically (set in REG36H[2]). The waiting period is programmable from 0s to 70s(set in REG37H[2:0]).

If POK width is more than 16s, then PMIC will force shutdown immediately. This feature can be set in REG8FH[3]. When PMIC force shutdown, VCC_RTC will be shut off for 2 seconds, with 1k resistor to pull VCC_RTC to ground and then it will turn back on.

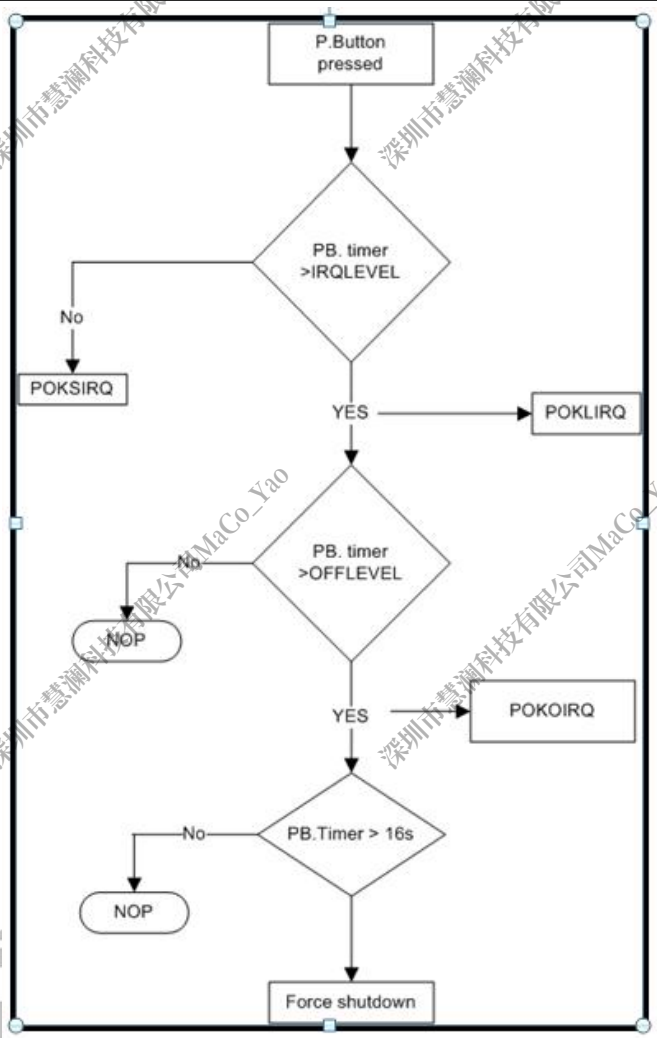


Figure 7-2 POK IRQ

Power off by write 1 to REG32H[7]

If Host write 1 to REG32H[7] of PMIC, the AXP707 will shutdown by itself. It's called soft power off.

7.4.2 Sleep and wakeup

To switch from power on mode to sleep mode, several power outputs should be disable.After that,REG31H[3] can be used to control whether following sources can be used to trigger wakeup.

1. ACIN connection/disconnection(REG40H[6:5] is set to 1);

2. VBUS connection/disconnection(REG40H[3:2} is set to 1);

3. POK press-long-key(REG44H[3] is set to 1);

4. POK negative edge(REG44H[5] is set to 1);

5. Battery low power warning Level 2(REG43H[1:0]are set to 1);

6. Detection of positive/negative edge when GPIO[1:0] functions is input (REG4CH[1:0],REG90H[7:6] and REG92H[7:6] are set to 1);

7. Software wakeup(REG31H[5] is set to 1);

8. IRQ wakeup(REG8FH[7] is set to 1);

9. Charging or Charge Done(REG41H[3:2] are set to 1).

After wakeup is triggered, each power output can be restored to default state in right power on sequence.

The Figure 7-3 is the Sleep/Wakeup control process.

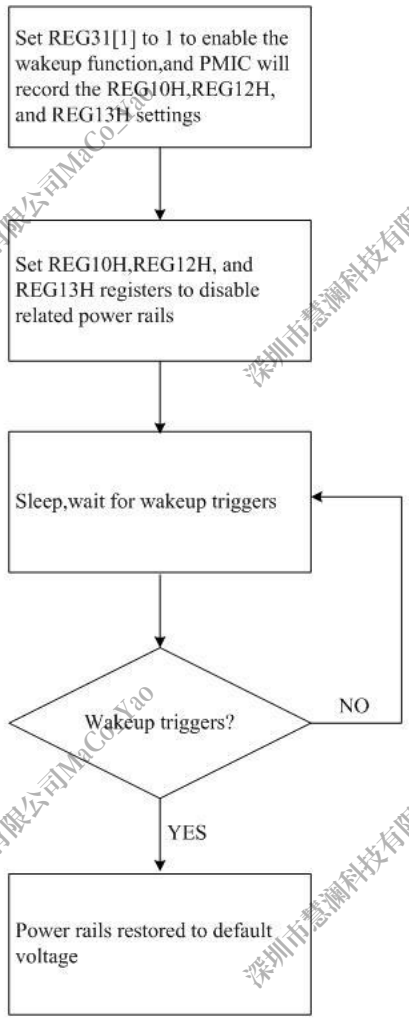


Figure 7-3 Sleep and Wakeup

7.5 IPS (Intelligent Power Select)

AXP707 has Intelligent Power Select (IPS) to select the appropriate source to power the system. The output of IPS, IPSOUT will then be used as power source for downstream regulators and battery charger. For single input power source system, the power source could be connected to ACIN and VBUS.

7.5.1 IPS overview

Input Power Sources Block Diagram

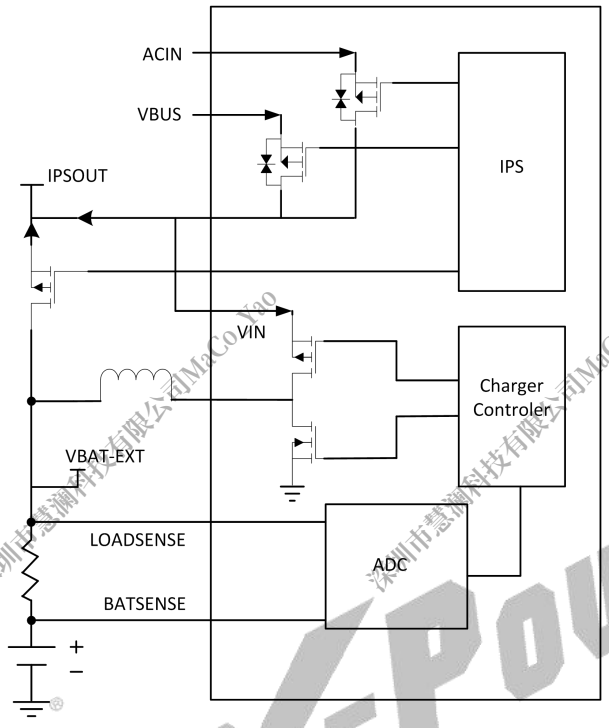


Figure 7-4 Input Power Sources Block Diagram

Single Input Power Source Connection Diagram

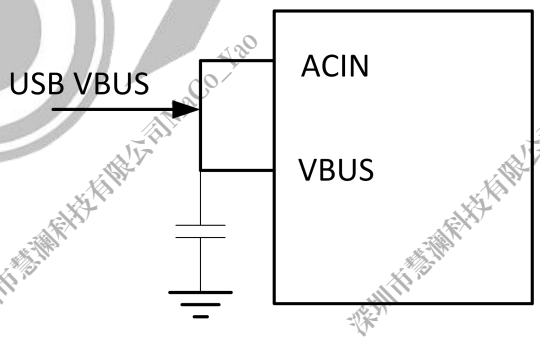


Figure 7-5 Single Input Power Source Connection Diagram

1. If only Li- Battery is available, and no external power input, Li- Battery is used for power input;
2. If external power is available (ACIN or VBUS), it is preferred in power supply;
3. If both ACIN and VBUS are available but not short together, then ACIN is preferred in power supply;
4. If both ACIN and VBUS are available and short together, they will be used at the same time;
5. If the current is still insufficient, charge current will be reduced to zero, and Battery is used for one of power sources;
6. If Li- Battery is available, it will “Seamlessly” switch to Li- Battery once external power is removed.

7.5.2 IPSOUT source selection

There are two power source, ACIN source is channeled to IPSOUT when REG3AH[7] is set to 1 (default). For

whatever reason, if ACIN source need to be disconnected from IPSOUT, set REG3AH[7] to 0. VBUS source is channeled to IPSOUT when REG30H[7] is set to 0 (default). For whatever reason, if VBUS source need to be disconnected from IPSOUT, set REG30H[7] to 1. Note that when BC Detection module is detecting, REG2CH[2] = 1, VBUS to IPSOUT channel is OFF. We can shorted ACIN and VBUS together to Reduce power path Resistor, and AXP707 can auto detect it and report it in REG00H[1].

ACIN Select Setting

Table 7-2 ACIN Select Setting

REG 3AH	Description	R/W	Default
Bit 7	ACIN path select control when ACIN valid 0: ACIN path Not selected 1: ACIN path selected	RW	1

VBUS Select Setting

Table 7-3 VBUS Select Setting

REG 30H[7]	REG 2CH[2]	VBUS_SEL
0	0	1
1	X	0
X	1	0

Table 7-4 VBUS path select control

REG 30H	Description	R/W	Default
Bit 7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path selected 1: VBUS path not selected	RW	0

Table 7-5 BC Detection status

REG 2CH	Description	R/W	Default
Bit 2	**BC_status (BC Detection status)** 1: Detecting, this bit is set when BC Detection start 0: Detection complete	RW	0

Input Source Select Setting

Table 7-6 Input Source Select Setting

VBUS_SEL	REG 00H[6]	REG 00H[4]	REG 00H[1]	IPSOUT from
×	0	0	×	VBAT-EXT
×	1	×	0	ACIN
0	0	1	×	VBAT-EXT
1	0	1	0	VBUS
1	0	1	1	VBUS

0	1	1	1	VBAT-EXT
×	1	0	1	ACIN
1	1	1	1	ACIN+VBUS

Table 7-7 Power source status

REG 00H	Description	R/W	Default
Bit 6	Indication ACIN can be used or not	R	0
Bit 4	Indication VBUS can be used or not	R	0

7.5.3 ACIN current/voltage limitation

ACIN input power source has minimum hold voltage (VHOLD) setting and current limit setting. When the input source voltage drops below its VHOLD setting, it is considered as not having sufficient power. IPS will limit the current draw automatically so that the input source voltage is hold to this minimum level.

ACIN VHOLD is set as max of VBAT+0.15V or 3AH[5:3] whereas ACIN current limit can be set through REG 3AH[2:0].

Table 7-8 ACIN path control

REG 3AH	Description	R/W	Default
Bit 5:3	ACIN VHOLD setting bit2-0 000: 4.0V; 001: 4.1V; 010: 4.2V; 011: 4.3V; 100: 4.4V; 101: 4.5V; 110: 4.6V; 111: 4.7V	RW	000
Bit 2:0	ACIN current limited setting bit2-0 000: 1.5A; 001: 2.0A; 010: 2.5A; 011: 3.0A; 100: 3.5A; 101: 4.0A; 010&011: Reserved Note: when ACIN and VBUS is shorted on PCB, the current limit is set by VBUS current limit(REG35[7:4]).	RW	000

7.5.4 VBUS current/voltage limitation

VBUS input power source has minimum hold voltage (VHOLD) setting and current limit setting. When the input source voltage drops below its VHOLD setting, it is considered as not having sufficient power. IPS will limit the current draw automatically so that the input source voltage is hold to this minimum level.

VBUS VHOLD is set as max of VBAT+0.15V or 30H[5:3] whereas VBUS current limit can be set through REG 35H[7:4].

Table 7-9 VBUS V_{HOLD} setting

REG 30H	Description	R/W	Default
Bit 5:3	VBUS V_{HOLD} setting bit 2-0 000: 4.0V; 001: 4.1V; 010: 4.2V; 011: 4.3V; 100: 4.4V; 101: 4.5V; 110: 4.6V; 111: 4.7V	RW	000

Table 7-10 VBUS current limit select

REG 35H	Description	R/W	Default
Bit 7:4	VBUS current limit select when VBUS Current limited mode is enable 0000: 100mA; 0001: 500mA; 0010: 900mA; 0011: 1500mA; 0100: 2000mA; 0101: 2500mA; 0110: 3000mA; 0111: 3500mA; 1xxx: 4000mA	RW	000

VBUS with the BC detection

For the case of battery charger detection enabled, once the USB charger detection is completed, VBUS current limit will be guided by the result of the detection. Subject to the type of USB charger detected, the current limit set in REG35H[7:4] will be auto updated by the value set in REG30H[1:0]. For example, if the BC detection result indicates SDP, the current limit in REG35H[7:4] will be set to 500mA (900mA if it is USB 3). If the detected USB charger is CDP or DCP, the current limit in REG35H[7:4] will then be updated according to the setting in REG30H[1:0].

Table 7-11 VBUS current limit according to BC detection result 1

REG 2FH[7:5]	Current limit	Description
SDP	500mA	USB connected. After communication, CPU can identify USB3.0, then change the current limit to 900mA.
Other	REG30H[1:0]	

Table 7-12 VBUS current limit according to BC detection result 2

REG 30H	Description	R/W	Default
Bit 1:0	Current limit default when BC1.2 detection result is non SDP 00: 900mA; 01: 1500mA; 10: 2000mA 11: 2500mA	RW	01

7.5.5 ACIN/VBUS input overvoltage protection

ACIN/VBUS to IPSOUT path have a regulator, target of 5.0V:

Table 7-13 ACIN/VBUS input overvoltage protection

Input power	IPSOUT	CHGLED	Contents
>7V	5V	Floating	AXP707 shutdown
>6.3V	5V	2Hz toggle	Work normally
>5.06V	5V	Charge LED	
<5.06	Vin-0.06V	Charge LED	
<3.5V	Vin-0.06V	Charge LED	Invalid

7.6 BC Detection Module

This section is primarily based on battery charging specification, for more information please refer to BC rev1.2 specifications. AXP707 is compatible with BC rev1.2 and can identify SDP/CDP/DCP except ACA The PMIC can detect the device type without software activity.

Table 7-14 BC1.2 device type

Device	Description	Compatible
SDP	Standard Downstream Port	PMIC can identify

CDP	Charging Downstream Port	PMIC can identify
DCP	Dedicated Charging Port	PMIC can identify
ACA	Accessory Charger Adapter	PMIC can't identify

Please refer to REG2FH for detailed information.

AXP707 has battery charger detection module that capable of detecting type of USB charger plug into the port. The Figure 7-6 is the battery charger detection flow.

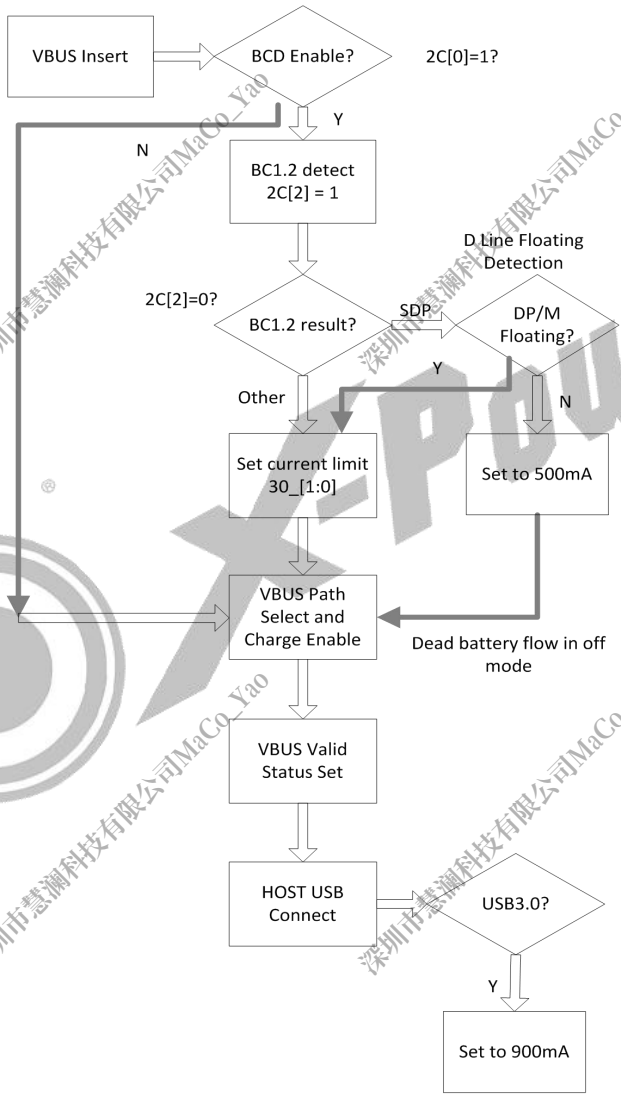


Figure 7-6 Battery charger detection flow

7.7 Adaptive PWM Charger

The AXP707 battery charger solution has two charging modes that it can be in. It is specifically designed to charge Li Ion or Li Polymer type batteries. The two modes are 1) Pre Charge Mode and 2) Fast Charge Mode. The delineation between these two modes is based on the battery voltage level of V_{TRKL} which is set at 3.0V.

When battery voltage, VBATSENSE is between 0V to 3.0V (VTRKL), the charger is in Pre Charge Mode where charging current is limited to a value of ITRKL (10% of ICHRG, default value is 120mA). This mode of operation is intended to prevent damage to the battery. Once VBATSENSE ≥ VTRKL, the charger will enter Fast Charge Mode. The Fast Charge Mode can be subdivided into two phases, namely the constant current phase (CC) and the constant voltage phase (CV). The CC phase takes place when VBATSENSE is in between VTRKL and VTRGT. It will charge with constant ICHRG. When VBATSENSE reach VTRGT, charger will operate at CV phase. At this phase, charger will charge with constant voltage of VTRGT.

7.7.1 Charger Overview

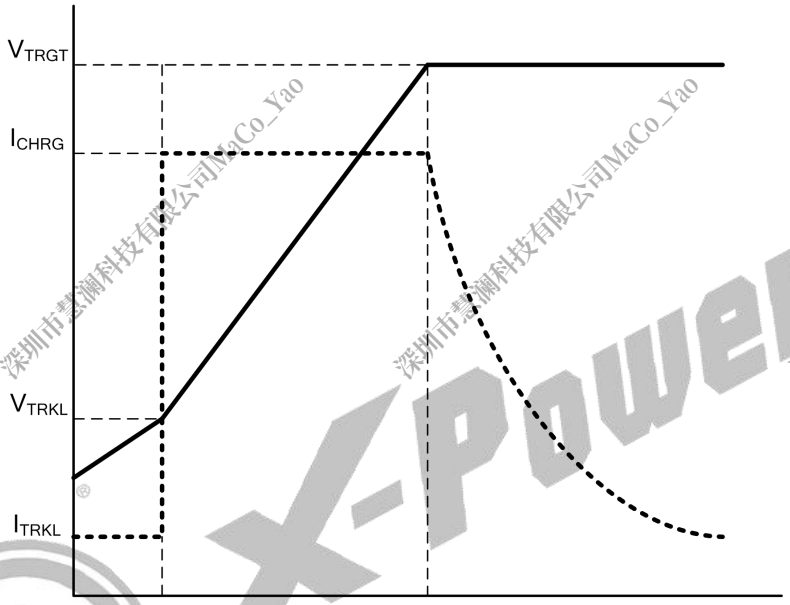


Figure 7-7 Charging process

VTRGT is programmed in REG33H[6:5] and ICHRG is in REG33H[3:0] whereas VTRKL is fixed at 3V and ITRKL is set as 10% of ICHRG.

7.7.2 Charging start and stop

When VBATSENSE is between 0V to (VTRGT-0.1V), the charge operation will start when ACIN/VBUS insert and REG 33H[7] is set to 1. The charging operation will cease when VBATSENSE is > (VTRGT-0.1V) and charging current < 10% of ICHRG.

7.7.3 Timeout activity

Refer to REG34H, there are 2 timers that can be programmed as charging expire time, REG34H[7:6] for Pre Charge and REG34H[1:0] for Fast Charge Mode. When the actual charge current is less than 20% of the ICHRG, the timer will automatically hold. When the timer expired, charger will no longer charge with programmed charging current. Instead, it will turn into safe mode. Under safe mode, charger will always charge the battery with 5mA until VBATSENSE > VTRGT – 0.1V. When the charger exits from safe mode, it will assert the IRQ. The safe mode status is reflected in REG01H[3] and SOC can get the mode status through this bit.

Table 7-15 Charger Control

REG 34H Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes;	RW	0

6	Pre-charge Timer length setting 0	10: 60 minutes; 11: 70 minutes.	RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

Table 7-16 Charger status

REG 01H	Description	R/W
Bit3	Indicate battery is in safe mode or not 0: not in; 1: in	R

There are two ways to reset or exit from safe mode. One is remove and re-insert the input power source, another is toggle charger enable bit.

7.7.4 CHGLED activity

AXP707 provides CHGLED pin. The LED connected to this pin can be used to indicate charger status and input power sources over voltage alarm. There are two Charge LED modes that can be configured through REG34H[4] if REG32H[3] is set to 1.

Table 7-17 CHGLED Mode select

REG 34H	Description	R/W	Default
Bit 4	CHGLED Mode select when REG32H[3] is 1 0: Type A; 1: Type B	RW	0

Table 7-18 CHGLED pin control

REG 32H	Description		R/W	Default
Bit 5-4	CHGLED pin control	00: Hi-Z 01: 25% 0.5Hz toggle 10: 25% 2Hz toggle 11: drive low	RW	00
Bit 3	CHGLED pin control	0: controlled by REG32H[5:4] 1: controlled by Charger	RW	0

Charge LED indicator

Table 7-19 Charge LED indicator

CHGLED pin	Mode A	Mode B
Z (tri-state)	Not charging	Not charging due to 1: no external power source; or 2: external power source is insufficient and battery is discharging
25% duty 1Hz (Z/Low)	Abnormality alarm due to 1: charger timeout; or 2: IC temperature > warning level 2	Charging
25% duty 4Hz (Z/Low)	Overvoltage alarm (VBUS > 6.3V)	Alarm due to 1: VBUS > 6.3V; or

		2: charger timeout; or 3: IC temperature > warning level 2
Low	Charging	Not charging due to battery is fully charged

7.7.5 Battery detection

When the VBATSENSE<2.2V, AXP707 judge it as battery is not present. When VBATSENSE goes higher than 2.2V, it indicates battery present or is inserted. For the case of battery insertion or removal, IRQ will be asserted. Battery presence status is indicated in REG01H[5]and the battery detection function can be set by REG32H[6]. When charger insert, AXP707 will send a pulse to detect battery is present or not per 16 seconds.

7.7.6 Temperature protection

AXP707 has built in thermal protection for the IC itself with 3 levels of warning. Each warning level has 6.8˚C different in threshold compare to the next level and each warning level has hysteresis gap of 13.6˚C. Below are the charger responses with respect to each thermal warning level.

Table 7-20 Response for thermal warning

Warning	AXP707 Response
Level 1	Once the IC temperature exceeds this level, charger will charge at minimum charging current. If REG35[3]=1, the charger will stop charging. When IC temperature drops below hysteresis limit, charger will automatically go back to its original charging state.
Level 2	If IC temperature continue to rise and exceeds this level, charger will continue to charge at minimum charging current. Charge LED will provide indication according to **Table 7-19**. If IRQ is enabled in REG43H[7], IRQ will be asserted and its status can be read from REG01H[7].
Level 3	If IC temperature exceeds this level, all the behavior is the same as level 2 but if REG8FH[2] is set to 1, IC will automatically shut down.

Table 7-21 Warning level 2 IRQ enable

REG 43H	Description	R/W	Default
Bit7	The PMIC temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0

Table 7-22 PMIC die over temperature indication

REG 01H	Description	R/W	Default
Bit7	Indication PMIC die over temperature or not 0: not over temperature; 1: over temperature	R	0

Table 7-23 Over temperature shut down control

REG 8FH	Description	R/W	Default
Bit 2	The PMIC shut down or not when Die temperature is over the warning level 3 0: not shut down; 1: shut down	RW	0

Beside built in IC thermal protection, AXP707 has the capability to sense one external thermal sensor (for battery temperature) through TS pin.

Block Diagram for Battery Temperature Measurement

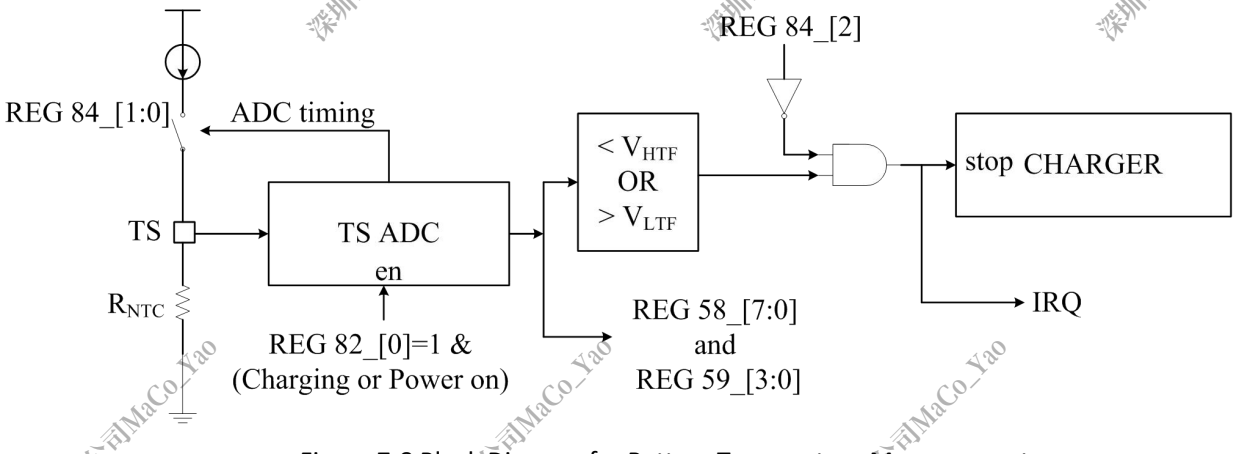


Figure 7-8 Block Diagram for Battery Temperature Measurement

AXP707 has built in current source that can be used to inject to external thermal sensor thru TS pin for temperature reading. This current source has 4 level of current which can be programmed through REG84H[5:4]. By default, the current source will only be injected when ADC is going to read the temperature data. The ADC to read TS pin input is enabled by setting REG82H[0] to 1. However the current source switch can be programmed to always OFF or ON or only ON when charger is charging through REG84H[1:0].

Table 7-24 TS pin control

REG 84H	Description	R/W	Default
Bit 5-4	Current source from TS pin control 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA	RW	11
Bit1-0	Current source from TS pin on/off enable bit [1:0] 00: off; 01: on when charging battery, off when not charging; 10: on in ADC phase and off when out of the ADC phase, for power saving; 11: always on Note: TS pin and GPIO0ADC pin are same current source, so if set the TS current source is always on, the GPIO0ADC is invalid	RW	10

Table 7-25 TS pin input to ADC enable

REG 82H Bit	Description		R/W	Default
0	TS pin input to ADC enable	0: off, 1: on	RW	0

When the current source is injected to thermal sensor (NTC), it will create a voltage drop across NTC and this voltage will be read by 12 bits ADC thru TS pin. The 12 bits code output of the ADC will then be stored in REG58H (HSB 8) & REG59H (LSB 4). The relation of TS pin voltage to 12 bits ADC output code is as below:

12 bits ADC output code = R_NTC(Ω) * REG84[5:4](μA) / (0.8 * 1000)

Table below is the example by using 10K NTC from Murata (NCP15XH103F03R).

Table 7-26 Relationship among temperature, equivalent resistance, detected voltage and ADC data

Temperature (˚C)	R_NTC (Ω)	TS Pin Voltage (V)	12 bits ADC output code	
			REG 58H[7:0]	REG 59H[3:0]
-10	40260	3.221	FBH	AH
0	26490	2.119	A5H	8H
25	10000	0.800	3EH	8H
40	5840	0.467	24H	7H
45	4924	0.394	1EH	CH
55	3550	0.284	16H	3H

There are 2 battery over temperature (OTP) and 2 under temperature (UTP) thresholds can be set to protect the battery by either controlling the charger or shutdown the system. The first level OTP & UTP thresholds are programmed by REG38H & REG39H. The second level OTP & UTP threshold are programmed by REG3CH & REG3DH. When battery temperature is higher or lower than the first level OTP or UTP threshold, IRQ is asserted, charger will stop charging and REG01H[6] change to 0 to reflect the status. When battery temperature is higher or lower than the second level OTP or UTP threshold, IRQ is asserted. System may or may not shutdown subject to SW decision. There is a hysteresis of 460.8 mV(refer to TS pin voltage) for UTP threshold, and there is a hysteresis of 57.6 mV for OTP threshold. Every time when the battery temperature comes out from first level over or under temperature, IRQ is asserted. Charger restores the original charging state and REG01H[6] change to 1. In normal case, first level of OTP & UTP thresholds should be set within the second level OTP & UTP thresholds.

The setting of using TS pin current source is showed in the following table:

Table 7-27 Setting of using TS pin current source

Usage condition	setting	Key point
Don't need temperature protection	TS = GND，REG84H[1:0] = 00，（default 00），REG84H[2] = 1	TS work as GPADC
Temperature protection when in charger	REG84H[1:0] = 01	Current source on when charging
Temperature protection when in charging and discharging	REG84H[1:0] = 10	
TS for GPADC or GPIO	REG84H[1:0] = 11 when need current source REG84H[1:0] = 00 when not need current source	

Logic Table：

Table 7-28 Logic Table

REG84H[2] Function	**REG82H[0] ADC Enable**	**REG84H[1:0] Current**	**Work mode**	**IRQ**	**Note**
0	0	xx	TS	NO	
0	1	00	TS	NO	

0	1	01	TS	IRQ when in Charging	all IRQ work
0	1	10/11	TS	IRQ all times	
1	0	xx	GPADC	NO	TS function disable

7.8 Multi-Power Outputs

DCDC1~6 are dual mode (PFM / PWM), by default is auto switch mode. All DCDC and PWM charger are synchronized with frequency of 3MHz (with spread spectrum option), hence small value external inductors and capacitors components can be used.

All DCDC and LDO have current limiting protection function. When the load current exceeds the current limit, the output voltage will drop. Meanwhile, all of the DCDC output voltage will be monitored. If the DCDC output voltage is 15% lower than the set value and DCDC 85% low voltage turn off PMIC function (REG81H) is enabled, PMIC will automatically force a shutdown and PWROK pin becomes low. DCDC output voltage monitor de-bounce time setting is available at REG8EH[7:6].

DCDC2~6 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. If the application does not require use of any DCDC, the LX pin can be left floating while VIN and PGND need to be connected. PMIC will automatically detect this state to turn off the DCDC.

Table 7-29 Features of Multi-Power Outputs

Power Rails	Input	Voltage Range	AXP707 Default Voltage	Max Current	Default State	Application Example
DCDC1	IPSOUT	1.6~3.4V	3.3V	1.5A	on	VCC-IO
DCDC2	IPSOUT	0.5~1.3V	0.9V	3.0A	on	VDD-CPU
DCDC3	IPSOUT	0.5~1.3V	0.9V	3.0A	on	VDD-CPU
DCDC4	IPSOUT	0.5~1.3V	0.9V	3.0A	on	VDD-SYS
DCDC5	IPSOUT	0.8~1.84V	1.5/1.36/1.24V	2.5A	on	VCC-DRAM
DCDC6	IPSOUT	0.6~1.52V	0.9V	2.5A	on	
ALDO1	IPSOUT	0.7~3.3V	1.8	0.5A	on	AVCC
ALDO2		0.7~3.3V	1.8	0.3A	on	VCC18-LPDDR
ALDO3		0.7~3.3V	3.3V	0.2A	on	VCC-USB
DLDO1	IPSOUT Or Others	0.7~3.3V	3.3V	0.5A	off	
DLDO2		0.7~4.2V	/	0.4A	off	
DLDO3		0.7~3.3V	/	0.3A	off	
DLDO4		0.7~3.3V	/	0.5A	off	
ELDO1	IPSOUT Or Others	0.7~1.9V	1.8V	0.4A	on	VCC-PC
ELDO2		0.7~1.9V	/	0.2A	off	
ELDO3		0.7~1.9V	/	0.2A	off	
FLDO1	IPSOUT Or Others	0.7~1.45V	0.9V	0.3A	on	VDD-CPUS
FLDO2		0.7~1.45V	0.8V	0.1A	off	
GPIO0LDO	IPSOUT	0.7~3.3V	/	0.1A	off	

GPIO1LDO		0.7~3.3V	/	0.15A	off	
VINT	IPSOUT	Fixed 1.8V	Fixed 1.8V	100mA	Always on	PMIC Internal
RTCLDO		Fixed 3.0 or 1.8V	Fixed 1.8V	60mA	Always on	VCC-RTC

Both VINT and RTCLDO input from IPSOUT. As long as any of the ACIN/VBUS or BAT power exists, they will not power down. VINT output is fixed at 1.8V, while VCC_RTC is fixed at 1.8V too for AXP707.

7.9 ADC

PMIC has a 12Bit SAR ADC. The ADC input range is 0V to 2.0475V, with is 0.5mV/step. Voltage and current ADC has sampling frequency option of 800/400/200/100Hz. The relationship between input signal and data is listed below:

Table 7-30 ADC signal and data

Channel function	**000H**	**STEP**	**FFFH**	**Condition**
BAT voltage (BATSENSE)	0mV	1.1mV	4.5045V	Power On
Current offset	0mA	1mA	4.095A	Charging or power on
BAT discharge current	0mA	1mA	4.095A	Power on
Internal temperature	-267.7+0.10625*xxxH (℃)			Charging or Power on
BAT charge current	0mA	1mA	4.095A	Charging or Power on
TS pin input	0mV	0.8mV	3.276V	Charging or Power on
GPIO0 pin input	0mV	0.8mV	3.276V	Power On

Current ADC measured the current through the 10mohm resistor between BATSENSE and LOADSENSE. For internal temperature, internal logic will do the ADC data comparison with register set warning level for sending over-temperature alarm or shutdown. To identify the battery current direction, the charge current and discharge current value will be compare base on status of charger enable, battery present and VBUS present indication.

7.10 Fuel Gauge

The Fuel Gauge comprises 3 modules – Rdc calculation module; OCV (Open Circuit Voltage) and Coulomb counter module; and calibration module. The Fuel Gauge system is able to export information about battery to application such as Battery capacity percentage (REGB9H), Battery Voltage (REG78H, REG79H), Battery charging current (REG7AH, REG7BH), Battery discharge current (REG7CH, REG7DH), Battery maximum capacity (REGE0H, REGE1H), Battery Rdc value (REGBAH, REGBBH). The Fuel Gauge can be enabled or disabled via REGB8H. The Battery low warning can be set in REGE6H, and IRQ (REG4BH) will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set in REGE6H.

Once a default battery is selected for a particular design, it is highly recommended to calibrate the battery to achieve better Fuel Gauge accuracy. The calibration procedure is documented in separate Application Guide – **AXP707 Battery Calibration Application Guide**. Once the calibration data are available, user can write the calibration info to REG C0~DFH (OCV percentage table) on each boot. Or user can choose not to do the calibration and use the default OCV percentage value. Additionally, the Fuel Gauge system is capable to learn the battery characteristic on each Full charge cycle. Information such as Battery Maximum capacity (REGE0H, REGE1H) and Rdc (REGBAH, REGBBH) will be updated automatically over time.

OCV Percentage Table

Table 7-31 OCV Percentage Table

Reg Address	Percent	OCV
	0	2.9920
C0	RW(H)	3.1328
C1	RW(H)	3.2736
C2	RW(H)	3.3440
C3	RW(H)	3.4144
C4	RW(H)	3.4848
C5	RW(H)	3.5552
C6	RW(H)	3.5904
C7	RW(H)	3.6080
C8	RW(H)	3.6256
C9	RW(H)	3.6432
CA	RW(H)	3.6608
CB	RW(H)	3.6960
CC	RW(H)	3.7312
CD	RW(H)	3.7664
CE	RW(H)	3.8016
CF	RW(H)	3.8192
D0	RW(H)	3.8368
D1	RW(H)	3.8544
D2	RW(H)	3.8720
D3	RW(H)	3.9072
D4	RW(H)	3.9424
D5	RW(H)	3.9776
D6	RW(H)	4.0128
D7	RW(H)	4.0480
D8	RW(H)	4.0832
D9	RW(H)	4.1184
DA	RW(H)	4.1360
DB	RW(H)	4.1536
DC	RW(H)	4.1888
DD	RW(H)	4.224
DE	RW(H)	4.2592
DF	RW(H)	4.2944
	100	4.3296

7.11 Interrupt Controller

PMIC Interrupt Controller monitors such as low power, bad battery, PWRON pin signal, over temperature, GPIO input edge signals such as trigger events. When the events occur, corresponding IRQ status will be set to 1, and will drive IRQ pin (NMOS open drain) asserted low. When host detect triggered IRQ signal, host will scan through the trigger events and respond accordingly. Meanwhile, Host will reset the IRQ status by writing '1' to status bit. Host will always check every IRQ status from time to time and only will take effect with respective relevant enabled IRQ bit only.

The input edge IRQ of GPIO will only functions when GPIO pin is set as Digital input, and the function will take

effect when input edge IRQ is enable . The input will go through about 1ms of de-bounce and corresponding IRQ will trigger when detect rising and falling edge. Rising, falling, or both edge triggering is control by corresponding IRQ register bit.

7bits event timer will issue timeout IRQ. Clearing IRQ does not start counter.

7.12 TWSI

The PMIC is compatible with a host-controlled environment, functioned as a slave port enabling serial interface compatible hosts to write to or read from internal registers. The PMIC only responds (ACK) to address 68H/69H.(The slave address can be ordered to 6A/6BH)

Table 7-32 TWSI address

BYTE	BIT							
	MSB	6	5	4	3	2	1	0
WRITE	0	1	1	0	1	0	0	0
READ	0	1	1	0	1	0	0	1
I/O DATA BUS	B7	B6	B5	B4	B3	B2	B1	B0

Incremental Read

The PMIC supports incremental read operations in normal TWI mode. The address increases by 1 automatically.

RSB

The PMIC supports RSB interface for Allwinner platform. The slave address is 0x01D1 or 0x0273.

7.13 Register

7.13.1 Register List

Address	Description	R/W	Default
00	Power source status	R	
01	Power mode and Charger status	R	
02	Power up/down reason register	RW	
03	IC type number	R	8'b01xx0001
04-0F	12 Data buffers	RW	00H
10	Output power on-off control 1	RW	3FH
12	Output power on-off control 2	RW	01H
13	Output power on-off control 3	RW	E4H
14	On/Off synchronous control	RW	08H
15	DLDO1 voltage control	RW	1AH
16	DLDO2 voltage control	RW	16H
17	DLDO3 voltage control	RW	16H
18	DLDO4 voltage control	RW	1AH
19	ELDO1 voltage control	RW	16H

1A	ELDO2 voltage control	RW	00H
1B	ELDO3 voltage control	RW	00H
1C	FLDO1 voltage control	RW	04H
1D	FLDO2 voltage control	RW	02H
20	DCDC1 voltage control	RW	11H
21	DCDC2 voltage control	RW	A8H
22	DCDC3 voltage control	RW	A8H
23	DCDC4 voltage control	RW	A8H
24	DCDC5 voltage control	RW	B3H
25	DCDC6 voltage control	RW	9EH
27	DCDC2~6 DVM control	RW	FCH
28	ALDO1 voltage control	RW	0BH
29	ALDO2 voltage control	RW	0BH
2A	ALDO3 voltage control	RW	1AH
2C	BC Module Global Register	RW	00H
2D	BC Module VBUS Control and Status Register	RW	30H
2E	BC USB Status Register	RW	40H
2F	BC Detect Status Register	R	20H
30	VBUS path control & Hold voltage setting	RW	01H
31	Power wakeup control & V_{OFF} setting	RW	03H
32	Power Disable, BAT detect and CHGLED pin control	RW	43H
33	Charger Control 1	RW	C5H
34	Charger Control 2	RW	45H
35	Charger Control 3	RW	18H
36	POK setting	RW	59H
37	POK Power off activity time setting	RW	00H
38	$V_{LTF\text{-}charge}$ setting	RW	A5H
39	$V_{HTF\text{-}charge}$ setting	RW	1FH
3A	ACIN path control	RW	80H
3B	DCDC frequency setting	RW	08H
3C	$V_{LTF\text{-}work}$ setting	RW	FCH
3D	$V_{HTF\text{-}work}$ setting	RW	16H
3E	Interface mode select	RW	00H
40	IRQ enable 1	RW	D8H
41	IRQ enable 2	RW	FCH
42	IRQ enable 3	RW	FFH
43	IRQ enable 4	RW	03H
44	IRQ enable 5	RW	7CH
45	IRQ enable 6	RW	00H
48	IRQ Status 1	RW	00H
49	IRQ Status 2	RW	00H
4A	IRQ Status 3	RW	00H

4B	IRQ Status 4	RW	00H
4C	IRQ Status 5	RW	00H
4D	IRQ Status 6	RW	00H
58	TS pin input ADC data, highest 8bit	R	00H
59	TS pin input ADC data, lowest 8bit	R	00H
5A	GPIO0 pin input ADC data, highest 8bit	R	00H
5B	GPIO0 pin input ADC data, lowest 8bit	R	00H
78	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00H
79	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00H
7A	Average data bit[11:4] for Battery charge current	R	00H
7B	Average data bit[3:0] for Battery charge current	R	00H
7C	Average data for Battery discharge current highest 8 bit	R	00H
7D	Average data for Battery discharge current lowest 4 bit	R	00H
80	DCDC PWM/PFM mode select	RW	80H
81	Off-Discharge and Output monitor control	RW	80H
82	ADC Enable	RW	E1H
84	ADC speed setting, TS pin Control	RW	F2H
85	ADC speed setting	RW	B0H
8A	Timer control	RW	00H
8E	DCDC output voltage monitor de-bounce time setting	RW	40H
8F	IRQ pin, hot-over shut down	RW	00H
90	GPIO0(GPADC) control	RW	07H
91	GPIO0LDO and GPIO0 high level voltage setting	RW	1AH
92	GPIO1 control	RW	07H
93	GPIO1LDO and GPIO1 high level voltage setting	RW	1AH
94	GPIO signal bit	R	00H
97	GPIO pull down control	RW	00H
A0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00H
A1	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00H
B8	Fuel Gauge Control	RW	C0H
B9	Battery capacity percentage for indication	R	64H
BA	RDC 1	RW	80H
BB	RDC 0	RW	5DH
BC	OCV 1	R	00H
BD	OCV 0	R	00H
E0	Battery maximum capacity	RW	00H
E1	Battery maximum capacity	RW	00H
E2	Coulomb meter counter	RW	00H
E3	Coulomb meter counter	RW	00H
E4	OCV Percentage of battery capacity	R	64H
E5	Coulomb meter percentage of battery capacity	R	64H
E6	Battery capacity percentage warning level	RW	A0H

E8	Fuel gauge tuning control 0	RW	00H
E9	Fuel gauge tuning control 1	RW	00H
EA	Fuel gauge tuning control 2	RW	00H
EB	Fuel gauge tuning control 3	RW	00H
EC	Fuel gauge tuning control 4	RW	00H
ED	Fuel gauge tuning control 5	RW	00H

7.13.2 Register Description

Note: hereinafter, "system reset" means that the Register will be reset when the PMIC power off, and "power on reset" means that the Register will be reset when IPSOUT voltage drop below 2.1V .

REG 00H: Power source status

Bit	Description	R/W
7	ACIN presence indication 0: ACIN not presence (ACIN<3.5V) 1: ACIN presence (ACIN>4.1V)	R
6	Indication ACIN can be used or not	R
5	VBUS presence indication 0: VBUS not presence (VBUS<3.5V) 1: VBUS presence (VBUS>4.1V)	R
4	Indication of VBUS valid (VBUS_Val) and VBUS can be selected	R
3	VBAT>3.5V or not 0: not; 1: yes	R
2	Indication Battery current direction 0: Battery discharge; 1: battery Charging	R
1	Indication ACIN and VBUS are shorted or not on PCB, IN_SHORT status 0: not; 1: yes	R
0	STARTUP_TRIGGER: indicate the startup trigger is ACIN/VBUS or not 0: not; 1: yes	R

REG 01H: Power mode and Charger status

Bit	Description	R/W
7	Indication PMIC die over temperature or not 0: not over temperature; 1: over temperature	R
6	Charging indication 0: Charger is not charging or charging is done; 1: Charger is charging	R
5	Battery presence indication 0: No Battery is connected to AXP707; 1: Battery is connected	R
4	REG 01H[5] valid flag 0: REG 01H[5] is invalid 1: REG 01H[5] is valid Indicate whether Battery detected or not yet	R
3	Indicate battery is in safe mode or not 0: not in; 1: in	R
2-0	Reserved	R

REG 02H: Power up/down reason register

Reset: Power on reset

Bit	Description	R/W	Default
7	Power on key override was the shutdown reason, write 1 to clear	R/W	0
6	Reserved	R/W	0
5	PMIC UVLO threshold was the shutdown reason, write 1 to clear	R/W	0
4	Reserved	R/W	0
3	Reserved	R/W	0
2	Battery insertion was the start up reason, write 1 to clear	R/W	0
1	Charger insertion was the start up reason, write 1 to clear	R/W	0
0	Power on key was the start up reason, write 1 to clear	R/W	0

REG 03H: IC type no.

Default: 8'b01xx0001 (Note: bit4&5 is uncertain)

Bit	Description	R/W
5-4	Reserved	R
7-6 & 3-0	IC type No. 010001: IC is AXP707 Others: Reserved	R

REG 04-0FH: 12 Data buffers

Default: 00H

Reset: Power on reset

Note: As long as one of the external powers, batteries or backup batteries exists, this data will be reserved and free from the startup and shutdown influence.

REG 10H: Output power on-off control 1

Default：3FH (Note: bit0~5 by default is customized)

Reset: system reset

Bit	Description		R/W	Default
7-6	Reserved			
5	DCDC6 on-off control	0: off; 1: on	RW	1
4	DCDC5 on-off control	0: off; 1: on	RW	1
3	DCDC4 on-off control	0: off; 1: on	RW	1
1	DCDC3 on-off control	0: off; 1: on	RW	1
1	DCDC2 on-off control	0: off; 1: on	RW	1
0	DCDC1 on-off control	0: off; 1: on	RW	1

REG 12H: Output power on-off control 2

Default：01H (Note: bit0/3~6 by default is customized)

Reset: system reset

Bit	Description		R/W	Default
7	DC1SW on-off control	0: off; 1: on	RW	0
6	DLDO4 on-off control	0: off; 1: on	RW	0
5	DLDO3 on-off control	0: off; 1: on	RW	0
4	DLDO2 on-off control	0: off; 1: on	RW	0

3	DLDO1 on-off control	0: off; 1: on	RW	0
2	ELDO3 on-off control	0: off; 1: on	RW	0
1	ELDO2 on-off control	0: off; 1: on	RW	0
0	ELDO1 on-off control	0: off; 1: on	RW	1

REG 13H: Output power on-off control 3

Default： E4H (Note: bit2~3/5~7 by default is customized)

Reset: system reset

Bit	Description		R/W	Default
7	ALDO3 on-off control	0: off; 1: on	RW	1
6	ALDO2 on-off control	0: off; 1: on	RW	1
5	ALDO1 on-off control	0: off; 1: on	RW	1
4	Reserved			
3	FLDO2 on-off control	0: off; 1: on	RW	0
2	FLDO1 on-off control	0: off; 1: on	RW	1
1-0	Reserved			

REG 14H: On/Off synchronous control

Default： 08H (Note: bit5&6 by default is customized)

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6	DCDC2&3 poly-phase control 0: DCDC2&3 is independent, not poly-phase DCDC 1: DCDC2&3 is Dual-phase DCDC	RW	0
5	DCDC5&6 poly-phase control 0: DCDC5&6 is independent, not poly-phase DCDC 1: DCDC5&6 is Dual-phase DCDC	RW	0
4-2	Reserved	RW	010
1	Power control register select 1: select buffer register, output value of control register to buffer 0-select the control register	RW	0
0	Outport buffer register value 1: outport to control register from buffer Bit[1:0], self clear to 0 after outport	RW	0

REG 15H: DLDO1 voltage control

Default： 1AH (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V 0.7V-3.3V, 100mV/step	RW	1AH

REG 16H: DLDO2 voltage control

Default： 16H

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.4V, 100mV/step 3.4V-4.2V, 200mV/step	RW	16H

REG 17H: DLDO3 voltage control

Default：16H

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.3V, 100mV/step	RW	16H

REG 18H: DLDO4 voltage control

Default：1AH

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V 0.7V-3.3V, 100mV/step	RW	1AH

REG 19H: ELDO1 voltage control

Default：16H (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 1.8V 0.7-1.9V, 50mV/step	RW	16H

REG 1AH: ELDO2 voltage control

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 0.7V 0.7-1.9V, 50mV/step	RW	00000

REG 1BH: ELDO3 voltage control

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 0.7V 0.7-1.9V, 50mV/step	RW	00000

REG 1CH: FLDO1 voltage control

Default：04H (Note: bit0~3 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	RW	000
3-0	voltage setting Bit 3-0, default is 0.9V 0.7-1.45V, 50mV/step	RW	04H

REG 1DH: FLDO2 voltage control

Default：02H (Note: bit0~3 by default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3-0	FLDO2 voltage setting Bit 3-0, default is 0.8V 0.7-1.45V, 50mV/step	RW	02H

REG 20H: DCDC1 voltage control

Default：11H (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, 1.6-3.4V, 100mV/step, default is 3.3V	RW	11H

REG 21H: DCDC2 voltage control

Default：A8H (Note: bit0~6 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 0.9V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	28H

REG 22H: DCDC3 voltage control

Default：A8H (Note: bit0~6 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 0.9V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	28H

REG 23H: DCDC4 voltage control

Default：A8H (Note: bit0~6 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 0.9V 0.50-1.20V：10mV/step	RW	28H

	1.22-1.30V：20mV/step		

REG 24H: DCDC5 voltage control

Default：B3H (DC5SET is tied to GND and in type 0. Note: type 0 or 1 is customized)

Reset: System reset

Bit	Description	R/W	Default			
7	DVM finished or not status bit 0: not finished 1: finished	R	1			
6-0	voltage setting Bit 6-0 0.80-1.12V：10mV/step 1.14-1.84V：20mV/step	RW	DC5SET is tied to :	GND	VINT	Floating
			Type 0	1.5V	1.36V	1.24V
			Type 1	0.9V	1.8V	1.0V

REG 25H: DCDC6 voltage control

Default：9EH (Note: bit0~6 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 0.9V 0.60-1.10V: 10mV/step 1.12-1.52V: 20mV/step	RW	1EH

REG 27H: DCDC2~6 DVM control

Default：FCH

Reset: System reset

Bit	Description	R/W	Default
7	Reserved	RW	1
6	DCDC6 DVM on-off control 0: disable; 1: enable	RW	1
5	DCDC5 DVM on-off control 0: disable; 1: enable	RW	1
4	DCDC4 DVM on-off control 0: disable; 1: enable	RW	1
3	DCDC3 DVM on-off control 0: disable; 1: enable	RW	1
2	DCDC2 DVM on-off control 0: disable; 1: enable	RW	1
1-0	Reserved	RW	00

REG 28H: ALDO1 voltage control

Default：0BH (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 1.8V 0.7-3.3V, 100mV/step	RW	0BH

REG 29H: ALDO2 voltage control

Default：0BH (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 1.8V 0.7-3.3V, 100mV/step	RW	0BH

REG 2AH: ALDO3 voltage control

Default：1AH (Note: bit0~4 default is customized)

Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V 0.7-3.3V, 100mV/step	RW	1AH

REG 2CH: BC Module Global Register

Default：00H

Reset: bit7 is system reset, bit[6:0] Power On reset

Bit	Description	R/W	Default
7	**DCD_SEL(DCD Detect Select)** Software writes 1 to this bit to select DCD Detection during BC Detect.	RW	0
6-5	**DCD_TIMEOUT_CTL(DCD Timeout Control)** Software writes these fields to configure the DCD timeout value. When the DCD_SEL is set, the BC Module read the MultValIdBc if pin contact has been detected or the time defined on these fields has been expired . When the DCD_SEL is not set, he BC Module read the MultValIdBc if the time defined on these fields has been expired . 00: 300ms 01: 100ms 10: 500ms 11: 900ms	RW	0
4	**Vlgc_Com_Sel(Vlgc Compare Select)** Software writes 1 to this bit to choose the Vlgc compare during Primary Detect when the ID pin is float. When this bit is set, the BC Module is optionally allowed to compare D- with Vlgc beside the Vdp_src comparing. The BC Module determine that it is attached to a DCP or CDP if D- is greater than Vdat_ref, but less than Vlgc. Otherwise, the BC Module determine that it is attached to a SDP, which may actually be a SDP, or a PS2 port, or a proprietary charge.	RW	0
3	**DBP_Timeout_CTL(DBP Hardware Timeout Control)** If this bit is set, the BC Module would clear the DB_Perform bit on the BC_USB_Sta_R register after Tsvld_con_wkb when the DB_Perform bit is set. Note: Tsvld_con_wkb = 45min	RW	0
2	**BC_status(BC Detection status)** Detection finish or not 1:Detecting,when starting BC Detect, set this bit	RW	0

	0:Detect finish		
1	**Reserved**	RW	0
0	**RS(Run/Stop)** Software writes 1 to this bit to start the BC Module operation. A transition from a zero to a one would cause the reset on the BC Module logic. If this bit = 1,when VBUS low go high, BC detection start automatically	RW	0

REG 2DH: BC Module VBUS Control and Status Register

Default：30H

Reset: Power On reset

Bit	Description	R/W	Default
7	**Reserved**	R	0
6	Indicate the first power on status Software write 1 to this bit to indicate not first time power on If Battery not present, and this bit is 0,the VBUS current limit set to 3A, for the F/W update in factory	RW	0
5	DP/DM floating Detection enable 0:disable 1:enable	RW	1
4	DP/DM pull down enable 0:disable 1:enable	RW	1
3-0	Reserved	RW	0

REG 2EH: BC USB Status Register

Default：40H

Reset: bit6 is power on reset, Reset by the VBUS negative edge

Bit	Description	R/W	Default
7	DB_Perform Dead Battery Perform Both BC Module and software write 1 to this bit to perform unconfig DBP clause and clean it to 0 to stop the unconfig DBP clause.	RW	0
6	Dead battery detect enable bit (Reset: power on reset) 0:disable 1:enable	RW	1
5	Reserved		
4	USB_Mode USB Speed Mode Flag This bit is used in good battery state. It is set by the USB driver to indicate the USB speed mode for the power manage. 0: High-Speed, Full-Speed or Low-Speed Mode 1: Super-Speed Mode	RW	0
3-0	Dev_Bus_State Device Bus State Flag These fields are used in good battery state. They are set by the USB driver to indicate	RW	0

	the USB bus state for the power manage. 000b: attached, physical signal pin contact 001b: connected, attached and when the downstream terminal is valid 010b: suspended 011b: configured 100b-111b: reserved		

REG 2FH: BC Detect Status Register

Default：20H

Reset: Reset by the VBUS negedge

Bit	Description	R/W	Default
7-5	**BC_Result** **BC Detect Result** These fields indicate the result of BC Detect performance. These fields should be used by the BC Module when the BC_Per bit of the BC_GLOBAL_R register transaction from 1 to 0.	R	001
4-0	**Reserved**	R	00000

Value	Meaning	Descriptor
000b	Reserved	/
001b	SDP	The insert port is Standard Downstream Port
010b	CDP	The insert port is Charging Downstream Port
011b	DCP	The insert port is Dedicated Charging Port
1xxb	Reserved	/

REG 30H: VBUS path control & Hold voltage setting

Default：01H

Reset: Bit [7] & bit [2] reset signal is System reset, and Bit [6:3] & bit [1:0] reset signal is Power on reset

Bit	Description	R/W	Default
7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path selected 1: VBUS path Not selected	RW	0
6	Reserved		
5-3	VBUS V_{HOLD} setting bit 2-0 000: 4.0V; 001: 4.1V; 010: 4.2V; 011: 4.3V; 100: 4.4V; 101: 4.5V; 110: 4.6V; 111: 4.7V	RW	000
2	DRIVEVBUS pin output status control 0: output low level; 1: output high level(IPSOUT)	RW	0
1-0	Current limit default when BC1.2 detection result is non SDP 00: 900mA; 01: 1500mA; 10: 2000mA 11: 2500mA	RW	01

REG 31H: Power wakeup control & VOFF setting

Default：03H

Reset: Bit 3 reset signal is system reset, Bit [7-4] and Bit [2-0] reset signal is Power on reset

Bit	Description	R/W	Default
7	PWROK drive low or not when Power wake up and REG 31_[3]=1	RW	0

	0: not drive low 1: drive low in wake up period		
6	Soft power restart, Write 1 to this bit, the output power will be restart, and then this bit will clear itself	RW	0
5	Soft Power wakeup, Write 1 to this bit, the output power will be waked up, then this bit will clear itself	RW	0
4	Control bit for IRQ output and wakeup trigger when REG 31_[3] is 1 0: IRQ pin is masked and IRQ can wakeup AW1660 when REG 31_[3] is 1 1: IRQ pin is normal and IRQ can't wakeup AW1660 when REG 31_[3] is 1	RW	0
3	Enable bit for the function that output power be waked up by IRQ source, or IRQ pin, or REG 31_[5], etc. write 1 to this bit will clear itself 0: function is disable 1: function is enable	RW	0
2-0	V_{OFF} setting bit 2-0 000: 2.6V; 001: 2.7V; 010: 2.8V; 011: 2.9V; 100: 3.0V; 101: 3.1V; 110: 3.2V; 111: 3.3V	RW	011

REG 32H: Power Disable, BAT detect and CHGLED pin control

Default：43H (Note: bit3 default is customized)

Reset: Bit 7 reset signal is system reset, and Bit [6:0] reset signal is Power on reset

Bit	Description	R/W	Default
7	Power disable control Write 1 to this bit will disable DCDCs&LDOs, and will clear this bit by itself. But RTCLDO and Charger are not controlled by this bit.	RW	0
6	Battery detection function control 0: disable; 1: enable	RW	1
5-4	CHGLED pin control 00: Hi-Z; 01: 25% 0.5Hz toggle; 10: 25% 2Hz toggle; 11: drive low	RW	00
3	CHGLED pin control 0: controlled by REG 32H[5:4] 1: controlled by Charger	RW	0
2	Output power down sequence control 0: output power down at the same time; 1: output power down sequence is the reverse of the start sequence	RW	0
1-0	control bit for Delay time between PWROK signal and power good time 00: 8ms; 01: 16ms; 10: 32ms; 11: 64ms	RW	11

REG 33H: Charger Control 1

Default：C5H (Note: bit3-0 default is customized)

Reset: Bit [7] reset is system reset, Bit [6:0] reset is power on reset

Bit	Description	R/W	Default
7	Charger enable control 0-disable; 1-enable	RW	1
6-5	Charger target voltage setting 00: 4.10V; 01: 4.15V; 10: 4.2V; 11: 4.35V	RW	10

4	Charger end condition setting: 0-when I_{CHARGE}<10% I_{CHG}， Charge is done; 1-when I_{CHARGE}<20% I_{CHG}， Charge is done;	RW	0
3-0	Charge Current setting 200mA-2.8A, 200mA/step, 14steps, 1110-1111 reserved. default is 1200mA	RW	0101

REG 34H: Charger Control 2

Default：45H

Reset: Power on reset

Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes; 10: 60 minutes; 11: 70 minutes.	RW	0
6	Pre-charge Timer length setting 0		RW	1
5	Charger output turn off or not when charging is end & the PMIC is on state 0: turn off; 1: do not turn off		RW	0
4	CHGLED Type select when REG 32_[3] is 1 0: Type A; 1: Type B		RW	0
3	PMOS turn off or not when on time of the PMOS is larger than 32us 0: don't turn off; 1: turn off		RW	0
2	Charger target voltage depending on charge current or not when target voltage is 4.2V 0: disable; 1: enable		RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

REG 35H: Charger Control 3

Default：18H

Reset: [7:4] is VBUS negedge reset , others Power on reset

Bit	Description	R/W	Default
7-4	VBUS current limit select when VBUS Current limited mode is enable 0000-100mA; 0001-500mA; 0010-900mA; 0011-1500mA; 0100-2000mA; 0101-2500mA; 0110-3000mA; 0111-3500mA; 1xxx-4000mA	RW	0001
3	Charger temperature loop enable 0: disable 1:enable	RW	1
2-0	Reserved		

REG 36H: POK setting

Default：59H

Reset: Bit 3 is reset by system reset, the others is reset by Power on reset

Bit	Description		R/W	Default
7	ONLEVEL setting 1	00: 128ms; 01: 1s; 10: 2s; 11: 3s	RW	0
6	ONLEVEL setting 0		RW	1
5	IRQLEVEL setting 1	00: 1s; 01: 1.5s; 10: 2s; 11: 2.5s	RW	0
4	IRQLEVEL setting 0		RW	1
3	Enable bit of the function which will shut down the PMIC when POK is larger than OFFLEVEL 0: disable; 1: enable		RW	1

2	The PMIC auto turn on or not when it shut down after off level POK 0: not turn on; 1: auto turn on		RW	0
1	OFFLEVEL setting 1	00: 4s; 01: 6s; 10: 8s; 11: 10s.	RW	0
0	OFFLEVEL setting 0		RW	1

REG 37H: POK Power off activity time setting

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Power off activity time setting 0/10/20/30/40/50/60/70 S	R/W	000

REG 38H: VLTF-charge setting

Default：A5H

Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LTF-charge}$ setting, M	M*10H，M=A5H: 2.112V; range is 0V-3.264V	RW	A5H

REG 39H: VHTF-charge setting

Default：1FH

Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LHF-charge}$ setting, N	N*10H，N=1FH: 0.397V; range is 0V-3.264V	RW	1FH

REG 3AH: ACIN path control

Default：80H

Reset: Power on reset, but bit7 is system reset

Bit	Description	R/W	Default
7	ACIN path selection signal 0: ACIN-IPSOUT path not be selected; 1: ACIN-IPSOUT path be selected	RW	1
6	Reserved	RW	0
5-3	ACIN VHOLD setting bit2-0 000: 4.0V; 001: 4.1V; 010: 4.2V; 011: 4.3V; 100: 4.4V; 101: 4.5V; 110: 4.6V; 111: 4.7V	RW	000
2-0	ACIN current limited setting bit2-0 000: 1.5A; 001: 2.0A; 010: 2.5A; 011: 3.0A; 100: 3.5A; 101: 4.0A; 010&011: Reserved Note: when ACIN and VBUS is shorted on PCB, the current limit is set by VBUS current limit(REG35[7:4]).	RW	000

REG 3BH: DCDC frequency setting

Default：08H

Reset: Power on reset

Bit	Description	R/W	Default
7	DCDC and PWM charger frequency spread enable 0: disable; 1: enable	RW	0

6	DCDC and PWM charger frequency spread range control 0: 50kHz; 1: 100kHz	RW	0
5	Reserved	RW	0
4	DCDC2/3/4 mode select 0: Always PWM; 1: PSM/PWM Auto switch	RW	0
3-0	DCDC frequency setting bit 3-0 f_{OSC}=3 /(1+ (8-N) *0.04) MHz When N=08, f_{OSC} is 3MHz, error is ±5%	RW	1000

REG 3CH: VLTF-work setting

Default：FCH

Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LTF-work}$ setting, M	M*10H，M=FCH: 3.226V; range is 0V-3.264V	RW	FCH

REG 3DH: VHTF-work setting

Default：16H

Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{HTF-work}$ setting, N	N*10H，N=16H: 0.282V; range is 0V-3.264V	RW	16H

REG 3EH: Interface mode select

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-0	Interface mode select 0111 1100 (7CH): select RSB; Others: select normal TWI	RW	00H

REG 40H: IRQ enable 1

Default：D8H

Reset: Power on reset

Bit	Description	R/W	Default
7	ACIN over voltage IRQ enable	RW	1
6	ACIN from low go high IRQ enable	RW	1
5	ACIN from high go low IRQ enable	RW	0
4	VBUS over voltage IRQ enable	RW	1
3	VBUS from low go high IRQ enable	RW	1
2	VBUS from high go low IRQ enable	RW	0
1-0	Reserved		

REG 41H: IRQ enable 2

Default：FCH

Reset: Power on reset

Bit	Description	R/W	Default
7	Battery append IRQ enable	RW	1
6	Battery absent IRQ enable	RW	1
5	Battery maybe bad IRQ enable	RW	1

4	Quit battery safe mode IRQ enable	RW	1
3	Charger is charging IRQ enable	RW	1
2	Battery charge done IRQ enable	RW	1
1-0	Reserved		

REG 42H: IRQ enable 3

Default：FFH

Reset: Power on reset

Bit	Description	R/W	Default
7	Battery over temperature in charge mode IRQ (CBTOIRQ) enable	RW	1
6	Quit Battery over temperature in charge mode IRQ (QCBTOIRQ) enable	RW	1
5	Battery under temperature in charge mode IRQ (CBTUIRQ) enable	RW	1
4	Quit Battery under temperature in charge mode IRQ (QCBTUIRQ) enable	RW	1
3	Battery over temperature in work mode IRQ (WBTOIRQ) enable	RW	1
2	Quit Battery over temperature in work mode IRQ (QWBTOIRQ) enable	RW	1
1	Battery under temperature in work mode IRQ (WBTUIRQ) enable	RW	1
0	Quit Battery under temperature in work mode IRQ (QWBTUIRQ) enable	RW	1

REG 43H: IRQ enable 4

Default：03H

Reset: Power on reset

Bit	Description	R/W	Default
7	The PMIC temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0
6-3	Reserved		
2	GPADC(GPIO0) ADC convert finished IRQ enable	RW	0
1	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); normally, for low power warning requisition	RW	1
0	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); normally, for power off requisition	RW	1

REG 44H: IRQ enable 5

Default：7CH

Reset: System reset

Bit	Description	R/W	Default
7	Event timer timeout IRQ enable	RW	0
6	POK positive edge IRQ (POKPIRQ) enable	RW	1
5	POK negative edge IRQ (POKNIRQ) enable	RW	1
4	POK short time active IRQ (POKSIRQ) enable	RW	1
3	POK long time active IRQ (POKLIRQ) enable	RW	1
2	POK off time active IRQ (POKOIRQ) enable	RW	1
1	GPIO1 input edge IRQ enable	RW	0
0	GPIO0 input edge IRQ enable	RW	0

REG 45H: IRQ enable 6

Default：00H

Reset: System reset

Bit	Description	R/W	Default

7-2	Reserved		
1	BC_USB_ChngInEn (BC USB Status Change Interrupt Enable)	RW	0
0	MV_ChngIntEn (Rid MV_ChngEvnt Interrupt Enable)	RW	0

REG 48H: IRQ Status 1

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	ACIN over voltage IRQ, write 1 to it or ACIN drop to normal will clear it	RW	0
6	ACIN from low go high IRQ, write 1 to it or ACIN from high go low will clear it	RW	0
5	ACIN from high go low IRQ, write 1 to it or ACIN from low go high will clear it	RW	0
4	VBUS over voltage IRQ, write 1 to it or VBUS drop to normal will clear it	RW	0
3	VBUS from low go high IRQ, write 1 to it or VBUS from high go low will clear it	RW	0
2	VBUS from high go low IRQ, write 1 to it or VBUS from low go high will clear it	RW	0
1-0	Reserved	RW	0

REG 49H: IRQ Status 2

Default：00H

Reset: power on reset

Bit	Description	R/W	Default
7	Battery append IRQ, write 1 to it or Battery remove will clear it	RW	0
6	Battery absent IRQ, write 1 to it or Battery append will clear it	RW	0
5	Battery maybe bad IRQ, write 1 to it or PMIC quit battery safe mode will clear it	RW	0
4	Quit battery safe mode IRQ, write 1 to it or The PMIC enter battery safe mode will clear it	RW	0
3	Charger is charging IRQ, write 1 to it or charging is stop will clear it	RW	0
2	Battery charge done IRQ, write 1 to it or charger restart charging will clear it	RW	0
1-0	Reserved		

REG 4AH: IRQ Status 3

Default：00H

Reset: power on reset

Bit	Description	R/W	Default
7	CBTOIRQ, write 1 to it or Battery temperature drop to normal will clear it	RW	0
6	QCBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
5	CBTUIRQ, write 1 to it or Battery temperature rise to normal will clear it	RW	0
4	QCBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0
3	WBTOIRQ, write 1 to it or Battery drop to temperature will clear it	RW	0
2	QWBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
1	WBTUIRQ, write 1 to it or Battery rise to temperature will clear it	RW	0
0	QWBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0

REG 4BH: IRQ Status 4

Default：00H

Reset: Bit [7] reset is power on reset, Bit [6:0] reset is system reset

Bit	Description	R/W	Default
7	OTIRQ, write 1 to it or IC temperature drop to normal will clear it	RW	0

6-3	Reserved	RW	0
2	GPADC(GPIO0) ADC convert finished IRQ, write 1 will clear it	RW	0
1	IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); write 1 to it or system power rise up to warning level 1 will clear it	RW	0
0	IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); write 1 to it or system power rise up to warning level 2 will clear it	RW	0

REG 4CH: IRQ Status 5

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7	Event timer timeout IRQ, write 1 will clear it	RW	0
6	POKPIRQ, write 1 to it will clear it	RW	0
5	POKNIRQ, write 1 to it will clear it	RW	0
4	POKSIRQ, write 1 to it will clear it	RW	0
3	POKLIRQ, write 1 to it will clear it	RW	0
2	POKOIRQ, write 1 to it will clear it	RW	0
1	GPIO1 input edge IRQ, write 1 will clear it	RW	0
0	GPIO0 input edge IRQ, write 1 will clear it	RW	0

REG 4DH: IRQ Status 6

Default：00H

Reset: Reset by VBUS negedge

Bit	Description	R/W	Default
7-2	Reserved		
1	BC_USB_ChngEvnt (BC USB Status Change Event) This bit indicates that there is a change in the BC_USB_Sta_R register. When this bit is 1, and the interrupt on the BC_Charge_ChngInEn is 1, the BC Module will issue an interrupt to the controller. This bit and associated interrupt is clean by writing '1'.	RW	0
0	MV_ChngEvnt (MultValIdBc Multi-Valued input changed Event) This bit indicates that there is a change in the value of MultValIdBc field. When this bit is 1, and the interrupt on the MV_ChngIntEn is 1, the BC Module will issue an interrupt to the controller. This bit and associated interrupt is clean by writing '1'.	RW	0

REG 58H: TS pin input ADC data, highest 8bit

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	TS pin input ADC data highest 8bits， Default is Battery temperature	R	00

REG 59H: TS pin input ADC data, lowest 4bit

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00

3-0	TS pin input ADC data lowest 4bits， Default is Battery temperature	R	00

REG 5AH: GPADC pin input ADC data, highest 8bit

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	GPADC pin input ADC data, highest 8bit	R	00

REG 5BH: GPADC pin input ADC data, lowest 4bit

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	GPADC pin input ADC data, lowest 4bit	R	00

REG 78H: Average data bit[11:4] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG 79H: Average data bit[3:0] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00

REG 7AH: Average data bit[11:4] for Battery charge current

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery charge current	R	00

REG 7BH: Average data bit[3:0] for Battery charge current

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery charge current	R	00

REG 7CH: Average data bit[11:4] for Battery discharge current

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery discharge current	R	00

REG 7DH: Average data bit[3:0] for Battery discharge current

Default：00H

Reset: System reset

Bit	Description	R/W	Default

7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery discharge current	R	00

REG 80H: DCDC PWM/PFM mode select

Default：80H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	R/W	1
6	Reserved	RW	0
5	DCDC6 PFM/PWM control 0: auto switch; 1: always PWM	RW	0
4	DCDC5 PFM/PWM control 0: auto switch; 1: always PWM	RW	0
3	DCDC4 PFM/PWM control 0: auto switch; 1: PSM/PWM When this bit is set as '1', refer to REG3B bit [4] for DCDC mode select	RW	0
2	DCDC3 PFM/PWM control 0: auto switch; 1: PSM/PWM When this bit is set as '1', refer to REG3B bit [4] for DCDC mode select	RW	0
1	DCDC2 PFM/PWM control 0: auto switch; 1: PSM/PWM When this bit is set as '1', refer to REG3B bit [4] for DCDC mode select	RW	0
0	DCDC1 PFM/PWM control: 0: auto switch; 1: always PWM	RW	0

REG 81H: Off-Discharge and Output monitor control

Default：80H

Reset: Power on reset

Bit	Description	R/W	Default
7	Internal off-Discharge enable for DCDC & LDO 0-disable; 1-enable	RW	1
6	Reserved	RW	0
5	DCDC6 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable	RW	0
4	DCDC5 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable	RW	0
3	DCDC4 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable	RW	0
2	DCDC3 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable		
1	DCDC2 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable	RW	0
0	DCDC1 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable	RW	0

REG 82H: ADC Enable

Default：E1H

Reset: Power on reset

Bit	Description		R/W	Default
7	BAT voltage ADC enable	0: off; 1: on	RW	1
6	BAT current ADC enable	0: off; 1: on	RW	1
5	Die temperature ADC enable	0: off; 1: on	RW	1
4	GPIO0 ADC enable	0: off; 1: on	RW	0
3-1	Reserved			
0	TS pin input to ADC enable	0: off; 1: on	RW	1

REG 84H: ADC speed setting, TS pin Control

Default：F2H

Reset: power on reset

Bit	Description	R/W	Default
7-6	Current source from GPIO0 pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA	RW	11
5-4	Current source from TS pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA	RW	11
3	reserved	RW	0
2	TS pin function select: 0-TS pin is the battery temperature sensor input and will affect the charger 1-TS pin is an External input for ADC and do not affect the charger	RW	0
1-0	Current source from TS pin on/off enable bit [1:0] 00: off; 01: on when charging battery, off when not charging; 10: on in ADC phase and off when out of the ADC phase, for power saving; 11: always on Note: TS pin and GPIO0ADC pin are same current source, so if set the TS current source is always on, the GPIO0ADC is invalid	RW	10

REG 85H: ADC speed setting

Default：B0H

Reset: power on reset

Bit	Description		R/W	Default
7	TS/GPIO0 ADC speed setting bit 1	100×2^n	RW	1
6	TS/GPIO0 ADC speed setting bit 0	So Fs=25, 50, 100, 200Hz	RW	0
5	Vol/Cur ADC speed setting bit 1	100×2^n	RW	1
4	Vol/Cur ADC speed setting bit 0	So Fs=100, 200, 400, 800Hz	RW	1
3	Reserved			
2	GPIO0 ADC work mode 0: not output current; 1: output current		RW	0
1-0	Reserved		RW	00

REG 8AH: Timer control

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7	Timer time out status	RW	0

	It indicate that timer time out when this bit from low go high Write this bit to 1, will clear the status and the timer		
6-0	Set threshold of the timer Write these 7 bits to all 0, will disable the timer	RW	0000000

REG 8EH: DCDC output voltage monitor de-bounce time setting

Default：40H

Reset: Power on reset

Bit	Description	R/W	Default
7-6	DCDC output voltage monitor de-bounce time setting, 00: 62us; 01: 124us; 10: 186us; 11: 248us	RW	01
5-0	Reserved	RW	00

REG 8FH: IRQ pin, hot-over shut down

Default：00H (Note: bit4 default is customized)

Reset: Power on reset

Bit	Description	R/W	Default
7	IRQ pin turn on or wakeup PMIC function enable 0: disable; 1: enable	RW	0
6	ACIN and VBUS short or not depending on 0: REG00[1], auto detect; 1: REG8F[5]	RW	0
5	ACIN and VBUS short or not setting 0: not short; 1: short	RW	0
4	N_VBUSEN pin function control 0: DRIVEVBUS, which is an output pin; 1: N_VBUSEN, which is an input pin	RW	0
3	The function control that 16s' POK trigger power on reset: 0-disable; 1-enable	RW	0
2	The PMIC shut down or not when Die temperature is over the warning level 3 0-not shut down; 1-shut down	RW	0
1	Voltage recovery enable bit when AXP707 wakeup from REG31H[3]=1 0: recovery to the default voltage; 1: not recovery to the default voltage, the voltage not change	RW	0
0	When PMIC is on work status, if drive low PWROK pin, the PMIC will restart function enable 0: disable; 1: enable	RW	0

REG 90H: GPIO0 (GPADC) control

Default：07H

Reset: system reset

Bit	Description	R/W	Default
7	Enable GPIO0 Positive edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable	RW	0
6	Enable GPIO0 Negative edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable	RW	0
5-3	Reserved	RW	0
2	GPIO0 pin function control bit 2 | 000: drive low	RW	1

		001: drive high		
1	GPIO0 pin function control bit 1	010: digital input, trigger point is about 1.2V 011: low noise LDO on	RW	1
0	GPIO0 pin function control bit 0	100: low noise LDO off 101-111: Floating, if ADC enable， then work as ADC input mode	RW	1

REG 91H: GPIO0LDO and GPIO0 high level voltage setting

Default：1AH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved		
4-0	GPIO0LDO and GPIO0 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 92H: GPIO1 control

Default：07H

Reset: system reset

Bit	Description		R/W	Default
7	Enable GPIO1 Positive edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable		RW	0
6	Enable GPIO1 Negative edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable		RW	0
5-3	Reserved			
2	GPIO1 pin function control bit 2	000: drive low 001: drive high	RW	1
1	GPIO1 pin function control bit 1	010: digital input, trigger point is about 1.2V 011: low noise LDO on	RW	1
0	GPIO1 pin function control bit 0	100: low noise LDO off 101-111: Floating	RW	1

REG 93H: GPIO1LDO and GPIO1 high level voltage setting

Default：1AH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	GPIO1LDO and GPIO1 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 94H: GPIO signal bit

Default：00H

Reset: system reset

Bit	Description	R/W	Default
7-2	Reserved		
1	This bit reflect the logic level of the GPIO1 pin when configured as digital input	R	0
0	This bit reflect the logic level of the GPIO0 pin when configured as digital input	R	0

REG 97H: GPIO pull down control

Default：00H

Reset: system reset

Bit	Description	R/W	Default
7-2	Reserved		
1	GPIO1 Pull down control in digital input mode 0: off; 1: on	RW	0
0	GPIO0 Pull down control in digital input mode 0: off; 1: on	RW	0

REG A0H: Real time data bit[11:4] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG A1H: Real time data bit[3:0] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00

REG B8H: Fuel Gauge Control

Default：C0H

Reset: power on reset

Bit	Description	R/W	Default
7	fuel gauge enable control(including OCV and coulomb meter) 0: Disable; 1: Enable	RW	1
6	Coulomb meter enable control 0: Disable; 1: Enable	RW	1
5	Battery maximum capacity calibration enable control 0: Disable; 1: Enable	RW	0
4	Battery maximum capacity calibration status 0: Not calibrating; 1: Is calibrating	R	0
3	OCV-SOC curve calibration enable control 0: Disable; 1: Enable Suggest set this bit as 0	RW	0
2	OCV-SOC curve calibration status 0: Not calibrating; 1: Is calibrating	R	0
1-0	Reserved	RW	0

REG B9H: Battery capacity percentage for indication

Default：64H

Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if battery capacity percentage for indication is valid 0: Not valid; 1: Is valid	R	0

6-0	Battery capacity percentage for indication	R	64H

REG BAH: RDC 1

Default：80H

Reset: Bit [7] & [4-0] reset is power on reset

Bit	Description	R/W	Default
7	RDC calculation control 0: disable; 1: enable	RW	1
6	RDC was right detected or not flag： 0: N; 1: Y	R	0
5	RDC has detected or not during this power on time 0: N; 1: Y	R	0
4-0	RDC value HSB 5 bit	RW	00000

REG BBH: RDC 0

Default：5DH

Reset: power on reset

Bit	Description	R/W	Default
7-0	RDC value LSB 8bit	RW	5DH

REG BCH: OCV 1

Default：00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	OCV HSB 8bit	R	00H

REG BDH: OCV0

Default：00H

Reset: power on reset

Bit	Description	R/W	Default
7-4	Reserved		
3-0	OCV LSB 4bit	R	0000

REG E0H: Battery maximum capacity

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if battery maximum capacity is valid 0: Not valid; 1: Is valid	R/W	0
6-0	battery maximum capacity bit[14:8]	RW	00H

REG E1H: Battery maximum capacity

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-0	battery maximum capacity bit[7:0] (Unit: 1.456mAh)	RW	00H

REG E2H: Coulomb meter counter1

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if coulomb meter counter is valid: 0: Not valid; 1: Is valid	RW	0
6-0	Coulomb meter counter[14:8]	RW	00H

REG E3H: Coulomb meter counter2

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-0	Coulomb meter counter[7:0] (Unit: 1.456mAh)	RW	00H

REG E4H: OCV Percentage of battery capacity

Default：64H

Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if OCV percentage of battery capacity is valid 0: Not valid; 1: Is valid	R	0
6-0	OCV percentage of battery capacity	R	64H

REG E5H: Coulomb meter percentage of battery capacity

Default：64H

Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if coulomb meter percentage of battery capacity is valid: 0: Not valid; 1: Is valid	R	0
6-0	Coulomb meter percentage of battery capacity	R	64H

REG E6H: Battery capacity percentage warning level

Default：A0H

Reset: Power on reset

Bit	Description	R/W	Default
7-4	Warning level 1: Warning threshold, 5-20%, 1% per step	RW	1010
3-0	Warning level 2: Shutting down threshold, 0-15%, 1% per step	RW	0000

REG E8H: Fuel gauge tuning control 0

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Battery capacity percentage for indication update minimum interval 000-30s 001-60s 010-120s 011-164s 100-immediately update when changed 101-5s 110-10s 111-20s	RW	0

REG E9H: Fuel gauge tuning control 1

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage calibrate the Coulomb meter percentage, maximum time interval 00-60s 01-120s 10-15s 11-30s	RW	0
5-3	Wait for the stability for charge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0
2-0	Wait for the stability for discharge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0

REG EAH: Fuel gauge tuning control 2

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1 11-2	RW	0
5-4	Coulomb meter Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1 11-2	RW	0

3	Battery maximum capacity and OCV-SOC curve calibration start condition: 0-OCV percentage < (REG E6H[3:0] + 3) 1-OCV percentage < (REG E6H[3:0] + 6)	RW	0
2	Battery maximum capacity calibration end condition 0 0-OCV percentage ≥ 95% 1-OCV percentage ＝ 100%	RW	0
1	Battery maximum capacity calibration end condition 1 0-wait for charge finished 1-do not wait for charge finished	RW	0
0	Battery maximum capacity calibration end condition 2 wait N ms for the charge finished indication signal after REG 01H[6] clear to 0, N is set: 0-68 1-120	RW	0

REG EBH: Fuel gauge tuning control 3

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	When charge status bit REG 01H[6] = 1,the percentage of indication can be decrease or not 0-decrease enable 1-decrease disable	RW	0
6-4	When REG 01H[6] = 1， percentage of indication decrease hysteresis(N) setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3%	RW	0
3	Calculation RDC current condition setting 0-≥300mA 1-≥150mA	RW	0
2-0	Calibrate RDC percentage changed threshold setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3% calibration： ΔOCVPCT > N	RW	0

REG ECH: Fuel gauge tuning control 4

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	ADC current data include offset0 or not(For debug) 0: Enable; 1: Disable	RW	0
6	ADC current data offset0 smooth control(For debug) 0: Enable; 1: Disable	RW	0
5	RDC re-calculate when PMIC power on for power off 0: Disable; 1: Enable	RW	0
4-3	The minimum battery voltage for RDC calculation 00: 3.5V; 01: 3.6V; 10: 3.7V; 11: 3.4V	RW	00
2-0	Coulomb counter calibration threshold，relative with REG_E6_[3:0] 000-REG_E6H[3:0]+7(default) 001-REG_E6H[3:0]+8 010-REG_E6H[3:0]+9 011-REG_E6H[3:0]+10 100-REG_E6H[3:0]+3 101-REG_E6H[3:0]+4 110-REG_E6H[3:0]+5 111-REG_E6H[3:0]+6	RW	000

REG EDH: Fuel gauge tuning control 5

Default：00H

Reset: Power on reset

Bit	Description	R/W	Default
7	OCV percentage relative with the charge/discharge rate control 0-Disable 1-Enable	RW	0
6	Update time when rate > 0.5C 0-30S 1-15S	RW	0
5-4	Update time when rate < 0.5C and rate > 0.1C 00-60S 01-75S 10-30S 11-45S	RW	00
3-2	Update time when rate < 0.1C 00-120S 01-180S 10-240S 11-60S	RW	00

1-0	Fixed update time 00-30S 01-45S 10-60S 11-15S	RW	00

8. Typical Application

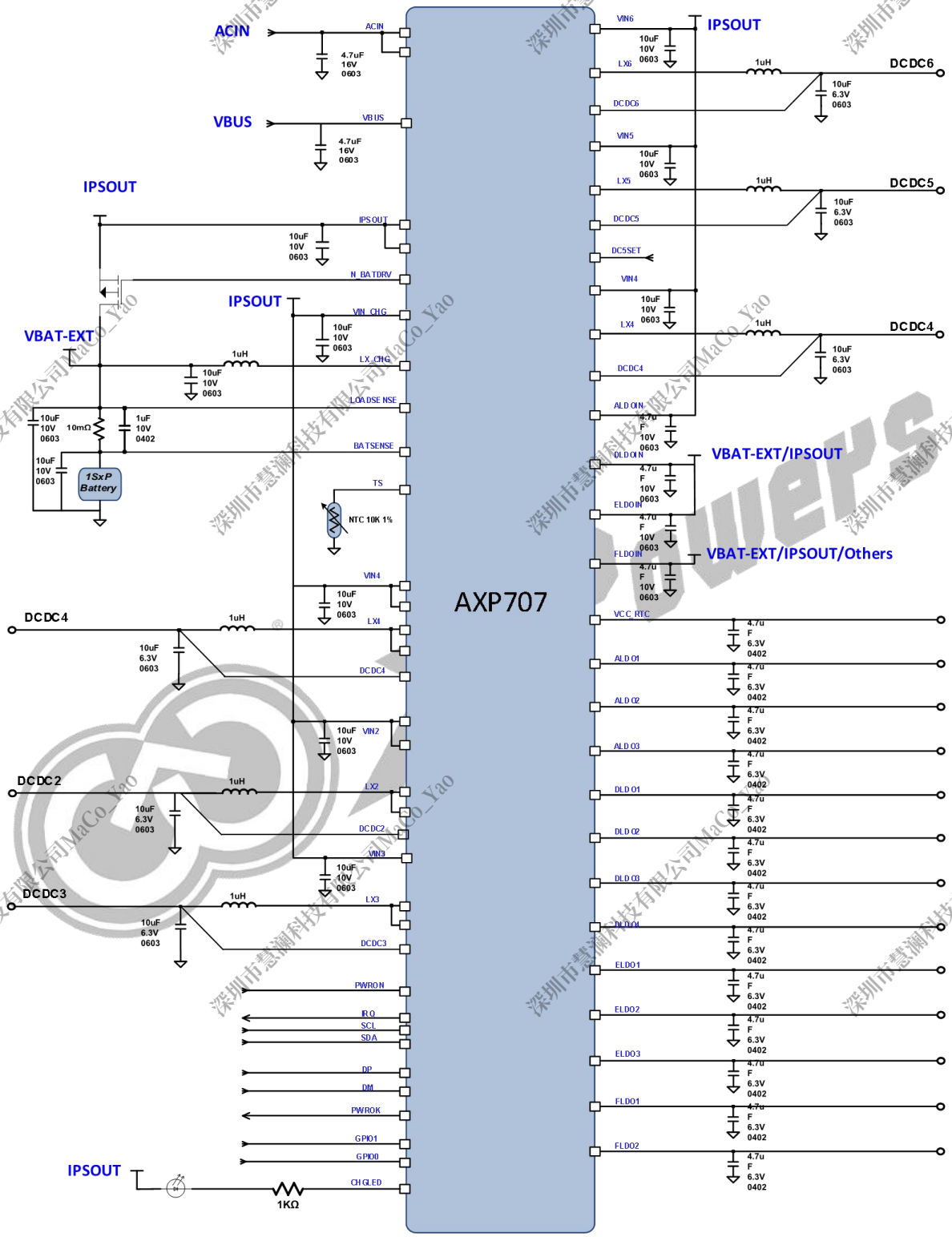
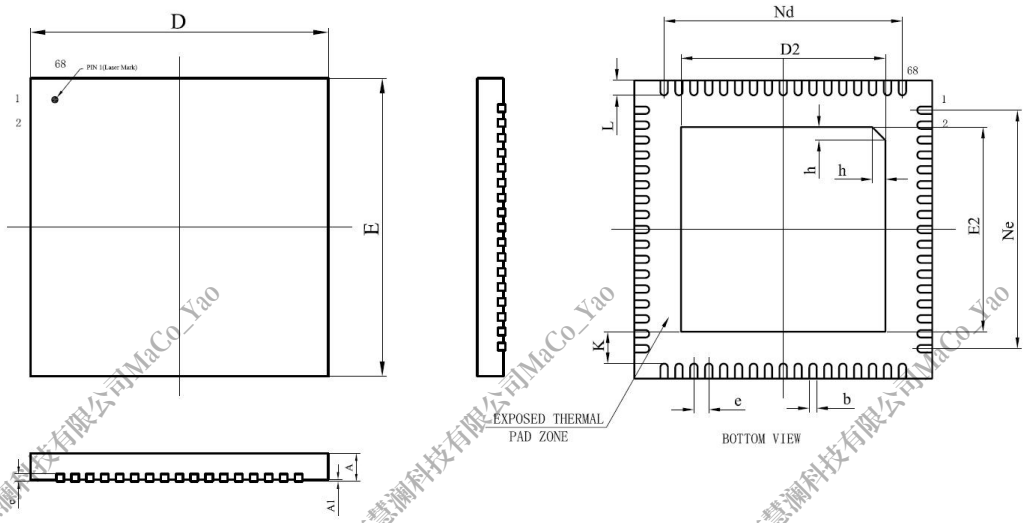


Figure 8-1 Typical Application

9. Package and Ordering Information

9.1 Package Information

AXP707 is available in 8mm x 8mm 68 pin QFN package.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	5.39	5.49	5.59
e	0.40BSC		
Nd	6.40BSC		
E	7.90	8.00	8.10
E2	5.39	5.49	5.59
Ne	6.40BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	240*240		

Figure 9-1 Package Information

9.2 Marking information

Figure 9-2 shows AXP707 marking.

Figure 9-2 AXP707 Marking

Table 9-1 describes AXP707 marking information.

Table 9-1 AXP707 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP707	Product name	Fixed
2	LLLLLEA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

9.3 Carrier

Table 9-2 shows AXP707 tray carrier information.

Table 9-2 Tray Carrier Information

Item	Color	Size
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm
Pearl cotton cushion (The Gap between vacuum bag and inside box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm
Inside Box	White	396mm x 196mm x 96mm
Outside Box	White	420mm x 410mm x 320mm

Figure 9-3 shows tray dimension drawing of AXP707.

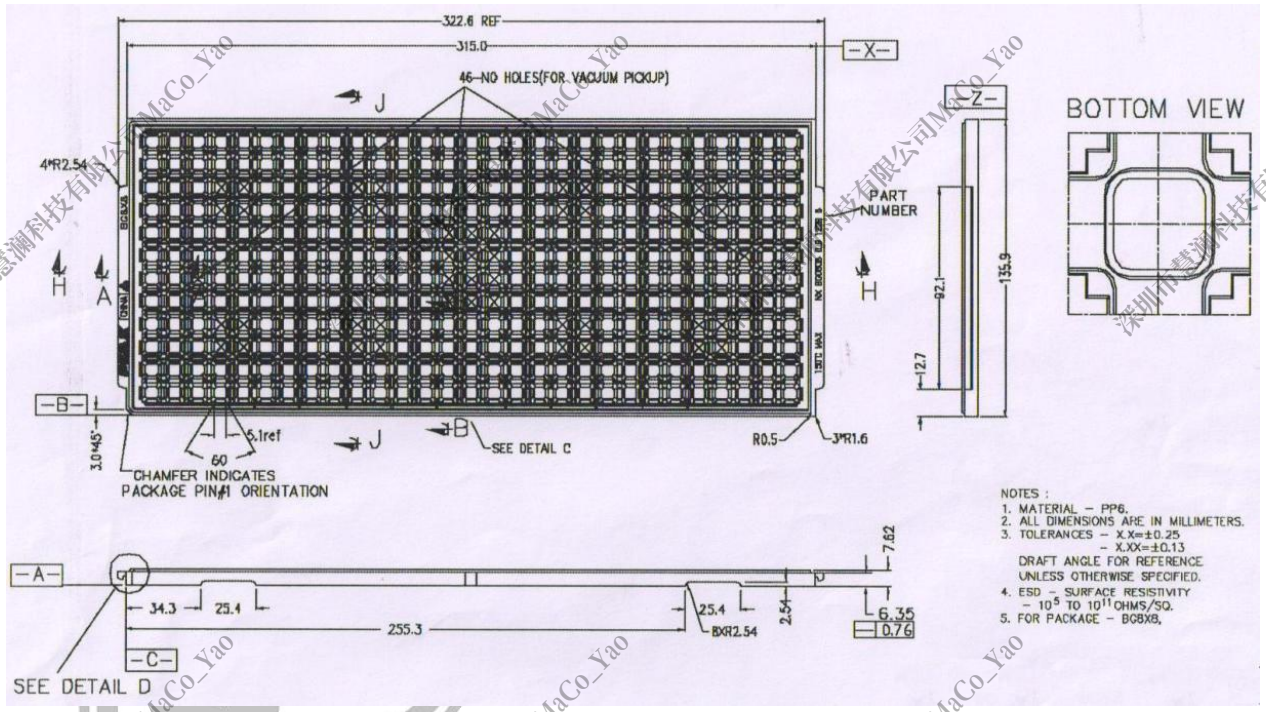


Figure 9-3 Tray Dimension Drawing

Table 9-3 shows AXP707 packing quantity.

Table 9-3 Packing Quantity Information

Type	Quantity	Part Number
Tray	348pcs/Tray 10trays/Package	AXP707

9.4 Storage

9.4.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in Table 9-4.

Table 9-4 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30℃/85%RH
2	1 year	≤30℃/60%RH

2a	4 weeks	≤30℃ /60%RH
3	168 hours	≤30℃ /60%RH
4	72 hours	≤30℃ /60%RH
5	48 hours	≤30℃ /60%RH
5a	24 hours	≤30℃ /60%RH
6	Time on Label(TOL)	≤30℃ /60%RH

AXP707 device samples are classified as MSL3.

9.4.2 Bagged Storage Conditions

The shelf life of AXP707 are defined in Table 9-5.

Table 9-5 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Shelf life	6 months

9.4.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP707 is as follows.

Table 9-6 Out-of-bag Duration

Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

9.5 Baking

It is not necessary to bake AXP707 if the conditions specified in Section 9.4.2 and Section 9.4.3 have not been exceeded. It is necessary to bake AXP707 if any condition specified in Section 9.4.2 and Section 9.4.3 have been exceeded.

Table 9-7 Baking Conditions

Surrounding	**Condition**	**Note**
Nitrogen	125℃/8 hours	Recommended condition. It is recommended to bake once, no more than three times.
CAUTION： If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature		

10. Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 10-1 shows the typical reflow profile of AXP707 device sample.

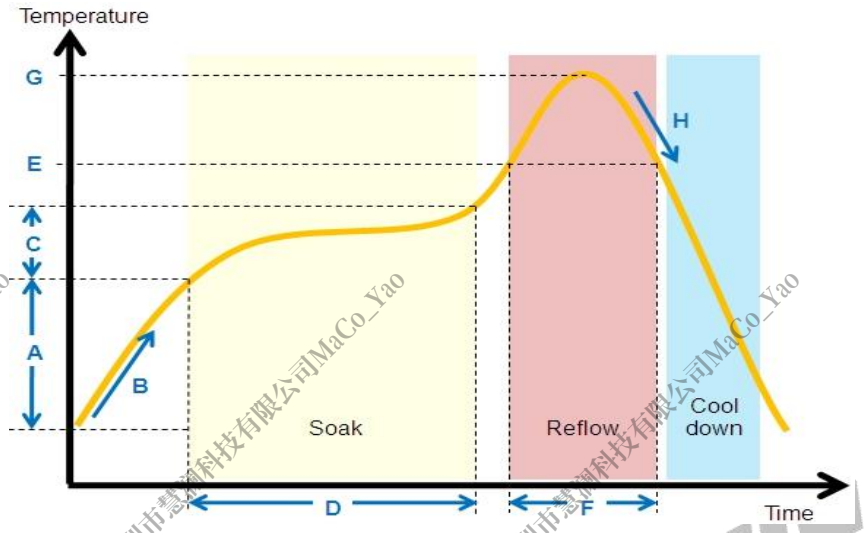


Figure 10-1 AXP707 Typical Reflow Profile

Reflow profile conditions of AXP707 device sample is given in Table 10-1.

Table 10-1 AXP707 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25℃ -> 150℃
B	Preheat ramp up rate	1.5~2.5 ℃/sec
C	Soak temperature range	150℃ -> 190℃
D	Soak time	80~110 sec
E	Liquidus temperature	217℃
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250℃
H	Cool down temperature rate	≤4℃/sec

Declaration