R818

PCB Design Manual

Revision 1.0

March 10, 2020

Revision History

Revision	Date	Author	Description
1.0	March 10, 2020	AWA XXX	Initial release version

Contents

Figures

1 About This Document

1.1 Purpose and Scope

This document introduces the PCB design points and notes when designing application solutions with R818 chip. The higher and higher circuit operating speed puts forward higher requirements on PCB design. You need to focus more on problems like signal integrity, power integrity, and electromagnetic compatibility. To ensure the quality of your PCB design, read this document carefully before you start your design.

1.2 Intended Audience

This document is intended for:

- PCB layout engineers
- Hardware development engineers
- Technical support engineers

2 Stack Up

2.1 Stack Structure and Impedance Control

The most common solution for R818 is 4-layer board architecture. The following figure shows the recommended settings for the stack structure and impedance control. If you want to adjust the thickness of the whole board, adjust the dielectric thickness between Layer 2 and Layer 3, and keep the thickness of the other dielectric layer fixed.

Figure 2-1 Typical 4-Layer Board Architecture

Total layers:	4
Board thickness:	1.0/1.6 mm +/- 10%
PCB material:	Typical FR4
Surface finish	ENIG

Stackup Control Table

..	Stackup Structure				Impedance Requirements				Layer definiion	
Layer	Type	Thickness (mil)		Dk(with Sim Z0)	Impedance spec (Ohms)	Reference layer	Width/space(mil)	Sim Z0(Ohms)	DDR	others
	solder mask	0.5	SM	3.8						
1	TOP	1.6	0.3oz+plating		50±10%	2	4	52.89	Signal	Signal
					50±10%(wifi)	2	5	47.57		
					50±10%(wifi)	1	20[1]	49.7		
					90±10%	2	4.5/6.5	91.16		
					100±10%	2	3.8/8.7	100.93		
	prepreg	2.9		4						
2	GND	1.2	1.0oz						GND	GND
	core	27/50		4.5						
3	PWR	1.2	1.0oz		50±10%	4	4	47.56	Signal	Power
					90±10%	4	3.8/8.7	**89.09**		
	prepreg	2.9		4						
4	BOTTOM	1.6	0.3oz+plating		50±10%	3	4	52.89	Power	Signal
					90±10%	3	4.5/6.5	91.16		
					100±10%	3	3.8/8.7	100.93		
	solder mask	0.5	SM	3.8						
	Board thickness:	39.4/62.4								

Note 1:

To control the impedance at 50 Ohms with the trace width 20 mils, the following requirements should be met:

- Shield the 20-mil signal traces with the ground trace and ensure the trace spacing between the signal and ground is 4 mils.
- Leave a 40-mil-width gap at Layer 2 right underneath the traces at Layer 1.

2.2 Tips for the Overall Layout

For the PCB overall layout, pay attention to the following items:

- After packaging all the components correctly, place them in the right position according to the schematic diagram. For the hole-type components, verify whether they are plated or non-plated.
- Ensure there is no interference around the components.
- Reserve bonding pads for the shielding case.
- Place the modules based on their functions and consider the heat dissipation problems.
- After finishing the overall layout, submit the .DXF file to the structural engineer to check whether there is structural interference.

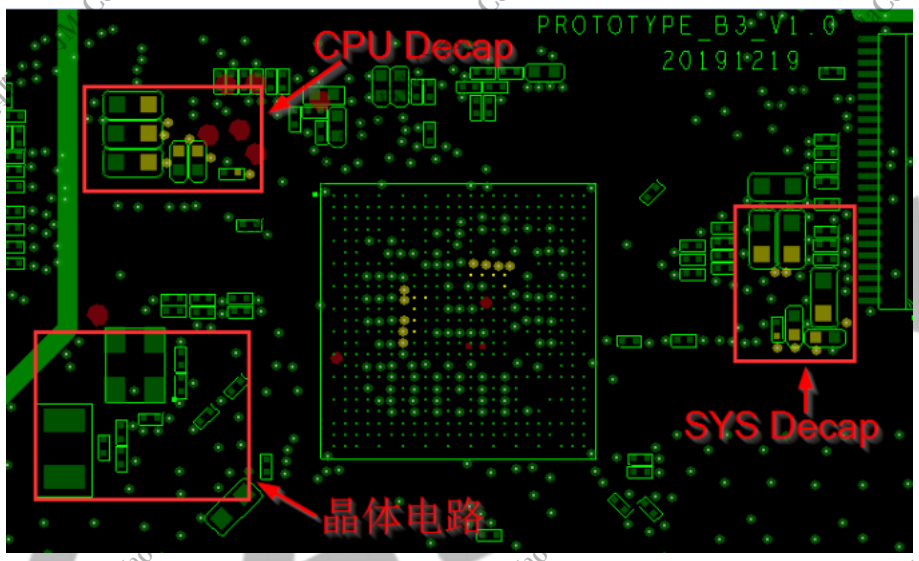
3 CPU

3.1 Layout

When placing the CPU, pay attention to the following items:

- Do not place the CPU to the edge of the board where is vulnerable to stress.
- Place decoupling capacitors according to their capacitance. The one with larger capacitance should be placed nearer to the pin of the IC power.
- Place the crystal near the SoC and keep it away from any interference source.
- Place the test point to a proper position of the back of the PCB.

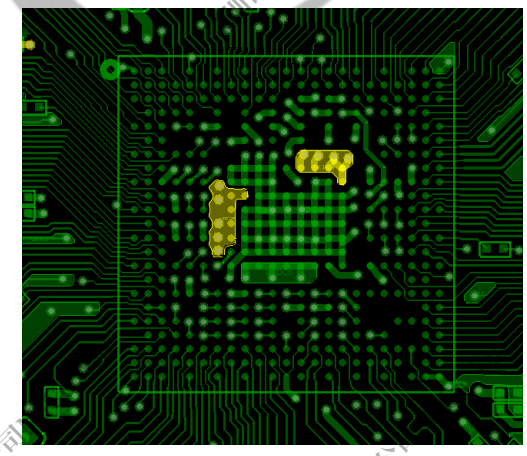
Figure 3-1 CPU Layout



3.2 Traces

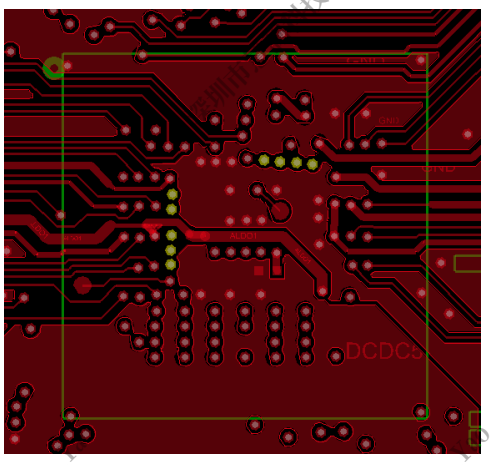
1. For balls on Round 1–3, fanout traces on the top layer. Normally, set both the width and spacing of the traces as 4 mils. For the conductor between balls, set both the width and spacing of the traces as 3 mils.

Figure 3-2 CPU Fanout (1)



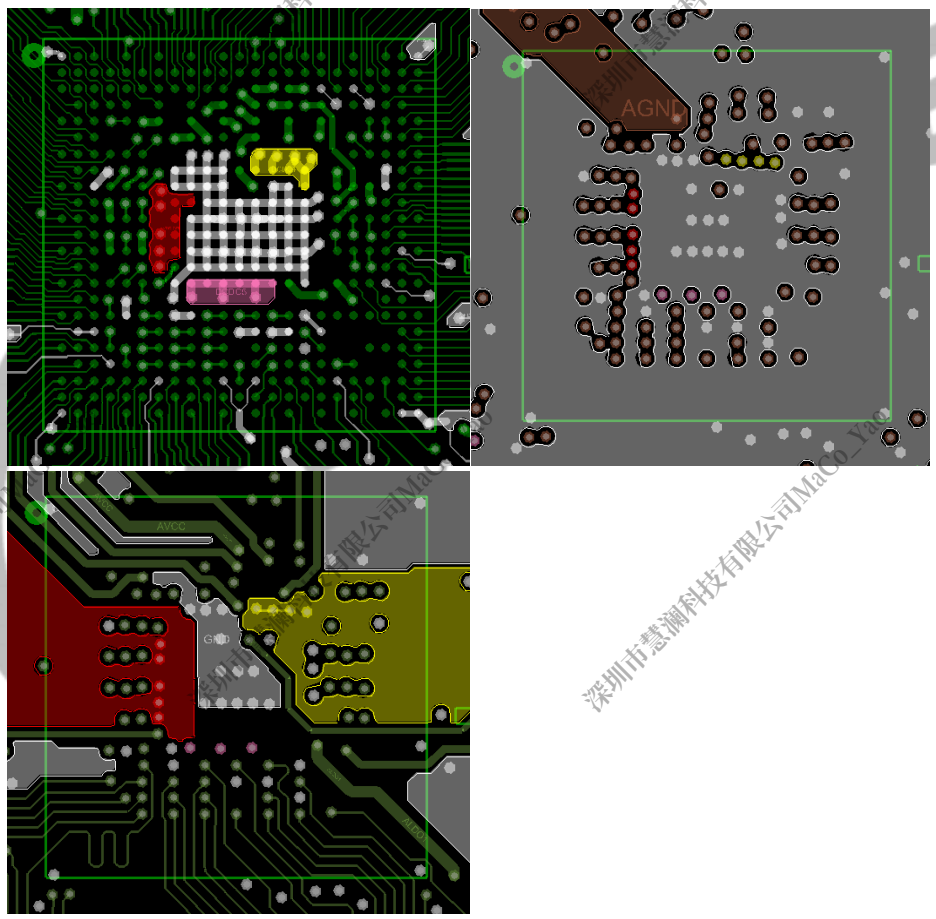
2. For balls on and within Round 4, fan out vias (8/16 mils) and route the traces on the bottom layer. Neatly place the via to reserve space for the other traces.

Figure 3-3 CPU Fanout (2)



3. For the Power and GND pins, fan out vias (8/16 mils) and route the traces on the inner layer with shapes. Reserve enough space for the shapes.

Figure 3-4 CPU Fanout (3)



3.3 Power/GND

1. Ensure the trace width of the three main power networks of R818: VDD-CPU, VDD-SYS, and VCC-DRAM. If possible, use shape to connect the power pins and set the width.

Figure 3-5 DC-DC Layer

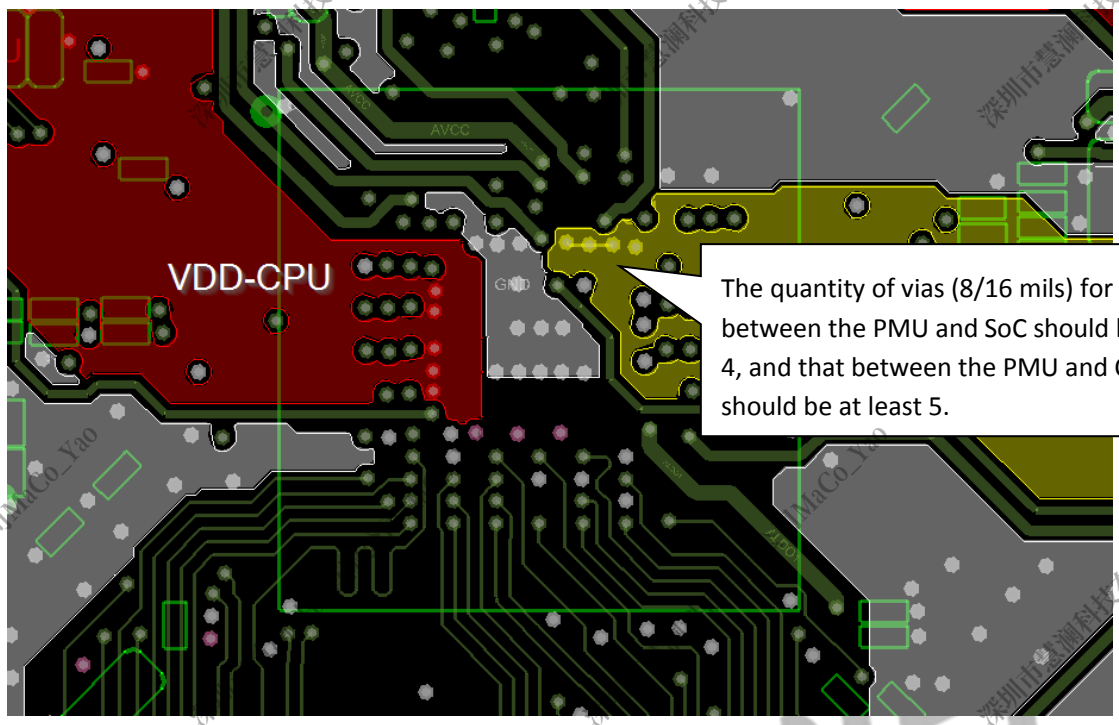


Figure 3-6 Impacts of Vias on the Plane (1)

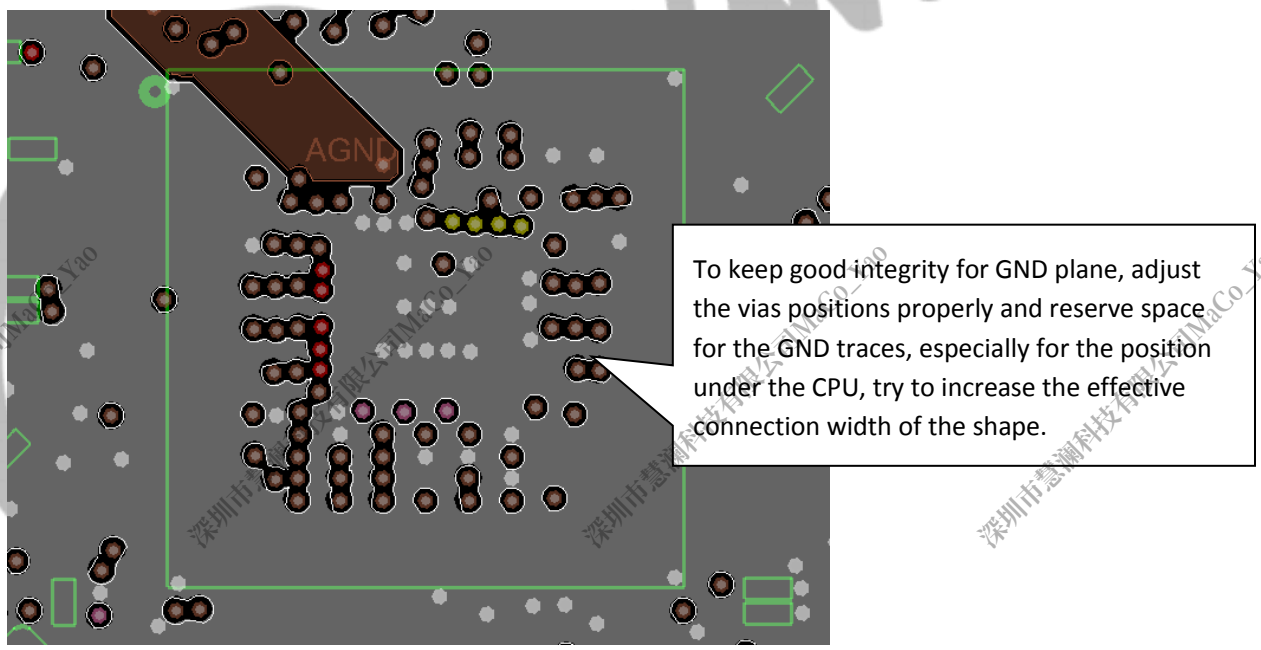
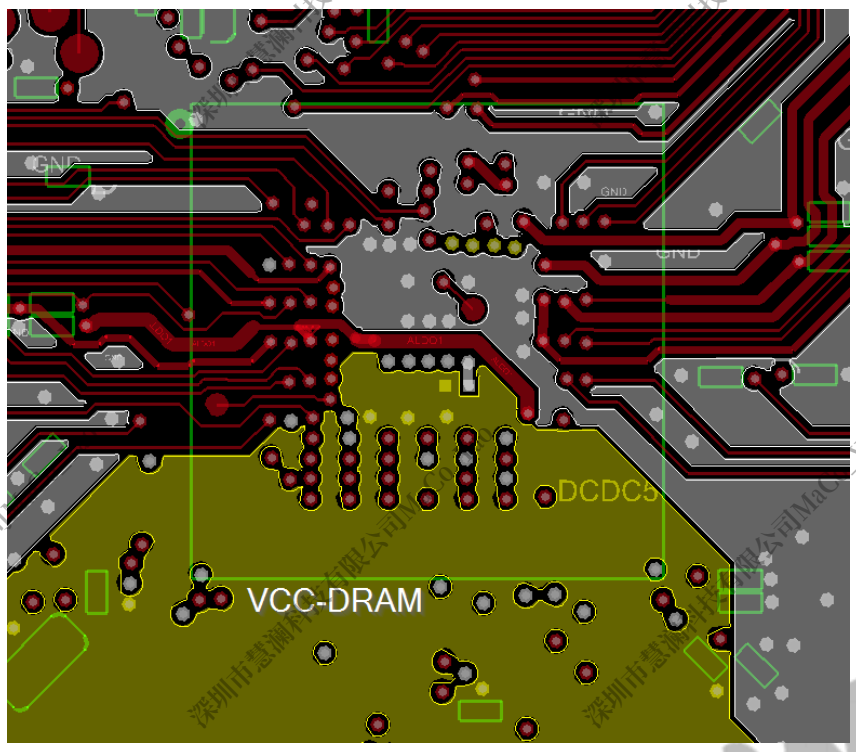
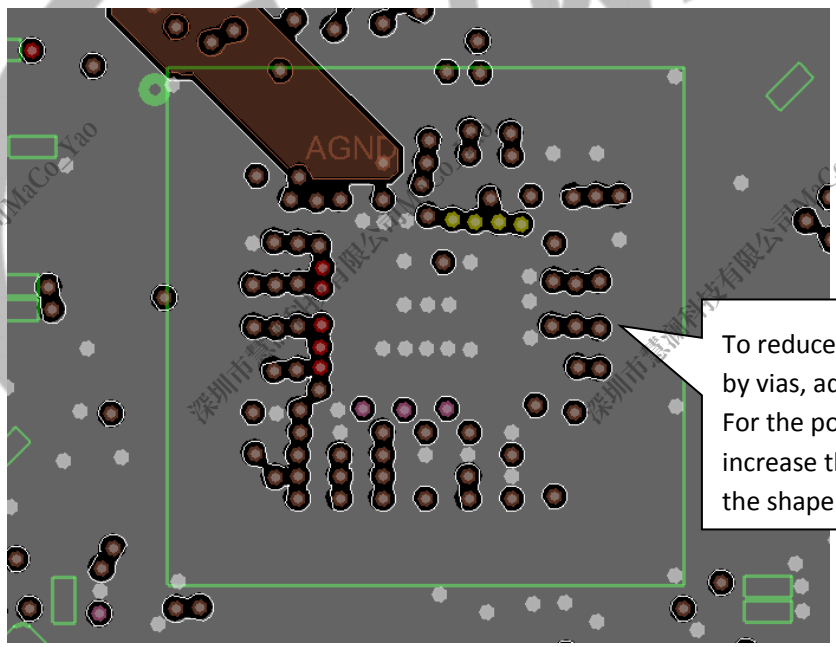


Figure 3-7 Impacts of Vias on the Plane (2)



2. Ensure the width of GND traces. If possible, use shape to connect the GND pins and set the shape width as large as possible.

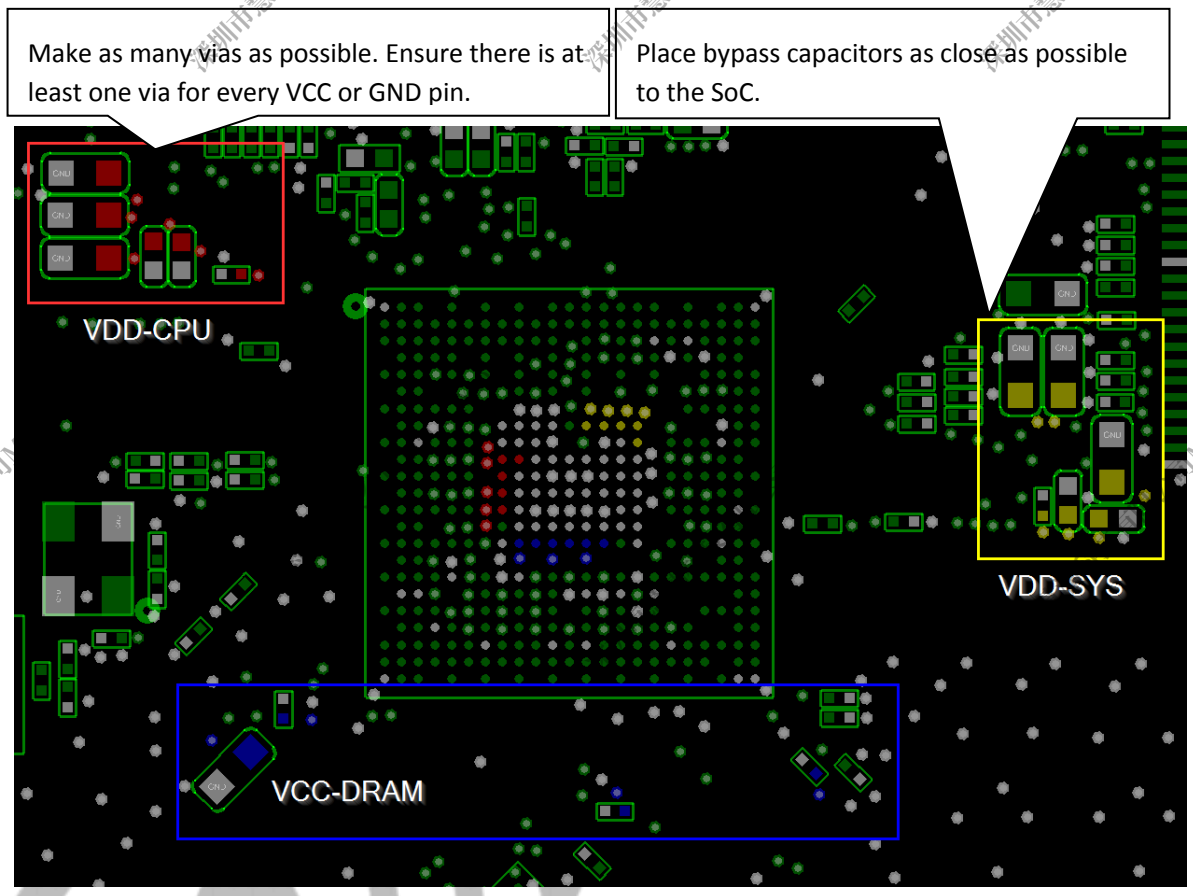
Figure 3-8 GND Plane



To reduce the damage to the plane caused by vias, adjust the vias positions properly. For the position under the CPU, try to increase the effective connection width of the shape.

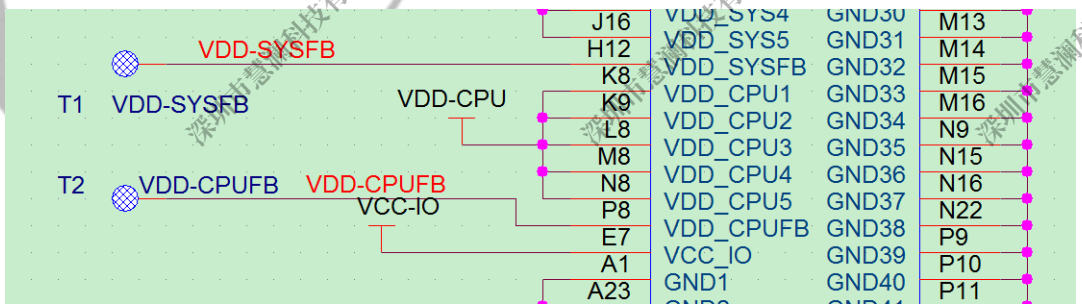
3. Follow the guidelines in the figure below to lay out the bypass capacitors.

Figure 3-9 Layout for Bypass Capacitors



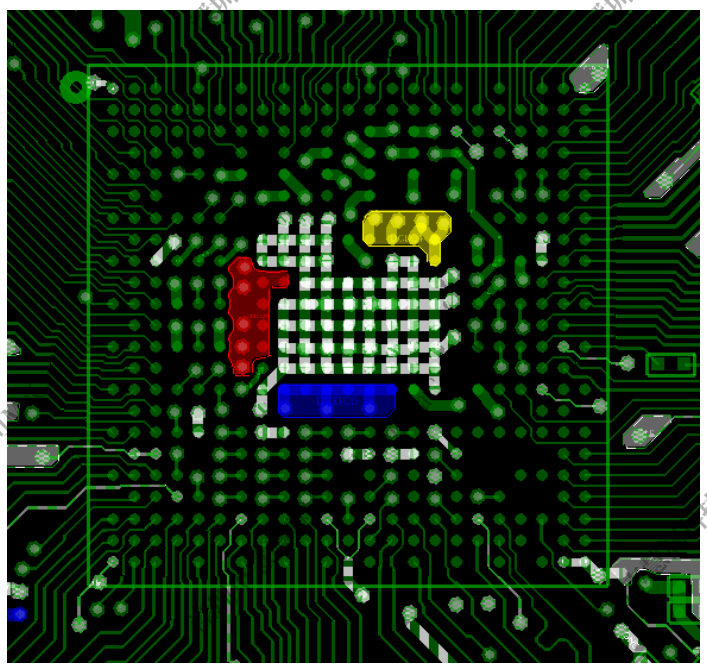
4. VDD-CPUFB and VDD-SYSFB are voltage feedback signals which should be away from the board edges and traces of some interference signals like DDR, CSI, SD, and Card. If possible, shield VDD-CPUFB and VDD-SYSFB with ground traces or process them with the 3W rule, and connect them to the load along the power plane.

Figure 3-10 Voltage Feedback Signals



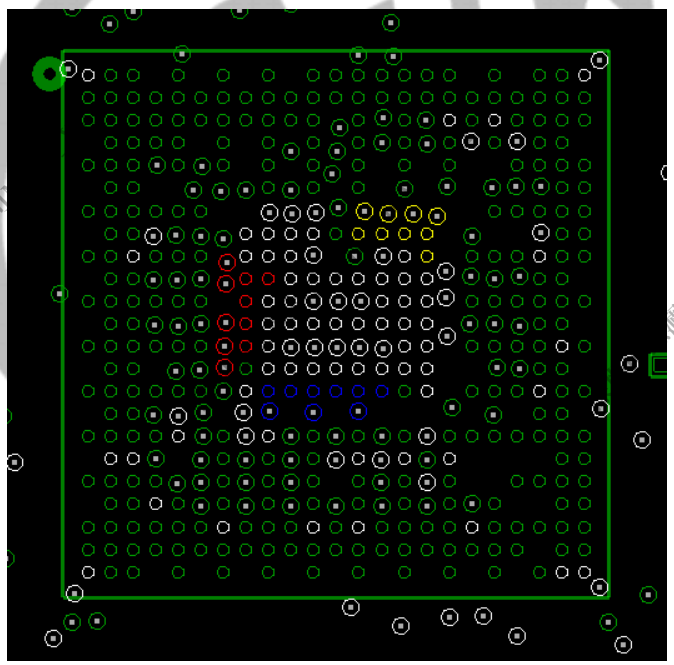
5. To prevent void-welding caused by fast dissipating, do not add a large area of GND shape near the BGA region (except the power balls) on the top layer.

Figure 3-11 Grounding of the BGA Area



6. To avoid the continuous signals and power vias break the continuity in the return path, ensure there are enough GND vias under the chip.

Figure 3-12 GND Vias Under BGA

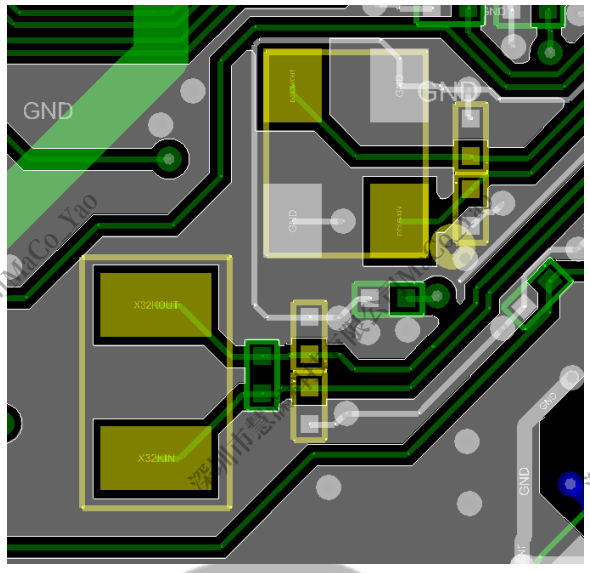


3.4 24 MHz Crystal

1. To minimize the parasitic capacitance of PCB traces and ensure the accuracy of frequency deviation, place the crystal as close to the IC as possible, and make sure the total length of X24MI and X24MO is less than 400 mils.

2. Place the matching capacitor for the crystal close to the crystal pins and shield the surrounding and adjacent layers of the crystal and its traces with GND. Do not route other traces. Avoid routing traces in the position under the crystal at Layer 3.
3. If space allows, ground the GND pin of the crystal and matching capacitor at a single point on the surface.

Figure 3-13 Crystal Circuit



4 Memory

4.1 DRAM

1. Import the DRAM layout template of Allwinner to your layout design. The template has passed the SI/PI simulating and can ensure the DRAM speed and stability.
2. If you fail to import the template, follow the DDR Layout Guide to design your layout. The following table shows the key points of impedance control, timing, and crosstalk.

Table 4-1 Key Points of DRAM Layout

Items \ Signals		DQ, DM	DQS	CLK	ADD, CTRL, CMD	RESET	ZQ
Impedance	Value (Ohm) (± 10%)	50	Differential Impedance: 100		50	50	50
	Reference Plane	GND	GND	GND/VCC-DRAM	GND/VCC-DRAM	GND/VCC-DRAM	GND/VCC-DRAM
Timing	Difference Pair Deviation	-	±5 mils		-	-	-
	Equal Length Settings	≤400, and be equal to DQS in length (Error Margin: ±400)	Be equal to CLK in length (Error Margin: ±800)	-	≤200, and be equal to CLK in length (Error Margin: ±400)	-	-
	T-Type Equal Length Settings (If data and DQS have branches)	-	-	The joining point should be near the memory and the branch length should be no more than 600 mils (Error Margin: ±50 mils)			-
Crosstalk	Spacing within Group	2w	-	-	2w	-	-
	Spacing with Non-DDR Signals	6 h (h is the thickness of the medium between the signal trace and reference surface)					
	Spacing with Power	≥ 15 mils					

Items \ Signals		DQ, DM	DQS	CLK	ADD, CTRL, CMD	RESET	ZQ
	Spacing with GND	⩾ 10 mils					
	Whether to Shield with GND	Shielded with GND if possible, and drill vias to the main GND every 3 mils. If you fail to drill the vias because of the limited space, omitting GND-enclosing is acceptable with the spacing requirements met. For each signal that form the differential signal pair, there must be a GND via near the signal via.					
Others	Recommended Routing Order	DQ, DM, DQS → CLK, ADD → CTRL, CMD → REST, ZQ					

Note:

- When adjusting the trace width, use the 3W rule to minimize coupling between traces. That is, the separation between traces must be three times the width of a single trace when measured from center to center.
- The adjacent layers of all traces should have a complete power or ground plane. The following figures show a 4-layer instance of LPDDR3.

Figure 4-1 GND Plane as the Reference Plane for the Traces

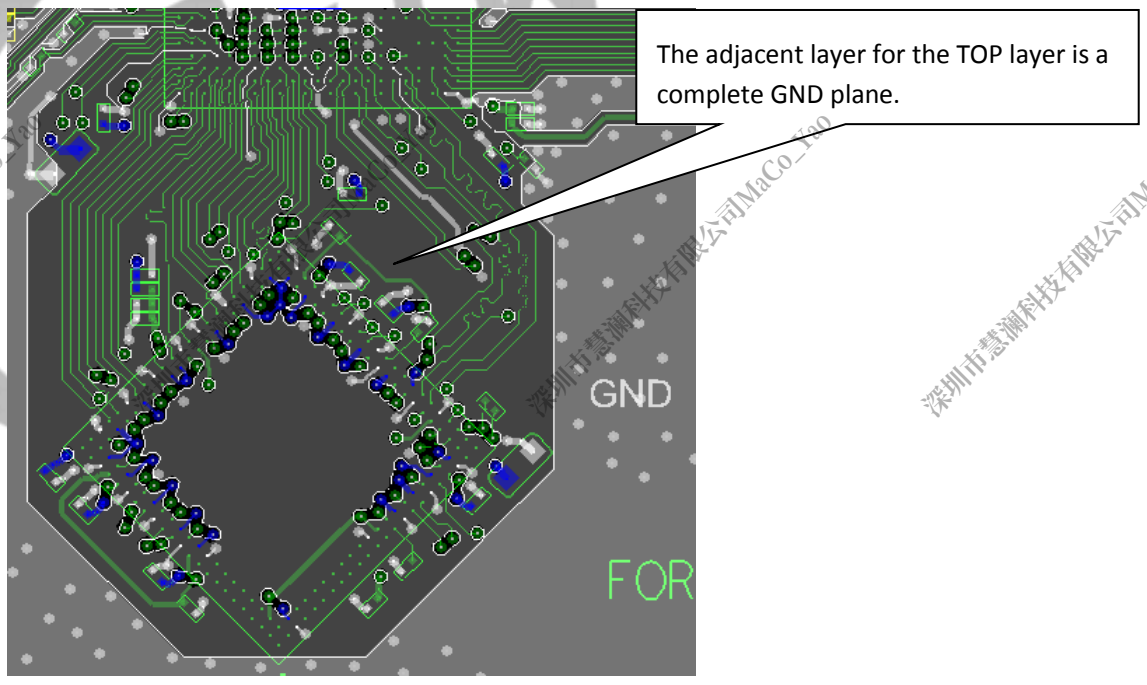
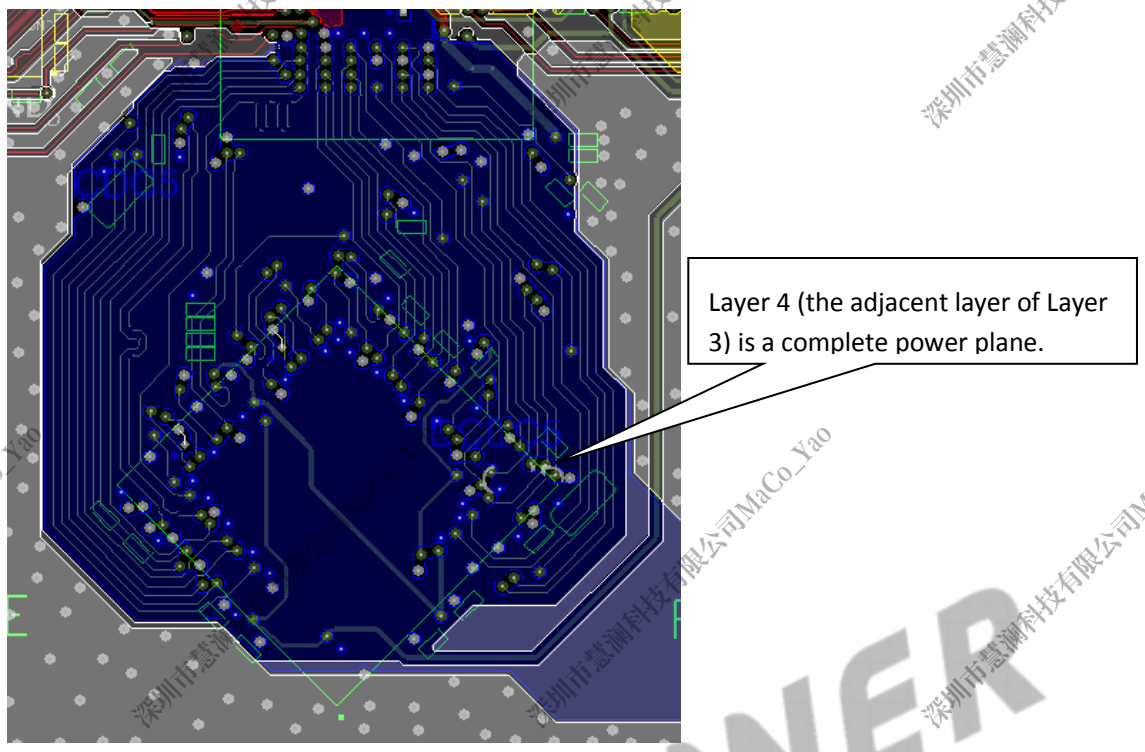
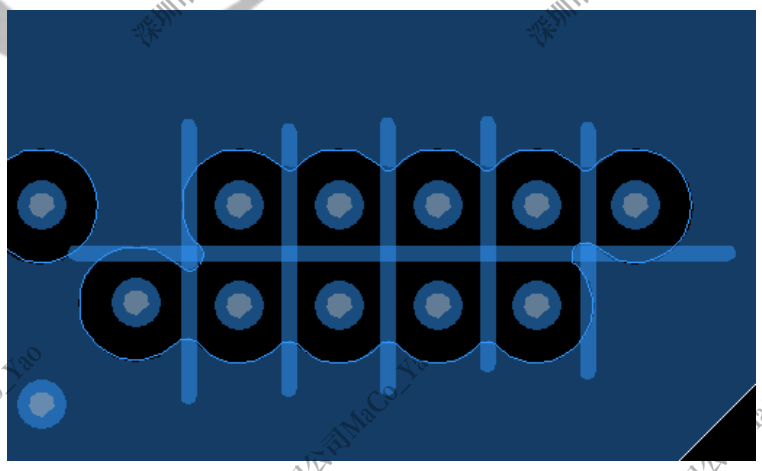


Figure 4-2 Power Plane as the Reference Plane for the Traces



- The traces of CK/CKB, CSx, ODTx, CKEx, Ax, BAx, CAS, RAS, and WE should adopt the Fly-By topology, and the stub should be as short as possible.
- Control the impedance of the differential pairs CK/CKB and DQSx/DQSBx at 100 ± 10% Ohms, the spacing from other networks as 4W (W is the trace width).
- Control the impedance of the single-ended trace at 50 ± 10% Ohms, the trace spacing as 2W (W is the trace width).
- Ensure the trace spacing between Vref and other networks is greater than 4W, and place the bypass capacitor as close to the Vref pin as possible.
- To avoid integrity broken to the power and GND plane, adjust the position and spacing of vias properly. For the breaking area of the plane, use traces for connection.

Figure 4-3 Optimizing the Reference Plane



- For single-side layout, place the power bypass capacitors as close to the power pins as possible. For double-side layout, place them to the bottom side of the PCB that facing the power pins. Drill at

least one power via and one GND via for each capacitor. Evenly distribute the capacitors and place the one with smaller capacitance nearer to the power pins.

Figure 4-4 Bypass Capacitor for Single-Plane Layout

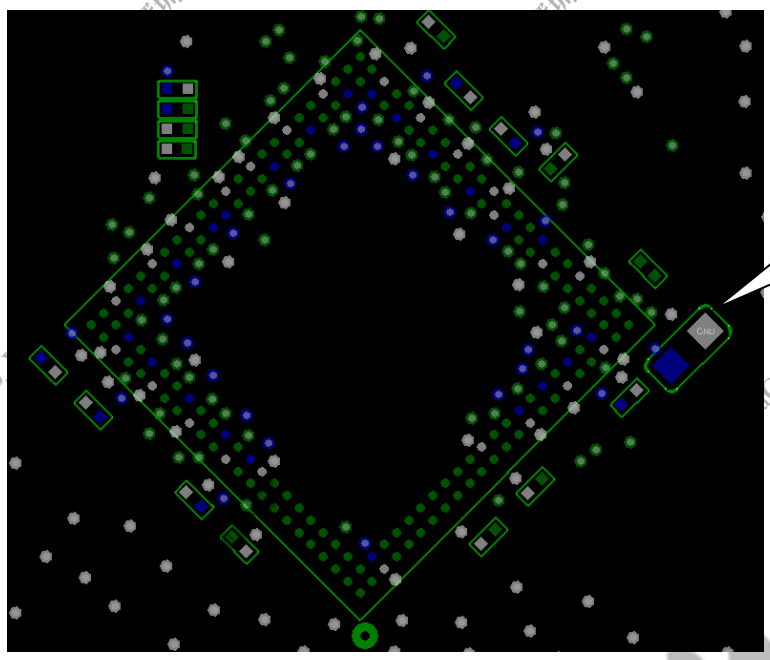


Figure 4-5 Bypass Capacitor for Double-Plane Layout

CAUTION

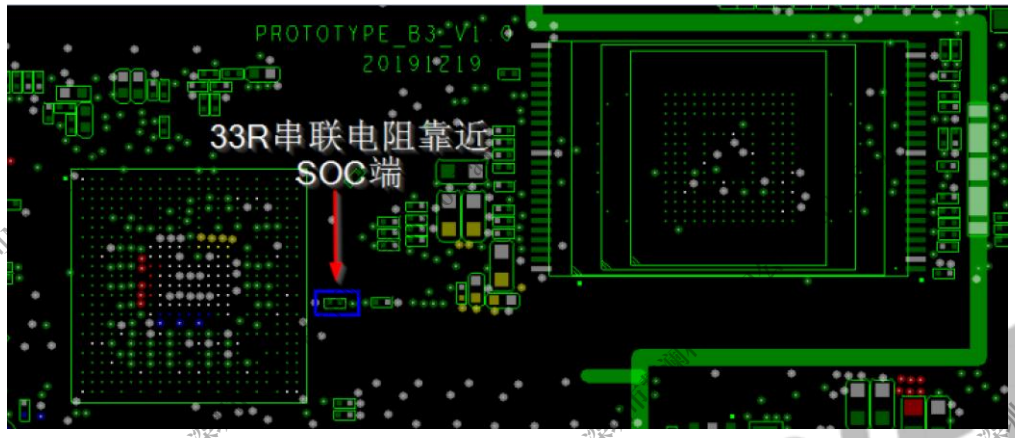
- It is strongly suggested that you adopt Allwinner stack up settings. If you do need to adjust the thickness of the whole board, adjust the dielectric thickness of the middle layers, and keep the thickness of the signal layers and their reference layers unchanged.
- When providing GERBER files to the PCB manufacturer, pay attention to the following items:
  - Ask the manufacturer not to decrease the trace spacing when adjusting the impedance of the DDR signal traces and require the engineering department to double-check this.
  - If you need to increase the trace width for impedance control, contact Allwinner FAE for evaluations and validations.

4.2 NAND/EMMC

4.2.1 Layout

1. Place the eMMC/NAND near the SoC and the SoC decoupling capacitor near the SoC power supply pin.
2. Place the 33R series resistor of CLK/RE signal source near the SoC, and ensure the trace length between the series resistor and the CLK of SoC is not greater than 300 mils.

Figure 4-6 Placing the 33R Series Resistor

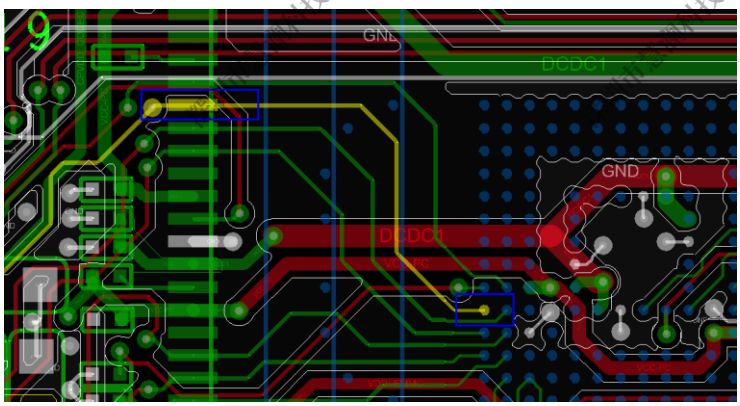


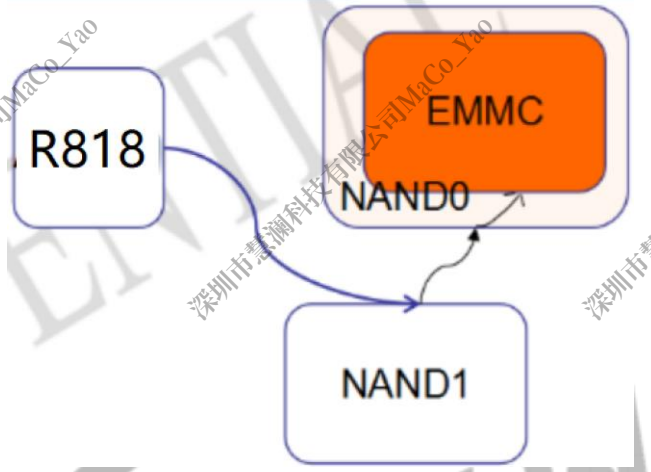
3. Place the pull-down resistor near the eMMC and ensure the stub length is not greater than 200 mils.

4.2.2 Traces

1. Ensure the trace length of eMMC/NAND and the SoC is not greater than 2000 mils. Control the impedance at 50 Ohms and the trace spacing not less than 2W (W is the trace width).
2. Set the D0−D7, and DS to be equal length to CLK/RE with the error margin within ± 300 mils. If possible, control the number of the vias for D0−D7 consistent.
3. Try to make the reference plane for all signal traces except Reset complete.
4. Ensure the width of the power traces is not less than 12 mils.
5. Shield the CLK (RE, WE, and DQS) and DS signals with ground traces, and connect the ground traces to the GND plane through vias. If you fail to shield them with ground, ensure the trace spacing is not less than 3W, and keep them away from high-frequency signals.
6. For eMMC/NAND or NAND with various packages, when it is double-layout, it should adopt the daisy-chain topology. Use eMMC or the component with the highest read/write speed as the end of the trace, and try to shorten the branch length. If the eMMC needs to run at a high frequency, you are suggested to use eMMC only, and ensure the eMMC to the IOs of the SoC are point-to-point (as shown in Figure 4-7).
7. Keep the EMMCNC and RFU pins floating. Do not connect them to the power, GND, or other eMMC signals for routing convenience. If you have trouble routing traces, modify the eMMC PCB package and remove some NC/RFU balls.

Figure 4-7 eMMC/NAND Double-lay Routing





5 PMU

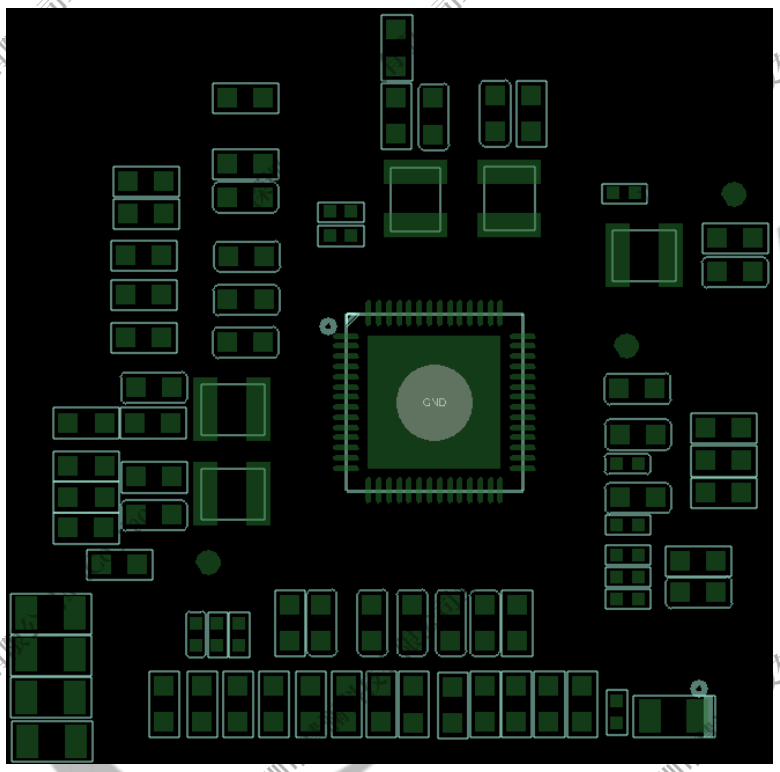
5.1 Layout

To ensure the power flows smoothly to the destination, place the capacitors and inductors for DC-DC (Buck and Boost) and LDO near the pins, and the priority for components to be placed close to the PMU is as follows:

- High priority: VBUS, ACIN bypass capacitors, DC-DC input, and the output bypass capacitors.
- Middle priority: Buck/Boost inductors and bypass capacitors for VREF and VCC-RTC.
- Low priority: bypass capacitors for LDO and SWOUT.

The following figure shows the layout for the bypass capacitors in the PMU module.

Figure 5-1 Layout for the Bypass Capacitors in PMU Module

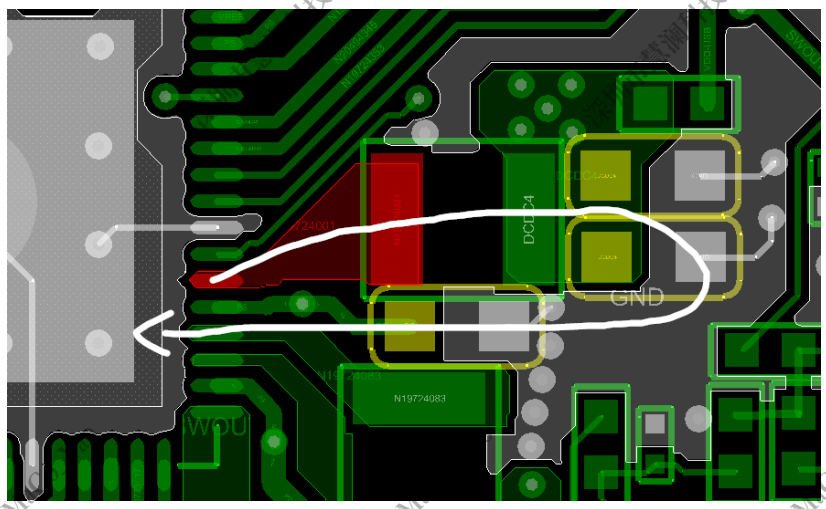


5.2 Traces

5.2.1 Power Traces

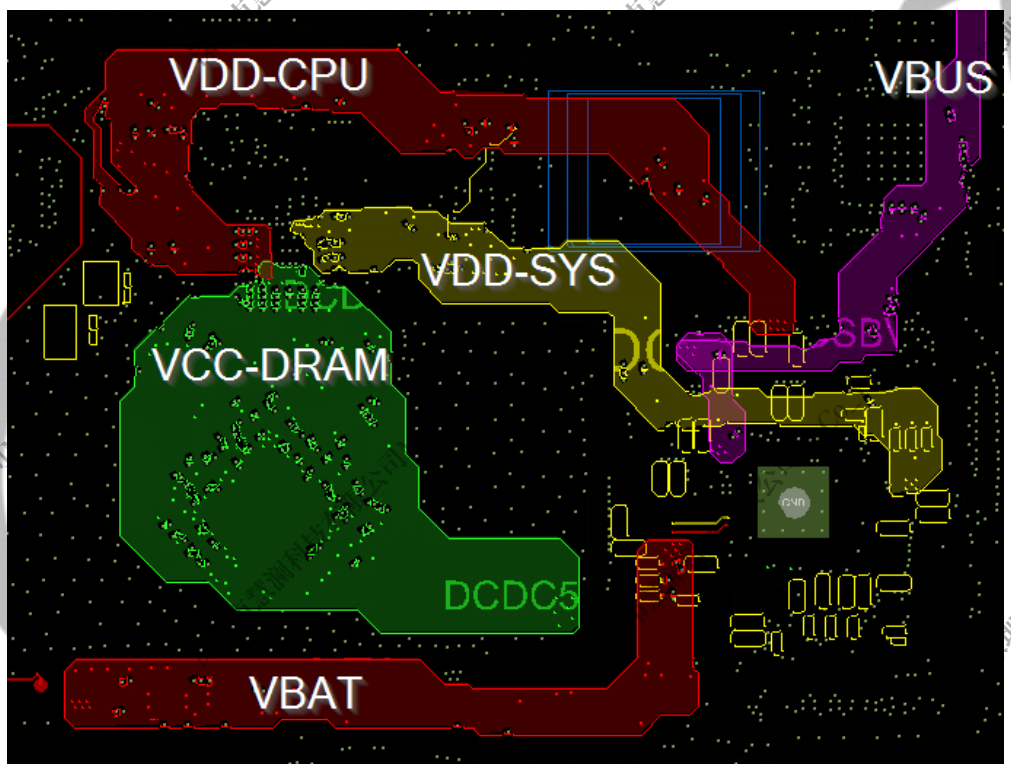
1. Minimize the loop area formed with the DC-DC (Buck) output capacitors, inductors, and feedback lines.
2. Keep the trace segment near the PMU pins as wide as the pad, and then widen the rest segments. Set a trace width that just meets the overflow needs. An over-wide trace for the alternating current (AC) may cause EMI problems.

Figure 5-2 AC Loop



3. To minimize the voltage drop, add shape among the ACIN (PS) and all DC-DCs with the trace width as greater as possible.

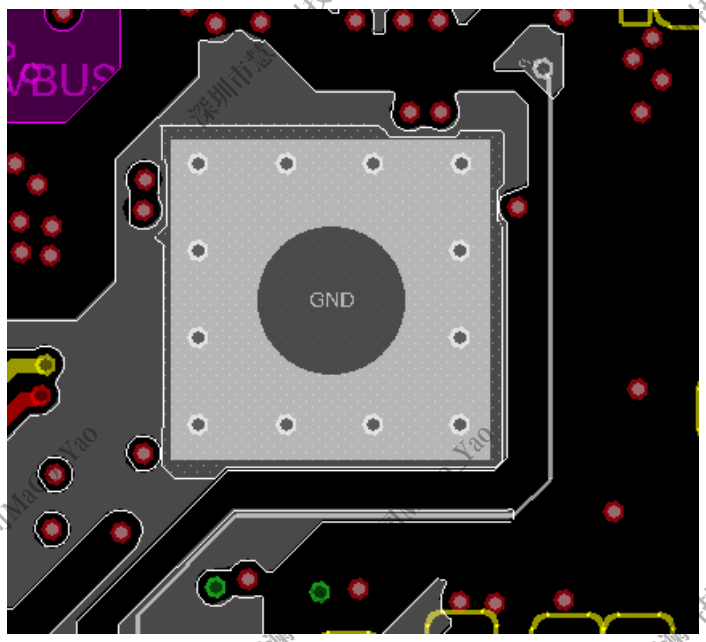
Figure 5-3 DC-DC Traces



5.2.2 Other Traces

1. Fully connect the e-pad that is under the PMU to the ground plane. Add some GND vias regularly to ensure all layers are fully grounded.

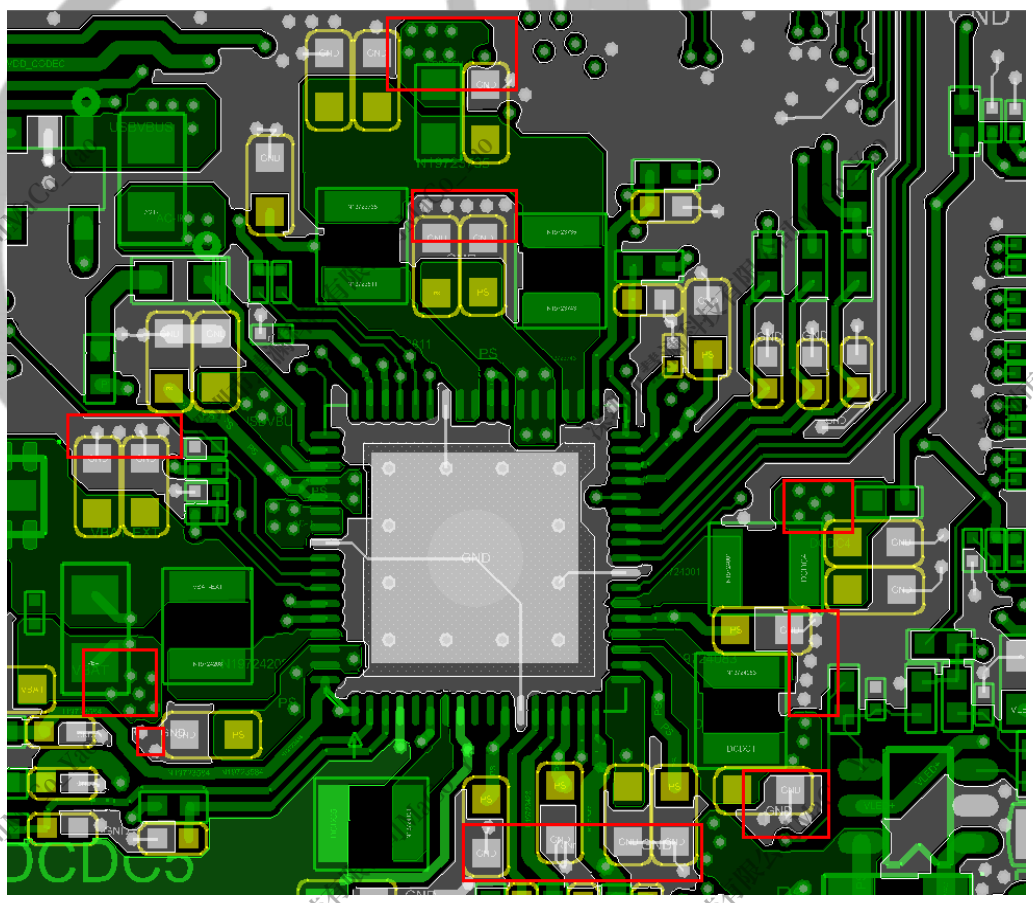
Figure 5-4 Add GND Vias on PMU cooling Pad



2. Generally, the number of vias is limited by the space around the PMU. For current that is smaller than 1 A, drill at least one via. For current that is from 1 A to 2 A, drill at least two vias. For current that is from 2 A to 3 A, drill at least 3 vias.

3. Add as many GND vias as possible around the buck capacitors to reduce the loop inductance.

Figure 5-5 Add GND Vias around Buck Capacitors

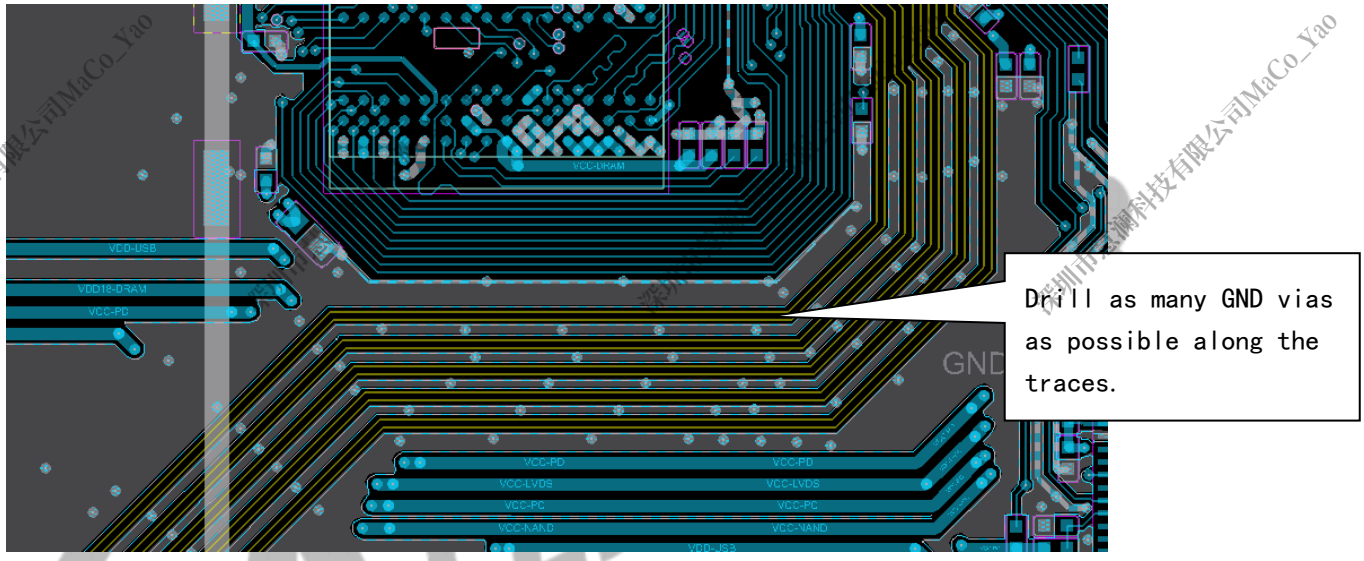


6 Interface

6.1 MIPI DSI

1. Control the differential impedance at 100 ± 10% Ohms. Ensure the reference plane complete and the differential pairs are equal length with the error margin within ± 50 mils.
2. Ensure the spacing between two differential pairs is not less than 12 mils.
3. Ensure the trace length is not greater than 3000 mils. For the 6-layer board, route traces on the inner layers if possible.

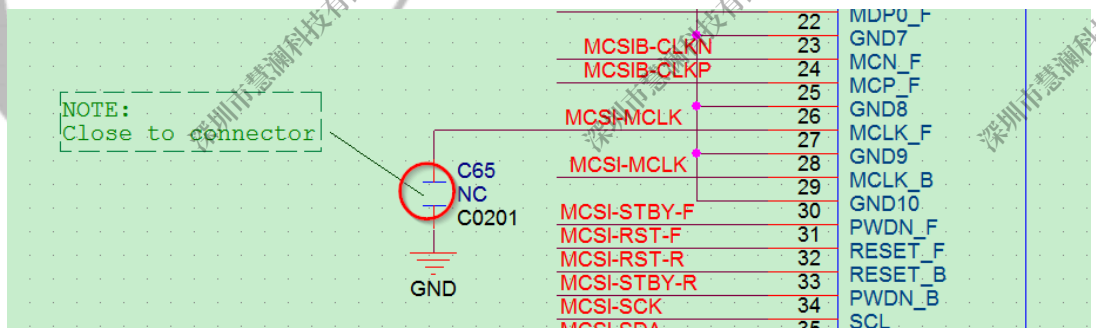
Figure 6-1 MIPI-DSI Traces



6.2 MIPI CSI

1. Place the grounded capacitor near the module and the series resistor near the SoC.

Figure 6-2 MCLK Bypass Capacitor



2. Control the impedance of the differential pairs MIPI at 100 ± 10% Ohms. Route traces with the minimum length and avoid changing layers if possible. Drill as many GND vias as possible on both sides of the traces.
3. For the traces within the differential pairs, set equal length with the error margin within ± 10 mils. For the traces among the differential pairs, set equal length with the error margin within ± 300 mils.
4. Place the test point near the SoC.

Figure 6-3 Placing the MCLK Series Resistor near the SoC

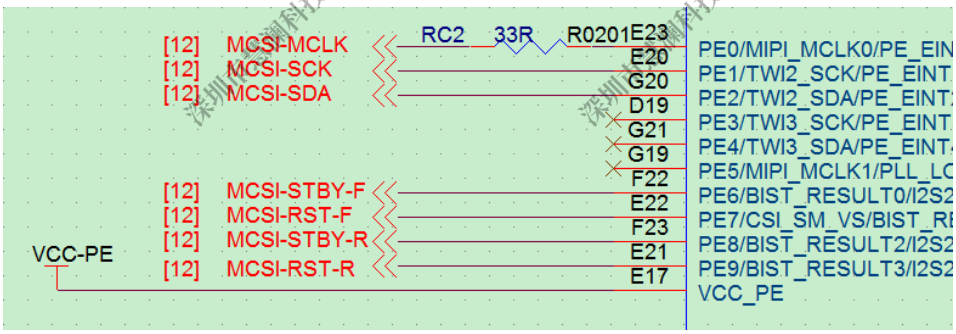
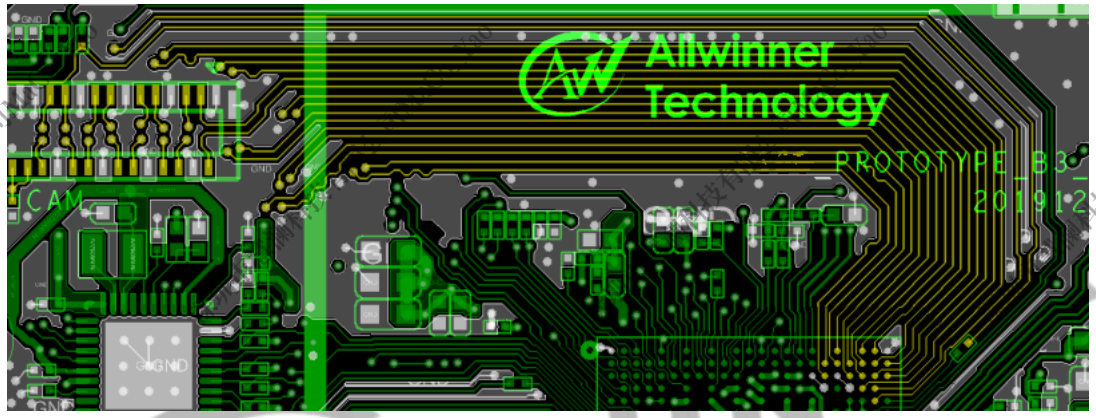
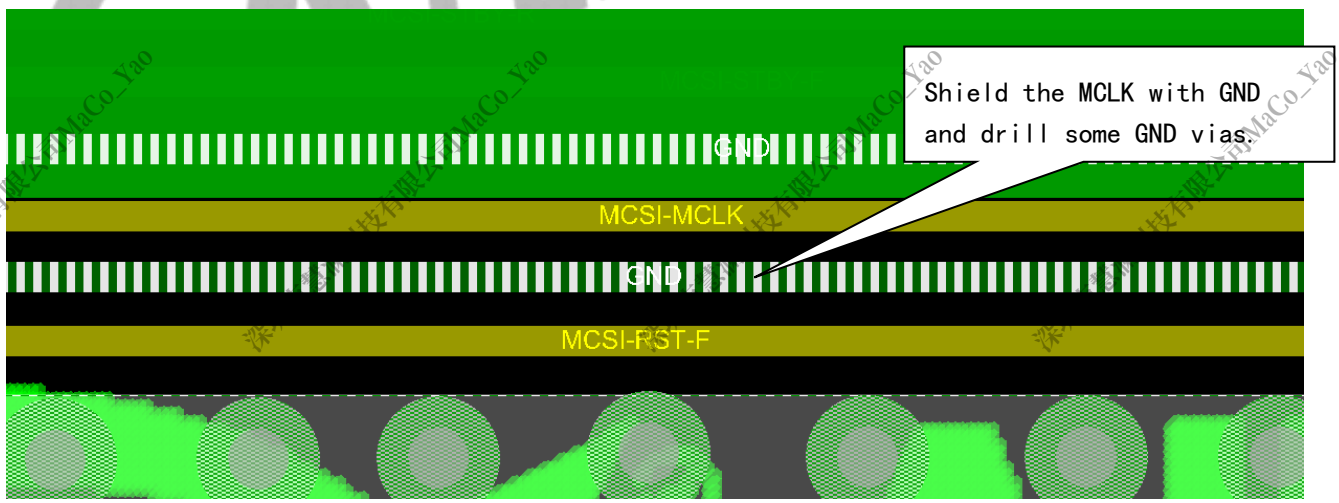


Figure 6-4 MIPI-CSI Traces



5. Shield the MCLK with ground traces. Route traces with the minimum length and avoid changing layers if possible. For the 6-layer board, route traces on the inner layers to improve the EMC performance.

Figure 6-5 Placing the MCLK Series Resistor near the SoC



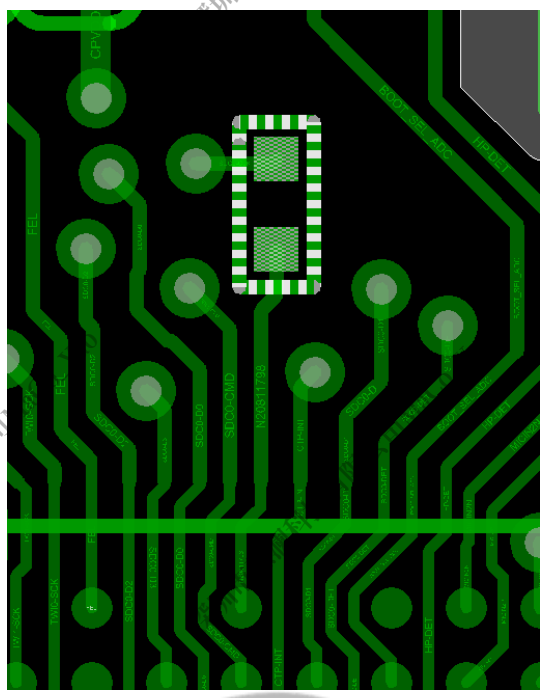
6.3 SDIO

6.3.1 Layout

1. Place the 33R series resistor of CLK near the SoC, and ensure the trace length between the series resistor and the CLK of SoC is not greater than 300 mils.
2. Place the ESD components near the corresponding pins of the connector or Wi-Fi module.
3. Place the resistors and capacitors of the VDD network near the connector or Wi-Fi module.

4. To avoid the pins of plug-in components interfere with the cards' insertion and extraction, do not place any plug-in components on the bottom of the connector.

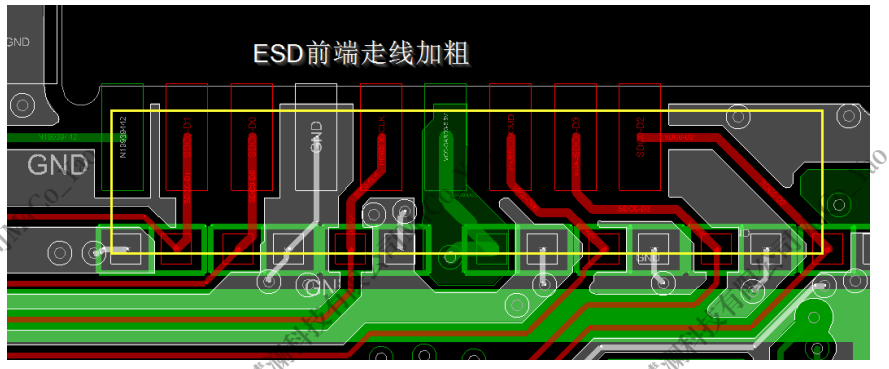
Figure 6-6 SDIO Series Resistors Layout



6.3.2 Traces

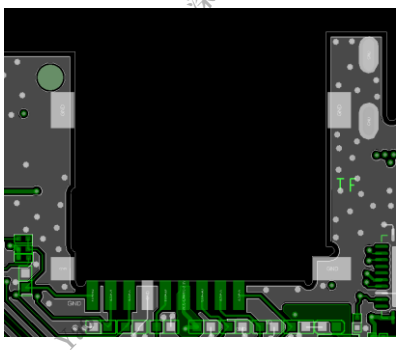
1. When routing traces, follow the guidelines below:
   - Control the trace impedance at 50 Ohms.
   - Ensure the trace spacing is not less than 2W.
   - Ensure the traces from CLK to D0–D3 are equal length, and the trace length is not greater than 500 mils.
   - Shield the CLK with ground traces and drill some GND vias on the ground traces for connecting to the ground plane. If space is limited, use the 3W rule to protect the CLK instead.
   - Keep the traces away from high-frequency signals.
2. R818 supports SDIO 3.0. The VDD width is suggested to be greater than 25 mils.
3. Connect the pins of the connector to the ESD components first, and then to other components. Widen the trace segment near the ESD. For the rest segment, avoid overlapping with the adjacent layers.

Figure 6-7 Widening the Trace Segment near the ESD



4. Fully ground the pad of the connector.

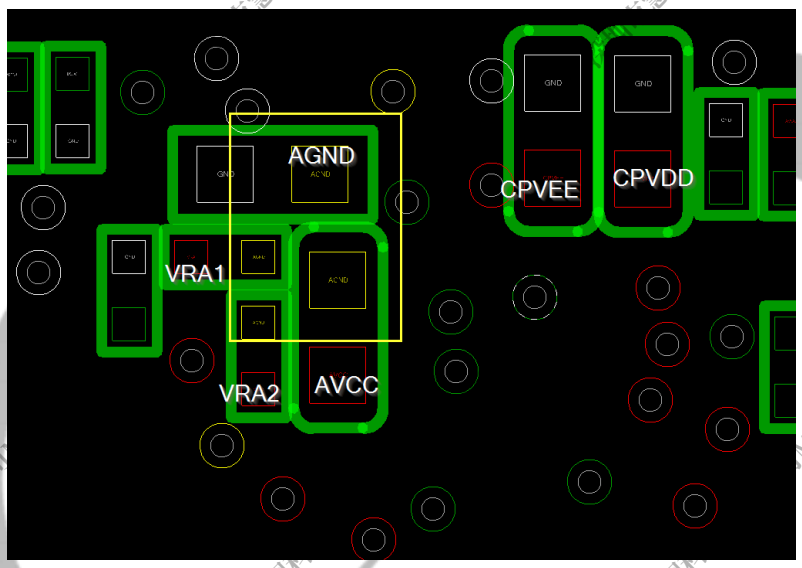
Figure 6-8 Fully Ground the Pad of the Connector



6.4 Audio

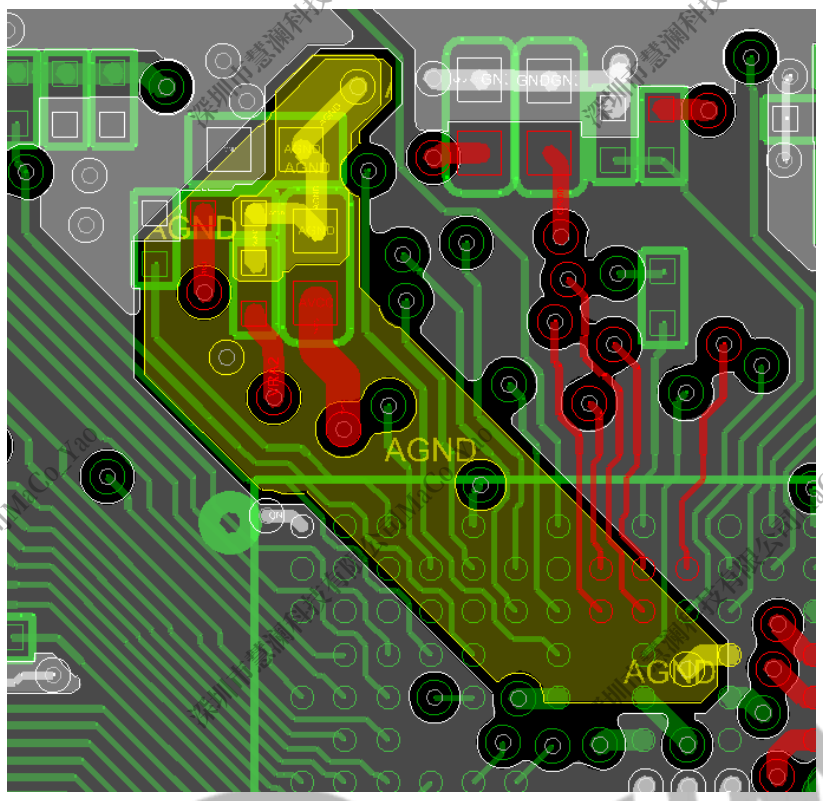
1. Place the grounded capacitors and resistors of AVCC, VRA1, VRA2, and AGND near the SoC.

Figure 6-9 Layout for the Audio Signal Bypass Capacitor



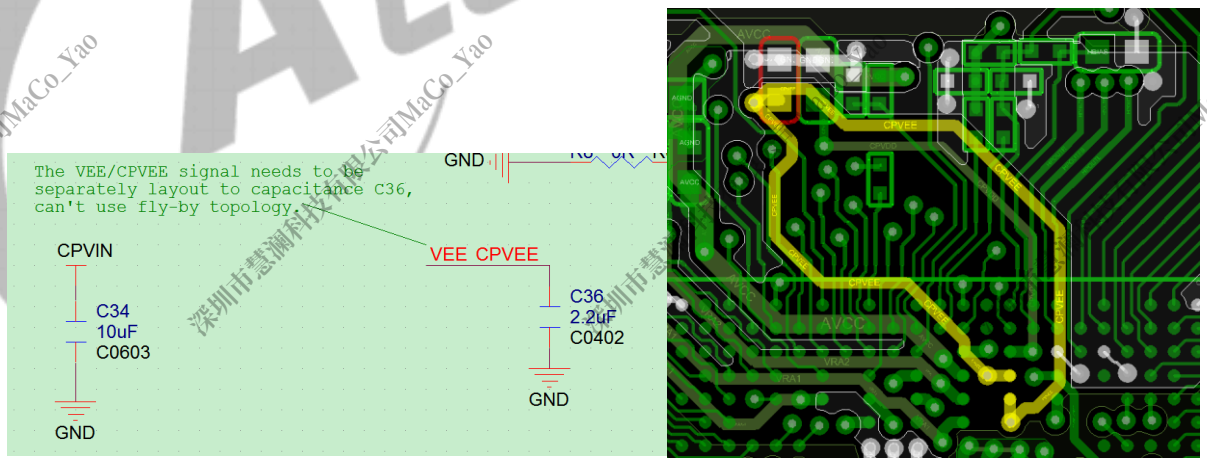
2. For AVCC, set the trace width not less than 16 mils. For VRA2, set the trace width not less than 10 mils and the trace width not greater than 300 mils. Keep them away from interference signals.
3. For AGND, set the trace width not less than 80 mils and add a shape if possible. Drill at least two GND vias for connecting the grounded resistors and the ground plane.

Figure 6-10 AGND Traces



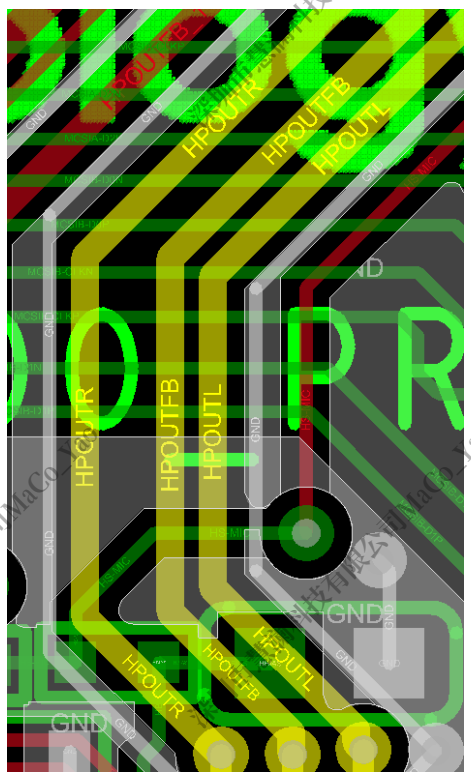
4. Use the start topology to connect the APVEE and VEE with the capacitor acts as the center. Do not directly connect them inside BGA. Set the trace width as 10 mils (trace width inside BGA should not be less than 6 mils).

Figure 6-11 Layout for the Audio Signal Bypass Capacitor



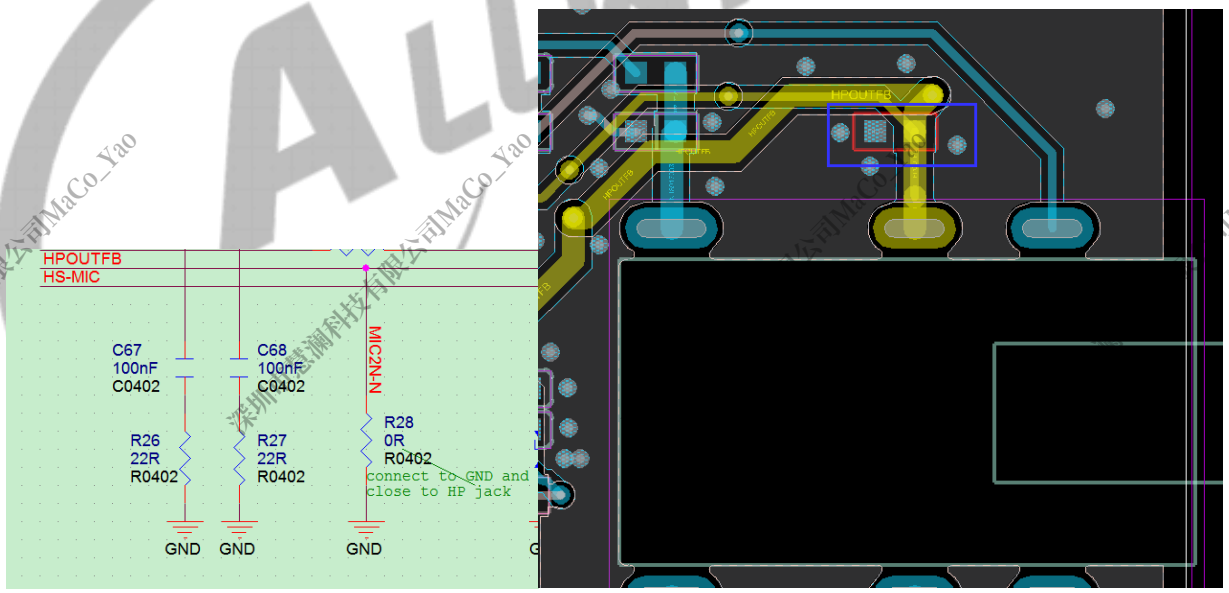
5. Route the traces for HPOUTL, HPOUTFB, and HPOUTR in parallel with the HPOUTFB in the middle and HPOUTL and HPOUTR on both sides. Set the trace width as 10 mils. Treat the three traces as a group and shield the group with ground traces. Keep the traces and vias away from high-speed signals and clock signals.

Figure 6-12 Traces for POUTL, HPOUTFB, and HPOUTR



6. Place the GND near the headphone jack and set the trace width not less than 15 mils.

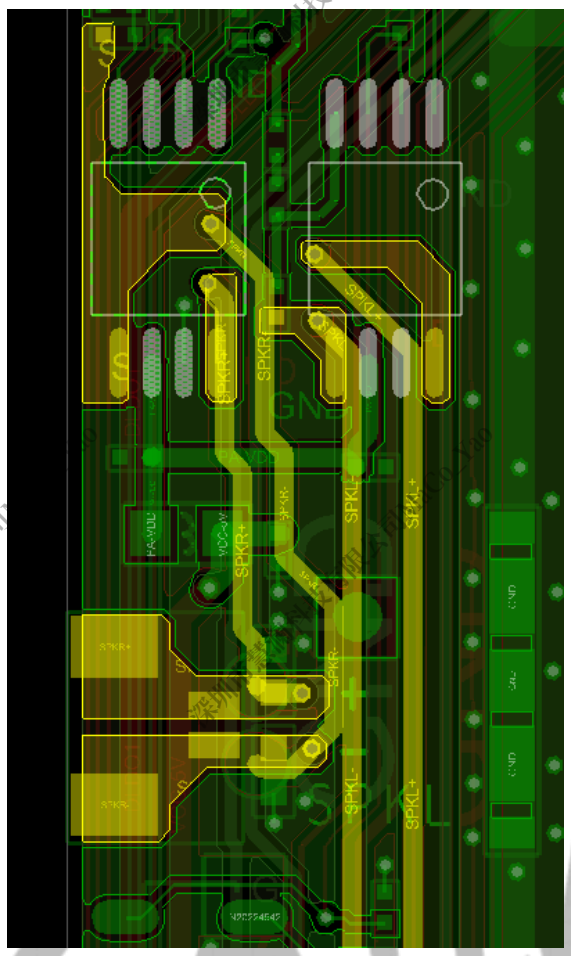
Figure 6-13 HSGND Traces



7. Route the traces for MBIAS, HBIAS, and MICxP/MICxN in parallel with the trace width of 10 mils. Treat the three traces as a group and shield the group with ground traces.

8. For HPOUTL and HPOUTR, widen the traces after the amplifier. The width of the traces near the BGA should be at least 16 mils. For the power amplifier traces pass through the magnetic bead, it is suggested that the width be at least 20 mils.

Figure 6-14 SPKP/N Traces



9. To ground the headphone with the MIC feature, pay attention to the following items:

- Ground MIC2N-N/HPOUTFB at a single point near the headphone jack, and route two independent traces for the two signals instead of merging the traces.
- Group MIC2N-N and HS-MIC as a pseudo-differential pair. Route traces in parallel.

Figure 6-15 Circuit Example for Headphone MIC

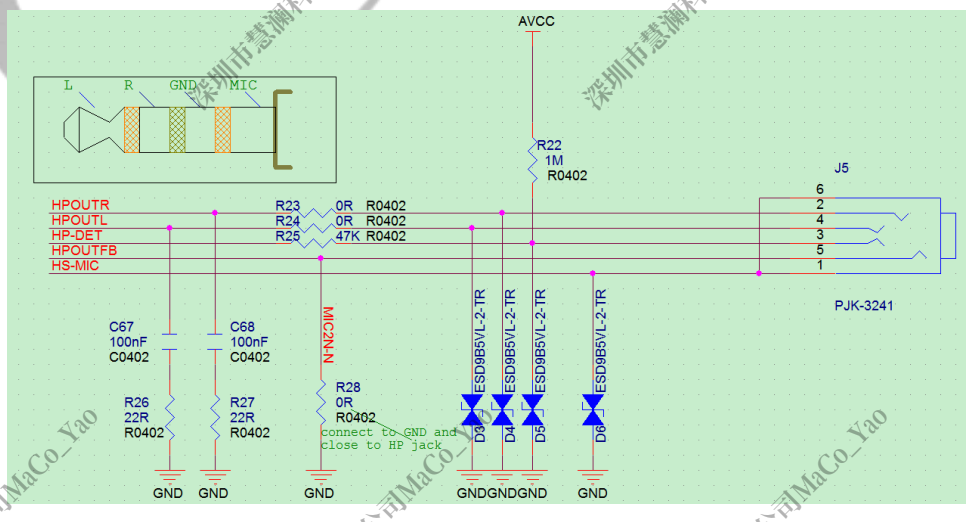
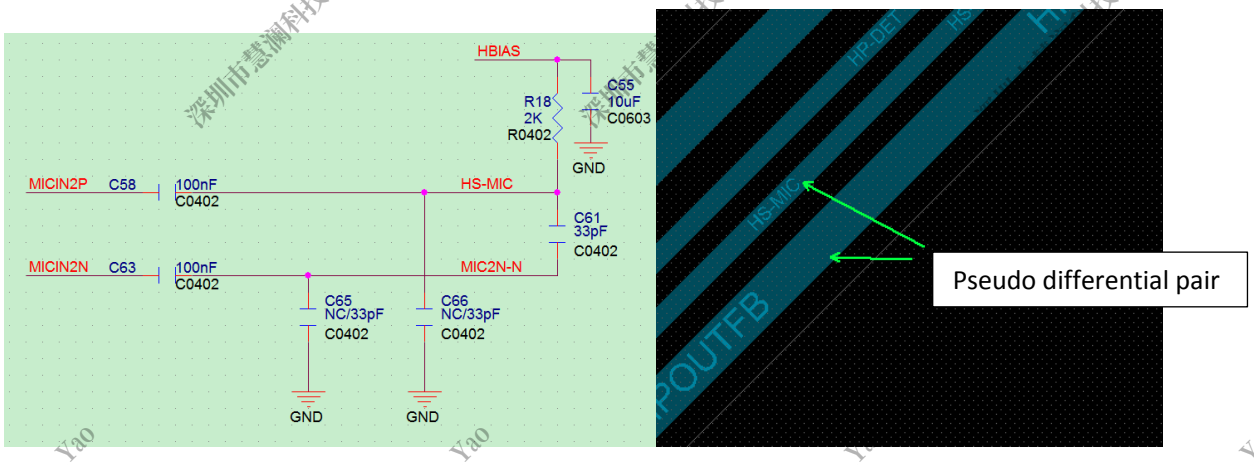


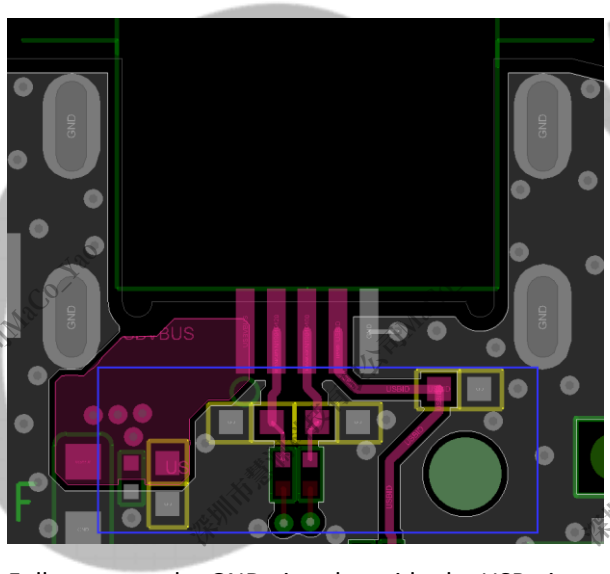
Figure 6-16 Traces for Headphone MIC



6.5 USB

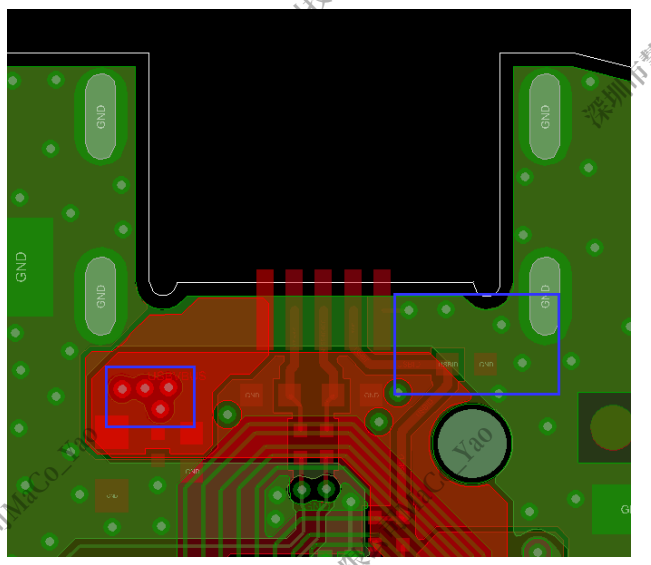
1. Place the ESD components on the same side of the board and close to the corresponding pins of the socket. The front end of ESD must be on the same layer.
2. To better discharge the static electricity, drill at least two GND vias for the GND pins of the ESD components, and the more the better.

Figure 6-17 ESD Processing in USB Circuit



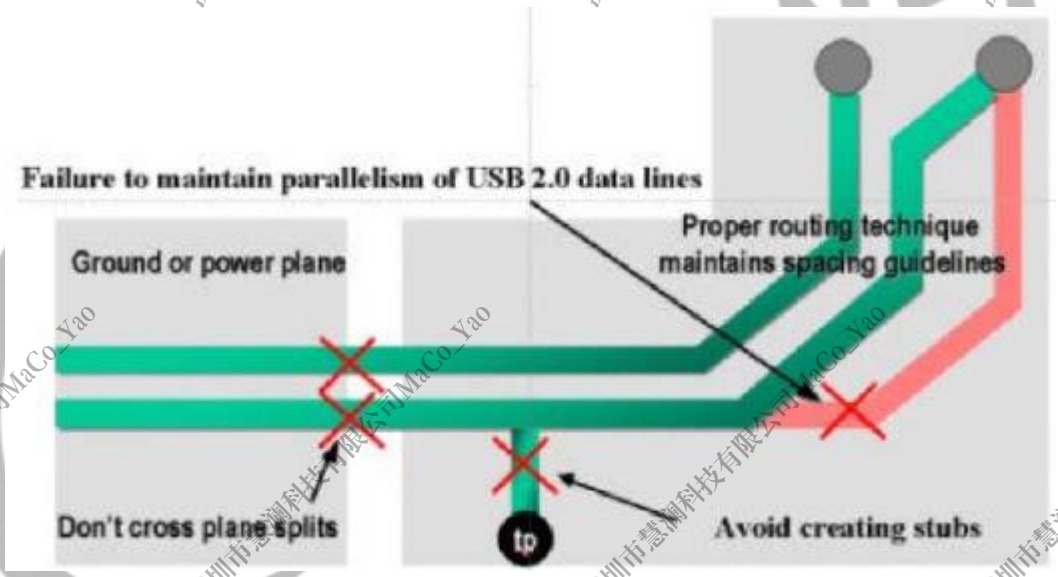
3. Fully connect the GND pins alongside the USB pin to the ground shape around. Drill as many GND vias as the VBUS power vias.
4. On each layer, fully connect the fixed GND pins of the USB socket to the ground shape.

Figure 6-18 Fully Connecting the Fixed GND Pins of the USB Socket to the GND Shape



5. Control the differential impedance of USB DP/DM at 90 ± 10% Ohms. Ensure the reference plane of the adjacent layers complete, and the trace length is not greater than 4000 mils.

Figure 6-19 Differential Traces for USB



6. If possible, avoid changing layers when routing traces for USB D+/D-. The maximum number of layer transfer vias is two. Drill as many GND vias as the layer transfer vias.

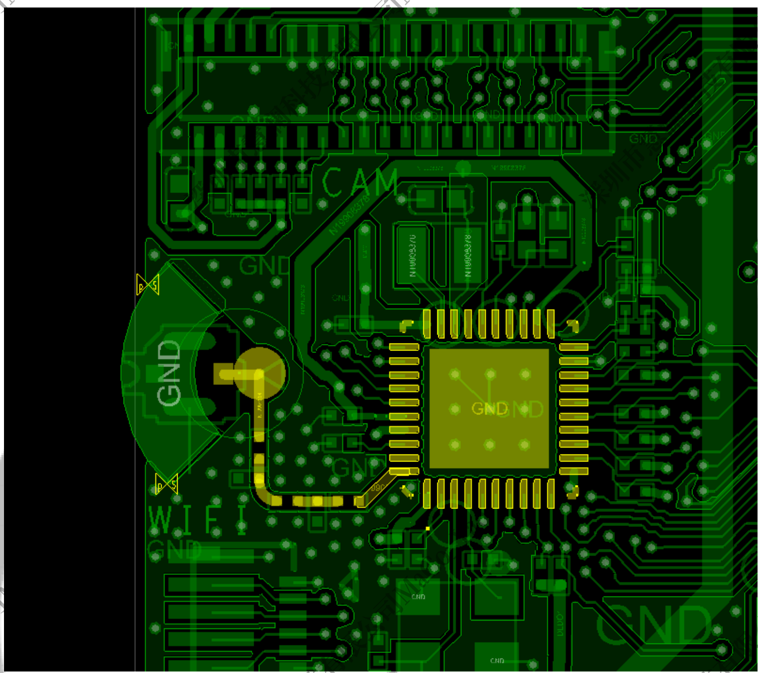
7 Wi-Fi/BT

1. Place the module as close to the antenna pad as possible and keep it away from interference sources like the large power supply, DDR, LCD circuit, cameras, and speaker. Protect the module with an individual shield casing.

2. Properly lay out the matching capacitors and resistors of the antenna so that the feedback line is smooth, short, and with no stubs, no vias, and fewer corners.

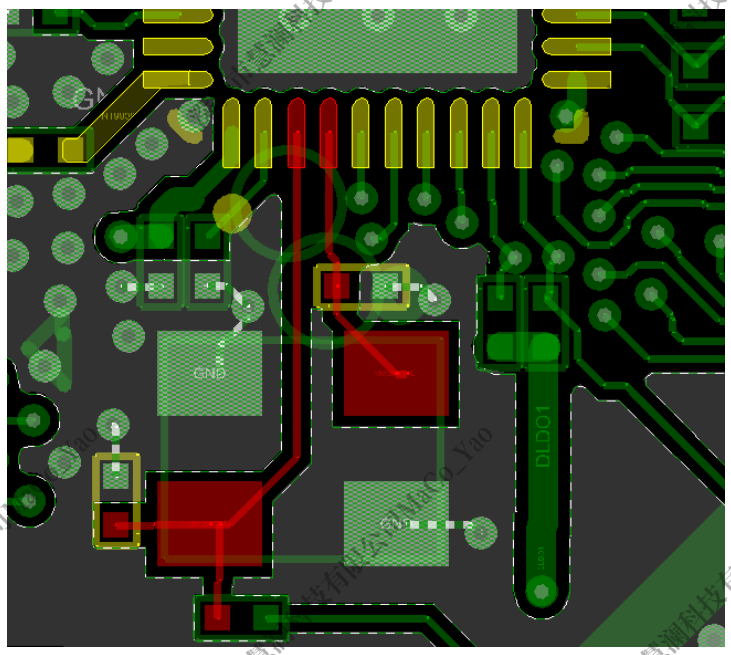
3. Control the impedance of the antenna at 50 ± 10% Ohms. Shield it with ground traces and drill some GND vias along the ground traces with the via spacing within 30 mils. Hollowed out the adjacent layers of the antenna feedback line to widen the traces and reduce loss. Set Layer 3 as a complete GND reference plane. For a 4-layer board, use Layer 2 as the complete GND reference plane instead because the dielectric between Layer 2 and Layer 3 is too thick.

Figure 7-1 Layout for the Wi-Fi Module



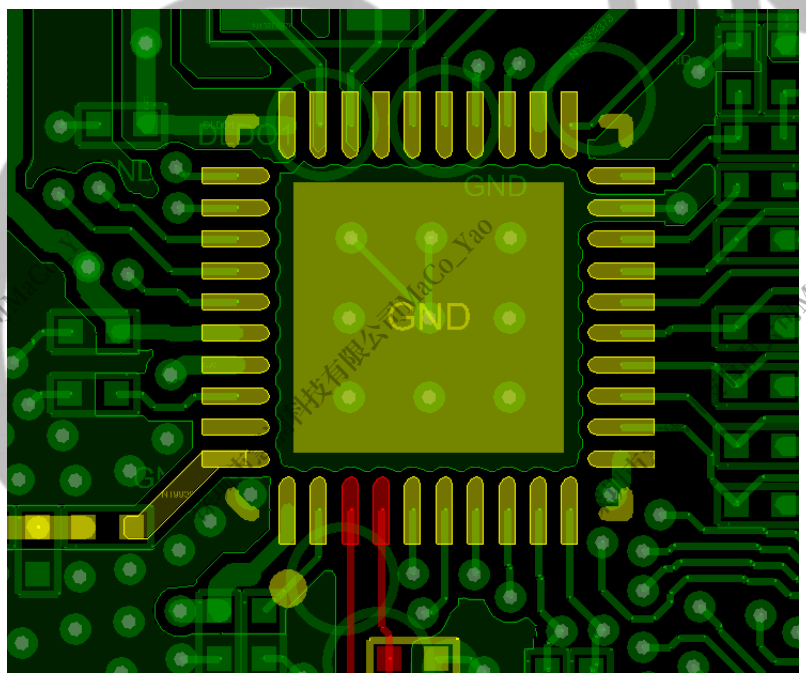
4. Place the crystal near the module and the matching capacitors near the corresponding pins of the crystal. Shield the traces with ground in 3D.

Figure 7-2 Layout for the Crystal Circuit



5. Avoid sensitive signal traces at layers under the Wi-Fi chip. Keep the GND shape complete right under the chip and try to drill some GND vias.

Figure 7-3 Keep the GND Shape Complete under the Wi-Fi Chip



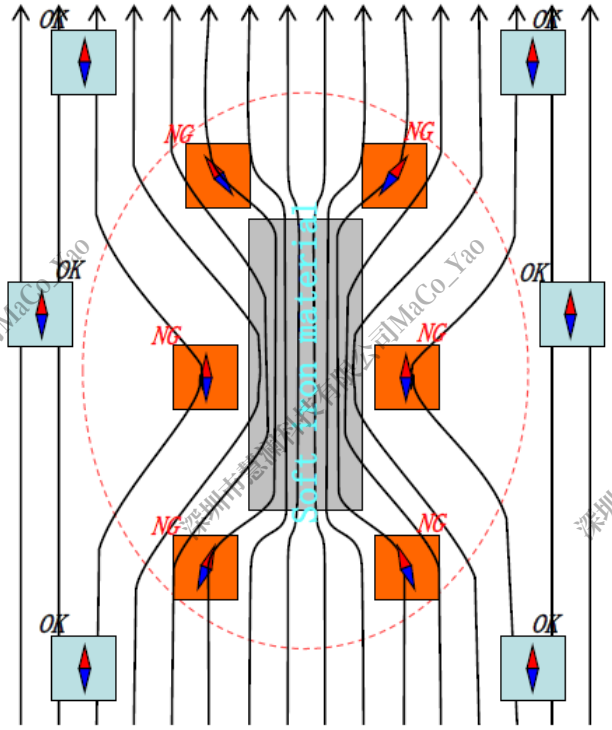
6. For the VCC-WIFI, the trace width should be not less than 30 mils. Drill two layer transfer vias for it. Then drill some GND vias near the bypass capacitor (the more the better).

7. Shield AP-CK32K-OUT and AP-CK24M-OUT with ground traces and keep the traces short. Do not change layers on the AP-CK24M-OUT traces.

8 Sensor

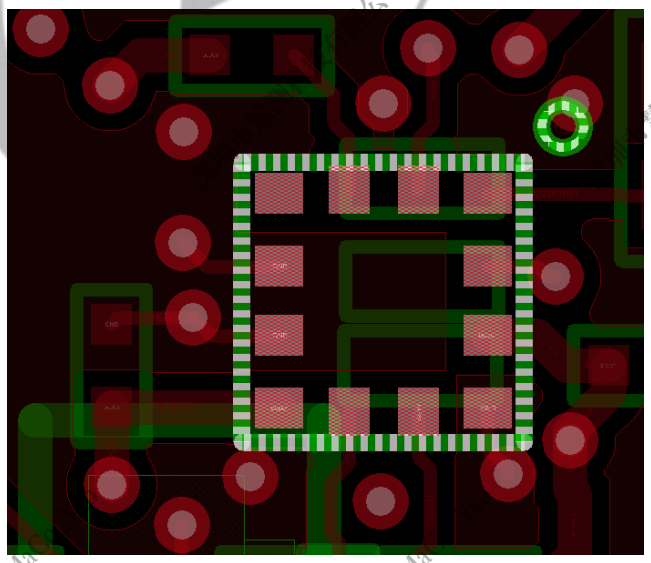
1. Keep COMPASS away from magnetic interferences like the SD connectors, RF shield casings, SIM card connectors, cameras, speakers, motor, and screw-holes.

Figure 8-1 Magnetic Field Lines Around Large Power Supply



2. To avoid affecting the accuracy and introduce sensor drift, keep the sensor away from heat sources like the SoC and PMU.
3. Do not drill any vias under the G-sensor. Keep it flat.

Figure 8-2 Flat Position under G-Sensor



9 ESD/EMC/Heat

9.1 ESD

1. When designing a stack-up PCB, ensure there is at least one complete layer for the GND plane and connect all ESD discharging traces to the GND plane through vias. A complete GND plane helps to fast transfer the charge.

2. Leave the copper exposed at the PCB surface and around the interfaces of components, and drill as many GND vias as possible for connectin to the GND plane. The exposed copper is used for connecting the conductive foam and metal planes like the LCD middle frame and metal shell.

Figure 9-1 Exposed Copper Around the Interfaces of Components

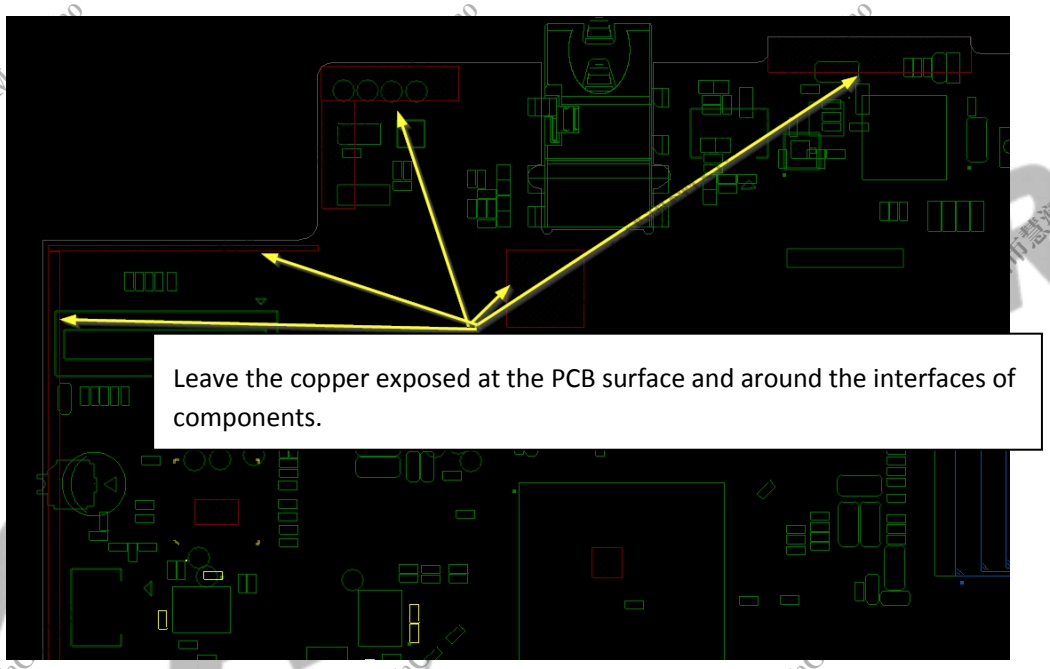
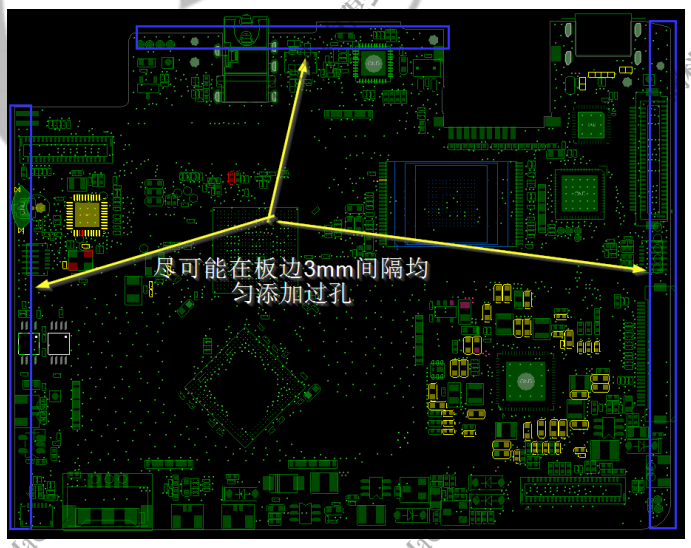


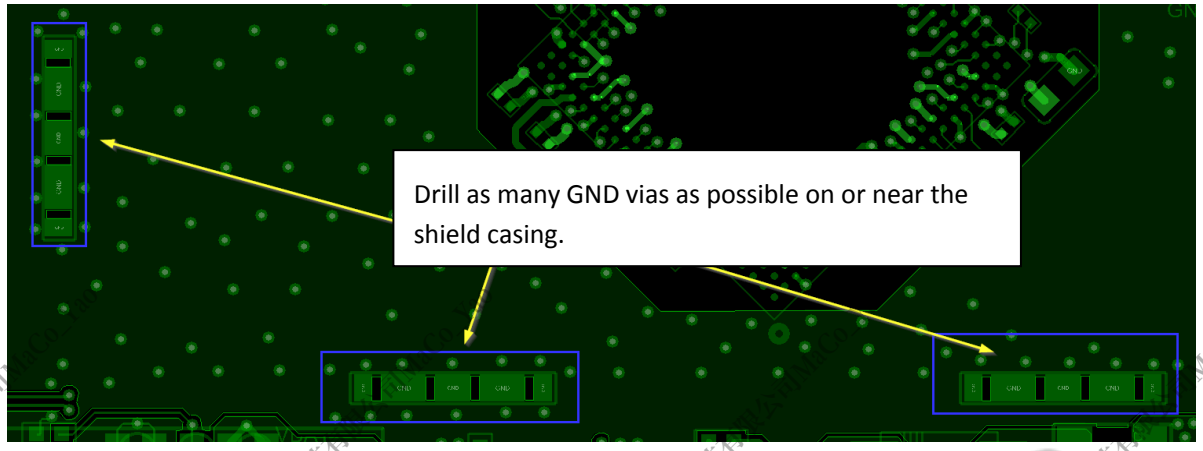
Figure 9-2 Drilling Vias Every 3 mm at the Board Edge



3. To avoid air discharges and electromagnetic coupling with the GND plane, keep the key signals like Rest, INT, and Clock at least 5 mm away from the board edge and 10 mils away from the GND shape which is at the board edge of the signal layers.

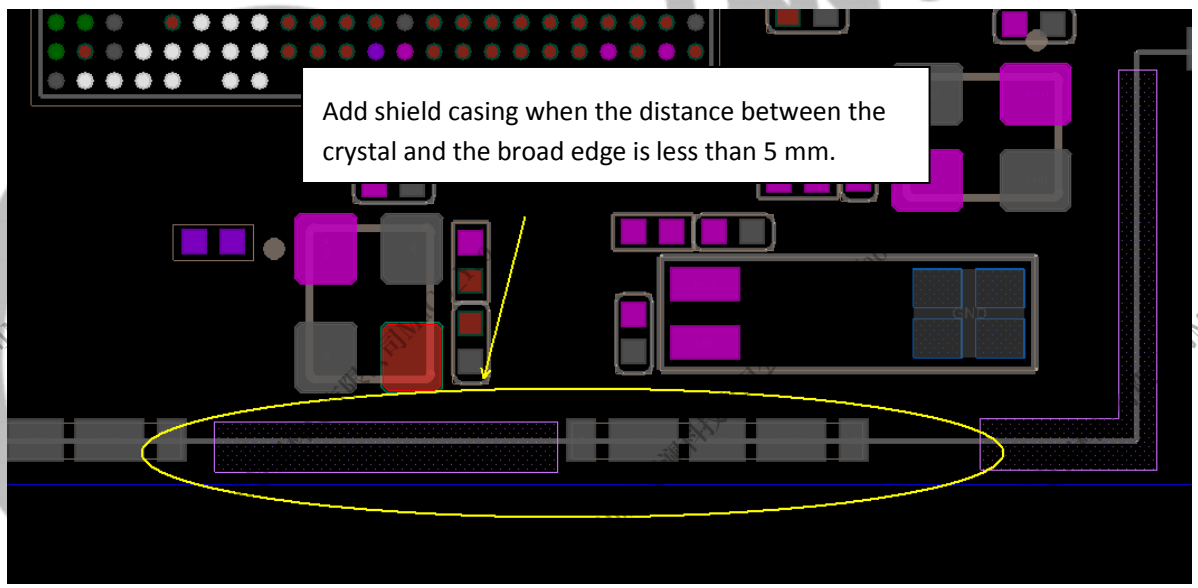
4. Shield the key circuit. Drill as many GND vias as possible on or near the shield casing to ensure all sides of the shield casing are well-grounded, which can prevent it from discharging to the inner components because of charge accumulation.

Figure 9-3 GND Vias on or near the Shield Casing



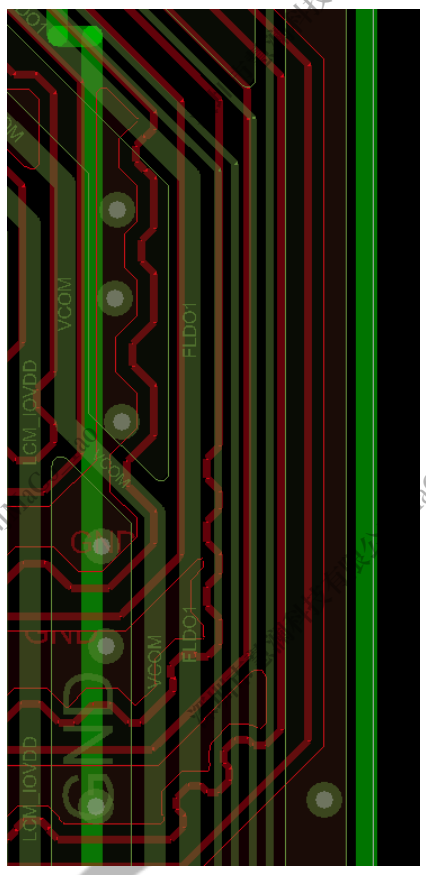
5. Keep ESD-sensitive components like CPU, DRAM, and crystal at least 20 mm away from the external metal interfaces. If the distance is less than 20 mm, shield them with a metal casing and keep it at least 5 mm away from other board edges (avoid the metal connector discharging to the inner components).

Figure 9-4 Adding Shield Casing When the Crystal is at the Board Edge



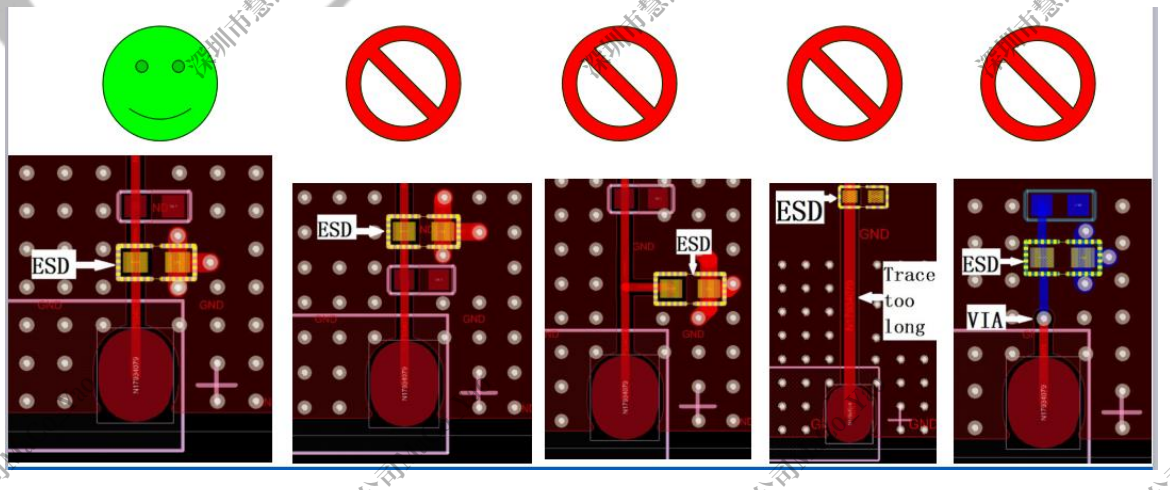
6. To avoid electromagnetic coupling from external signals, try to avoid the key signals like Reset, INT, and clock be adjacent and parallel with external interface signals like the USB, SD, and headphone. If it is inevitable, ensure the length of the parallel traces is not greater than 100 mils.

Figure 9-5 Avoid Parallel Traces among Adjacent Layers



7. Place a 1 nF bypass capacitor near the AP end of the reset signal.
8. To avoid antenna effect, point discharge, and EMI interference, avoid unnecessary stubs on the board.
9. All ESD components should be placed as close to the interfaces as possible.
10. Widen the traces near the ESD and do not change layers if possible.
11. Connect the pins of the ESD components to the main GND plane with short and wide (at least 20 mils) traces through the GND vias. The more GND vias, the better.

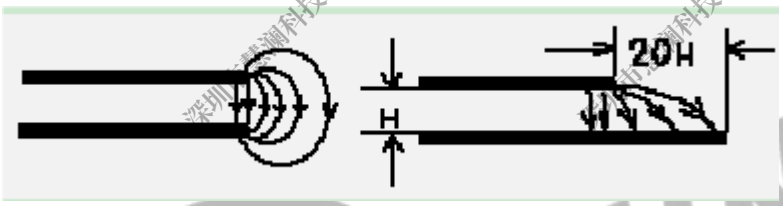
Figure 9-6 ESD Traces



9.2 EMC

1. To minimize radiation, shield the area of the DDR traces on the top. Keep the distance of the GND pins for DRAM, CPU, and shield casing less than 10 mm. For boards that have over four layers, do not route DDR traces at the bottom layer.
2. Reserve a complete reference plane for the LCD/CSI traces if possible. The resistance of the series resistors for the signal traces is 33 Ohms. For boards that have over four layers, you are suggested to route traces on the inner layers.
3. Try to route traces for SDIO CLK, SDC CLK, and CSI MCLK on the inner layers or shield them with ground traces. Drill GND vias with the via spacing not greater than 10 mm along the ground traces.
4. To avoid power radiation, apply the 20H rule. As the following figure shows, H is the height from the ground to power. Making the power plane 20H smaller than the adjacent ground plane can keep 70% of the electric field be absorbed into the ground plane. The value increases to 80% when the power plane is 100H smaller than the ground plane. If space is limited, keep the power plane 3H away from the edge.

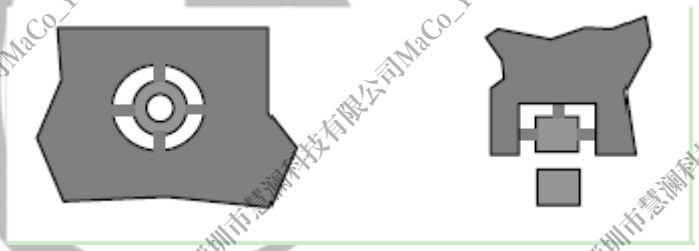
Figure 9-7 20H Rule



9.3 Heat

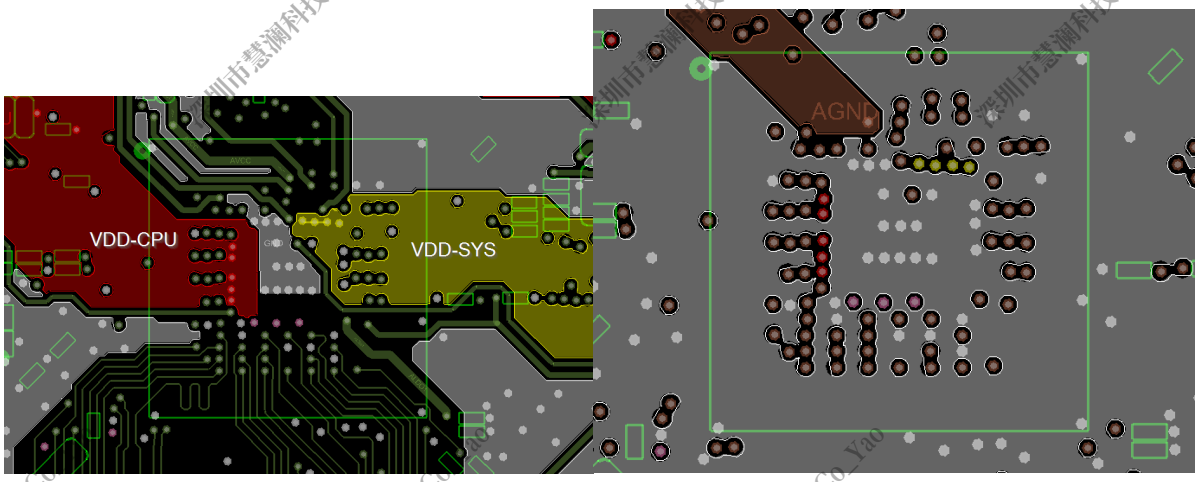
1. For components smaller than 0603, to avoid problems like void-welding caused by the over large heat capacity, use the thermal relief pad to connect the GND and shape.

Figure 9-8 Connecting Components Smaller Than 800603 to the GND with Thermal Relief Pad



2. Ensure the continuity and completeness of the GND plane and all power planes (at the power layer).

Figure 9-9 Complete GND and Power Planes



3. If space allows, add a large area of shape for the GND at the bottom layer for better heat dissipation.
4. Balls in the central region of the CPU are the main path to dissipate heat to other layers, ensure the via quantity for connecting the balls. The recommended via diameter ranges from 8 mils to 12 mils, and the recommended via spacing from center to center ranges from 30 mils to 40 mils. For areas around unused GPIO, also drill as many vias as possible.
5. Evenly place the components with large power, and avoid placing several heat sources together. Place the SoC in the center of the chip. Place PMU and BMU at least 2 cm away from the SoC.
6. Place the temperature-sensitive components at least 1 cm away from the heating components. For example, chips like Wi-Fi/BT and sensor should be placed 1 cm away from the PMU.
7. For components with EPAD, use pads that are slightly larger than the EPAD. Fully connect the vias of the EPAD with the GND. The GND plane should be larger than the EPAD and kept complete. You can expose the copper on the EPAD for better heat dissipation.

Figure 9-10 Layout for Heat Dissipation

Figure 9-11 Exposing Copper on Both Sides of the PMU Cooling Pad