

AC107/AC107S 2-Channel High Performance Voice Capture ADCs with I2C/I2S

1 Features

- 103 dB dynamic range(A-weight) @ 0 dB boost gain
- 85 dB THD+N @ 0 dB boost gain
- ADC sample rates supported: 8kHz~96kHz
- · Two fully differential microphone inputs
- One digital microphone SCLK output @1.024M~3.072M
- PLL support a wide clock input for 6/12MHz, 6.144MHz, 5.6448MHz,13MHz,16MHz,19.2MHz and 24MHz
- Programmable low noise Microphone Bias 1.8V~3.0V
- <20mW 2-ADC for low power consumption application

2 Applications

- Smart Voice Assistant Systems
- Voice Recorders
- · Digital Cameras and video cameras
- · Voice Conferencing System

3 Description

The AC107 is a highly integrated 2-channel ADC with I2S/TDM output transition. It's designed for multi-microphone array in high definition voice capture and recognition application platforms.

The integrated digital PLL supports a large range of input/output frequencies, and it can generate required system clocks from common reference clock such as 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, 13MHz, 19.2MHz, 24.576MHz and other non-standard audio

system clocks. The audio sample 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz is supported.

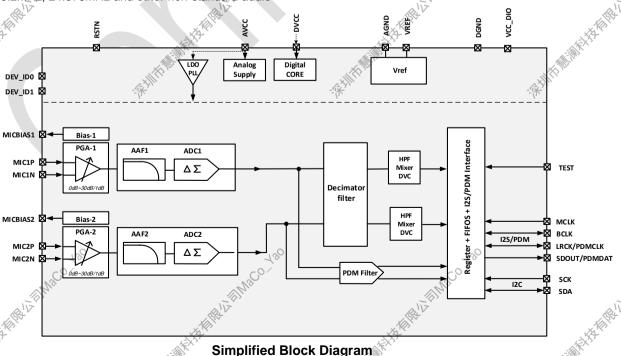
The AC107 integrates stereo synchronized ADCs with independent programmable mic bias voltage and mic boost amplifier to deliver valid channel data that channel crosstalk can be eliminated. The analog input port MIC1P/N ~MIC2P/N is designed as two differential microphone pin or single-ended line-in pin. Independent digital volume controllers are provided in each channel.

The AC107 can transit its 2 channels output data over the I2S port by standard I2S or PCM format. Also, one to eight device can be combined to transit up to 16 channels output data by a single TDM line. Furthermore, A new format called encoding mode can be used to transit 16 channels data when the I2S format of AP is normal protocol types.

The AC107 is controlled through TWI (2-wire serial interface, I2C compatible). The clock supports up to 400 KHz rate. It works only in the slave mode.

Device Information

Part Number	Package	Body Size		
AC107	QFN-20	3.0mm*3.0mm		
AC107S	QFN-24	4.0mm*4.0mm		





4 Revision History

Revision	Date	Description
V1.0	Dec.12, 2018	Initial internal release
¥1.1	Mar. 22, 2019	Add power consumption
V1.2	Apr. 26, 2019	Add marking information and carrier
V1.3	May. 8,2019	Change carrier from tray to tape reel
V1.4	May. 20,2019	Update PGA input resistance and PDM description

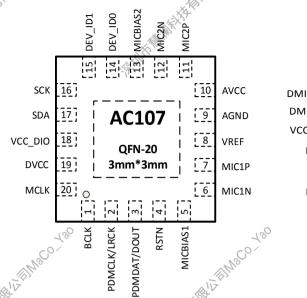
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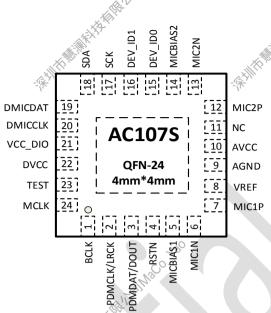
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5 Pin Configuration and Functions





PIN DESCRIPTION

Pin Number		ımber	r Name		
- (i)	AC107	AC107S	Name	I/O	Description Description
-11	1	1	BCLK	Ю	I2S interface serial bit clock
	2	2	LRCK/PDMCLK	Ю	I2S interface synchronous clock/PDM interface synchronous clock
	3 3 SDOUT/PDMDATA				I2S interface serial data output/PDM interface serial data output
	4 4 RSTN				Chip rest pin
	5 5 MICBIAS1				Bias voltage output for MIC1
	6	6	MIC1N	1	Negative differential input for MIC1
	7	7	MIC1P		Positive differential input for MIC1
	8	8 78	VREF	0	Internal reference voltage
	9	90	AGND	G	Analog Ground
	10	10	AVCC	PL	The analog part Power input
		11	NC		Not connected
	14	12	MIC2P	_	Positive differential input for MIC2
	12	13	MIC2N		Negative differential input for MIC2
······································	13	14	MICBIAS2	0	Bias voltage output for MIC2
/,	14	15	DEV_ID0		TWI interface device ID control
	15	16	DEV_ID1	I	TWI interface device ID control
	16	17	SCK	I	TWI interface serial clock input
	17	18	SDA	Ю	TWI interface serial data(Open-drain)
		19	DMICDAT/SDIN	Ю	Digital MIC stereo data input/I2S interface serial data input
		20	DMICCLK	Ю	Digital MIC CLK output
	18	21	VCC_DIO	Р	Digital power for digital I/O buffer
	19 22 🕸 DVCC		Р	The digital part Power input	
		23	TEST	1	Scan test for QAQC
	20	24	MCLK/SYNCCLK	IO	I2S interface master input clock/synchronous clock output
	EPAD GND				Digital Ground

Note: O for output, I for input, I/O for input/output, P for power, and G for ground



6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	\$\frac{1}{2}\limith	-流州市	MIN	MAX	UNIT
	DVCC	/,	-0.3	2.4	V
Supply voltage range	AVCC		-0.3	3.9	V
	VCC_DIO		-0.3	3.9	V
Output voltage range	MBIAS		-0.3	3.0	V
Digital Input voltage to groun	nd		-0.3	VCC_DIO+0.3	V
Analog input voltage to grou	nd		-0.3	AVCC+0.3	V
Operating Temperature, T _A			-40	85	$^{\circ}$
Junction temperature, T _J	180		- 18	125	$^{\circ}$
Storage temperature, T _{stg}	1,20		-65 🟑	150	$^{\circ}$

⁽¹⁾ Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

6.2 ESD Ratings

×	W. Committee	chill the children of the chil	VALUE	UNIT
K	V	Human body model(HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±4000	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
	V(ESD)	Charged device model(CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
DVCC	Input power for digital domain cell control	1.62	1.8	1.98	V
AVCC	Input power for analog part	3.0	3.3	3.63	V
VCC_DIO	Digital power for digital I/O buffer	1.62	3.3	3.63	N Way
Vi	Analog full-scale 0-dB input voltage	0.934	0.955	1.122	Vrms
V XA	VCC_DIO=3.3V	2.4	3.3	3.63	V
ViH	High Level Input Voltage VCC_DIO=1.8V	1.4	1.8	1.98	V
VAL.	Low Level Input Voltage	-0.3	0	0.7	V
Vон	High Level Output Voltage	£ 2.7	3.3	3.63	V
VoL	Low Level Output Voltage	-0.3	0	0.4	V
Соит	Digital output load capacitance			10	pF

6.4 Thermal Information

	THERMAL METRIC(1)	AC107	UNIT
θја	Junction-to-ambient thermal resistance	31.9	
θјс	Junction-to-case(top) thermal resistance	18.2	°C/W
θјв	Junction-to-board thermal resistance	ا 10.1	

⁽¹⁾ Thermal metrics are calculated refer to JEDEC document JESD51-2.

⁽²⁾ Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Analog Characteristics

At 25°C, AVCC=3.3V, DVCC=1.8V, VCC_DIO=3.3V, 24-bit audio data, 1kHz sine wave input

Parameter	Test Conditions	Min	Тур	Max	Unit
AUDIO ADC			111	XX	
Full scale input	PGA gain = 0dB, @THD<-40dB		0.5%		Vrms
DR(A-weighted)	DCA goin - 0dB @Fo_16KH7		103		dB
THD+N	PGA gain = 0dB, @Fs=16KHz		-85		dB
DR(A-weighted)	DCA goin 12dB @Fo 16KH=		102		dB
THD+N	PGA gain = 12dB, @Fs=16KHz		-84		dB
DR(A-weighted)	DCA gain 24dD @Fo 46KHz		94		dB
THD+N	PGA gain = 24dB, @Fs=16KHz		-82		dB
DR(A-weighted)	DCA coin 20dD @Fo 46KH-	0	89		dB
THD+N	PGA gain = 30dB, @Fs=16KHz	780	-81		dB
DR(A-weighted)	DCA rain AdD @Fo 40KH-	118	103		dB
THD+N	PGA gain = 0dB, @Fs=48KHz		-82		₩ dB
DR(A-weighted)	DCA gain 24dD @Fo 49KHz		92	XX	dB
THD+N	PGA gain = 24dB, @Fs=48KHz		-80	A SANTA	dB
P\$RR	217 Hz, 100 mVPP on AVCC, differential input		71		dB
Crosstalk (L/R)	10mV, 1KHz, 30dB Gain		-100 🖹	Ç.,	dB
MICBIAS					
Output Scale		1.8	3	AVCC	V
Bias Current			4		mA
Noise Level(A-weighted)		1.7	4		uV

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6.6 Electrical Characteristics

At 25 C, AVCC=3.3V, DVCC=1.8V, VCC_DIO=3.3V, MCLK=12.288MHz, I2S, 32bit

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
POWER CONSUMPION	\$\mathref{x}\)			籴	70	
Standby	Default register state after Power on	I _{1.8V}		0.46		uA
Standby	and Reset, MCLK/BCLK/LRCK off	I _{3.3V}		0.22		uA
1 ADC		I _{1.8V}		0.271		mA
1-ADC	DCA goin OdD @Fo 46KHz	I _{3.3V}		1.682		mΑ
0.400	PGA gain = 0dB, @Fs = 16KHz	I _{1.8V}		0.319		mΑ
2-ADC		I _{3.3V}		3.094		mA
4.400		I _{1.8V}		0.6		mA
1-ADC	4%°	I _{3.3V}	78	1.881		mA
2 ADC (M/8)	PGA gain = 0dB, @Fs = 48KHz	I _{1.8V}	113	0.745		mA
2-ADC	ARIV S	I3.3V		3.483		mÃ
4.400.4	X	l _{1.8} V		1.166	XXX	mΑ
1-ADC	DCA - OdD @Fo OCKU-	13.3V		2.169	**************************************	mA
***************************************	PGA gain = 0dB, @Fs = 96KHz	1 _{1.8} V		1.448		mA
2-ADC	\$\frac{1}{2}\text{III.}	I _{3.3V}		4.106		mA

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7 Detailed Descriptions

7.1 Overview

The AC107 is a highly integrated 2-channel ADC with I2S/TDM output transition. It's designed for multi-microphone array in high definition voice capture and recognition application platforms.

The integrated digital PLL supports a large range of input/output frequencies, and it can generate required system clocks from common reference clock such as 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, 13MHz, 19.2MHz, 24.576MHz and other non standard audio system clocks. The audio sample 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz is supported.

The AC107 integrates stereo synchronized ADCs with independent programmable mic bias voltage and mic boost amplifier to deliver valid channel data that channel crosstalk can be eliminated. The analog input port MIC1P/N ~MIC2P/N is designed as two differential microphone pin or single-ended line-in pin. Independent digital volume controllers are provided in each channel.

The AC107 can transit its 2 channels output data over the I2S port by standard I2S or PCM format. Also, one to eight device can be combined to transit up to 16 channels output data by a single TDM line. Furthermore, A new format called encoding mode can be used to transit 16 channels data when the I2S format of AP is normal protocol types.

The device includes several DSP features such as high-pass filter, mixer, and volume control.

AC107 is controlled through TWI (2-wire serial interface). The clock supports up to 400 KHz rate. It works only in the slave mode.

The device is available in a 20-pin 3mm*3mm QFN package or in a 24-pin 4mm*4mm QFN package.

7.2 Functional Block Diagram

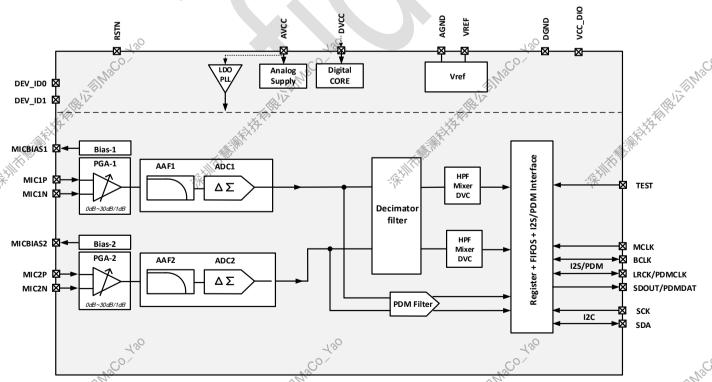


Figure 7-1. AC107 Block Diagram



7.3 Feature Description

7.3.1 Power

AC107 has a clear power management to make sure analog circuit work in a high performance status. All the supply voltages are illustrated in the below figure.

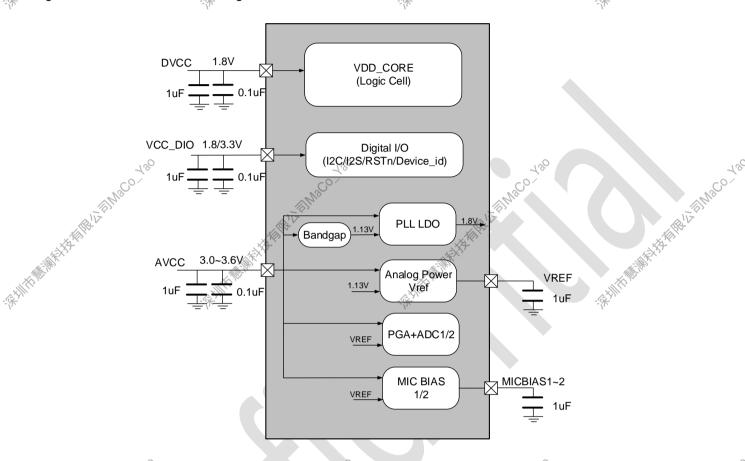


Figure 7-2. Power Management

DVCC is the digital power input for the logic cell control. AVCC is the analog power supply rail input to the analog circuit, which usually needs a clear LDO to make sure analog circuit work in a high performance status. VREF is designed to be a low noise voltage as analog power reference. VDD_DIO is digital I/O power for TWI, I2S ,Device_IDx and RSTN.

The power supplies are designed to operate from 3.0 V to 3.63 V for AVCC, from 1.62 V to 1.98 V for DVCC and from 1.62 V to 3.63 V for VCC_DIO. Any value out of these ranges must be avoided to ensure the correct behavior of the device. The power supplies must be well regulated. Placing a decoupling capacitor close to the AC107 improves the performance of the device. A low equivalent-series-resistance (ESR) ceramic capacitor with a value of 0.1 µF is a typical choice. If the AC107 is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the AVCC connections.

When the AC107 is not working, it need to set the supply properly to prevent power leakage. It's best to power off all the supply.

7.3.2 Reset

There are a Power-Reset circuit in AC107 used to reset all the circuit and register to a standby state after power up. The Power-Reset circuit make all the supply power need no specific timing.

The power reset and soft reset diagram is below:



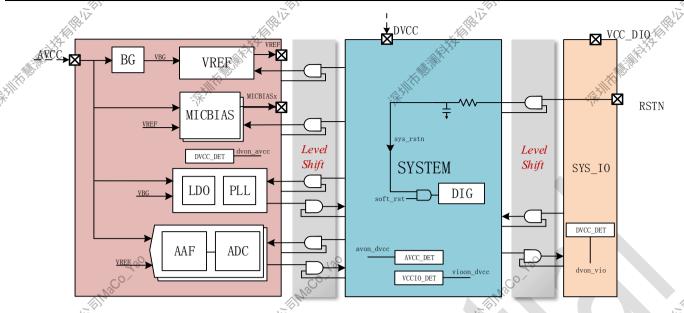


Figure 7-3. Reset Management

7.3.3 Clock

Revision 1.4

The system clock (SYSCLK) of AC107 must be 256*fs(fs=48KHz of 44.1KHz). So the system should arrange the divider to generate 12.288MHz for audio clock series of 48KHz or 11.2896MHz for series of 44.1KHz.

SYSCLK, which always provided by externally clock or internal PLL, can be selected from MCLK/I2S_BCLK or PLL, while the PLL reference clock can be selected from MCLK, I2S_BCLK or PDMCLK. SYSCLK is the clock reference of ADC, DVC, MIXER, HPF and I2S module except TWI. If MCLK&BCLK are both not 12.288MHz for ADC 48KHz series sample rate or 11.2896MHz for ADC 44.1KHz series sample rate, SYSCLK must be selected from PLL. SYSCLK always need to be configured in these cases.

SCK pin is always an external clock input pin and the clock is used as the reference of the TWI clocking zone.

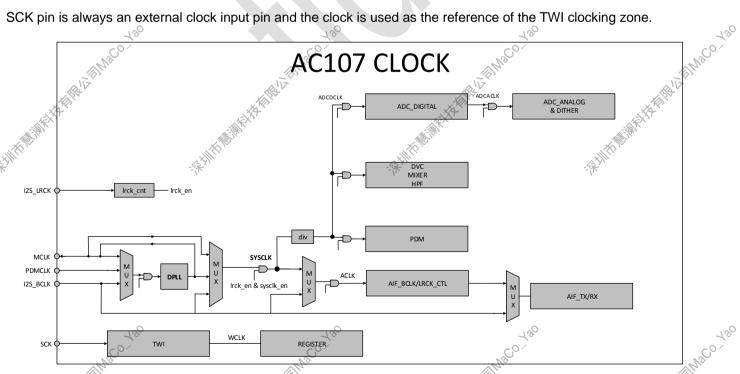


Figure 7-4. Clock Management Unit

The clock management related registers are Reg[0x20]~Reg[0x22].



731 DII

A Phase-Locked Loop (PLL) is designed to cover a flexible input clock range from 400KHz to 24MHz. The clock sources of the PLL can be set to MCLK, BCLK or PDMCLK by setting register *Reg[0x20]*. The PLL output is always used to provide the system clock (SYSCLK) for AC107 when 12.288MHz or 11.2896MHz cannot be provided from MCLK and BCLK. The PLL transmit formula as below:

FOUT =(FIN * N) / ((M1+1) * (M2+1)*(K1+1)*(K2+1));

Table 7-1. clock setting for SYSCLK=12.288MHz

FIN	M1	M2	Fref	N	Fvco	K1	K2	FOUT
400K	0	0	400K	983	393.2M	15	1	12287500
512K	0	0	512K	960	491.52M	19	1	12288000
768K	0 180	0	768K	√8° 640	491.52M	19,1%	1	12288000
800K	O /	0	800K	768	614.4M	24	1	12288000
1.024M	Who 0	0	1.024M	480	491.52M	19 19	1	12288000
1.6M	[V 0	0	1.6M	384	614.4M	24	1	12288000
2.048M	0	0	2.048M	240	491.52M	19	1	12288000
3.072M	0	0@	3.072M	160	491.52M	19	1	12288000
4.096M	0	0	4.096M	120	491.52M	19	1	12288000
6M	4	6 Fill 1	1.2M	512	614.4M	24	1	12288000
6.144M	1	Ó	3.072M	160	491.52M	19	1	12288000
12M	9	0	1.2M	512	614.4M	24	1	12288000
13M	12	0	1M	639	639M	25	1	12288462
15.36M	9	0	1.536M	320	491.52M	19	1	12288000
16M	9	0	1.6M	384	614.4M	24	1	12288000
19.2M	11	0	1.6M	384	614.4M	24	1	12288000
19.68M	15	1	615K	999	614.385M	24	1	12287700
24M	9	0	2.4M	256	614.4M	24	1	12288000

Table 7-2. clock setting for SYSCLK=11.2896 MHz

FIN	M1	M2	Fref	N	Fvco	KI KI	К2	FOUT
400K	0	0	400K	1016	406.4M	17	1	11288889
512K	0	0	512K	882	451.584M	19	1	11289600
7 68K	0	0	768K	588	451,584M	19	1	11289600
800K	0	0.1177	800K	508	406.4M	17	1,11	11288889
1.024M	0	0	1.024M	441	¹ 451.584M	19	1	11289600
1.6M	0	0	1.6M	254	406.4M	17	1	11288889
2.048M	1	0	1.024M	441	451.584M	19	1	11289600
3.072M	0	0	3.072M	147	451.584M	19	1	11289600
4.096M	3	0	1.024M	441	451.584M	19	1	11289600
6M	1	0	3M	143	429M	18	1	11289474
6.144M	1	0	3.072M	147	451.584M	19	1	11289600
12M	3	0	3M	143	429M	18	1	11289474
13M	12	0	1M	429	429M	18	1	11289474
15.36M	14	0	1.024M	441	451.584M	19	1	11289600
16M	24	0	640K	882	564.48M	24	1	11289600
19.2M	4	0	3.84M	147	564.48M	24	1	11289600
19.68M	13	1	703K	771	541.90M	23	1	11289643
24M	24	0	960K	588	564.48M	24	1	11289600

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7.3.5 TWI Interface

TWI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is used for data. SCK clock supports up to 400KHz rate and SDA data is an open drain structure.

Amaster controller initiates the transmission by sending a "start" signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave 7-bit address followed by a R/W bit. The 7-bit chip address changed by external two Pins DEV_ID0 and DEV_ID1. The chip address is defined by Table 7-3 below. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at SDA while SCK is high.

Table 7-3. The Chip Slave address

7-bit Address	DEV_ID1	DEV_ID0
0x36(011 0110)	0	0 180
0x37(011 0111)	0	1,00
0x38(011 1000)	1	0
0x39(011 1001)	1	1

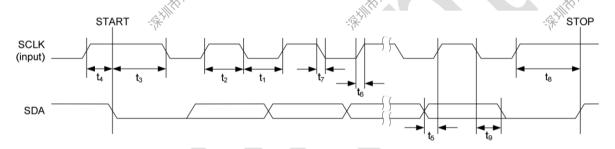


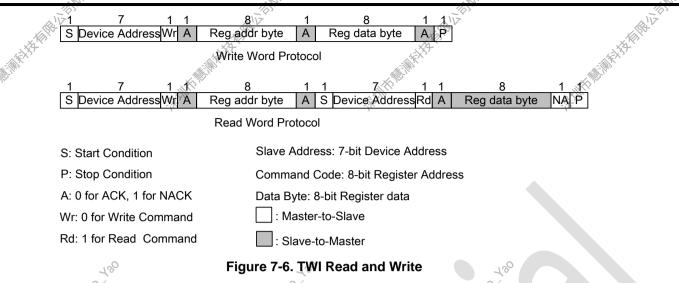
Figure 7-5. TWI Interface

Table 7-4. TWI Timing Requirement

Parameter	Symbol	Min	Typ	Max	Units
SCK Frequency			A STATE OF THE STA	400	KHz
SCLK Low Pulse-Width	t ₁	1300	X		ns
SCLK High Pulse-Width	t ₂	600			ns
Hold Time(Start Condition)	t ₃	600		-	ns
Setup Time(Start Condition)	t ₄	600			ns
Data Setup Time	t 5	100			ns
SDA,SCLK Rise Time	t ₆			300	ns
SDA,SCLK Fall Time	t ₇			300	ns
Setup Time(Stop Condition)	t ₈	600			ns
Data Hold Time	t ₉			900	ns
Pulse Width of Spikes suppressed	t _{ps}			30	ns

The formats of "write" and "read" instructions are shown in below.





7.3.6 I2S/PCM Interface

There are only one I2S/PCM output engine which can be configured as master mode or slave mode in AC107. The I2S/PCM interfaces provide flexible transit protocol to support varied formats processors.

The serial data is normally driven on negative edge of BCLK. MSB bit of data is normally transmitted first. In the general case, the digital audio interface uses three pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC1~ADC2 data

I2S audio interface support three different data protocol types below.

- 12S/PCM normal mode
- I2S/PCM TDM mode
- I2S/PCM Encoding mode

I2S/PCM normal mode support four different data format types below. Normal mode is used to transmit 2 channel data on left and right channel simultaneously. data on left and right channel simultaneously.

- 12S justified mode
- Left justified mode
- Right justified mode
- PCM short/long frame mode

I2S/PCM TDM mode support four different data format types below. TDM mode is used to transmit up to 16 channel data on timeslot0~timeslot15 when eight AC107 work simultaneously.

- I2S justified TDM mode
- Left justified TDM mode
- Right justified TDM mode
- PCM short/long frame TDM mode

I2S/PCM Encoding mode support four different data format types below. Encoding mode is used to transmit up to 16 channel data using normal I2S format by setting the I2S rate to multi-times of ADC. For example, when the sample rate of ADCs is 16KHz, I2S/PCM Encoding mode can transit 8 channel data by setting I2S LRCK to 16KHz*(8/2) And the last 4 bits of the sample data indicate the channel number.

- 12S justified Encoding mode
- Left justified Encoding mode



- Right justified Encoding mode
- PCM short/long frame Encoding mode

The timing of I2S in Master mode shows below:

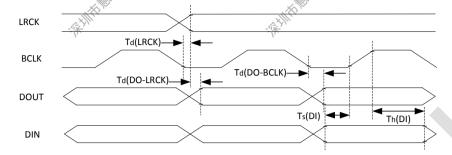


Figure 7-7. I2S Master Mode Timing

Table 7-5, 12S Timing in Master Mode

PARAMETER		MIN	MAX	UNITS
Td(LRCK)	LRCK delay		10	ns
Td(DO-LRCK)	LRCK to DOUT delay(For LJF)		10	ns
Td(DO-BCLK)	BCLK to DOUT delay		<u></u>	ns
Ts(DI)	DIN setup	4	110	ns
Th(DI)	DIN hold	4		ns
Tr	BCLK Rise time		8	ns
Tf	BCLK Fall time		8	ns

The timing of I2S in slave mode shows below:

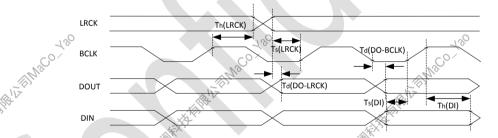


Figure 7-8. I2S Slave Mode Timing Table 7-6. I2S Timing in Slave Mode

	,			
PARAMETER	·	MIN	MAX	UNITS
Ts(LRCK)	LRCK setup	4		ns
Th(LRCK)	LRCK hold	4		ns
Td(DO-LRCK)	LRCK to DOUT delay(For LJF)		10	ns
Td(DO-BCLK)	BCLK to DOUT delay		10	ns
Ts(DI)	DIN setup	4		ns
Th(DI)	DIN hold	4		ns
Tr 480	BCLK Rise time	180	4	ns
Tf	BCLK Fall time	18C0	4	ns No

The I2S/PCM management related registers are Reg[0x30]~Reg[0x3D].



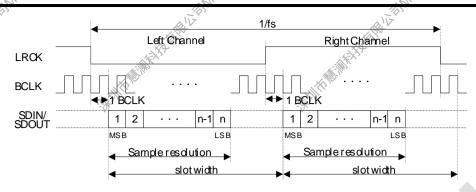


Figure 7-9. I2S Justified mode

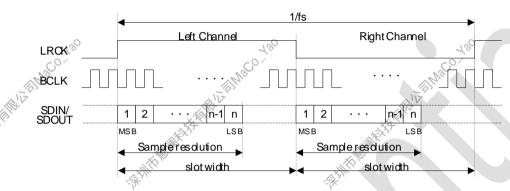


Figure 7-10. Left Justified mode

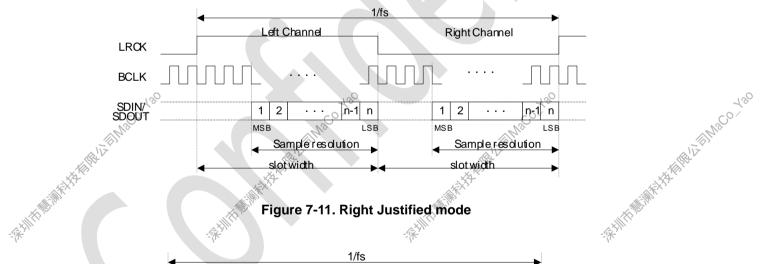


Figure 7-11. Right Justified mode

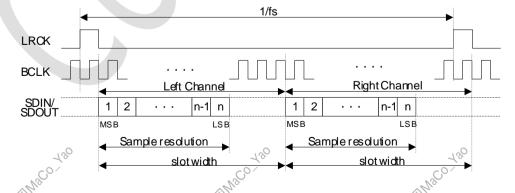


Figure 7-12. PCM mode A(Offset=1)

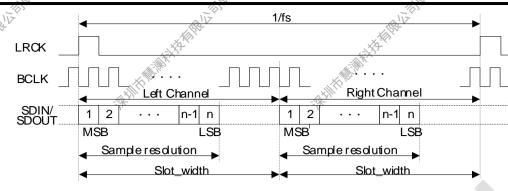


Figure 7-13. PCM mode B(Offset=0)

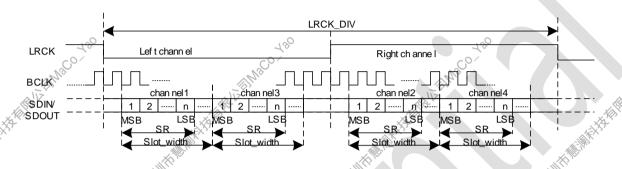


Figure 7-14. I2S TDM mode

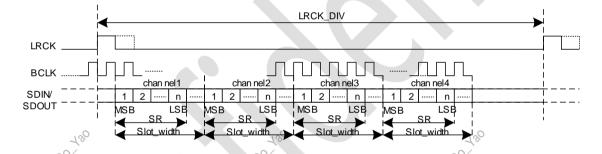


Figure 7-15. PCM TDM mode

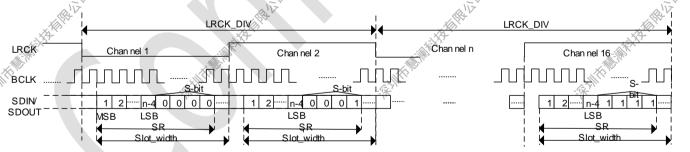


Figure 7-16. I2S Encoding mode

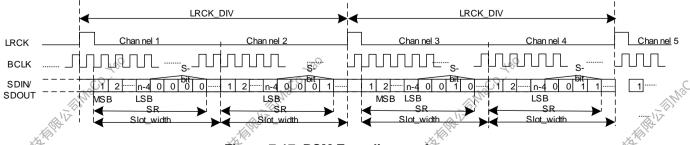
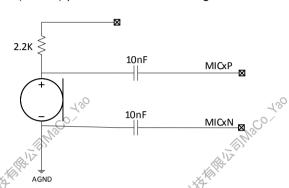


Figure 7-17. PCM Encoding mode



7.3.7 Analog Microphone Input

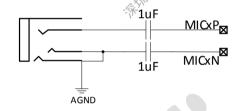
MIC1P/N, MIC2P/N provide differential input to the ADC1, ADC2 record path. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. There are two independent AAF (Anti-Alias Filter) and PGA(Pre-Gain Amplifier) for the two differential microphone inputs. The gain for each pre-amplifier can be set independently using MIC1BOOST, MIC2BOOST. Two MICBIASx (x=1~2) provide reference voltage for electret condenser type (ECM) microphones.



1.1K ≥ 10nF MICxP ≥ 1.1K ≥ 10nF MICxN ≥ 1.1K ≥ 10nF

Figure 7-18. Suggested Single-Ended Mic Input

Figure 7-19. Suggested Differential Mic Input



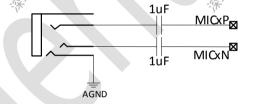


Figure 7-20. Suggested Single-Ended Line-in

Figure 7-21. Suggested Differential Line-in

7.3.8 Analog ADC Data Path

The analog ADC data path includes separate programmable Pre-gain amplifier (PGA), anti-aliasing low-pass filter (AAF) and delta-sigma modulator (DSM). The PGA is designed to amplify input signals to the maximum full-scale signal. The AAF is designed to minimize the noise folded down to the audio band by the oversampling ADC, AAF ensure at least 60 dB attenuation at the modulator switching frequency. The DSM oversampling frequency runs at 128fs. The analog ADC data path related registers are $Reg[0xA0] \sim Reg[0xA9]$.

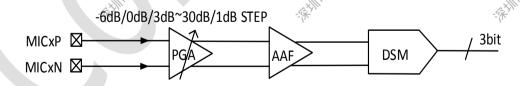


Table 7-7. PGA Gain Setting

	PGA Gain Setting								
pga_gain [4:0]	Gain Setting	Output-Referred	Max Input Level	Output Level	Input Resistance				
(decimal)	(dB)	Gain (dB)	(Vrms diff)	(Vrms diff)	(kΩ)				
0	-6	0 0	2.000	2 (۲	16				
1	0	16 No	1.000	国际 2	8 III				
2	0	6	1.000	2	8				
3	0	6	1.000	2	8				



, O.		,01,		101,	101
4	3	9	0.710	2	100/75/50/25
5	4	10	0.632	2	100/75/50/25
	···	\$\hat{x}^{2}\dagger'		2	100/75/50/25
N-5	N-6	N	2/[10^(N/20)]	2	100/75/50/25
	· · · · · · · · · · · · · · · · · ·		-\$XXXX	2	100/75/50/25
31	30	36	0.032	2	100/75/50/25

NOTE: The PGA output referred gain = gain setting + 6 dB due to the single-ended to differential conversion.

7.3.9 Digital Data Path

The digital data path is provided with digital audio data source select, DSM decimation filter, HPF, volume controller and data mixing to two I2S output paths. Then the digital output of the DSM is decimated down to the required sample rate and then DC cancellation, digital amplification are implemented. Finally a digital selector and mixer is available to map any analog input into any channel or combine multiple channels into any single channel. It's separately controlled by the register $Reg[0x61] \sim Reg[0x7F]$.

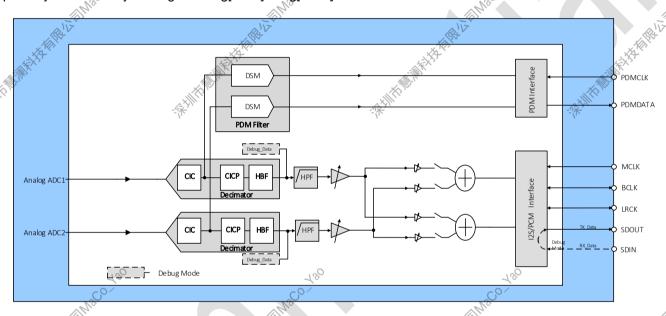


Figure 7-22. Digital Data Path

7.3.10 PDM Input and PDM Output Interface

One PDM (Pulse Density Modulation) input interface is used for dual DMICs application (Only supported on AC107S). DMICCLK is generated by AC107 and DMICDAT data comes from external DMICS. The circuit share decimation filter with audio ADC. DMICCLK can be output 64fs when the DMIC over sample rate is 32kHz~48kHz and 128fs when the DMIC over sample rate is 8kHz~24kHz (fs= ADC sample rate).

Table	7-8. Digital	Microphone	Clock
-------	--------------	------------	-------

Fs(kHz)	8	12	11.025	16	22.05	24	32	44.1	48
n	128	128	128	128	128	128	64	64	64
Freq(kHz)	1024	1536	1411.2	2048	2822.4	3072	2048	2822.4	3072

Digital Microphone power usually falls between the range 1.6V-3.6V, typical 1.8V. And the Clock frequency is between the the range 1.024MHz-3.072MHz.



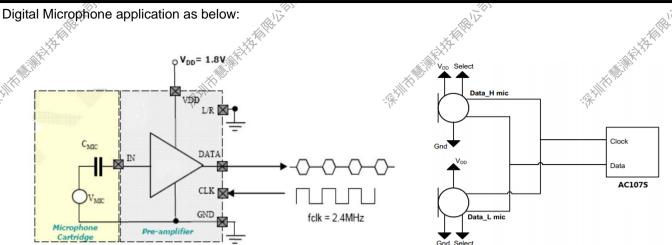


Figure 7-23. Digital Microphone Application

Digital Microphone timing as shown in Table 7-9 and Figure 7-24 below.

One PDM output interface is used to transit the ADC channel data instead of using I2S interface. Therefore, the combination of AC107 plus AMIC can be used as 2 digital MIC. It is particularly emphasized that the timing of the DMIC PDMIN and the timing of the AC107 PDMOUT interface are somewhat different. For DMIC, because different mics drive data lines in turn, the key thing here is that the H-Z state needs to occur before valid data to ensure no bus contention occurs. Also note there is a small window (t_z) to sample data. It is essential that every valid data bit is sampled to avoid errors. As shown in figure 7-24, for DMIC PDMIN, the DAT1 data outputs during the clock low period and then turns high impedance during the high period, the DAT2 data operates in a similar way, but outputs valid data on the high clock phase. The delay time $t_{\rm DD} > t_{\rm Dz}$ in order to have interim H-Z state in both signals. For AC107 PDMOUT, the DAT1 and DAT2 is generated by ADC filter and no interim H-Z state required. The duty of data valid is half the $f_{\rm CLOCK}$ Frequency cycle.

PDM output timing as shown in Table 7-9 and Figure 7-24 below.

Table 7-9. PDM Input and Output Timing requirement

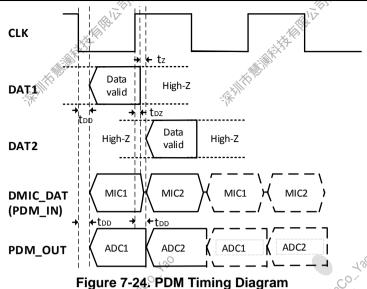
0		milparalia Carpar Illimig IC	40	. ^0		
Parameter	Symbol	Conditions	Min	Тур	Max	Units
Clock Frequency Range	f _{CLOCK}	Mo	1.024	1	3.072	MHz
Digital power for digital I/O buffer	V _{IO}		1.64	1.8	2.86	WIN
Logic Input High	VIHX		0.65V _{IO}	-	V _{IO} +0.3	√
Logic Input Low	VIL		-0.3	1	0.35V ₁₀	V
Clock Duty Cycle	Hill	f _{CLOCK} ≤2.475 MHz	40	1	60	%
Clock Duty Cycle		2.475 MHz \leq f _{CLOCK} \leq 3.072 MHz	48	50	52	%
Delay Time for Data Assertion	t _{DD}		18	28	-	ns
Delay Time for High Z	t _{DZ}		3	-	16	ns

Table 7-10. PDM input clock

Fs(kHz)	8	12	11.025	16	22.05	24	32	44.1	48
PDMCLK(kHz)	1024	1536	1411.2	2048	2822.4	3072	2048	2822.4	3072

Thinks 180





rigure 7-24. PDM Timing Diagram

7.4 Basic Setup Sequences

AC107 configuration: I2S Slave, I2S Justified mode, MCLK=12.288MHz, BCLK=1.024MHz, LRCK=16KHz, 2 channel, 32bit Slot width, 24bit Sample resolution.

2-ADC 16KHz Record setup sequence:

Reg[0x00] = 0x12; //reset to default status

Reg[0x01] = 0x80; //verf enable, verf fast startup enable

Reg[0x02] = 0x55; //MICBIAS enable

Reg[0x21] = 0x07; //Module clock enable<I2S, ADC digital, ADC analog>

Reg[0x22] = 0x03; //Module reset de-asserted<l2S, ADC digital>

Reg[0xA4] = 0x40;//enable ADC1 analog part

Reg[0xA9] = 0x40;//enable ADC2 analog part

Reg[0x20] = 0x01;//system clock enable

Reg[0x30] = 0x15; //I2S TX enable & I2S slave

Reg[0x33] = 0x1F; //set LRCK_PERIODL=32*BCLK width

Reg[0x34] = 0x15; //set I2S format; I2S Justified mode

Reg[0x35] = 0x75;//set Slot width=32-bit, Sample resolution=24-bit

Reg[0x38] = 0x01; //set I2S TX Channel (slot) number: 2

Reg[0x39] = 0x03; //I2S TX Channel 1 ~ Channel 2 (slot) enable

Reg[0x3C] = 0x02; //I2S TX mapping

Reg[0x60] = 0x03; //set ADC Sample Rate: 16KHz

Reg[0x61] = 0x07; //enable ADC digital part

Reg[0x66] = 0x03; //enable HPF

Reg[0xA2] = 0x19;//ADC1 Analog PGA Gain: 24dB

Reg[0xA7] = 0x19;//ADC2 Analog PGA Gain: 24dB

Reg[0x01] = 0xA0; //verf enable, verf fast startup disable

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7.5 Register Maps

7.5 Register Iviaps		
Register Name	Offset	Description
CHIP_AUDIO_RST	0x00	Soft Reset Register
PWR_CTRL1	0x01	Power Control 1 Register
PWR_CTRL2	0x02	Power Control 2 Register
PLL_CTRL1	0x10	PLL Configure Control 1 Register
PLL_CTRL2	0x11	PLL Configure Control 2 Register
PLL_CTRL3	0x12	PLL Configure Control 3 Register
PLL_CTRL4	0x13	PLL Configure Control 4 Register
PLL_CTRL5	0x14	PLL Configure Control 5 Register
PLL_CTRL6	0x16	PLL Configure Control 6 Register
PLL_CTRL7	0x17	PLL Configure Control 7 Register
PLL_LOCK_CTRL	0x18	PLL Configure Control 8 Register
SYSCLK_CTRL	0x20	System Clock Control Register
MOD_CLK_EN	0x21	Module Clock Enable Control Register
MOD_RST_CTRL	0x22	Module Reset Control Register
I2S_CTRL	0x30	I2S Control Register
I2S_BCLK_CTRL	0x31	I2S BCLK Configure Register
12S_LRCK_CTRL1	0x32	I2S LRCK Configure 1 Register
I2S_LRCK_CTRL2	0x33	I2S LRCK Configure 2 Register
I2S_FMT_CTRL1	0x34	I2S Format Configure 1 Register
I2S_FMT_CTRL2	0x35	I2S Format Configure 2 Register
I2S_FMT_CTRL3	0x36	I2S Format Configure 3 Register
I2S_TX_CTRL1	0x38	I2S TX Control 1 Register
I2S_TX_CTRL2	0x39	I2S TX Control 2 Register
I2S_TX_CTRL3	0x3A	I2S TX Control 3 Register
I2S_TX_CHMP_CTRL1	0x3C	I2S TX Channel Mapping Control 1 Register
I2S_TX_CHMP_CTRL2	0x3D	I2S TX Channel Mapping Control 2 Register
I2S_RX_CTRL1	0x50	I2S RX Control 1 Register
I2S_RX_CTRL2	0x51	I2S RX Control 2 Register
I2S_RX_CTRL3	0x52	I2S RX Control 3 Register
I2S_RX_CHMP_CTRL1	0x54	I2S RX Channel Mapping Control 1 Register
I2S_RX_CHMP_CTRL2	0x55	I2S RX Channel Mapping Control 2 Register
PDM_CTRL	0x59	PDM Control Register
ADC_SPRC	0x60	ADC Sample Rate Select Register
ADC_DIG_EN	0x61	ADC Digital Part Enable Register
HPF_EN	0x66	Digital HPF Enable Register
ADC1_DVOL_CTRL	0x70	ADC1 Digital Channel Volume Control Register
ADC2_DVOL_CTRL	0x71	ADC2 Digital Channel Volume Control Register
ADC1_DMIX_SRC	0x76	ADC1 Digital Mixer Source Control Register
ADC2_DMIX_SRC	0x77	ADC2 Digital Mixer Source Control Register
ADC_DIG_DEBUG	0x7F	ADC Digital Debug Control Register
A. C.		



40.	, N.	10.
ADC_ANA_DEBUG2	0x81	ADC Analog Debug Control 2 Register
I2S_PADDRV_CTRL	0x82	I2S Pad Drive Control Register
DIG_ADC_CTRL	0x83	ADC Digital Control Register
ANA_ADC1_CTRL1	0xA0	ADC1 Analog Control 1 Register
ANA_ADC1_CTRL2	0xA1	ADC1 Analog Control 2 Register
ANA_ADC1_CTRL3	0xA2	ADC1 Analog Control 3 Register
ANA_ADC1_CTRL4	0xA3	ADC1 Analog Control 4 Register
ANA_ADC1_CTRL5	0xA4	ADC1 Analog Control 5 Register
ANA_ADC2_CTRL1	0xA5	ADC2 Analog Control 1 Register
ANA_ADC2_CTRL2	0xA6	ADC2 Analog Control 2 Register
ANA_ADC2_CTRL3	0xA7	ADC2 Analog Control 3 Register
ANA_ADC2_CTRL4	0xA8	ADC2 Analog Control 4 Register
ANA_ADC2_CTRL5	0xA9	ADC2 Analog Control 5 Register
ADC_DITHER_CTRL	0xAA	ADC Dither Control Register

Reg 00h_Chip Soft Reset Register

Default: 0x4B		1.	Register Name: CHIP_AUDIO_RST
Bit	Read/Write	Default	Description
7.0	R/W	0v4D	Reading this register will indicate device type and version.
7:0	R/VV	0x4B	Writing this register 0x12 resets all register to their default state.

Reg 01h_Power Control 1 Register

Default:	0x00		Register Name: PWR_CTRL1	
Bit	Read/Write	Default	Description	2
	What a		VREF_ENABLE VREF_Enable	Ma
7	R/W	0	VREF ENABLE VREF Enable 0 Disable	Q'
, .×3	10,00	U	0 ⊆ Disable	
A STATE OF THE PARTY OF THE PAR			1 = Enable	
-111/H-1-1-1			VREF_LPMODE	
6	R/W	0 %	VREF Low Power Mode Control	
	10,00		0: Normal	
			1: Low Power	
			VREF_FSU_DISABLE	
5	R/W	0	VREF Fast Start Up Disable	
	10,00		0: Enable	
			1: Disable	
			VREF_RESCTRL	
	780		VREF Output Resistor Control	
4:3	DVVV/SCO	0	00: 1M Qhm	"NSC
4.5	R/M/NO		VREF Output Resistor Control 00: 1M Ohm 01: 2-2k Ohm 10: 10M Ohm	
×	No.		10: 10M Ohm	
The Name of the Na			11: 100k Ohm	



		M		M		10/1-
		WIN.		IGEN_TRIM	WIV.	WIN.
	XXX	Mary		Tune bias current gen	erator for all audio input channels	XATORIV
				000=Nominal (5uA)		
	III A BELL		III/KI III	001=-4.8%		A THE REAL PROPERTY OF THE PARTY OF THE PART
1	2:0	R/W	0 深圳村市	010=-9.1%	The state of the s	-宋二
	2.0	10,00	O	011=-13%		
				100=+25%		
				101=+17.6%		
				110=+11%		
				111=+5.2%		

Reg 02h_Power Control 2 Register

Default: 0)x11		Register Name: PWR_CTRL2
Bit	Read/Write	Default	Description (III)
7	R/W	0	VREF_SEL VREF Source Selection 0: From BandGap 1: From AVCC
6	R/W	0	MICBIAS2_EN MICBIAS2 Enable 0: Disable 1: Enable
5:4	R/W	1	MICBIAS2_VCTRL MICBIAS2 Voltage Control 00: 1.8V 01: 2.1V 10: 2.4V 11: 3V
3	1	1	
2 ANTON THE PROPERTY OF THE PARTY OF THE PAR	R/W	O CHINE	MICBIAS1_EN MICBIAS1 Enable 0: Disable 1: Enable
1:0	R/W	1	MICBIAS1_VCTRL MICBIAS1 Voltage Control 00: 1.8V 01: 2.1V 10: 2.4V 11: 3V

Reg 10h_PLL Configure Control 1 Register

Default: 0x48		Register Name: PLL_CTRL1	20120	O NO.	
Bit	Read/Write	Default	Description	AIV.	\$1V
7		/	15th	XX TON	XX AND THE REAL PROPERTY OF THE PERTY OF THE



		Mo		
		WIN.		PLL IBIAS PLL internal bias current tuning
	XXX	No.		PLL internal bias current tuning
	6:4	R/W	0x4	0: min
	WHI THE STATE OF T			
-4	<u> </u>		-(*X)	7: max ***********************************
				PLL_NDET
	3	R/W	0x1	PLL loop divider factor detection
	3	17,77	0.00	0: Disable
				1: Enable
				PLL Locked status
	2	R	0x0	0: Not locked or not enabled
				1: Enabled and locked
		180		PLL_COM_EN
	1	RWW.Co	0x0	PLL Common voltage Enable
	'	R/W/N	OXO	0: Disable
				1: Enable
	CXX A			PLL_EN
	A STATE OF THE STA		A A A A A A A A A A A A A A A A A A A	PLL Enable
-4	0	R/W	0x0	0: Disable
1			/,	1: Enable
				The PLL output FOUT= $FIN*N/((M1+1)*(M2+1)*(K1+1)*(K2+1));$

Reg 11h_PLL Configure Control 2 Register

Default:	0x00		Register Name: PLL_CTRL2	
Bit	Read/Write	Default	Description	
7:6	/	/	1	
	180		PLL_PREDIV2	
_	DAME	0,40	PLL pre-divider factor M2	. NSC
5	R/W	0x0	PLL pre-divider factor M2 Factor=0, M2=0	Relation Management
,	C TO SECOND		Factor=1, M2=1	
TAX TAX	57		PLL_PREDIV1	A PARTY AND A PART
A THE STATE OF THE			PLL pre-divider factor M1	A THE STATE OF THE
4:0	R/W	0x0	Factor=0, M1=0	**************************************
4.0	R/VV	UXU	Factor=1, M1=1	
			Factor=31, M1=31	

Reg 12h_PLL Configure Control 3 Register

Default	t: 0x03		Register Name: PLL_CTRL3	
Bit	Read/Write	Default	Description	
7:2	1 400	/	1 100	, (
	Mac		PLL_LOOPDIV_MSB	Mo
1.0	RW	0.42	The 2-High Bit of PLL Loop Divider Factor N.	WIN.
1:0	74/VV	0x3	Factor=0, N=0	XA KINST
	×5′		Factor=1, N=1	in the state of th



40/	* W/-	10/1	a William
_''(\(\rangle\)	7.40,	_''\(\rangle\)	7/4>
W.\/	DIV	1V	W//>
Sept.	F-1-1 4000 N 4000		NO.
X1.	Factor=1023, N=1023	XX.	XX
CEXST .	A Tantau N in a sural to IDI I	L LOOPDIV MOD DIL LOODD	N/ LODE
	Factor IN IS equal to [PLI	$L_LOOPDIV_MSB$, PLL_LOOPD	IV_LSB/K

Reg 13h_PLL Configure Control 4 Register

Default: 0x0D			Register Name: PLL_CTRL4
Bit	Read/Write	Default	Description
			PLL_LOOPDIV_LSB
			The 8-Low Bit of PLL PLL Loop Divider Factor N.
			Factor=0, N=0
7:0	R/W	0x0D	Factor=1, N=1
	00		
	7.0		Factor=1023, N=1023
	Ma		Factor N is equal to [PLL_LOOPDIV_MSB, PLL_LOOPDIV_LSB]

Reg 14h_PLL Configure Control 5 Register

Default: 0x00			Register Name: PLL_CTRL5
Bit	Read/Write	Default	Description
7:6	/	1 -1/1	1
			PLL_POSTDIV2
5	R/W	0,40	PLL post-divider factor K2
5	K/VV	0x0	Factor=0, K2=0
			Factor=1, K2=1
			PLL_POSTDIV1
			PLL post-divider factor K1
4:0	DAM 180	0x0	Factor=0, K1=0
4.0	R/W	UXU	Factor=1, K1=1
	R/W		Factor=1, K1=1
	WIV.		Factor=31, K1=31

Reg 16h_PLL Configure Control 6 Register

Default	:: 0x0F	- 12 Hilli	Register Name: PLL_CTRL6
Bit	Read/Write	Default	Description
			PLL_LDO
			PLL internal Ido voltage tuning
7.6	DAM	0.40	00: 1.8V
7:6	R/W	0x0	01: 2.0V
			10: 2.2V
			11: 2.4V
5	1 480	/	1 780
	,20/		PLL_CP CO
4:0	R/W	0xF	PLL plice current tuning
4.0	KAVV	UXF	PLL_CP CO PLL pll cp current tuning 0: min
; ;	X		



31: max

Reg 17h_PLL Configure Control 7 Register

Default: 0xD0			Register Name: PLL_CTRL7	
Bit	Read/Write	Default	Description	
			PLL_CAP	
			PLL loop filter capacitance tuning	
7:6	R/W	0x3	0: min	
			3: max	
			PLL_RES	
	780		PLL loop filter resistance tuning	
5:4	R/W	0x1	0: min	c S
	R/W		Kho	110
	ALV.		3: max	
3:0	X 1	/	Marin	

Reg 18h_PLL Configure Control 8 Register

Default:	: 0x00	2/1	Register Name: PLL_LOCK_CTRL
Bit	Read/Write	Default	Description
7	/	/	1
			HOLD_TIME
			SYSCLK hold time T
6:4	R/W	0x0	T=0, Bypass
0.4	I K/VV	UXU	T=1, 1 LRCK width
	180		7%
	780		T=7, 7 LRCK width
			LOCK_LEVEL1 PLUIOCK level1 00: 21-29 clock cycles
	SELV.		PLL lock level1
3:2	R/W	0x0	00: 21-29 clock cycles
			01: 22-28 clock cycles
FIIILE SE		till fit is	1x: 20-30 clock cycles
←		-1X-	LOCK_LEVEL2
1	R/W	0x0	PLL lock level2
'	1000	OXO	0: 24-26 clock cycles
			1: 23-27 clock cycles
			PLL_LOCK_EN
0	R/W	0x0	PLL clk lock enable
J	17/ ۷۷	0.00	0: disable
			1: enable

Reg 20h_System Clock Control Register

YA.	Y/A \	YA \
J'K''	J.K.	· · · · · · · · · · · · · · · · · · ·
Defectis@v.00	TO CHAIR NAME OVER LY CTRIVAL	·21-`
Default: 0x00	Register Name: SYSCLK CTRL	XT
	(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)	λ-X'3



	Mo		Way.20.2015
Bit	Read/Write	Default	Description
XX	NZ.		PULCLK_EN
7	R/W	0x0	PLLCLK Enable
III AND IN	K/VV	UXU	0: Disable
X		-(**X)	1: Enable
6	/	/	
			PLLCLK_SRC
			PLL Clock Source Select
5:4	R/W	0x0	0: MCLK
5.4	K/VV	UXU	1: BCLK
			2: PDMCLK
			3: Reserved
	1/80/180		SYSCLK_SRC System Clock Source Select 0: MCLK
	- 2/18CO		System Clock Source Select
3:2	RW	0x0	0: MCLK
J.Z	STAN .		1; BCLK
TXXX		-A	2: PLL
			3: Reserved
	/	1 - 1	
ř		/.	SYSCLK_EN
0	R/W	0x0	SYSCLK Enable
U	17/ 7/	UXU	0: Disable
			1: Enable

Reg 21h_Module Clock Enable Control Register

Default	Default: 0x00		Register Name: MOD_CLK_EN	
Bit	Read/Write	Default	Description 180	
7:3	1 200	1	1 Mag	18 Jan 30
	WIN.		Module clock enable control	7/2
	XX.		0-Clock disable	*
2:0	R/W	0x0	1-Clock enable	
2.0	IX/VV	OXO THE	BIT2- ADC analog	
* X/III.		深圳	BIT1- ADC digital	
			BIT0- I2S	

Reg 22h_Module Reset Control Register

Default: 0	0x00		Register Name: MOD_RST_CTRL	
Bit	Read/Write	Default	Description	
7:5	/	/	1	
4	R/W	0x0	Connect Globe Enable to I2S reset control 0: Enable 1: Disable	<i>"118</i> 0
3:2	LIV	/	1 812	ALIV TO THE PERSON OF THE PERS
1:0	R/W	0x0	Module reset control 0-Reset asserted	
Revision 1.4		Copy	right © 2018 X-Powers Limited. All Rights Reserved.	26



" M.	401	401	101
WILL.	1-Reset de-asserted	WIN.	WIN.
***	BIF1- ADC digital	A A A A A A A A A A A A A A A A A A A	14 Albar
The state of the s	BIT0- I2S		

Reg 30h_I2S Control Register

Default: 0x00			Register Name: I2S_CTRL
Bit	Read/Write	Default	Description
			BCLK_IOEN
7	R/W	0x0	0: Input
			1: Output
			LRCK_IOEN
6	R/W	0x0	0: Input
	CO /		1: Output
	Ma		MCLK JOEN
5	RW	0x0	0: Input
	XX		1. Output PLL_test
	×,		SDO_EN
4/2	R/W	0x0	0: Disable, Hi-Z state
, y		-1/2	1: Enable
3	/	1	1
			TXEN
2	R/W	0x0	Transmitter Block Enable
2	10,00	0.00	0: Disable
			1: Enable
			RXEN
1	R/W	0x0	Receiver Block Enable
•	1000	OXO	0: Disable
	Was a		1: Enable
	BA IV		GEN-
	XX		Globe Enable
0	R/W	0x0	A disable on this bit overrides any other block or channel enables.
WANTED IN		III/A	0: Disable
7/11		绿洲	1: Enable

Reg 31h_I2S BCLK Configure Register

Default: 0x00			Register Name: I2S_BCLK_CTRL
Bit	Read/Write	Default	Description
7:6	/	/	
			EDGE_TRANSFER
5	R/W	0x0	0: SDO drive data and SDI sample data at the different BCLK edge
	180		1: SDO drive data and SDI sample data at the same BCLK edge
	Ma		BCLK_POLARITY HIP
4	R/W	0x0	0: normal mode, negative edge drive
×A	E ST		1 invert mode, positive edge drive
3:0	R/W	0x0	BCLKDIV



			, 0/1	, W
	WIN.		BCLK Divide Ratio from SYSCLK	\$\\V\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
	A PARTY		0 reserved	A CONTRACTOR OF THE PARTY OF TH
		:	1: Divide by 1	
	A A A A A A A A A A A A A A A A A A A	177	2: Divide by 2	A THINGS
-4	.x////`	-1×11111	3: Divide by 4	- Şilli
		·	4: Divide by 6	
			5: Divide by 8	
			6: Divide by 12	
			7: Divide by 16	
			8: Divide by 24	
			9: Divide by 32	
			10: Divide by 48	
	120 120 120 120 120 120 120 120 120 120		11: Divide by 64	780
	, sco /		12: Divide by 96 13: Divide by 128 14: Divide by 176	-0/
			13: Divide by 128	The Talke
			14: Divide by 176	
	A A A A A A A A A A A A A A A A A A A	, Ag	15: Divide by 192	THE WAY
			This bit is only used in master mode	

Reg 32h_I2S LRCK Configure 1 Register

Default:	: 0x00		Register Name: I2S_LRCK_CTRL1
Bit	Read/Write	Default	Description
7:5	/	/	
			LRCK_POLARITY
			When apply in I2S / Left-Justified / Right-Justified mode:
			0: Left channel when LRCK is low
4	R/W 480	0x0	1: Left channel when LRCK is high
	120		When apply in PCM mode:
	The state of the s		0: PCM LRCK asserted at the negative edge
			1: PCM LRCK asserted at the positive edge
3:2	1	1	
			LRCK_PERIODH
illi, Li		Z HILL	The 2-High bit of LRCK period value. It is used to program the number of
		-711	BCLKs per channel of sample frame. This value is interpreted as follow:
			PCM mode: Number of BCLKs within (Left + Right) channel width
			I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each
4.0	DAM	0:-0	individual channel width (Left or Right)
1:0	R/W	0x0	N+1
			For example:
			n = 7: 8 BCLKs width
	780		1%
	.00		n = 1023: 1024 BCLKs width
	Who.		This bit is must be configured in master or slave mode



Reg 33h_I2S LRCK Configure 2 Register

Default: 0x00		,	Register Name: I2S_LRCK_CTRL2
Bit	Read/Write	Default	Description
*			LRCK_PERIODL **
			The 8-Low bit of LRCK period value. It is used to program the number of
			BCLKs per channel of sample frame. This value is interpreted as follow:
			PCM mode: Number of BCLKs within (Left + Right) channel width
			I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each
7:0	R/W	0x0	individual channel width (Left or Right)
7.0	R/VV	UXU	N+1
			For example:
	-Whoo too		n = 7: 8 BCLKs width
	"18Co		
	A LIZ		n = 1023: 1024 BCLKs width
	, 18 C		This bit is must be configured in master or slave mode

Reg 34h_I2S Format Configure 1 Register

Default	Default: 0x00		Register Name: I2S_FMT_CTRL1
Bit	Read/Write	Default	Description
			ENCD_FMT
			Encoding Mode coding format Selection
7	R/W	0x0	0: 0,1,,N-1
			1: 1,2,,N
			N is the channel (slot) number
			ENCD_SEL
6	R/W	0x0	Encoding Mode Selection
O	N/W Co	UXU	0: disable
	AIV		1: enable
,	A TOP OF THE PERSON NAMED IN COLUMN TO THE PERSON NAMED IN COLUMN		MODE_SEL
THE REAL PROPERTY.	87	0x0	Mode Selection
5.4	R/W		0: PCM mode (offset 0: PCM_B; offset 1: PCM_A)
ķ. '×λ'~+	IV/VV		1: Left-Justified mode (offset 0: LJ mode; offset 1: I2S mode)
			2: Right-Justified mode
			3: Reserved
3	1	1	
			TX_OFFSET
2	R/W	0x0	TX offset tune, TX data offset to LRCK
2	IX/VV	0.00	0: no offset
			1: data is offset by 1 BCLKs to LRCK
	180		TX_SLOT_H(Z) 480
1	R/W	0x0	0: normal mode for the last half cycle of BCLK in the slot
	ALE STATE OF THE S		1: turn to hi-z state for the last half cycle of BCLK in the slot
0	R/W	0x0	TX_STATE
X	37 17 77	0.00	0: transfer level 0 when not transferring slot



1: turn to hi-z state (TDM) when not transferring slot

Reg 35h_I2S Format Configure 2 Register

Default: 0x55			Register Name: I2S	_FMT_CTRL2
Bit	Read/Write	Default	Description	-1/K
7	/	/	/	
			SW	
			Slot Width Select	A
			0: Reserved	
			1: Reserved	
6:4	R/W	0x5	2: Reserved	
6.4	R/VV	UXS	3: 16-bit	The Cotos
	601		4: 20-bit	50,
	Na		5: 24-bit	Was
	KW TSO		6: 28-bit	III III II III II II II II II II II II
,	A CONTRACTOR OF THE PARTY OF TH		7:32-bit	Apply Apply
3	/	1	7	
			SR	
÷,,,			Sample Resolution	· · · · · · · · · · · · · · · · · · ·
			0: Reserved	
			1: Reserved	
2:0	R/W	0x5	2: Reserved	
2.0	IN/ VV	UXS	3: 16-bit	
			4: 20-bit	
			5: 24-bit	
			6: 28-bit	
	120		7: 32-bit	480

Reg 36h 12S Format Configure 3 Register

Default;	0x60		Register Name: I2S_FMT_CTRL3	-XX
Bit	Read/Write	Default	Description	
XIII KANDO		· till the	TX MLS	· sill Hilling
* ·	R/W	0,0	MSB / LSB First Select	
'	K/VV	0x0	0: MSB First	
			1: LSB First	
			SEXT	
			Sign Extend in slot [sample resolution < slot width]	
6:5	R/W	0x3	0: Zeros or audio gain padding at LSB position	
0.5	IN/VV	UXS	1: Sign extension at MSB position	
			2: Reserved	
	780		3: Transfer 0 after each sample in each slot	- 0
4	1 11/20	1		Ma
	ARLIV.		SDOUT Mute	WILL.
3	R/W	0x0	0 normal transfer	XA KAN
TX.	>'		1: force DOUT to output 0	in the second se



Y	Reliv		LRCK_WIDTH LRCK width	THE TOTAL STATE OF THE PARTY OF
2	R/W	0x0	0: LRCK = 1 BCLK width (short frame)	A KANA
A TO THE WAY		A THE THE	1: LRCK = 2 BCLK width (long frame)	NA PARTY.
XIII.		-1×1/11.	(this bit is only used in PCM mode)	- Film
			TX_PDM	
			PCM Data Mode	
			0: Linear PCM	
1:0	R/W	0x0	1: reserved	
			2: 8-bits u-law	
			3: 8-bits A-law	
			(this bit is only used in PCM mode)	

Reg 38h_I2S TX Control 1 Register

Default:	0x00		Register Name: I2S_TX_CTRL1	
Bit	Read/Write	Default	Description	
7:4	/	1		
A THE STATE OF THE			TX_CHSEL (A)	
**************************************			TX Channel (slot) number Select for each output	
			0: 1 channel (slot)	
3:0	R/W	0x0		
3.0	IX/VV	UXU	7: 8 channels (slots)	
			8: 9 channels (slots)	
			15: 16 channels (slots)	

Reg 39h_I2S TX Control 2 Register

Default: 0x00			Register Name: I2S_TX_CTRL2	
Bit Read/Write Default			Description	
×	XX		TX_CHEN_LOW	
			TX Channel1 ~Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or	
7:0	R/W	0x0,,,,	more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state	
K		·徐"	0: disable	
			1: enable	

Reg 3Ah_I2S TX Control 3 Register

Default: 0x00			Register Name: I2S_TX_CTRL3	
Bit	Read/Write	Default	Description	
			TX_CHEN_HIGH	
	180		TX Channel9 Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one	
7:0	R/W	0x0	or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state	
	W.o.		0: disable	
	JAN 10		1: enable	



Reg 3Ch_I2S TX Channel Mapping Control 1 Register

Default: 0x00		^^_	Register Name: I2S_TX_CHMP_CTRL1	
Bít	Read/Write	Default	Description	
× XX		-1/2	TX_CH8_MAP	
-	DAM		TX Channel8 Mapping	
7	R/W	0x0	0: 1st adc sample	
			1: 2th adc sample	
			TX_CH7_MAP	
6	DAM	0.40	TX Channel7 Mapping	
6	R/W	0x0	0: 1st adc sample	
			1: 2th adc sample	
	180		TX_CH6_MAP	
E	R/M/NOO TO	0.40	TX_CH6_MAP TX Channel6 Mapping 0: 1st adc sample	No
5	R/W	0x0	0: 1st adc sample	77.
			1: 2th adc sample	
The state of the s	257	-56	TX_CH5_MAP	
NA THE THE	R/W	Ovo ×	TX Channel5 Mapping	
* H	K/VV	0x0	0: 1st adc sample	
ī		1.	1: 2th adc sample	
			TX_CH4_MAP	
3	R/W	0x0	TX Channel4 Mapping	
3	IX/VV	UXU	0: 1st adc sample	
			1: 2th adc sample	
			TX_CH3_MAP	
2	R/W	0x0	TX Channel3 Mapping	
2	780	UNO	0: 1st adc sample	
	20/		0: 1st adc sample 1: 2th adc sample	, 20
	The state of the s		TX_CH2_MAP	Mr.
1	R/W	0x0	TX Channel2 Mapping	
- T	X	O/IO	0: 1st adc sample	
			1: 2th adc sample	
XIII.		:ÆHIITT	TX_CH1_MAP	
0	R/W	0x0	TX Channel1 Mapping	
-			0: 1st adc sample	
			1: 2th adc sample	

Reg 3Dh_I2S TX Channel Mapping Control 2 Register

Default: 0x00		Register Name: I2S_TX_0	CHMP_CTRL2		
Bit	Read/Write	Default	Description		
	180		TX_CH16_MAP	180	
_	DAN 80	00	TX Channel16 Mapping	18CO/	
/	R/W	0x0	0: 1st adc sample	The state of the s	
			1: 2th adc sample		
6	R/W	0x0	TX_CH15_MAP		A KANA



	" No		100		May.20.2019
	WILL.		TX Channel15 Mapping	WILL.	WIN.
X			0:1st adc sample	A A A A A A A A A A A A A A A A A A A	XA TOP YOU
			1: 2th adc sample	**************************************	
		W. Kaling	TX_CH14_MAP		A TOP TO THE PERSON NAMED IN COLUMN
5	R/W	0x0	TX Channel14 Mapping	-\$************************************	'in
	TO VV	OXO	0: 1st adc sample		
			1: 2th adc sample		
			TX_CH13_MAP		
4	R/W	0x0	TX Channel13 Mapping		
-	IX/VV	OXO	0: 1st adc sample		
			1: 2th adc sample		
			TX_CH12_MAP		
3	R/W	0x0	TX Channel 12 Mapping	780	
	1000		0: 1st adc sample	"18Co	2180
	112		1: 2th adc sample		112
			TX_CH11_MAP		
2	R/W	0x0	TX Channel11 Mapping	in the last of the	TAXXX
Z AND THE S	IX/VV	OXO	0: 1st adc sample		A TOTAL STATE OF THE STATE OF T
ZIII'r'		TEXIII'I'	1: 2th adc sample		West of the second
1.		-/1,	TX_CH10_MAP	11.	
1	R/W	0x0	TX Channel10 Mapping		
'	K/VV	UXU	0: 1st adc sample		
			1: 2th adc sample	· ·	
			TX_CH9_MAP		
0	R/W	0x0	TX Channel9 Mapping		
	IX/VV	UXU	0: 1st adc sample		
	180		1: 2th adc sample	-180	
· · · · · · · · · · · · · · · · · · ·		· ·			·

Reg 50h 12S RX Control 1 Register

Default: 0x00			Register Name: I2S_RX_CTRL1		
Bit ***	Read/Write	Default	Description		
7:4	1	1	1 Albita	H. M. S. C.	
* XIIII		採圳	RX_CHSEL	-::\hat{\psi}	
			RX Channel (slot) number Select for each input	1	
			0: 1 channel (slot)		
3:0	R/W	0x0			
3.0	IN/VV	UXU	7: 8 channels (slots)		
			8: 9 channels (slots)		
			15: 16 channels (slots)		

Reg 51h_I2S RX Control 2 Register

Default: 0x03		Register Name: I2S_RX_CTRL2		#1/A
Bit Read/Write	Default	Description	AL TOP TO THE PARTY OF THE PART	XX TO THE TOTAL PROPERTY OF THE TOTAL PROPER
7:0 R/W	0x3	RX_CHEN_LOW		



* M.		* 101.			
ALV		RX Channel1 ~0	Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or	
XA XXV		more slot(s) is(a	re) disabled, the affected slot	(s) is(are) set to disable state	
		0: disable			
A TOP TO SERVICE AND A SERVICE	A A A A A A A A A A A A A A A A A A A	1: enable		A A A A A A A A A A A A A A A A A A A	

Reg 52h_I2S RX Control 3 Register

Default: 0x00			Register Name: I2S_RX_CTRL3
Bit Read/Write Default		Default	Description
			RX_CHEN_HIGH
			RX Channel9 ~Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one
7:0	R/W	0x0	or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state
	-0		0: disable
	780		1: enable

Reg 54h_I2S RX Channel Mapping Control 1 Register

Default: 0x00		Á	Register Name: I2S_RX_CHMP_CTRL1
Bit	Read/Write	Default	Description
HILL		- SE HILLS	RX_CH8_MAP
7	R/W	0x0	RX Channel8 Mapping
<i>'</i>	K/VV	UXU	0: 1st adc sample
			1: 2th adc sample
			RX_CH7_MAP
6	R/W	0x0	RX Channel7 Mapping
0	IN/VV	UXU	0: 1st adc sample
			1: 2th adc sample
	180		RX_CH6_MAP RX Channel6 Mapping 0: 1st adc sample 1: 2th adc sample
5	R/W	0x0	RX Channel6 Mapping
3		UAU	0: 1st add sample
	SELV.		1: 2th adc sample
(ZX)			RX_CH5_MAP
4	R/W	0x0	RX Channel5 Mapping
HIM HIM	1000	OXO HITTER	0: 1st adc sample
*		**	1: 2th adc sample
			RX_CH4_MAP
3	R/W	0x0	RX Channel4 Mapping
3	10/00	OXO	0: 1st adc sample
			1: 2th adc sample
			RX_CH3_MAP
2	R/W	0x0	RX Channel3 Mapping
_	10,00	OAO	0: 1st adc sample
	180		1: 2th adc sample
	Ma		RX_CH2_MAP
1	R/W 0x0	0x0	RX Channel2 Mapping
	20,00	0,0	0:1st adc sample
		:@	1: 2th adc sample



No		10/10	100	Way.20.2019
ALIV TO		RX_CH1_MAP	ALIV TO	WIN.
0 R/W	0x0	RX Channel1 Mapping	×4 th	XA TOP NO.
O TOVV	UNU	0: 1st adc sample		
A A A A A A A A A A A A A A A A A A A	10 10 10 10 10 10 10 10 10 10 10 10 10 1	1: 2th adc sample	All the second s	A A A A A A A A A A A A A A A A A A A

Reg 55h_I2S RX Channel Mapping Control 2 Register

Default: 0x00			Register Name: I2S_RX_CHMP_CTRL2
Bit Read/Write Default		Default	Description
			RX_CH16_MAP
7	DAM	00	RX Channel16 Mapping
7	R/W	0x0	0: 1st adc sample
	-0		1: 2th adc sample
	7,0		RX_CH15_MAP
0	RAW	0.40	RX Channel15 Mapping
6	R/W	0x0	0: 1st adc sample
	XA S		1. 2th adc sample
	X	## T	RX_CH14_MAP
. * 5 ***********************************	R/W	ONO INTERNATIONAL	RX Channel14 Mapping
.×	R/VV	0x0	0: 1st adc sample
			1: 2th adc sample
			RX_CH13_MAP
4	R/W	0.40	RX Channel13 Mapping
4	R/VV	0x0	0: 1st adc sample
			1: 2th adc sample
			RX_CH12_MAP
3	R/W	0x0	RX Channel12 Mapping
3	1/4/	UXU	0: 1st adc sample
	1800		0: 1st adc sample 1: 2th adc sample RX_CH11_MAP RX_Channel11 Mapping
	WIN TO SHARE		RX_CH11_MAP
2	R/W	0x0	RX Channel11 Mapping
2	17/17	UNU	0: 1st adc sample
A TOTAL STATE OF THE STATE OF T		A STATE OF THE STA	1: 2th adc sample
XIIII.		读删	RX_CH10_MAP
1	R/W	0x0	RX Channel10 Mapping
•	10,00	UNU	0: 1st adc sample
			1: 2th adc sample
			RX_CH9_MAP
0	R/W	0x0	RX Channel9 Mapping
5	1 X/ V V	0.00	0: 1st adc sample
			1: 2th adc sample

Reg 59h_PDM Control Register

Default: 0x00		Register Name: PDM_CTRL	\$1\range \text{\$\sigma_1\range}\$
Bit Read/Write	Default	Description	
7:2	1		,



		" OI,		
		ALIV TO THE PROPERTY OF THE PR		PDM_TIMING
	X	West Control of the C	×	PDM timing control
	1	R/W	0x0	0: Latch ADC1 data on rising clock edge. Latch ADC2 data on falling clock
		IX/VV	OXO MAIN	edge.
-4	XIII.		宗科州	1: Latch ADC1 data on falling clock edge. Latch ADC2 data on rising clock
			·	edge.
				PDM_EN
				PDM interface Enable
	0	R/W	0x0	0: Disable
	0	IX/VV	OXO	1: Enable
				When PDM_EN = 1, LRCK is used for PDMCLK input and SDOUT is used
				for PDMDATA output.

Reg 60h_ADC Sample Rate Select Register

Default: 0x00			Register Name: ADC_SPRC
Bit	Read/Write	Default 🐰	Description
7:4	/	1	
·IIIXI			ADC_FS_I2S
**************************************		- (** XIII.	ADC Sample Rate synchronized with I2S clock zone
			0000: 8KHz
			0001: 11.025KHz
			0010: 12KHz
3:0	R/W	0x0	0011: 16KHz
3.0	17/ 77	OXO .	0100: 22.05KHz
			0101: 24KHz
			0110: 32KHz
	780		0111: 44.1KHz
	-11/480 180		1000: 48KHz Other: Reserved
	NIZ.		Other: Reserved

Reg 61h_ADC Digital Part Enable Register

Default:	0x00		Register Name: ADC_DIG_EN
Bit	Read/Write	Default	Description
			REQ_WIDTH
7:4	R/W	0x0	0:min
7.4	IK/VV	OXO	
			15:max
			REQ_EN
3	R/W	0x0	0: Disable
			1: Enable
	780		DG_EN 488
0	DAMARO	0.40	ADC Digital part globe enable 0: Disable
2	R/W	0x0	ADC Digital part globe enable 0: Disable
J	The state of the s	,	(A): Enable
1	R/W	0x0	ENAD2



	Me		Me	Me	. The
	WILL.		ADC2 digital part enable	WIV.	WIV.
×4	West of the second	×	0: Disable	XX (A)	XX (A)
THE WAY			1: Enable	A TANK	
WANTED TO THE PARTY OF THE PART			ENAD1	'i'	
***	R/W	0x0	ADC1 digital part enable		-(* *)
0	IN/VV	UXU	0: Disable		
			1: Enable		

Reg 66h_Digital HPF Enable Register

Default:	0x03		Register Name: HPF_EN
Bit	Read/Write	Default	Description
7:2	1	/	1
	co/		DIG_ADC2_HPF_EN
1 RAW		Digital ADC2 channel HPF enable	
	RAW	0x1	0: Disable
×		×	T: Enable
A SANTA		A STATE OF THE PARTY OF THE PAR	DIG_ADC1_HPF_EN
William.	DAM	0x1	Digital ADC1 channel HPF enable
**************************************	R/W		0: Disable
			1: Enable

Reg 70h_ADC1 Digital Channel Volume Control Register

Default: ()xA0		Register Name: ADC1_DVOL_CTRL	
Bit	Read/Write	Default	Description	
			DIG_ADCL1_VOL	
	180		ADC1 Digital channel volume Control	
	-13/10 Teo		(-119.25dB To 71.25dB, 0.75dB/Step)	C.C
	William		0x00; Mute	8
	IR IV		0x00: Mute 0x01: -119.25dB	
7:0	R/W	0xA0	The state of the s	
			0x9F = -0.75dB	
HIII HIN		till History	0xA0 = 0dB	
*		条"	0xA1 = 0.75dB	
			0xFF = 71.25dB	

Reg 71h_ADC2 Digital Channel Volume Control Register

Default: 0xA0			Register Name: ADC2_DVOL_CTRL
Bit	Read/Write	Default	Description
	180		DIG_ADCL2_VOL
	.00		ADC2 Digital channel volume Control
7:0	R/W	0xA0	(-119.25dB To 71.25dB, 0.75dB/Step)
,	WIV .		0x00: Mute
A XX	Ø.	, EX	0x01: -119.25dB



Reg 76h_ADC1 Digital Mixer Source Control Register

Default:	0x01		Register Name: ADC1_DMIX_SRC
Bit	Read/Write	Default	Description
7:4	1	/	1
	0		ADC1_DMXL_GC
	7.0		ADC1 channel digital mixer gain control
3:2	R/W	0x0	0: 0dB //f: -6dB
	ARIV .		Bit3: ADC2 data
1			Bit2: ADC1 data
A THE YEAR			ADC1_DMXL_SRC
			ADC1 channel digital mixer source select
1:0	R/W	0x1	0: Disable 1: Enable
			Bit1: ADC2 data
			Bit0: ADC1 data

Reg 77h_ADC2 Digital Mixer Source Control Register

Default: ()x02		Register Name: ADC2_DMIX_SRC	
Bit	Read/Write	Default	Description	
7:4	1	/	1 120	
	GO/		ADC2_DMXL_GC	C
	Was a		ADC2 channel digital mixer gain control	Was all the second
3:2	RW	0x0	0: 0dB 1: -6dB	CANAL PROPERTY OF THE PROPERTY
	8)		Bit3: ADC2 data	
			Bit2: ADC1 data	
XIII KIND		till His	ADC2_DMXL_SRC	A THE THE PARTY OF
*		- 宋	ADC2 channel digital mixer source select	·**
1:0	R/W	0x2	0: Disable 1: Enable	
			Bit1: ADC2 data	
			Bit0: ADC1 data	

Reg 7Fh_ADC Digital Debug Control Register

Default: 0x00			Register Name: ADC_DI	G_DEBUG	
Bit	Read/Write	Default	Description_	180	
7:4	1 ,00	/	1 20	,20	, C
	- Tille		I2S_LPB_DEBUG		
3	R/W	0x0	RX-> TXdata loopback	R.V	THE IV
52	XX Company		0: disable	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	XXX



		4 60		4.60
		\$1\rangle \(\sqrt{1}\rangle \)		1: enable
	XXX	Apr.		ADC_PTN_SEL
	THE WAY			ADC Pattern Select
	A A A A A A A A A A A A A A A A A A A		IN THE PARTY.	000: Normal
-4	X		-1/2/11	001: 0x5A5A5A(24-bit)
	2:0	R/W	0x0	010: 0x123456 (24-bit)
				011: zero data
				1xx: I2S_RX data
				When this bit selected, the digital path data source will be changed to internal
				rom data

Reg 81h_ADC Analog Debug Control 2 Register

Default: ()x11		Register Name: ADC_ANA_DEBUG2
Bit	Read/Write	Default	Description (N)
7	AIV	/	
×A		×	Pad Select for DEV_ID1 PIN.
G. A.	DAM	0x1	000: IO Disable
6:4	R/W		001: DEV_ID1
****			other: Reserved
3	/	/	
			Pad Select for DEV_ID0 PIN.
2.0	DAM	0x1	000: IO Disable
2:0	R/W		001: DEV_ID0
			other: Reserved

Reg 82h_I2S Pad Drive Control Register

Default: 0)x55		Register Nam	ne: I2S_PADDRV_CTRL	.03
Bit	Read/Write	Default	Description	(i) Mo	WW.
	NA TOP TO THE PARTY OF THE PART		Pad programn	nable drive control for MCLK.	A STATE OF THE STA
7:6	R/W	0x1	00: Level 0	01: Level 1	A A A A A A A A A A A A A A A A A A A
			10: Level 2	11: Level 3	
A KINITED TO THE PARTY OF THE P			Pad programn	nable drive control for BCLK.	i till the
5:4	R/W	0x1	00: Level 0	01: Level 1	(\vec{k}')
			10: Level 2	11: Level 3	
			Pad programn	nable drive control for LRCK.	
3:2	R/W	0x1	00: Level 0	01: Level 1	
			10: Level 2	11: Level 3	
			Pad programn	nable drive control for SDOUT.	
1:0	R/W	0x1	00: Level 0	01: Level 1	
	.0		10: Level 2	11: Level 3	

Reg A0h_ADC1 Analog Control 1 Register

Default:0x00		Register Name: ANA_ADC	1_CTRL1	
Bit R/W	Default	Description	A STATE OF THE STA	XXXX



	No		Way.20.2019
	ARIV TO		RX1_PGA_OI_CTRL
XX	AN AND AND AND AND AND AND AND AND AND A		Channel 1 PGA Output Current Driver Strength Control
			0=301 4=501
7:5	R/W	0x0	1 = 251 5 = 451
**************************************		-(*X)	2 = 401 6 = 601
		,	3 = 35l 7 = 55l
			I = Bias current of OTA, default = 5uA
			RX1_PGA_AMP_IB_SEL
		00	Channel 1 PGA Bias Current Control
4:2	R/W		0 = 5 uA 4 = 3 uA
4.2	R/VV	0x0	1 = 5.5 uA 5 = 3.5 uA
			2 = 6 uA 6 = 4 uA
	7.	o o	3 = 6.5 uA 7 = 4.5 uA
	120		RX1_PGA_IN_VCM_CTRL
	THE WAY		Channel 1 PGA High-gain Common-Mode Voltage Control $0 = 1.65V$
	No.		0 = 1,65V
1:0	R/W	0x0	1, ± 1.45V
			2 = 1.39V
EXIII TO		- (<u>-</u> <u>X</u>)	3 = 1.29V
- IV		-//	when PGA work on low-gain(0/-6dB), the Common-Mode Voltage is fixed 1.65V.

Reg A1h_ADC1 Analog Control 2 Register

Default:0)x00		Register Name: ANA_ADC1_CTRL2
Bit	R/W	Default	Description
7:6	/	/	
			RX1_PGA_OI_NM_CTRL
	7.	0	Channel 1 PGA High Gain Output Current Driver Strength Control
	1/8CO.		0 = 21 4 = 33
5:3	R/W	0x0	0 = 21 4 = 33 1 = 24 5 = 36 2 = 15 6 = 27 3 = 18 7 = 30
,	A CONTRACTOR OF THE PARTY OF TH		2 = 151 6 = 271
A KANA			3 = 18 I 7 = 30 I
			F = Bias current of OTA, default = 5uA
*iller		-ŵ.	RX1_PGA_NMAMP_IB_SEL
		11.	Channel 1 PGA High Gain Bias Current Control
2:0	D AAA	0x0	0 = 5 uA 4 = 3 uA
2.0	R/W	UXU	1 = 5.5 uA 5 = 3.5 uA
			2 = 6 uA 6 = 4 uA
			3 = 6.5 uA 7 = 4.5 uA

Reg A2h_ADC1 Analog Control 3 Register

Default:0x00		%0	Register Name: ANA_ADC1_CTRL3		
Bit	R/W	Default	Description		100
7	1 IV	/	1	DIV.	AIV
6:5	R/W	0x0	RX1_PGA_CTRL_RCM Channel 1 high-gain PGA inpu	t impedance control	



	N.o.		No		No.	IVIAY.20.20 198
	ALV STATE		0 = 100 kΩ		A Party of the Par	A LIVE
A XA	K.		1 = 75 kΩ 2 = 50 kΩ		A STATE OF THE STA	A STATE OF THE STA
			$3 = 25 \text{ k}\Omega$			
*ill(t)		- <u>^</u>		on 0dB/-6dB	the input impedance is 8K/16k	
		,	RX1_PGA_GAIN	N_CTRL		7.
			Channel 1 PGA	gain settings:		
			0 = -6 dB	16 = 15 dB		
			1 = 0 dB	17 = 16 dB		
			2 = 0 dB	18 = 17 dB		
			3 = 0 dB	19 = 18 dB		
			4 = 3 dB	20 = 19 dB		
	7,	,O		$21^{\circ} = 20 \text{ dB}$	480	
4:0	R/W/N	0x0	" Vo	22 = 21 dB	Wild Maco Jao	1/20
	AIV		. \\>	23 = 22 dB		THE IT THE
, Xa	A CONTRACTOR OF THE PARTY OF TH		8 = 7 dB	24 = 23 dB	A MARKET	NAME OF THE PERSON OF THE PERS
- AKXY			9 = 8 dB	25 = 24 dB		in KXXX
X III			10 = 9 dB		1 Hillian	A THE STATE OF THE
XIIII		-(x)	11 = 10 dB	27 = 26 dB) ::[x] · ·
		,	12 = 11 dB	28 = 27 dB		,
			13 = 12 dB			
			14 = 13 dB	30 = 29 dB		
			15 = 14 dB	31 = 30 dB		

Reg A3h_ADC1 Analog Control 4 Register

Default:0	x00		Register Name: ANA_ADC1_CTRL4
Bit	R/W 49	[©] Default	Description 180 180
	Msco		RX1_DSM_OTA_IB_SEL
	ALIZ		Channel 1 DSM Integrator Bias Current Control
7:5	R/W	0x0	0 = 6 uA 4 = 4 uA
7.5	N/VV	UXU	1 ⇒ 6.5 uA 5 = 4.5 uA
			2 = 7 uA 6 = 5 uA
EXIII TO		金料	3 = 7.5 uA 7 = 5.5 uA
(1-		-11.	RX1_DSM_COMP_IB_SEL
			Channel 1 DSM Comparator Bias Current Control
4.0	DAM	0.40	0 = 6 uA 4 = 4 uA
4:2	R/W	0x0	1 = 6.5 uA $5 = 4.5 uA$
			2 = 7 uA 6 = 5 uA
			3 = 7.5 uA $7 = 5.5 uA$
			RX1_DSM_OTA_CTRL
	1.0	Ó	Channel 1 DSM Integrator Driver Strength Control
4.0	DAM CO		0 = 100% enabled
1:0	R/W	0x0	1 = 80% enabled 2 = 60% enabled
	SELIZ		2 = 60% enabled
	(P)		3 = 40% enabled



Reg A4h_ADC1 Analog Control 5 Register

Default	t:0x00		Register Name: ANA_ADC1_CTRL5
Bit	R/W	Default	Description
₹ 7	/	/ 籴	
			RX1_GLOBAL_EN
6	DAM	0x0	Channel 1 Global Enable
O	R/W	UXU	0 = Disable
			1 = Enable
			RX1_DSM_DISABLE
5	R/W	0x0	Channel 1 DSM Disable
3	10,00	0.00	0 = Enable
	7,	2	1 = Disable
	18 18 18 18 18 18 18 18 18 18 18 18 18 1		RX1_DSM_DEMOFF
4	R/W	W 0x0	Channel 1 DSM DEM Control
,	TK/VV		0 = Enable DEM
The same of the sa	××′		1 Disable DEM
III A THE TO SERVE THE SERVE THE TO SERVE THE TO SERVE THE TO SERVE THE SER		4	RX1_SEL_OUT_EDGE
3	R/W	0x0	ADC clocking edge Select
			0 = DSM output is clocked on falling edge of input clock
			1 = DSM output is clocked on rising edge of input clock
			RX1_DSM_VRP_LPMODE
2	R/W	0x0	Channel 1 VREFP Low Power Mode
_			0 = Normal
			1 = Low Power Mode
			RX1_DSM_VRP_OUTCTRL
	7.	\$ ⁰	Channel 1 VREFP Output Strength Control
1:0	R/W _M	0x0	0 = 100%
	ALZ		1 = 75%
	X MINE		2 = 50%
4	XX		3 = 25%

Reg A5h_ADC2 Analog Control 1 Register

Defaul	Default:0x00		Register Name: ANA_ADC2_CTRL1	
Bit	R/W	Default	Description	
			RX2_PGA_OI_CTRL	
			Channel 2 PGA Output Current Driver Strength Control	
			0 = 30l 4 = 50l	
7:5	R/W	0x0	1 = 25l 5 = 45l	
			2 = 401 6 = 601	
	-	130	3 = 35l 7 = 55l√∞ √∞	
	1,80		I = Bias current of OTA, default = 5uA	ç
	The state of the s		RX2_PGA_AMP_IB_SEL	
4:2	R/W	0x0	RX2_PGA_AMP_IB_SEL Channel 2 PGA Bias Current Control	
4	X		0.= 5 uA 4 = 3 uA	



	allo				
	WIN.		1 = 5.5 uA 5 = 3.5 uA	WIL.	WIN.
.X4	(h)		2 = 6 uA 6 = 4 uA	XA TANK	XX (A)
			3 = 6.5 uA $7 = 4.5 uA$	A STATE OF THE STA	in the state of th
11/4/1/2 K			RX2_PGA_IN_VCM_CTRL		WAS CALLED TO THE PARTY OF THE
***		-(*X)	Channel 2 PGA High-gain Co	mmon-Mode Voltage Control	深圳
			0 = 1.65V		
1:0	R/W	0x0	1 = 1.45V		
			2 = 1.39V		
			3 = 1.29V		
			when PGA work on low-gain(0/-6dB), the Common-Mode Vo	ltage is fixed 1.65V.

Reg A6h_ADC2 Analog Control 2 Register

Default:0	x00	8	Register Name: ANA_ADC2_CTRL2
Bit	R/W	Default	Description 100 100
7:6	LIV	/	
			RX2_PGA_OI_NM_CTRL
A STATE OF THE PARTY OF THE PAR			Channel 2 PGA High Gain Output Current Driver Strength Control
A THE STATE OF THE			0 = 21 I 4 = 33 I
5:3	R/W	0x0 🕸	1 = 24 5 = 36 **********************************
			2 = 15 6 = 27
			3 = 18 7 = 30
			I = Bias current of OTA, default = 5uA
			RX2_PGA_NMAMP_IB_SEL
			Channel 2 PGA High Gain Bias Current Control
0.0	D 444	00	0 = 5 uA 4 = 3 uA
2:0	R/W	0x0	1 = 5.5 uA 5 = 3.5 uA
	73	8	2 = 6 uA 6 = 4 uA
	-18Co.		3 = 6.5 uA 7 = 4.5 uA

Reg A7h_ADC2 Analog Control 3 Register

Default	t:0x00		Register Name: ANA_ADC2_CTRL3
Bit	R/W	Default	Description
7	1	/ 宋	/ · · · · · · · · · · · · · · · · · · ·
			RX2_PGA_CTRL_RCM
			Channel 2 high-gain PGA input impedance control
			$0 = 100 \text{ k}\Omega$
6:5	R/W	0x0	1 = 75 kΩ
			$2 = 50 \text{ k}\Omega$
			$3 = 25 \text{ k}\Omega$
			when PGA work on 0dB/-6dB, the input impedance is 8K/16K.
	7,	2	RX2_PGA_GAIN_CTRL
	Talso.		Channel 2 PGA gain settings:
4:0	R/W	0x0	0 = ¬6 dB 16 = 15 dB
	74 18 ST		Channel 2 PGA gain settings: 0 = -6 dB 16 = 15 dB 1 = 0 dB 17 = 16 dB
	Ŷ\$ ^T		2 = 0 dB 18 = 17 dB



WIN.	3 = 0 dB 19 = 18 dB	
A STATE OF THE STA	4 = 3 dB 20 = 19 dB	A THE STATE OF THE
The state of the s	5 = 4 dB 21 = 20 dB	NT CONTRACTOR OF THE PARTY OF T
	6 = 5 dB 22 = 21 dB	
4. July 1997	7 = 6 dB 23 = 22 dB	-(\$\frac{1}{2}\t
	8 = 7 dB 24 = 23 dB	
	9 = 8 dB 25 = 24 dB	
	10 = 9 dB 26 = 25 dB	
	11 = 10 dB 27 = 26 dB	
	12 = 11 dB 28 = 27 dB	
	13 = 12 dB 29 = 28 dB	
	14 = 13 dB 30 = 29 dB	
120	15 = 14 dB 31 = 30 dB	480

Reg A8h ADC2 Analog Control 4 Register

	. S. V		
Default:0)x00		Register Name: ANA_ADC2_CTRL4
Bit ***	R/W	Default	Description
WAS TO SEE SEE SEE SEE SEE SEE SEE SEE SEE SE			RX2_DSM_OTA_IB_SEL
*******		-4	Channel 2 DSM Integrator Bias Current Control
7:5	R/W	0x0	0 = 6 uA 4 = 4 uA
7.5	IK/VV	UXU	1 = 6.5 uA 5 = 4.5 uA
			2 = 7 uA 6 = 5 uA
			3 = 7.5 uA 7 = 5.5 uA
			RX2_DSM_COMP_IB_SEL
			Channel 2 DSM Comparator Bias Current Control
4:2	R/W	0.0	0 = 6 uA 4 = 4 uA
4.2	1,44	0x0	1 = 6.5 uA 5 = 4.5 uA
	VPUSCO_1,		2 = 7 uA 6 = 5 uA
	A LIZ		3 = 7.5 uA 7 = 5.5 uA
			RX2_DSM_OTA_CTRL
- AFX			Channel 2 DSM Integrator Driver Strength Control
1:0	R/W	0x0	0 ≥ 100% enabled
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	IX/VV	UXU -	1 = 80% enabled
1		-11.	2 = 60% enabled
			3 = 40% enabled

Reg A9h_ADC2 Analog Control 5 Register

Default:0x00			Register Name: ANA_ADC2	_CTRL5	
Bit	R/W	Default	Description		
7	/	/	/		
6	R/M/NSO	0x0	RX2_GLOBAL_EN Channel 2 Global Enable 0 = Disable 1 = Enable	* Table Tab	A THE STATE OF THE
5	R/W	0x0	RX2_DSM_DISABLE	A CONTRACTOR OF THE CONTRACTOR	A CONTRACTOR OF THE PARTY OF TH



	77.00	No		May.20.2019	
		ARIV (III)		Channel 2 DSM Disable	
	X	(A)		0 = Enable	
	THE WAY			1 Disable	
				RX2_DSM_DEMOFF	
-4	*	DAM	0.0 ·	Channel 2 DSM DEM Control	
	4	R/W	0x0	0 = Enable DEM	
				1 = Disable DEM	
		R/W		RX2_SEL_OUT_EDGE	
	2		0x0	Channel 2 ADC clocking edge Select	
	3			0 = DSM output is clocked on falling edge of input clock	
				1 = DSM output is clocked on rising edge of input clock	
				RX2_DSM_VRP_LPMODE	
	2	R/W T	180 Ov0	Channel 2 VREFP Low Power Mode	~
	2		0x0	0 = Normal	9
				1 = Low Power Mode	
	.1			RX2_DSM_VRP_OUTCTRL	
	XX			Channel 2 VREFP Output Strength Control	
	1:0	R/W	٥٧٥	0 = 100%	
N. N.	till (0	IX/VV	-4	1 = 75%	
-1	r			2 = 50%	
				3 = 25%	

Reg AAh_ADC Dither Control Register

Default:0	Default:0x00		Register Name: ADC_DITHER_CTRL
Bit	R/W	Default	Description
7:6	/	/	1
	7,	, O	DSM_DITHER_CTRL
	18C0		Control of the input pin: dsm_dither_sign and dsm_dither_data
E. 1	R/W	0.40	Control of the input pin: dsm_dither_sign and dsm_dither_data 00: single-stage shaped pseudorandom dither signal 01: original pseudorandom dither signal 10: offset voltage of the positive direction
5:4	TX/VV	0x0	01: original pseudorandom dither signal
THE WAY			10: offset voltage of the positive direction
1000			11: offset voltage of the negative direction
*		·ķ ^X	DSM_DITHER_EN
3	R/W	1	Dither Enable
3	K/VV		0 = Disable
			1 = Enable
			DSM_DITHER_LVL
2:0	R/W	0v0	Dither level control(Dither level is positive related to the ctrl bits)
2.0	FX/VV	0x0	000 have no level
			1 is the mim level and 7 is the max level

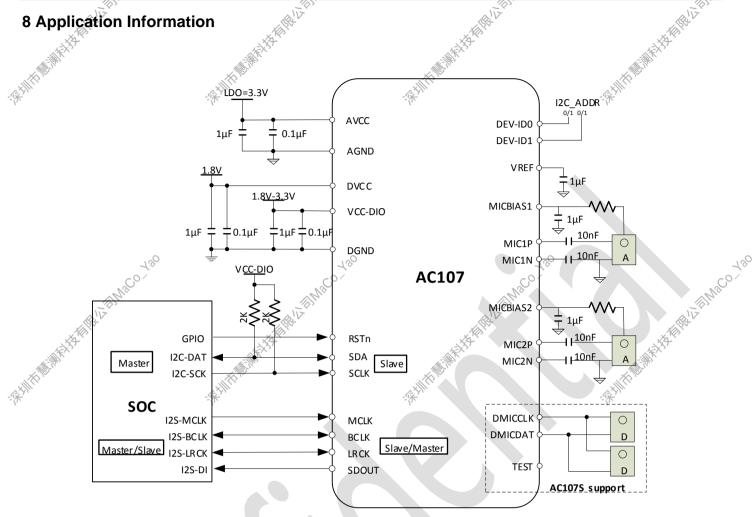


Figure 8-1. Typical Application Diagram

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9 PCB Layout Guidelines

Each system design and PCB layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the AC107 performance:

- 1. The decoupling capacitors for the power supplies must be placed close to the device terminals. Figure 8-1 shows the recommended decoupling capacitors for the AC107.
- 2. For analog differential audio signals, they must be routed differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to avoid undesirable crosstalk.
- 3. Analog and digital grounds must be separated to prevent possible digital noise from affecting the analog performance of the board.

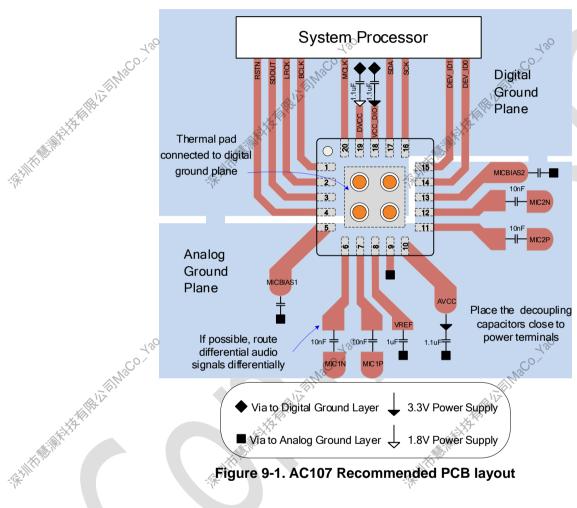


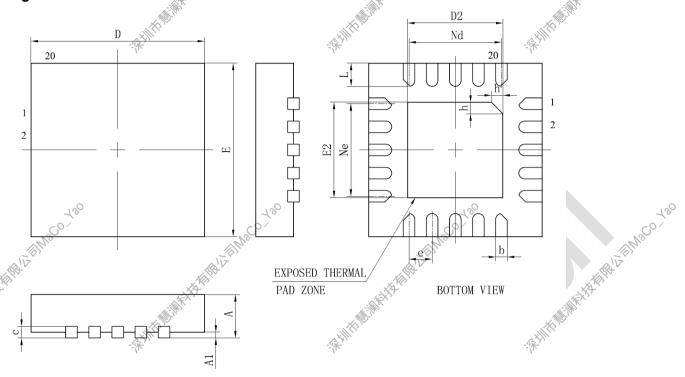
Figure 9-1. AC107 Recommended PCB layout

- Filling White Har Barre Co. 180



10 Package And Ordering Information

10.1 Package Information



A1

				· ·
SYMBOL	M	ILLIMETI	ER	
SIMBOL	MIN	NOM	MAX	
A	0.70	0.75	0.80	
A1		0.02	0.05	
b	0.15	0. 20	0. 25	Whiso to
c A	0. 18	0. 20	0. 25	(I) Ma
District	2. 90	3.00	3.10	7
D 2	1. 55	1. 65	1. 75	
e e		0. 40BSC	<i></i>	
Ne		1. 60BSC		
Nd		1.60BSC		
Е	2. 90	3. 00	3. 10	
E2	1. 55	1.65	1. 75	
L	0.35	0.40	0.45	
h	0,20	0. 25	0.30	180

Figure 10-1, AC107 Package Dimension: 20 QFN

75*75

L/F载体尺寸

- FEHITIME THE LINE OF YOU

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Figure 10-2. AC107S Package Dimension: 24 QFN

3.90

2.40

0.35

0.30

Е

E2

L

h

L/F载体尺寸

4.00

2.50

0.40

0.35

110x110

4.10

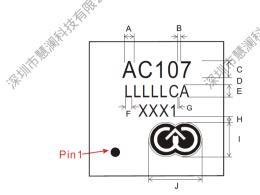
2.60

0.45

0.40



10.2 Marking Information



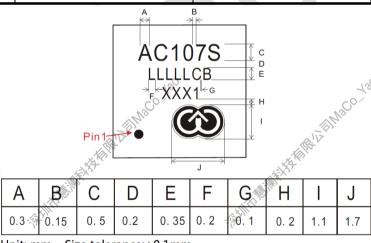
Α	В	С	D	Ε	F	G	Ι	1	J
0.25	0.06	0. 4	0.15	0.28	0. 15	0.06	0. 1	1.0	1.5

Unit: mm Size tolerance: ±0.1mm

Figure 10-3. AC107 Marking

Table 10-1. AC107 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1 1	AC107	Product name	Fixed
2	LLLLLCA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4	©	X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed



Unit: mm Size tolerance: ±0.1mm

Figure 10-4. AC107S Marking

Table 10-2. AC107S Marking Definitions

No.	No. Marking		Fixed/Dynamic
1	AC107S	Product name	Fixed
2	LLLLLCB	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4 60 188		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed



10.3 Carrier

Table 10-3. Reel Carrier Information

A STATE OF THE STA	Item	A TOWN	Color	Size
XIIII.	Reel	***	Blue	13 inches
Aluminum foil bags			Silvery white	440mm x 370mm x 0.15mm
Inside Box			White	336mm x 336mm x 48mm
	Outside Box		White	423mm x 358mm x 365mm

Direction of Feed -

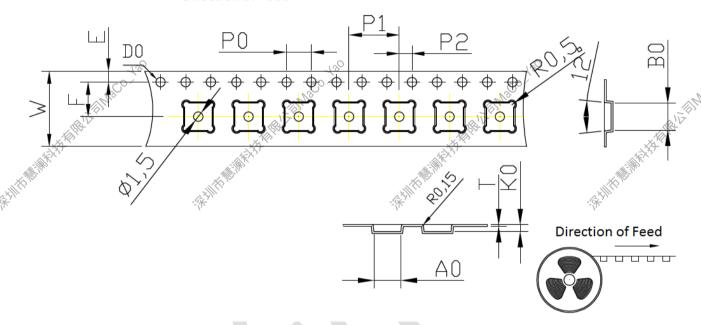


Figure 10-5. Tape Dimension Drawing

Table 10-4. Tape Dimension

Table 10-4. Tape Dimension						
Device	W(mm)	A0(mm)	B0(mm)	K0(mm)	P0(mm)	P1(mm)
AC107	12±0.30	3.30±0.1	3.30±0.1	1.10 +0.10	4.0±0.1	8.00±0.1
AC107S	12±0.30	4.30±0.1	4.30±0.1	1.10 +0.05 -0.00	4.0±0.1	8:00±0.1
Device	P2(mm)	F(mm)	E(mm)	D0(mm)	T(mm)	\$*************************************
AC107	2.0±0.1	5.5±0.1	1.75±0.1	1.5 +0.10	0.3±0.05	
AC107S	2.0±0.1	5.5±0.1	1.75±0.1	1.5 +0.10	0.3±0.05	

Table 10-5. Packing Quantity Information

Туре	Quantity	Part Number
Tape Reel	3000pcs	AC107
Tape Reel	3000pcs	AC107S



11 REFLOW PROFILE

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 11-1 shows the typical reflow profile of AC107 device sample.

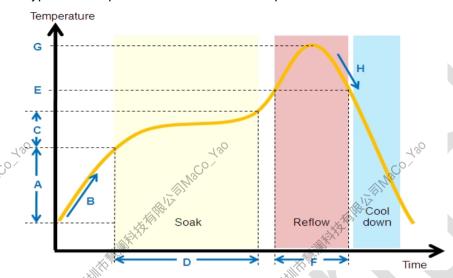


Figure 11-1 AC107 Typical Reflow Profile

Reflow profile conditions of AC107 device sample is given in Table 11-1.

Table 11-1 AC107 Reflow Profile Conditions

			_
	QTI typical SMT reflow profile	conditions (for reference only)	
	Step	Reflow condition	
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used	
Environment	If yes, O2 ppm level	O2 < 1500 ppm	
Α ,,,ο	Preheat ramp up temperature range	25°C,⁻> 150°C	1,00
B	Preheat ramp up rate	1.5~2.5 °C/sec	60
(C)	Soak temperature range	√150°C -> 190°C	- III Maco
D D	Soak time	80~110 sec	12
E	Liquidus temperature	217℃	
F	Time above liquidus	60-90 sec	
G	Peak temperature	240-250℃	
Н	Cool down temperature rate	≤4°C/sec 🏋	



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